

# Accelerated Spatially Resolved Electrical Simulation of Photovoltaic Devices Using Photovoltaic-Oriented Nodal Analysis

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**Abstract**—This paper presents photovoltaic-oriented nodal analysis (PVONA), a general and flexible tool for efficient spatially resolved simulations for photovoltaic (PV) cells and modules. This approach overcomes the major problem of the conventional Simulation Program with Integrated Circuit Emphasis-based approaches for solving circuit network models, which is the limited number of nodes that can be simulated due to memory and computing time requirements. PVONA integrates a specifically designed sparse data structure and a graphics processing unit-based parallel conjugate gradient algorithm into a PV-oriented iterative Newton–Raphson solver. This first avoids the complicated and time-consuming netlist parsing, second saves memory space, and third accelerates the simulation procedure. In the tests, PVONA generated the local current and voltage maps of a model with  $316 \times 316$  nodes with a thin-film PV cell in 15 s, i.e., using only 4.6% of the time required by the latest LTSpice package. The 2-D characterization is used as a case study and the potential application of PVONA toward quantitative analysis of electroluminescence are discussed.

**Index Terms**—Circuit simulation, nodal analysis, numerical simulation, parallel computing, photovoltaic (PV) cells.

## I. INTRODUCTION

PHOTOVOLTAIC (PV) cells are often simplified as a lumped diode model without spatial considerations. This is a simplification which is only valid for small cells in relatively low irradiances. This approximation is not valid, e.g., in the case of devices with very high currents (e.g., concentrator devices) or larger thin film devices with strong lateral resistance effects. The effect of this on the current–voltage ( $I$ – $V$ ) curve is demonstrated [1] when considering lateral resistances in a thin-film device using a 1-D distributed model. Moreover, the lumped model does not allow the representation of faults

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seen in a production environment. Methods of quality control currently are largely  $I$ – $V$  measurements, which show the effect of any production issue but not the issue itself. With the development of modern scanning and imaging characterization methods, e.g., laser-beam-induced current [2], electroluminescence (EL) [3], photoluminescence [4], and lock-in thermography [5], some manufacturers are moving to include spatial measurement techniques into their quality control. However, the commonly used luminescence imaging in industrial environments is often qualitative and thus does not realize the full potential of these measurements. This requires a tool that allows the modeling of the local electrical properties in a 2-D approach, with reasonable spatial resolution (e.g., equivalent to a mega-pixel image) in an industrially relevant speed. This paper will present such a simulation engine that can be used in computing intensive high-resolution simulations.

2-D modeling techniques take the spatial nature of devices into account and were mainly done by circuit simulation tools, e.g., Simulation Program with Integrated Circuit Emphasis (SPICE) derivatives. Galiana *et al.* [6] presented a model with detailed parameterization for concentrator PV cells and demonstrated its fidelity on depicting localized properties. Eidelloth *et al.* [7] proposed an elaborate model structure for wafer-based cells with metal contact grid. However, the case study of a  $400 \times 400$  nodes simulation requires a 5-GB memory space and 8 h for a single bias condition. Vorasayan *et al.* [8] and Ott *et al.* [9] simplified model structures were implemented, and simulations for mismatched thin-film modules were achieved. Pieters [10], [11] further introduced a variable meshing system to adjust the resolution and can describe complicated geometric patterns of the contact grid.

The 2-D approach for describing PV devices has been widely accepted and applied. Grabitz *et al.* [12] utilized a multidiode model to study how the overall performance of solar cells deteriorates with increasing inhomogeneities. Grote *et al.* [13] and Hinken *et al.* [14] investigated lateral variations in solar cells using SPICE-based approaches. Michl *et al.* [15] reviewed and analyzed series resistance measurement methods based on luminescence imaging techniques, and Bothe and Hinken [16] advanced this by implementing quantitative EL analysis using network modeling and simulations. Haase *et al.* [17] and Petermann *et al.* [18] employed 2-D models on loss analyses, respectively, which were also SPICE based.

However, the SPICE-based approaches require not only complicated preparation (e.g., generating and parsing net lists) but also significant memory consumption and long execution time increasing quadratically with node number, which rule them out for high-resolution simulations, e.g., a full-resolution EL image, in industrial environments. Recently, simulation approaches based on the finite-element method have been proposed [19] for 2-D modeling of PV cells with high computational speeds, based on an advanced meshing strategy. The meshing may reduce computational loads when carrying out simulations but does not link directly to the measurements taken, e.g., by a camera and needs to be adjusted in a case-by-case basis as it otherwise might lose information of defects in the wrong locations. Thus, it is complementary to SPICE-based modeling in generating understanding of the effects of faults, though SPICE may be better when it comes to creating tools for the analysis of imaging measurements.

A PV-oriented nodal analysis (PVONA) is presented in this paper that allows efficient 2-D simulations of PV cells and modules. This is achieved by integrating a specifically designed sparse data structure and a graphics processing unit (GPU)-based parallel conjugate gradient (CG) algorithm into a PV-oriented Newton–Raphson solver. Tests based on a normal PC with a consumer-level graphics card and achieved significant improvements than the conventional SPICE-based approaches, demonstrating the ability to simulate mega-pixel camera images (which is not possible in many SPICE derivatives due to memory allocation issues) and requiring about 5% of the time required by a SPICE version used for comparative purposes. The approach could be easily deployed on various high-power parallel computing platforms, which should allow deployment in industrial applications.

## II. SPATIALLY RESOLVED MODELING FOR PV CELLS

Spatially resolved modeling allows the investigation of the local electrical properties in a large-area device. The local characteristics of a PV cell can be described as a Poisson problem as given in [10]. However, analytically solving the continuous Poisson equation can be inefficient. Using circuit simulation to solve a discrete equivalent circuit model, i.e., a spatially resolved model (SRM), then becomes a commonly accepted alternative.

An SRM of a PV cell is composed by an array of finite areas, i.e., subcells, where each one is an analogue of a segment of the PV material. It makes the assumption that current through the solar cell is only in the vertical direction and thus the device can be broken down into virtual subcells or nodes that do not interact with each other except for resistances that represent the contacts and lateral currents [8]. As sketched in Fig. 1(a), each subcell (block with an arrow) represents a rectangular-shaped segment of the bulk, while the resistor network on the top represents the front contact scheme. Since the resistivity of the metal contact is low and can be assumed uniform, the back contact scheme is neglected in this paper, as done in [6] and [20]. The benefit of this simplification will be seen when constructing the nodal equation system (Section III-B). The front resistor network can be configured to suit both the contact grid for

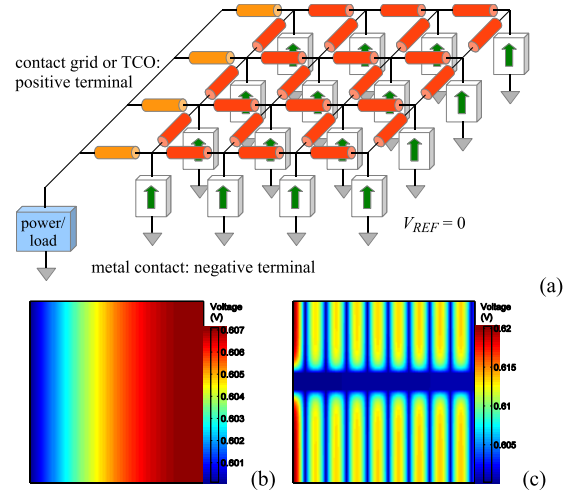


Fig. 1. (a) Schematic of the SRM structure of a PV cell. (b) and (c) Simulated voltage maps of a thin-film cell and a wafer-based cell operating under their maximum power points, respectively.

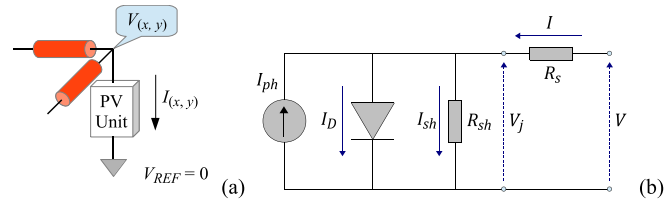


Fig. 2. (a) Schematic of a subcell. (b) Single-diode model used as the PV unit in a subcell.

TABLE I  
CALCULATION OF THE LOCALIZED ELECTRICAL PARAMETERS  
WITH RESPECT TO THE MESH SIZE

Photocurrent ( $I_{ph}$ )	$J_{ph}wl$
Dark saturation current ( $I_{sat}$ )	$J_{sat}wl$
Ideality factor ( $n$ )	$n$
Internal series resistance ( $R_s$ )	$\Gamma_s/wl$
Front sheet resistance ( $R_{\square}$ )	$\rho_{\square}w/ld$ or $\rho_{\square}l/wd$
Shunt resistance ( $R_{sh}$ )	$\Gamma_{sh}/wl$

wafer-based cells and the transparent conducting oxide sheet for thin-film devices, as demonstrated in Fig. 1(b) and (c), respectively.

A subcell is the elementary component of the SRM, as shown in Fig. 2(a). A subcell is composed by two lateral resistors for the front contact scheme and a PV unit. The PV unit is represented by a diode model that reflects the behavior of the semiconductor material used. In this paper, the single-diode model, as shown in Fig. 2(b), is used for demonstration purposes, while it can be easily replaced by double-diode model or Merten's model [21]. In this paper, only rectangular (square by default) meshes are used as this links to the pixel resolution delivered by EL cameras. The mesh size depends on the resolution of the model and remains invariable throughout each simulation. The local electrical parameters of each subcell are corrected with respect to their geometries [1], [6], as shown in Table I. Here,  $w$  and  $l$  are the width and length of a subcell, respectively;  $J_{ph}$  is the photocurrent density;  $J_{sat}$  is the diode dark saturation current density;  $n$  is the diode ideality factor;  $\Gamma_s$  is the internal series resistance corrected by the area;  $\Gamma_{sh}$  is the shunt resistance

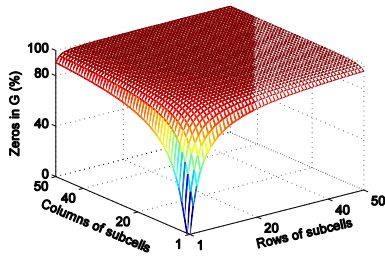


Fig. 3. 3-D chart shows the ratio of zero elements in the  $\mathbf{G}$  matrix as the size of the SRM increases.

corrected by the area; and  $\rho_{\square}$  and  $d$  are the resistivity and thickness of the front layer, respectively.

### III. SPARSE NODAL EQUATION SYSTEM

#### A. Nodal Equation System and Sparsity

Using nodal analysis or its derivatives is the most common way to solve a circuit network [22]. The complete nodal equation system (NES) of a model can be organized into a matrix–vector form as given in

$$\mathbf{G}\mathbf{V} = \mathbf{I} \quad (1)$$

where  $\mathbf{V}$  is the unknown vector of node voltages,  $\mathbf{G}$  is the admittance matrix, and  $\mathbf{I}$  is the current vector containing all the independent current sources. The target of nodal analysis is to solve the node voltages  $\mathbf{V}$ , through which all the local operating conditions in the circuit can be derived.

For the SRM of a PV cell, special features can be found in the NES. The admittance matrix  $\mathbf{G}$  represents the ohmic interconnections between adjacent nodes in the circuit as given in

$$G_{ij} = \begin{cases} \sum_{b=1}^N \frac{1}{R_{ib}}, & i = j \\ -\frac{1}{R_{ij}} = -\frac{1}{R_{ji}}, & i \neq j \end{cases} \quad (2)$$

where  $1 \leq i, j \leq N$  (the number of nodes),  $N$  is the total number of branches connected to the  $i$ th node, and  $R_{ij}$  represents the resistance between the  $i$ th and  $j$ th nodes. Therefore,  $\mathbf{G}$  is first symmetric and second highly sparse when the size of the model is large (for example, zero elements occupy 99.95% space in an SRM with a size  $100 \times 100$ , which increases with bigger sizes), as shown in Fig. 3. Moreover, the  $\mathbf{G}$  matrix is strictly diagonally dominant [23] by satisfying

$$|G_{ii}| > \sum_{k=1, k \neq i}^N |G_{ik}|, \quad 1 \leq i \leq N. \quad (3)$$

Being symmetric and strictly diagonally dominant,  $\mathbf{G}$  is guaranteed to be positive definite [24]. This special feature is not satisfied in most general circuit simulation scenarios (an SRM including the full back contact scheme only holds positive semidefinite) and enables efficient numerical solvers to be applied for solving (1).

#### B. Sparse PV-Oriented Data Structure

For an SRM consisting of  $R$  rows and  $C$  columns, the  $RC + 1$  nodes (one top node for each subcell plus one positive

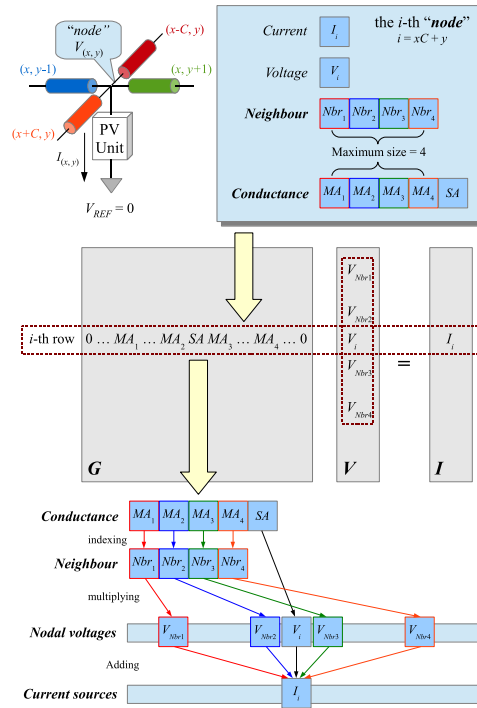


Fig. 4. Schematic of a node object in the SpNES data structure and its indexing mechanism in matrix–vector multiplications.

terminal node, while the negative terminal is set as the reference) produce a  $\mathbf{G}$  matrix of the size  $(RC + 1)^2$  in which only a very small amount of entries are nonzero. A sparse data structure for the NES (SpNES) is developed and shown in Fig. 4 (top).

The SpNES is built based on the *node* objects and records only the existing interconnections by two vectors, namely *neighbor* and *conductance*. For example, if the  $i$ th node is in connection with the  $j$ th node, then  $j$  is attached to *neighbor* as the index and the mutual admittance (MA) between the two is attached to *conductance* with the same sequence number. The self-admittance of the node itself is attached as the last element of *conductance*. Each *node* can replace a row of the NES (1), as shown in Fig. 4 (middle), where  $V_i$  is the node voltage to be solved and  $I_i$  is the local current. The use of SpNES not only significantly saves the memory space for large matrices originated from high-resolution simulations but also provides a seamless interface to the iterative computing processes.

### IV. NUMERICAL SOLVING PROCEDURE

The NES of the SRM is a nonlinear system. The most common approach to solve such a nonlinear system is to iteratively solve a sequence of linearized equations, for which the method of linearization is determined by the nonlinear root-finding algorithm. A solver based on dense matrices and a direct equation solving algorithms was shown to be ineffective for SRMs with a high number of nodes [25]. By integrating the SpNES and CG algorithm, the performance of a Newton-Raphson (NR) solver can be significantly improved for high-resolution simulations.

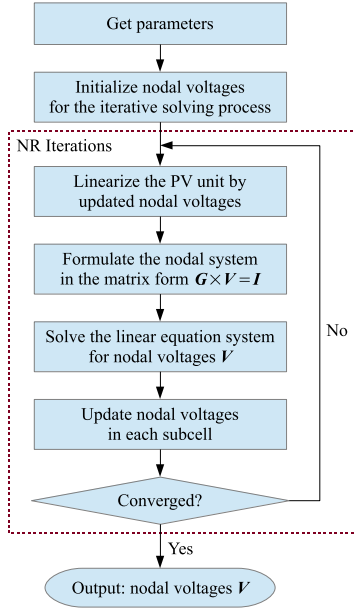


Fig. 5. Flowchart shows the Newton–Raphson loops to iteratively solve a nonlinear circuit network.

### A. Newton–Raphson Iterations and Linearization

Fig. 5 shows the steps of using NR to solve the SRM for one voltage-bias condition [25]. These steps repeat until the difference between the solutions from two successive iterative sequences meets the stopping criterion

$$\|V_k - V_{k-1}\|_2 < \varepsilon \|V_k\|_2 \quad (4)$$

where  $k$  represents the active iterative sequence. A small tolerance value e.g.,  $\varepsilon = 10^{-6}$  is set to evaluate the convergence. If the number of iterations exceeds the maximum limit and the stopping criterion is still not satisfied, which can be caused by diverging or low converging rate, the solving process will abort as a failure. However, PVONA has shown good stability for the simulations using typical parameters for PV devices.

The PV-oriented linearization in the NR loop distinguishes PVONA from general-purpose simulation tools. In standard linearization, each nonlinear component, e.g., a diode in the circuit is linearized individually [26]. In PVONA, however, the entire diode model [Fig. 2(b)] is treated as a single entity, as shown in Fig. 6. The tangent  $G_{eq}$  of the  $I$ – $V$  curve is calculated in each NR iterative sequence by the given operating voltage  $V_x$ . Only the values for  $V_x$ ,  $G_{eq}$  and  $I_{eq}$  need to be updated in each NR loop. The following shows the  $I$ – $V$  characteristic and the  $G_{eq}$  and  $I_{eq}$  derived from it:

$$I + I_{ph} - I_0 \left\{ \exp \left[ \frac{q(V - IR_s)}{nkT} \right] - 1 \right\} - \frac{V - IR_s}{R_{sh}} = 0 \quad (5)$$

$$G_{eq} = \left. \frac{dI}{dV} \right|_{V_x} = \frac{\frac{I_0 q}{nkT} \exp \left[ \frac{q(V - I_x R_s)}{nkT} \right] + \frac{1}{R_{sh}}}{1 + \frac{I_0 q R_s}{nkT} \exp \left[ \frac{q(V - I_x R_s)}{nkT} \right] + \frac{R_s}{R_{sh}}} \quad (6)$$

$$I_{eq} = I_x - G_{eq} V_x \quad (7)$$

where  $I_x$  is obtained by solving (6) with respect to  $V_x$  using an inner NR loop. As a consequence, the number of circuit

### Algorithm 1 Sequential and Parallelized CG Algorithm

```

1   $x^{(0)} \leftarrow 0$ 
2   $r^{(0)} \leftarrow b$ 
3   $p^{(0)} \leftarrow r^{(0)}$ 
4  for  $k \leftarrow 0$  to  $k_{max}$ 
5     $\alpha^{(k)} \leftarrow \langle r^{(k-1)}, r^{(k-1)} \rangle / \langle p^{(k-1)}, A p^{(k-1)} \rangle$ 
6     $x^{(k)} \leftarrow x^{(k-1)} + \alpha^{(k)} p^{(k-1)}$ 
7    if  $k$  is divisible by 10,000
8       $r^{(k)} \leftarrow b - A x^{(k-1)}$ 
9    else
10    $r^{(k)} \leftarrow r^{(k-1)} - \alpha^{(k)} A p^{(k-1)}$ 
11    $\beta^{(k)} \leftarrow \langle r^{(k)}, r^{(k)} \rangle / \langle r^{(k-1)}, r^{(k-1)} \rangle$ 
12    $p^{(k)} \leftarrow r^{(k)} + \beta^{(k)} p^{(k-1)}$ 
13   if the exit criterion is not satisfied
14      $k \leftarrow k + 1$ , continue the for-loop
15   else
16     break the for-loop and return  $x^{(k)}$ 

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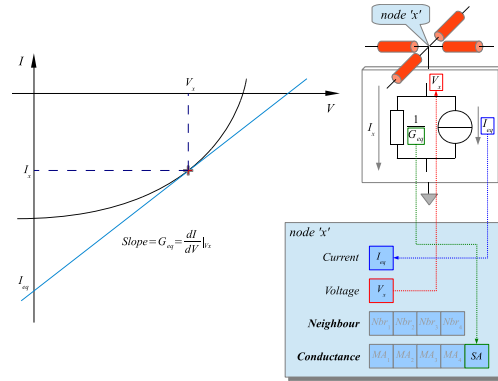


Fig. 6. Schematic of the PV-oriented linearization of a local PV unit and the parameters involved in the node object.

components of each single-diode model is reduced from 4 to 2, while the number of nodes is reduced from 2 to 1, which simplifies considerably the NES especially when the size of the SRM is large. The same rule can be applied on double-diode and Merten’s models [21].

### B. Parallelized Conjugate Gradient Algorithm

Solving the linearized NESs is the predominant factor that makes SRM simulation time consuming. In SPICE packages, direct, e.g., triangular (LU)-factorization-based solvers are normally used. Although such a direct analytical method has high numerical stability [27], the exponentially increasing time complexity with the increasing size of the SRM quickly becomes bottleneck for high-resolution images. Iterative methods can have lower time complexity and thus higher efficiency than direct ones. Being row independent [28], they are suitable to combine sparse matrix techniques.

For the symmetric positive definite SpNESs of the SRM, CG is introduced as the solving algorithm. The iterative steps of CG are shown in Algorithm 1. The use of the SpNES structure provides an efficient indexing system for matrix–vector multiplication [Fig. 4 (bottom)], in which

each MA element in conductance can locate its multiplier in  $V$  directly by the index stored in the corresponding position in neighbor, without extra indexing operations. The correlation

$$\|r_k\|_2 < \varepsilon \|r_{k-1}\|_2 \quad (8)$$

is used as the stopping criterion for the CG, where  $\varepsilon = 10^{-6}$ . The same analysis as done for the stopping criterion of the NR loops (5) can also apply. The *if-else* block from lines 7 to 10 introduces a regular round-off error removal process, in which the exact residual will be recalculated regularly to eliminate accumulated floating point error in the recursive formula [29].

Some computing-intensive applications for high-resolution SRMs, e.g., the  $I$ - $V$  calculation or the iterative local parameter fitting, require more efficient approaches to keep the accumulated computing time acceptable. This is especially important in time-critical situations, e.g., the quality control in a production line. Parallel computing is an appropriate candidate for accelerating a program with intensive matrix computations. It enables allocating independent row-wise computations to the equipment, which is able to run these smaller segments simultaneously and then to synchronize and reassemble them [30]. This can be employed cost-effectively using a GPU that can contain thousands of cores and is therefore efficient for simultaneously handling multiple small tasks for a PC-based solution. The compute unified device architecture (CUDA) is a GPU computing architecture proposed by Nvidia, enabling transfer of sequential code to parallel, i.e., heterogeneous programming [31].

The parallelism of CG is performed by offloading row-independent matrix arithmetic to a GPU, while the remainder still runs on the CPU. Each iterative sequence of CG involves a few inner products (Lines 5 and 11), matrix-vector multiplications (Lines 5, 8 and 10) and scaled vector additions (Lines 6, 8, 10 and 12), as marked in Algorithm 1. These row-independent operations can be manipulated by functions *dotc*, *multiply* and *axy*, respectively, using CUDA built-in libraries *cuSPARSE* and *cuBLAS* [32], [33]. In this paper, an open source library CUSP is chosen as it provides a parallelized CG solver *cusp::cg* that utilizes those built-in functions with adaptive thread dispatching [34]. The parallel CG is integrated into the NR loop for solving the linearized SpNESs while the other operations remaining sequential.

It will be demonstrated in the following sections that the use of these libraries together with the sparse nodal analysis delivers the speed up and capabilities to analyze high-resolution problems.

## V. PERFORMANCE EVALUATION AND DISCUSSION

To verify PVONA, the latest SPICE-based circuit simulator LTSpice v4.22 [35] is used as the reference. A desktop PC with an Intel Core i5 CPU (3.20 GHz) and 4-GB memory is used as the basic test platform. For the CUDA-based parallel computing, a consumer-level Nvidia GeForce GTX760 graphic card equipped with 1.03-GHz clock rate, 2-GB device memory, and 1152 computational cores is used.

TABLE II

LOCAL ELECTRICAL PARAMETERS FOR THE THIN-FILM PV CELL

$J_{ph}$	$1.35 \times 10^{-2}$ A/cm <sup>2</sup>
$J_{sat}$	$1.0 \times 10^{-10}$ A/cm <sup>2</sup>
$n$	2.0
$R_s$	$10.0 \Omega \cdot \text{cm}^2$
$R_{sh}$	$5.30 \times 10^5 \Omega \cdot \text{cm}^2$
$R_{\square}$	$8.0 \Omega/\square$

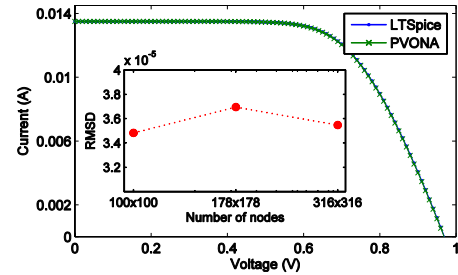


Fig. 7.  $I$ - $V$  curves of the  $100 \times 100$  model generated from LTSpice and PVONA. Inset: RMSD values of the  $I$ - $V$  curve pairs for the  $100 \times 100$ ,  $178 \times 178$ , and  $318 \times 318$  models.

Identical model structures with randomly selected electrical parameters and external bias conditions were set up and solved by both PVONA and LTSpice. The simulation of a thin-film PV cell is demonstrated here as an example. The size of the active area is  $1 \text{ cm} \times 1 \text{ cm}$  and the local electrical parameters are listed in Table II. The standard test conditions, i.e., irradiance  $1000 \text{ W/m}^2$  and temperature  $25 \text{ }^\circ\text{C}$ , were used to set the environmental parameters. Five test cases with 10000 ( $100 \times 100$ ), 31684 ( $178 \times 178$ ), 99856 ( $316 \times 316$ ), 315844 ( $562 \times 562$ ), and 1000000 ( $1000 \times 1000$ ) nodes were chosen.

Fig. 7 overlays the  $I$ - $V$  curves from both PVONA and LTSpice simulated between 0 and 1.0 V with 100 intervals, using a  $100 \times 100$  model. Visually they show perfect alignment. The maximum difference, approximately 1 mV, was found at the  $V_{OC}$  (0.963 V) area, giving only a 0.1% variation. This deviation is considered marginal in the context of the overall modeling accuracy and should be sufficient for all applications. The good agreement between  $I$  and  $V$  curves can be confirmed by calculating the root-mean-square deviation (RMSD) [36] values. The inset of Fig. 7 demonstrates the RMSDs between the  $I$  and  $V$  curve pairs of different node numbers. It clearly shows that the RMSDs remain in a low range, with an order of magnitude of  $10^{-5}$ . LTSpice failed for the  $562 \times 562$  and  $1000 \times 1000$  cases due to memory shortage. PVONA was able to handle these and produced results consistent with the lower resolution cases.

The good consistency implies that the accuracy and convergence are appropriately controlled in the three iterative loops (outer NR loop for solving the nonlinear network, inner NR loop for solving operating current in linearization, and CG algorithm for solving linearized SpNES) in PVONA. Double-precision floating point numbers were used, resulting in: 1) the reduction of total round-off error and 2) the lower possibility of numerical overflow. As to convergence, for CG, the symmetric positive definite  $G$  matrix guarantees the

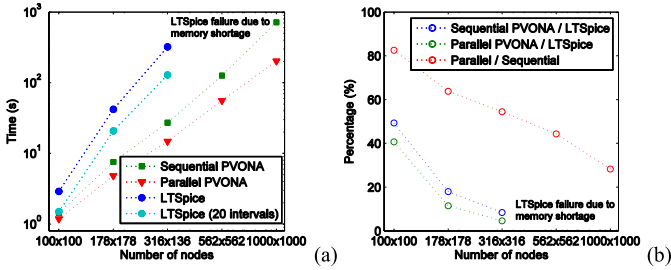


Fig. 8. (a) Averaged time for solving one voltage-bias condition by PVONA and LTSpice for a varying number of nodes. (b) Percentage of time consumption between PVONA and LTSpice for a different number of nodes.

convergence [23]. However, the convergence rate can depend on the features, e.g., the condition number [23] of the  $G$  matrix. For this reason, the application of preconditioned CG may provide further improvement to the solver. The performance of an NR solver may be affected by more complicated and subtle issues, e.g., oscillations, ill-suited initial values, and ill-conditioned NESs [26]. Nevertheless, PVONA has shown good stability for the simulations using typical parameters for PV devices and defects.

For each of the five listed test cases, the time for solving six voltage biases (0, 0.2, 0.4, 0.6, 0.8, and 1.0 V) were recorded and averaged. In terms of the computing speed, PVONA does not necessarily have advantages over LTSpice when the size of the model is relatively small, especially lower than  $50 \times 50$  nodes. For smaller sizes, the iterative CG algorithm may require more time than a direct method, e.g., LU factorization to solve linearized NESs [25], and the time for parsing a short netlist in SPICE is negligible. However, it is evident that PVONA is significantly faster as the size of the problem increases, as shown in Fig. 8. The sequential PVONA used 8.4% of the time required by LTSpice for the  $316 \times 316$  model. The improvement due to the parallelized CG is also noticeable, enabling another 54% faster than the sequential counterpart in this case, i.e., only 4.6% compared with LTSpice. It is noticeable that in LTSpice, since a large amount of time is consumed on the initialization, e.g., netlist parsing and system matrix generation stages, a high number of bias conditions in a single run may balance the cost for the initialization. For example, the average time needed from a 20-interval  $I$ - $V$  simulation is significantly shorter than that in the original five-interval cases, as shown in Fig. 8(a). However, it is still highly inefficient comparing with PVONA, especially for the simulation of a single bias, e.g., an EL image.

The implementation of the SpNES allows simulations for a higher number of nodes possible. The sequential and parallel PVONA managed to solve the  $1000 \times 1000$  model (equivalent to a mega-pixel image) within 12 and 3.4 min, respectively. Although the time consumption of a task can vary significantly depending on the features of the NES and thus the parameter values, the benefit of using PVONA is overwhelming. In addition, further parallelization may be implemented for PVONA. For example, the linearization processes can also be parallelized due to the fact that the linearization for each local diode model can be carried out independently.

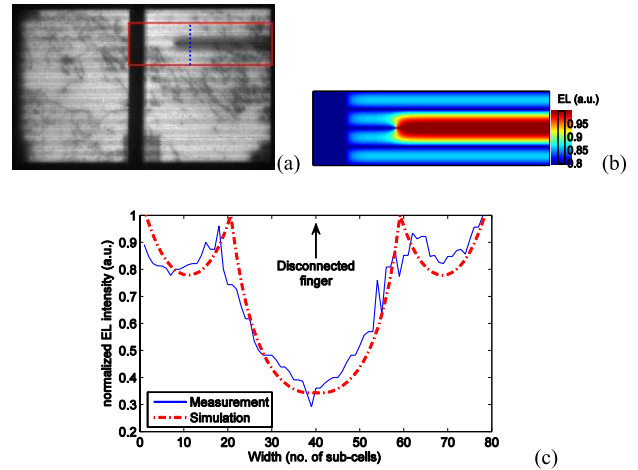


Fig. 9. (a) EL images show a partially disconnected finger in a c-Si cell. (b) Simulated EL image of the rectangle area marked in (a). (c) Comparison of the measured and simulated (normalized) EL profile of the line marked in (a).

However, extra efforts are needed to balance the overhead and latency effects for the data transfer between the main memory and the GPU memory [31]. For the same reason, using CUDA-supported data structure, e.g., matrices and vectors in the SpNES, may allow another level of improvement to PVONA.

## VI. POTENTIAL APPLICATIONS TOWARD 2-D PV CELL CHARACTERIZATION AND PARAMETER EXTRACTION

One of the aims of developing PVONA is the analysis and quantification of imaging techniques e.g., EL. In the following, this is demonstrated in two case studies. They demonstrate the initial steps toward 2-D analysis combining PVONA and the EL. Two EL images with notable defects are shown in Figs. 9(a) and 10(a) for a crystalline and a thin film device, respectively. These features are illustrated using a line scan, as the line-plot demonstrates the agreement between simulations and measurements better. It shows that by properly adjusting the local parameters, an excellent reproduction of all features seen in the given examples can be achieved, although there remains a missing calibration factor as well as an explanation of the jitter seen in the camera images. The simulation of an EL image is achieved by setting the illumination level to zero and reversing the direction of the current at the electrodes of the cell. The interpretation from the local operating points to EL intensities is done by the following equation [3] at the subcell level:

$$\Phi = C \exp\left(\frac{qV_j}{kT}\right) \quad (9)$$

where  $\Phi$  is the local EL intensity,  $C$  is the calibration factor, and  $V_j$  is the local junction voltage.

Fig. 9(a) shows the EL image (about  $230 \times 380$  pixels) of a multicrystalline Si PV cell taken under the current bias equals to its  $I_{SC}$  (0.914 A). The EL image clearly reveals a dark strip in the rectangle area marked, which is typically caused by an interruption in, or lack of contact of, the metal finger. This is because the disconnected finger cuts the current

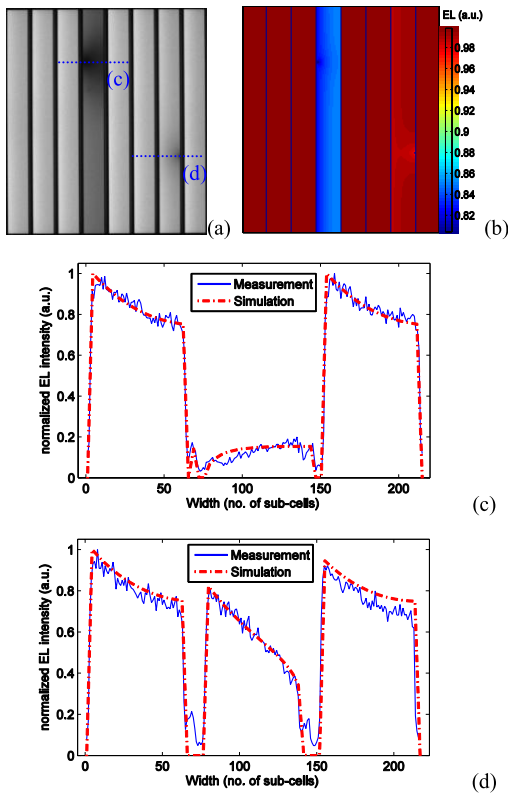


Fig. 10. (a) EL images show two local shunts in a thin-film a-Si mini-module. (b) Simulated EL image of the mini-module. (c) and (d) Comparison of the measured and simulated (normalized) EL profiles of the lines marked in (a).

pathway from the particular area to the metal contact grid and therefore the local current has to flow through a longer distance. As a consequence, the increasing voltage drop results in the lower local junction voltage, which is proportional to the EL intensity [37].

In the 2-D modeling, the rectangle area was reconstructed using the same resolution (a  $0.43 \text{ cm} \times 1.47 \text{ cm}$  area with  $65 \times 220$  nodes), with the initial parameters  $J_{\text{ph}} = 0.04 \text{ A/cm}^2$ ,  $J_{\text{sat}} = 5.0 \times 10^{-7} \text{ A/cm}^2$ ,  $R_s = 0.03 \Omega \cdot \text{cm}^2$ ,  $R_{\blacksquare} = 80.0 \Omega/\square$ ,  $R_{\text{sh}} = 8.35 \times 10^4 \Omega \cdot \text{cm}^2$ , and  $n = 1.12$ . These parameters were extracted from the  $I$ - $V$  curve of a reference cell of the same type using a hybrid fitting algorithm introduced in [38], while the  $R_{\blacksquare}$  is an empirical value [39]. The disconnection point was simulated by setting the resistance of the finger as  $R_{\blacksquare}$ .  $R_s$  and  $R_{\blacksquare}$  were gradually adjusted, stopped at  $R_s = 0.05 \Omega \cdot \text{cm}^2$  and  $R_{\blacksquare} = 65.0 \Omega/\square$ , so that the pattern of the simulated normalized EL profile in Fig. 9(b) agrees with the original. Furthermore, the line scan shown in Fig. 9(c) clearly demonstrates the agreement. It can be observed that the features are represented excellently, but there remains some room for improvement in showing smaller variations of the device across area, i.e., a single set of parameters does not fully represent the measured data. This now demonstrates the strength of PVONA as well, as the speed is high enough to develop an optimizer that will allow a better estimation of parameters.

The simulation can be extended to the module level by implementing a hierarchical architecture, as described in [25].

The  $I$ - $V$  curves of all the individual cells are generated by PVONA, and the characteristic of the module can be obtained by combining all these curves by interpolation. Fig. 10 shows the EL image of a thin-film a-Si mini-module taken under the current bias equal to its  $I_{\text{SC}}$  ( $0.034 \text{ A}$ ) and simulated global and line-scanned EL profiles. Two local shunts are found on the fourth and the seventh cells, respectively. The local parameters in Table I were used for the  $180 \times 20$  SRMs (resolution  $0.05 \text{ cm} \times 0.05 \text{ cm}$ ). For the stronger shunt in the fourth cell,  $R_s = 0.001 \Omega \cdot \text{cm}^2$  and  $R_{\text{sh}} = 0.001 \Omega \cdot \text{cm}^2$  were applied, and for the weaker shunt in the seventh cell,  $R_s$  and  $R_{\text{sh}}$  were set to  $0.01 \Omega \cdot \text{cm}^2$  and  $0.01 \Omega \cdot \text{cm}^2$ , respectively.

To move this to quantitative measurements, further work is required to qualify EL cameras better. The jitter seen in Fig. 10, for example, is most likely not due to production inhomogeneities but more to read out issues of the camera involved. Work to quantify these is currently ongoing. Thus, the next steps in this paper will be to optimize the localized parameters and to link measurement uncertainty to parameter extraction.

## VII. CONCLUSION

A PVONA is presented in this paper that enables significantly faster 2-D simulations of PV devices than SPICE-based tools. The use of the sparse CG algorithm and CUDA-based parallel computing techniques not only significantly saves the memory space but also accelerates the numerical solving procedure for high-resolution simulations. Further acceleration is possible by upgrading to a dedicated GPU and higher power CPUs. In the test, the accelerated PVONA managed to accurately solve a  $1000 \times 1000$  model, equivalent to the pixel number of a mega-pixel EL image, of a thin-film cell in only 3.4 min. The timing presented here depends obviously on the hardware involved. The equipment used was a reasonable PC with a high specification graphics card, but even this was not top of the range.

The presented method presents a step toward quantitative analysis as it allows simulations in reasonable times and reasonable computing expense for the potential iterative-based 2-D parameter determination algorithms. This will potentially allow a more quantitative assessment of EL images and similar tools. The speed presented should, with some further adaptations, allow the application in a production environment.

The quality of the model is validated against EL images with notable features. This demonstrates the need for further quantification of the analysis, which will be achieved by a localized optimization procedure and quantification of measurement uncertainties of EL images.

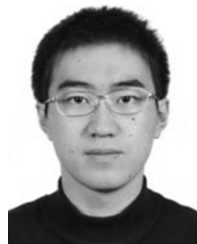
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