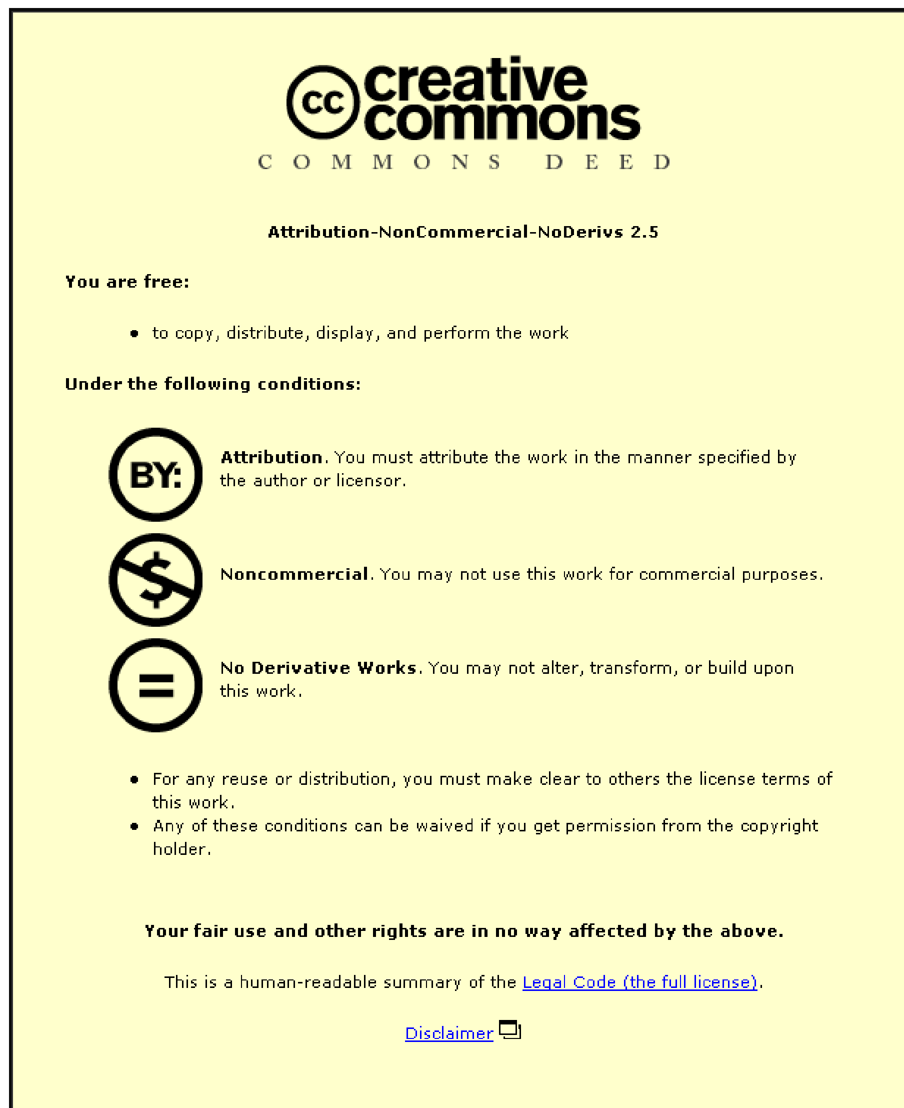
Loughborough University

This item was submitted to Loughborough University as a PhD thesis by the author and is made available in the Institutional Repository (https://dspace.lboro.ac.uk/) under the following Creative Commons Licence conditions.



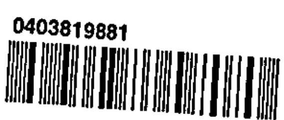
For the full text of this licence, please go to:
http://creativecommons.org/licenses/by-nc-nd/2.5/

University Library

Author/Filing Title HEGDE, P.

Class Mark T

Please note that fines are charged on ALL overdue items.



Mechanical Behaviour and Reliability of Sn3.8Ag0.7Cu Solder for a Surface Mount Assembly

By

Pradeep Hegde

A Doctoral Thesis

Submitted in Partial Fulfilment of the Requirements

for the Award of Doctor of Philosophy of

Loughborough University

Wolfson School of Mechanical and Manufacturing Engineering

December 2008

© By Pradeep Hegde, 2008

Loughborough University
Pilkington Library

Date 26/2/10

Class T

Acc No. 0403819881

Abstract

The demands for compact, light weight and low cost electronic products have resulted in the miniaturisation of solder interconnects to a sub-millimetre scale. With such a reduction in size, the solder joints cannot be assumed to behave in the same way as bulk solder in terms of reliability due to the fact that their material behaviours are influenced by the joint size and microstructure. The complexity of their reliability assessment is furthermore compounded by the demand for the replacement of traditional SnPb solder alloys with lead-free alloys, due to the presence of the toxic and health hazardous element (Pb) in the former alloy. However, these new lead-free alloys have much less history of industrial applications, and their material and reliability data is not as well developed as traditional lead-based alloys. In addition, most previous reliability assessments using finite element analysis have assumed a uniform distribution of temperature within the electronic assembly, which conflicts the actual temperature conditions during circuit operation. Therefore, this research was undertaken to analyse the effect of solder joint size on solder material properties from which material models were developed, and to determine the effect of an actual (non-uniform) temperature distribution in an electronic assembly on the reliability of its solder joints. Following a review of lead-free solders and potential lead-free alloys, lead-free solder microstructures, and the reliability issues and factors affecting the reliability of solder joints, the practical aspects of this research were carried out in two main parts.

The first part consisted of substantial work on the experimental determination of the temperature distribution in a typical surface mount chip resistor assembly for power cycling conditions, and the stress-strain and creep behaviour for both Sn3.8Ag0.7Cu solder joints and reflowed bulk solder. This also included building material models based on the experimental data for the solder joints tested and comparison with that for bulk solder. Based on the comparison of the material properties, two extreme material models were selected for the reliability study. Size and microstructure effects on the solder material properties were also discussed in this part.

The second part comprised of extensive finite element analysis of a surface mount chip resistor assembly and reliability assessment of its solder joints. The simulation began with elasto-plastic analysis for 2D and 3D chip resistor assemblies to decide upon the kind of formulation to be used when the full complexity of both plasticity and creep is considered. The simulation was carried out considering the determined non-uniform temperature distribution and idealized or traditional uniform temperature condition. The solder joint's material properties were modelled using the two material models determined from the experimental results. The effect of temperature distribution during thermal cycling and of the selected material models on the solder joint reliability was demonstrated using finite element analysis and subsequent fatigue life estimation.

In summary, this research has concluded that the material behaviour of the solder joint is different from that of bulk solder due to the effect of its size and microstructure. The anisotropic behaviour of the solder joint cannot be ignored in reliability studies, since it has a significant effect on the solder joint's fatigue life. The research also showed the significant effect of an actual (non-uniform) temperature distribution in the electronic assembly on the solder joint fatigue life.

Acknowledgements

I would like to express my sincere gratitude to my supervisors Mr. David C. Whalley and Prof. Vadim V. Silberschmidt, whose relentless support, effort and patience has been dependable source of insight and advice throughout my PhD study.

I would also like to acknowledge the Wolfson School of Mechanical and Manufacturing Engineering for the financial support during my research studies, and the technical and administration support staff, particularly Clive Turner, David Walters and Jo Mason.

My thanks also go out to the following people in Wolfson School for their kind support: Mr. Andy Sandaver, for sample preparation; Mr. John Jones and Mr. Bill Veitch, for guiding and operating machine tools; Mr. Jagpal Singh for providing help in metrology lab.

Thanks for the discussions, suggestions and help from both Mechanics of Advanced Material Group and Interconnection Group.

Finally, I would like to thank my family for all their love and support during my research.

Table of Contents

Abstract i

Acknowledgements iii

Table of Contents iv

Notations and Abbreviations viii

List of Figures xv

List of Tables xxiii

Chapter 1: Introduction 1

1.1 Electronic Packaging 1

1.2 Lead-Free Solder Alloys 4

1.2.1 Requirements of New Solder Alloys 6

1.2.2 Prospective Lead-Free Alloys 7

1.3 Research Objective 10

1.4 Thesis Structure 12

Chapter 2: Mechanical Behaviour of Metals and Alloys 14

2.1 Introduction 14

2.1.1 Stress and Strain in Materials 14

2.1.2 Stress-Strain Diagram 17

2.1.3 True Stress and True Strain 20

2.2 Time Independent Plasticity 22

2.2.1 Yield Criteria 23

2.2.2 Flow Curves 25

2.2.3 Strain Hardening Rules 26

2.3 Viscoplasticity and Creep 29

2.3.1 Viscoplasticity 30

2.3.2 Creep 33

2.4 Summary 39

Chapter 3: Microstructure of Lead-Free Solder 40

3.1 Introduction 40

3.2 Microstructure of Lead-Free Solder 40

3.2.1 Sn Dendrites and Grains 41

3.2.2 Ag_3Sn Plates 44

3.2.3 Cu-Sn Intermetallic Compounds and their Growth 45

3.3 Influence of Microstructure on Lead-Free Solder Mechanical Properties .48

3.3.1 Influence of Microstructure 48

3.3.2 Mechanical Influence of the Intermetallic Layer 51

3.4 Summary 53

Chapter 4: Solder Joint Reliability..54

4.1 Introduction 54

4.2 Solder Joint Failure 55

4.2.1 Thermal Fatigue Failure of Solder Joints 56

4.2.2 Creep and Thermo-Mechanical Fatigue in Solder Joint 58

4.3 Reliability Tests 59

4.4 Fatigue Life Prediction Models 61

4.5 Summary 63

Chapter 5: Temperature Distribution Study for a Surface Mount Chip Resistor Assembly 65

5.1 Introduction 65

5.1.1 Construction of 1206 Chip Resistors 66

5.1.2 Specimen Preparation 68

5.2 Experiment 70

5.2.1 Experimental Setup 70

5.2.2 Experimental Procedure 71

5.2.3 Results and Discussion 74

5.3 Finite Element Thermal Analysis 78

5.3.1 2-D Thermal Analysis 82

5.3.2 3D Thermal Analysis 89

5.4 Summary 93

Chapter 6: Stress-Strain Properties of Sn3.8Ag0.7Cu Solder 94

6.1 Introduction 94

6.2 Experimental Methodology 95

6.2.1 Experimental Setup 95

6.2.2 Measurement Technique 96

6.2.3 Determination of Required Sample Size 102

6.3 Tensile Test for Reflowed Bulk Solder 103

6.3.1 Specimen Fabrication and Mechanical Test 103

6.3.2 Tensile Test Methodology 106

6.3.3 Results and Discussion 107

6.4 Tensile Testing of Small-Scale Solder Joints 111

6.4.1 Specimen Preparation for the Tensile Tests 111

6.4.2 Results and Discussion 115

6.4.3 Parameter Determination for the Johnson-Cook Model 118

6.5 Comparative Study of Stress-Strain Properties 120

6.5.1 Effect of Size and Constraints 122

6.5.2 Microstructure Effect 130

6.6 Summary 140

Chapter 7: Creep Properties of Sn3.8Ag0.7Cu Solder 141

7.1 Introduction 141

7.2 Tensile Creep Test of Small-Scale Solder Joints 142

7.2.1 Creep Test Procedure 142

7.2.2 Result and Discussion 144

7.3 Shear Creep Testing of Small-Scale Solder Joints 151

7.3.1 Specimen Preparation 151

7.3.2 Creep Testing Method 152

7.3.3 Results and Discussion 156

7.4 Tensile Creep Testing of Bulk Solder 160

7.4.1 Specimen Preparation and Creep Test Methodology 160

7.4.2 Results and Discussion 161

7.5 Comparative Study of Creep Properties 165

7.6 Summary 170

Chapter 8: Creep Properties of Sn3.8Ag0.7Cu Solder 172

8.1 Introduction 172

8.2 Geometric and FE Modelling of the 1206 Chip Resistor Assembly 174

8.3 Elastic-Plastic Analysis 175

8.3.1 Boundary Conditions 176

8.3.2 Thermal History 178

8.3.3 Material Properties 182

8.3.4 Results and Discussion 184

8.4 Creep Analysis 192

8.4.1 Creep Material Properties 193

8.4.2 Creep Study for Power Dissipation Cycles at Room Temperature ...194

8.4.2.1 Thermal History 194

8.4.2.2 Results and Discussion 197

8.4.3 Creep Study for Constant Power Dissipation Cycles within a Varying Ambient Temperature 208

8.4.3.1 Thermal History 208

8.4.3.2 Results and Discussion 209

8.5 Summary 221

Chapter 9: Conclusions and Future Work 224

9.1 Future Work 227

References 228

Appendices

Appendix 1 Load Levels and Creep Constant Estimation 240

Appendix 2 Journal Paper

Finite Element Analysis of Lead-Free Surface Mount Devices 242

Appendix 3 Conference Paper

Creep Analysis of a Lead-free Surface Mount Device 251

Appendix 4 Journal Paper

3D Study of Thermal Stresses in Lead-Free Surface Mount Devices 258

Appendix 5 Conference Paper

Thermo-mechanical Damage Accumulation during Power Cycling of Lead-Free Surface Mount Solder Joints 275

Appendix 6 Journal Paper

Creep Damage Study at Powercycling of Lead-Free Surface Mount Device ..284

Notations and Abbreviations

Symbols	Meaning	Units
A	Normal area	mm^2
A^l	Inclined area	mm^2
A_i	Instantaneous area	mm^2
A_o	Initial area	mm^2
A_1	Constant	
A_2	Constant	
A_t	Temperature-dependent constant	
B	Constant	
B_1	Constant	
b	Time exponent	
C	Specific heat capacity	J/kg K
C_1	Constant	
C_2	Fatigue ductility constant	
C_3	Constant	
E	Young's modulus	MPa
E_c	Young's modulus of copper	MPa
E_p	Surface emissive power	W/m^2
E_r	Allowable error	
F	Function	
G	Shear modulus	MPa
g	Gap	
h	Height	mm
ΔH	Activation energy	eV
H_s	Height of solder joint	mm
I	Electrical current	Ampere
J_2	Second deviatoric stress invariant	
K	Bulk modulus, Stiffness	MPa, N/m
K_p	Stress	MPa
$[K]$	Thermal conductivity matrix	

k_o	Constant	
k, k_x, k_y	Thermal conductivity	W/m K
L	Length	mm
L_c	Length of copper	mm
L_i	Instantaneous length	mm
L_o	Initial length	mm
L_f	Final length	mm
m	Material constant	
N_f	Number of cycles to failure or fatigue life	
N_s	Sample size	
n	Hardening exponent, power law exponent	
n_1, n_2	Stress exponent	
P	Load	N
P_n	Normal load	N
P_t	Tangential load	N
P_c	Power dissipation	W
p	Sinh power law exponent	
Q, Q_1, Q_2	Activation energies	
Q_g	Heat generation	W/m^3
q, q_x, q_y	Heat flux	W/m^2
R	Gas constant	J/K mol
R_c	Resistance	Ohm
R_t	Triaxiality ratio	
r	Fatigue ductility exponent	
S	Size effect factor	
s	Material parameter	
T	Temperature	K
T_{op}	Operating temperature	K
T_m	Melting temperature	K
T_h	Homologous temperature	
T_{max}	Maximum temperature	K

T_{min}	Minimum temperature	K
T_o	Stress free state temperature	K
T_b	Temperature	K
t	Time, thickness	Second, mm
$\{T_\partial\}$	Temperature derivative	
u	Displacement	mm
U_O	Total strain energy	J
U_D	Distortional strain-energy	J
U_{DY}	Distortional strain-energy at yield	J
U_V	Strain-energy for volume change	J
V	Voltage	Volts
v	Displacement	mm
W	Width	Mm
w	Displacement	mm
$x^{\cdot}$	Kinematic hardening variable	
X_{imc}	Intermetallic layer thickness	μm
x,y,z	Cartesian coordinates	
X_x, X_y, X_z	Body force component	
α	Thermal expansion coefficient	/°C
β	Stress multiplier	
δ_t	Total displacement	mm
δ_m	Machine compliance displacement	mm
δ_c	Copper displacement	mm
δ_{ext}	Extensometer displacement	mm
δ_s	Solder displacement	mm
β_1	Thermal moduli	
$\varepsilon, \varepsilon_x, \varepsilon_y, \varepsilon_z$	Strain	
ε_T	True strain	
ε_E	Engineering strain	
ε_e	Elastic strain	

ε_p	Plastic strain	
$\Delta\varepsilon_p$	Plastic strain range	
$\dot{\varepsilon}_p$	Plastic strain rate	/s
ε_{ep}	Equivalent plastic strain	
$\dot{\varepsilon}^{*}_{ep}$	Dimensionless equivalent plastic strain rate	
ε_o	Initial strain	
$\dot{\varepsilon}_o$	Reference strain rate	/s
$\dot{\varepsilon}_s$	Secondary or steady state strain rate	/s
ε_{cr}	Creep strain	
ε_{in}	Inelastic strain	
ε_s	Emissivity of the surface	
$\gamma, \gamma_{xy}, \gamma_{yz}, \gamma_{zx}$	Shear strain	
$\Delta\gamma$	Shear strain range	
$\dot{\gamma}_s$	Steady state shear strain rate	/s
ν	Poisson's ratio	
λ	Lame's constant	
ϕ	Material constant	
ρ	Density	Kg/m^3
σ	Stress	MPa
$\sigma_{xx}, \sigma_{yy}, \sigma_{zz}$	Component stress	MPa
σ_T	True stress	MPa
σ_E	Engineering stress	MPa
σ_y	Yield stress	MPa
σ_u	Ultimate stress	MPa
$\sigma_1, \sigma_2, \sigma_3$	Principal stresses	MPa
σ_e	Equivalent or von Mises stress	MPa
σ_{yi}	Initial yield stress	MPa

σ_c	Stress coefficient	
σ'	Stress derivative	
σ_o	Material constant	
σ_{sb}	Stefan-Boltzmann constant	$W/m^2\ K^4$
σ_{sd}	Standard deviation	
σ_h	Hydrostatic stress	MPa
σ_n	Normal stress	MPa
σ_m	Volume average of equivalent stress	MPa
$\{\Delta\sigma_n^i\}$	Stress error vector	
$\{\sigma_n^a\}$	Averaged stress vector	
$\{\sigma_n^i\}$	Stress vector	
σ_j^{mnb}	Minimum stress magnitude	MPa
σ_j^{mxb}	Maximum stress magnitude	MPa
$\Delta\sigma_i$	Maximum absolute value $\{\Delta\sigma_n^i\}$	MPa
$\Delta\sigma_n$	Root mean square of $\Delta\sigma_i$	MPa
$\sigma_{j,n}^a$	Average stress	MPa
$\tau, \tau_{xy}, \tau_{yz}, \tau_{zx}$	Shear stress	MPa
θ	Angle	Degree
υ	Constant	

Abbreviations	**Meaning**
2D	Two Dimensional
3D	Three Dimensional
Ag	Silver
ASTM	American Society for Testing Material
BCT	Body-Centred Tetragonal
BERR	Business, Enterprise and Regulatory Reform
Bi	Bismuth

CC	Chip Carrier
CCC	Ceramic Chip Carrier
CPU	Central Processing Unit
CTE	Coefficient of Thermal Expansion
Cu	Copper
DfA	Design for Assembly
DfM	Design for Manufacturability
DfR	Design for Reliability
DfT	Design for Testability
DIP	Dual In-line Package
DTI	Department of Trade and Industry
EU	European Union
FC	Flip Chip
FE	Finite Element
FEA	Finite Element Analysis
FPA	Focal Plane Array
IBM	International Business Machine
In	Indium
I/O	Input/output
ICs	Integrated Circuits
IDEALS	Improved Design Life and Environmentally Aware Manufacturing of Electronics Assemblies by Lead-free Soldering
IMC	InterMetallic Compound
IR	Infrared
ITRI	International Tin Research Institute
IMCs	Intermetallic compounds
NEMI	National Electronics Manufacturing Initiative
OSP	Organic Solderability Preservative
Pb	Lead
PCB	Printed Circuit Board
PCs	Personal Computers
RoHS	Restriction of Hazardous Substance

Sb	Antimony
SEM	Scanning Electron Microscope
SMCs	Surface Mount Components
SMDs	Surface Mount Devices
SMT	Surface Mount Technology
Sn	Tin
SOIC	Small-Outline IC
TAB	Tap Automated Bonding
THT	Through Hole Technology
TMF	Thermo-Mechanical Fatigue
UTS	Ultimate Tensile Strength
WEEE	Waste from Electrical and Electronics Equipment
YS	Yield Stress
Zn	Zinc

List of Figures

Fig. 1-1	Different levels of electronic packaging	2
Fig. 1-2	Schematic of printed circuit board technologies: (a) SMT; (b) THT	4
Fig. 1-3	Thesis structure	13
Fig. 2-1	Cylindrical bar subjected to axial load	15
Fig. 2-2	Cylindrical bar with (a) load on an inclined plane; (b) shear strain	17
Fig. 2-3	Typical engineering stress-strain diagram for a tensile test	18
Fig. 2-4	Engineering stress-strain curve vs. a true stress-strain curve	21
Fig. 2-5	Isotropic hardening in which the yield surface expands with plastic deformation and the corresponding uniaxial stress-strain curve	27
Fig. 2-6	Reversed loading with isotropic hardening showing (a) the yield surface; (b) the resulting stress-strain curve	28
Fig. 2-7	Kinematic hardening showing: (a) the translation, 1x1 of the yield surface with plastic strain; (b) the resulting stress-strain curve with shifted yield surface in compression - the Bauschinger effect	29
Fig. 2-8	(a) The von Mises yield surface in plane stress for viscoplasticity with linear isotropic hardening and viscous (or over) stress; (b) the corresponding stress-strain curve	31
Fig. 2-9	Typical creep curve showing the three stages of creep	35
Fig. 2-10	Minimum (or steady state) creep rate vs. applied stress indicating changes in dominant mechanism	38
Fig. 3-1	Typical microstructure of Sn-Ag-Cu solders	42
Fig. 3-2	Isothermal sections of the Sn3.9Ag0.9Cu system at several temperatures	43
Fig. 3-3	Sn3.9Ag0.6Cu cooled at a rate of 1 K/sec from a temperature of 523 K: (a) bright-field image and (b) cross-polarised light image	44
Fig. 3-4	Optical micrographs (bright-field images) of cross sections of SnAgCu alloys of various Cu concentrations: (a) Sn3.9Ag; (b) Sn3.9Ag0.27Cu; (c) Sn3.9Ag0.59Cu; and (d) Sn3.9Ag0.86Cu	45
Fig. 3-5	Optical micrographs (bright-field image) of near-eutectic SnAgCu samples: (a) an ingot as cooled in the arc melter, (b) a sample cooled at	

a rate of 0.1K/s, and (c) a view of a larger region of the sample of (b) 47
Fig. 3-6 The interfacial IMC layer developed during 1,000 cycles for Sn3.5Ag joint 48
Fig. 3-7 The shear strengths of as reflowed and aged solder joints on OSP finished Cu pads 50
Fig. 3-8 Microstructure of (a) Eutectic SnAgCu; (b) hypoeutectic SnAgCu; (c) hypereutectic SnAgCu, on Cu pads with an OSP surface finish 50
Fig. 3-9 Typical profile used in reflow soldering 52
Fig. 3-10 Crack initiation and void formation due to thermo-mechanical fatigue 53
Fig. 4-1 Effect of thermal excursions on ceramic chip carrier solder joint (a) zero strain; (b) elevated temperature (T > To); and (c) reduced temperature (T < To) 58
Fig. 4-2 Typical temperature cycle during accelerated testing 60
Fig. 5-1 Construction of a typical chip resistor 67
Fig. 5-2 Dimensions of the chip resistor used in the experiment 68
Fig. 5-3 Derating curves for Panasonic chip resistors 68
Fig. 5-4 Components of the chip resistor assembly: (a) front view; (b) plan view; (c) actual cross section 69
Fig. 5-5 (a) The Thermosensorik infrared (IR) camera; (b) schematic of experimental setup 72
Fig. 5-6 (a) Locations used for temperature distribution study; (b) temperature distribution over chip resistor 75
Fig. 5-7 Comparison of temperature distribution over the chip resistor: (a) along line 1; (b) along line 2 76
Fig. 5-8 Temperature distribution on the substrate: (a) top right corner; (b) bottom left corner 77
Fig. 5-9 Locations used for temperature measurement comparison 78
Fig. 5-10 Heat flux through sides of a plane differential element 81
Fig. 5-11 Geometrical details of chip resistor assembly model: (a) side view; (b) front view 83
Fig. 5-12 2-D finite element mesh of the 1206 resistor assembly 84
Fig. 5-13 Thermal boundary condition zones 86

Fig. 5-14 Predicted full temperature distributions in the chip resistor for 0.25 W 87
Fig. 5-15 Comparison of predicted and experimental temperature distributions over chip resistor for 2D analysis 88
Fig. 5-16 Predicted temperature distributions at 0.15 W: (a) for an ambient temperature of 398 K; (b) for an ambient temperature of 218 K 89
Fig. 5-17 3-D finite element mesh for the 1206 resistor assembly 90
Fig. 5-18 Zones for thermal boundary conditions for 3-D thermal analysis: (a) side view; (b) top view 91
Fig. 5-19 Fig. 5-19: Predicted full 3-D temperature distribution (K) in chip resistor for 0.25 W 92
Fig. 5-20 Comparison of predicted and experimental temperature variation along line 1 over chip resistor for 3D analysis 92
Fig. 5-21 Comparison of predicted and experimental temperature variation along line 2 over chip resistor for 3D analysis 93
Fig. 6-1 Main components of Instron MicroTester 97
Fig. 6-2 Solder joint specimen details 98
Fig. 6-3 Load profile used for tensile test of copper 99
Fig. 6-4 Experimentally obtained stress-strain curve for C103 copper 100
Fig. 6-5 Measured Young's modulus for copper 101
Fig. 6-6 Planer T-TRACK reflow oven 104
Fig. 6-7 Temperature profile used to fabricate bulk solder specimen 105
Fig. 6-8 Fabrication of bulk specimen: (a) ground specimen after reflow; (b) final fabricated specimen; (c) actual specimen after final polish 106
Fig. 6-9 True stress-strain data for bulk reflowed solder at strain rates: (a) 0.00036 s^{-1}; (b) 0.0037 s^{-1}; (c) 0.0357 s^{-1} 109
Fig. 6-10 Fig. 6-10: Average stress-strain curves for bulk solder at different strain rates 110
Fig. 6-11 Effect of strain rate on Young's modulus of bulk solder 110
Fig. 6-12 Effect of strain rate on yield stress (YS) and ultimate tensile strength (UTS) of bulk solder 111
Fig. 6-13 Solder joint specimen fabrication: (a) dimensions of the copper pieces used; (b) an actual sample after reflow 112
Fig. 6-14 Buehler ISOMET low speed saw 113

Fig. 6-15 Specimen temperature profile used to fabricate the solder joints 114
Fig. 6-16 Preparation of solder joint specimen: (a) ground specimen after reflow; (b) final fabricated specimen; (c) actual specimen after final polish 114
Fig. 6-17 True stress-strain data for tensile tests on solder joints: (a) at a strain rate of 0.00075 s^{-1}; (b) at a strain rate of 0.004 s^{-1}; (c) at a strain rate of 0.013 s^{-1} 117
Fig. 6-18 Averaged true stress-strain curves for the three different strain rates 118
Fig. 6-19 Effect of strain rate on the UTS and YS 118
Fig. 6-20 Comparison of stress- plastic strain curve for a strain rate of 0.00075 s^{-1} 119
Fig. 6-21 Comparison of stress- plastic strain curves for strain rates of: (a) 0.004 s^{-1}; (b) 0.013 s^{-1} 120
Fig. 6-22 Comparison of average yield stress for solder joints and bulk solder 121
Fig. 6-23 Comparison of average UTS for solder joints and bulk solder 122
Fig. 6-24 Geometry of solder joint specimen and its octant used in full model analysis 123
Fig. 6-25 Full model, sub model and boundary conditions for the FEA 124
Fig. 6-26 Experimental and simulated stress-strain curves for the solder joint 124
Fig. 6-27 Meshes used in the FEA: (a) full model; (b) zoomed view of full model; (c) zoomed view for submodel 125
Fig. 6-28 Fig. 6-28: Equivalent stress distribution in the solder joint with a 1.5 mm gap length 126
Fig. 6-29 Distribution of equivalent stresses in the solder joint with a 0.15 mm gap length: (a) on the symmetry plane; (b) at the interface 126
Fig. 6-30 Size effect and triaxiality ratio as functions of gap length to thickness ratio 128
Fig. 6-31 Comparison of yield stress for solder joints (0.35 mm and 1.1 mm) and bulk solder for various strain rates 129
Fig. 6-32 Comparison of ultimate tensile strength for solder joints (0.35 mm and 1.1mm) and bulk solder for various strain rates 129

Fig. 6-33 Microstructure of small-scale solder joint: (a) inside solder joint; (b) at the interface between substrate and solder joint 132
Fig. 6-34 Microstructure of reflowed bulk solder 133
Fig. 6-35 Location used for microstructural study 134
Fig. 6-36 Fig. 6-36: Bright-field images of microstructure of strongest solder joint at location U1 135
Fig. 6-37 Bright-field images of microstructure of strongest solder joint at location U2 136
Fig. 6-38 Microstructure of weakest solder joint under polarised light: (a) general view; (b) and (c) grain boundary areas 137
Fig. 6-39 Microstructure of weakest solder joint under polarised light: (a) general view; (b) grain boundary; (c) microstructural features 138
Fig. 6-40 Microstructure of a solder joint in a chip resistor assembly: (a) general view; (b) zoomed view; (c) grain structure 139
Fig. 7-1 Tensile creep curves at 16.7 MPa 145
Fig. 7-2 Tensile creep curves at 26.7 MPa 145
Fig. 7-3 Microstructure of weakest solder joint specimen SC13 in 16.7 MPa test: (a) voids in the solder joint; (b) detailed view of selected location 146
Fig. 7-4 Microstructure of weakest solder joint specimen SC44 in 26.7 MPa test: (a) grains; (b) microstructure at the grain boundary 147
Fig. 7-5 Microstructure of strongest solder joint specimen SC43 in 26.7 MPa test: (a) grains; (b) microstructure at the grain boundary 148
Fig. 7-6 Calculation of the steady-state strain rate during secondary creep 149
Fig. 7-7 Comparison of experimental data and fitted hyperbolic sine law for steady-state strain rate for strongest and weakest joints tested 150
Fig. 7-8 Fabrication of lap solder joint: (a) copper specimen after formation of solder joint and grinding; (b) final shape of specimen; and (c) actual specimen after final polish 152
Fig. 7-9 Shear load application for the creep tests 153
Fig. 7-10 Geometric and boundary conditions used in FEA 153
Fig. 7-11 FEA model of creep specimens showing direction and orientation of UX displacement 154

Fig. 7-12 Variation of local shear strain field in the creep specimen: (a) along line 1; (b) along line 2 155
Fig. 5-13 Scatter of shear creep curves for stress levels: (a) 1.5 MPa; (b) 5.0 MPa 157
Fig. 7-14 Comparison of experimental and hyperbolic sine law creep data for the weakest and strongest solder joints 158
Fig. 7-15 Deformation of Sn-dendrites under shear loading 160
Fig. 7-16 Tensile creep results for bulk solder specimens at a stress of 5 MPa 162
Fig. 7-17 Comparison of experimental creep data for bulk solder with the fitted hyperbolic sine model for weakest and strongest joints 162
Fig. 7-18 Microstructure of the bulk solder specimen: (a) weakest (BC1); (b) strongest (BC2) 164
Fig. 7-19 Comparison of steady-state strain rates for the three type of creep tests for: (a) weakest specimens; (b) strongest specimens 168
Fig. 7-20 Comparison of steady-state strain rates with those of Pang *et al.* 169
Fig. 7-21 Comparison of steady-state strain rates for lap solder joints with published data 170
Fig. 8-1 Boundary condition details for: (a) 2D FE model; (b) 3D FE model 179
Fig. 8-2 Case A thermal history used in the elasto-plastic analysis 181
Fig. 8-3 Case B thermal history used in the elasto-plastic analysis 181
Fig. 8-4 Assumed multilayer chip resistor assembly 183
Fig. 8-5 Stress-strain curve used for the solder 184
Fig. 8-6 Total displacement magnitude plot for the assembly at the end of reflow (point Q in Fig. 8-2 and 8-3) 185
Fig. 8-7 Distribution of: (a) equivalent stress; (b) shear stress; (c) plastic equivalent strain; (d) plastic shear strain in 2D chip resistor assembly 186
Fig. 8-8 Evolution of: (a) shear stress; (b) total shear strain; (c) total shear strain on a bigger scale in the 2D chip resistor simulation 188
Fig. 8-9 Distribution of: (a) shear stress; and (b) plastic shear strain in the solder joint at point R of thermal history for 3D simulation 189

Fig. 8-10 (a) Comparison of shear stress; (b) total shear strain for the 2D and 3D chip resistor models 190

Fig. 8-11 Distribution of shear stress in the solder joint at the end of third load step (point R in Fig. 8-2 and 8-3) of thermal history for: (a) 2D model; (b) 3D model 191

Fig. 8-12 Thermal histories used for the creep simulation of power cycling at room temperature: (a) case A; (b) case B; (c) power dissipation 196

Fig 8-13 Distribution of: (a) equivalent; (b) shear thermal stress (MPa) in the solder joint at the end of reflow (point Q in Fig. 8-12) 198

Fig. 8-14 Evolution of shear stress in the solder joint for creep model 1 199

Fig. 8-15 Distribution of shear stress in the solder joint at the beginning of the first hot dwell: (a) Case A; (b) Case B 200

Fig. 8-16 Evolution of accumulated inelastic shear strain at the maximum stress location in the solder joint for creep model 1 202

Fig. 8-17 Distribution of: (a) equivalent; (b) shear thermal stress in the solder joint at the end of reflow (point Q in Fig. 8-12) 203

Fig. 8-18 Evolution of shear stress in the solder joint for power cycling at room temperature for creep model 2 204

Fig. 8-19 Evolution of inelastic strain in the solder joint for power dissipation at room temperature for creep model 2 205

Fig. 8-20 Thermal histories used for creep analyses for powered temperature cycling: (a) case C; (b) case D; (c) power dissipation 210

Fig. 8-21 Evolution of shear stress in the solder joint for creep model 2 over the entire simulation 212

Fig. 8-22 Predicted evolution of accumulated inelastic strain in the solder joint using creep model 1 for constant power dissipation within a varying ambient temperature 213

Fg. 8-23 Evolution of plastic and creep strain in the solder joint using creep model 1 for constant power dissipation within a varying ambient temperature: (a) Case C; (b) Case D 214

Fig. 8-24 Shear stress-strain hysteresis loop for thermal Case C using creep model 1 215

Fig. 8-25 Evolution of shear stress in the solder joint for creep model 2 over the entire simulation 217

Fig. 8-26 Shear stress-strain hysteresis loop for thermal case C using creep model 2 218

Fig. 8-27 Evolution of accumulated inelastic strain in the solder joint using creep model 2 for constant power dissipation within a varying ambient temperature 218

Fig. 8-28 Evolution of plastic and creep strain in the solder joint using creep model 2 for constant power dissipation within a varying ambient temperature: (a) Case C; (b) Case D 219

Fig. 8-29 Comparison of predicted fatigue life for creep model 1........ 222

Fig. 8-30 Comparison of predicted fatigue life for creep model 2........ 223

List of Tables

Table 1-1 Major groups of solders and some significant characteristics 9

Table 5-1 Specifications at different power rating 73

Table 5-2 Comparison of temperatures measured using thermocouples and thermal camera 78

Table 5-3 Material properties used in the thermal analysis 84

Table 5-4 Temperatures applied to the different zones in the 2-D thermal analysis 87

Table 5-5 Temperatures applied at the different zones in the 3-D thermal analysis 91

Table 6-1 Young's modulus measurement for C103 copper 101

Table 6-2 Johnson-Cook parameters for Sn3.8Ag0.7Cu solder 119

Table 6-3 Size and microstructure effect on solder material properties 130

Table 7-1 Parameters for hyperbolic sine constitutive equation for creep 150

Table 7-2 Parameters for hyperbolic sine constitutive equation for creep under shear load 158

Table 7-3 Fitted parameters for hyperbolic sine constitutive equation of creep for bulk solder 163

Table 7-4 Comparison of steady state strain rates at an equivalent stress of 15 MPa 169

Table 8-1 Elastic material properties used in analysis 184

Table 8-2 Hyperbolic sine creep model parameters used in the ANSYS simulations 194

Table 8-3 Details of the thermal history specified for the creep analysis 195

Table 8-4 Stress range in the solder joint with creep model 1 and power dissipation cycling at room temperature 199

Table 8-5 Predicted inelastic strain range in the solder joint for power dissipation at room temperature for creep model 1 201

Table 8-6 Predicted inelastic strain range in the solder joint for power dissipation at room temperature for creep model 2 205

Table 8-7 Predicted fatigue life of the solder joint with Case A thermal condition for power cycling at room temperature 207

Table 8-8 Predicted fatigue life of the solder joint with Case B thermal condition for power cycling at room temperature 207
Table 8-9 Details of thermal history used for constant power dissipation within varying ambient temperatures 211
Table 8-10 Predicted stress range in the solder joint using creep model 1 and constant power dissipation within a varying ambient temperature 213
Table 8-11 Predicted inelastic strain accumulation in the solder joint using creep model 1 for constant power dissipation within a varying ambient temperature 215
Table 8-12 Stress range in the solder joint with creep model 2 and constant power dissipation within a varying ambient temperature 217
Table 8-13 Predicted inelastic strain accumulation in the solder joint using creep model 2 for constant power dissipation within a varying ambient temperature 218
Table 8-14 Predicted fatigue life of the solder joint with Case C thermal condition for constant power dissipation within a varying ambient temperature 220
Table 8-15 Predicted fatigue life of the solder joint with Case D thermal condition for constant power dissipation within a varying ambient temperature 221

1. Introduction

This chapter presents an overview of the purpose and different levels of electronic packaging, the reasons new lead-free solder alloys are required, and, brief details of the prospective lead-free solders. With the continued demand for miniaturisation alongside the implementation of new lead-free solders, manufacturing of reliable products has been a major concern for the electronics industry. In addition the mechanical behaviour of small-scale solder joints is different from that of bulk solder. Therefore, to accurately predict the reliability of the solder joint, detailed knowledge of its operating conditions and mechanical behaviour is essential. This chapter also discusses the objectives of the research.

1.1 Electronic Packaging

Electronic packaging encompasses a range of technologies for protecting electronic components and providing electrical interconnections. At the heart of modern electronics are (mainly) silicon integrated circuits (ICs). These ICs are not isolated entities. They communicate with other chips in the circuit through an input/output (I/O) system of interconnects and the fragile chip and its embedded circuitry are dependent on the package for support and protection. The package serves three main purposes [1, 2]. First, to protect the components from the environment and from abusive handling, which may occur in manufacturing, and from mechanical loads and vibration that may occur in service. Second, it facilitates the interconnection of the circuits on the component, which in turn helps for heat dissipation from its top surface. Finally, it serves to facilitate the manufacturing process by providing a rugged housing that can be handled with automatic machinery. Therefore, one of the most critical levels of electronic packaging is that of packaging and interconnecting integrated circuits (ICs) and semiconductor devices.

There are several layers of interconnection/packaging within any electronic system. A hierarchy established by IBM [3] for their smaller computer system, which, in general, may be applied to any electronic system is shown in Fig 1-1. The hierarchy is as follows [1-3]:

(a) Individual component packaging – components are assembled to a package such as a chip carrier (CC), small-outline IC (SOIC), or dual-in-line package (DIP), and interconnected by wire bonding, tape automated bonding (TAB) or flip chip (FC) assembly techniques.

(b) The packaged components are assembled onto a printed circuit board (PCB) or to another type of substrate.

(c) Printed circuit boards are connected to a mother board to form a module. At this and subsequent stages connectors are usually separable, as opposed to the normally permanent connections at earlier stages.

(d) Subsystems are assembled to form modules.

(e) Subsystems are interconnected to give the final system configuration.

Some variation occurs between different systems, e.g. small systems may miss one or more of the intermediate levels.

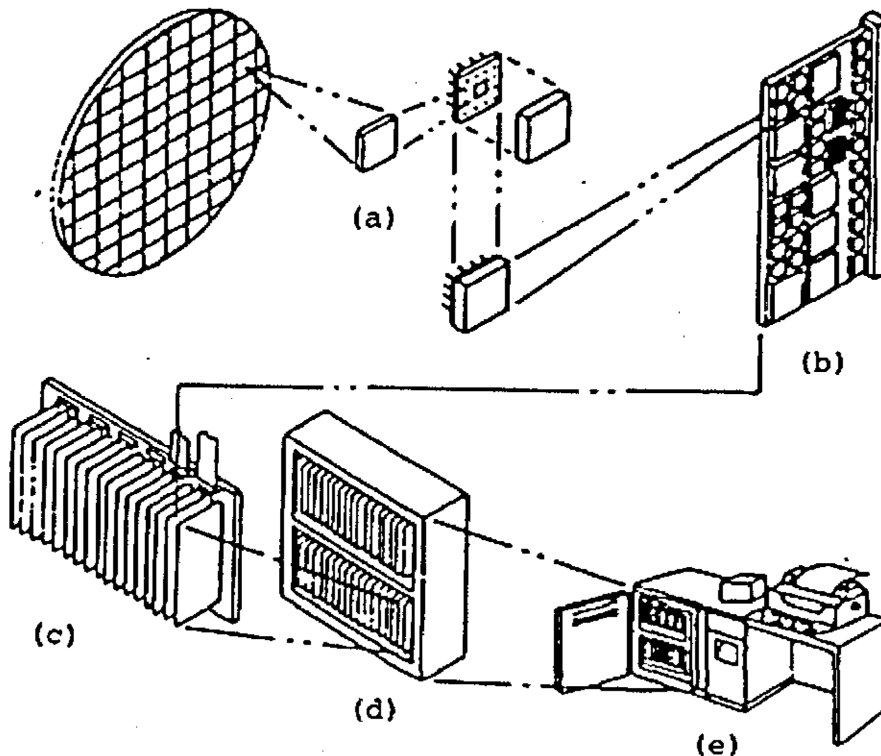


Fig. 1-1: Different levels of electronics packaging [3]

In electronic packaging, solder joints are very common interconnections in levels (a) and (b). These perform two very important functions by providing the required electrical connections and mechanical support to the package. With the continued demand for miniaturised and lightweight products, electronic industries are facing a challenge to meet these demands. Miniaturisation demands smaller, more compact and higher performance products at low cost. These objectives are accomplished by reducing the solder pad size and spacing on the chip [1]. This leads to an increased density of the packaging system. Some examples are videocameras and camcoders, electronic organisers, personal computers (PCs), laptops (notebook), mobile phones etc. In the process of miniaturisation, electronic production worldwide has been undergoing revolutionary changes in both components and manufacturing techniques. One new packaging technique that emerged as a result of miniaturisation was surface mount technology (SMT).

Surface Mount Technology (SMT)

Surface mount technology was a revolutionary change for the electronics industry. This technique emerged during the mid-1960s with the advantage of being able to place components on both sides of the hierarchy level (b) substrate. However, SMT did not become common for PCB assembly until about 15 years later. During the late 1970s, the conventional through hole technology (THT) ran into increasing difficulty in meeting the constant need for smaller, higher performance, less expensive and more reliable electronic assemblies [4, 5]. The conventional method required the drilling of hole in the substrate for every component lead, because of the universal 2.54 mm (0.1 inch) interconnection grid in use, and because of the entrenched position of the ubiquitous plastic dual-in-line package for almost all integrated circuits. Figure 1-2 (a) and (b) show the SMT and THT connections respectively to the PCB [5], and thereby explain the differences between them. It required a sweeping change of thought to make the move to surface mount components (SMCs) on boards rather than through hole mount them because, with this seemingly small change, have also come changes in component packaging shapes and sizes, changes to fully automated component handling, new component attachment methods using screen printed solder pastes, innovative changes in board design algorithms, and changes in the requirements of post assembly cleaning, testing and inspection.

SMT can meet three important industrial demands i.e. reduced size, reduced cost and increased performance. Adopting this packaging technology can result in 40 % and 50% reduction in assembly size and cost, respectively [4]. The electrical performance of a surface mounted assembly is superior to that of a conventional assembly, particularly at high frequencies, and, despite early concerns, the reliability has proved to be at least as good [4, 5]. The technology is applicable to all applications such as aerospace, high reliability, industrial, commercial or consumer. Today most common components used in applications, such as capacitors, resistors, transistors, diodes, inductors, ICs, and connectors are available as SMCs. Even though this packaging technique meets most of the industrial needs, like all packaging techniques, it has some disadvantages. The manufacturing processes for SMT are much more sophisticated than through-hole boards, raising the initial cost and time of setting up for production. Manual handling of surface mount devices (SMDs) become difficult, due to their very small sizes and lead spacings, making component-level repair of devices or manual prototype assembly extremely difficult, and often uneconomical.

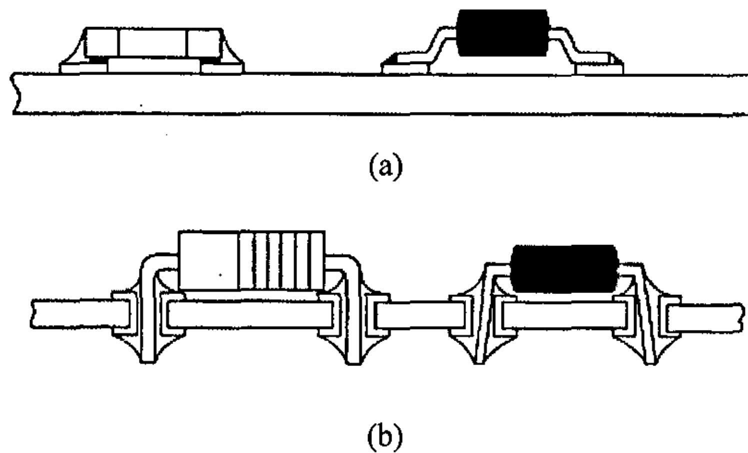


Fig. 1-2: Schematic of printed circuit board technologies: (a) SMT; (b) THT [5]

1.2 Lead-Free Solder Alloys

The advent of industrialization in the 1900s resulted in an unprecedented revolution in manufacturing technology. These new technologies led to rapid growth of the economy in many countries. Numerous inventions took place in this short span of time; and the development of electronic products was one of them. Electronic products have come to dominate human life, and become part and parcel of it with the invention of radio, television, telephones, mobile phones, computers, etc.

Industrialization has also led to related effects on lives and the environment. Lead (Pb) has been widely used as one of the constituents of interconnection materials in electronic products. However, it is well known that lead (Pb) is hazardous to health and the environmental due to its toxic nature [6, 7]. This toxic and health hazardous element has been found to result in numerous diseases such as reduced intelligence in children, kidney, liver and brain damage, and impaired memory. Such diseases occur due to lead levels in the blood of more than 0.25 mg/l [6, 8, 9]. Human beings are prone to these diseases when they live or work in such a toxic and health hazardous environment.

The correct waste management of lead containing products is one of the main concerns for avoiding lead being discharged to the environment. It can be argued that the amount of lead used in electronic products was less than 0.49 % of the total lead consumption [6, 9]. However, due to the faster growing waste from the electronic industry it became a major concern for the environment and health. Another concern is that employees working within the industry were constantly exposed to higher level of lead and, there is a worry that lead could be carried home on his/her clothing, which leading to contamination in the home [10]. There are different forms in which Pb containing waste is generated by the electronic industry:

- Waste solder
- Solder dross
- Used wipes
- Empty packaging containers

Some wastes can be recycled and some have to be disposed as hazardous. However, in general electronic manufacturing sites are clean and safe environments in which to work, but governments across the world have targeted the removal of lead from electronic products due to pollutants generated by the electronic industry as well as other industries. A great number of lead containing products such as radios, televisions, telephones and other electronic products are being disposed of in landfills. All modern landfills have leachate treatment systems, but these can be overloaded or treatment systems can malfunction. Hence, Pb from these products can leach into the

environment as a hazardous material [9]. Therefore, the European Union implemented legislation called the Restriction of Hazardous Substances in electrical and electronics equipment (RoHS) directive, which, for the majority of applications, prohibits the manufacturing or import of lead-containing electronic or electrical components by its member countries. The European Union also introduced the Waste from Electrical and Electronics Equipment (WEEE) directive to improve the disposal of waste electronic and electrical products. Similarly, in Asia, Japan has voluntarily removed lead from all electronic and electrical products.

Since electronic products are a significant source of environmental pollution, there has been a strong drive to remove lead from them. Solder joints are common features in most electronic products and are the main use of lead in most electronic products. Traditionally most solder joints were created using the well established tin-lead (SnPb) family of solder alloys, the most common of which are near-eutectic 60Sn40Pb and eutectic 63Sn37Pb. Therefore, many researchers are studying the possibility of replacing the eutectic/near-eutectic SnPb solder alloys with a lead-free solder alloy. Furthermore, the new solder materials must meet the requirements of a good solder alloy. This has motivated researchers to undertake extensive research on new solder materials and to test them in the field before industrial implementation.

1.2.1 Requirements of New Solder Alloys

Electronic and electrical products and components are considered to be lead-free if they are assembled without any intentional use of lead as a raw material or in the manufacturing process. But lead may exist as an impurity. According to the National Electronics Manufacturing Initiative (NEMI) definition, the amount of lead in solder joints should be less than 0.2 % [6]. Tin-lead solder alloys have been used widely across the electronic and electrical industries. This alloy is of low cost, and satisfies the requirements of a good solder alloy [7, 11]. It has a long history of application in electronic packaging, as well as proven temperature-dependent material data and reliability models. Any next-generation lead-free solders, which replace tin-lead solder alloys, should satisfy the same requirements in a practical and economic way. Also, temperature-dependent material data and reliability models have to be developed. The

following are requirements any new solder alloy should meet considering the existing tin-lead solder alloy as a baseline [6, 8]:

1. Low melting temperature
2. Comparable cost
3. Small pasty range (small difference between liquidus and solidus temperatures)
4. Good wetting and wetting speed
5. Acceptable physical properties: density, coefficient of thermal expansion (CTE), and electrical and thermal conductivity
6. Good mechanical properties (strength and ductility)
7. Good reliability and fatigue performance
8. Low toxicity
9. Compatibility with the fabrication needs for various solder forms
10. Acceptable impact and shock performance
11. High process yields with existing processing equipments

1.2.2 Prospective Lead-Free Alloys

The search for new lead-free alloys started due to the proposed bans on the use of lead in electronic products, as well as some companies wishing to voluntarily remove such health hazardous substances to allow marketing of products as environmentally friendly. Many new solder alloys are tin rich, with a variety of other elements added to enhance various characteristics [12, 13]. The most basic solders are binary alloys that have been used for years in electronic applications. Tin-lead has been a suitable standard alloy for many years simply because it meets most of the requirements of electronic assembly [8, 14]. However, with an urgent need for controlled recycling and reduction of hazardous waste related to finished products, the greater use of lead-free solders has lead to the discovery of some of their noteworthy characteristics. For example, high joint strength, better fatigue resistance, improved high temperature life and harder solder joints are among the features seen in some of the newer materials [12, 15]. Nevertheless, it is important to remember that these benefits are very much dependent on the specific alloy and its intended applications, and each alloy should be thoroughly investigated before implementation into production.

Ever since the commencement of research and development of lead-free solders, a large number of solder alloys have been proposed. Table 1 gives options for various lead-free solders as well as their composition, melting point, and notable characteristics. Prospective lead-free solders are generally benchmarked against conventional tin-lead solder. It is evident from various lead-free compositions that most of the lead-free alloys are tin (Sn) rich, typically containing more than 90 % of Sn with alloying elements such as bismuth (Bi), indium (In), silver (Ag), copper (Cu), zinc (Zn) and antimony (Sb). This suggests that the physical, chemical, and mechanical properties of the proposed lead-free solders will be heavily influenced by the properties of pure Sn, in contrast to tin-lead eutectic, which comprises a mixture of Sn-rich and Pb-rich phases.

From the review of prospective lead-free solders, most of them melt at a temperature higher than that of SnPb which has eutectic melting point of 183 ^{o}C. The exceptions are alloys containing indium or bismuth, which tend to significantly lower the melting temperature. The main problem with indium is its cost, with prices in the area of €125/kg, which is about 23 time higher than that of Sn [9]. As for bismuth-based lead-free alloys, a lower melting temperature (138 ^{o}C) than that of SnPb is obtainable together with a cost similar to that of Sn. Unfortunately, bismuth in soldering alloys tends to cause embrittlement, and if a bismuth-based alloy picks up any lead, a ternary eutectic of SnBiPb is formed with an even lower melting temperature of 95 ^{o}C. This is considered a manufacturing and reliability issue [6, 16]. Zinc based solders are cost effective, but they are prone to oxidation and corrosion [16]. These limitations leave SnCu, SnAg and SnAgCu solders as prime candidates for the transition to lead-free. Even though SnCu solder is lowest in cost amongst these three and is high temperature resistant, it has a lower tensile strength than eutectic SnPb. Better creep and tensile behaviour can be achieved by addition of Ag to SnCu [9, 16]. In the case of SnAg, when soldering to copper terminations/substrates, the increased dissolution of copper in the SnAg binary alloy affects the solder joint microstructure, and therefore the mechanical properties. This can be decreased by addition of low levels of copper in to the SnAg solder alloy. Therefore, SnAgCu alloys have become mainstream lead-free alloys for electronic assembly. NEMI, the International Tin Research Institute (ITRI) and the former UK Department of Trade and Industry (DTI is now BERR) have recommended these alloys [6, 9]. In Europe, the EU funded IDEALS consortium has

recommended Sn3.8Ag0.7Cu as the best lead-free alloy based on the results of temperature cycling testing from 253 K to 398 K for up to three thousand cycles and power cycling from 298 K to 383 K for five thousand cycles [6]. However, knowledge of the performance of this alloy is still considerably less than that of traditional SnPb solders, and it needs to be investigated thoroughly for its reliability within various applications and operating conditions before implementation.

Table 1-1: Major groups of solders and some significant characteristics [6, 9, 16, 17]

Alloy group	Typical alloy composition	Melting temperature (T_m, °C)	Characteristics
SnPb	Sn37Pb Sn37Pb2Ag	183 179	High ductility
SnBi	Sn58Bi	138	Low melting point, sensitive to Pb contamination, brittle
SnZn	Sn8Zn3Bi Sn9Zn	195 199	Low cost, Zn oxidation and corrosion problem
SnAgBi	Sn3.5Ag6Bi Sn3.5Ag3BI Sn2.8Ag1Bi Sn2.0Ag3Bi	206 210 215 220	Good tensile strength, sensitive to Pb contamination
SnAg	Sn3.5Ag	221	Good fatigue properties, Cu dissolution from substrate affect the solder joint properties
SnAgCu	Sn3.8Ag0.7Cu	217	Improved fatigue properties, reduced Cu dissolution from substrate, mainstream lead-free alloy
SnCu	Sn0.7Cu	227	Common low cost alternative for wave soldering
SnIn	Sn51In	120	Low melting point, poor fatigue properties, expensive
SnSb	Sn5Sb	236-243	Poor wetting and toxic

1.3 Research Objective

Due to the miniaturisation of electronic products, new packaging technologies such as surface mount packaging were invented. Although, surface mount technology brought in many advantages such as high performance, lower cost, and more compact products, this technology also resulted in a new reliability threat to the integrity of the products. For example the components such as chip resistors and capacitors are mounted onto PCBs through small leadless solder joints. In such a situation, only the solder joint, which is the interconnecting element between the component and substrate, can accommodate any differential movement between the component and substrate. This differential displacement is primarily due to mismatches in the thermal expansion between them under cyclic variations of thermal loading. Even if the component and substrate are made of similar CTE materials, under power cycling thermal conditions, the temperature difference between the component and substrate introduces differential movement between them. This differential movement results in inelastic strain in the solder joint. Thus, this thermally excited inelastic deformation of the solder joints ultimately results in their low cycle fatigue.

Although this issue has been recognised for about 40 years [5], the issue of reliability in surface mount components needs to be investigated due to the introduction of lead-free solders in the electronic industries. These solders neither have much history of application in the industry nor does sufficient material properties data exist for reliability predictions to be made with confidence. As mentioned earlier SnAgCu is the most common alloy being used to replace SnPb, due to its better chemical, physical and mechanical properties compared with traditional Sn-Pb alloys. The exact composition of the SnAgCu alloy used varies, however in Europe 95.5Sn3.8Ag0.7Cu is considered the best composition [6, 9, 18]. With such a high level of Sn in the solder alloy, its material properties are mainly influenced by the Sn. Generally the SnAgCu solder joint microstructure consists of Sn-grains, Sn dendrites and β-Sn matrix. Since Sn has a body centre tetragonal (BCT) structure, the solder joints are expected to show considerable anisotropic behaviour [19]. Thus the number of Sn-grains and their orientation play an important role in the mechanical behaviour of the solder joint. Miniaturisation also results in smaller solder joints. In some applications solder joint dimensions could be less than 100 μm. This reduced size also influences the

mechanical behaviour of the solder joint. Thus, it is important to understand the mechanical behaviour of Sn3.8Ag0.7Cu solder joints that are of a size commensurate with the real application and manufactured using processes resembling typical fabrication conditions.

Reliability testing of solder joints is time consuming and expensive. Therefore, finite element analysis (FEA) has been used quite frequently as an alternative, with which any geometry and operating conditions can be modelled [20]. However, the temperature distribution in the electronic assembly has been generally idealised as uniform in such modelling. This idealisation is unlike the actual thermal conditions typically occuring in the assembly. Hence, this research has initially used experimental approaches to study both the mechanical behaviour of small-scale Sn3.8Ag0.7Cu solder joints, and the temperature distribution in an actual surface mount assembly when powered. These findings are then combined in a study of the reliability of the lead-free solder joints in a real application.

Thus, the research novelties addressed in this thesis are:

- Contributions of microstructure and size effect on the increased mechanical behaviour of lead-free solder joint over bulk solder.
- The effect of a non-uniform temperature distribution on the temperature cycling reliability of lead-free solder joints.

The thesis also addressed couple of other research issues while achieving the research novelties. They are:

- Effects of tensile and shear loading on the visco-plastic behaviour of lead-free solder joints.
- The influence of material properties on the solder joint reliability using sensitivity studies.

1.4 Thesis Structure

Figure 1-3 shows the structure of the thesis, which is broken into four different sections: research background and literature review, experimental research, finite element simulation of a real problem, and conclusions from the drawn research.

The research background and literature review encompasses chapters one to four. Chapter 1 presents some background information about electronic packaging and the requirements for lead-free solders. This chapter also lays out the research issues addressed in the thesis. Chapter 2 discusses the general mechanical behaviour of metals and alloys. The microstructural effects on the mechanical behaviour of the solder joints are reviewed in chapter 3. Finally, chapter 4 discusses the reliability aspects of solder joints in electronic products.

The experimental research encompasses three chapters, and highlights important findings. Chapter 5 deals with determination of the temperature distribution in a surface mount chip resistor assembly during power cycling. The determined stress-strain and creep properties of solder joints and their comparison with those of bulk solder are discussed in chapters 6 and 7, respectively.

Finite element simulation of a real problem consists of only one chapter, chapter 8. In this chapter the reliability of the lead-free solder joints of a surface mount chip resistor is simulated using outcomes from the experimental research.

The final section within the thesis contains a single conclusions chapter, which discusses the final conclusions of this research and also highlights potential areas of further work.

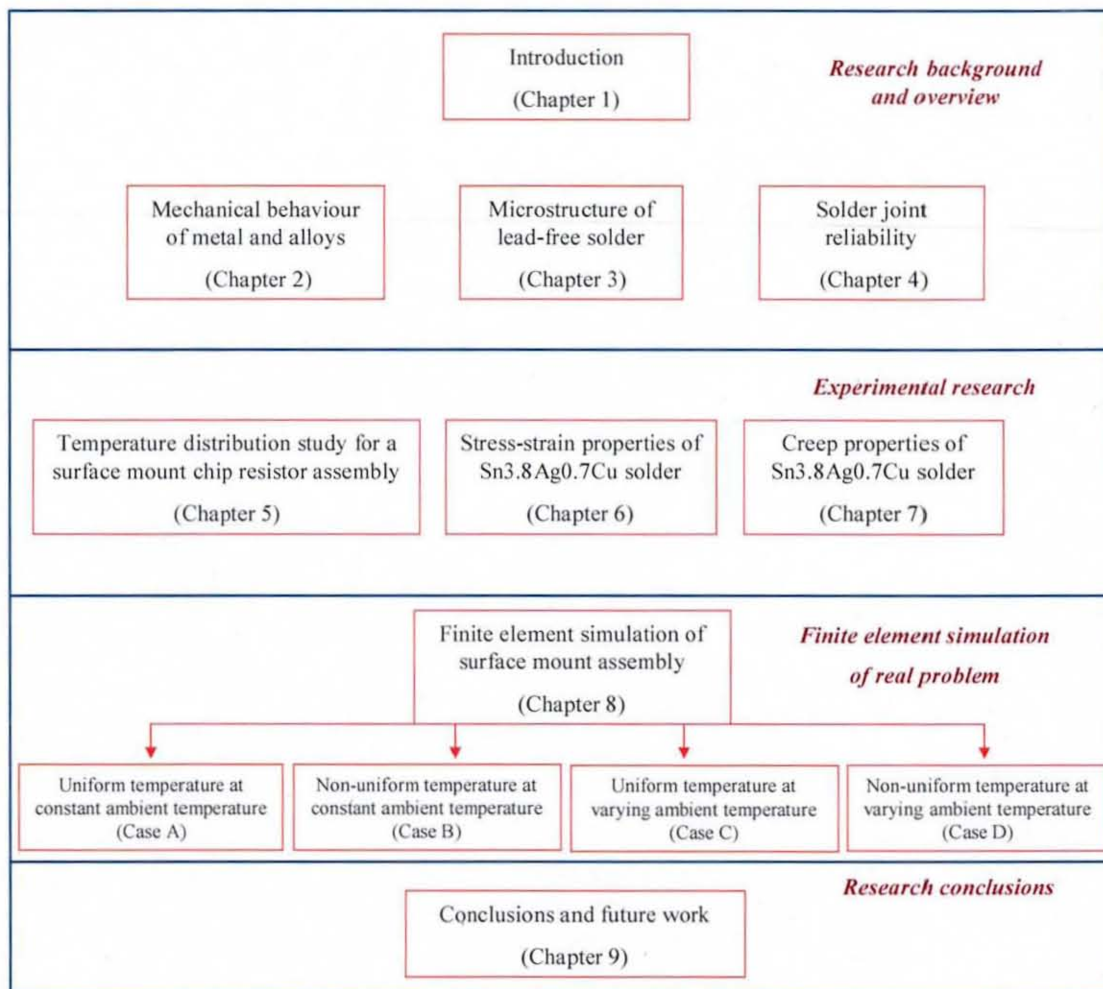


Fig. 1-3: Thesis structure

2. Mechanical Behaviour of Metals and Alloys

This chapter discusses the mechanical behaviour of metals and alloys including solder materials. It also reviews the plasticity theory for time-independent plasticity, viscoplastic, and creep behaviour in metals and alloys. In addition, the constitutive equations for creep and viscoplasticity and their importance for modelling of the solder joint behaviour are discussed.

2.1 Introduction

In all engineering applications the components of a structure are subjected to various kinds of loads. Such components must be properly designed to resist the actual or probable loads that may be imposed upon them. Before designing any structure, the materials used in that structure must be studied thoroughly for all the operating conditions that they will be subjected to. Therefore, the mechanics of materials and their metallurgy are important subjects which enable engineers to understand various mechanical properties and the influence of microstructure on them. Solder joints in electronic products have a primary function of providing electrical connection, but must also withstand mechanical harsh loads due to environmental conditions. Due to the removal of lead from electronic products, the new lead-free materials must be tested to obtain their mechanical properties. These properties can be obtained by performing tension, compression or shear tests. Before moving on to describe the practical experiments conducted on lead-free solder joints, the background related to the elastic, plastic and creep behaviour of metals and alloys, including lead-free solders, are discussed.

2.1.1 Stress and Strain in Materials

All structural materials deform when subjected to an external load. When a body is subjected to an external load, there are also internal forces developed to resist the deformation of the body, and this force per unit of area is called a stress. Consider an example of a uniform cylindrical bar subjected to an axial tensile load (Fig. 2-1). Assume that two gauge marks are put on the surface of the bar in its unstrained state and that L_o is the gauge length between these marks. A load P is applied to both ends of the bar. As a result of this axial load, the diameter of the bar decreases and the

distance between the gauge marks increases by an amount δ. This increase in the gauge length from L_o to L ($L = L_o + \delta$) is called deformation. Thus the average engineering strain, ε_E, is given by the ratio of the change in length to the original length [21-23]:

$$\varepsilon_E = \frac{\delta}{L_o} = \frac{L - L_o}{L_o} \quad 2.1$$

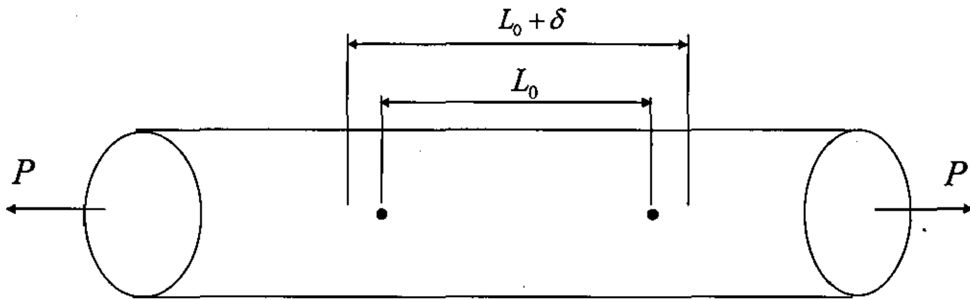


Fig. 2-1: Cylindrical bar subjected to axial load

Strain is a dimensionless quantity since both δ and L_o are expressed in units of length. When the external load P is applied, it is balanced by the internal resisting force which is integral of the stress normal to the cross sectional area A of the bar. Thus the equilibrium equation is:

$$P = \int \sigma dA \quad 2.2$$

where σ is the stress is the material. Assuming σ is constant over the area, A, Eq. (2.2) becomes [23]:

$$P = \sigma \int dA = \sigma A$$

and therefore:

$$\sigma = \frac{P}{A} \quad 2.3$$

In general, the stress will not be uniform over the area A, and therefore Eq. (2.3) represents an average engineering stress in the direction normal to the cross section. Apart from the normal stress, there is a shear stress which acts along the plane and perpendicular to it. Consider an inclined plane mn (Fig. 2-2a) with cross sectional area A^1. The axial load P can be resolved into a normal load P_n and tangential load P_t on this plane. The tangential load P_t causes a stress along the plane mn and it is given by [21-24]:

$$\tau = \frac{P_t}{A^1} \tag{2.4}$$

The shear stress acting along the surface causes angular changes in the geometry of a body, which is known as shear strain. The Fig. 2-2(b) illustrates the strain produced by the pure shear of one face of a cube. The angle at A, which is originally 90°, is decreased by the application of shear stress by a small amount θ. The shear strain γ is the displacement a divided by the distance between the planes, h. This ratio also represents the angle through which the element has been rotated. Therefore, shear strains are often expressed as angles of rotation [23].

$$\gamma = \frac{a}{h} = \tan\theta \tag{2.5}$$

It is also found from mechanical tests that up to a certain limiting load a solid will recover its original dimensions when the load is removed. This phenomenon of a solid body is known as elastic behaviour. Usually this kind of mechanical property of a metal is obtained from tensile tests. The following sections will discuss the general mechanical properties of materials with the help of stress-strain curves under a tensile test on a typical metal.

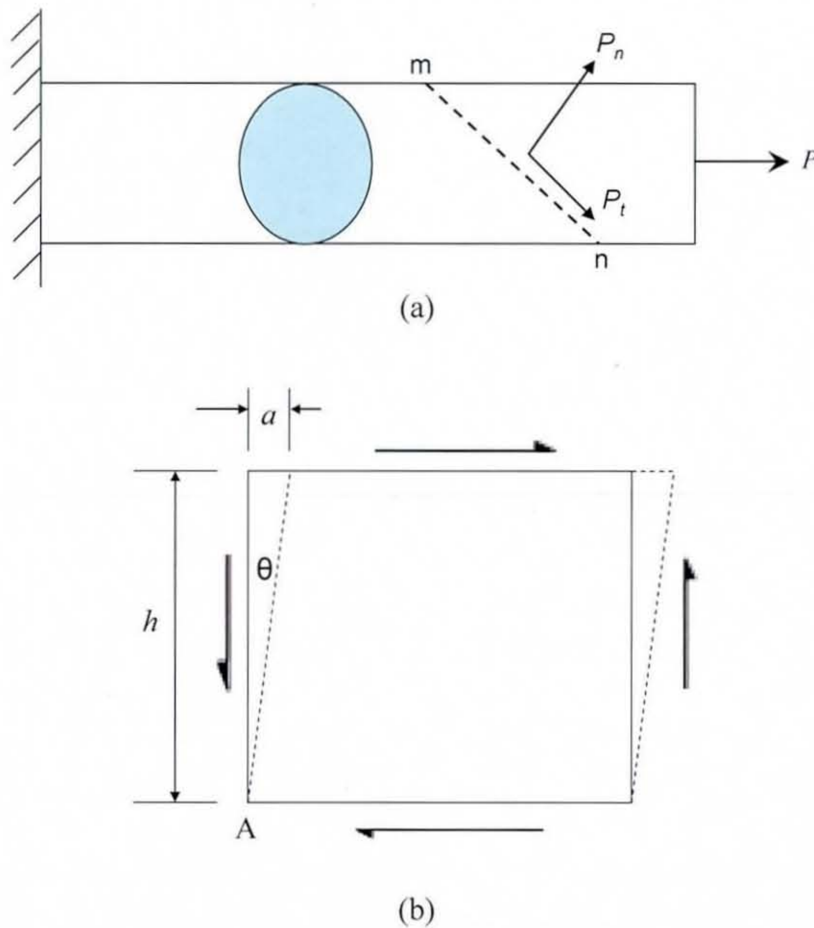


Fig. 2-2: Cylindrical bar with: (a) load on an inclined plane; (b) shear strain

2.1.2 Stress-Strain Diagram

The line OAF in Fig. 2-3 shows a typical stress-strain diagram for a metal. From this diagram the important characteristics such as yield point, ultimate strength and amount of plastic elongation can be obtained. In a tensile test the strain, ε, increases with the applied load *P*. The stress in the material is usually proportional to the strain, as long as loading is within the proportional limit, which is represented by 'A' in the figure. This is also called linear elasticity, where Hooke's law holds. The proportionality constant is called the Young's Modulus, *E*, i.e.:

$$\sigma = E\varepsilon \quad 2.6$$

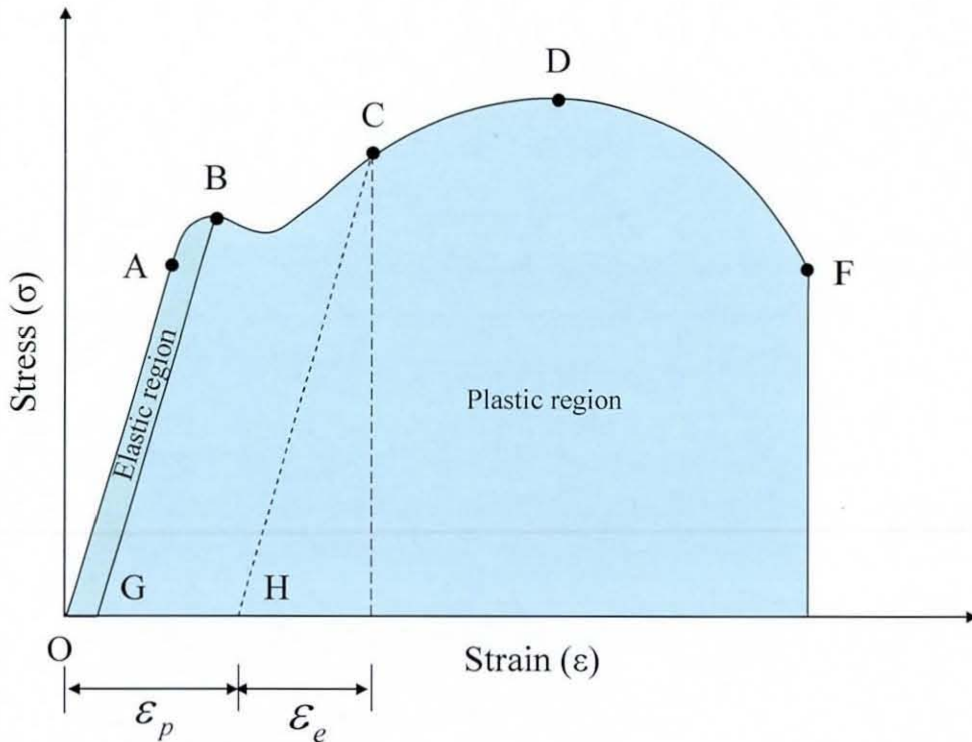


Fig. 2-3: Typical engineering stress-strain diagram for a tensile test

The maximum stress at which the material remains within the elastic limit is referred to as the elastic limit. Usually, the elastic limit is larger than the proportional limit. In determining the proportional limit, sensitive extensometers are necessary in order to detect the slightest deviation from a straight line during the tensile test. In order to obtain greater uniformity in results, a specified amount of permanent set or a certain deviation from proportionality is often taken as the basis for determining the proportional limit. The 1906 International Congress for Testing Materials in Brussels defined the proportional limit as the tensile stress at which the permanent set is 0.001 percent. Since then there has been a tendency to increase this limiting magnitude of permanent set to 0.01 percent [25-27].

When the load produces a stress (point C in the Fig. 2-3) that exceeds the elastic limit, the strain does not disappear upon unloading, instead it follows curve CH with a slope equal to that of the straight line OA. The strain recovered after unloading from C is called elastic strain, ε_e, while the remaining strain is called plastic or permanent

strain, ε_p. Thus the total strain at C is the sum of permanent strain and elastic strain, and is given by Eq. (2.7). This is called classical additive decomposition of strain [28].

$$\varepsilon = \varepsilon_e + \varepsilon_p \tag{2.7}$$

The yield point (point B in Fig. 2-3) is a very important characteristic for materials such as ductile metallic alloys. Ductile materials such as steel show a pronounced yield point, while this is unclear for some other metal alloys such as inconel, titanium and aluminium based alloys. The Yield stress (σ_y) is obtained for such materials with the straight line BG drawn from the offset strain value, with a slope equal to that of line OA. The commonly used offset value of permanent set is 0.2 percent [22-27]. Materials behave inelastically beyond this point, the yield point, which is very important for more detailed study of the material.

Another important characteristic that can be determined from the stress-strain diagram is the ultimate tensile strength or ultimate tensile stress, σ_u, which is defined as the stress obtained by dividing the maximum load born by the specimen by the initial cross-sectional area. This quantity is often taken as a basis for determining the allowable working stress.

The percent elongation is a measure of ductility of the material. It is calculated by dividing the change in length by original length and multiplied with 100. As the specimen elongates, its lateral dimensions decrease, thereby reduce the cross sectional area. The ratio of change in lateral dimensions to axial dimension is constant for a given material. This constant is known as Poisson's ratio (ν). However, this decrease in cross sectional area is not considered in the calculation of engineering stress and engineering strain. True stress and true strain, which give the true indication of the deformation characteristics of a material, consider the change in the cross sectional area.

Below the elastic limit, Hooke's law also holds for shear stress and strain. Therefore, shear stress is proportional to shear strain, and this proportionality is called the shear

modulus (G). The relationship between young's modulus (E) and shear modulus is [23, 24]:

$$G = \frac{E}{2(1+\nu)} \quad 2.8$$

The changes in the specimen dimensions also results in volume change. This volumetric change is proportional to the applied stress and inversely proportional to the quantity K, which is called the bulk modulus of elasticity. The relationship between Young's modulus and bulk modulus is [23, 24]:

$$K = \frac{E}{3(1-2\nu)} \quad 2.9$$

2.1.3 True Stress and True Strain

True stress can be defined as the ratio of applied load, P and the instantaneous cross sectional area A_i:

$$\sigma_T = \frac{P}{A_i}. \quad 2.10$$

True stress can also be related to the engineering stress with the assumption that there is no volume change in the specimen before and after loading. Therefore, the volume before the test is equal to that after the test, i.e.

$$A_i \cdot L_i = A_o \cdot L_o.$$

Then, true stress is given as [23]:

$$\sigma_T = \frac{P}{A_i} = \frac{P}{A_o} \cdot \frac{L_i}{L_o} = \sigma_E (1+\varepsilon_E) \quad 2.11$$

The true strain is defined as the sum of all the instantaneous engineering strains. Therefore, true strain is given as [23]:

$$\varepsilon_T = \int d\varepsilon = \int_{L_o}^{L_f} \frac{dL}{L} = \ln\frac{L_f}{L_o} = \ln\frac{L_o + \Delta L}{L_o} = \ln(1+\varepsilon_E) \qquad 2.12$$

Thus, the true strain can also be related back to engineering strain through the above manipulations. Figure 2-4 shows a comparison of an engineering stress-strain diagram with a true stress-strain diagram. The stress-strain diagram remains coincident till the yield point, but thereafter necking occurs. As the strain increases and the cross-sectional area of the specimen decreases, the true stress can be much larger than the engineering stress.

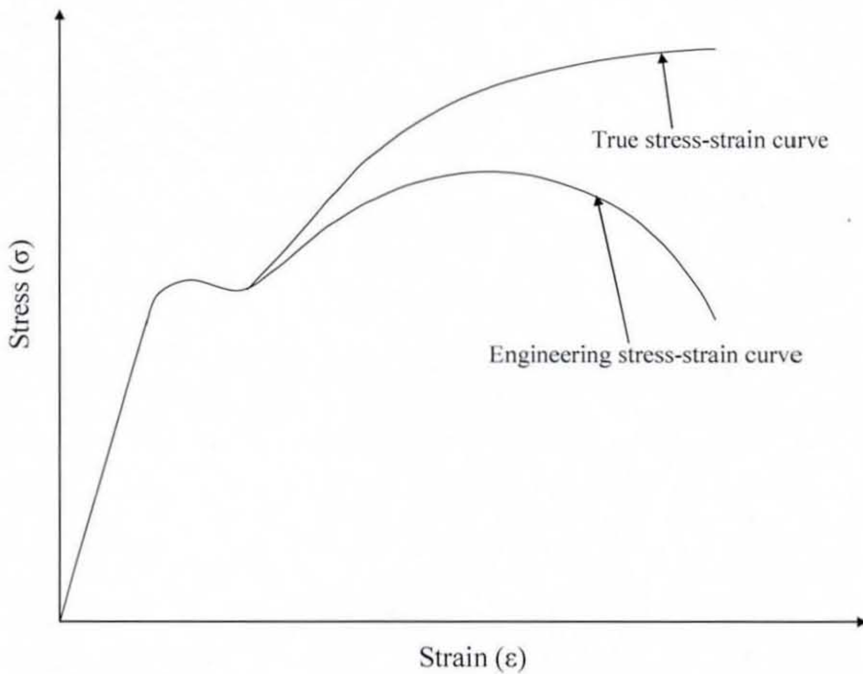


Fig. 2-4: Engineering stress-strain curve vs. a true stress-strain curve

The design of an engineering structure becomes easier when the loads in the structure remain within the elastic limit. However, many engineering structures are subjected to complicated loadings where deformation is beyond the elastic limit. In addition, sometimes they operate in high temperature environments. For example, the solder joints in electronic packaging may operate at high temperatures compared to their melting temperature. The usual operating temperature range is between 218 K and 423 K depending on the application compared with melting temperature of 490 K for

SnAgCu solder. Under these circumstances, the response of solder joints may be a combination of elastic, plastic, viscoplastic, creep or fracture [22, 29-31]. Thus, plasticity, viscoplasticity and creep behaviour play a very important role in selecting a new lead-free solder alloy as a replacement for tin-lead solder. The elastic response in general of materials has been discussed in brief in the above section, but understanding the basics of plasticity, viscoplasticity and creep is also important.

2.2 Time Independent Plasticity

Time independent plastic deformation refers to a material behaviour that results from fast loading rates. The term plasticity is used to describe the inelastic behaviour of a material that retains permanent deformation on complete unloading. Unlike elastic deformation, plastic deformation is a result of microstructural changes in the material during deformation [32]. Usually tension, compression or shear tests are used to determine the stress-strain behaviour of a material under uniaxial loading conditions with strain rates in the range of 0.0033 to 0.1667 per min [22]. The material properties obtained under these conditions are often used in a wide range of engineering design situations. However, in practice the kind of loading on the structural member may create a state of stress that is biaxial or triaxial in nature. Such conditions place limitations on the use of material properties obtained from uniaxial tests [22]. For example, plastic deformation can occur in a member where the imposed load results in a multiaxial stress state, even if none of the individual stress components exceed the uniaxial yield stress for the material. This indicates that, under multiaxial stress states, the initiation of yielding is governed by some quantity other than the individual stress components themselves [22, 23, 28]. Thus it is necessary to combine all components of stress into an effective uniaxial stress. This effective stress is then compared usually with the uniaxial yield stress, using an appropriate yield criterion to predict the onset of plastic deformation. The study of the behaviour of materials that yield is known as plasticity theory. In general, a complete plasticity theory has three components: a yield criterion that defines the initiation of yield in a material, a flow rule that relates the plastic strain increment to the stress increment after initiation of yielding, and a strain hardening or softening rule that predicts changes in the yield surface owing to the plastic strain [22]. These three components of plasticity theory are discussed briefly below.

2.2.1 Yield Criteria

The problem of deducing mathematical relationships for predicting the conditions at which yielding begins when a material is subjected to any possible combination of stress is an important consideration in the field of plasticity. For uniaxial loading, macroscopic plastic flow begins at the yield stress, σ_y. Unfortunately, quantitative criteria for yielding of materials under multiaxial states of stress are incomplete and as such are an ongoing field of research [22]. However, it is expected that yielding under a situation of combined stresses can be related to some particular combination of component or principal stresses.

The yielding criteria are essentially based on experimental relationships. A yield criterion must be consistent with a number of experimental observations, the chief of which is that pure hydrostatic pressure does not cause yielding in a material. Therefore, only deviatoric stresses are considered to be involved with yielding [23]. There are many yield criteria that have been developed for predicting the onset of yielding in both ductile and brittle materials. However, the discussion here will be limited only to the von Mises or distortion-energy criteria, due its wide range of application and its usage in the present research work.

The von Mises or Distortion-Energy Criterion

This yield criterion was proposed by von Mises in the year 1913 and it is also called the distortion-energy criterion [22, 23]. According to this criterion, yielding in a material begins when the distortional strain-energy density at a point equals the distortional strain-energy density at yield in uniaxial tension (or compression). The distortional energy density is that energy associated with a change in the shape of a body. Thus, the total strain energy, U_O, can be broken into two parts: one that causes the volumetric change, U_V, and another which causes distortion, U_D. U_O is defined as [22]:

$$U_O = \frac{(\sigma_1+\sigma_2+\sigma_3)^2}{18K} + \frac{(\sigma_1-\sigma_2)^2+(\sigma_2-\sigma_3)^2+(\sigma_3-\sigma_1)^2}{12G} \qquad 2.13$$

where K is the bulk modulus; G is the shear modulus; and σ_1, σ_2 and σ_3 are principal stresses along three mutually perpendicular axes. The first term on the right hand side of Eq. (2.13) is U_V, the strain-energy density associated with pure volume change. The second term of Eq. (2.13) is the distortional strain-energy density, U_D i.e.:

$$U_D = \frac{(\sigma_1 - \sigma_2)^2 + (\sigma_2 - \sigma_3)^2 + (\sigma_3 - \sigma_1)^2}{12G} \qquad 2.14$$

Under uniaxial stress a material yields when $U_D = U_{DY} = \sigma_y^2 / 6G$. Thus, for a multiaxial stress state, yielding is initiated when the distortional energy density U_D equals $\sigma_y^2 / 6G$ [21-23, 28]

The distortional energy density U_D can alternately be written in terms of the second deviatoric stress invariant, J_2, as [23]:

$$U_D = \frac{1}{2G}|J_2| \qquad 2.15$$

where:

$$J_2 = -\frac{1}{6}\left[(\sigma_1 - \sigma_2)^2 + (\sigma_2 - \sigma_3)^2 + (\sigma_3 - \sigma_1)^2\right] \qquad 2.16$$

At yield in uniaxial tension (or compression), $\sigma_1 = \pm\sigma_y$ and $\sigma_2 = \sigma_3 = 0$. Then:

$$|J_2| = \frac{1}{3}\sigma_y \qquad 2.17$$

From Eqs. 2.13 and 2.15, the yield function (F) for the distortional energy density (von Mises) may be written as:

$$F = \frac{1}{6}\left[(\sigma_1 - \sigma_2)^2 + (\sigma_2 - \sigma_3)^2 + (\sigma_3 - \sigma_1)^2\right] - \frac{1}{3}\sigma_y^2 \quad 2.18$$

The yield function can also be written as [23, 28]:

$$F = \sigma_e^2 - \sigma_y^2 \quad 2.19$$

where the effective stress is

$$\sigma_e = \sqrt{\frac{1}{2}\left[(\sigma_1 - \sigma_2)^2 + (\sigma_2 - \sigma_3)^2 + (\sigma_3 - \sigma_1)^2\right]} = \sqrt{3|J_2|} \quad 2.20$$

In terms of direct and shear stresses, the effective stress for the von Mises criterion can be written as

$$\sigma_e = \sqrt{\frac{1}{2}\left[(\sigma_{xx} - \sigma_{yy})^2 + (\sigma_{yy} - \sigma_{zz})^2 + (\sigma_{zz} - \sigma_{xx})^2\right] + 3(\tau_{xy}^2 + \tau_{yz}^2 + \tau_{zx}^2)} \quad 2.21$$

where σ_{xx}, σ_{yy}, and σ_{zz} are the normal stresses acting in the x, y, and z direction respectively; τ_{xy} is the shear stress acting in the y-direction of the plane normal to the x-axis; τ_{yz} is the shear stress acting in the z-direction of the plane normal to the y-axis; and τ_{zx} is the shear stress acting in the x-direction of the plane normal to the z-axis.

2.2.2 Flow Curves

The stress-strain curve obtained during unixial loading is of fundamental interest in plasticity when the curve is plotted in terms of true stress σ_T and true strain ε_T. A true stress-strain curve is frequently called a flow curve because it gives the stress required to cause the metal to flow plastically to any given strain [23]. A typical true stress-strain is illustrated in Fig. 2-4. The material is assumed to be elastic up to the yield stress, σ_y. Beyond this value, metals usually deform plastically. Most metals strain-harden in the plastic region, meaning that higher stress values than the initial yield stress are required to produce increased strain. However, unlike the situation in the

elastic region, the stress and strain are not related by any simple constant of proportionality.

Many attempts have been made to fit mathematical equations to flow or hardening curves. The most common is a power law expression of the form [23]:

$$\sigma = K_p \varepsilon^n \quad 2.22$$

where K_p is the stress at a strain ε=1.0 and n is a strain-hardening coefficient. This equation is valid only from the beginning of plastic flow to the maximum load at which the specimen begins necking. Generally the flow equations used are the best fit obtained to the experimentally determined true stress-strain curve. Some materials exhibit increased strength with increased strain rate. The flow equation can also capture the sensitivity of the hardening curve to the strain rate, which is known as rate-dependent plasticity. Rate-dependent plasticity is discussed later in this chapter.

2.2.3 Strain Hardening Rules

Experiments show that if a material is plastically deformed, then unloaded, and then re-loaded so as to induce further plastic flow, its resistance to plastic flow will have increased. This is known as strain hardening. Strain hardening can be modelled by relating the size and shape of the yield surface to the plastic strain in some appropriate way. The most commonly used strain hardening rules, ie. isotropic and kinematic hardening, are discussed here. Both these hardening rules are discussed considering the von Mises yield criterion which is used later in the simulations of solder joint behaviour.

Isotropic Hardening

Hardening of metals is primarily a function of accumulated plastic strain, ε_p, which can be written as [28]:

$$\varepsilon_p = \int d\varepsilon_p = \int \dot{\varepsilon}_p dt \quad 2.23$$

where $\dot{\varepsilon}_p = d\varepsilon_p / dt$ and $d\varepsilon_p$ are the plastic strain rate and plastic strain increment, respectively. A uniaxial stress-strain curve with non-linear hardening is illustrated in Fig. 2-5, together with schematic representations of the initial and subsequent von Mises yield surfaces. In this instance, the subsequent yield surface can be seen to have expanded compared with the original. When the expansion is uniform in all directions in stress space, the hardening is referred to as isotropic. In this case the origin of the yield surface remains same. For example, in Fig. 2-5 the loading is in the 2-direction. Thus the load point moves in the σ_2 direction from zero until it meets the yield surface at $\sigma_2 = \sigma_y$, which point yield occurs. In order for hardening to take place, and for the load point to stay on the yield surface, the yield surface must expand as σ_2 increases, as shown in Fig. 2-5. The amount of expansion is often taken to be a function of accumulated plastic strain, ε_p, and the yield function can be given as [28, 33]:

$$F\left(\sigma, \varepsilon_p\right) = \sigma_e - \sigma_y = \sigma_e - \sigma_y(\varepsilon_p) = 0 \qquad 2.24a$$

$$\sigma_y\left(\varepsilon_p\right) = \sigma_{yi} + r\left(\varepsilon_p\right) \qquad 2.24b$$

where σ_{yi} is the initial yield stress and $r\left(\varepsilon_p\right)$ is an isotropic hardening function that can be a constant, a linear function, or a power law function.

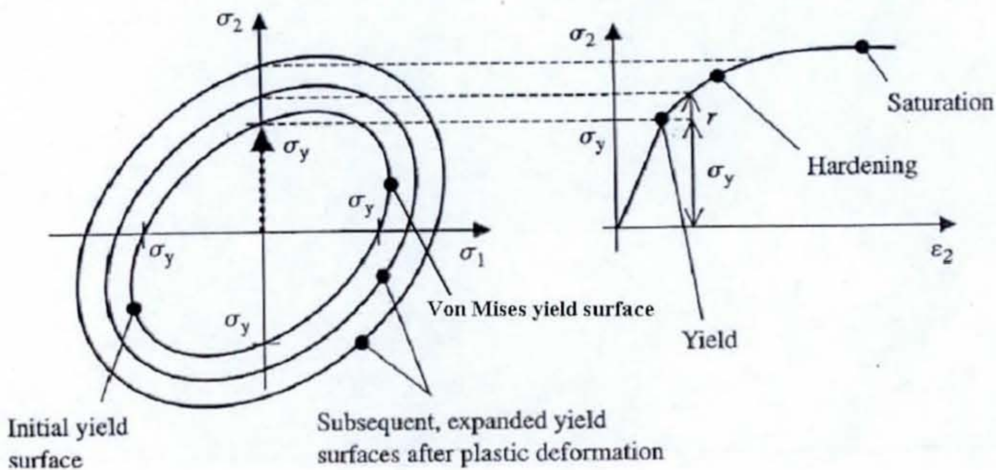


Fig. 2-5: Isotropic hardening in which the yield surface expands with plastic deformation and the corresponding uniaxial stress-strain curve [28]

Kinematic Hardening

In the case of monotonically increasing loading, it is often reasonable to assume that any hardening that occurs is isotropic. The use of an isotropic hardening rule in the case of reversed loading can be erroneous, due to the equal yield surface expansion. Consider a material which hardens isotropically, shown schematically in Fig. 2-6. At a point of ε_i, corresponding to load point (1) shown in the figure, the load is reversed so that the material behaves elastically (the stress is now lower than the yield stress) and linear stress-strain behaviour results until load point (2). At this point, the load point is again on the expanded yield surface, and any further increase in load results in plastic deformation. Figure 2-6(b) shows that isotropic hardening leads to a very large elastic region, on reversed loading, which is often not what would be seen in experiments. In fact, a much smaller elastic region is expected and this results from what is called the Bauschinger effect [28].

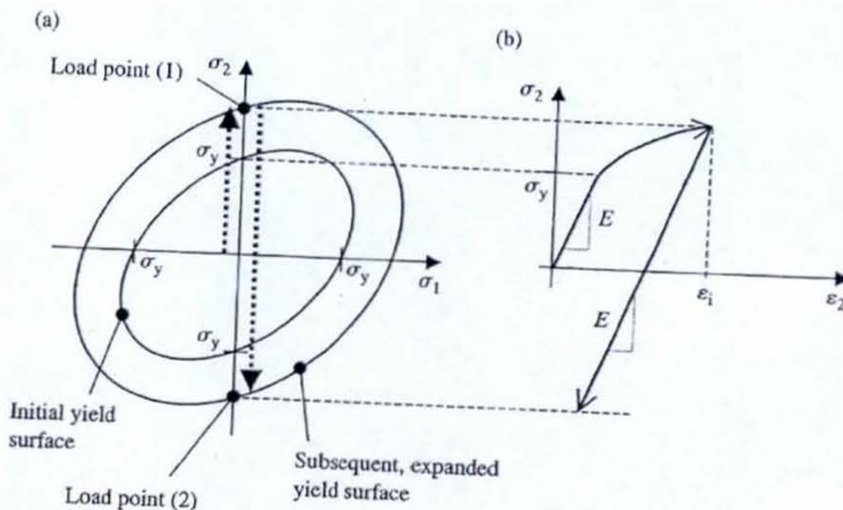


Fig. 2-6: Reversed loading with isotropic hardening showing (a) the yield surface and (b) the resulting stress-strain curve [28]

To include this effect, an alternative law called kinematic hardening is used. In this hardening law, the yield surface translates in stress space, rather than expanding. The graphical representation of this law is shown in Fig. 2-7. In Fig. 2-7a, the stress increases until the yield stress, σ_y, is achieved. With any further increase of the load, the material deforms plastically and the yield surface translates in the dominant stress direction, in this case σ_2, such that the initial centre shifts by $|x|$. When the load is reversed from load point (1) on the yield surface, the material behaves elastically until

load point (2). The elastic region for kinematic hardening is $2\sigma_y$, whereas for isotropic hardening it is $2(\sigma_y + r)$, where r is the expansion of the yield surface.

In the absence of kinematic hardening, the yield function is written in terms of tensor stresses[28, 33]:

$$F = \sigma_e - \sigma_y = \left(\frac{3}{2}\sigma' : \sigma'\right)^{\frac{1}{2}} - \sigma_y \qquad 2.25$$

where $\sigma_e = \left(\frac{3}{2}\sigma' : \sigma'\right)^{\frac{1}{2}}$, deviatoric stress, $\sigma' = \sigma - \frac{1}{3}(\sigma.I)I$ and $\sigma' : \sigma'$ is the contracted tensor product [28]. With kinematic hardening, however, it is:

$$F = \sigma_e - \sigma_y = \left(\frac{3}{2}(\sigma' - x') : (\sigma' - x')\right)^{\frac{1}{2}} - \sigma_y \qquad 2.26$$

where x' is the kinematic hardening variable and is often called the back stress.

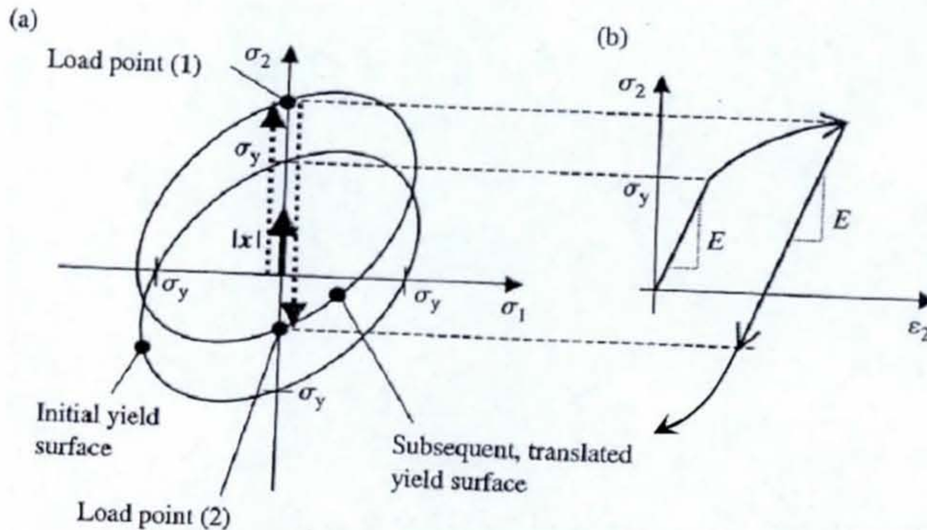


Fig. 2-7: Kinematic hardening showing (a) the translation, 1x1 of the yield surface with plastic strain, and (b) the resulting stress-strain curve with shifted yield surface in compression - the Bauschinger effect [28]

2.3 Viscoplasticity and Creep

The previous section discussed time-independent plasticity, that is, the stress-strain behaviour has been assumed to be independent of both time and rate of loading, whether it is strain or stress controlled. But the rate of loading, hold time and temperature can have significant effects on the stress-strain behaviour of the material.

Viscoplasticity is where plasticity is affected by the rate of loading. Similarly, creep also results in material plasticity, but it is time dependent under sustained load. Creep is normally used to describe low strain rate, time-dependent irreversible deformation which is either diffusion controlled, or influenced by diffusion, though there may well be crystallographic slip still occurring [22, 23, 28, 32].

2.3.1 Viscoplasticity

Inelastic deformation in crystalline solids is, in general, rate-dependent. Therefore, rate-independent plasticity theories represent idealizations, which have limited applicability. Viscoplasticity describes rate-dependent plasticity in solids in which crystallographic slip is the dominant deformation process. Higher rates of loading usually results in larger strains and strain rates in the material, which affects the stress-strain behaviour.

Consider a material that behaves in a ductile manner in a standard tensile test. For such a material, the stress-strain curve will generally have an elastic region, followed by a plastic (inelastic) region. If the tensile test is conducted at a high load (strain) rate, the amount of inelastic deformation before the failure of the test specimen may be reduced considerably, relative to that under normal load rates. This results in a material response which appears less ductile, and also increases the apparent Young's modulus E, yield strength σ_y and flow stress. Tin based alloys are highly strain rate sensitive. Also solder material properties are very sensitive to operating temperature (T_{op}), because typically $T_{op} > 0.5T_m$ (melting temperature). Various researchers have carried out experimental studies across the world to find out the rate- and temperature-dependent stress-strain response for lead-free solders in bulk and as in the form of solder joints [34-37]. They have used a wide range of strain rates and temperatures to evaluate their effect on solder properties such as Young's modulus, yield strength and ultimate strength. All of these experimental results have shown similar effects, such as an increase in Young's modulus, yield strength and ultimate strength with increases in strain rate, while an increase in temperature showed the opposite effect.

In viscoplasticity, the elastic-plastic strain decomposition as discussed in section 2.1.2 still holds, and determination of yield is similar to that for time independent plasticity

with a yield function. In the case of viscoplasticity, once yielding has occurred, the material may harden isotropically or kinematically. An important difference with rate-independent plasticity is that the load point may lie outside of the yield surface. As a result, some viscoplasticity models are referred to as over-stress models. Figure 2-8 illustrates schematically the material stress-strain response and the corresponding yield surface, which is assumed to expand due to linear isotropic hardening. At load point (1) shown on the yield surface in Fig. 2-8(a) and at the corresponding point on the uniaxial stress-strain curve in Fig. 2-8(b), for the case of time-independent plasticity, the stress achieved is the yield stress, σ_y, together with the contribution from any linear isotropic hardening, $r(\varepsilon_p)$, so that:

$$\sigma = \sigma_y + r(\varepsilon_p) \tag{2.27}$$

The resulting stress-strain curve is shown by the broken line in Fig. 2-8(b) [28, 33]. However, for the case of viscoplasticity, the stress is augmented by the viscous stress, σ_v, also schematically shown in Fig 2-8(b) by the solid line [28].

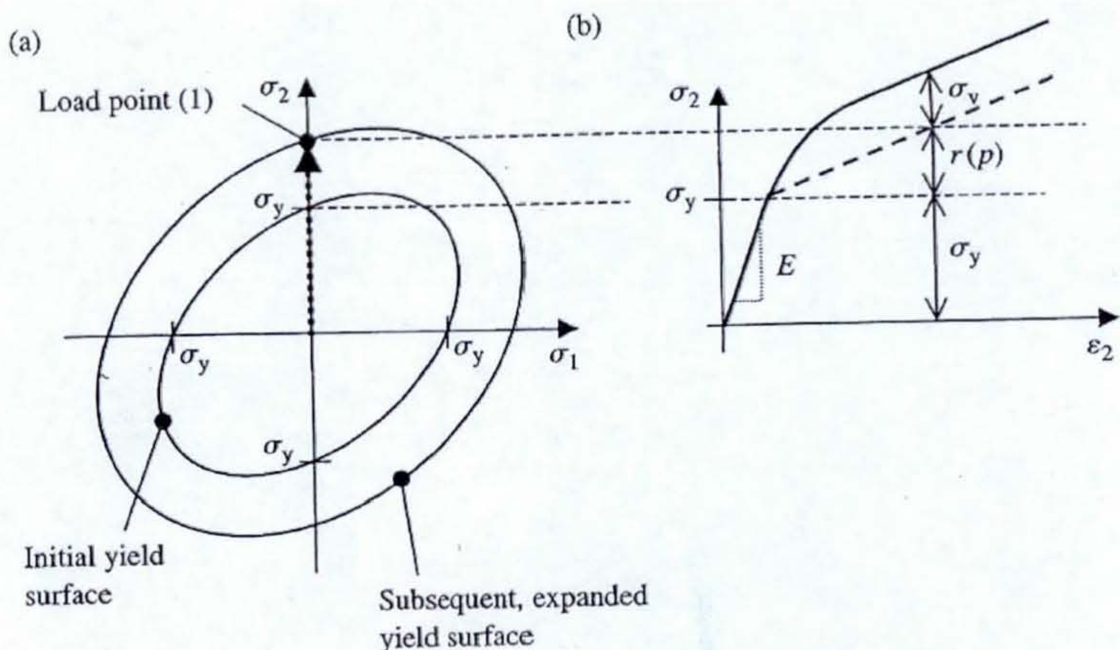


Fig. 2-8: (a) The von Mises yield surface in plane stress for viscoplasticity with linear isotropic hardening and viscous (or over) stress and (b) the corresponding stress-strain curve [28]

One of the major aims of obtaining these rate- and temperature-dependent properties is to use them in reliability studies of solder joints in electronic packaging. The rate- and temperature-dependent material properties can be represented in a constitutive equation to use in the finite element simulation. There are many constitutive models which can adequately represent both high-rate loading and temperature dependency. The most commonly used models are modified Ramberg-Osgood and Johnson-Cook [37-41]. Pang *et al.* [37] used a modified Ramberg-Osgood model to include the effect of both rate and temperature in the stress strain curve for a lead-free solder. The general form of the Ramberg-Osgood model is:

$$\varepsilon = \frac{\sigma}{E} + \phi\left(\frac{\sigma}{\sigma_o}\right)^n \tag{2.28}$$

where n is the hardening exponent, and ϕ and σ_o are material constants. However to represent strain rate and temperature dependencies, some modifications have been required and the Pang *et al.* [37] modified Ramberg-Osgood model is:

$$\varepsilon(T,\dot{\varepsilon}) = \frac{\sigma}{E} + \phi\left(\frac{\sigma}{\sigma_o(T,\dot{\varepsilon})}\right)^{n(T,\dot{\varepsilon})} \tag{2.29}$$

In this model, both the hardening exponent, n, and stress coefficient, σ_o, are temperature and strain rate dependent. The strain rate and temperature dependency of n and σ_o can easily be obtained from tensile tests that various strain rates at different temperatures.

The alternative Johnson Cook (JC) constitutive equation for viscoplastic behaviour is given below [38, 40, 41]:

$$\sigma_e = \left(A_1 + B\varepsilon_{ep}^n\right)\left(1 + C_1 \ln \dot{\varepsilon}_{ep}^*\right)\left(1 - T_h^m\right) \tag{2.30}$$

where ε_{ep} is equivalent plastic strain, $\dot{\varepsilon}_{ep}^{*} = \dot{\varepsilon}_{ep} / \dot{\varepsilon}_{o}$ is the dimensionless equivalent plastic strain rate, $\dot{\varepsilon}_{ep}$ and $\dot{\varepsilon}_{o}$ are the current and reference strain rates, and T_h is the homologous temperature. The five material constants are A_1, B, n, C_1 and m. In the JC model, the equivalent stress is the product of a strain hardening factor $\left(A_1 + B\varepsilon_{ep}^{n}\right)$, a viscoplastic part $\left(1 + C_1 \ln \dot{\varepsilon}_{ep}^{*}\right)$, and a temperature sensitivity part $\left(1 - T_h^{m}\right)$. If the experimental stress-strain data are available only for a single temperature, temperature effects must be neglected. The material parameters A_1, B, n, C_1 and m are determined by using the results from tensile or compression tests at different strain rates and temperatures.

2.3.2 Creep

The term creep denotes the slow deformation of solid matter under sustained loading. At elevated temperatures, a sustained load may produce inelastic (plastic) deformation in a material that increases with time. Creep is defined as time-dependent inelastic strain under a sustained load at elevated temperature [22, 23, 42]. The first systematic studies providing some quantitative information on the nature of creep were those of Andrade in 1910 [22, 23, 42]. During this time there was a rapid increase in the steam admission temperatures in power plants which were approaching the creep range of low-alloy steels. Early creep research focused on finding a creep limit, below which creep would not occur, but use of more accurate experimental techniques showed this idea to be false [42]. Creep will occur in any metal subjected to a constant load at a temperature even slightly above its recrystallization temperature. At this temperature, the atoms become quite mobile. As a result time-dependent alterations of the metal structure occur. As a rule of thumb, the temperature at which creep becomes important for designers is about 0.4 of the melting temperature of the material considered [22, 23, 42]. Usually this temperature is expressed as the homologous temperature (T_h), which is the ratio (in Kelvin) of the working temperature to the melting temperature of the material. In reality the homologous temperature at which creep is active must be determined individually for each material on the basis of its behaviour. In addition, when materials are subjected to a strain controlled environment at high homologous temperature the induced stress decreases over time with the accumulation of creep

deformation. This phenomenon is known as stress relaxation, which is very common in solder joint operating environments.

Creep has become a major consideration for the designers of high operating temperature power generation plants, steam and gas turbines, oil refineries, and chemical plants. In electronic packaging, the solder joints used as interconnections are subjected to creep due to their high operating temperatures compared to their melting temperature. The melting temperature of potential lead-free solder alloys ranges from 411 K to 516 K, but typical extreme operating temperatures vary from 218 K to 423 K, depending on the application. This results in a high homologous temperature for solder materials and they are therefore prone to creep during operation. For example, the homologous temperature for 95.5Sn3.8Ag0.7Cu solder at room temperature is 0.6. Therefore, creep performance plays an important role in the selection of solder materials for electronic packaging.

Creep Curves

A creep curve is a graphical representation of the dependence of the strain on the time for a constant stress and temperature. An idealized shape of creep curve is shown in Fig. 2-9. The initial strain, ε_o, is developed immediately upon loading. The creep curve can be divided in to three main regions: the primary, or transient stage; the secondary, or steady state stage; and the tertiary stage.

During primary or transient creep, the creep rate decreases with time, due to the increase in resistance of the material. It is a relatively complex phenomenon because of the underlying microstructural deformation mechanism, and therefore, the strain rate changes with time. Defects, which may either be already present or be created on application of the load, play an important role in primary creep deformation. The density of defects increases further with the progression of creep deformation. The decreasing strain rate at the end of primary creep occurs due to the exhaustion of defects that support creep strain [20]. The primary creep strain can be represented as a logarithmic function of time i.e.[20, 42]:

$$\varepsilon = A_t \ln(\upsilon t)^m \qquad 2.31$$

where A_t is a temperature-dependent constant, and υ and m are constants.

The creep rate remains almost constant in the middle region of the creep curve, which is called secondary or steady state creep. The constant strain rate during secondary creep can be explained by two theories: (a) there is a balance between the creation and annihilation of defects during this period, or (b) there is a relatively constant supply of defects having a constant velocity that establishes the creep rate. The creep rate is determined by the stress level and temperature and is also a thermally activated process. This theory is referred to as the Nabarro-Herring creep process [20]. The steady state creep rate for this region can be calculated using the following equation.

$$\dot{\varepsilon}_s = \frac{d\varepsilon}{dt} \qquad 2.32$$

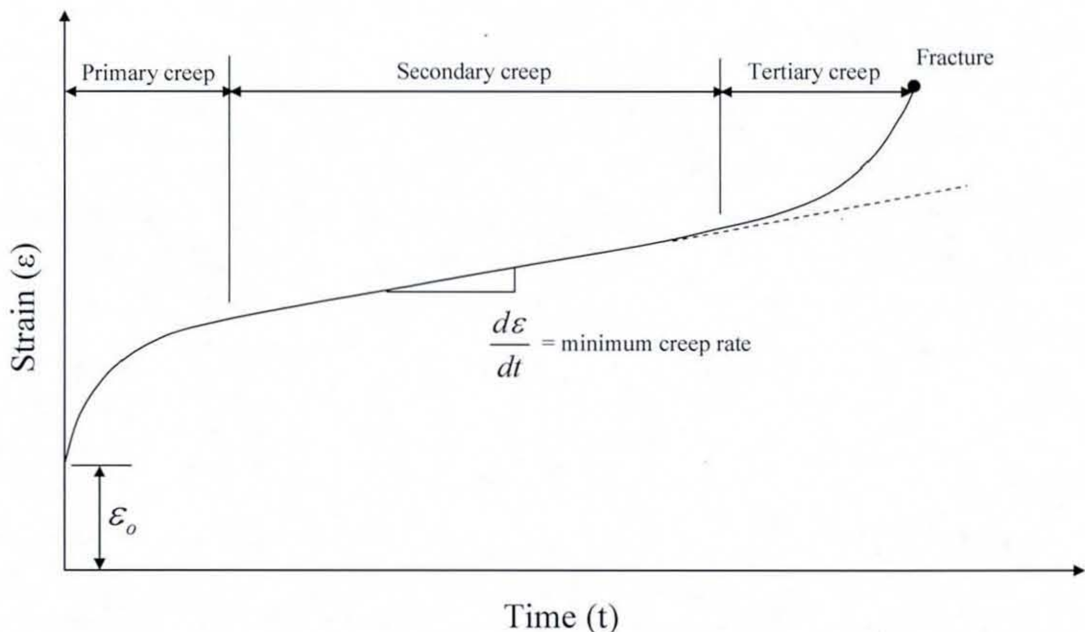


Fig. 2-9: Typical creep curve showing the three stages of creep

The region beyond secondary creep is called tertiary creep. Tertiary creep occurs when there is an effective reduction in the cross sectional area, either because of necking or internal void formation.

In the case of electronic packaging, the solder will deform primarily in the primary and secondary stages due to the service environments. Therefore, the emphasis in the creep tests described in chapter 7 is on the precise determination of strain, particularly the determination of the steady state or minimum creep rate. Under low stresses, the steady state creep stage duration is much larger than that for the other two stages, so the steady state creep rate becomes an important design parameter. Creep rupture tests are similar to creep tests, except that the test is always carried out until material failure.

Creep Mechanisms

A great deal of research has been done into the physical mechanisms for creep deformation. The chief creep deformation mechanisms can be grouped as follows [20, 23, 43]:

Dislocation glide/dislocation climb: In this deformation mechanism, dislocations move along slip planes and overcome any barriers such as grain boundaries or crystals by thermal activation. Creep resulting from a dislocation glide mechanism occurs at stress levels ($\sigma / G > 10^{-2}$), which are high relative to those normally considered in creep deformation.

Dislocation creep: This mechanism involves the movement of dislocations, which overcome barriers by thermally assisted mechanisms involving the diffusion of vacancies or interstitials. This mechanism occurs for $10^{-4} < \sigma / G < 10^{-2}$.

Diffusion creep: In the diffusion creep mechanism, an external stress influences the flow of vacancies and interstitials through a crystal or around the grain boundary in a polycrystal. This mechanism occurs for $\sigma / G < 10^{-4}$.

Creep Equations

Although primary and secondary creep are often analysed as different responses to the applied stress and temperature, they occur as a continuous transition within the material microstructure. The distinction between the two regimes has developed because of the difficulty of combining the two observed behaviours into a single mathematical expression. Because of the relatively high temperatures that are required

to establish steady-state creep in metals and alloys, diffusion-controlled mechanisms typically underlie the resulting deformation. The energy required for this mechanism is represented as an activation energy (ΔH) [20]. For lead-free solders the operating temperature can be as low as 218 K, but this still results in a homologous temperature of about 0.45. Therefore, diffusion controlled mechanisms can dominate the creep behaviour.

Several constitutive equations have been developed to model the steady state creep and the most commonly used is the power law stress dependence, which can be represented as [20, 42]:

$$\dot{\varepsilon}_s = A_1 \sigma^{n_1} \exp\left(\frac{\Delta H}{RT}\right) \qquad 2.33$$

where A_1 is a material constant, n_1 is the stress or power law exponent, R is the gas constant, and ΔH is the activation energy for the dominant creep mechanism. Such a power law represents the steady state creep very well at low stresses, but as the magnitude of the applied stress increases the stress exponent, n_1, no longer remains constant and increases with stress level. This is known as power law breakdown [20, 44]. Figure 2-10 illustrates this dependency of the creep mechanism on applied stress. The change in slope shows the transition from one creep mechanism to another. For solders, it is not uncommon to have more than one transition over the range of applied stresses [16]. Thus the modelling of secondary creep strain becomes challenging.

There has been a lot of research carried out to come up with a constitutive equation for steady state creep deformation, which can represent different kinds of mechanisms in both lead based and lead-free solder materials. For instance, Wiese *et al.* [45] studied the creep behaviour of Sn4.0Ag0.5Cu for both bulk solder and flip chip solder joints. Their study identified two kinds of creep mechanism for steady state deformation and which are attributed to climb controlled (low stress) and combined glide/climb (high stress) behaviour. This creep behaviour has been modelled with a double power law equation, as presented in Eq. (2.34) by Wiese *et al.* [45].

$$\dot{\varepsilon}_s = A_1 \exp\left(\frac{-Q_1}{RT}\right)\left(\frac{\sigma_e}{\sigma_c}\right)^{n_1} + A_2 \exp\left(\frac{-Q_2}{RT}\right)\left(\frac{\sigma_e}{\sigma_c}\right)^{n_2} \qquad 2.34$$

where A_1 and A_2 are constants, Q_1 and Q_2 are activation energies for the two different mechanisms of creep, σ_e is the equivalent stress, σ_c is the stress coefficient, and n_1 and n_2 are the stress exponents.

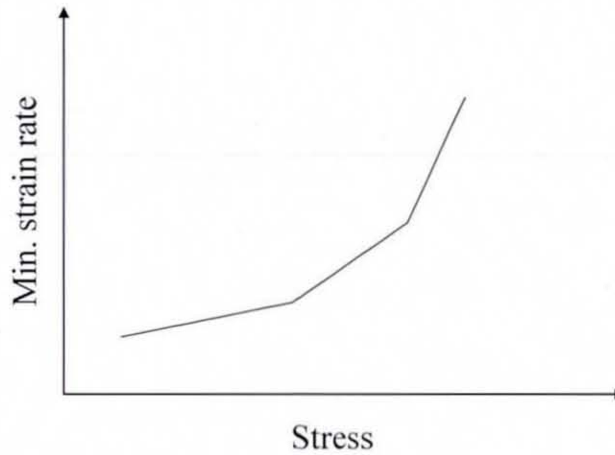


Fig. 2-10: Minimum (or steady state) creep rate vs. applied stress indicating changes in dominant mechanism

Similar research has been carried out by Schubert *et al.* [46] and Zang *et al.* [47], and both have identified two regions of stress-creep strain rate behaviour. Both modelled the steady state creep rate with a classical sine hyperbolic creep law, given as [34, 44, 48]:

$$\dot{\varepsilon}_s = B_1\left[\sinh(\beta\sigma)\right]^p \exp\left(\frac{-Q}{RT}\right) \qquad 2.35$$

where B_1 is a constant, β is the stress multiplier, p is the sinh law exponent, and Q is the activation energy. This creep law reduces to a power law in the low stress area ($\beta\sigma < 0.8$) [44] and to an exponential model in the high stress area ($\beta\sigma > 1.2$) [44]. The sine hyperbolic creep model has been shown to work well for most lead based and lead-free solder materials [20]; hence it has been widely used in reliability studies of solder joints due to creep damage.

2.4 Summary

Stress-strain properties play an important role in the design of any mechanical structure. The loading rate and temperature also have considerable effects on the stress-strain properties. In the case of solder materials, which operate under variable strain rates and extreme temperature conditions, viscoplastic and creep properties are important for the study of their reliability in electronic packaging. In addition the new lead-free solder materials, for which there is less material data available and a short history of practical applications, demand extensive material testing for different environmental conditions that are commensurate with the practical applications. Material data from testing can be represented using a constitutive equation to allow extensive reliability studies. The evaluation of viscoplastic properties for lead-free 95.5Sn3.8Ag0.7Cu solder will be discussed in chapter 6, while chapter 7 discusses the evaluation of creep properties for the same material. The parameters for the Johnson-Cook and hyperbolic sine law models are calculated based on the material test data, and later used in the finite element analyses which are presented in chapter 8.

3. Microstructure of Lead-Free Solder

This chapter reviews the microstructure of lead-free solders or solder joints and the effects of microstructure on the mechanical behaviour of solder joints. The review has been confined to SnAgCu or SnAg solder joints on Cu or Ni substrates to keep within the scope of this research.

3.1 Introduction

The theories of strength of materials, elasticity, and plasticity lose much of their power when the internal structure of the metal becomes an important consideration. Microstructures can no longer be considered to behave as a homogeneous medium. For example, metals operating at high temperatures may change their metallurgical structure with time. As the size of the component reduces the mechanical properties become more dependent on the microstructure, particularly when only a few grains are present over a critical area of the structure. For instance, electronic products have been miniaturised to meet the constant demand for compact and light weight, which in turn has resulted in smaller interconnecting joints. Therefore, in electronic packaging applications the microstructure inside a solder joint and at the interface between the solder joint and the substrates determines the mechanical properties of the solder joint. The microstructure of the solder joint is initially determined by the soldering process, and then by subsequent ageing and thermal cycling at the solid state [20]. The interfacial reaction between the solder and the substrate material forms an intermetallic compound (IMC), which affects wetting, joint strength, and reliability. The formation of IMC is desirable for good wetting and metallurgical bonding, but excessive interfacial reactions may degrade the solder joint integrity and reliability [16, 20]. Thus, the reviews on the microstructure of lead-free solders and the solder joints before the determination of its mechanical behaviours give the necessary parameters to be considered in the reflow soldering, and subsequent experiments and reliability study.

3.2 Microstructure of Lead-Free Solder

With the efforts of many researchers, several lead-free alternatives to conventional SnPb have been developed. Most of the proposed lead-free solders are tin (Sn)-rich,

and alloyed with other elements such as Ag, Cu, Zn, Bi, In and Sb. Among the binary eutectic lead-free alloys, SnAg, SnZn and SnCu are considered to be the better ones to replace tin-lead (SnPb). As for ternary alloys, those in the SnAgCu family have been most widely adopted. The SnAgCu lead-free solders are quite important, because they are generally recognised as the first choice for a lead-free solder due to their slightly lower melting temperature than SnAg and SnCu solders, and better fatigue and creep behaviour [49-51].

The equilibrium solidification of SnAgCu alloys near the ternary eutectic composition consists of three stages: primary, secondary, and tertiary, and involves the liquid, L and three solid phases, β-Sn, Ag_3Sn and Cu_6Sn_5. If the three solid phases are denoted generally as S1, S2 and S3, the primary stage is $L \Rightarrow L + S1$, and the temperature at which the primary solid S1 starts forming, is the liquidus temperature. S1 can be any of the three solid phases β-Sn, Ag_3Sn and Cu_6Sn_5, depending upon the composition of the alloy relative to the ternary eutectic composition. As the temperature decreases, the secondary solidification starts, $L \Rightarrow L + S1 + S2$, followed by a tertiary stage of the solidification, $L \Rightarrow S1 + S2 + S3$, at the ternary eutectic temperature (around 490 K for SnAgCu alloy) [20]. Figure 3-1 shows a typical lead-free solder microstructure composed of β-Sn dendrites in the volume fraction ranging between 20 and 80 %. These dendrites are surrounded by eutectic compound, which consists of β-Sn matrix, Ag_3Sn and Cu_6Sn_5 as shown in Fig. 3-1 [13, 49, 51, 52].

3.2.1 Sn Dendrites and Grains

The dendrites of the β-Sn phase are the result of primary solidification in a Sn rich alloy. The presence of β-Sn dendrites in eutectic SnAg solder joints are due to (a) the large undercooling below the eutectic temperature prior to nucleation of the formation of the β-Sn phase, and (b) the shift of the solder composition away from the eutectic as a result of dissolution of Cu from the PCB or component terminations into the solder [20, 53, 54]. Due to the lower nucleation temperature of β-Sn than the eutectic temperature, the original composition of SnAgCu or SnAg no longer represents the eutectic composition at the lowered solidification temperature. The variability in the alloy composition during soldering processes was studied by NEMI [6] for a SnAgCu ternary alloy. The equilibrium phase diagrams are presented in Fig. 3-2 at different

isothermal sections for Sn3.9Ag0.6Cu. The size of the oval indicates variability in alloy composition, and therefore the joint composition would be different from the composition of the solder paste. This results in a microstructure consisting of primary β-Sn phase and eutectic mixture of Ag_3Sn, Cu_6Sn_5 and the β-Sn phase [20]. As the cooling rate increases, the undercooling increases, which results in a larger volume fraction of the β-Sn dendrites, and a smaller fraction of the eutectic lamellar region. The lamellar spacing also becomes finer with the increased cooling rate [54].

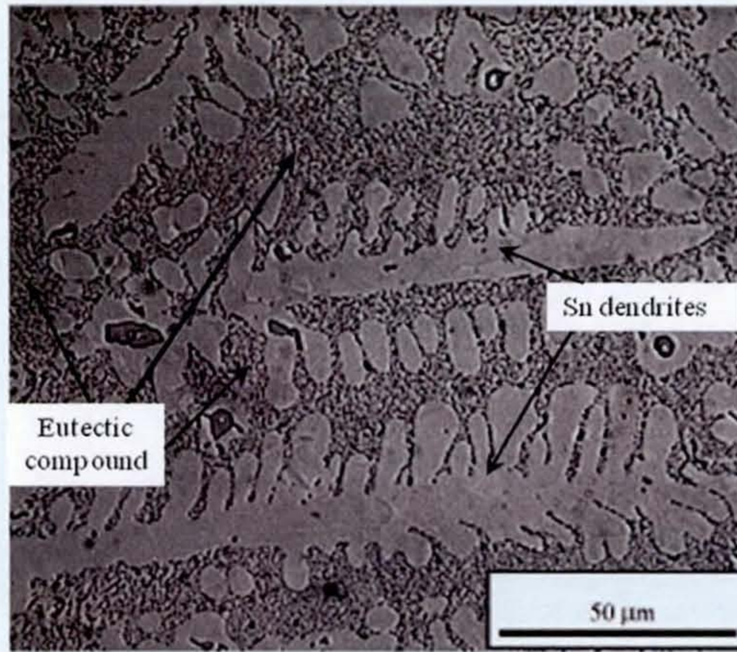


Fig. 3-1: Typical microstructure of Sn-Ag-Cu solders [55]

Diffusion of copper from the substrate is another reason for the nucleation of β-Sn dendrites in the solder joint by shifting the solder composition from its eutectic point. A study of eutectic SnAgCu BGA solder joints between two Cu pads, between a Cu pad and an Au-Ni(P) pad and between two Au-Ni(P) pads, resulted in a higher volume density and finer spacing of the β-Sn dendrites in the solder joints bounded by two Au-Ni(P) pads [56]. Also, a comparative study of microstructure between Sn3.5Ag0.5Cu and Sn3.5Ag0.5Ni solder joints showed a higher density of β-Sn dendrites and with a finer spacing in the Ni-containing solder joints [57].

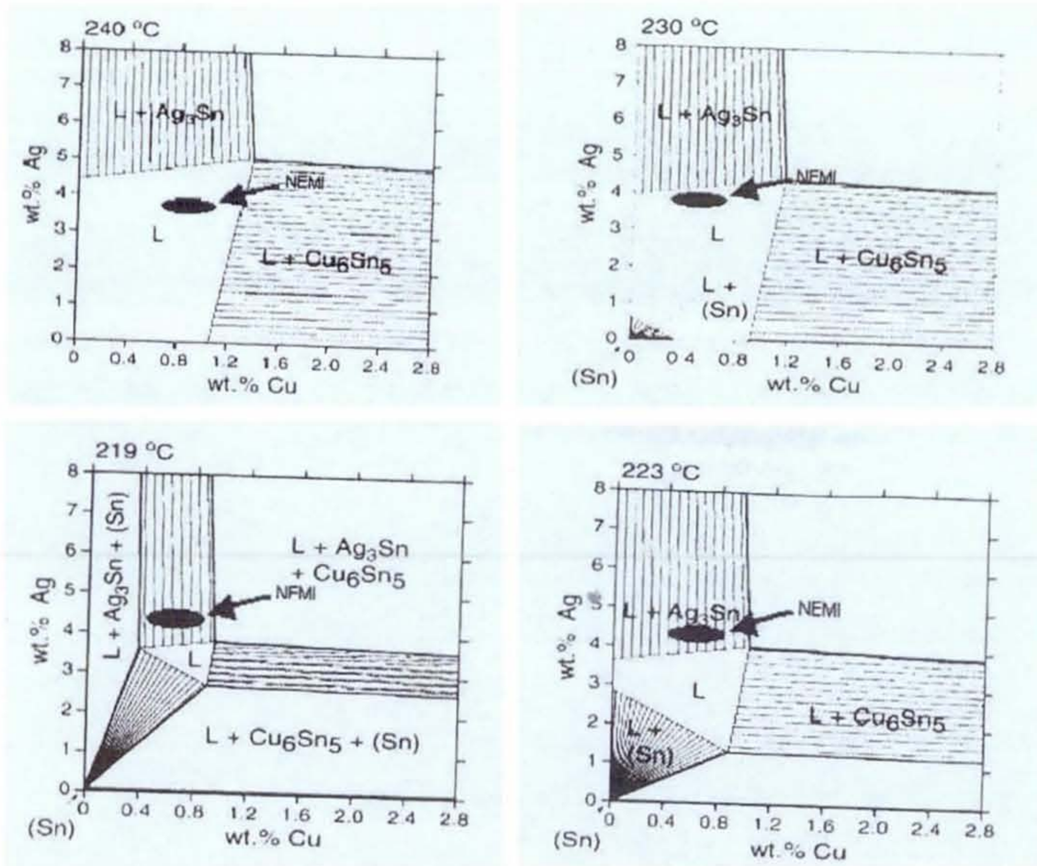


Fig. 3-2: Isothermal sections of the Sn3.9Ag0.9Cu system at several temperatures [6]

Microstructural investigations of lead-free solders have also showed the formation of Sn grains in the solder joints [58-60]. Sn-dendrites are the main constituents of these Sn grains. Figure 3-3(a) exhibits Sn-dendrites formed in a solder joint undercooled 34°C below the eutectic temperature before solidifying. A careful observation of the Sn-dendrites showed that the direction of the dendrites is not uniform across the solder joint. This results in the formation of Sn grains in the solder joints which are shown in Fig. 3-3 (b) with cross-polarisation. The size and orientation of the Sn grains in the SnAgCu and Sn-Ag solder joints have been studied by varying both composition and cooling rate. This study showed that Sn grain sizes in SnAgCu solder joints tend to increase with increasing Cu content. Similarly, an increased Sn grain size has been observed for Sn-Ag solder at an increased cooling rate [58].

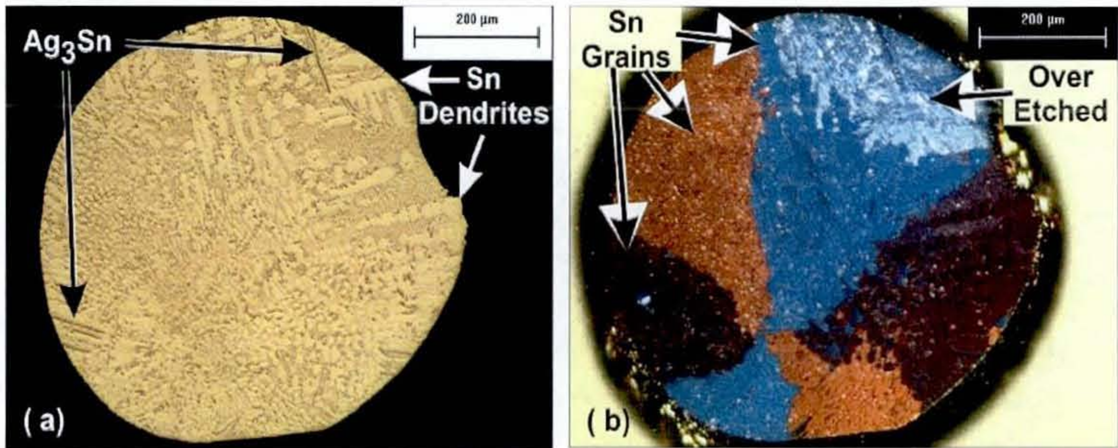


Fig. 3-3: Sn3.9Ag0.6Cu cooled at a rate of 1 K/sec from a temperature of 523 K.: (a) bright-field image and (b) cross-polarised light image [58]

3.2.2 Ag3Sn Plates

Plates of Ag_3Sn IMC, are formed in solder joints with minimal undercooling, while the β-Sn phase requires undercooling of 15 to 30 °C for its nucleation [61]. During the solidification process, the Ag_3Sn therefore nucleates first and may grow into large plates before the β-Sn matrix is solidified. For example, Sn3.8Ag0.7Cu BGA solder balls solidified at a very slow cooling rate of 0.02 K/s have been shown to result in large Ag_3Sn plates [20]. These large Ag_3Sn plates create adverse effects on the ductility and fatigue resistance of the solder joint.

The nucleation of large Ag_3Sn plates has been reported to depend on three factors: (a) Ag content, (b) cooling rate, and (c) Cu content [20]. A high Ag content promotes the Ag_3Sn formation. Thus the recommended Ag content in the solder alloy is less than 3 % by wt. A slower cooling rate gives time for Ag_3Sn plates to grow, which requires the long-range diffusion of Ag and Sn atoms in the liquid phase. Therefore, to avoid large Ag_3Sn plates in surface mount solder joints, a cooling rate in the range of 0.83 to 2 K/s is used [62]. A high Cu content in the solder can also promote the formation of large Ag_3Sn plates in the solder joint. It was reported that the percentage of the large Ag_3Sn plates increased with increased Cu content in the microstructures of Sn3.8Ag0.7Cu, Sn3.8Ag0.35Cu, and Sn3.5Ag [62]. Some studies also reported large Ag_3Sn plates adjacent to the Cu substrate, where Cu atoms will have dissolved into the molten solder joint [63]. The nucleation of Ag_3Sn plates in SnAgCu solder joints were studied by Lehman et al. [58] for a varying Cu content, but a constant Ag content (3.9

%) and cooling rate of 1 K/s. It is apparent from Fig. 3-4 that precipitates (Ag_3Sn and/or Cu_6Sn_5) can constitute a significant volume fraction of the solidified alloy. This study clearly showed that the average composition of the remaining volume of such alloys differs substantially from the average composition of the entire alloy as a significant amount of Ag or Cu has been removed from the remaining volume. The quantity of Ag_3Sn precipitate increased with increased Cu content until 0.59 %, but then decreased for a 0.86 % Cu content due to the increased formation of Cu_6Sn_5. This was explained by Moon et al. [64] through the consideration of liquidus surfaces of the SnAgCu system.

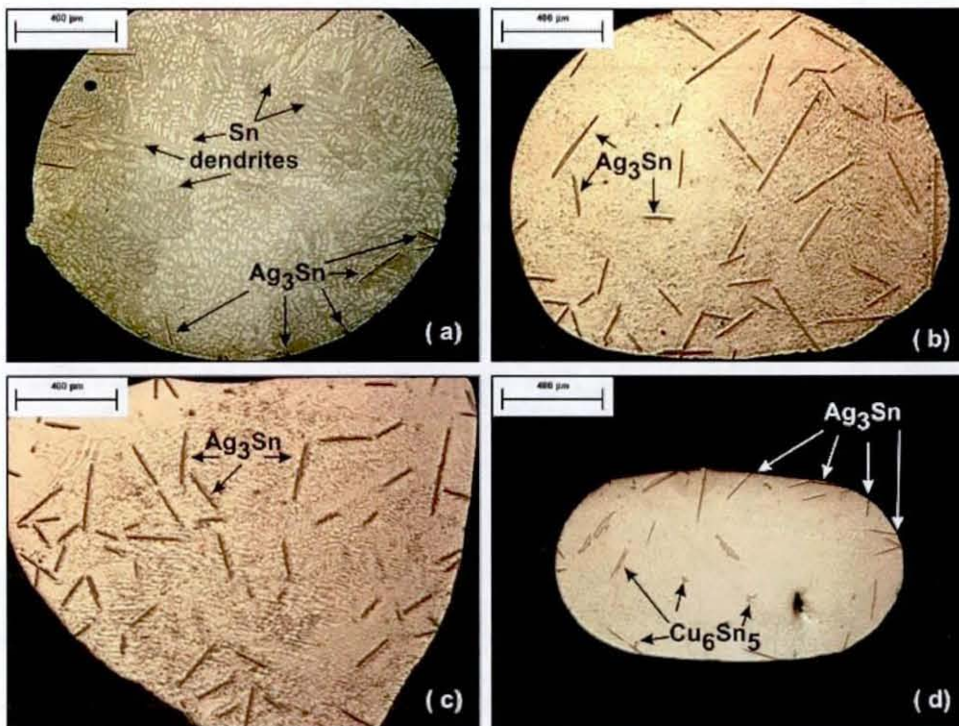


Fig. 3-4: Optical micrographs (bright-field images) of cross sections of SnAgCu alloys of various Cu concentrations: (a) Sn3.9Ag; (b) Sn3.9Ag0.27Cu; (c) Sn3.9Ag0.59Cu; and (d) Sn3.9Ag0.86Cu [58]

3.2.3 Cu-Sn Intermetallic Compounds and their Growth

For SnAgCu solders, the addition of Cu results in formation of Cu_6Sn_5 intermetallic compound (IMC) in the solder joint. These IMCs are also formed at the interface between tin based solders and copper substrates. During the soldering process Cu atoms from the substrate diffuse in Sn and forming ternary Cu_6Sn_5 at metallization interfaces. This is termed as intermetallic layer and it can also be found at the interface between SnAg solder and copper substrates. In a eutectic SnAgCu solder joint, the

Cu_6Sn_5 phase appears as block shaped particles, while Ag_3Sn forms as elongated plates. The amount of Cu_6Sn_5 particles in eutectic Sn-Ag and SnAgCu solder joints on Cu substrates increases with increased reflow time and reflow temperature, because of the increased Cu dissolution. Figure 3-5 shows the formation of Cu_6Sn_5 IMCs having a hexagonal outline with a hollow or pipe like centre in Sn3.9Ag1.4Cu solder joints formed at cooling rate of 0.1 K/s. These IMCs are surrounded by Sn-dendrites [9, 54, 58, 65].

The intermetallic layers formed at the interface between a solder joint and substrate are essential to achieving good bonding between them. If the substrate material is copper, a layer of Cu_6Sn_5 is formed, while a Ni_3Sn_4 layer is formed on a nickel substrate with both SnAg and SnAgCu solders. When Cu is present in the solder, a complicated interfacial product is formed due to the presence of Sn, Cu and Ni. The intermetallic layer is formed due to the interaction of molten solder and solid substrate material. It is less certain if the other stable tin-copper IMC, $\varepsilon-$ phase (Cu_3Sn), forms or not, at the interface between the Cu substrate and η – phase during soldering, because the $\varepsilon-$ phase IMC is usually very thin and identification is difficult with a scanning electron microscope (SEM) [20]. A study of IMC showed that $\varepsilon-$ phase was formed in the solder joint formed at 598 K. In addition, $\varepsilon-$ phase of IMC is also formed during solid state thermal aging of solder joints [20].

The solid state growth of intermetallic layers is diffusion controlled. Generally the growth of this layer takes place during thermal aging. Several studies have been carried out to understand the parameters affecting the intermetallic layer growth and have demonstrated that the layer thickness, X_{imc}, can be modelled with a power law as a function of time and temperature [9, 20, 66, 67]:

$$X_{imc}(t,T) = k_{imc}(t)^{b} \tag{3.1}$$

where t is time, T is temperature, $k_{imc} = k_0 \exp\left(\frac{-Q}{RT}\right)$ and b is a time exponent. The growth mechanism can be distinguished based on the value of the time exponent, b. The $\varepsilon-$ phase IMC Cu_3Sn is also formed during growth of the intermetallic layer due to thermal aging wherein diffusion of Sn and/or Cu through the intermetallic layer

takes place. Choi *et al.* [68] studied the formation of Cu_3Sn with isothermal aging between 258 and 423 K for 1000 cycles. The thermal aging resulted in the formation of ε – phase (Cu_3Sn, Fig. 3.6) between the Cu_6Sn_5 layer and the copper substrate due the diffusion of Cu and/or Sn at elevated temperature [69]. Generally the thickness of the initially formed intermetallic layer (Cu_6Sn_5) varies from 1 to a few μm, depending on the temperature and duration of the soldering process [69].

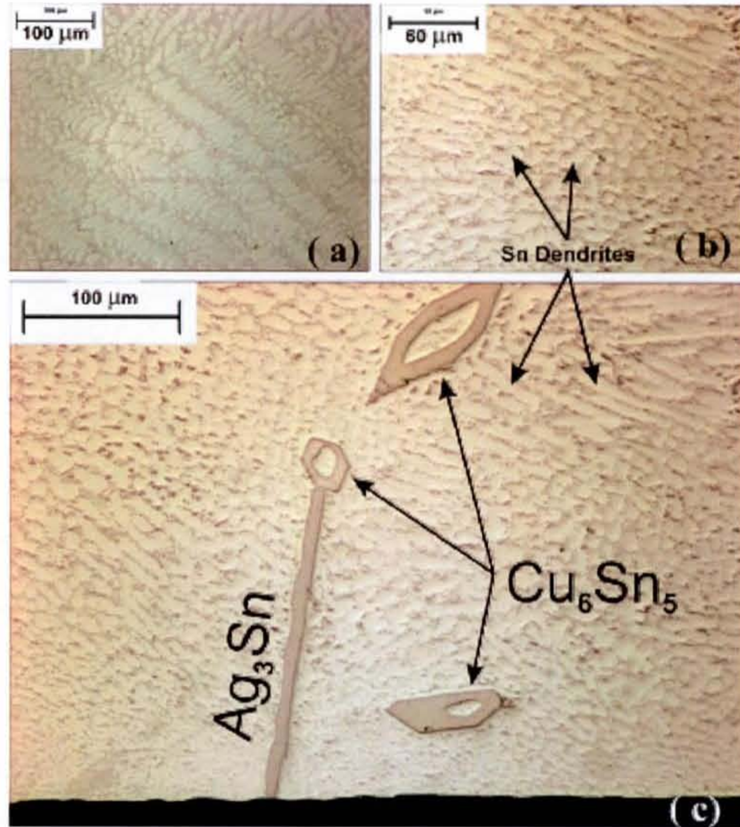


Fig. 3-5: Optical micrographs (bright-field image) of near-eutectic SnAgCu samples: (a) an ingot as cooled in the arc melter, (b) a sample cooled at a rate of 0.1K/s, and (c) a view of a larger region of the sample of (b) [58]

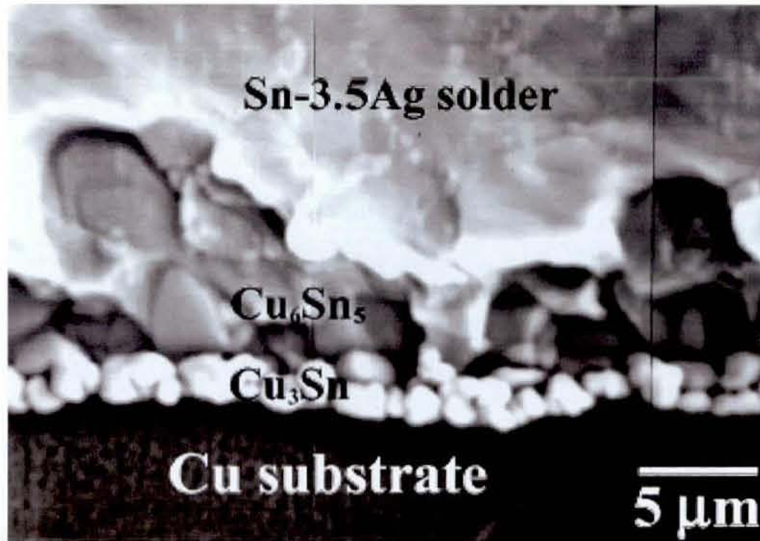


Fig. 3-6: The interfacial IMC layer developed during 1,000 cycles for Sn3.5Ag joint [69]

3.3 Influence of Microstructure on Lead-Free Solder Material Properties

So far the microstructure and intermetallics in lead-free solder joints have been discussed. Also discussed are the different factors which affect the microstructure evolution and the intermetallic layer growth. Due to miniaturisation trends in electronic packaging, the average size of the solder joints is diminishing and the material properties are increasingly influenced by the microstructure. The presence of the intermetallic layer between the substrate and solder also has a significant influence on the material properties of solder joints. Therefore, this section deals with the influence of both microstructure and intermetallic layer on solder material properties.

3.3.1 Influence of Microstructure

The mechanical and physical properties of solder joints significantly depend on the microstructure. Most of the lead-free alternatives are Sn-rich and hence physical, chemical and mechanical properties are heavily influenced by the properties of pure tin (Sn). Tin exhibits anisotropic behaviour with variations in properties between crystallographic directions. At room temperature the body centred tetragonal structure of tin provides ample opportunity for this. For instance, the coefficient of thermal expansion (CTE) varies by a factor of two according to the direction in which it is

measured, and the Young's modulus may experience a threefold variation. Significant stresses may develop at grain boundaries, according to the orientation of the neighbouring grains [19, 70, 71]. This characteristic of tin in turn affects the properties of solder alloys and solder joints. As discussed in the previous section, the microstructure of the solder joints mainly consists of Sn-dendrites, eutectic compound and intermetallics. The size of the Sn-dendrites, size and number of equilibrium precipitates (e.g. Ag_3Sn and Cu_6Sn_5 in the eutectic compound of lead-free solder) can affect the mechanical response of the solder joint [72]. Sundelin *et al.* [55] conducted a study to evaluate the effect of Sn-dendrites and eutectic compound on the shear strength of SnAgCu (SAC) solder joints on Cu pads with an organic solderability preservative (OSP) surface finish. The test matrix of mechanical tests included three different SnAgCu pastes with compositions of 96.5Sn3.0Ag0.5Cu, 95.5Sn-3.8Cu-0.7Cu, and 95.5Sn4.0Ag0.5Cu. These compositions are hypoeutectic, eutectic, and hypereutectic, respectively. Figure 3-7 shows a comparison of shear strengths between these three different SAC alloys and eutectic Sn-Pb solder joints. The eutectic SAC joints exhibited higher shear strengths as reflowed, while the shear strength after aging was nearly the same. The important reason for the different shear strength of the solder joints is the variation in the microstructure due to the change in compositions of the solder pastes. Figure 3-8 illustrates the microstructure of the three different compositions of SAC solder. The main difference between the eutectic joints and hypoeutectic joints is the total amount of Ag_3Sn dispersion is higher in the eutectic joints (Fig. 3-8 (a) and (b)). In addition, the appearance of dendritic (β-Sn) formation was clearly lower in the hypoeutectic joints than in the eutectic SnAgCu joints. For the hypereutectic solder joints, the Ag_3Sn dispersion was very coarse in the as reflowed state (Fig. 3-8(c)). The average diameter of the dispersions varied in this case between 0.5 μm and 5 μm from sample to sample. The amount of the Cu_6Sn_5 phase in the hypoeutectic, eutectic and hypereutectic solder joints were at the same level as in the bulk solder. Thus, this study indicates that the microstructure of the solder joints is initially different and hence results in the influence on the material behaviour. However, after thermal aging in spite of different composition of the joints, the microstructure of the joints becomes similar and therefore does not influence the material behaviour.

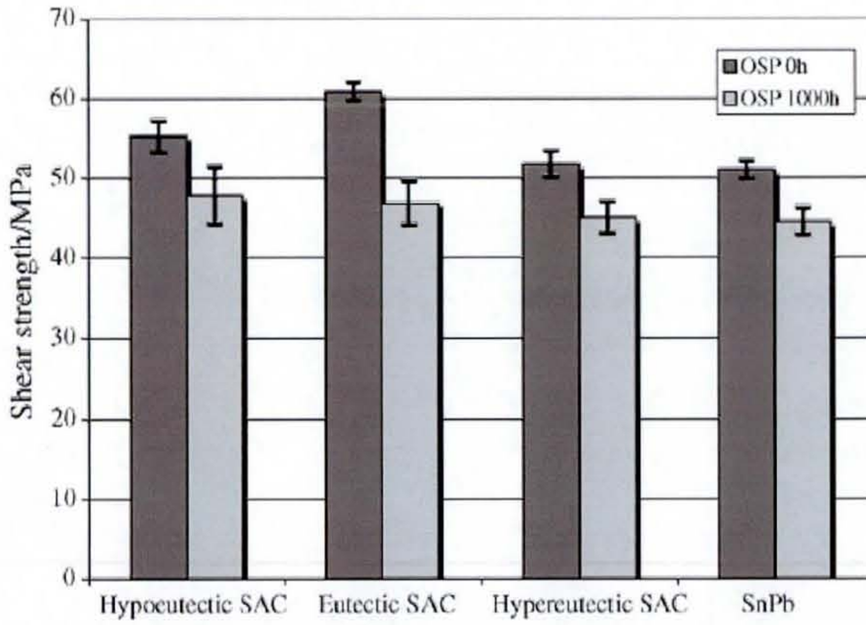


Fig. 3-7: The shear strengths of as reflowed and aged solder joints on OSP finished Cu pads [55]

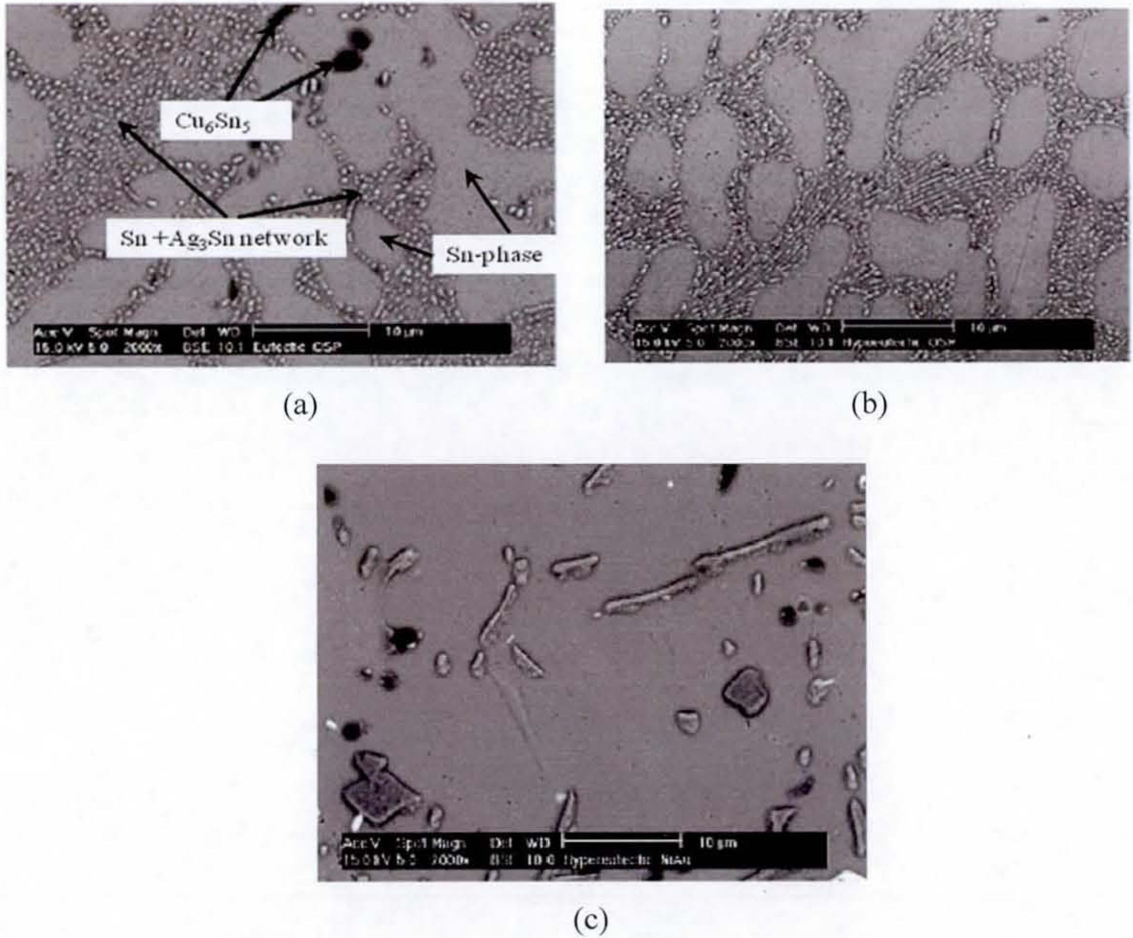


Fig. 3-8: Microstructure of (a) Eutectic SnAgCu; (b) hypoeutectic SnAgCu; (c) hypereutectic SnAgCu, on Cu pads with an OSP surface finish [55]

The mechanical properties of solder joints are also affected by the number and orientation of the Sn-grains in them. Bieler *et al.* [60] examined the thermo-mechanical response of SAC solder joints as a function of Sn-grain size and orientation. From this study, solder balls with Sn grains of a particular orientation (a-axis perpendicular to the substrate) were observed to fail before neighbouring balls with different orientations. This results from the fact that the coefficient of thermal expansion of Sn along the a-axis is half the value along the c-axis; joints observed to be damaged had maximum mismatch in the coefficient of thermal expansion between solder and substrate at the joint interface [59, 60, 72].

3.3.2 Mechanical Influence of the Intermetallic Layer

Apart from the microstructure, the mechanical responses of lead-free solder joints are also influenced by the presence of the intermetallic layer(s) between the bulk of the solder joint and the substrate metallisation. The intermetallic layer formed is brittle in nature compared to the solder joint and it grows with thermal aging. There exists a critical thickness of IMC layer at which the shear strength is a maximum. This critical thickness of the IMC is approximately 1.2 μm, corresponding to a reflow time of approximately 60 s for pure Sn and approximately 15 s for Cu-containing solders [20]. Reflow time is the time above the melting temperature of the solder alloy during reflow soldering. Figure 3-9 presents the typical profile used in reflow soldering. As the reflow time increases, the higher diffusion of the Cu from the substrate results in the increased layer thickness, and shear strength increases with increased Cu_6Sn_5 precipitates in the Sn-matrix. When the interfacial thickness grows beyond the critical value during soldering, the diffusion of Cu into the bulk solder joint is restricted by the IMC layer, hence decreasing the shear strength of the joint. When the IMC layer thickness is thinner than the critical thickness, shear failure occurs inside the bulk solder. Thus, the reflow time place an important role in the IMC thickness. However, attaining above mentioned required reflow time (15 s) is difficult in the actual electronic packaging. Therefore, IPC came up with IPC/JEDEC J-STD-20C standards for reflow soldering with reflow time of 120 – 150 seconds.

The intermetallic layer grows with thermal aging during which the Cu_3Sn layer is also formed. During the formation of Cu_3Sn the mass imbalance, due to the different

diffusion rates of Sn and Cu, induces vacancies or kirkendall voids in the vicinity of the interface of the solder joint. These vacancies accumulate to form a line of voids that severely diminishes mechanical strengh. Thus, the brittle nature of the intermetallic layer along with porosity often leads to reduced mechanical strength of the solder joint at the interface [20, 73]. The mode of failure during thermo-mechanical fatigue of electronic assemblies is usually either delamination at the interface between the solder joint and intermetallic layer or between intermetallic layer and substrate. The brittle intermetallic layer causes localised softening near the interface between solder joint and the layer, making it an easy location for crack initiation and propagation to occur [73]. Figure 3-10 shows an example of the initiation of a crack between voids during thermal cycling of a lead-free interconnection.

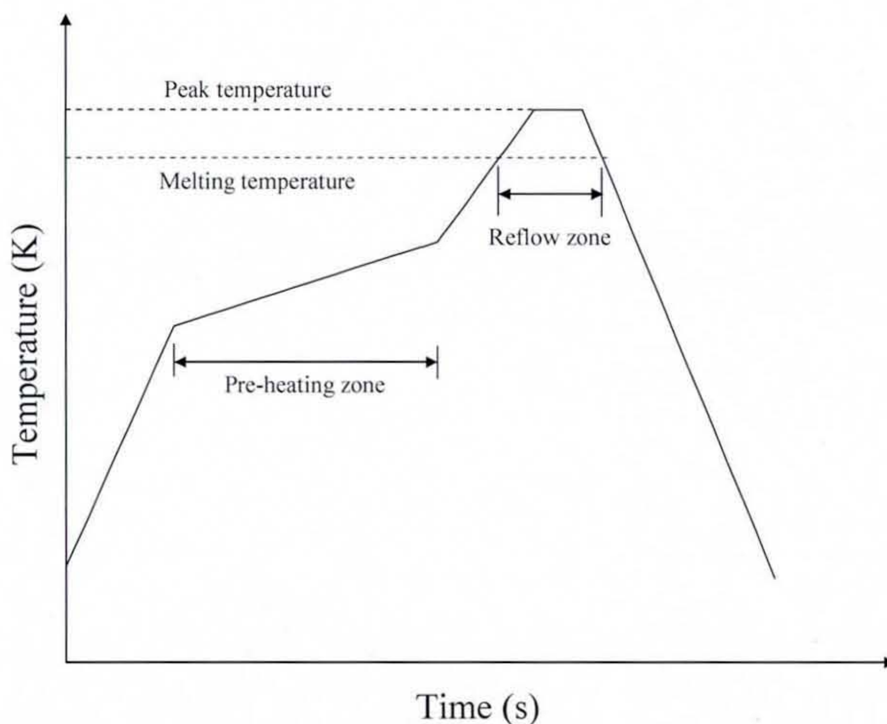


Fig. 3-9: Typical profile used in reflow soldering

Fig. 3-10: Crack initiation and void formation due to thermo-mechanical fatigue [73]

3.4 Summary

The major constituents of lead-free solder joints' microstructure are β-Sn dendrite, intermetallic and eutectic compound. Eutectic compound consists of β-Sn matrix, Ag_3Sn and Cu_6Sn_5. The proportions of β-Sn dendrites, intermetallic compound and eutectic compound in the solder joints depends on the composition of the solder, substrate material, and the reflow time, peak temperature and the cooling rate. In addition, Sn grains are also formed during the solidification of the solder joints, which have anisotropic mechanical properties. Such a complex microstructure has a prominent influence on the mechanical properties of the solder joints. The intermetallic layer developed at the interfaces between solder joints and substrate metallisations grows with thermal aging, resulting in formation of voids. This causes the interface to become brittle and weak, and therefore become a favoured location for crack initiation and propagation during operation.

4. Solder Joint Reliability

This chapter presents a review on the reliability of solder joints in electronic products considering its various operating conditions. The reasons for fatigue failure of solder joints are discussed in brief along with the experimental tests used for reliability assessment. The review also includes the different approaches for fatigue life estimation that have been used and the use of finite element analysis (FEA) as part of them.

4.1 Introduction

Even though emerging new technologies may offer a number of advantages, ensuring the long-term reliability of electronic products, utilising these technologies, is a challenging task. Electronic products are used in various applications ranging from entertainment to satellite applications. Electronic devices used in a satellite may see millions of thermal excursions over a period of years in space as the device powers up and down, and as the ambient temperature is affected by the space craft orientation with respect to the sun [1]. Military equipments may be stored for long periods in desert or arctic conditions (or alternating between the two), can be subjected to severe mechanical stresses during field commissioning, and then be used in earnest in the battlefield scenario, again under the most environmentally and mechanically difficult conditions. Electronic circuitry has been used in household goods for years. Consumer awareness and ferocious competition between suppliers mean that manufacturers of such items as televisions and washing machines are now being forced to offer ever-increasing warranty periods on goods that are the subject of almost constant use, stringent duty cycles, and minimal respect from the user. The electronic systems in cars also function under severe environmental conditions. With such a wide range of applications, ensuring reliability of electronic products is of the utmost importance.

In a broad sense reliability is defined as the ability of a product to function under given conditions and for a specified period of time without exceeding acceptable failure levels. In practice reliability is application-specific, and is traditionally established through the acquisition of failure distributions under certain test conditions, followed

by a careful extrapolation of failure data to service conditions [74]. Reliability in electronic assemblies requires a definitive design effort that has to be carried out concurrently with other design functions during the developmental phase of the product [75]. There is a misconception in some parts of the industry that quality manufacturing is all that is required to assure reliability of an electronic assembly [75]. Of course, consistent high-quality manufacturing is essential, but it implies that Design for Manufacturability (DfM), Design for Assembly (DfA), Design for Testability (DfT), etc. is a necessary prerequisite to assure reliability of the product. However, only a Design for Reliability (DfR) approach can assure that the designed system, if manufactured to a good quality standard, will be reliable in performing its intended function [75].

The solder joints which are used in electronic packaging are a primary location for reliability hazards due to the severe operating conditions of electronic products. In addition, solder joints also provide structural integrity to the assembly and often serve critical heat transfer functions as well. With its primary function of providing electrical connection, a single solder joint failure generally results in the malfunctioning or failure of the electronic product to perform its intended function. The introduction of new lead-free solders has also increased concerns over reliability, due to the shorter history of their industrial application, and material models are not as well developed as for the traditional SnPb solders. Hence, it is important to understand the reliability of solder joints in microelectronic applications and the various aspects which affect their reliability, including the new lead-free solders. This chapter, therefore, reviews various reliability prediction models currently used in the microelectronic industries.

4.2 Solder Joint Failure

The prominent failure concerns for solder joints are thermal cycling durability, creep deformation, mechanical cycling and vibration durability, solder joint ageing, intermetallic growth, and electro and electrochemical migration [20]. Understanding the physics of these causes of failure aids reliability evaluation and improvement. Some of these concerns such as solder joint ageing, intermetallic growth and electrochemical migration have been discussed in chapter 3. In this section solder joint

failures relating only to thermal cycling and creep are discussed as they are the focus of the current research study.

4.2.1 Thermal Fatigue Failure of Solder Joints

Thermal stresses in a structure can be developed due to various reasons. For instance, a body restricted from its free expansion due to a change in the uniform distribution of temperature experiences thermal stresses as well as a component subjected to a non-uniform temperature distribution. Thermal stresses can also be induced due to a mismatch in the coefficient of thermal expansion (CTE) between different components of the assembly. However, in electronic assemblies, solder joints generally experience thermal stresses due to the combined effects of non-uniform temperature distributions in the package and a mismatch in CTE between the component and substrate material [29, 76, 77]. A non-uniform distribution of temperature results from the differences in temperature between the constituents of the assembly during its operation. Most often the constituents of electronic assemblies are a variety of different materials and hence there is a mismatch in the material properties. For example, surface mount chip resistors are principally made up of alumina (Al_2O_3) and connected to a FR4 substrate (PCB). This global mismatch in coefficients of thermal expansion (CTEs) between component and substrate results in thermal stresses and strains in the solder joint during thermal excursions. The CTE mismatch typically ranges from 2 ppm/K for CTE-tailored high reliability assemblies to 14 ppm/K for ceramic components on a FR4 PCB.

These thermal excursions are a result of the operating conditions of the electronic components. In operation, the extremes of environmental temperature variation in aerospace systems for example can be between 218 K and 398 K. In testing and simulation this range of temperatures is applied as a thermal cycle wherein the temperature distribution across the assembly is assumed to be uniform. The assembly may also be subjected to temperature excursions during power on and off, variations in power dissipation in CPUs etc. which is called power cycling wherein the temperature distribution is non-uniform. These cyclic temperature excursions result in cyclic stresses and strains in the solder joints and the repetition of such cyclic strains can result in fatigue failure of the solder joints. In through hole (TH) devices, the strain

due to the temperature changes was generally accommodated by the flexibility of their leads and such failures were rare [29]. However, with the advent of surface mount devices, where the solder joints are very small and there is little compliance between the component and board, the solder joints have to accommodate the plastic deformation taking place in service for structural integrity [4].

Consider an example of a Ceramic Chip Carrier (CCC) mounted on a PCB, as shown in Fig. 4-1(a). In such a assembly the component and substrate are fairly rigid and the the shear strain range, $\Delta\gamma$, in the solder joint due to the change in the temperature of the assembly can be approximated as:

$$\Delta\gamma = \frac{L\Delta\alpha}{h}(T - T_o) \qquad 4.1$$

where L is the half distance between the two most extreme solder joints, $\Delta\alpha$ is the difference between PCB and CCC thermal expansion coefficients, h is stand-off height, T is the temperature of the assembly, T_o is the stress free state temperature (reference temperature). The stress free state of the chip carrier assembly, when the temperature of the assembly is T_o, is shown in Fig. 4-1(a). As the temperature of the assembly increases above T_o, the solder joints shear due to the greater thermal growth of the PCB material, which is illustrated in Fig. 4-1 (b). Figure 4-1(c) illustrates the shearing of the solder joint in the opposite direction due to a decrease in the assembly temperature T below T_o. Thus, repeated changes in the assembly temperature results in cyclic shear stresses and strains in the solder joints, which in turn are responsible for their fatigue failure.

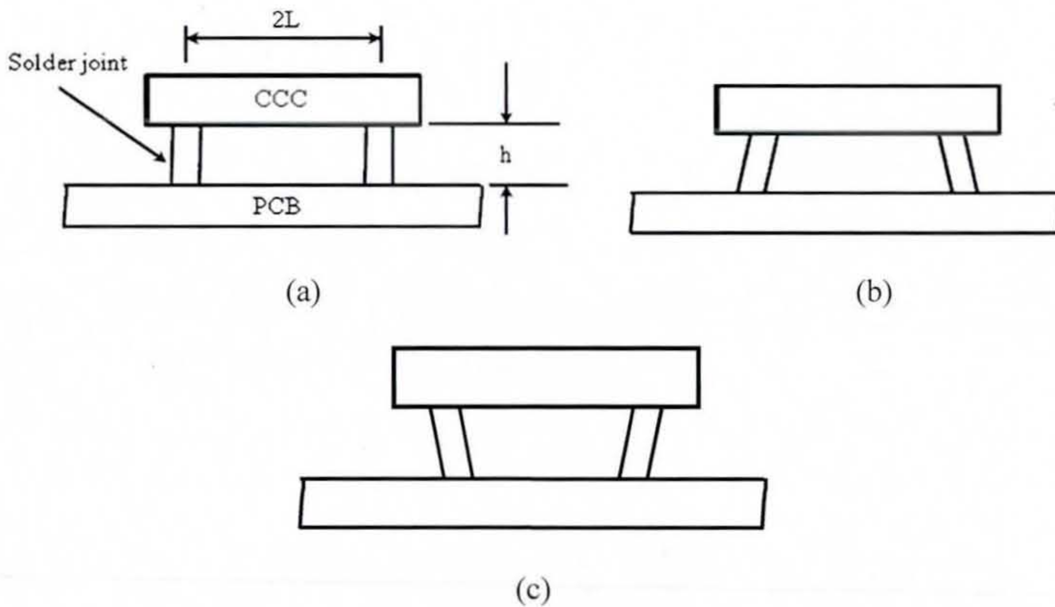


Fig. 4-1: Effect of thermal excursions on ceramic chip carrier solder joint (a) zero strain; (b) elevated temperature ($T > T_o$); and (c) reduced temperature ($T < T_o$)

4.2.2 Creep and Thermo-Mechanical Fatigue in Solder Joint

Sustained loads raise the spectre of time-dependent failure mechanisms involving the phenomenon known as creep. Creep is also a temperature dependent phenomenon and the temperature at which creep typically becomes active in a metal is approximately $0.4T_h$ [42]. The operating temperature extremes are between $0.45T_h$ and $0.81T_h$ for most lead-free solders. As a consequence, creep strain is probably the most important time-dependent damage accrual mechanism; under prolonged thermal loading conditions the solder joints of leadless parts can be expected to undergo significant levels of strain due to creep. The accrual of creep deformation in the solder joints eventually results in their ductility exhaustion. Thus, temperature variations, in combination with a thermal expansion mismatch between the component and substrate, can result in fatigue for which the creep becomes a primary contributor to the solder joint deformation; this condition is referred to as thermo-mechanical fatigue (TMF). The creep induced strain has the same damaging effect as immediately induced plastic strain [9, 20], and must therefore be added to any plastic strain to evaluate the total damage accrued during operation. The sum of these plastic and creep strains is the inelastic or permanent strain. Therefore, the total strain ε can be written as:

$$\varepsilon = \varepsilon_e + \varepsilon_{in} \quad 4.2$$

where:

$$\varepsilon_{in} = \varepsilon_p + \varepsilon_{cr} \quad 4.3$$

where ε_e, ε_p, ε_{cr} and ε_{in} are the elastic, plastic, creep and inelastic strains respectively. As discussed in Chapter 2, creep curves have three distinct stages: primary or transient, secondary or steady state and tertiary. It is common practise to characterise the creep response of solder joints solely with steady state constitutive equations. The constitutive equations discussed in section 2.3.2 are commonly used for steady state creep modelling of solder joints.

4.3 Reliability Tests

So far discussions have been confined to reliability and different reliability concerns in solder joints. A proper understanding of reliability of the solder joints is essential for the good design of electronic products and their reliability assessment. It is often difficult to improve the reliability of an electronic product after it has been released on to the market, so as much effort as possible must be exerted to design units that are inherently reliable. There are a number of standard experimental tests which are typically used to assess the reliability of products before release to the market [78, 79]. However, assessing the reliability of electronic packages based on real service conditions is time-consuming. Therefore, accelerated testing becomes more important and is the focus of intensive research recently driven by demands of the short-time-to-market and low cost. However, highly accelerated tests have a high potential to produce misleading results because such tests may not activate the failure mechanism that plays a leading role in the application environment [20]. Thus, it is important to consider the solder joint failure mechanisms and material properties while designing accelerated tests. In this section, the accelerating tests which are relevant to the above discussed failure mechanisms are presented.

As discussed earlier, thermal and power cycling are the two types of thermal excursions occurring in service environments. Therefore, accelerated thermal and power cycling tests are used in reliability assessments. The accelerated thermal cycling test is the most popular approach to estimate the expected lifetime or the expected failure rate of solder joints in a given environment. In a thermal cycling test, the

specimen is subjected to a temperature-time profile, usually between two temperature extremes. A typical thermal cycle is shown in Fig. 4-2. At each temperature extreme, the specimen is held for a certain dwell time and the temperature transfer is accomplished by a controlled ramp rate. The creep strain accumulation during these cycles depends on both the ramp rate and dwell time [20, 80]. For instance, during a rapid ramp between two extreme dwell temperatures, there is less time for creep deformation to occur. On the other hand a slow ramp rate increases the opportunity for creep deformation. Similarly, longer dwell time at the extremes of temperature, especially at the maximum cycle temperature (T_{max}), results in increased creep strain accumulation. Therefore, in the selection of a thermal history either for accelerated testing or for finite element modelling ramp rate and dwell time are important.

In accelerated tests for power cycling, the specimen is subjected to an electrical load, thus producing heat resembling real operation. In thermal cycling, only strains due to CTE mismatches are accounted for. However in power cycling, strain due to the temperature difference between component and substrate is also accounted. Basically, the same principles as those used in thermal cycling tests apply in power cycling tests. There are limitations in the achievable temperature extremes in power cycling tests, since the electrical load that can be applied is limited and thus the temperature swing is restricted by the equilibrium of heat dissipation and transformation of electrical energy to heat.

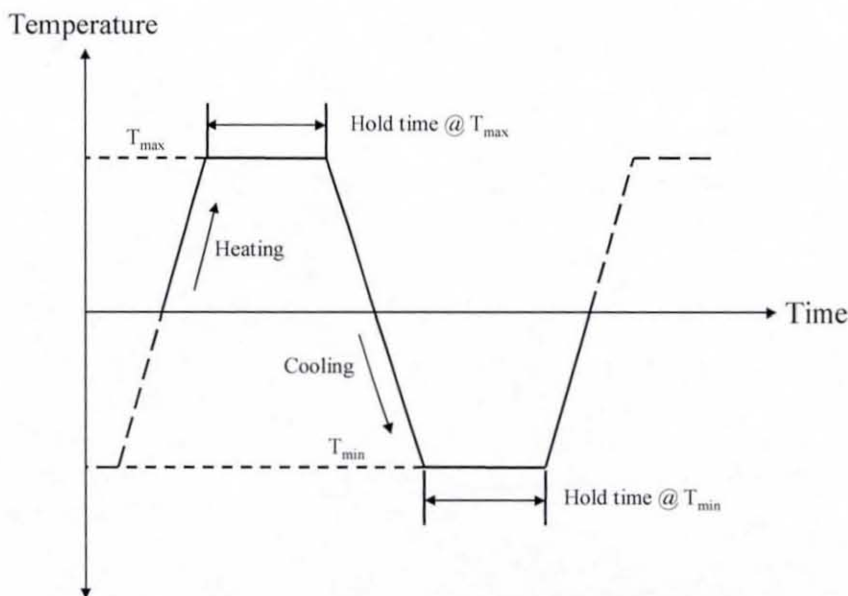


Fig. 4-2: Typical temperature cycle during accelerated testing

4.4 Fatigue Life Prediction Models

For high density electronic products, it becomes very important to assure the reliability of the resulting smaller solder joints. Most of the time solder joint failures are due to TMF. Even though accelerated tests can predict the reliability of the solder joints, these tests take a long time. For example, IPC-SM-785 proposed 14600 one-hour thermal cycle test between 0 and 100 °C for a leadless electronic assembly requires over 600 days to complete [79, 81]. Even the 6000 failure-free cycles proposed by IPC-9701 mean 250 days, i.e. more than 8 months [81, 82]. Therefore, fatigue life prediction is an important step towards assessing the reliability of electronic products. With the help of accelerated tests, solder joint reliability data can be obtained for various operating conditions. These data can be used to establish an empirical model, and with the help of this model the life of solder joints can be predicted.

The definition of fatigue failure for a solder joint plays a critical role in understanding failure mechanisms and fatigue models. There are, in fact, wide variations in the failure definition used in the literature. For instance, expedient fatigue failure criteria recommended in industry guidelines include complete electrical circuit opens, a 50 % load reduction on the solder joint, and 20 % crack propagation across the solder joint [79, 81]. Any life prediction model deduced from the experimental reliability data of either bulk solder samples or geometrically simple model joints is based on one such failure criteria. Having obtained the life prediction model, solder joint fatigue life can be estimated for a given electronic package under assumed operating conditions. A number of life prediction approaches have been proposed over the past few years [83-86]. These approaches can be classified into the following major categories:

1. Coffin-Manson approach
2. Strain energy approach
3. Fracture mechanics approach,
4. Damage mechanics approach.

A stress-based approach is less commonly used for solders, although it can be useful for modelling "high-cycle" fatigue due to vibration or physically shocked or stressed components. There is no single dominant model which is universally used in

electronic packaging. However, Coffin-Manson approach is the most common, and is discussed below.

The Coffin-Manson equation is an empirical relation obtained by fitting a power law to the experimental fatigue data. Generally the predicted life using this equation is the number of load cycles required for the initiation of a fatigue crack which is observable upon inspection. This is an indication of local ductility exhaustion. There may be a large percentage of life left before the complete fracture of the component; however this comes in the realm of assessment of the fatigue crack propagation after it has been initiated. The general form of the Coffin-Manson equation is given as [29, 87, 88]:

$$N_f^r \Delta\varepsilon_p = C_2 \tag{4.4}$$

where N_f is the number of cycles to failure, $\Delta\varepsilon_p$ is the plastic strain range, C_2 is the fatigue ductility constant, and r is the fatigue ductility exponent. C_2 and r are empirically derived. With the repetition of service load (thermal or power cycle), the load carrying ability of the solder joint diminishes with the grain growth or the accumulation of damage in the solder joint. This results in the formation of micro-voids at the grain boundary intersections. These micro-cracks grow and coalesce into macro-cracks leading to total fracture. The value of material constant r is determined based on the load reduction for a constant strain. For high levels of damage, r tends toward lower values. In the IPC guidelines, the number of cycles to 50 % load reduction on the solder joint is considered as failure, and this can be obtained by using the values of material constants determined from the experimental reliability data obtained for 50 % load reduction on the solder joint. The value of r varies between 0.4 to 0.6 for common engineering metals [29, 89].

In order to predict the fatigue life using the Coffin-Manson equation, it is essential to establish the cyclic plastic strain range for the solder joint under study. Equation 4.1 is a simple analytical model to calculate the plastic strain for a single cycle. It assumes that only shear forces act on the solder joint, and hence it ignores any additional forces e.g. due to curvature of the component or substrate. It is also unable to take account of any compliance in the assembly. In addition, the Eq. 4.1 does not separately account

for the plastic and creep strain in the solder joint. Whalley *et al.* [90] demonstrated this simple approach is effective for situations where the cyclic strain is large and therefore life is short, but as the life increases the model has little predictive capability. This simple model also cannot be used to study the effect of non-uniform temperature distribution in the electronic assembly, which is one of the objectives of this research. Finite element modelling techniques have therefore been widely used in reliability studies of the solder joints in electronic assemblies [91-93]. With this method, the electronic assemblies can be simulated to establish the thermal stresses and strains while including both plasticity and creep material properties for the solder joints, and the resulting inelastic strains can then be used in Coffin-Manson based estimates of reliability. The plasticity and creep behaviours of the solder alloys were discussed in chapter 2. This method can also take into account non-uniform temperature distributions in the assembly and any compliance in the assembly.

The finite element modelling approach in fatigue life estimation consists of three primary steps. First, a theoretical or constitutive equation for the solder stress-strain relationship is constructed using appropriate assumptions, which forms the basis for modelling. Secondly, this constitutive equation is implemented within a FEA program and a model created. The FEA program calculates the stress-strain values for the system under study for the simulated conditions. Thirdly, the FEA results are used as inputs to a model predicting the number of cycles to failure, N_f.

4.5 Summary

Electronic products have a wide range of application environments. Ensuring the reliability of electronic products is an important step towards manufacturing good quality products. These products may operate under harsh environmental conditions where variations of temperature can be as extreme as between 218 K and 398 K. With such cyclic temperature excursions, solder joints used for electrical connections are subjected to cyclic stresses and strains. In addition, the high homologous operating temperature makes solder joints prone to creep deformation. Therefore, thermo-mechanical fatigue is the common type of failure in solder joints. This is further worsened in surface mount devices due to the small solder volumes available for accommodating the deformation. There is no unique model which addresses all issues

in the solder joints fatigue life prediction. However, the Coffin-Manson based approaches are commonly used for fatigue life estimation of the number of load (temperature) cycles required for the failure criteria specified by the IPC guideline. In this research, plastic strain range based Coffin-Manson equation is used for life prediction. This is due to the fact that life prediction models do not affect the comparative study of effect of two different thermal conditions on solder joint fatigue life. This is discussed in chapter 8 of the thesis.

5. Temperature Distribution Study for a Surface Mount Chip Resistor Assembly

This chapter discusses the work on the measurement of temperature for a surface mount chip resistor assembly. The chapter begins by discussing the reasons for obtaining the temperature distribution. Then discussed are the chip resistor construction, specimen preparation, experimental technique and methodology used for temperature measurement. The validation techniques used for the temperature measurements is also discussed in this chapter. Obtaining the internal temperature distribution, for use in the subsequent reliability studies of the assembly, using finite element analysis (FEA) is also presented.

5.1 Introduction

Experimental methods for the reliability evaluation of solder joints in electronic products are laborious and time consuming. Therefore, FEA has been increasingly employed in recent years to simulate the field operating conditions of electronic products, enabling the manufacturer to perform "virtual" reliability studies before releasing them onto the market. Also FEA is cost effective compared to experimental reliability tests. Such simulations require establishing relevant material properties data for the expected operating conditions, and actual representation of these operating conditions or of the qualification tests that the product will be required to pass. As discussed in Chapter 4, the main reason for failure of solder joints is cyclic thermally induced plastic/creep strain, which is responsible for thermo-mechanical fatigue. However, most of the reported finite element simulations on thermo-mechanical fatigue in solder joints have been carried out considering thermal cycling, which is the application of a changing, but uniform, temperature distribution to the electronic assembly [48, 92, 94-97]. However, in operation, electronic assemblies are subjected to non-uniform temperature distributions due to changes in the power dissipation. Such power changes may be due to the system being switched on and off or to e.g. variations in central processing unit (CPU) code execution demands. The assumption of uniform temperature distribution in such cases therefore results in a simplified representation of the operating conditions and it is important to know if the resulting

life prediction is pessimistic or conservative. In addition, in applications such as automotive, aerospace, etc., the ambient temperature can vary significantly when the electronic devices are in operation and temperature distribution in the assembly can be above the ambient temperature. This type of situation is very difficult to include in experimental accelerated life testing to understand its influence on the fatigue damage. However, in FEA such varying operating conditions can be readily included. Therefore, it is very important to establish accurate estimates of the actual temperature distribution in the electronic assembly for such conditions before their use in the finite element simulations.

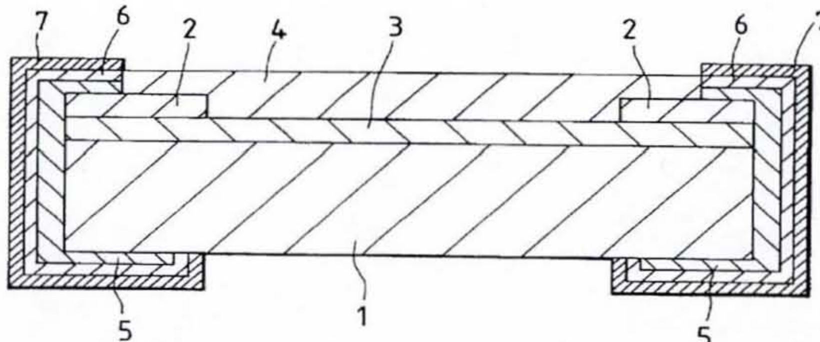
A series of experiments were carried out to find out the actual temperature distribution in a typical powered electronic assembly. To ensure applicability to the subsequent finite element analysis, a surface mount chip resistor assembly was used in the experimental work. The current chapter discusses the temperature measurement technique, measured temperature profile, validation of the measured temperatures and subsequent finite element thermal analysis used to obtain the full temperature distribution within the assembly. The construction of a typical chip resistor and chip resistor on PCB assembly, and its operating conditions, are also examined in this chapter.

5.1.1 Construction of 1206 Chip Resistors

Thick film chip resistors comprise of an insulating substrate, end terminations, the resistor film and a protective coating. The construction of the chip resistor is shown in Fig. 5-1 [98]. The resistor film is generally printed on one face of an alumina substrate (1) by the thick film technique of screen printing and firing at high temperature. The upper-face electrode layers (2) are also printed onto the end areas of the resistor film (3), to make surface contact with the resistor film. The resistor film and the upper-face electrode layers are fired simultaneously. The resistor film is an electrically resistive material containing cermet, such as ruthenium oxide. Next, the resistor film is trimmed to attain the desired resistance value. Thereafter, a protective film (4) is formed to cover a part of the resistance film (3). The construction of the chip resistor ends with the formation of end electrodes at either ends of the substrate. The end electrode consists of 3 layers as shown in Fig 5-1. First, end-face electrode layers (5) are formed

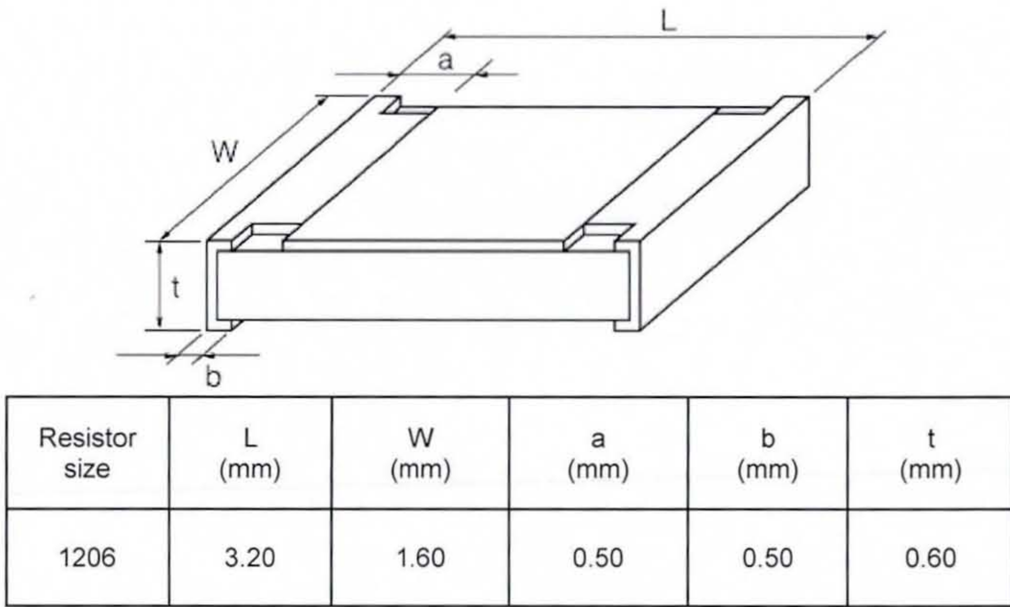
in a U-like shape on the opposing edges of the substrate (1) and on portions of the resistor film which are not covered by the protective film. This electrode layer is formed of an Ag/Pd thick film material. Subsequently, plated Ni film (6) covering the end-face electrode layers (5) is applied, and finally, (electro) plated Sn/Pb or Sn films (7) are formed over the Ni [98, 99]. These three layers of end electrodes are used to increase the performance and reliability of the chip resistor.

In the experiment a 1206 chip resistor manufactured by Panasonic was used. 1206 represents the size of the chip resistor, wherein the first two digits represents the length L (=0.12'') and last two digits represent width W (= 0.06''). The dimensions of the 1206 chip resistor are illustrated in Fig. 5-2. This type of resistor has a maximum power dissipation of 0.25W and can operate at ambient temperatures ranging between -55 °C (218 K) and 155 °C (428 K). However, this chip resistor can only operate at its maximum rated power (0.25W) up to an ambient temperature of 70 °C (343 K). If the operating ambient temperature increases beyond 70 °C (343 K), the maximum operating power of the chip resistor must be decreased to keep it within the safe operating range. Figure 5-3 shows the load derating curve to be used for various Panasonic chip resistors at high ambient temperatures. This curve is selected based on the resistor type such as 1G, 2R, 3E, 8E etc. The chosen 1206 chip resistor is of the 8E type, so the respective load derating curve is considered for power calculation at high ambient temperature. The available resistance of the 1206 resistor film varies from 10 Ω to 2.2 MΩ. However, in our experimental study chip resistors with 1.8 KΩ were used because of the limitation to achieve the drive voltage for attaining the maximum rated power.



1 – Alumina substrate; 2 – Upper-face electrode; 3 – Resistor film; 4 – Protective film; 5 – End-face electrode layers; 6 – Ni-plated films; 7 – Solder plated films

Fig. 5-1: Construction of a typical chip resistor [98]



Resistor size	L (mm)	W (mm)	a (mm)	b (mm)	t (mm)
1206	3.20	1.60	0.50	0.50	0.60

Fig. 5-2: Dimensions of the chip resistor used in the experiment [99]

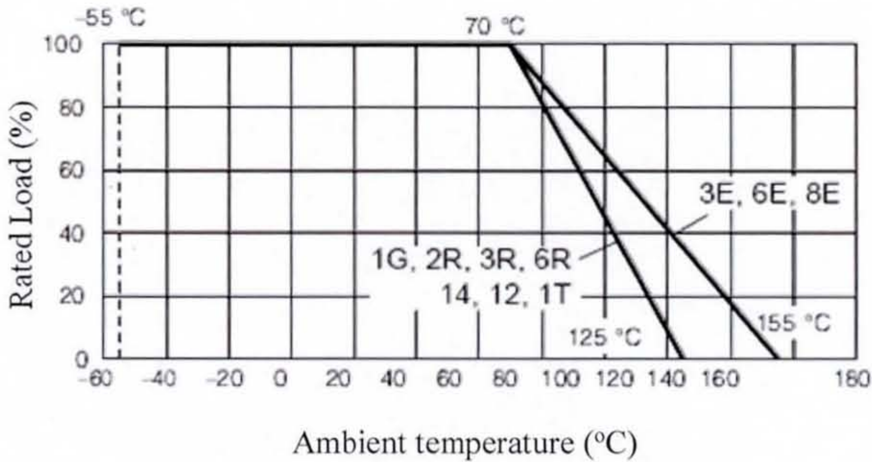


Fig. 5-3: Derating curves for Panasonic chip resistors [99]

5.1.2 Specimen Preparation

The chip resistor assembly consists of a FR4 substrate with copper pads, the solder joints and the 1206 chip resistor. The FR4 substrate, which has 35 μm thick copper tracks at a suitable spacing to mount the 1206 chip resistor, was 12 mm × 3.2 mm × 1.6 mm. The copper tracks are also used for making the necessary electrical connections. The 1206 chip resistor was mounted onto the copper tracks using reflow soldering and electrical connections were made soldering wire to other ends of the

tracks. Sn3.8Ag0.7Cu (by weight) solder paste with a contained particle size ranged from 25 μm - 45 μm and rosin flux was used for the reflow soldering. The flux is used to clean the soldered surfaces (copper tracks and component pads) and remove any oxide layer present to promote good wetting. Figure 5-4 shows a 2-dimensional schematic of the chip resistor assembly.

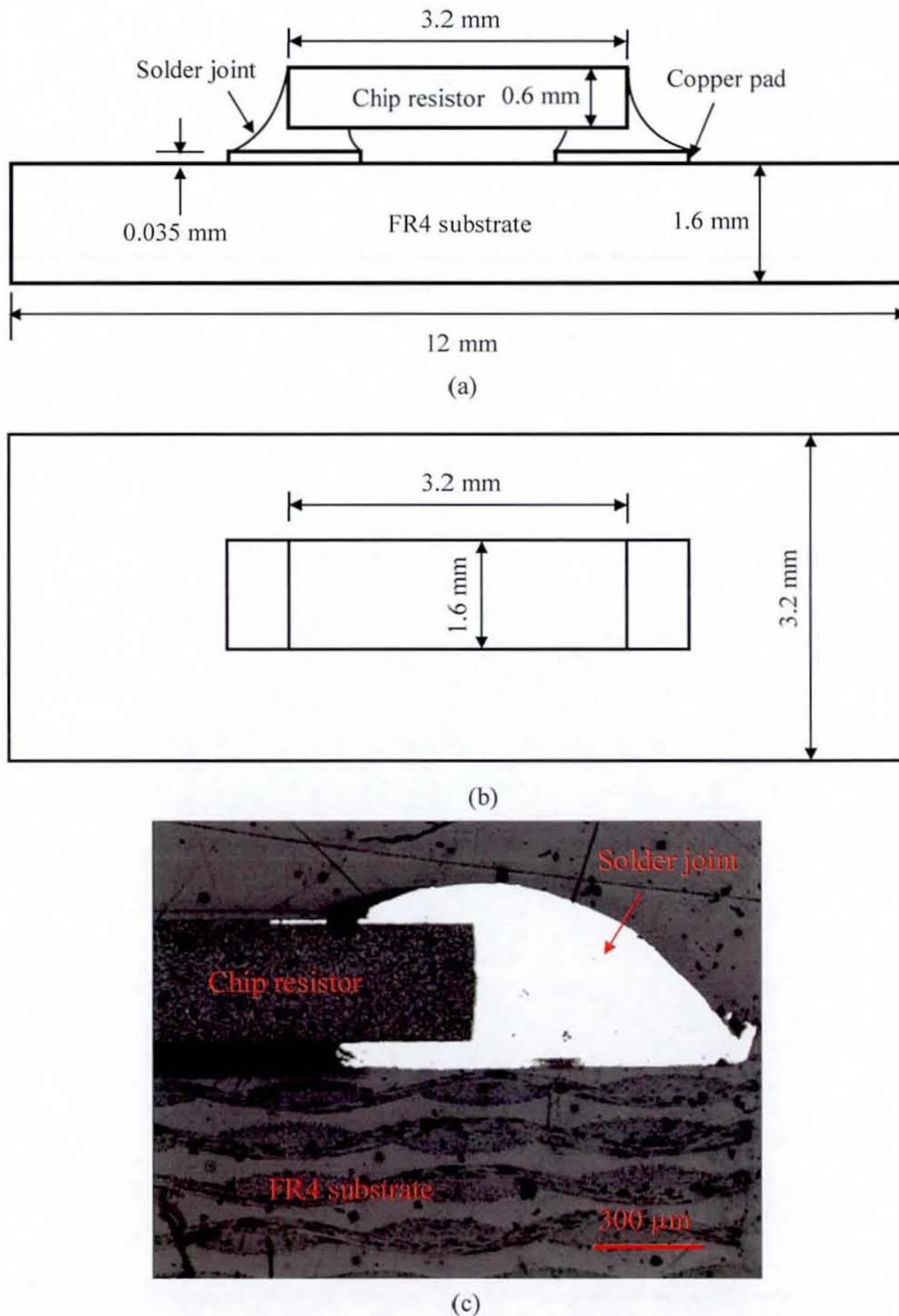


Fig. 5-4: Components of the chip resistor assembly: (a) front view; (b) plan view; (c) actual cross section

5.2 Experiment

5.2.1 Experimental Setup

A very simple experimental setup was used for measuring the surface temperatures of the chip resistor assembly. The experimental setup comprised of an infrared (IR) thermal imaging camera, specimen mounting and a power supply. All matter emits radiation as long as it has a finite (greater than absolute zero) temperature. IR thermal cameras capture this thermal radiation emitted from the surface, which has a wavelength spectrum dependent on the temperature, structure and composition of the surface. The rate at which radiation energy is emitted is usually quantified by the Stefan-Boltzmann law [100, 101]:

$$E_p = \varepsilon_s \sigma_{sb} T_b^4 \qquad 5.1$$

where E_p is the surface emissive power, ε_s is the emissivity of the surface, σ_{sb} is the Stefan-Boltzmann constant and T_b is the absolute temperature of the surface. The higher the temperature, the more radiation is emitted from the surface. This radiation is mainly infrared for surface temperature up to a few hundred °C and, therefore not perceptible with the naked eye, but is made visible and measurable by infrared cameras. Equation 5.1 shows emissive power depends on the emissivity of the surface. A blackbody is an ideal surface which emits the maximum possible thermal radiation at a given temperature, but most real surfaces emit less radiation than the black body. Through analysis of the emitted radiation it is possible to measure temperature and indirectly thermal conductivity, mechanical stress, material composition, defects and various kinds of in-homogeneities in the materials [100]. IR measuring technology is contactless and non-destructive, and supplies information with a spatial and temporal resolution that is not achievable with other measuring techniques.

A Thermosensorik IR camera (Fig.5-5 (a)) was used for the experiments and consists of a central processing unit with data processing software and an IR detector head with a focal plane array (FPA) detector sensitive in the range 1 μm – 14 μm. An infrared microscopic lens, with a focal length of 22 mm was used for this experiment. The camera is interfaced with software providing real-time acquisition and analysis of the infrared data. This camera has a very good temperature resolution of 20 mK and

spatial resolution of 20 μm per pixel [100]. The temperature analysis, based on the acquired surface radiation, is done using the reference temperatures provided to the software. Thus, the accuracy of the temperature measurement is dependent on the accuracy of the input reference temperatures.

The chip resistor assembly was mounted on a wooden block. The wooden block was used due to its low thermal conductivity (about 0.17 Wm/K) and it was placed on a lab jack to control the specimen height. Figure 5-5 (b) is a schematic of the experimental setup. The resistor was connected to a power supply to apply the required power. The chip resistor assembly was painted matt black to ensure a uniform high emissivity over the temperature measuring surface. An aerosol matt black paint, which has an emissivity of about 0.95 was used.

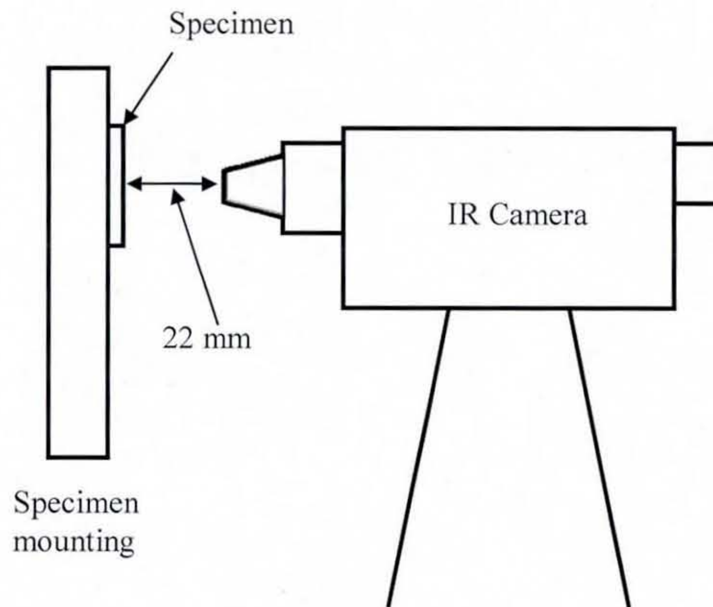
5.2.2 Experimental Procedure

As discussed in the previous chapters, the extremes of operating temperature for electronics can be between 218 K and 398 K. But the 1206 Panasonic chip resistor can only operate at its maximum rated power (0.25 W) up to an ambient temperature of 343 K. Therefore, two different power conditions were considered for obtaining the temperature distributions on the chip resistor. The two power conditions used were:

1. The maximum rated power condition of: 0.25 W at room temperature.
2. A de-rated power condition of: 0.15 W, as according to Fig. 5-3, when the ambient temperature increases to 398 K, the maximum operating power of the chosen chip resistor decreases to 0.15 W, which is approximately 60 % of the maximum rated power.

The temperature distribution obtained at full power (0.25 W) will be used for the simulation of power cycling at room ambient temperatures, while the distribution obtained from the de-rated condition (0.15 W) will be used for the simulation of a continuously heat dissipating chip for varying ambient temperatures between 398 K and 218 K. Having decided upon the power dissipation conditions to be used in the experiment, the voltage required to obtain the required power dissipation was found using the Eq. 5.2 [102].

(a)



(b)

Fig. 5-5: (a) The Thermosensorik infrared (IR) camera; (b) schematic of experimental setup

$$P_c = \frac{V^2}{R_c} \qquad 5.2$$

where P_c is power dissipation of the chip resistor, V is the required voltage for the specified power dissipation and R_c is resistance. Table 5-1 gives the required voltage to obtain the different power ratings. The following procedures were followed to conduct the experiment.

1. First the chip resistor was powered by supplying the required voltage to attain the power dissipation, and left for 10 minutes to stabilise to attain a steady state temperature distribution.
2. The thermal camera system was started.
3. Two reference temperatures, one lower and another higher, were set up using the same calibrated black body.
4. The chosen reference temperatures were beyond the two extremes of the expected temperatures of the chip resistor. The system calculates the temperature of the surface by comparing and interpolating the measured radiation from the sample against the radiation measured for the reference temperatures.
5. Once the steady state temperature distribution was achieved in the specimen and the reference temperatures were set, the thermal camera was brought in front of the specimen at a distance of approximately 22 mm (the lens focal length) and then focused on the centre of the resistor.
6. After attaining a clear image, the temperature profile was captured.
7. Similarly the thermal camera was focused on all sides of the specimen substrate and surface temperature profiles were captured.
8. All 7 steps were then repeated for the second power condition.

Table 5-1: Specifications at different power rating.

Required Power, P_c (watts)	Resistance, R_c (ohms)	Current, I (amps)	Voltage, V (volts)
0.25	1800	0.0118	21.2
0.15	1800	0.0091	16.4

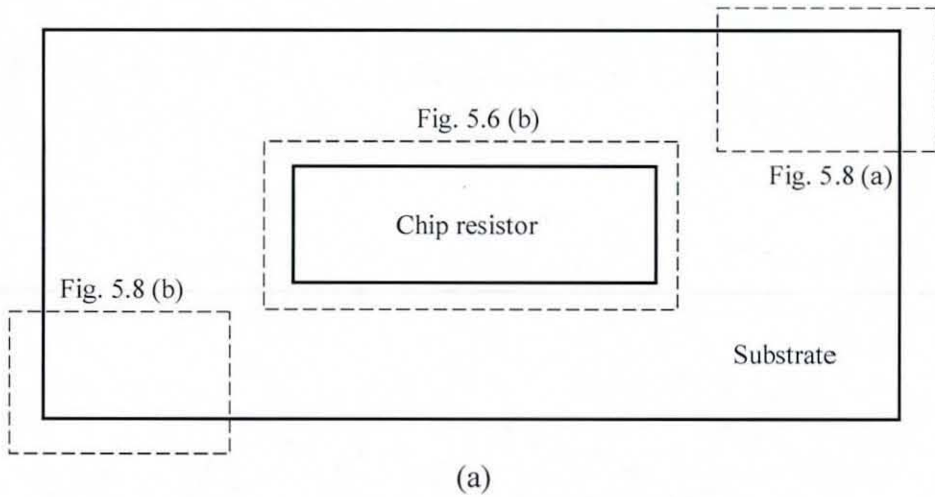
5.2.3 Results and Discussion

The experimental objective was to determine the surface temperature of the chip resistor assembly under steady state conditions. The transient state of the assembly either during heating or cooling was ignored because of the short time before attaining steady state temperature (chip resistor attained steady state within 300-360 seconds). In addition, as discussed in Chapter 4, during temperature cycling most of the creep strain occurs during the dwells at temperature extremes, during which the chip resistor would reach steady state. In steady state conditions, the surface temperature measurement gives the temperature distribution after accounting for the heat loss due to conduction, natural convection and radiation from the assembly. Therefore, in this section the experimental temperature measurements obtained under steady state conditions are discussed.

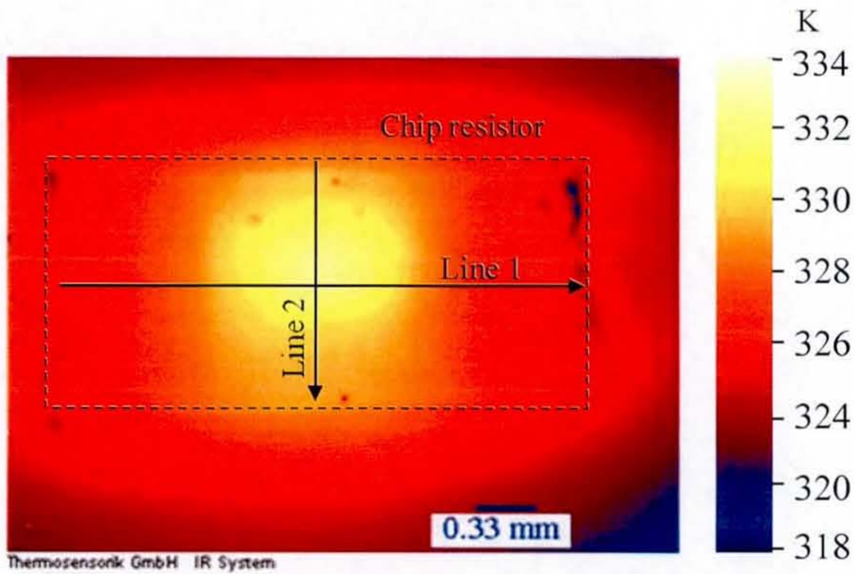
The surface temperatures of the chip resistor and substrate were analysed after capturing them using the thermal camera. Figure 5-6 (a) shows the different locations used to analyse the temperature distribution over the specimen. The distribution of temperature over the chip resistor at maximum rated power is illustrated in Fig. 5-6 (b). It is evident from the temperature distribution that the maximum temperature is within the resistor film area which is where the heat is generated. The temperature decreases towards the boundaries of the resistor film due to conduction away of the generated heat. A similar temperature distribution over the chip resistor was observed at the de-rated power (0.15W), but with a lower magnitude. The variation of temperature over the chip resistor was studied in more detail along two paths in 2-perpendicular directions i.e. line 1 and line 2 as shown in Fig. 5-6 (b). Figure 5-7 (a) shows the variation in temperature along line 1 for both the maximum and de-rated power conditions. As expected the temperature distribution is symmetric with a constant difference in magnitude between the two conditions. Similar observation can be made for the variation of temperature in the perpendicular direction (line 2), which is presented in Fig. 5-7 (b).

The temperature distribution over the substrate was also studied. The generated heat in the chip resistor is conducted into the substrate through the solder joints and copper tracks used for electrical connection. Figures 5-8 (a) and (b) illustrate the surface

temperature distribution at the top right and bottom left corners of the substrate respectively at for maximum rated power. The temperature distribution on the substrate for the de-rated power condition was similar to that observed for maximum rated power, but with a lower magnitude.

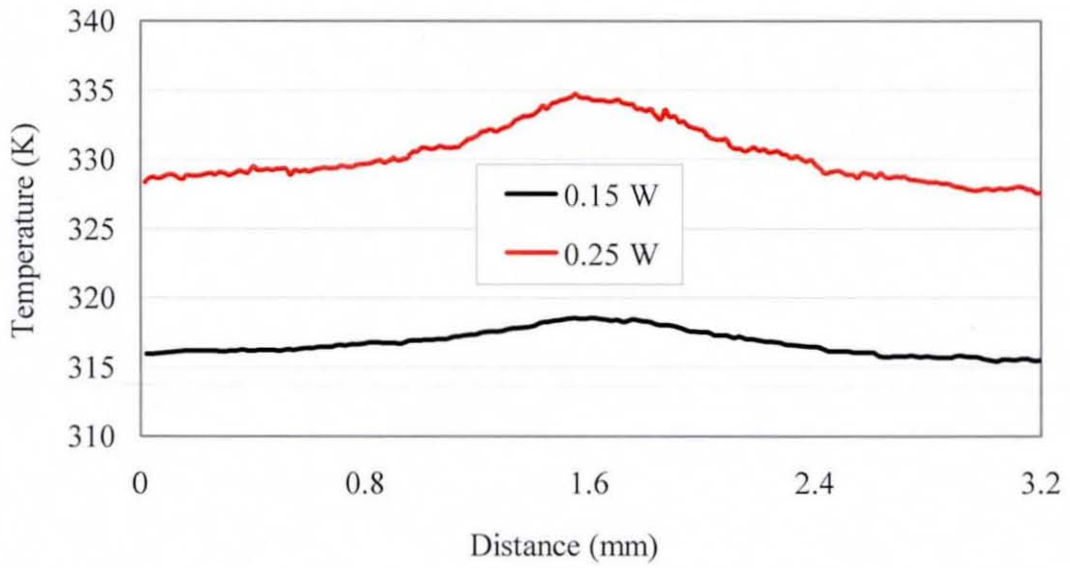


(a)

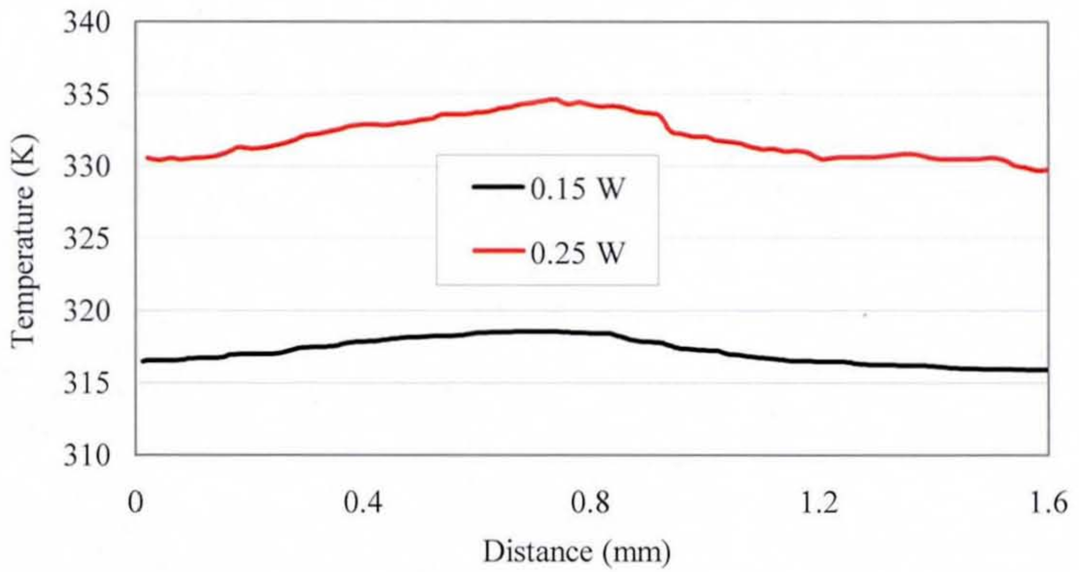


(b)

Fig. 5-6: (a) Locations used for temperature distribution study; (b) temperature distribution over chip resistor

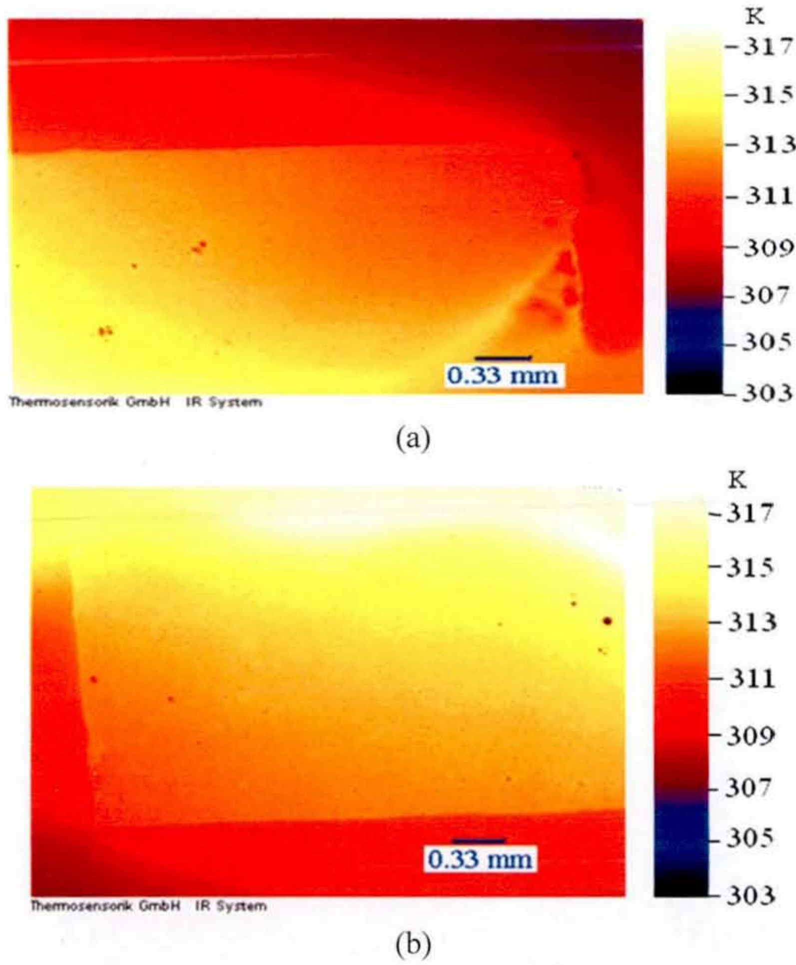


(a)



(b)

Fig. 5-7: Comparison of temperature distribution over the chip resistor: (a) along line 1; (b) along line 2



(a)

(b)

Fig. 5-8: Temperature distribution on the substrate: (a) top right corner; (b) bottom left corner

The temperature distribution obtained using the IR thermal camera was validated by comparison with the temperature measurements from thermocouples bonded to the specimen on the centre line at the eight locations indicated in Fig. 5-9. Calibrated K-type thermocouples with a wire diameter of 40 μm were used and these thermocouples were connected to a digital thermometer. The thermocouples were calibrated before bonding to the specimen by dipping in boiling water [103]. Table 5-2 presents a comparison of the temperatures at these locations for both power (0.25 W and 0.15 W) conditions. Comparison of temperatures could not be made at the bottom of the substrate where thermal imaging was not feasible. However, the temperatures match pretty well at the other locations with a maximum discrepancy of 1K between the two measurement methods. The temperature gradient, which is the difference between the maximum and minimum temperature (locations 1 and 5), obtained from the thermal

camera measurements is calculated to be 21.8 K and 12.6 K for the maximum and de-rated power respectively. The decrease in the temperature gradient for the de-rated condition is in proportion to the decrease in the power input.

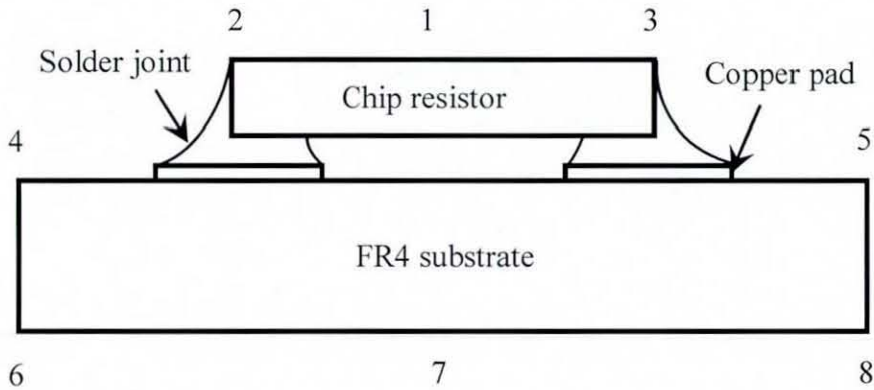


Fig. 5-9: Locations used for temperature measurement comparison

Table 5-2: Comparison of temperatures measured using thermocouples and thermal camera

Location (Fig. 5-9)	Maximum power (0.25W)		De-rated power (0.15W)	
	Thermal camera (K)	Thermo-couple (K)	Thermal camera (K)	Thermo-couple (K)
1	334.8	333.5	318.6	318.5
2	327.5	329.0	316.5	316.0
3	328.5	327.0	316.0	315.0
4	313.0	312.0	307.0	308.0
5	313.0	312.0	306.0	307.0
6		311.0		306.0
7		318.0		312.0
8		311.0		306.0

5.3 Finite Element Thermal Analysis

Finite element analysis (FEA), also called the finite element method (FEM), is a method of numerical solution of field problems, which require the determination of spatial distribution of one or more dependent variables. For example the distribution of displacements and stresses in a mechanical structure or the distribution of temperature in an electronic circuit board. Mathematically, a field problem is described by differential equations or by an integral expression [104]. Either description may be

used to formulate finite elements. Finite element (FE) formulations, in ready-to-use form, are contained in general purpose FEA programs. In finite element analysis the structure being analysed is divided into small regions known as elements. These elements are connected at points called nodes. The assemblage of elements is called a finite element mesh. Numerically, a FE mesh is represented by a system of algebraic equations to be solved for the unknown variables at nodes. Nodal unknowns are values of the field quantity and, depending on the element type, may also include its first derivatives. The solution for nodal quantities, when combined with the assumed (thermal/stress) field in any given element, completely determines the spatial variation of the field in that element. Thus the field quantity over the entire structure is approximated element by element, in piecewise fashion. However, a FEA solution is not exact (unless the problem is simple), but the solution accuracy can be improved by using more elements to represent the structure.

FEA has advantages over most of the other numerical analysis methods available due to its versatility. It is applicable to most field problems such as heat transfer, stress analysis, magnetic fields, etc. Also there is no restriction on the geometry to be analysed, boundary conditions and loading. Enhancements to FEA codes have allowed various types of material behaviour to be included such as anisotropic, orthotropic, elasto-plastic, creep, etc. Thus, FEA can be used to study many engineering problems such as new product design, improving existing products (e.g. their reliability), in studies of new materials, etc. In the present chapter, the use of finite element analysis for heat transfer analysis to establish the full temperature distribution within the chip resistor assembly is discussed. Thermal analysis of the chip resistor assembly was carried out for the full 3D geometry and also using a 2D approximation. The results are later used as the loads in finite element structural analysis.

Heat transfer in electronics packaging can occur in two ways, transient (power on/off or devices switching state) and steady-state (during continuous operation). In both cases the temperature distribution in the package is calculated by solving the heat conduction equation. Two-dimensional heat conduction based on the Fourier equation can be given as [29, 101, 104]:

$$q_x = -k_x \frac{\partial T}{\partial x} \qquad 5.3$$

$$q_y = -k_y \frac{\partial T}{\partial y} \qquad 5.4$$

It can also be written as:

$$\begin{Bmatrix} q_x \\ q_y \end{Bmatrix} = -\begin{bmatrix} k_x & 0 \\ 0 & k_y \end{bmatrix} \begin{Bmatrix} \frac{\partial T}{\partial x} \\ \frac{\partial T}{\partial y} \end{Bmatrix} \text{ or } \begin{Bmatrix} q_x \\ q_y \end{Bmatrix} = -[K] \begin{Bmatrix} \frac{\partial T}{\partial x} \\ \frac{\partial T}{\partial y} \end{Bmatrix} \qquad 5.5$$

where q_x and q_y are the heat fluxes in x and y direction, and k_x and k_y are thermal conductivities in x and y directions. The negative sign indicates that the direction of heat flow is opposite to the temperature gradient. For a body of unit thickness, the rate of heat generation (Q_g) within a differential element $dx\ dy$ is $Q_g dxdy$. Heat fluxes across the edges of a differential element in the xy plane are shown in Fig. 5-10. Here the lateral surfaces of the body (parallel to the xy plane) are assumed to be insulated. The net rate of heat flow into a differential element of unit thickness is given by:

$$Q_g dxdy - \left(\frac{\partial q_x}{\partial x} dx \right) dy - \left(\frac{\partial q_y}{\partial x} dy \right) dx \quad \text{or} \quad \left(Q_g - \frac{\partial q_x}{\partial x} - \frac{\partial q_y}{\partial y} \right) dxdy \qquad 5.6$$

Inwards heat flow produces an increase of stored energy, specifically $c\rho dxdy\dot{T}$. Hence

$$Q_g - \frac{\partial q_x}{\partial x} - \frac{\partial q_y}{\partial x} = c_p \rho \dot{T} \qquad 5.7$$

where c_p is the specific heat and ρ is the density. Combination of Eqs. 5.5 and 5.7 provides,

$$\frac{\partial}{\partial x}\left(k_x \frac{\partial T}{\partial x}\right)+\frac{\partial}{\partial y}\left(k_y \frac{\partial T}{\partial y}\right)+Q_g - c\rho\dot{T}=0 \qquad 5.8$$

For an isotropic and homogeneous medium, $k_x = k_y = k$ and Eq. 5.8 can be simplified to:

$$k\left(\frac{\partial^2 T}{\partial x^2}+\frac{\partial^2 T}{\partial y^2}\right)+Q_g - c\rho\dot{T}=0 \qquad 5.9$$

For steady state conditions ($\dot{T} = 0$) and $Q_g = 0$, Laplace's equation for two-dimensional heat flow can be written as:

$$\frac{\partial^2 T}{\partial x^2}+\frac{\partial^2 T}{\partial y^2}=0 \qquad 5.10$$

For these conditions and without internal heat generation Eq. 5.9 can also be written as:

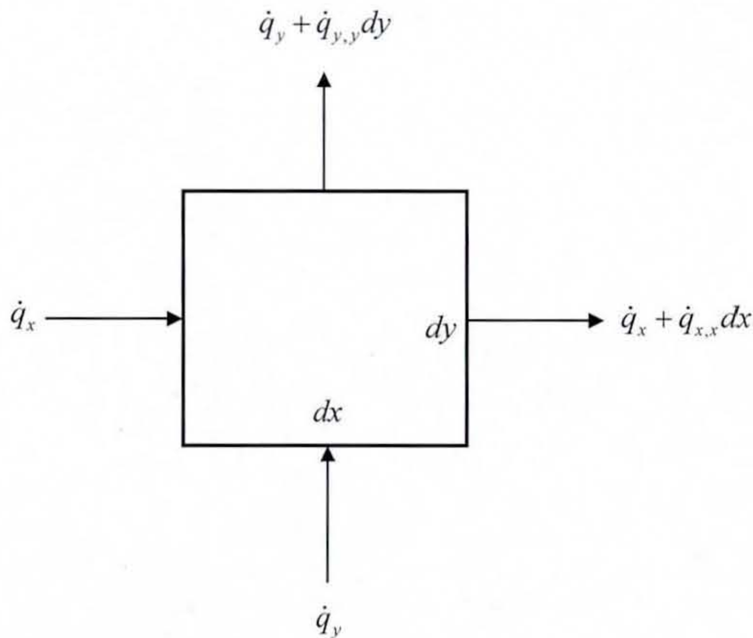


Fig. 5-10: Heat flux through sides of a plane differential element

$$\{\partial\}^T ([K]\{T_\partial\}) = 0 \qquad 5.11$$

where $\{\partial\} = \begin{Bmatrix} \frac{\partial}{\partial x} \\ \frac{\partial}{\partial y} \end{Bmatrix}$, $\{T_\partial\} = \begin{Bmatrix} \frac{\partial T}{\partial x} \\ \frac{\partial T}{\partial y} \end{Bmatrix}$

Equation 5.11 is known as the governing equation for conduction without internal heat generation in solid bodies.

5.3.1 2-D Thermal Analysis

Geometric and FE modelling

The geometry of the chip resistor assembly used in the finite element analysis was similar to the one used in the above experimental work, with the exception of the end terminations (electrodes) and resistor film of the chip resistor. Both end terminations and resistor film are thin layers which do not have much impact on the outcomes of either the thermal or structural analysis. Only one-half of the geometry was considered in the finite element analysis, making use of the structure symmetry and due to the symmetry in the temperature load. The model dimensions are presented in Fig. 5-11. A 0.1 mm gap was maintained between chip resistor and substrate, which was obtained from cross sectioning the tested specimen. 2D geometric modelling, FE modelling and thermal analysis were carried out using ANSYS version 11. The FE modelling was done using 2-D planar thermal solid elements (PLANE55). PLANE55 can be used as a planar element or as an axisymmetric ring element with a 2-D thermal conduction capability. This element type has four nodes each with a single degree of freedom, temperature [105]. This element was used in the thermal analysis using the thickness option which allows the thickness of the different components of the geometry (i.e. in the Z-direction) to be specified. Figure 5-12 shows the mesh used for the chip resistor assembly.

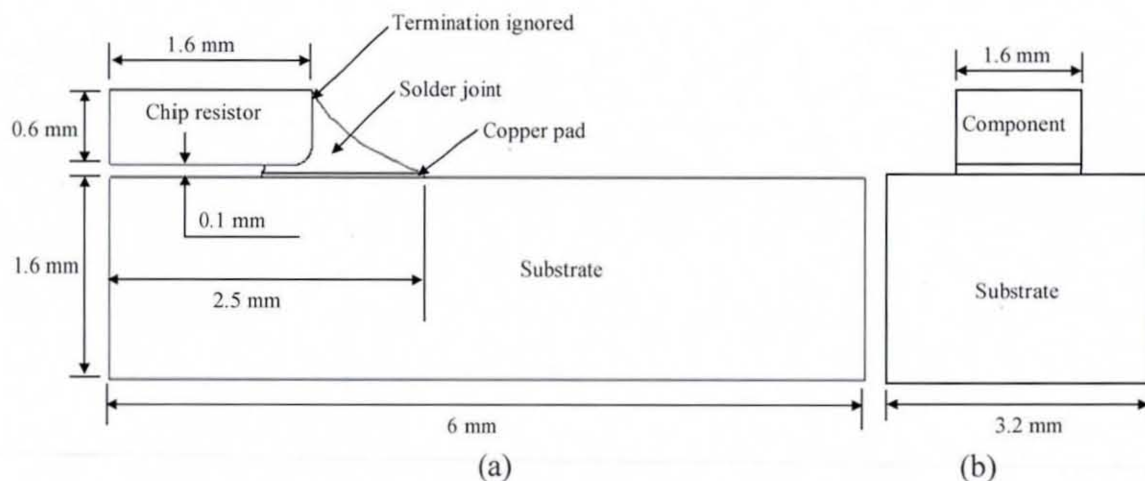


Fig. 5-11: Geometrical details of chip resistor assembly model: (a) side view; (b) front view

Thermal Material Properties

The thermal material properties used in the analysis are presented in Table 5-3. Only thermal conductivity was defined since the thermal analysis was restricted to steady state conduction. All the materials used were considered to be isotropic and homogeneous. In the finite element analysis the chip resistor (component) was considered to be a single material as the resistor film and end electrodes were ignored in the modelling. Therefore, the component was modelled using the thermal conductivity of 96 % alumina, which is its major constituent. The thermal conductivity of 95.5Sn3.8Ag0.7Cu was used for the solder joint, while the substrate of the assembly was modelled using a typical published thermal conductivity value for glass reinforced epoxy which is generally referred to as FR4.

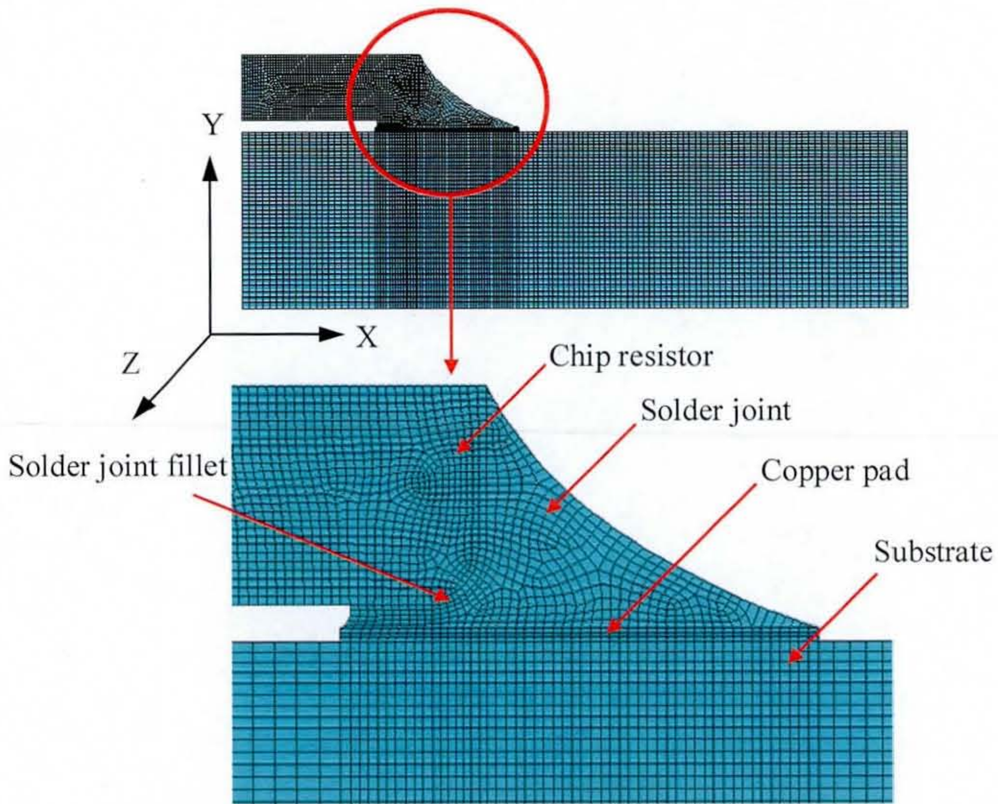


Fig. 5-12: 2-D finite element mesh of the 1206 resistor assembly

Table 5-3: Material properties used in the thermal analysis [106, 107]

Material	Thermal conductivity (W/mK)
Alumina	25
Solder (SAC)	60.32
Copper	400
FR4	0.3

Boundary conditions

The experimental temperature measurement for the chip resistor assembly only provided its surface temperature. To account for the effects of temperature gradients on the structural integrity of the solder joint using finite element analysis, the internal temperature distribution is essential for application as a thermal load. Therefore, thermal analysis of the chip resistor assembly was carried out. For this analysis it was only necessary to consider conduction heat transfer. As discussed before, under steady state conditions the generated heat in the chip resistor assembly is lost to the surroundings by natural convection and radiation from its sides. Thus the measured surface temperature gives the actual distribution on the assembly after accounting for heat loss from its sides. Therefore, in this thermal analysis the surface temperatures obtained from the experiments were used as boundary conditions instead of using heat generation and connection cooling out. Thermal analyses were carried out for three temperature conditions to use the obtained full temperature distribution within the assembly for the simulation of both power cycling at constant ambient temperature and continuous power dissipation in the chip resistor combined with ambient temperatures cycling between 398 K and 218 K. The three sets of conditions are:

1. Maximum rated power (0.25W) at room temperature (294 K).
2. De-rated power (0.15W) at an ambient temperature of 398 K.
3. De-rated power (0.15W) at an ambient temperature of 218 K.

The temperature boundary conditions used in the thermal analysis for the maximum rated power condition were directly taken from the experimentally measured surface temperatures for the same power level. Figure 5-13 shows the thermal zones used for the application of boundary conditions based on the experimental measurements. For example, to apply the maximum temperature observed on the chip resistor due to heat generated by the resistive element, zone A on the top surface of the component was selected and the temperature measured at this location was applied. Similarly other temperature zones were selected and their respective temperature conditions applied, as listed in Table 5-4. The surfaces on which temperature boundary conditions are not applied were considered to be adiabatic. A linearly varying temperature was applied on the bottom surface of the substrate, which is between zone D and E, to replicate the real distribution when the chip resistor was powered.

To obtain the appropriate temperature conditions for the de-rated thermal analysis, the increase in the surface temperature above room temperature was first determined at the locations shown in Fig. 5-13 from the experiment results. This increased temperature was added to the relevant ambient temperature to obtain the temperature boundary conditions for the thermal analysis being conducted. The two extremes of ambient temperature considered were 398 K and 218 K. Table 5-4 also presents the temperature levels used for different zones of the resistor assembly for these ambient temperatures. These were the assumptions made in the analysis at high and low ambient temperature:

1. Heat transfer out of the assembly will be the same as that at room temperature (294 K)
2. Time required for attaining steady state is the same as that required at room temperature
3. The material properties of the chip resistor assembly constituents do not change with temperature

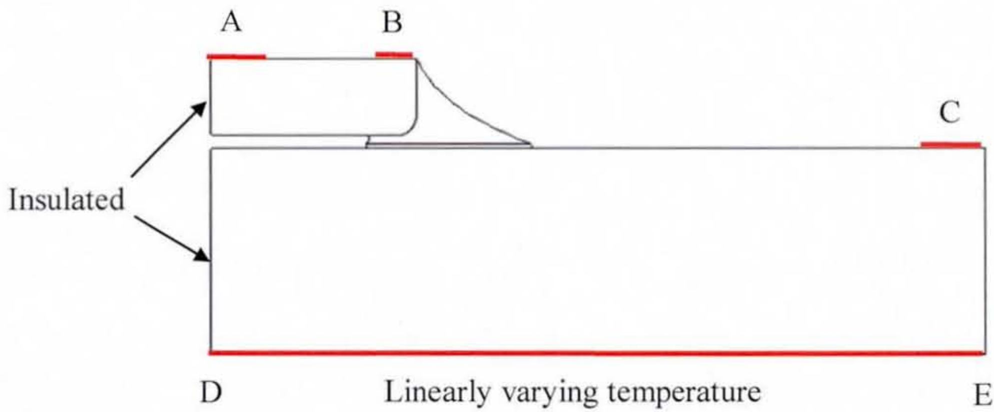


Fig. 5-13: Thermal boundary condition zones

Table 5-4: Temperatures applied to the different zones in the 2-D thermal analysis

Thermal zone (Fig. 5.13)	Zone temperature (K)		
	Maximum rated power at room temperature	De-rated power (0.15W)	
		Ambient temperature of 398 K	Ambient temperature of 218 K
A	334.8	421.6	241.6
B	328.0	419.0	239.0
C	313.0	410.0	230.0
D	318.0	415.0	235.0
E	311.0	409.0	229.0

Temperature Distribution Results

Figure 5-14 illustrates the predicted full temperature distribution in the chip resistor assembly at maximum rated power. The temperature distribution is the same that obtained from the experiment. A comparison of this predicted distribution with the experimental temperature variation over the right half of the chip resistor is presented in Fig. 5-15. The predicted temperatures compare well with the experimental one with a maximum discrepancy of slightly more than 1 K in the area between the boundary of the chip resistor and resistor film.

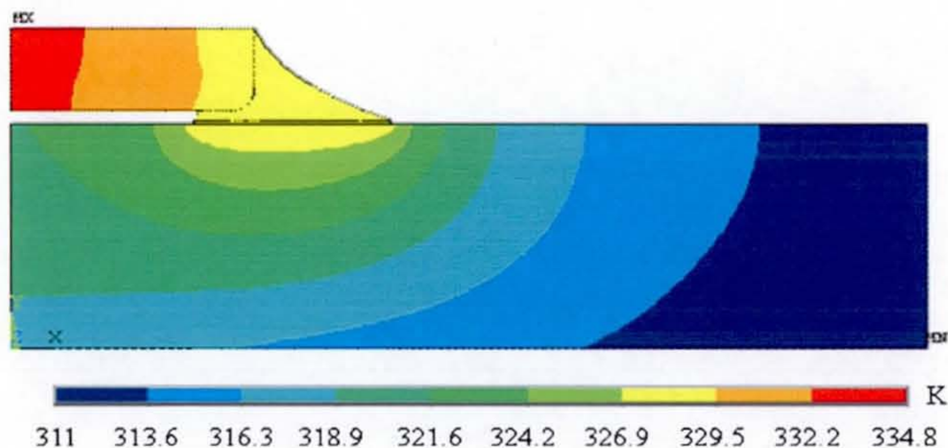


Fig. 5-14: Predicted full temperature distributions in the chip resistor for 0.25 W

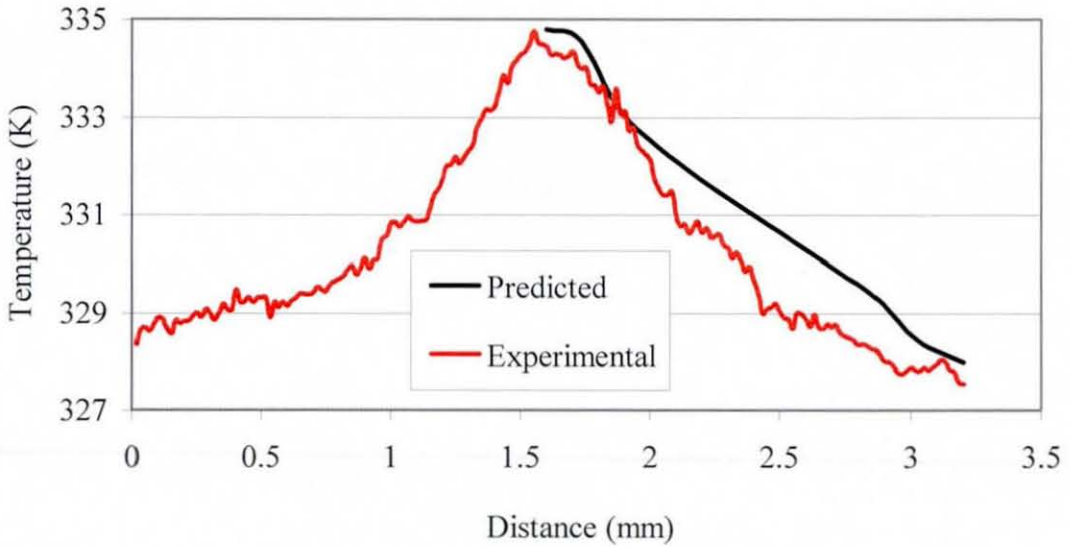
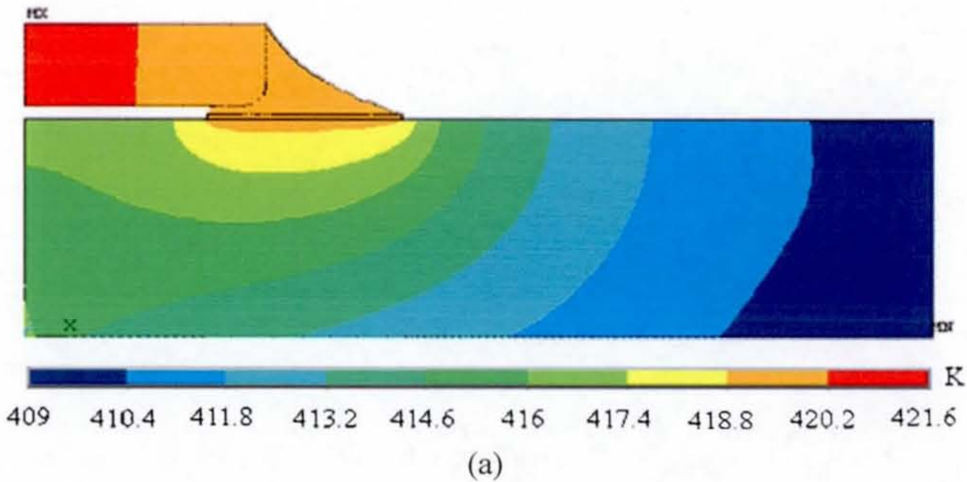
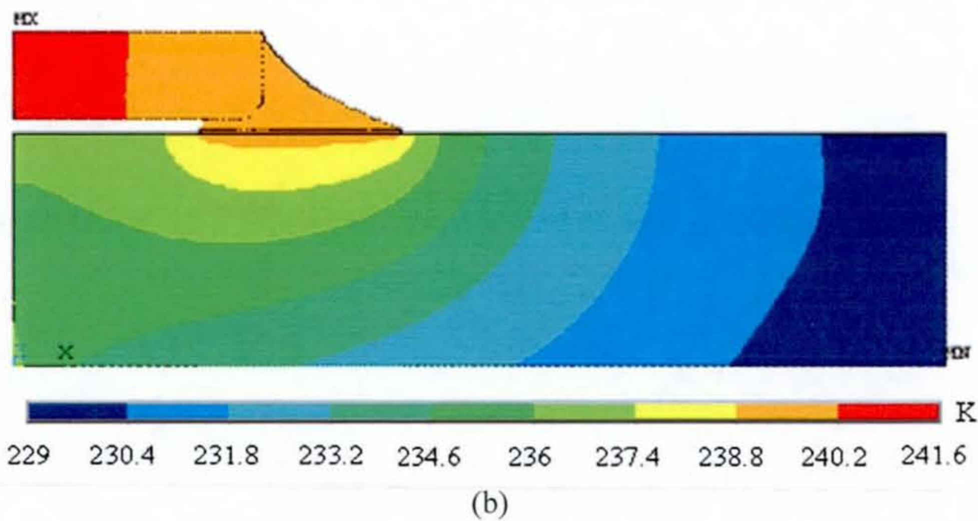


Fig. 5-15: Comparison of predicted and experimental temperature distributions over chip resistor for 2D analysis

For the de-rated power conditions (0.15W) Figs. 5-16 (a) and (b) show the full temperature distribution in the assembly for ambient temperatures of 398 K and 218 K respectively.



(a)



(b)

Fig. 5-16: Predicted temperature distributions at 0.15 W: (a) for an ambient temperature of 398 K; (b) for an ambient temperature of 218 K

5.3.2 3D Thermal Analysis

3D thermal analysis was carried out to decide upon which approximation (2D or 3D model) is appropriate for the detailed structural analysis. Therefore, it was carried out only for maximum power condition, which results in the maximum temperature gradient in the assembly and hence maximum structural effect.

Geometric and FE modelling

The geometry of the chip resistor assembly modelled in the 3-D finite element thermal analysis was exactly the same as that for the 2-D analysis, which is illustrated in Fig. 5.11. The half symmetry of the structure was also utilised in the 3-D model since the predicted temperatures could then be directly applied onto same structural model. The 3D FE model was built in ANSYS using 3-D thermal solid elements, SOLID70. This element type has eight nodes with a single degree of freedom, temperature, at each node. In addition, it is applicable to steady-state and transient thermal analysis. The mesh used is shown in Fig. 5-17.

The material properties used for this 3-D thermal analysis were the same as those used in the 2-D thermal analysis (Table 5-4).

Boundary conditions

Unlike the 2-D thermal analysis, the 3-D analysis was carried out only for the maximum power condition discussed in the above section. The method of application of temperature boundary conditions was the same as explained for the 2-D thermal analysis, but with temperatures specified for a few additional locations. These additional locations were considered to take account of the three-dimensional variation of temperature in the chip resistor assembly. Figure 5-18 shows the locations of the thermal zones and the respective temperature levels used are presented in Table 5.5. A linearly varying temperature was applied between thermal zones O and P along the bottom surface of the substrate.

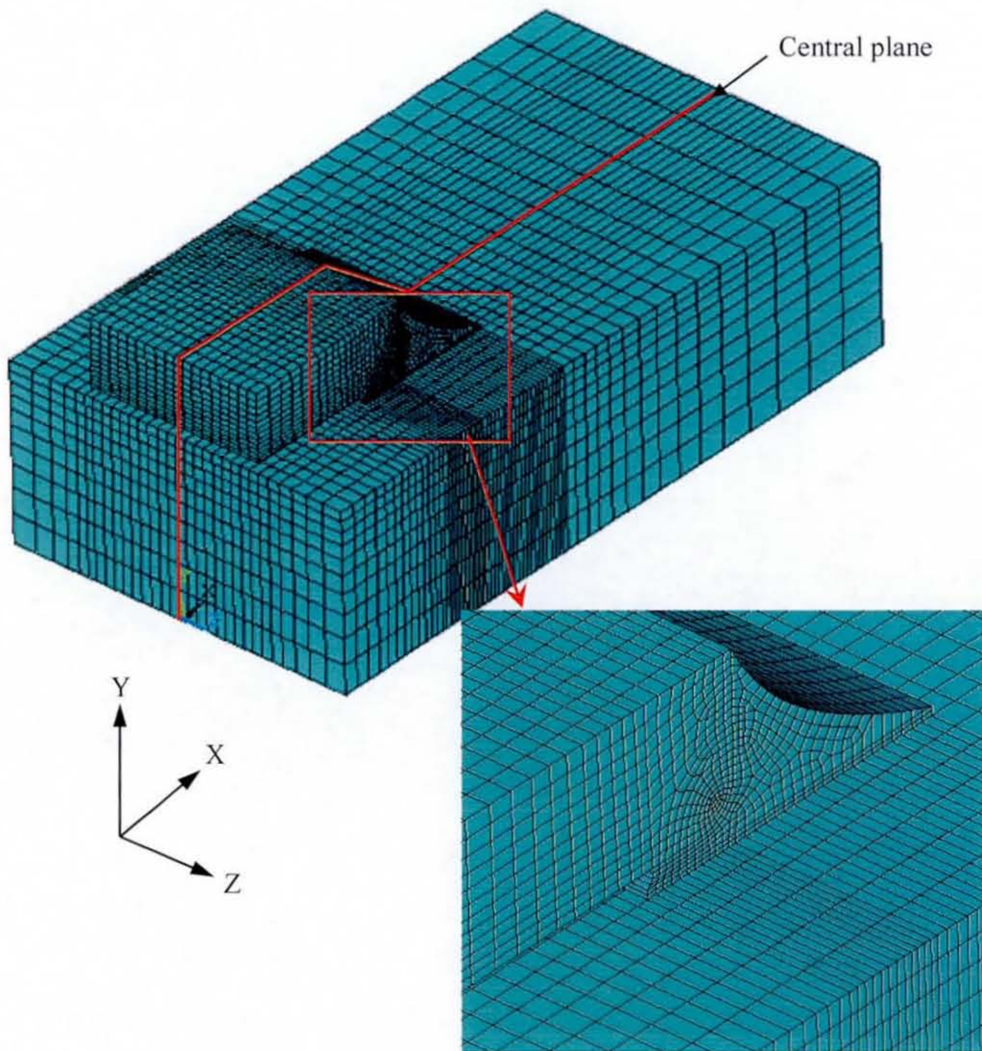


Fig. 5-17: 3-D finite element mesh for the 1206 resistor assembly

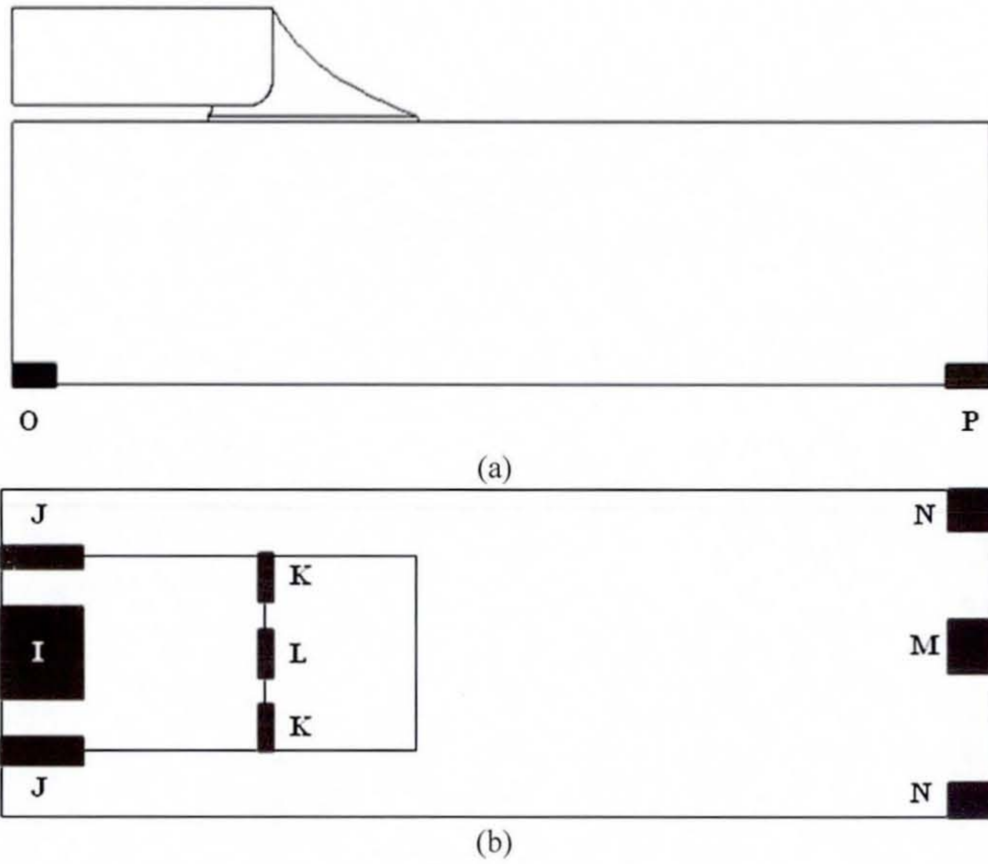


Fig. 5-18: Zones for thermal boundary conditions for 3-D thermal analysis: (a) side view; (b) top view

Table 5-5: Temperatures applied at the different zones in the 3-D thermal analysis

Thermal zone (Fig. 5.18)	Temperature (K)
I	334.8
J	330.0
K	328.0
L	324.0
M	313.0
N	311.0
O	318.0
P	311.0

Temperature Distribution

The predicted 3-D temperature distribution in the chip resistor assembly is illustrated in Fig. 5-19 for the maximum rated power (0.25W) at room temperature. The comparison of the predicted and the experimental temperature variations along line 1 and line 2 (see Fig. 5-6) shows good correlation, which is presented in Figs. 5-20 and 5-21, respectively. The maximum discrepancy along the line 1 is about 1 K with predicted being on the higher side, while that along line 2 is between 1 and 2 K.

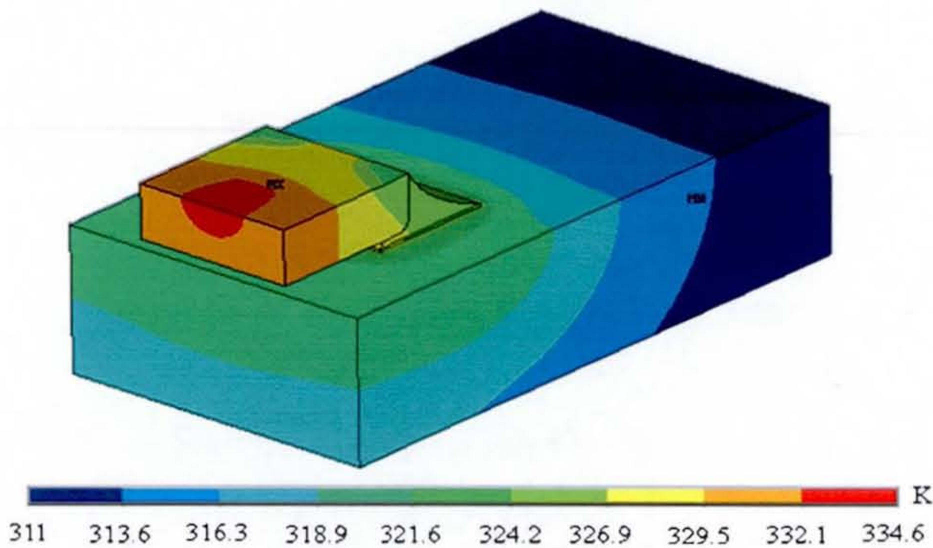


Fig. 5-19: Predicted full 3-D temperature distribution (K) in chip resistor for 0.25 W

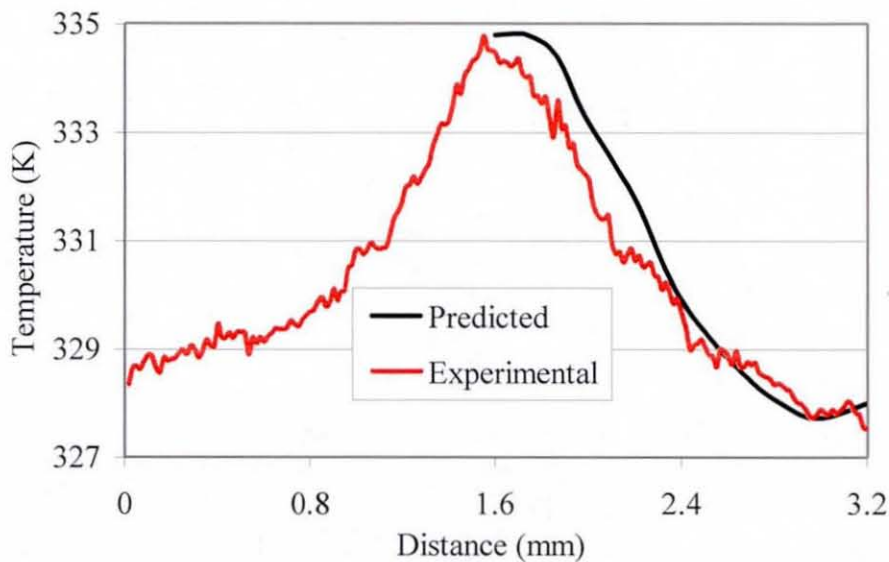


Fig. 5-20: Comparison of predicted and experimental temperature variation along line 1 over chip resistor for 3D analysis

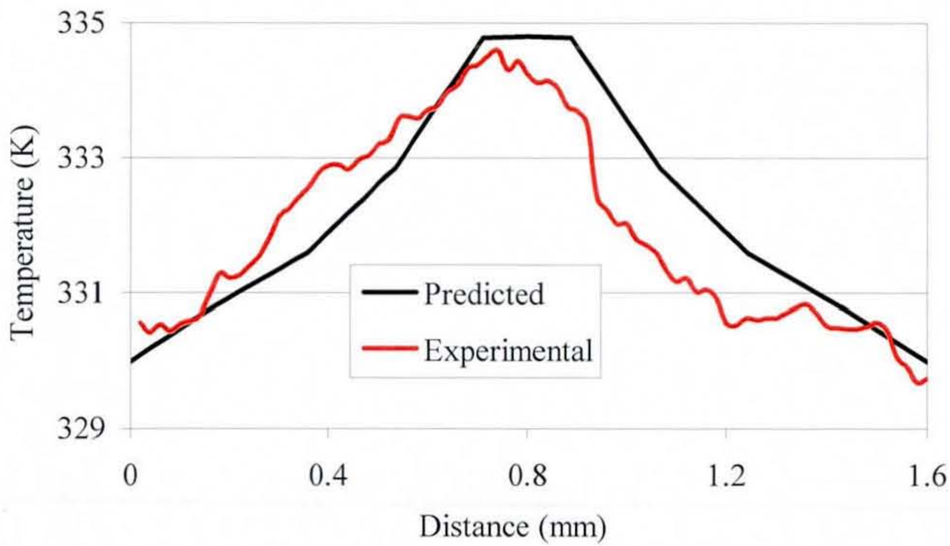


Fig. 5-21: Comparison of predicted and experimental temperature variation along line 2 over chip resistor for 3D analysis

5.4 Summary

This chapter discussed experiments carried out to obtain the real surface temperature distributions in a chip resistor assembly and the use of them as thermal boundary conditions in finite element thermal analysis to obtain the full temperature distribution within the same assembly. The contactless infrared (IR) temperature measurement technique used provides a realistic temperature distribution and matches very well with the spot temperature measurements from thermo-couples. The experimental results proved that the steady state distribution of temperature in the chip resistor assembly is non-uniform when the chip resistor is powered. The obtained temperature distribution from the experiment was over the surface of the assembly; hence finite element analysis was used to also obtain the full temperature distribution within the assembly. Finite element thermal analyses were carried out for both 2-D and 3-D geometry and these thermal results will be used later as boundary conditions in finite element structural analyses to study the effects of a non-uniform temperature distribution in the assembly on its structural integrity.

6. Stress-Strain Properties of Sn3.8Ag0.7Cu Solder

The properties as well as the factors affecting these material properties of lead-free Sn3.8Ag0.7Cu solder are less understood than traditional Sn-Pb solders. Therefore, the present chapter focuses on the determination of stress-strain properties for both small-scale solder joints and the bulk solder for three different strain rates. The chapter also analyses the obtained experimental results, and compares material properties between the solder joint and the bulk solder. The reasons for the differences in the observed material properties are discussed and their effect is separated with the use of finite-element analysis.

6.1 Introduction

One of the biggest challenges for electronic devices is to be reliable in harsh environments. As discussed in previous chapters solder joints are typically the weakest connecting part in what is a multilayered assembly. Therefore, to ensure the structural integrity of an electronic assembly, an appropriate solder material and knowledge of its material properties are essential.

Although a fair amount of studies have been conducted on obtaining different material properties for Sn3.8Ag0.7Cu solder using bulk solder specimens [34, 36, 108], its properties at the microscale i.e below 100 μm are less understood. A bulk specimen contains a large number of randomly oriented grains and the characteristic effective behaviours, such as elastic, plastic and creep, describe the average performance of these grains. Therefore, bulk specimens are usually considered as isotropic and homogeneous. However, it is different for small-scale solder joints that contain only one or a few grains [59, 109-111]. Their performance is expected to shift from a polycrystal-based behaviour to an inter- or intragranular-based one. In such cases individual grains play an important role in the behaviour of the individual solder joints. As discussed in chapter 3, β-Sn, the matrix of SnAgCu solder, has a body centred tetragonal structure, so the mechanical behaviour of a single grain is expected to have considerably anisotropic characteristics. In such a case, the grain orientation can also be a key factor in determining the behaviour of the solder joint [19, 60, 111].

In addition to the grains and their orientation, the size and substrate of the solder joints can also affect their mechanical behaviour. Since solder joints are usually used to join dissimilar materials, the influence of joint size on the solder material behaviour increases as the size decreases. Solder joints can also be compared with brazed joints where the tensile strength of a thin transverse brazed joint proved to be considerably higher than that of the bulk joint material [112-114]. Therefore, the assessment of reliability of small-scale solder joints based on the properties data for bulk material can be inaccurate. Thus it is essential to evaluate the material properties of solder joints which are of a scale commensurate to the real application, as well as the various factors affecting its mechanical behaviour.

In the present chapter, an experiment designed to evaluate the stress-strain properties of small-scale solder joint is described. A commercial solder paste containing Sn3.8Ag0.7Cu powder was used to fabricate solder joints between copper substrates. Comparison of the properties is made with those for bulk specimens, and factors affecting them, such as the microstructure and size of the solder joints, are discussed. The chapter also presents the use of finite element analysis to separate the influences of the microstructure of the solder joint and its size on the observed material properties.

6.2 Experimental Methodology

6.2.1 Experimental Setup

The objectives of the experimental work were to determine the stress-strain relationship for a solder joint which is commensurate in scale or other properties to real life applications, and which could also be used to isolate and study the effects of microstructure and size in the lead-free solder materials. The properties were obtained under tensile loading conditions. Since the size of the solder joint specimens used in the tests was small, a high precision tensile testing machine was required. The Instron MicroTester (5848) material testing system provides a solution to the challenges of testing microcomponents and microelectronic specimens. Accurate testing of such specimens requires high-precision displacement measurement, coupled with a load frame that maintains both alignment and high stiffness throughout its load range. Because of these factors, standard universal testing machines usually lack the

precision needed for small-deformation measurements. The expected deformation in the specimens is at the scale of micro-metres.

The MicroTester, which is ideal for tests requiring less than 2 kN force, is equipped with Instron's 5500 series controller and Bluehill-2 software for monotonic and simple cyclic applications. This can be fitted with a wide range of grips and fixtures for tension, compression, bending and component testing. The MicroTester load frame features two precision aligned columns fixed to a rigid support base and moveable upper crosshead. The design offers an extremely stiff reaction frame, ensuring accurate and repeatable deformation information and displacement control [115].

Through the use of a precision digital encoder mounted directly to the loading actuator, Instron guarantees a displacement accuracy better than 0.5 μm over short distances, and a resolution better than 20 nm. Instron control electronics, along with load measurement transducers designed and manufactured by Instron, provide flexible and accurate force measurement. In the case of the 5500 series controller, a load measurement accuracy of 0.5% of reading is guaranteed down to 1/250 of the load cell capacity. As mentioned earlier, this machine is fitted with Bluehill-2 software for operating it. Bluehill-2 software is also interfaced with the data acquisition where essential data such as displacement, load etc. can be output in ASCII format for further use, which makes the machine user-friendly. Considering this versatility, the Instron MicroTester was used for tensile testing of small-scale solder joints and its main components are shown in Fig. 6-1.

6.2.2 Measurement Technique

Even though the MicroTester is fitted with an accurate data acquisition unit, the measured displacement includes the effects of compliance. The compliance effect can be from machine parts, such as fixtures and linkages, and from the copper substrates of the specimen. In typical electronic packaging techniques, solder joints connect the components and PCB. Printed circuit boards usually contain copper tracks which forms a substrate material for the solder joints. Copper is also a common component termination material, although a range of other materials (such as nickel, silver, paladium etc.) are also used. Therefore, high purity copper (Cu) is used as the

substrate for fabrication of the test solder joints as shown in Fig. 6-2. Therefore, the total displacement (δ_t) given by the data acquisition system can be written as:

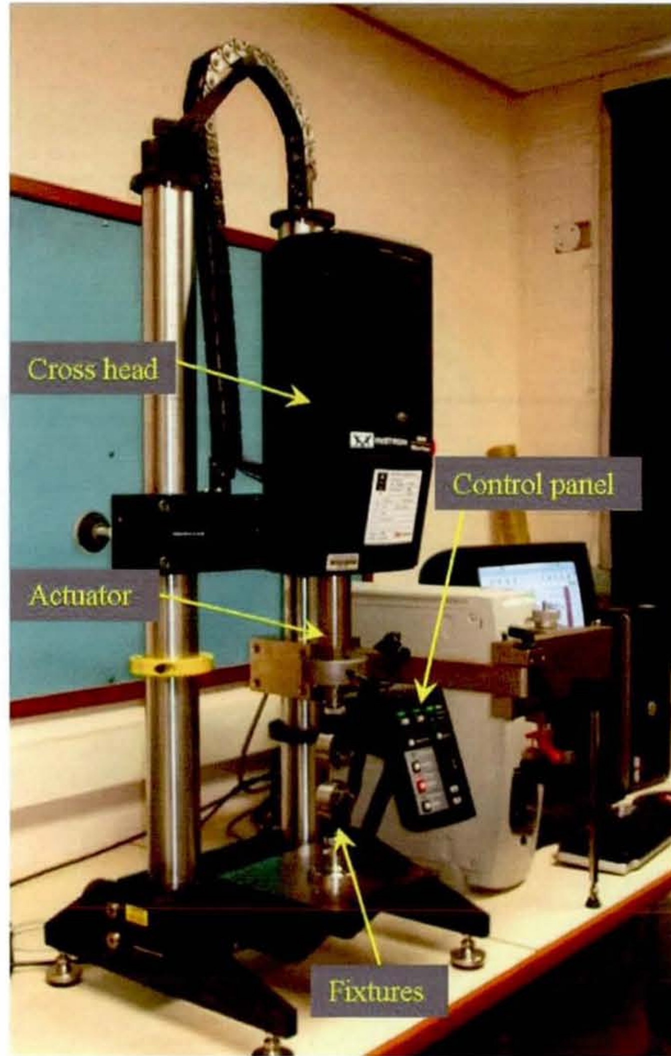


Fig. 6-1: Main components of Instron MicroTester

$$\delta_t = \delta_m + \delta_c + \delta_s \qquad 6.1$$

where δ_m is the displacement due to machine compliance, δ_c is the displacement due to the elasticity of the copper and δ_s is the solder joint displacement. To separate the effect of machine compliance, a highly sensitive Instron 2630-100 series extensometer was used. Its lightweight and rugged cross-brace design eliminate errors caused by physical distortion, while built-in protection ensures that damage is not caused by overextension. The low operating-force arms of the extensometer reduce the possibility of knife-edge slippage when testing hard or smooth surfaced materials. The

extensometer has a gauge length of 10 mm and can accommodate axial travel of up to +/-5 mm. This extensometer can be plugged in to the MicroTester's data acquisition system so that the displacement measurement is transferred to a file along with the other data. During the tensile test, the extensometer is mounted onto the test specimen and the displacement taking place within its gauge length is measured. Thus the displacement output from the extensometer (δ_{ext}) consists of only the displacement within the copper and solder joint and can be given as:

$$\delta_{ext} = \delta_c + \delta_s \qquad 6.2$$

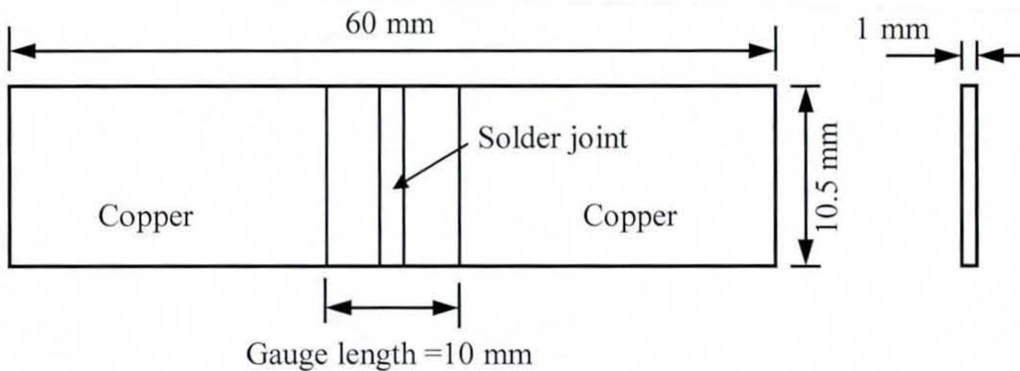


Fig. 6-2: Solder joint specimen details

Now the aim is to eliminate the displacement of copper from the extensometer output. To achieve this, an experiment was conducted with a sample of the copper used as the substrate for the fabrication of solder joints. C103 grade copper (Cu) was used with a chemical composition of a minimum of 99.99 % copper and less than 0.0005 % oxygen (O). The copper has a tensile strength of 253 MPa and yield strength of 195 MPa. In this experiment, the copper specimen was loaded up to, 1200 N (equivalent to approximately 120 MPa) and then unloaded to 100 N (approximately 10 MPa). The load curve used in the experiment is demonstrated in Fig. 6-3.

A general comparison of the material properties of copper and most lead-free solders shows that lead-free solders have much lower tensile and yield strengths than copper. This allows achievement of plastic strain in the solder joint material whilst the copper remains in the elastic range. This assumption is supported by the experimental results from the loading and unloading tests on the copper specimen. The experimentally

obtained stress-strain curve for a specimen is illustrated in Fig. 6-4. The unloading part of the stress-strain curve demonstrates the presence of permanent deformation if the curve is extended to full unloading. However, the amount of this permanent deformation is significantly smaller than the 0.2 % strain, which is used for obtaining the yield strength and up to which the material is considered to be elastic. In addition, as will be seen later the maximum load withstood by the small-scale solder joints falls within the linear elastic region of the copper stress-strain curve. Therefore, the copper deformation is considered to be in the linear elastic range during the actual solder joint experiments. Thus, to obtain the actual deformation of the solder joint, the elastic deformation of the copper δ_c can be subtracted from the displacement recorded by the extensometer (δ_{ext}). The copper deformations δ_c can be given by:

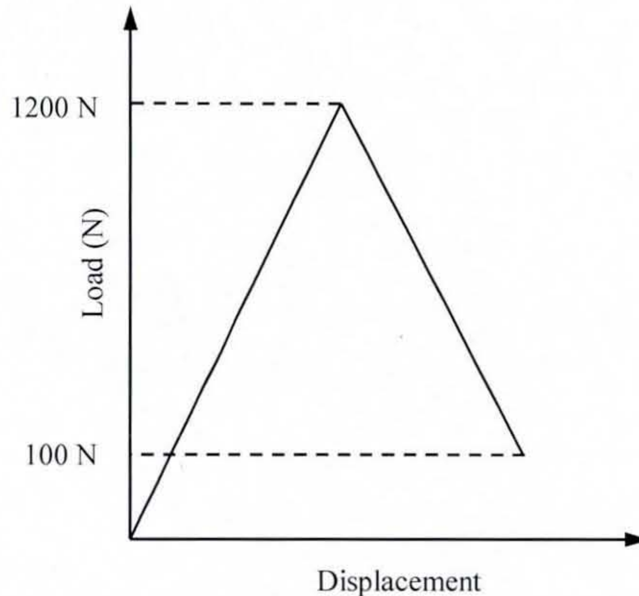


Fig. 6-3: Load profile used for tensile test of copper

$$\delta_c = \frac{PL_c}{AE_c} \qquad 6.3$$

where P is the applied load, L_c, A and E_c are the length of copper specimen, its area of cross section and the Young's modulus of copper, respectively. The Young's modulus of copper is obtained from the experimental stress-strain data; this is a cumbersome task since the proportional limit for metals occurs at a very small displacement. Therefore, a low displacement rate was used in the experiment so that enough data

was captured. The initial linear part of the stress-strain curve within the 0.01 percent permanent set and the linear part of the unloading curve was chosen as the region for calculating loading and unloading Young's modulus, respectively. According to ASTM standard E111-04 [25], the slope of this region corresponds to the Young's modulus of an material. In Fig. 6-4 the regions used for the Young's modulus calculation in the loading and unloading part of the stress-strain curve are shown. The calculated values of the Young's modulus for both loading and unloading are presented in Table 6-1 and comparison between these two is shown in Fig. 6-5. This comparison shows some variation in both loading and unloading stress-strain curves for the same composition samples and experimental conditions. However, the average data provides better estimation of the measurement if any random errors occur during testing as explained in section 6.2.3. Therefore, the calculated Young's moduli were averaged. The agreement between the average Young's moduli for loading and unloading is very good and also compares very well with literature data according to which the Young's modulus of

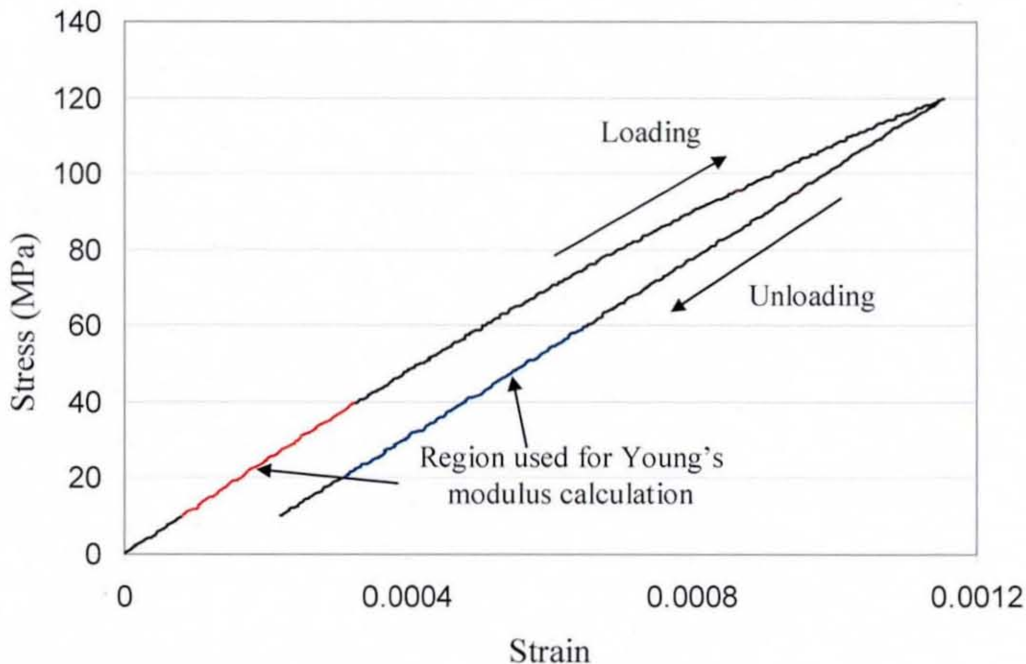


Fig. 6-4: Experimentally obtained stress-strain curve for C103 copper

Table 6-1: Young's modulus measurement for C103 copper

Sample	Young's Modulus (GPa)	
	Loading	Unloading
1	97.1	105.5
2	116.5	106.5
3	117.5	115.6
4	112.0	105.1
5	115.3	115.0
6	99.2	108.9
7	109.4	102.7
8	110.3	104.5
Average	**109.7**	**108.0**
Standard deviation	**7.7**	**5.0**

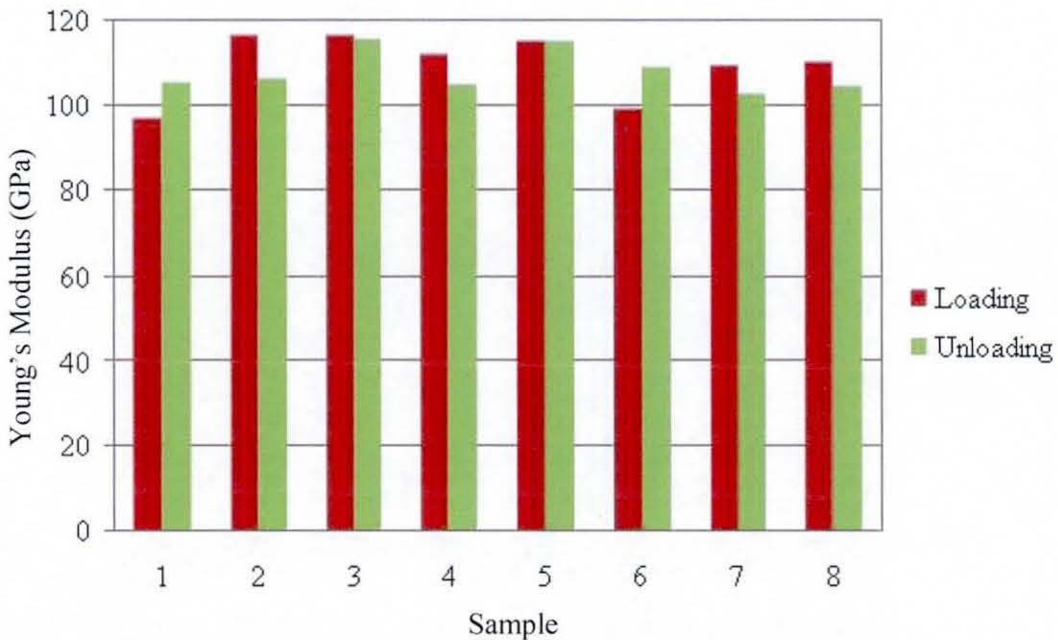


Fig. 6-5: Measured Young's modulus for copper

copper varies from 110 GPa to 125 GPa depending on its chemical composition and the strain rate used in the experiment [116]. Therefore, in the calculation of the solder joint deformation, the average magnitude of the Young's modulus from the loading part of the stress-strain is considered. The good comparison of Young's modulus between literature data and experimentally determined demonstrates the validation of displacement measurement using the Instron extensometer.

6.2.3 Determination of Required Sample Size

In any experiments, there will be measurement errors and some of these errors are random. No matter how sophisticated is the design of the testing machine and measuring system, inaccuracy in the system is difficult to avoid, and therefore, some errors could occur during testing. For example in these experiments, the electromechanical driven crosshead of the testing machine uses a gear reduction system and lead screws to move it up or down. Any backlash in this system can introduce an error in to measurements. Another example of an error could be specimen slippage in the grip while testing. Sometimes errors can also be introduced due to slippage of the extensometer. Differences in dimensions between specimens may also introduce an error in spite of the similar fabrication procedure being used. Correct alignment of the grips and the specimen, when clamped in the grips, is important. Offsets in alignment will create bending stresses which will result in a lower tensile stress for a given load. Some of these sources of errors, such as backlash in gears, slippage in the extensometer, etc. are unavoidable and very difficult to distinguish from the extensometer reading. It is clear from the above experiment that even though all of the copper specimens were made from one larger sheet and the same measurement technique was used, variation in the measured value of Young's modulus exists. However, the average Young's modulus value for the sample size of 8 compares very well with the lower extreme of published data. Therefore, it is wise to establish an average value from a number of samples instead of relying on data from one sample. The number of specimens is called the sample size. According to ASTM standard E 105-58, the required sample size, N_s, can be determined from the following equation [117]:

$$N_s = \left(2.56 \frac{\sigma_{sd}}{E_r} \right)^2 \qquad 6.4$$

where σ_{sd} is an advance estimate of the standard deviation of the sample size or lot, E_r is the maximum allowable error between the estimate to be made for the specimens and the actual average of the whole population, and 2.56 is a factor corresponding to a 1 % probability that the difference between the specimen estimate and the true average of whole population is greater than E_r. The approximate precision desired for the

estimate must be prescribed. That is, it must be decided what maximum deviation, E_r, can be tolerated between the estimate to be made from the test specimens and the average that would be obtained by measuring the whole population.

The sample size required for the solder joint experiments was calculated based on the results from the copper testing. With such a wide published range of the Young's modulus i.e. 110 GPa to 125 GPa, the average Young's modulus of copper from the literature was assumed to be 117.5 GPa. Thus, the expected average value of experimentally calculated Young's modulus was 117.5 GPa, but the obtained value of Young's modulus was 109.7 GPa. The difference between the average of published values and the experimentally obtained value, 7.8 GPa is considered to be the maximum allowable error, E_r, for calculation of sample size. The advance estimate of standard deviation (σ_{sd} = 7.7) was also taken from the copper experiment, which is presented in Table 6-1. Hence the required the sample size, n, was estimated from Eq. 6.4 to be:

$$N_s = \left(2.56\frac{7.7}{7.8}\right)^2 = 6.4$$

So, in all of the subsequent solder joint experiments, 7 (i.e. the next largest integer number) specimens were tested.

6.3 Tensile Test for Reflowed Bulk Solder

This section discusses the determination of the stress-strain properties for Sn3.8Ag0.7Cu bulk solder. This enables the comparison with the properties obtained for small-scale solder joints, which is discussed later in this chapter.

6.3.1 Specimen Fabrication and Mechanical Test

In the fabrication of bulk solder specimen, Sn3.8Ag0.7Cu solder paste was placed into a ceramic container with internal dimensions of 65 mm (length) × 10 mm (width) × 5 mm (depth). This container with the solder paste was reflowed in a planar T-TRACK reflow oven (Fig. 6-6). The oven is controlled by a computer program to follow the required reflow profile for reflow soldering and the actual reflow profile used is shown

in Fig. 6-7. It shows the air temperature in the oven as well as the ceramic container temperature, which was measured using a thermocouple. The maximum air temperature in the oven at dwell is 543 K, which resulted in the peak container temperature of 523 K. Since the ceramic container needs longer to heat up, more time is needed to achieve the required reflow temperature. The liquidus temperature for this solder alloy is 490 K and the reflow time is 120 – 150 seconds as per the IPC/JEDEC J-STD-20C standards [118].

Fig. 6-6: Planer T-TRACK reflow oven

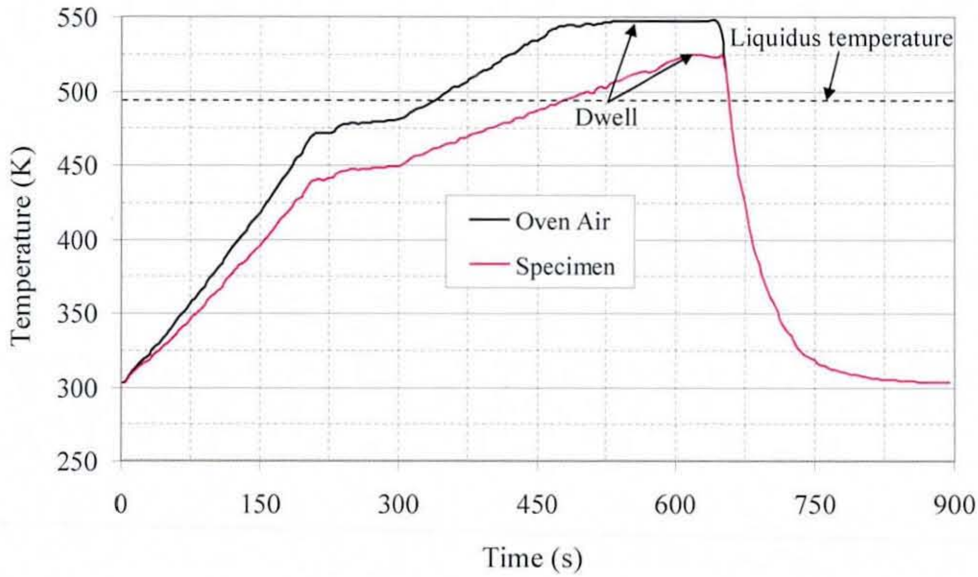


Fig. 6-7: Temperature profile used to fabricate bulk solder specimen

As discussed in chapter 3, the cooling rate plays a very important role in the solidification of the solder joint by affecting its microstructure. Generally, in surface mount soldering, a cooling rate between 1-2 K/s is used. Therefore, the cooling rate used in the solidification of the solder was about 1.5 K/s. To achieve this cooling rate, an external fan was used since the cooling rate achieved by the oven was insufficient.

After the solidification of the solder, it was carefully ground to bring its size down to 55 mm (length) × 7.5 mm (width) × 2 mm (thickness) as shown in Fig. 6-8 (a). Next, the specimen was milled to a dog bone shape as shown in Fig. 6-8 (b) along with its final dimensions, which were measured using a vernier caliper. These dimensions conform with the ASTM standard on tensile testing of metallic materials [119]. Finally specimens were polished using 800 grit paper, as shown in Fig. 6-8 (c).

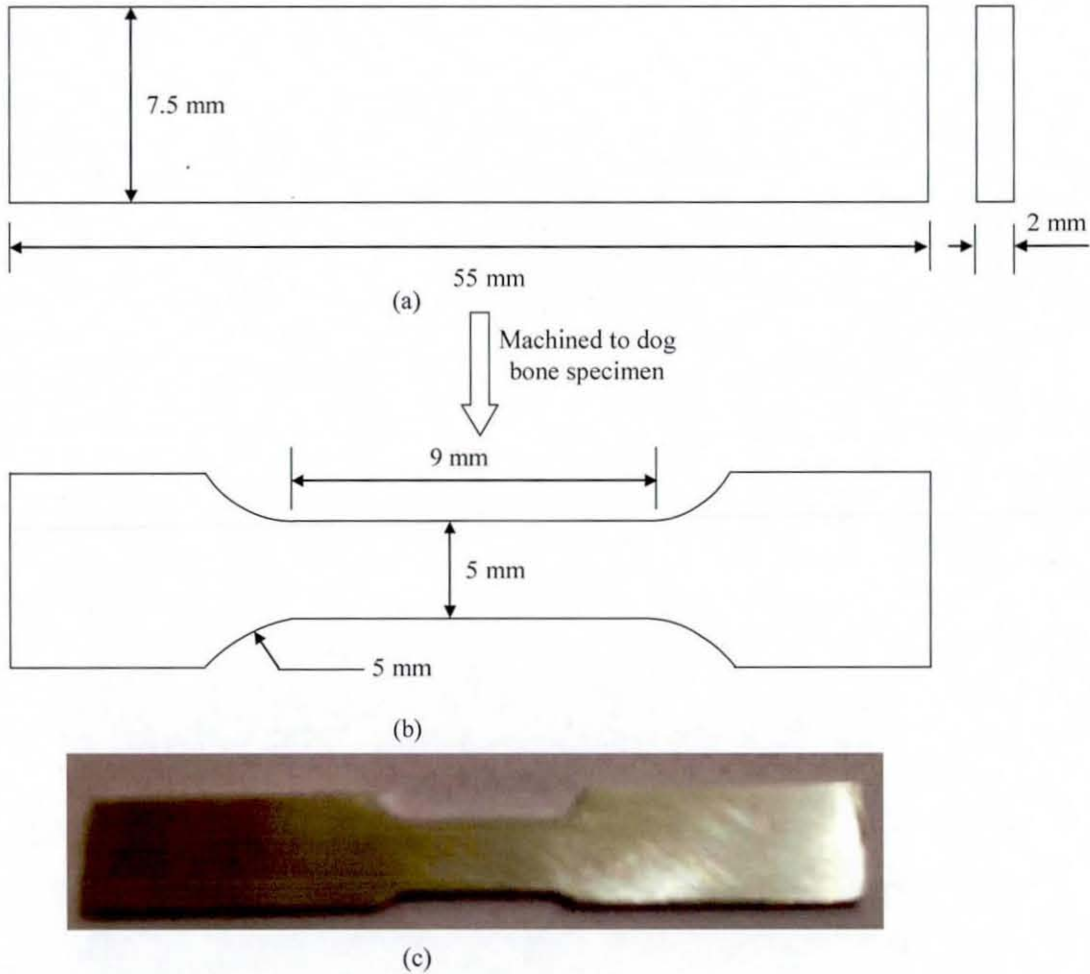


Fig. 6-8: Fabrication of bulk specimen: (a) ground specimen after reflow; (b) final fabricated specimen; (c) actual specimen after final polish

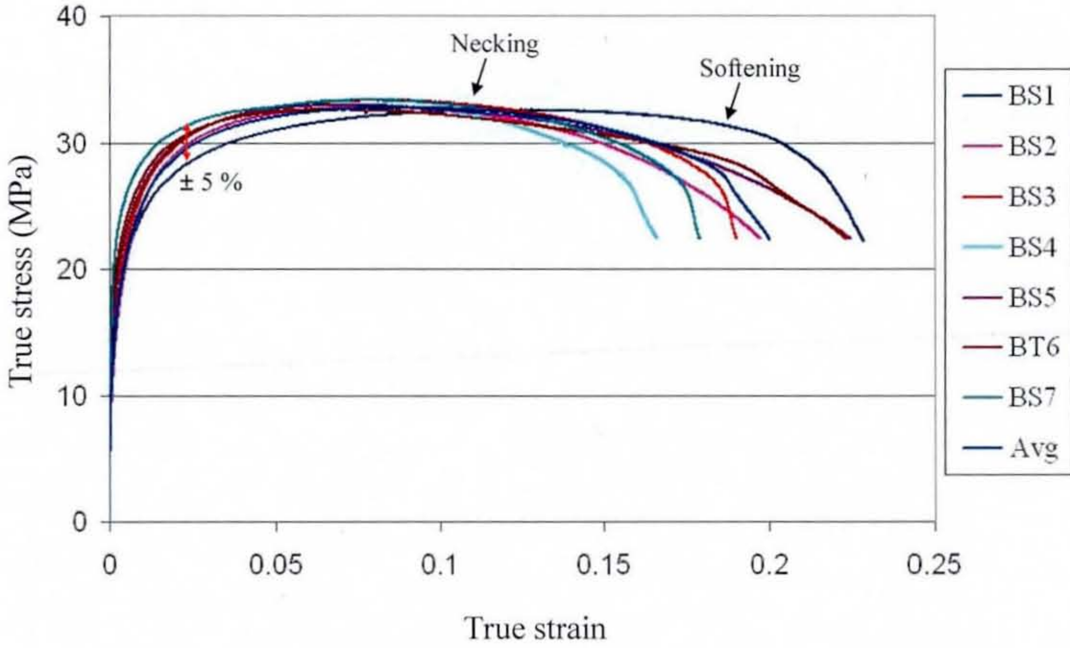
6.3.2 Tensile Test Methodology

The tensile tests for obtaining stress-strain data for the bulk solder were carried out using the same Instron MicroTester which was used for the copper specimen tensile tests. The displacement measurement was achieved using an extensometer. Since the specimen was made of a single material, the measured extensometer displacement (δ_{ext}) would directly give the deformation taking place in the solder material within the specific gauge length. As discussed in Chapter 2, the apparent stress-strain properties of metals depend on the strain rate. In order to study this strain-rate dependency, a displacement-controlled method of testing was adopted. In this method, a specific displacement rate is applied, which results in a constant strain rate. The Instron Bluehill software gives a wide variety of control methods such as stress, strain,

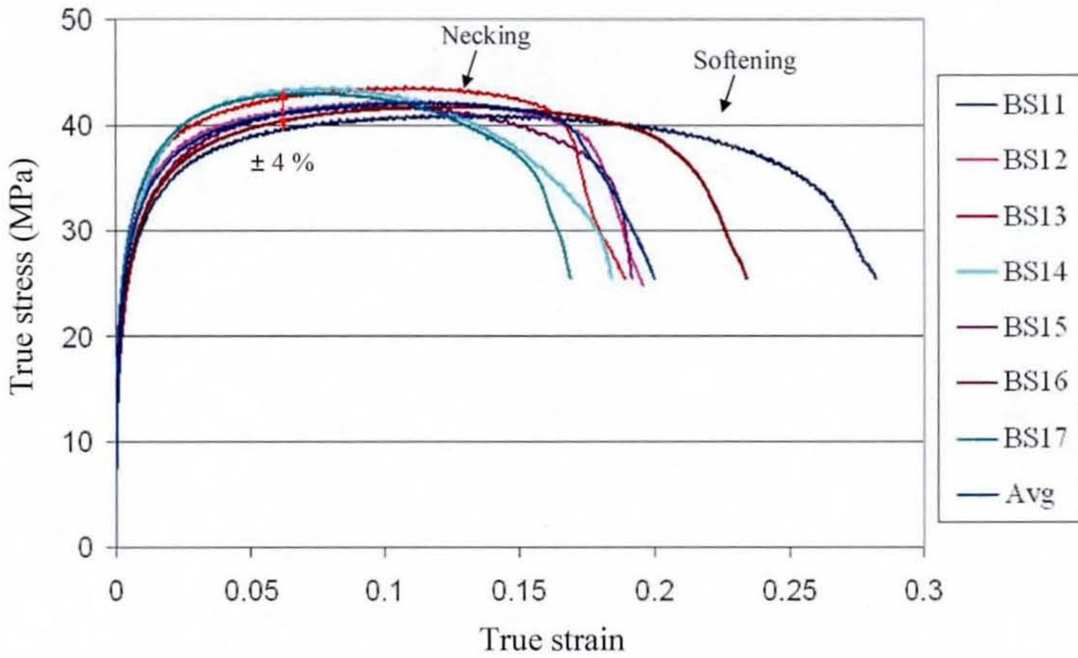
displacement etc. for mechanical testing. The displacement rate in the MicroTester is controlled by the displacement of the actuator. In a tensile test three different displacement rates were selected in such a way that the resulted strain rates do not fall into the creep regime. This was decided based on the time spent at the maximum stress level (saturation stress) during trial tests. The three displacement rates were 0.005 mm/s, 0.05 mm/s and 0.5 mm/s resulting in average strain rates of 0.00036 s^{-1}, 0.0037 s^{-1} and 0.0357 s^{-1}, respectively. Finally, true stress-strain data were calculated using Eqs. 2.11 & 2.12. For each strain rate 7 specimens were tested and the average true stress-strain data were calculated.

6.3.3 Results and Discussion

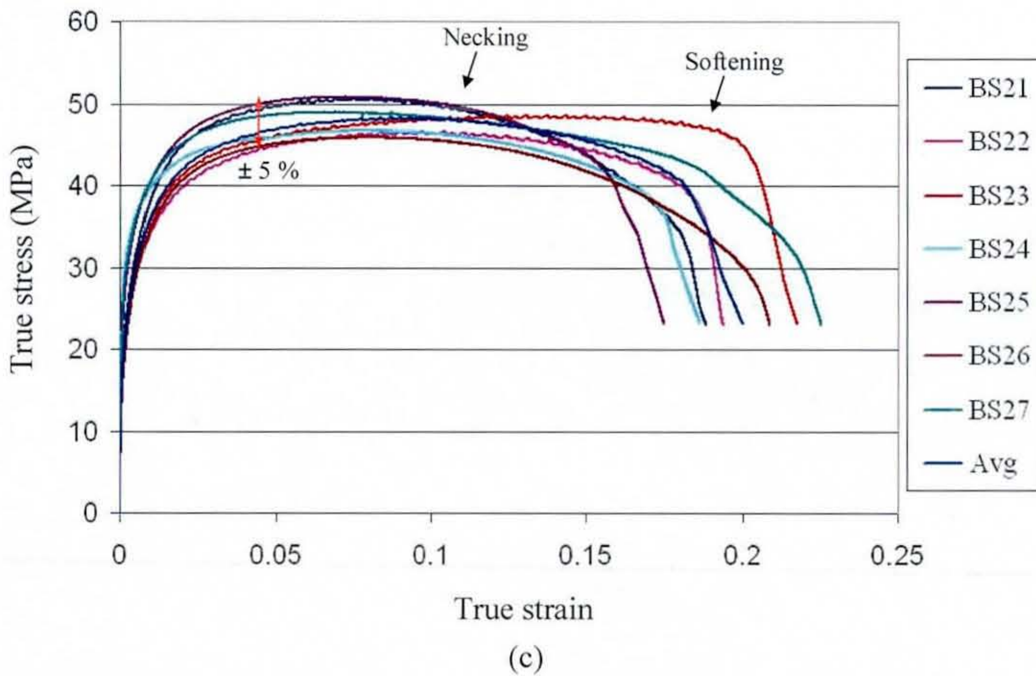
The experimentally obtained true stress-strain curves for the bulk solder specimens at a strain rate of 0.00036 s^{-1} are presented in Fig. 6-9 (a). These curves were not corrected after necking because softening part of the stress-strain curve was not important in the comparison study. 7 specimens were tested and the average stress-strain curve was obtained. The elastic parts of the stress-strain curves are very similar for all the specimens, while a slight scatter is observed in the hardening part of the plastic region. A ± 5 % spread in the data is observed at the beginning of the plastic region, which decreases as plasticity progresses. It is clear from the softening part of the stress-strain data that microstructural changes taking place in the solder during plasticity have a major impact during this stage. Therefore, a notable scatter of the stress-strain data is observed in this region. The true stress-strain data for other strain rates, i.e. 0.0036 s^{-1} and 0.0357 s^{-1}, are shown in Fig. 6-9 (b) and (c), respectively. It is obvious from these stress-strain data that the variations are similar to those observed at 0.00036 s^{-1}. Again, the elastic parts of the stress-strain curve are (very) similar, while some spread is observed in the non-linear part of the stress-strain curve. However, from comparison of the stress-strain data for the bulk material and the solder joint, the scatter for the bulk solder is lower with a maximum scatter of ± 5 % up to the end of the strain hardening portion of the graphs, compared with 15 % for the joints.



(a)



(b)



(c)

Fig. 6-9: True stress-strain data for bulk reflowed solder at strain rates: (a) 0.00036 s^{-1}; (b) 0.0037 s^{-1}; (c) 0.0357 s^{-1}

The average stress-strain curves for the three strain rates are shown in Fig. 6-10. As the strain rate increases the maximum load carrying capacity of the solder increases. The effect of the strain rate on the stress-strain behaviour of the bulk solder material is considered in terms of the Young's modulus, yield stress and ultimate strength. In experiments with the bulk solder, the displacement measurement was good enough to capture sufficient data below the proportionality limit so that the Young's modulus can be calculated. The change in the apparent Young's modulus with strain rate, calculated according to ASTM standards [25], is demonstrated by Fig. 6-11. It increases approximately linearly in proportion to the log strain rate. Since there is no distinguishable yield point for the tested solder alloy, it is calculated based on the offset method recommended by the ASTM standard. The variation of both the yield stress (YS) and the ultimate tensile strength (UTS) is shown in Fig. 6-12. This demonstrates that both the YS and the UTS increases nearly linearly with the applied strain rate, which is a common feature in metals.

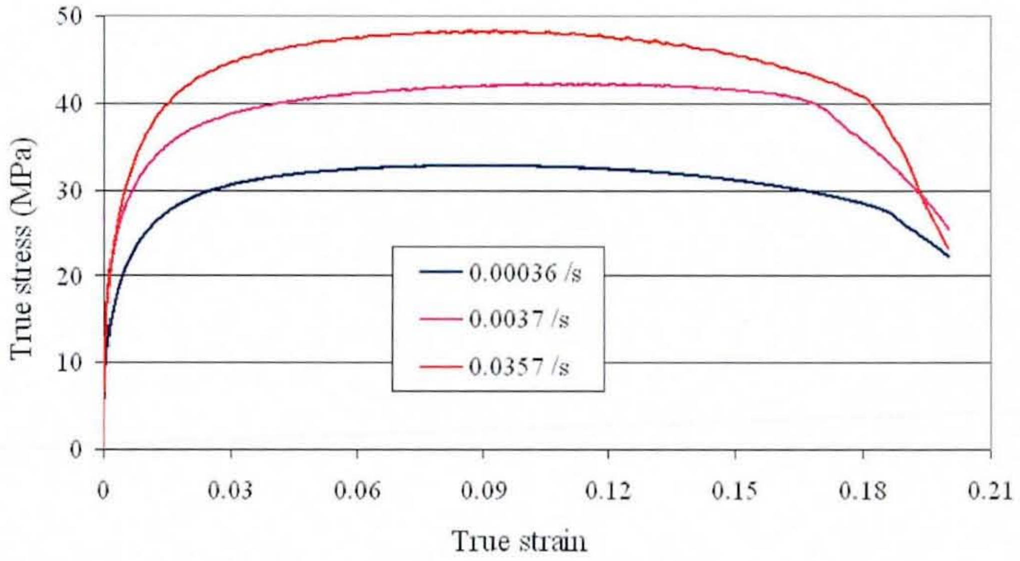


Fig. 6-10: Average stress-strain curves for bulk solder at different strain rates

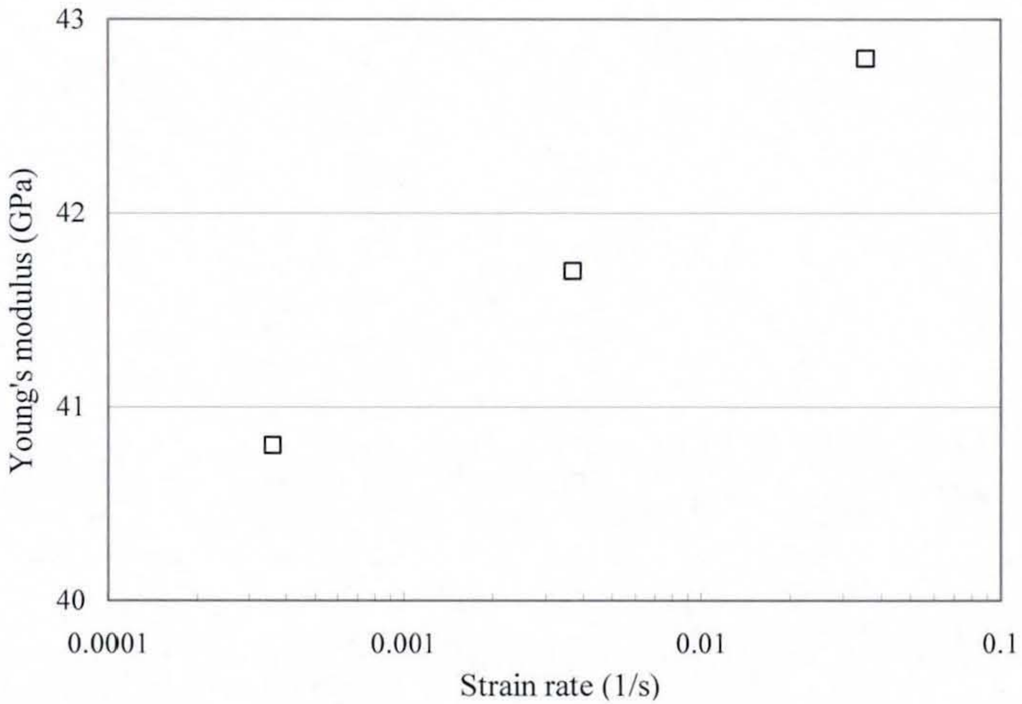


Fig. 6-11: Effect of strain rate on Young's modulus of bulk solder

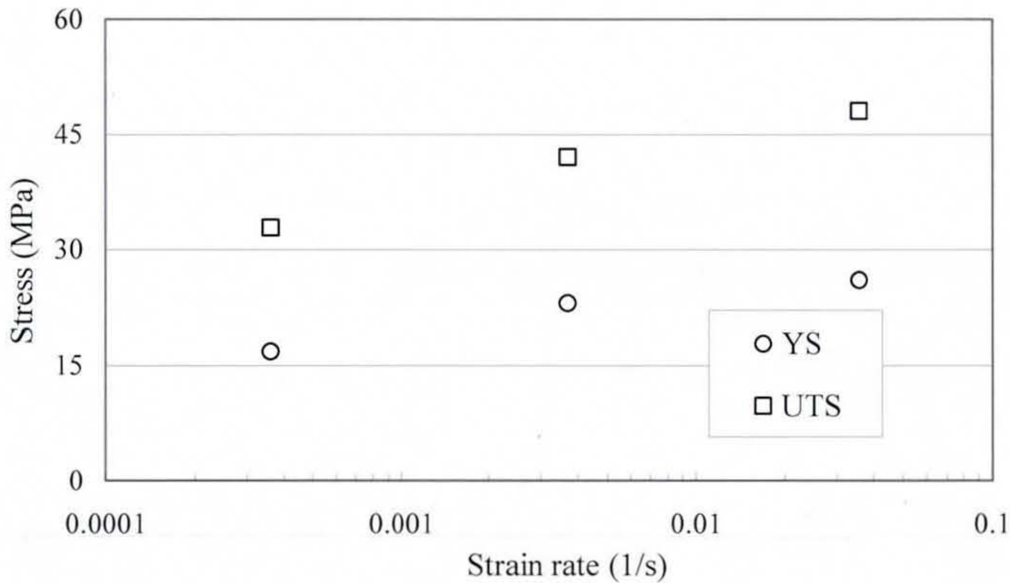


Fig. 6-12: Effect of strain rate on yield stress (YS) and ultimate tensile strength (UTS) of bulk solder

6.4 Tensile Testing of Small-Scale Solder Joints

In order to obtain the material properties of actual solder joints, tensile experiments were carried out for reflowed small-scale Sn3.8Ag0.7Cu solder joint specimens. These experimental results make it possible to compare the properties obtained for small-scale solder joints and bulk material manufactured using similar fabrication processes and analyse the factors contributing to variations. In this section, the fabrication of small-scale solder joint specimens and their properties measurement results are discussed.

6.4.1 Specimen Preparation for the Tensile Tests

To obtain the stress-strain properties of the solder joint, the same commercial solder paste, containing Sn3.8Ag0.7Cu powder was used to fabricate small-scale solder joints. The solder particle size ranged from 25 μm - 45 μm, and the paste contained a rosin flux. Flux is used to clean soldering surfaces and remove any oxide layer present to promote good wetting. The paste is specially designed for surface mount soldering, and is therefore suitable for fabrication of small-scale solder joints. The solder joints were formed in a gap between two C103 copper substrates to ensure both reliable bonding with the solder and rigidity for subsequent mechanical tests. In the experiment a 1 mm thick copper sheet was used and cut in to pieces 60 mm × 17 mm,

as shown in Fig. 6-13 (a). To create a small-scale solder joint in the copper piece, a slot was cut using a low-speed saw that is illustrated in Fig. 6-14. The low speed saw has a diamond cutting wheel with thickness 0.3 mm, which results in an approximate average gap of 0.34 ± 0.015 mm. The slot was cut to a depth of 14 mm to avoid separation of the copper piece into two parts. With this method it is easier to maintain the parallelism of two substrates after fabrication of the specimen. Having created the slot, one side of the copper was covered with a high-temperature tape. Then the solder paste was placed in the gap, the high temperature tape keeping it inside the gap. This copper piece, with the solder paste in its gap, then had the solder joint created using reflow soldering.

To reflow the solder, the Planer T-TRACK (Fig. 6-6) reflow oven was again used. Figure 6-15 shows the profile used for the fabrication of solder joints. In this case, the oven air temperature profile is slightly different from the previous profile (Fig. 6-7). Since the copper substrate heats up very quickly, the lag of the specimen temperature by oven air temperature was considerably small. Therefore, the maximum oven temperature in this profile was 523 K as compared to 543 K in the previous profile, and similar temperature profile was obtained for specimen as that used for the bulk specimen fabrication.

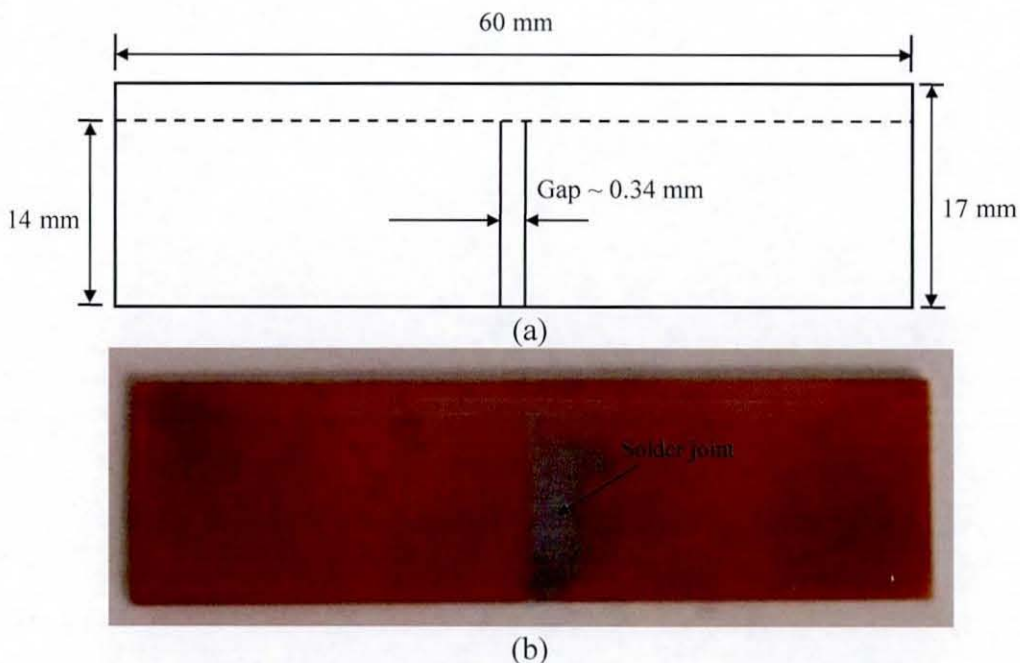


Fig. 6-13: Solder joint specimen fabrication: (a) dimensions of the copper pieces used; (b) an actual sample after reflow

Fig. 6-14: Buehler ISOMET low speed saw

In this fabrication process a cooling rate of about 1.5 K/s was used, which is similar to that used for fabrication of the bulk solder specimens. An actual specimen after reflow is shown in Fig. 6-13 (b). After the solder joint was fabricated, the sample was carefully hand ground to remove any extra solder that had spread over the copper surface and a planed (ground) specimen as shown in Fig. 6-16 (a) was obtained. Then the planed specimens were cut to a width of 10.5 mm using the low-speed saw (Fig. 6-16 (b)). The specimens were finally polished using 800 grit paper on all sides to make them ready for mechanical testing. The final dimensions (60 mm × 10.5 mm × 0.95 mm) of the polished specimens (Fig. 6-16 (c)) were measured using a vernier caliper. The solder joint gap length of each specimen was measured using a SIM universal optical measuring machine. Three measurements each on either side of the specimen were taken across the width of the solder joint. An average (0.34 $\pm$ 0.015 mm) of these measurements was considered as the gap length of the solder joint in the strain calculations. The specimens were fabricated in batches of 7 and these were stored at room temperature. Finally, these specimens were tensile tested within two days of their fabrication.

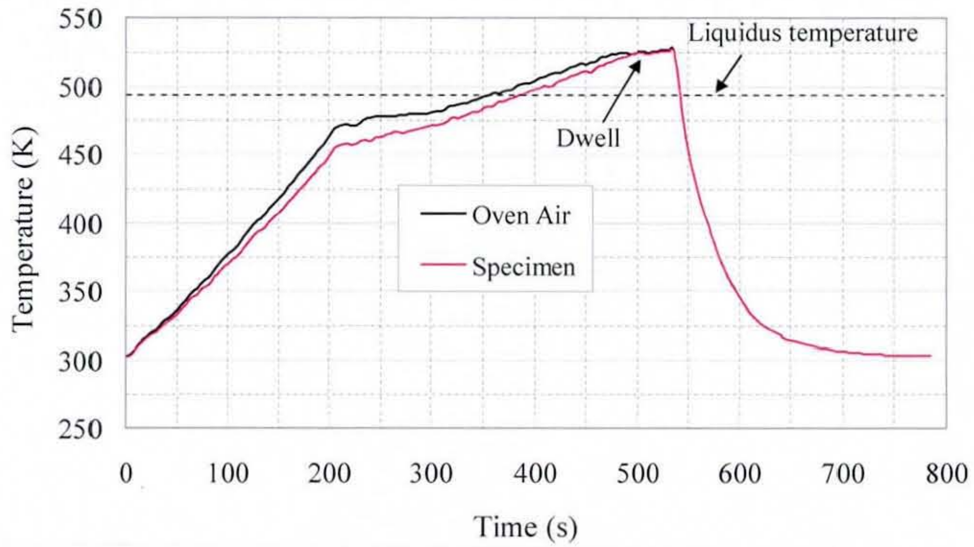


Fig. 6-15: Specimen temperature profile used to fabricate the solder joints

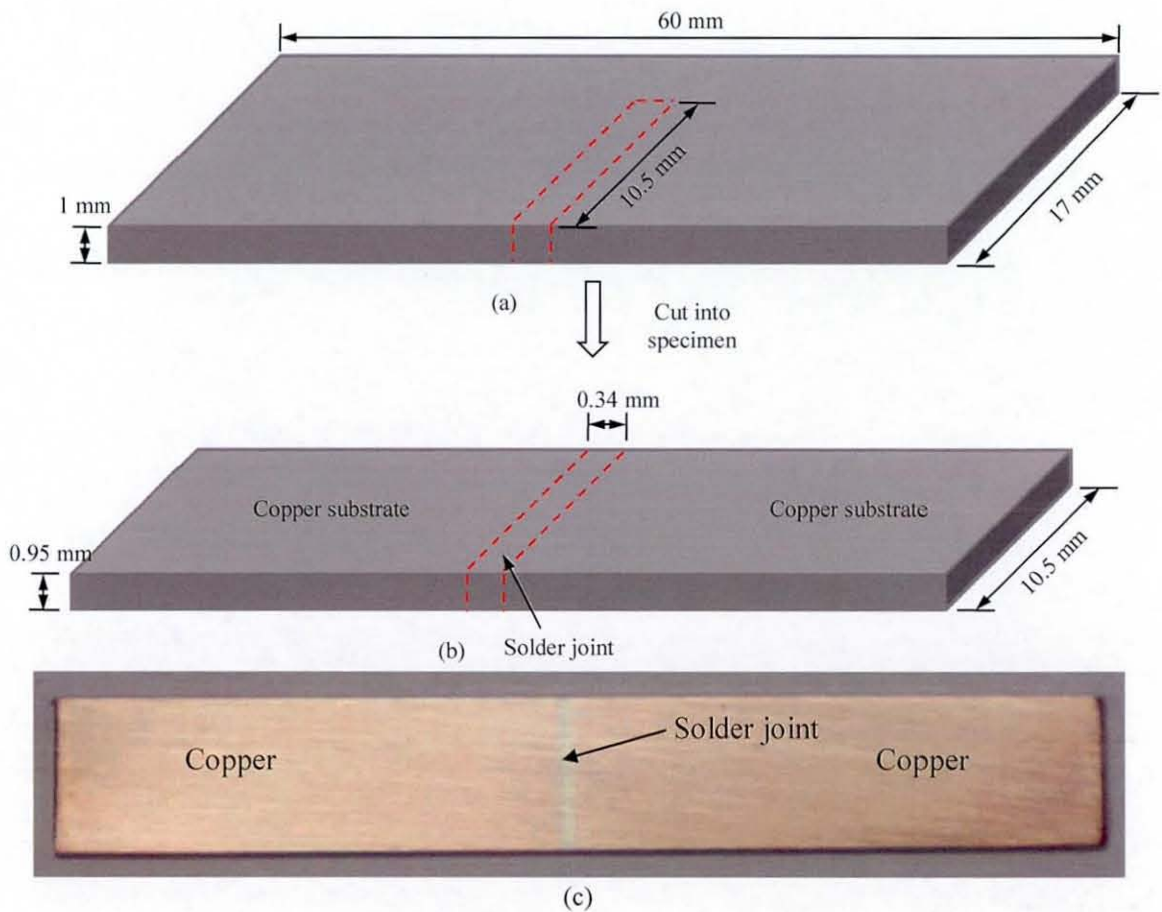
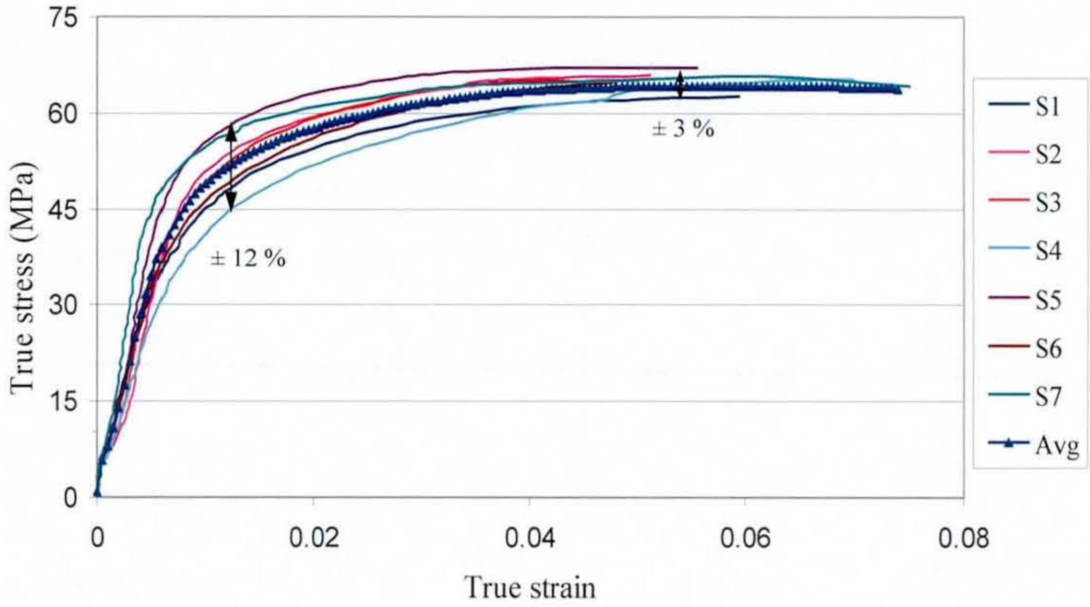


Fig. 6-16: Preparation of solder joint specimen: (a) ground specimen after reflow; (b) final fabricated specimen; (c) actual specimen after final polish

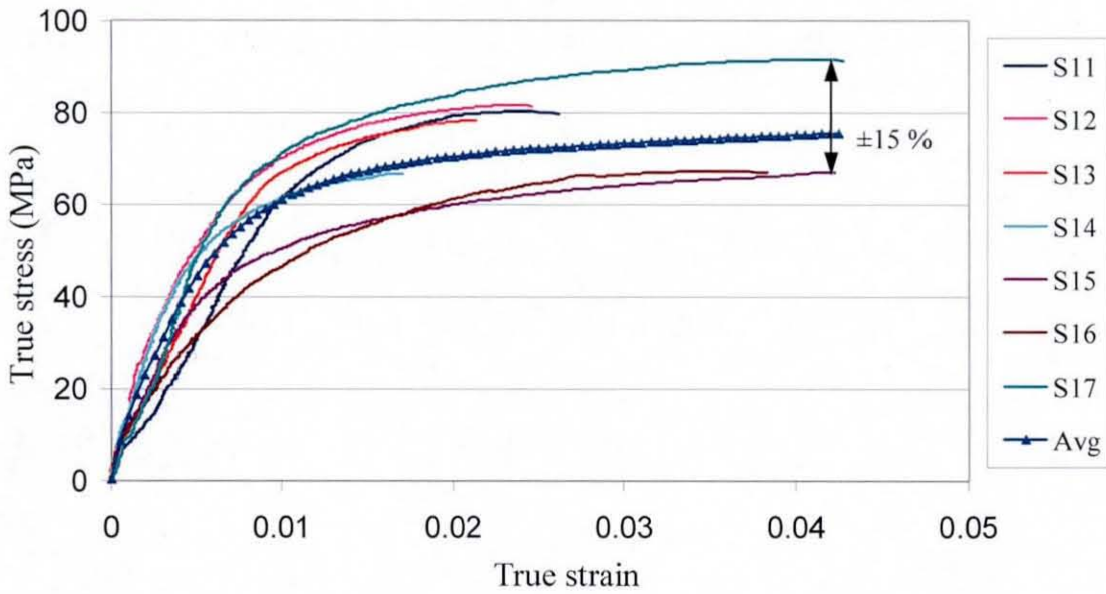
As for the bulk solder, the tensile tests were carried out for three different displacement rates. The displacement rates were selected in such a way that the resulting strain rates do not fall into the creep regime. This was decided based on the time spent at the maximum stress level (saturation stress) during trial tests. The displacement rates used were 0.005 mm/s, 0.05 mm/s and 0.5 mm/s, which resulted in average strain rates of 0.00075 s^{-1}, 0.004 s^{-1} and 0.013 s^{-1}. The load measurement was obtained directly from the load transducer, while the displacement measurement technique used in the experiments was explained in the previous section 6.2.2. Thus, for each specimen its load-displacement relationship was measured and engineering stress-strain data was calculated. Finally, true stress-strain data were calculated using Eqs. 2.11 & 2.12. For each strain rate 7 specimens were tested and the average true stress-strain data were calculated.

6.4.2 Results and Discussion

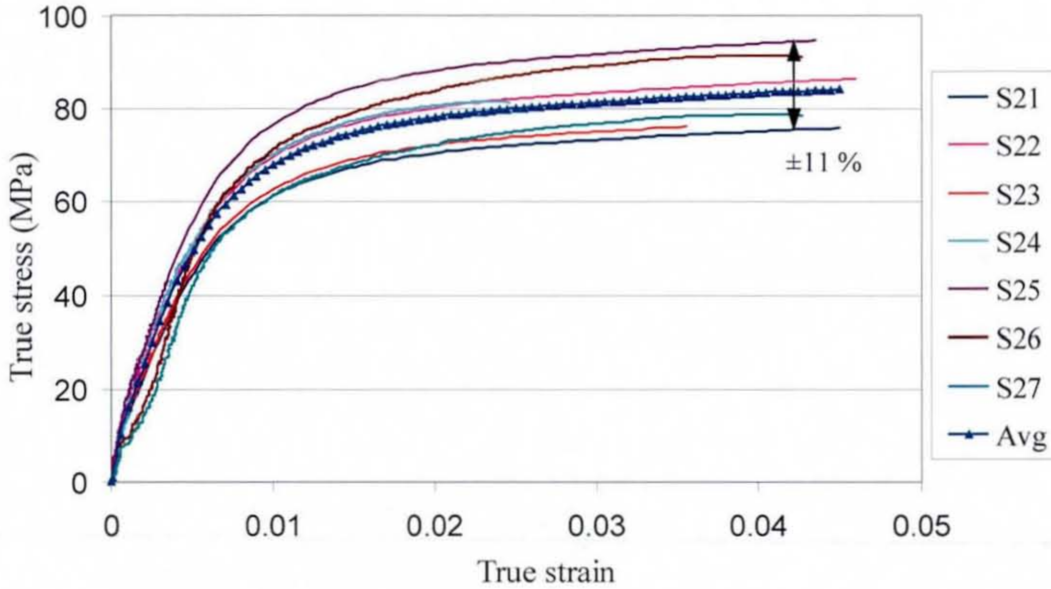
The experimentally obtained true stress-strain curves for the small-scale Sn3.8Ag0.7Cu solder joints are presented in Fig. 6-17 for an average strain rate of 0.00075 s^{-1}. An average for the 7 specimens is also presented in the same figure. It is clear from the stress-strain data that even though the dimensions and conditions of the fabrication process for solder joints were the same, the specimens have different responses for the same testing conditions. The elastic parts of stress-strain curves are similar, but the curves start deviating at the beginning of the plastic region, which is evident from Fig. 6-17 (a). The spread in the stress-strain curves with regards to the average has a maximum magnitude of $\pm$ 12 % in the early part of the plastic region and it decreases to $\pm$ 3 % toward the end of the test. The true stress-strain data for strain rates of 0.004 s^{-1} and 0.013 s^{-1} are given in Figs. 6-17 (b) and (c), respectively. These stress-strain data exhibit similar characteristics to those observed for the lower strain rate (0.00075 s^{-1}). Of the three strain rates, the data scatter is highest for 0.004 s^{-1} with $\pm$ 15 % deviation from the average, which is nearly constant unlike in the case of the strain rate of 0.00075 s^{-1}. The lowest deviation, $\pm$ 11 %, is observed for the higher strain rate of 0.013 s^{-1}. To understand the reason for the large scatter in the stress-strain data, a microstructure study discussed later was conducted for the tested solder joint specimens.



(a)



(b)



(c)

Fig. 6-17: True stress-strain data for tensile tests on solder joints: (a) at a strain rate of 0.00075 s^{-1}; (b) at a strain rate of 0.004 s^{-1}; (c) at a strain rate of 0.013 s^{-1}

A comparison of the averaged stress-strain data was carried out for the three different strain rates and is presented in Fig. 6-18. Since the stress-stress curves for the solder material are dependent on the strain rate, an increased strain hardening is exhibited by the lead-free Sn3.8Ag0.7Cu solder joints for the increased strain rate. Under high-rate loading, the time for any crystallographic deformation diminishes, resulting in an increased load necessary for the solder joint failure. The characteristics of the averaged stress-strain curves are very much the same, but the strain rate has an effect on the important parameters of the mechanical behaviour i.e. apparent Young's modulus, yield stress and ultimate tensile strength. The deformation of the solder exceeds the proportionality limit at low stresses/strains, making it difficult to capture enough data for accurate Young's modulus calculation. Therefore, only the plastic parts of the stress-strain curves were focused on in the analysis. The yield stress and the ultimate tensile strength were calculated for each strain rate, and their variation with the strain rate was studied. The estimation of the yield strength was based on the stress offset method [25]. Figure 6-19 shows the effect of strain rate (logarithmic scale) on both the yield stress and the ultimate tensile strength. As expected both parameters increased with the strain rate, and the variation is proportional to the log of the strain rate.

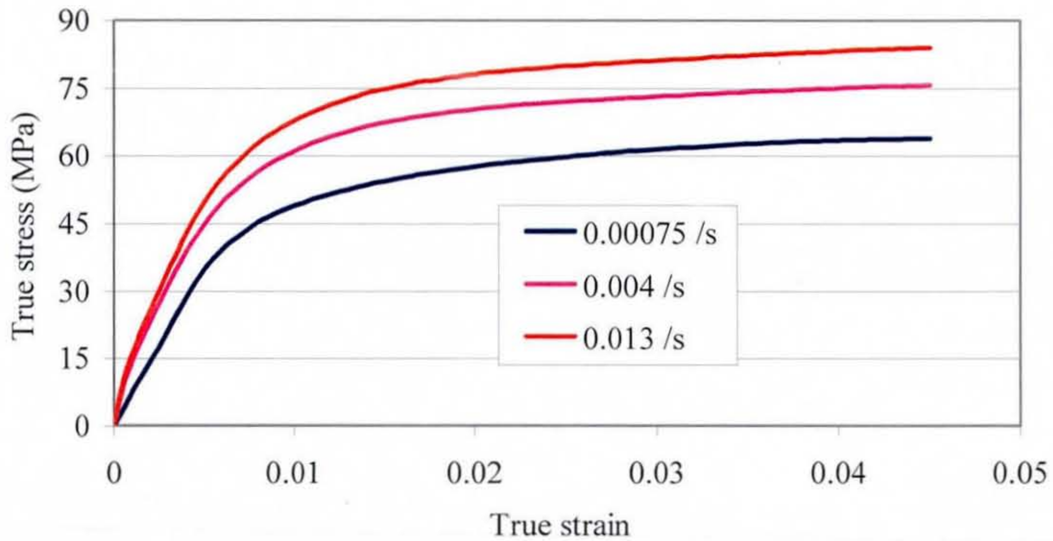


Fig. 6-18: Averaged true stress-strain curves for the three different strain rates

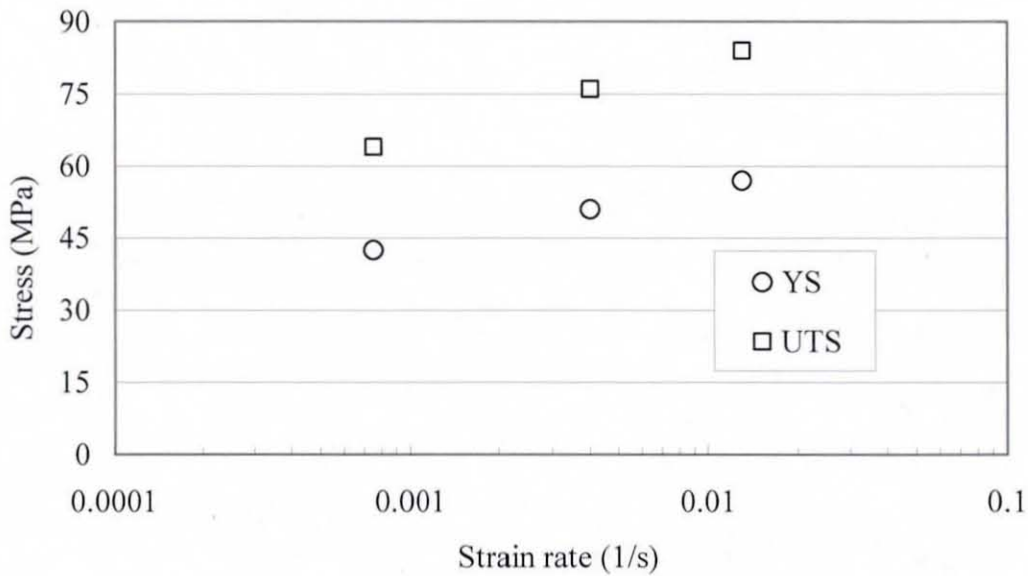


Fig. 6-19: Effect of strain rate on the UTS and YS

6.4.3 Parameter Determination for the Johnson-Cook Model

Based on the experimental stress-strain data for the three different strain rates, a constitutive equation can be fitted to the experimental data in order to account for the strain rate dependent mechanical behaviour. As discussed in chapter 2, the Johnson-Cook constitutive model is commonly used for metals and alloys to model the rate dependent plasticity [38, 40, 41]. The general form of this model is given by Eq. 2.30. Therefore, using the average stress-strain data for three different strain rates,

parameters for the Johnson-Cook constitutive equation were determined. This constitutive equation can include the effects of strain hardening, strain rate (viscoplastic behaviour) and temperature. However, the experiments were carried out only for room temperature conditions; therefore, temperature effects are neglected. The determined parameters, which can describe the plastic part of the stress-strain curve, are presented in Table 6-2. Using these parameters, a comparison of the stress-strain curves predicted by the Johnson-Cook equation with the experimental ones was made. Figure 6-20 shows this comparison for strain rate of 0.00075 s^{-1}, and these curves match well. The comparison of experimental and predicted plastic stress-strain curve for strain rates of 0.004 s^{-1} and 0.013 s^{-1} are shown in Figs. 6-21 (a) and (b), respectively, and these also compare well. Hence, using these parameters in the Johnson-Cook equation, stress-strain curves for solder joints can be successfully predicted for strain rates which are above the creep regime.

Table 6-2: Johnson-Cook parameters for Sn3.8Ag0.7Cu solder

A_1	B	C_1	n	$\dot{\varepsilon}_o$
27	95	0.0897	0.185	0.004

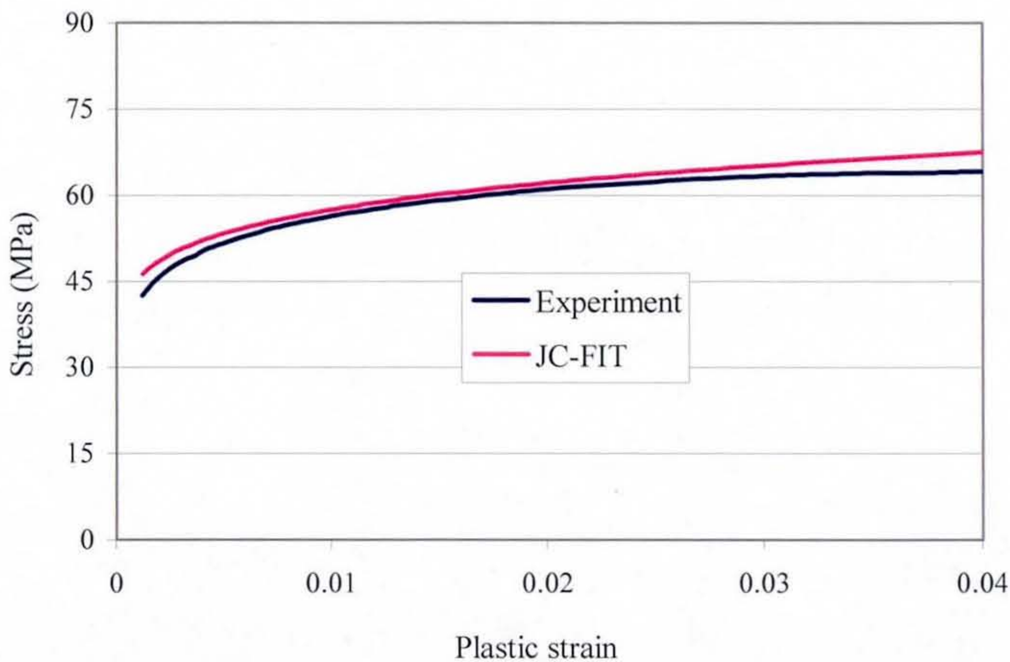
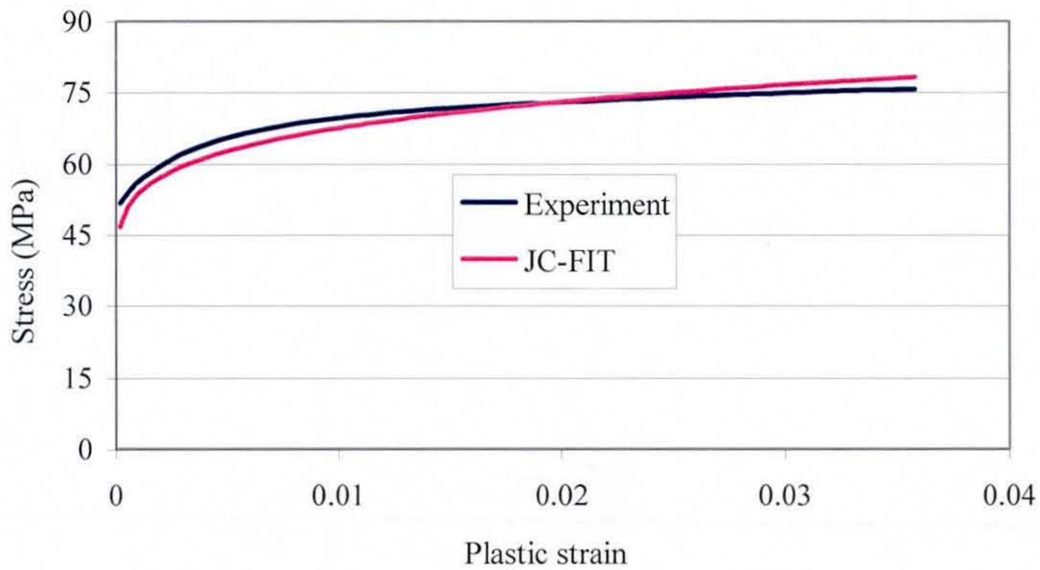
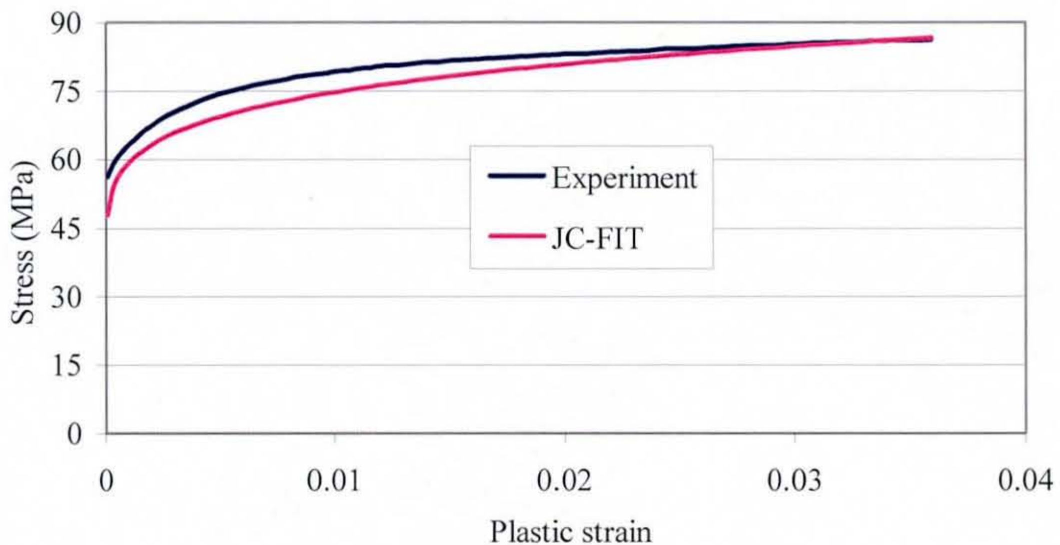


Fig. 6-20: Comparison of stress- plastic strain curve for a strain rate of 0.00075 s^{-1}



(a)



(b)

Fig. 6-21: Comparison of stress- plastic strain curves for strain rates of: (a) 0.004 s^{-1}; (b) 0.013 s^{-1}

6.5 Comparative Study of Stress-Strain Properties

Having measured the stress-strain behaviour for both small-scale solder joints and bulk solder, a comparison was carried out. The comparison of the yield stress for the two types of solder specimens is illustrated by Fig. 6-22 in semi-logarithmic coordinates. It is evident from the comparison that the solder joint yield strength is more than twice that of the bulk solder. The graphs show slight divergence as the

strain rate increases due to a higher strain rate sensitivity for the solder joints. Similar observations can be made for the comparison of the ultimate tensile strength (Fig. 6-23), where the tensile strength in the solder joints is higher by a factor that is slightly less than 2.

The comparison of averaged stress-strain curves indicates that in the case of small-scale solder joints, strain softening is hardly present. Unlike the reflowed bulk solder, the fabricated solder joints have copper substrates on either side, which are still in the elastic state and constrain the solder joints from plastic deformation. Therefore, during the tensile testing the solder joints failed without showing significant strain softening. In order to understand the higher solder joint properties over bulk solder, the size and microstructure effect studies were conducted. Therefore, the following section discusses the effect of size and constraints on the solder material properties.

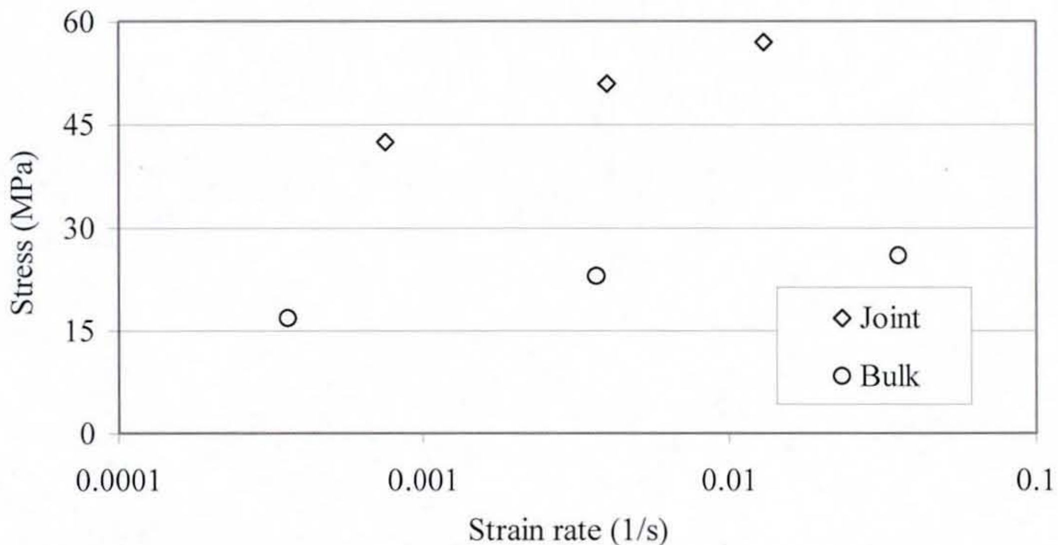


Fig. 6-22: Comparison of average yield stress for solder joints and bulk solder

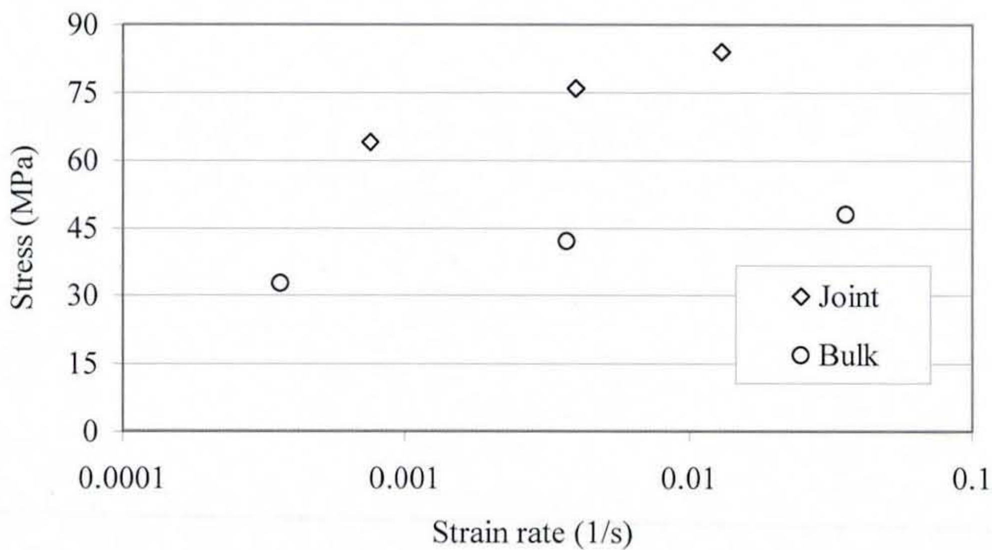


Fig. 6-23: Comparison of average UTS for solder joints and bulk solder

6.5.1 Effect of Size and Constraints

The effects of size and constraints on the solder joint were studied using finite element simulation of the tensile tests on the fabricated solder joints. In the finite element analysis 1/8th of the fabricated solder joint specimen was considered, as shown in Fig. 6-24. A parametric model of the geometry of the 1/8th of the solder joint specimen was built. The gap (g), which represents the axial size of the solder joint between the two copper substrates, was varied along with the length (L) of the specimen to keep the gap to length ratio (g/L) constant for all geometries of the joint. With this approach the effect of the size of the solder joint, due to varying gap to thickness (g/t) ratio, could be studied. The gap was varied between 0.15 mm and 1.5 mm. Since the gap is small compared to the total length of the geometry, capturing the stress field in the solder joint was difficult with the full model. Therefore, the analysis was carried out in two steps. In the first step, a full-model analysis with a coarse mesh was carried out in order to obtain the displacement field for the submodel used in the second step. In this step a sub model of the full FE model, which is shown in Fig. 6-25, was built with a high mesh density near the solder joint, which is the area of interest. The cut plane for the submodel was chosen so that it is sufficiently far from the solder joint and does not affect the developing stress field in it. The distance of the cut plane from the transverse symmetry plane used is illustrated in Fig. 6-25.

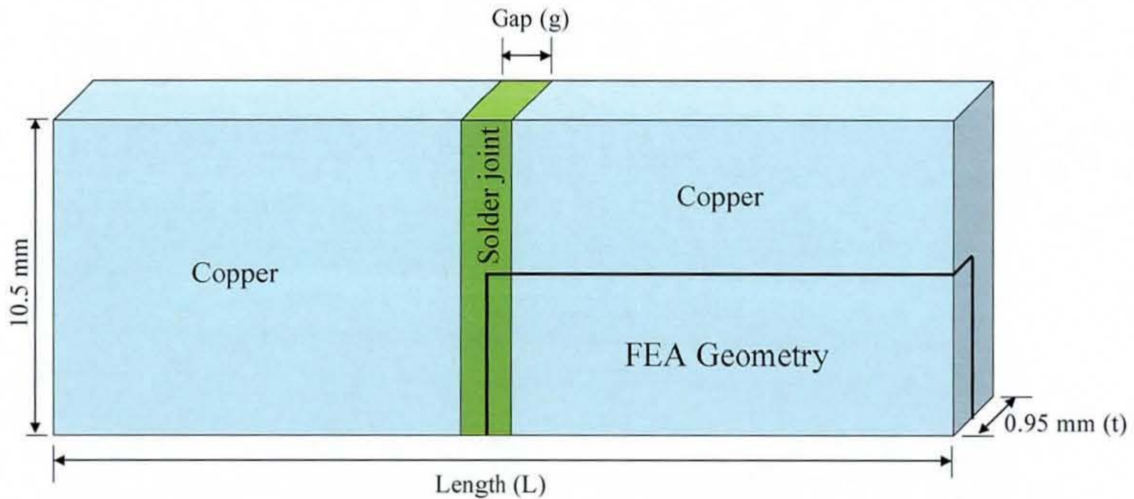


Fig. 6-24: Geometry of solder joint specimen and its octant used in full model analysis

In the finite element analysis, the solder joint was modelled using the homogeneous bulk solder material properties as measured for the strain rate of 0.00036 s^{-1}. A comparison of the experimental and simulated stress-strain curves is presented in Fig. 6-26. The simulated stress-strain curve was created using the multi-linear isotropic hardening material model due to the monotonic uniaxial tensile loading. The copper substrate was modelled as linear elastic with a Young's modulus of 110 GPa and Poisson's ratio of 0.343.

The finite-element modelling was performed using 8-noded 3D hexahedral structural solid elements. The mesh used for both full and sub models with a solder joint gap of 0.35 mm is illustrated in Fig. 6-27. The symmetry boundary conditions used in the full model and submodel are shown in Fig. 6-25. The displacement boundary condition was applied at the far end-face of the full model (Fig. 6-25) and the value of the applied displacement is such that the maximum total equivalent strain induced in the solder joint is about 11%. This value is selected so that the ultimate tensile stress of (32.6 MPa measured) for the strain rate of 0.00036 s^{-1} was achieved in the solder joint. After the full model is analysed, the displacements are extracted at the cut plane and applied to the submodel along with the symmetry boundary conditions.

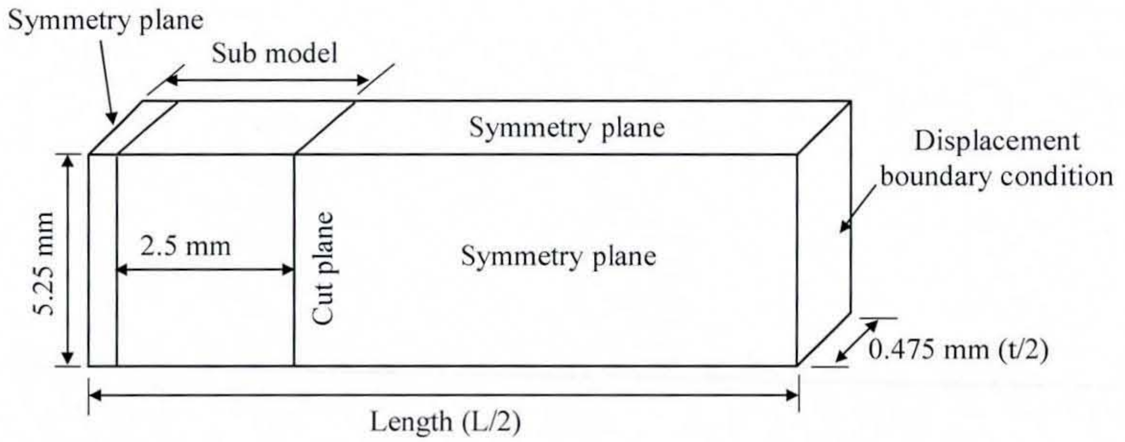


Fig. 6-25: Full model, sub model and boundary conditions for the FEA

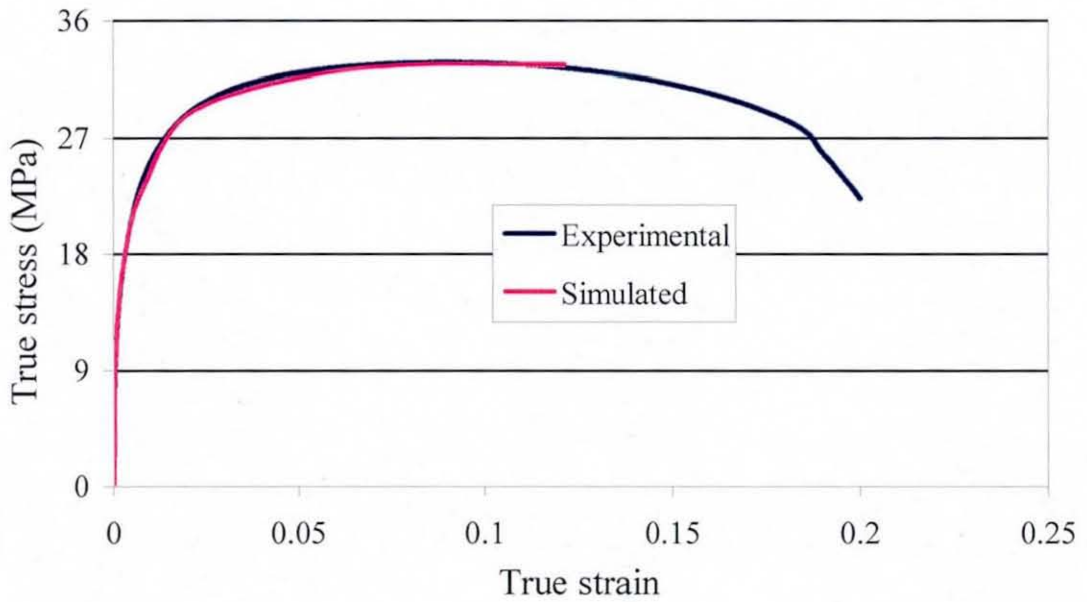


Fig. 6-26: Experimental and simulated stress-strain curves for the solder joint

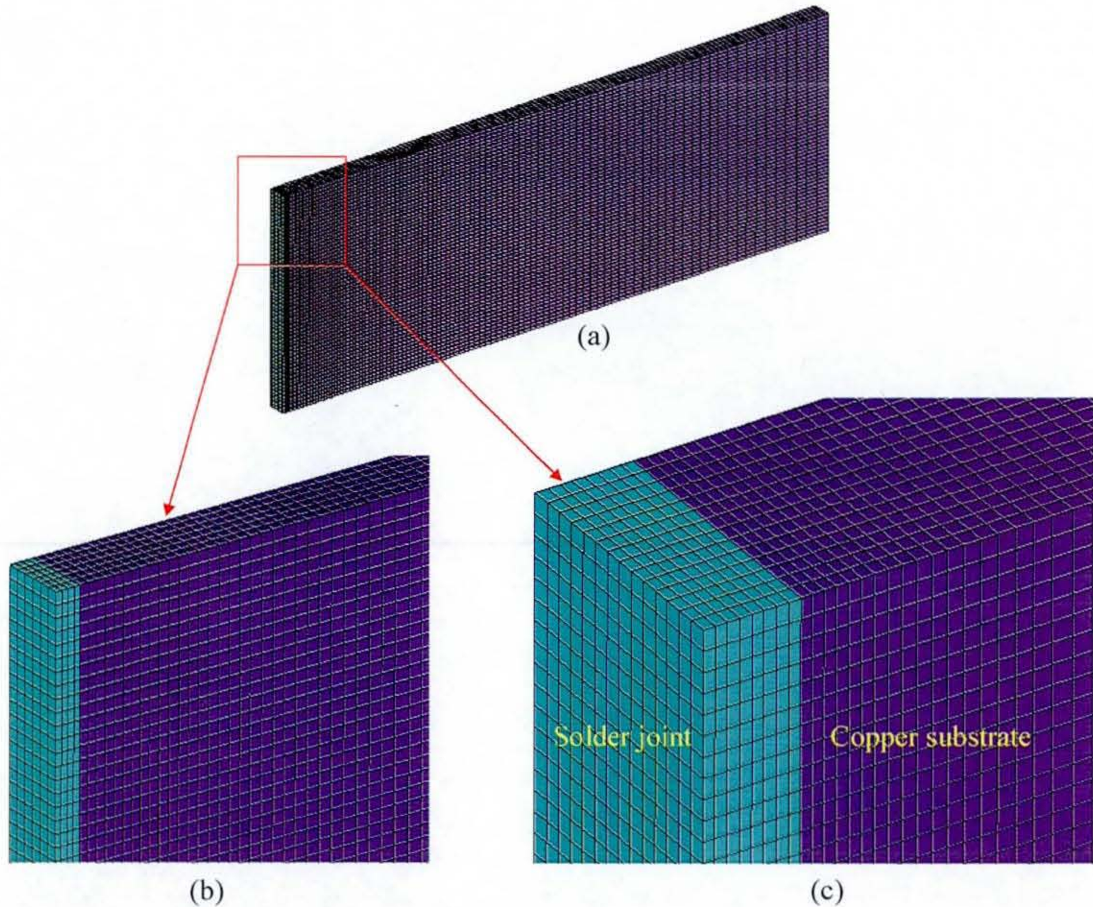


Fig. 6-27: Meshes used in the FEA: (a) full model; (b) zoomed view of full model; (c) zoomed view for submodel

The stress distribution in the solder joint for the two extreme gap lengths, 1.5 mm and 0.15 mm, are given in Fig. 6-28 and 6-29, respectively. For the solder joint gap of 1.5 mm, the equivalent stress is maximum at the center of the solder joint (i.e. on the symmetry plane) and diminishes towards the joint interface. The equivalent stress distribution in the 0.15 mm gap solder joint is quite different, with the maximum stress at the interface between the solder joint and copper. The comparison of equivalent stresses for these two extreme gap lengths illustrates the effect of the size of the solder joint. As the gap length increases, the plastic deformation taking place in the solder joint is less restricted by the copper substrate, which is in the elastic state. However, as the gap length decreases, the space available to accommodate the same amount of plastic deformation in the solder joint decreases and the copper plates constrain the transfer of this plastic deformation. The size effect on the solder joint is studied by calculating a dimensionless factor, S:

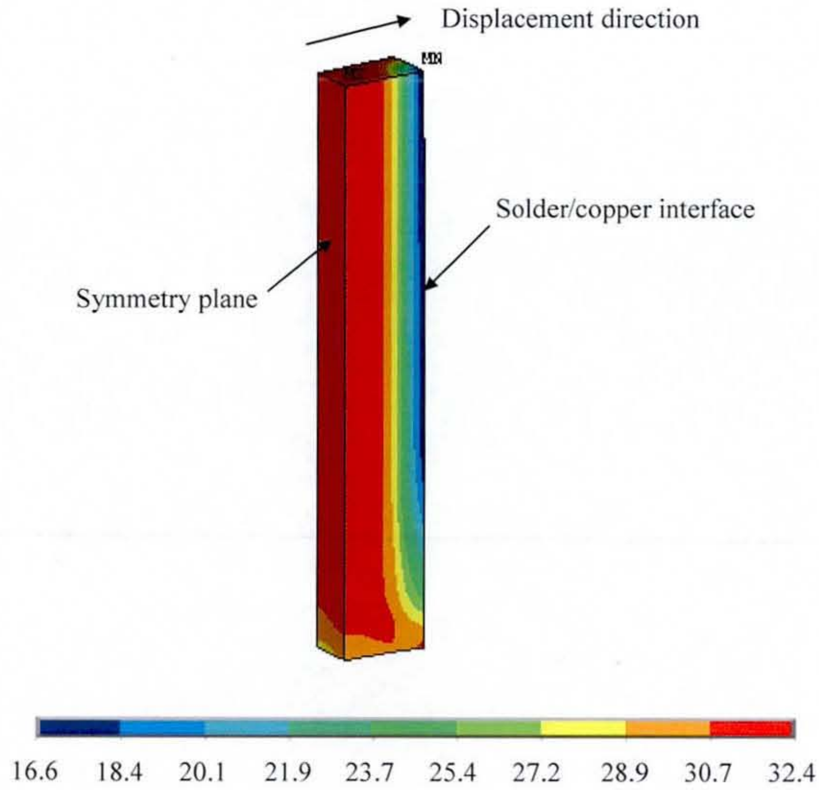


Fig. 6-28: Equivalent stress distribution in the solder joint with a 1.5 mm gap length

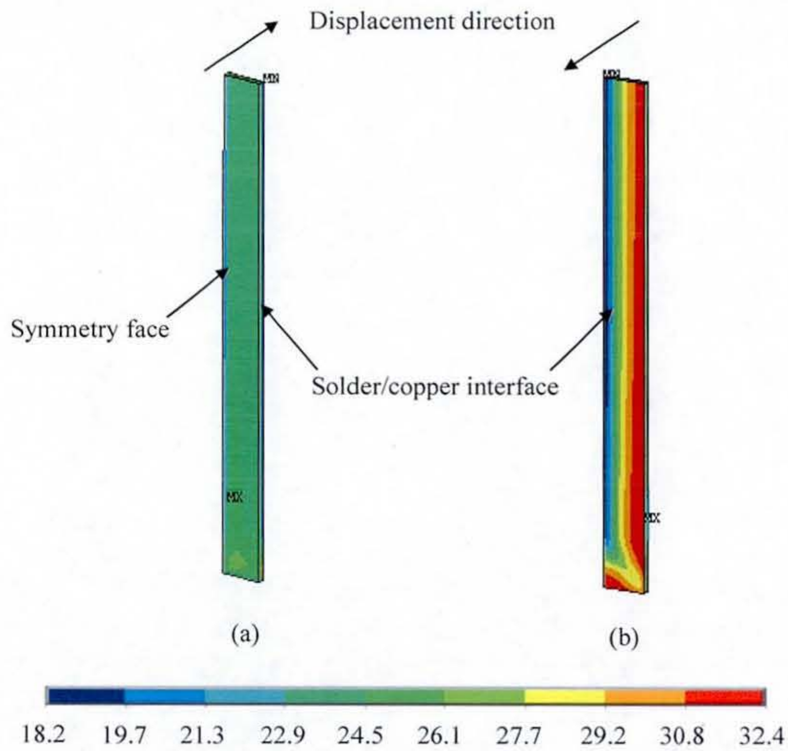


Fig. 6-29: Distribution of equivalent stresses in the solder joint with a 0.15 mm gap length: (a) on the symmetry plane; (b) at the interface

$$S = \frac{\sigma_n}{\sigma_e} \qquad 6.5$$

where σ_n is normal stress (applied load divided by the area of the solder joint) and σ_e is the equivalent stress. The size effect can be better explained by considering the variation of S with the gap to thickness ratio (g/t) as illustrated in Fig. 6-30. As the gap length decreases, the size effect becomes more prominent, resulting in an increased normal stress being required to induce the same strain in the solder joint. Thus, the apparent strength of the solder joint is artificially increased. The size effect also causes a change in the stress state in the solder joint. During plastic or creep deformation, the material tends to keep its volume constant. Since the plastic flow in the direction of the substrate is restricted, the solder joint shrinks in the lateral direction resulting in a 3D stress state. This can be better explained by considering a triaxiality ratio, R_t, that can be given as [120]:

$$R_t = \frac{\sigma_h}{\sigma_m} \qquad 6.6$$

where σ_h is the volume average of hydrostatic stress in the solder joint and, σ_m is the volume average of von Mises (equivalent) stress in the solder joint. The stress triaxiality versus gap to thickness (g/t) ratio is shown in Fig. 6-30. As the gap length (g) decreases the hydrostatic stress in the solder joint increases, due to the constraining effect in the loading direction and the Poisson's effect in the lateral direction. Therefore, even though loading is uniaxial, in the small-scale solder joints the stress field becomes triaxial due to the size effect, but as the gap length increases the triaxility decreases.

The size effect on the apparent solder material properties was confirmed experimentally by conducting further tensile tests with a solder joint gap of 1.1 mm. The specimen preparation, displacement measurement technique, and test conditions are exactly the same as those described for the solder joint gap of 0.35 mm. A comparison of the yield stress and the ultimate tensile strength are made for the two different solder joints (0.35 mm and 1.1 mm) and bulk solder. Figures 6-31 and 6-32

demonstrate this comparison for solder joints and bulk solder for three different strain rates. The variation of the yield stress and ultimate strength are nearly linear for a logarithmic strain rate scale. It is evident from these graphs that the stress-strain properties for solder joints with the 1.1 mm gap lie between the properties of the bulk solder and the solder joints with the gap of 0.35 mm. This is consistent for all three strain rates. Therefore, as the gap of the solder joint decreases, its apparent yield stress and ultimate strength increase. The comparison study also indicates that the properties of solder joints with sufficiently large gaps converge towards the properties of the bulk solder.

The contribution of the joint size to the increased tensile material properties of the solder compared with bulk solder is also studied. It is explained by considering the ultimate tensile strength of solder joints and the bulk solder at the strain rate of 0.00036 s^{-1}. Table 6-3 presents an analysis of size effect on the solder material properties. From Fig. 6-30, the percentage contribution of the size effect to the increase in the strength of the solder joint above that of bulk material can be determined for a specific gap to thickness (g/t) ratio. For example, for a given ratio of g/t, S is determined from g/t *vs.* S graph, and $((S\text{-}1)\times 100)$ gives the percentage contribution from the size of the solder joint, which is given in the fourth column of the Table 6-3. Table 6-3 shows the increase in strength cannot be explained only by the size effect. The reminder of the increase is attributed to the different microstructure of the joints, as further discussed in the following section.

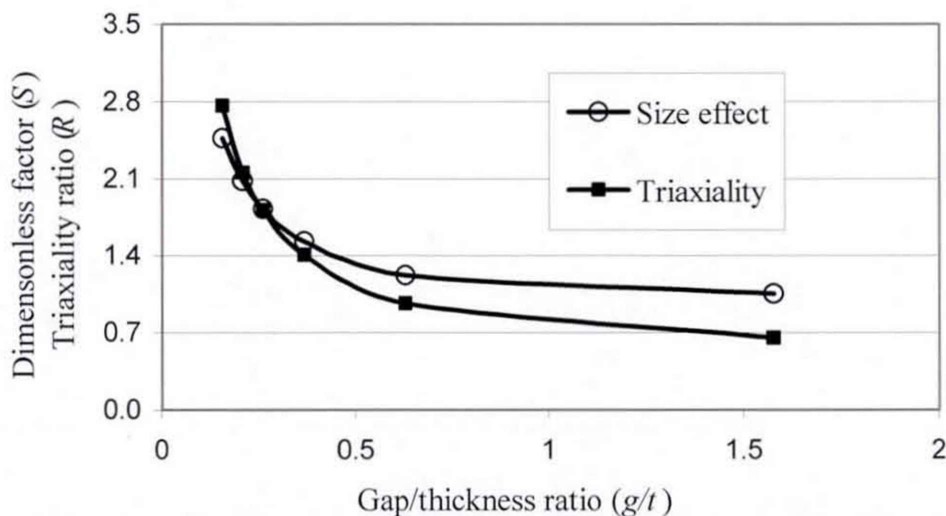


Fig. 6-30: Size effect and triaxiality ratio as functions of gap length to thickness ratio

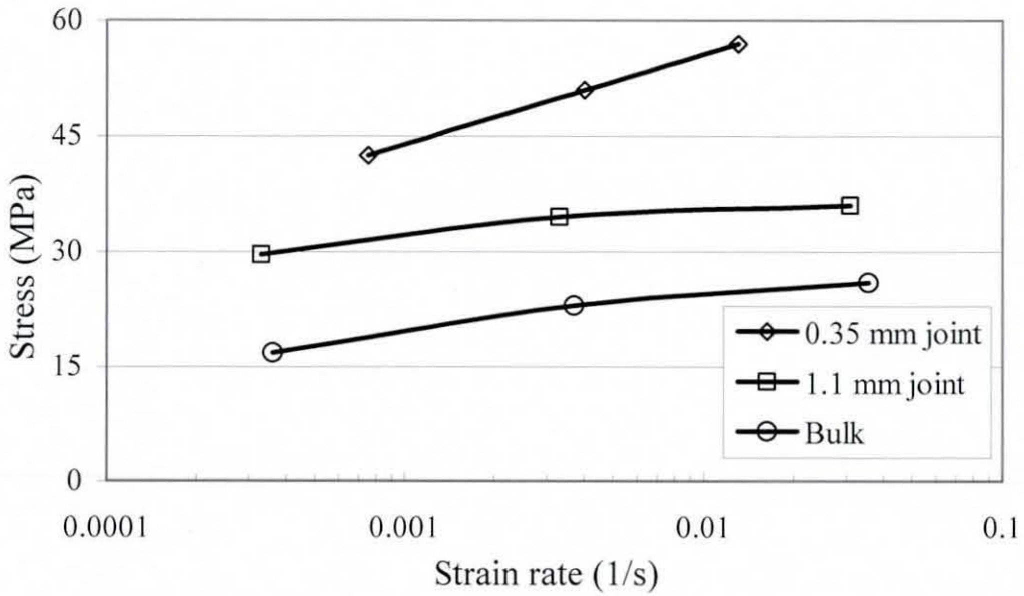


Fig. 6-31: Comparison of yield stress for solder joints (0.35 mm and 1.1 mm) and bulk solder for various strain rates

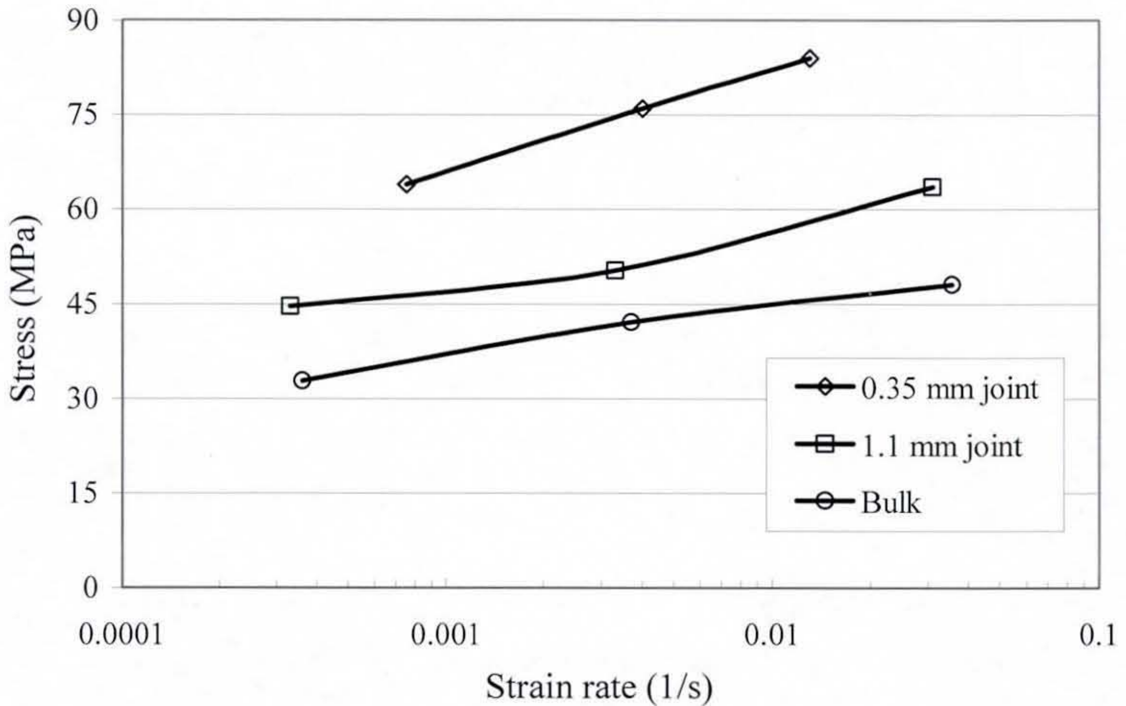


Fig. 6-32: Comparison of ultimate tensile strength for solder joints (0.35 mm and 1.1mm) and bulk solder for various strain rates

Table 6-3: Size and microstructure effect on solder material properties

Solder type	Ultimate strength (MPa)	Increase above bulk solder (%)	Size effect, $[(S\text{-}1)\times 100]$ (%)	Microstructure effect (%)
Bulk	32.8			
1.1 mm	44.6	36	15	21
0.35 mm	59.1	80	50	30

6.5.2 Microstructure Effect

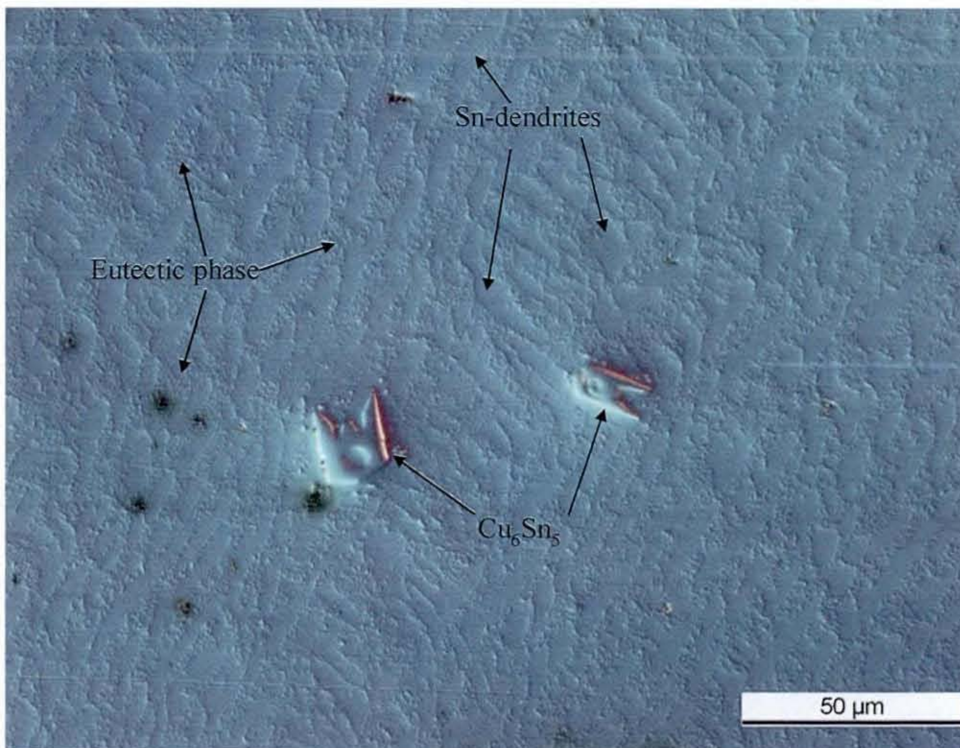
In the above section the size effect on the material properties of the solder were discussed. The microstructure of the solder joint also has an effect on its material properties. Table 6.3 also presents the effect of microstructure on the solder material properties. For example, for a solder joint with a gap of 0.35 mm, the increase in the UTS above bulk solder for the 0.00036 s^{-1} strain rate is 80 %, out of which 50 % can be explained due to the size effect. The remaining effect (30 %) therefore comes from the differences in the microstructure between the solder joint and bulk solder. This microstructure effect is separated using the results of the FE analysis, which is based on the assumption of homogeneous solder material properties, and does not include the properties of different constituents of the microstructure such as Sn-dendrites, the eutectic phase, and any intermetallic compounds (IMCs).

In order to study the microstructural differences between the bulk solder and solder joint, reflowed specimens were selected. These specimens were cut into an appropriate size and cold mounted using an epoxy resin for metallographic analysis. The reason for using cold mounting is that the low curing temperature in cold mounting avoids any changes to the solder microstructure. Once mounted, the samples were ground on a series of polishing papers with increasingly finer grits, 200, 400, 800, 1200, 2500 and 4000, which indicate the size of the abrasive particle. These ground samples were then polished using standard metallographic techniques on 0.5 μm size polishing cloth using diamond slurry. Final polishing of the samples was done on a colloidal silica pad using 0.05 μm particle size colloidal silica slurry for 2 minutes. This exposed the intermetallic compounds and grains present in the solder.

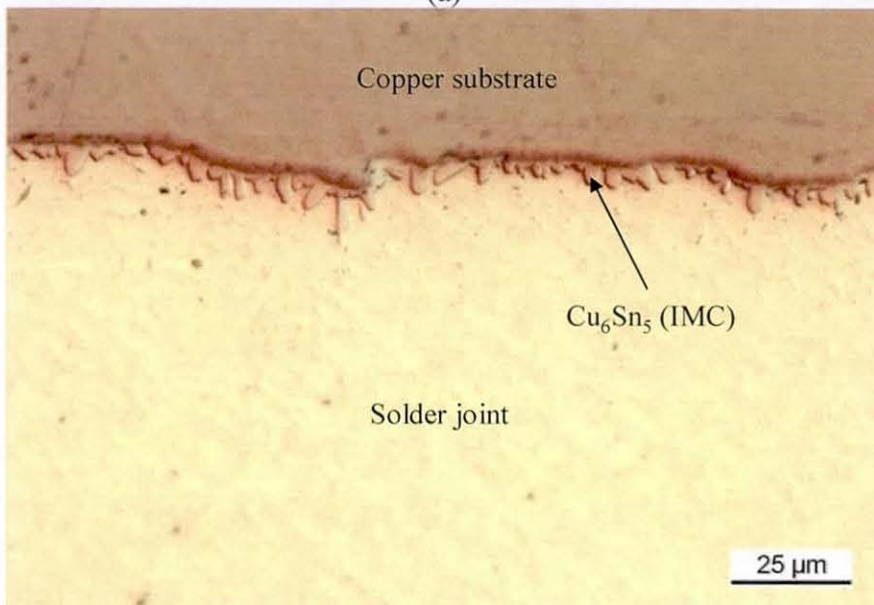
Figures 6-33 (a) and (b) present bright field images of the microstructure of an as reflowed solder joint on a copper substrate that typically consists of Sn-dendrites, the eutectic phase and intermetallic compounds. The microstructure of the reflowed bulk

solder shown in Fig. 6-34 consists predominantly of Sn-dendrites and the eutectic phase. The Sn-dendrites in the bulk solder are large compared to those in the solder joints. The overall comparison of microstructures also shows that the fraction of the eutectic phase is higher in the bulk solder. Unlike in the solder joint, Cu_6Sn_5 intermetallic compounds are hardly present within the bulk solder, due to the absence of dissolution of additional copper in the molten solder during reflow. In addition, there is no intermetallic layer in the bulk solder due to the absence of a substrate, as shown in Fig 6-33 (b). Ag_3Sn intermetallic compound is also more common in the solder joints than in bulk solder. Grains of Sn are observed both in the bulk solder and the solder joint, but they are larger in the bulk solder. Thus, the microstructure of the solder joint is comparatively finer than that of the bulk solder. Since the microstructure also depends on the cooling rate, the same cooling rate was used for both cases during solidification, however the discrepancy could be due to the diffusion of copper into the solder from the substrate which alters the composition of the solder joint. It is well known that a finer microstructure improves the material properties of solder materials [121-123]. Therefore, the differences in the microstructures between the solder joint and the bulk solder also contribute to the increased tensile material properties of the solder joints along with the joint size effect.

As discussed earlier, there is also a significant scatter, as high as 15 %, in the measured stress-strain properties of the solder joints. To understand this scatter, microstructure studies of the tested solder joints were carried out. The specimens that demonstrated the highest and lowest strength were selected from each strain rate tensile test population. All these specimens were cut using the low speed saw, cold mounted and polished as explained before. As demonstrated in this section, as well as by various other researchers, as the size of the solder joint decreases, the material properties are largely controlled by the microstructure developed during its solidification process [113, 122, 123]. The chemical composition of the solder material can also change due to diffusion processes during reflow. In addition, due to the small volume of the solder joint, defects such as voids may also play a significant role. For example local reduction in cross-sectional area of the solder joints may occur due to the formation of voids.



(a)



(b)

Fig. 6-33: Microstructure of small-scale solder joint: (a) inside solder joint; (b) at the interface between substrate and solder joint

The microstructure study of the solder joints was carried out using an optical microscope with both bright-field and polarised light. The polarised light was used to

visualise grains in the solder joints. The microstructure of the strongest solder joints showed that these consisted of very few (1-4) grains. Some of these solder joints comprised of a single grain and in such cases the solder joints behave as a single crystal material. The microstructure of the solder joints were studied over their entire area. However, microstructures are presented only for two locations, since the entire area could not be covered in a single image from the microscope. The locations selected and loading direction for the strongest solder joint (S5) are illustrated in Fig. 6-35. The bright-field image of the microstructure of this solder joint for location U1 is shown in Fig. 6-36. The microstructure typically consists of β-Sn dendrites surrounded by the eutectic phase. A few voids were also observed in the solder joint, which reduce the effective load carrying area, and also these become the locations of stress concentration. One important observation made was that the β-Sn dendrites in the microstructure are approximately oriented along the direction of loading, which helps the solder joint to withstand higher loads [110, 124]. A similar microstructure was also observed at location U2 of the solder joints, for which a typical example is illustrated in Fig. 6-37.

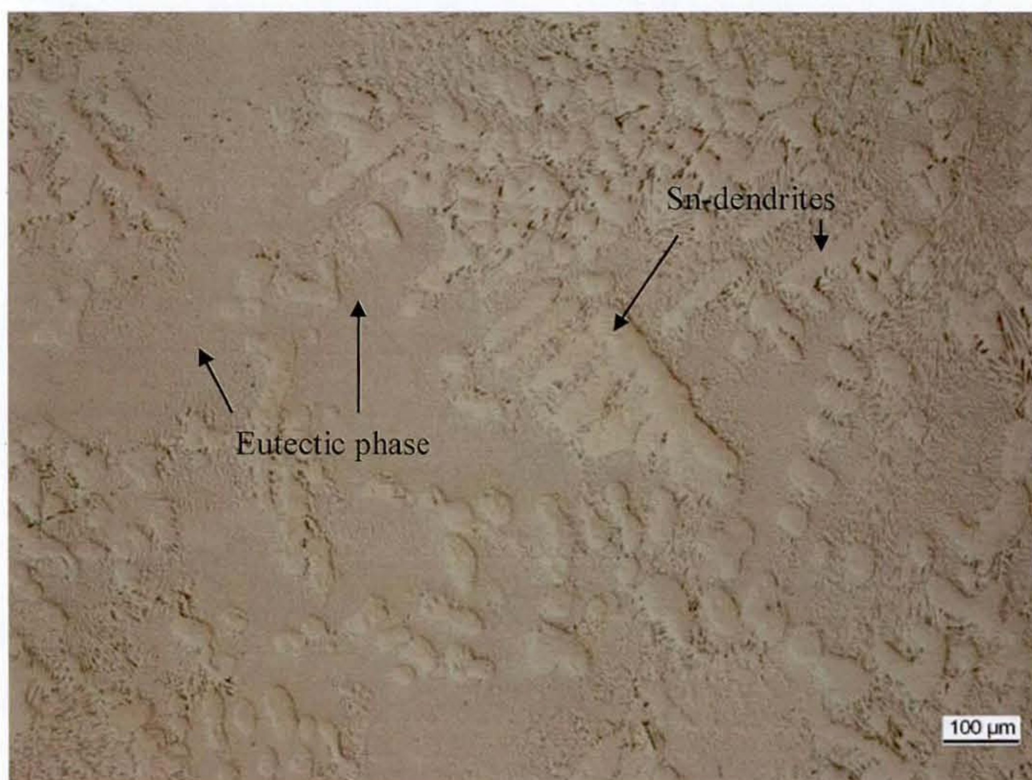


Fig. 6-34: Microstructure of reflowed bulk solder

The microstructure of the weakest solder joint for each strain rate i.e. S4, S15 and S21 exhibited a higher number of grains as compared to the strongest lot, with between 10 and 20 visible over the sample face studied. Figure 6-40 illustrates the microstructure in the vicinity of a grain boundary. Under polarised light the grains with different orientations can be distinguished and three different grains are visible in Fig. 6-38 (a). In Fig. 6-38 (b), the microstructure near the boundary between grains 1 and 2 clearly demonstrates that the orientation of Sn-dendrites in grain 2 is along the loading direction, while in grain 1 it is approximately at an angle of 45° to this direction. Similarly different orientations of Sn-dendrites are observed at the boundary between grains 2 and 3 (Fig. 6-38 (c)). Figure 6-39 shows the orientation of Sn-dendrites at grain boundaries at another location within the same solder joint; in this case the Sn-dendrites are much shorter. The presence of such grain boundaries, along with different grain orientations, results in the lower load carrying capacity of such joints.

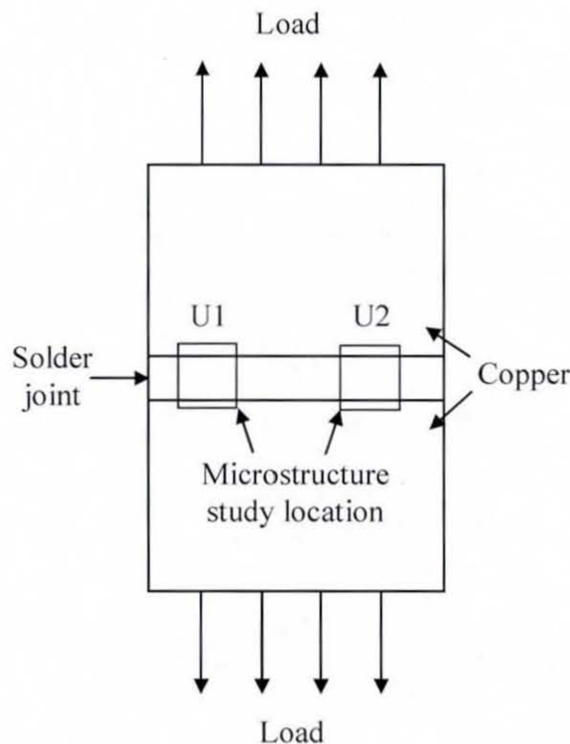


Fig. 6-35: Location used for microstructural study

Comparison of the microstructures of the strongest and weakest solder joints showed a vivid difference in microstructure. Although the main features of the microstructure are the same, the number of grains and orientation of Sn-dendrites in them are very different. It has been shown that a single grained solder joint with Sn-dendrites orientated along the direction of loading had the highest tensile strength. A higher

number of grains in the solder joint resulted in an increased effect of the grain boundaries with Sn-dendrites changing their orientations with regard to the loading direction, thereby reducing the strength of such joints. Hence, the difference in solder joint microstructure could have contributed to the wide scatter in the stress-strain data. Even though solder joint specimens are carefully fabricated and selected for testing, such a preliminary microstructure study was not possible for selecting samples for the testing procedure. Thus, the average stress-strain curve of the 7 samples per strain rate was calculated and considered as a representative material behaviour of the solder joints at that strain rate. Comparisons of microstructure between as reflowed and tested solder joints were also made. However, due to the lower levels of solder joint deformation (about 15 μm), there was no significant difference in the microstructure.

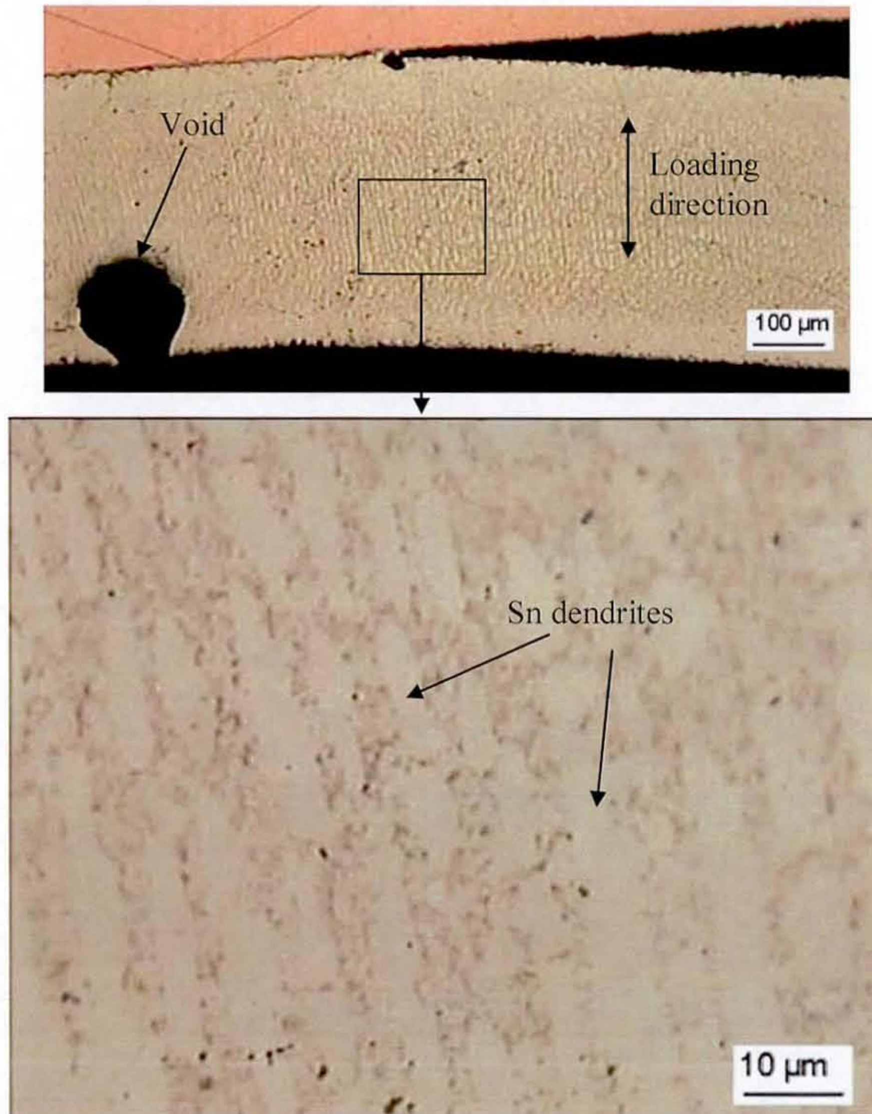


Fig. 6-36: Bright-field images of microstructure of strongest solder joint at location U1

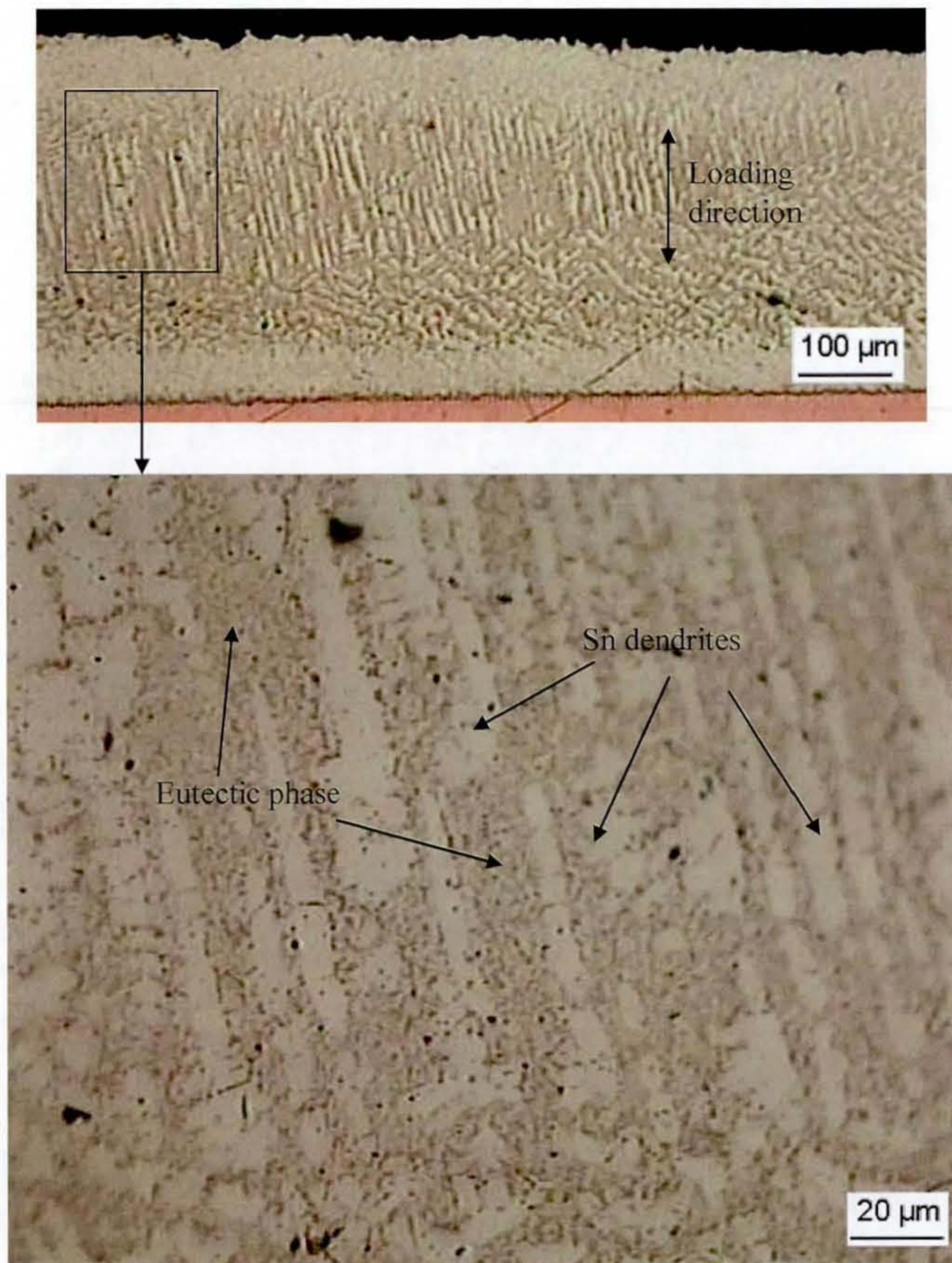


Fig. 6-37: Bright-field images of microstructure of strongest solder joint at location U2

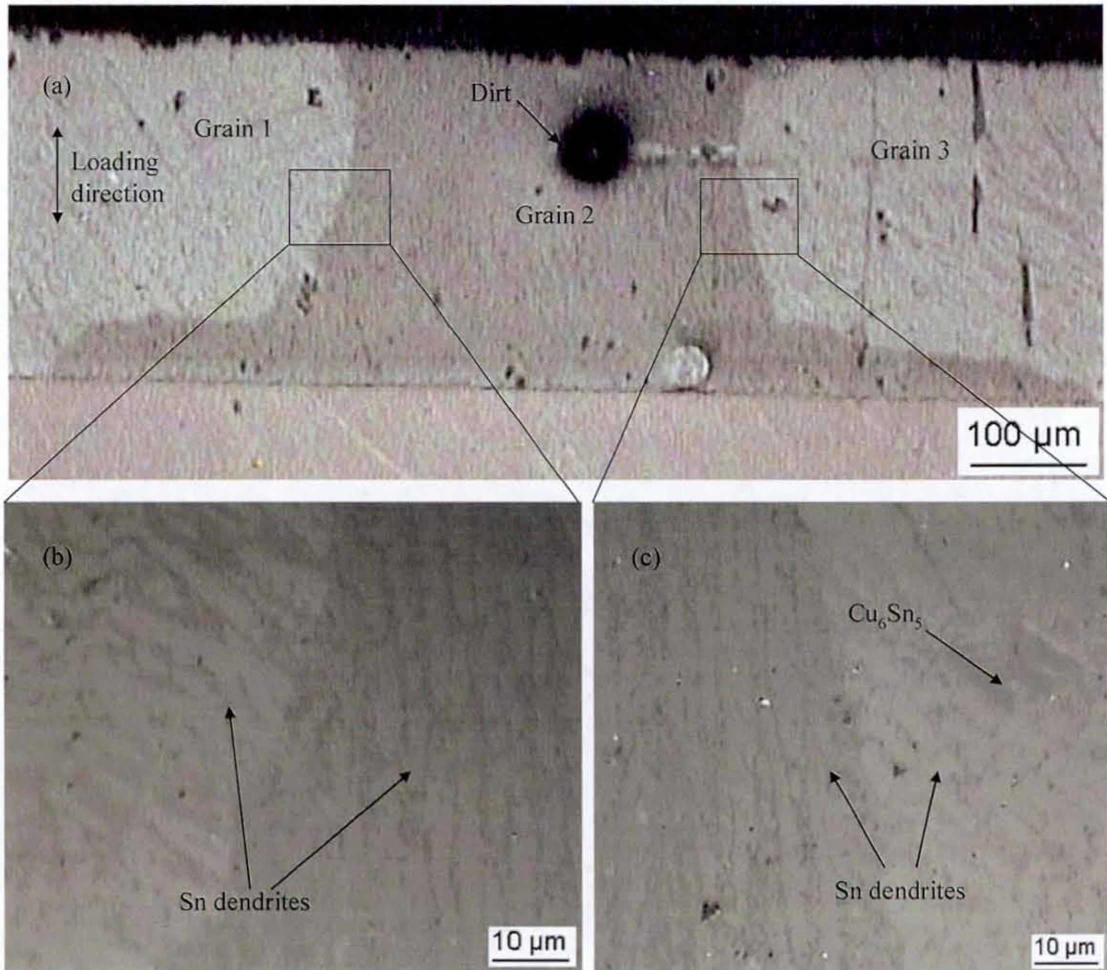


Fig. 6-38: Microstructure of weakest solder joint under polarised light: (a) general view; (b) and (c) grain boundary areas

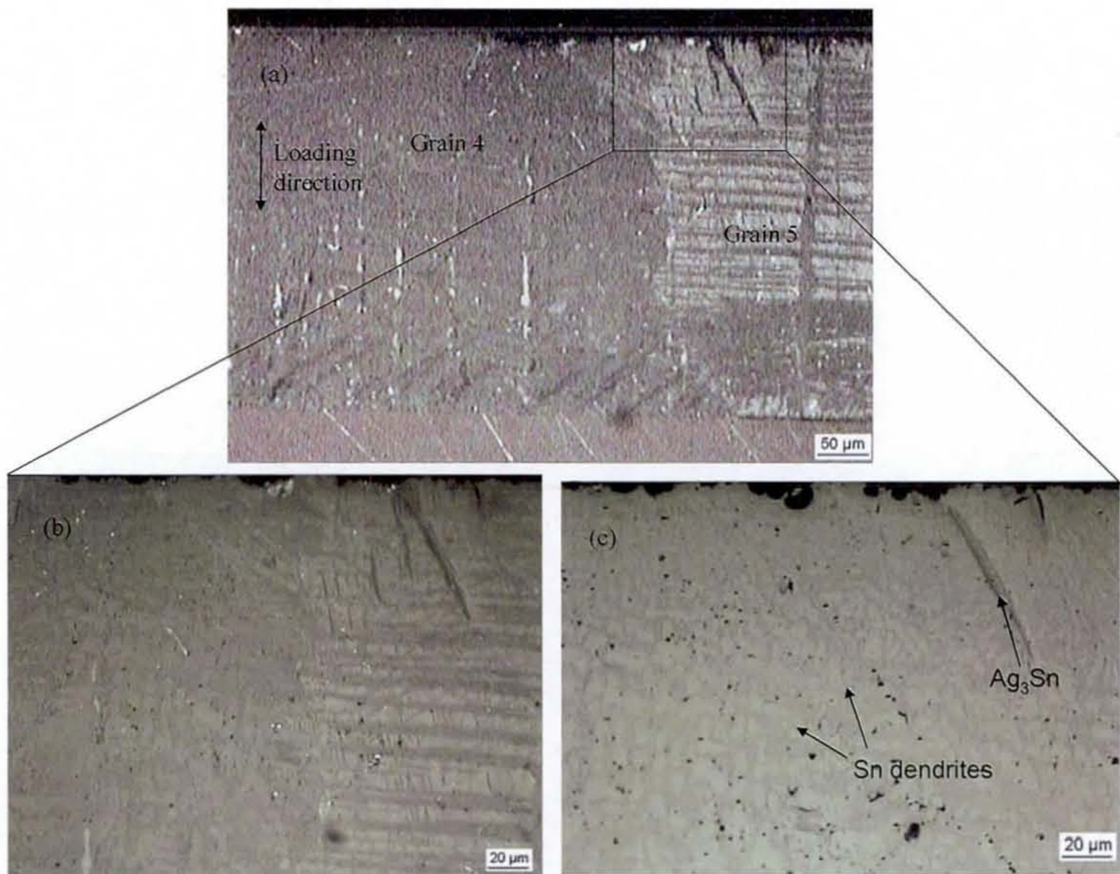


Fig. 6-39: Microstructure of weakest solder joint under polarised light: (a) general view; (b) grain boundary; (c) microstructural features

A microstructure of the tested solder joints was also compared with that of solder joints in the chip resistor assembly fabricated with the same reflow conditions. Figure 6-40 shows the microstructure of one of the solder joints in the sectioned chip resistor assembly. The microstructure is similar to that observed for the tested solder joints, with it consisting of Sn-dendrites, eutectic phase and Cu_6Sn_5 intermetallic compound. As shown in Fig. 6-40 (c), Sn-grains are also observed in the chip resistor solder joint. Thus, due to the similarity in microstructure between the tested solder joints and the solder joints in the chip resistor assembly, the use of experimentally determined solder joint material properties in the future FE simulation of surface mount assembly is justified.

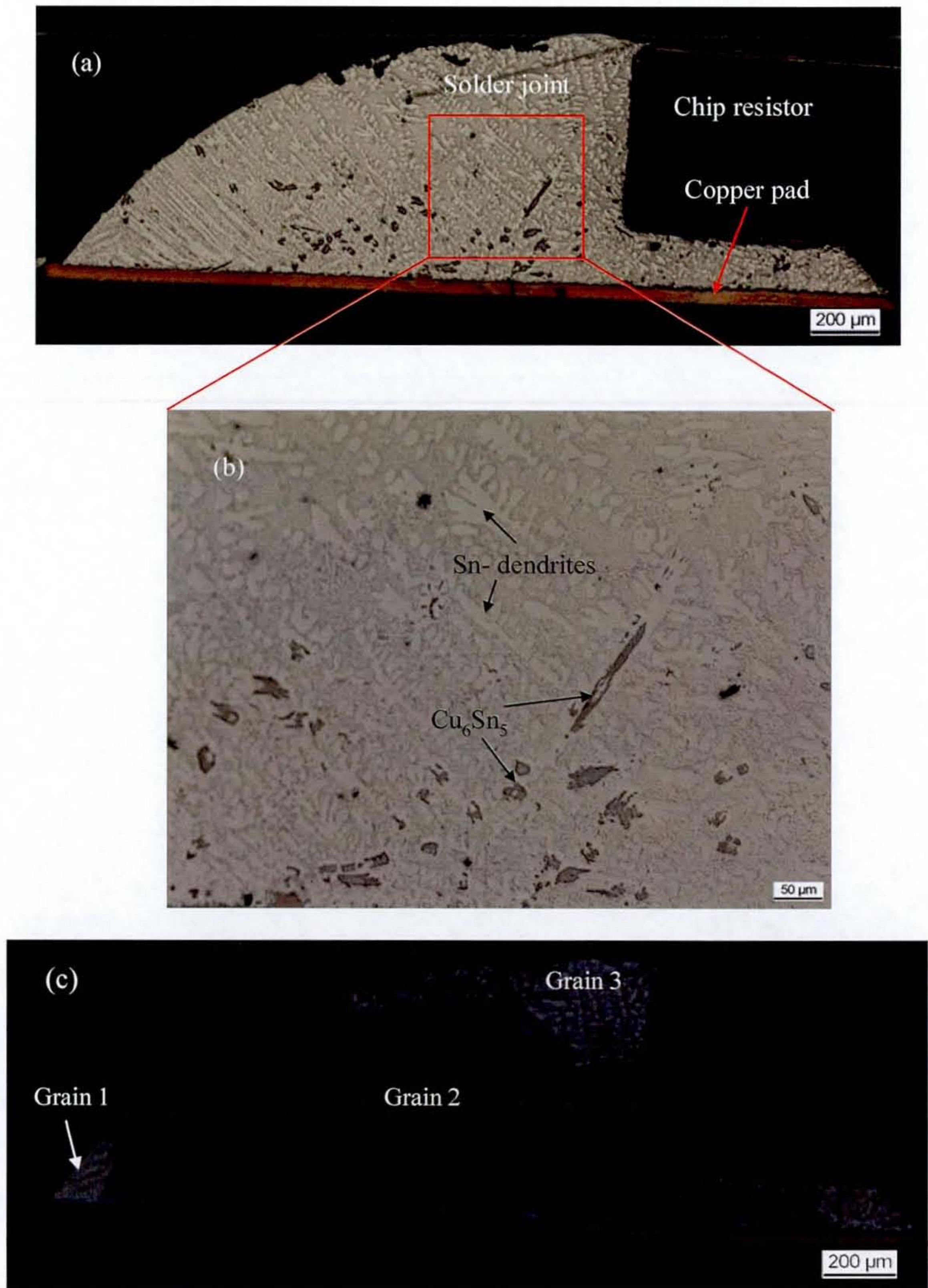


Fig. 6-40: Microstructure of a solder joint in a chip resistor assembly: (a) general view; (b) zoomed view; (c) grain structure

6.6 Summary

In this chapter the tensile material properties of Sn3.8Ag0.7Cu solder alloy were discussed. Those properties were determined experimentally for both a small-scale solder joint (gaps of 0.35 mm and 1.1 mm) and the reflowed bulk solder. The tensile experiments were carried out for three different strain rates. The obtained stress-strain data for the solder joints showed a wide range of scatter, as high as 15% about the averaged data, while the data in the bulk solder showed only a 5 % scatter. Greater strain hardening was observed at the higher strain rates in both cases. This result is in line with observations made by other researchers for lead-free solders with different compositions [125-127]. However, comparison of the stress-strain data for the solder joint and the bulk solder showed significantly increased apparent tensile properties for the former. The study of the reasons for this increase in comparison with the bulk solder revealed the contribution of size and microstructure effect on the solder material properties. As the size of solder joint decreases the plastic deformation taking place in the solder joint is constrained by the stiffer copper substrates, which are in the elastic state. This constraining effect of the copper results in a 3D stress state in the solder joint even though the specimen was loaded uniaxially. The extent of the size effect on the material properties of the solder joint was determined with the help of finite-element analysis for the specific range of the gap to thickness ratio (g/t) that covers the experimental case. Microstructure studies of both the solder joints and the reflowed bulk solder illustrated that the solder joint has a finer microstructure than the bulk solder. It has been well established that a finer microstructure improves the material properties; a similar effect was observed by comparing material properties of the bulk solder and the solder joint. With the help of the finite-element analysis the effects of the size and microstructure were separated, and the size effect can be quantified for the given solder joint gap. Further, the microstructure effect includes the effect of Sn-dendrites, the eutectic phase, the volume faction of IMCs, and the intermetallic layer. The intermetallic layer and IMCs in the solder joint contribute most to the microstructure effects. Finally, a conclusion can be made from the tensile experiments that the strength of the solder joint is the result of a superposition of material properties of the bulk solder, the size of the solder joint and the effect of microstructure.

7. Creep Properties of Sn3.8Ag0.7Cu Solder

As discussed in chapter 4, damage due to time-dependent deformation or creep is one of the major reliability concerns for solder joints operating with cyclic variation of temperature. Even room temperature (294 K) is high with regard to the melting point and should be treated as an elevated temperature for solder alloys. As discussed in chapter 6, the stress-strain properties of solder joints are predominantly size- and microstructure-dependent. Therefore, in this chapter the determination of creep properties for solder joints under conditions that correspond to their actual application under both tensile and shear loading is discussed. The chapter also presents the calculation of creep parameters for a model fitted to the experimentally obtained creep properties and comparison of the solder joint creep data with the data for bulk solder.

7.1 Introduction

Due to the high homologous operating temperature, most of the solder joint deformation in service environments occurs by creep as discussed in section 4.2.2. Accurate material data is crucial to allow modelling of the creep behaviour of solder joints using the finite element method. Commonly in modelling of solder (joint) creep behaviour, only the steady-state strain rate is considered since it contributes a major proportion of the creep strain as was discussed in section 2.3.2. However, published material properties data is sparse for lead-free solders, such as the commonly used SnAgCu alloys, due to their recent introduction into electronic applications.

The creep properties for lead-free SnAgCu solders can be determined easily for the bulk solder, but as demonstrated in the previous chapter, the tensile material properties of an actual solder joint are strongly dependent on its size and microstructure. Therefore, the use of creep data for bulk solder in the modelling of the creep behaviour of solder joints may result in an inaccurate representation of the real field behaviour. Generally solder joints are subjected to shear loads due to the relative displacement between a component and PCB during cyclic temperature changes. Pang *et al.* [128] carried out creep tests for Sn3.8Ag0.7Cu solder for a wide range of temperatures and stress levels, however these tests were conducted on bulk solder and at stress levels above 5 MPa under tensile loading. They also showed that the von Mises stress transformation applies quite well for tensile and shear loads. However, the

applicability of the von Mises criteria to SnAgCu solders is not fully established. Dusek *et al.* [129] and Zhang *et al.* [47] determined the steady-state shear strain rate for a lap solder joint of Sn3.8Ag0.7Cu and Sn3.9Ag0.6Cu solder, respectively. Dusek *et al.* used a reflow and water-quenching process to fabricate their specimens, whilst the processing conditions were not mentioned for Zhang *et al.* Even though the compositions of the solder alloys were nearly the same, the curves of steady-state shear strain rate against shear stress had an order of magnitude difference between Dusek *et al* and Zhang *et al.* A creep test for a lap solder joint was also carried out by Morris *et al.* [130], which displayed a similar trend to that observed by Dusek *et al.*, but with a higher steady-state strain rate. Thus, the previous creep studies showed that the creep behaviour for common SnAgCu solder alloys can vary significantly even though their compositions are similar. In addition, due to the dependency of creep properties of the solder joint on its microstructure, the processing conditions play an important role. However, these processing conditions are not always clearly described by the researchers. Therefore, in this chapter, experiments carried out to determine the steady-state creep behaviour of solder joints with a structure relevant to real-life applications are discussed. The specimen fabrication processes, such as the reflow profile and cooling process, are similar to those used for actual surface mount applications. These creep experiments were carried out for both tensile and shear loading conditions. The steady-state strain rates for both types of load are compared with those obtained for the bulk solder. After this comparison of the steady state-strain rates, creep data based on the lowest and highest creep resistance demonstrated in the experiments are used for creep modelling using FEA.

7.2 Tensile Creep Test of Small-Scale Solder Joints

The dimensions and fabrication procedure for the solder joints used in the creep tests were exactly the same as in the study of stress-strain properties described in 6.4.1. The same Instron experimental setup was also used together with the high precision Instron 2630-100 series extensometer for the displacement measurement.

7.2.1 Creep Test Procedure

Creep is a time-dependent deformation phenomenon. Thus, the creep strain is measured as a function of time for an applied constant load at constant temperature. Creep tests are usually long-term experiments to include all three stages of creep -

primary, steady state (secondary) and tertiary creep, as outlined in Fig. 2-9. The effect of primary creep on reliability is not fully understood, and secondary creep behaviour is most widely used in reliability studies, since secondary creep is usually the longest stage in the creep domain. The presence and prominence of all three stages in the creep curve depends on the stress level at which the creep test is being conducted. Generally, stress levels of 20 %, 40 %, 60 % and 80 % of the yield stress are considered appropriate [20]. However, in creep tests at a normal stress of 15 MPa (36 % of yield stress), the deformation of the solder joint was so small that it couldn't be recorded using the extensometer during measurements made over 8 hrs and with a resolution of 0.2 μm. Therefore, the creep tests for tensile loading were carried out at normal stress levels of 20 MPa, 25 MPa, 30 MPa, 35 MPa and 40 MPa, which resulted in equivalent stress levels of 13.3 MPa, 16.7 MPa, 20 MPa, 23.3 MPa and 26.7 MPa respectively in the solder joint. These equivalent stresses were calculated considering the size effect discussed in Section 6.5.1 and presented by Eq. 6.5. The resulting equivalent stresses represent 31, 39, 47, 55 and 63 percent of the yield stress of the solder joint, which, as shown in 6.4.3, is 42.5 MPa. All creep tests were carried out at room temperature, and a temperature of 295 K ± 2 was maintained throughout the experiments to avoid any effect of temperature.

Before a creep test was carried out for the solder joint specimens, a copper strip as shown Fig. 6-2 was tested in creep at a stress of 40 MPa to determine if there was any creep deformation in the copper. However, no creep was found, indicating that the copper would be deformed only elastically during the creep test of the actual solder joint specimens and any creep deformation would therefore only be due to the solder joint. Thus, the actual solder joint's deformation was obtained by subtracting the linear elastic deformation of the copper (δ_c) from the extensometer displacement (δ_{ext}) as explained in Section 6.2.2. From this measured deformation of the solder joint with time, strain rate in the solder was calculated. In the creep test, as for the tensile stress-strain test, a sample size of 7 specimens was used. In each creep test, the specimen was ramped to the specified stress at a displacement rate of 0.005 mm/s and that stress was then maintained throughout the test.

7.2.2 Results and Discussion

Although, tensile creep tests were carried out for equivalent stress levels of 13.3 MPa, 16.7 MPa, 20 MPa, 23.3 MPa and 26.7 MPa, creep curves are presented only for 16.7 MPa and 26.7 MPa due to the similarity of the obtained results. Figure 7-1 illustrates the creep curves for an equivalent stress of 16.7 MPa. The creep test at this stress was continued for at least 5 hrs or until failure of the solder joint. It is evident from the figure that the primary creep duration for all curves is short compared to that for the secondary creep. All of the creep curves, except SC13, exhibited prolonged secondary creep beyond 5 hrs, while SC13 failed within 5 hrs. Significant scatter of the creep curves is also observed in the creep test, as was the case for stress-strain curves (see chapter 6). The scatter of the creep curves is an order of magnitude in terms of the steady-state creep rate. The creep curves for an equivalent stress of 26.7 MPa are shown in Fig. 7-2. In this case the creep tests were all continued until failure of the specimen. It is evident that although the same fabrication process was adopted for all the specimens, their creep responses are significantly different. The dispersion in creep behaviour is seen both for the failure time and the secondary creep rate. Similar variation of the creep curves was observed for the other equivalent stress levels – 13.3 MPa, 20 MPa and 23.3 MPa. Comparison of the creep data at different stresses demonstrates that, as the stress increases, the creep resistance of the solder joint decreases.

To understand the reasons for the scatter in the creep curves, despite the same experimental and fabrication conditions, a microstructure study of the tested solder joints was carried out. The strongest and weakest specimen for every stress level was selected. The microstructure of these solder joints was studied in detail and the number of grains, orientation of the Sn dendrites, and the size and distribution of voids in the solder joints were identified. As discussed in section 6.5.2, the variations in microstructure between the specimens could contribute to the scatter of the data. The microstructure study was carried out using both bright-field and polarised light. Figure 7.3 illustrates the microstructure of the weakest specimen (SC13). The weaker specimens had a higher number of either voids, which reduced the effective load carrying volume, or Sn-grains with unfavourable orientation. Sometimes these specimens contain Sn dendrites orientated at an angle to the load direction, which

could reduce the load carrying capacity of the solder joint (section 6.5.2). With such a microstructure, the solder joint exhibits higher deformation under a given stress, resulting in a higher steady-state creep strain rate. The number of Sn-grains in weaker specimens varied from 10 to 18 along their width compared with 1 to 4 for the stronger specimens. The microstructure in the vicinity of a grain boundary is shown Fig. 7-4. Here Sn dendrites in grain 1 are oriented in the direction of loading, while those in grain 2 are oriented at approximately 45° to this direction.

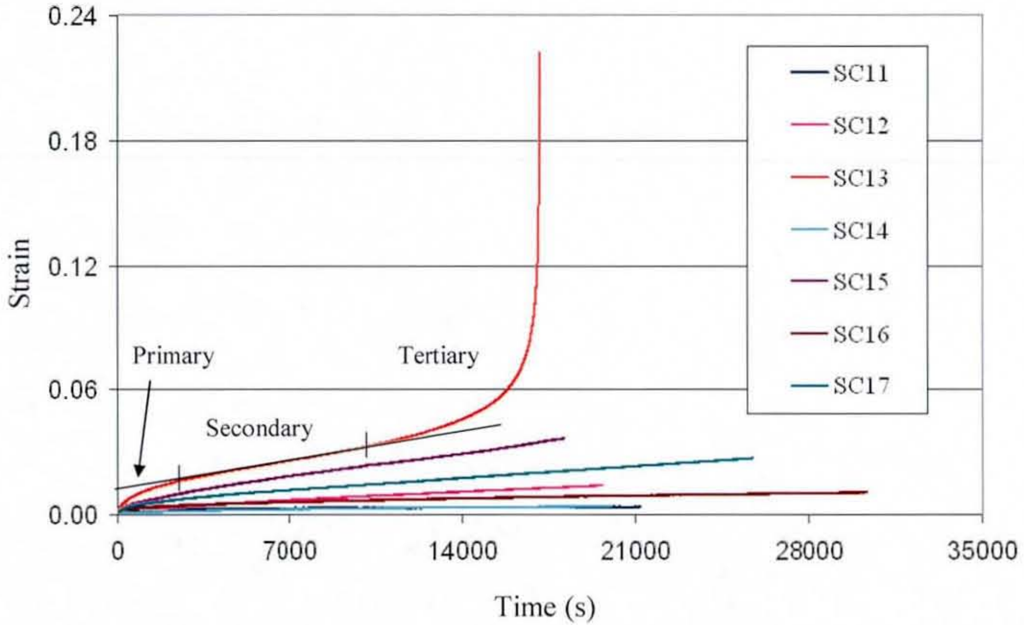


Fig. 7-1: Tensile creep curves at 16.7 MPa

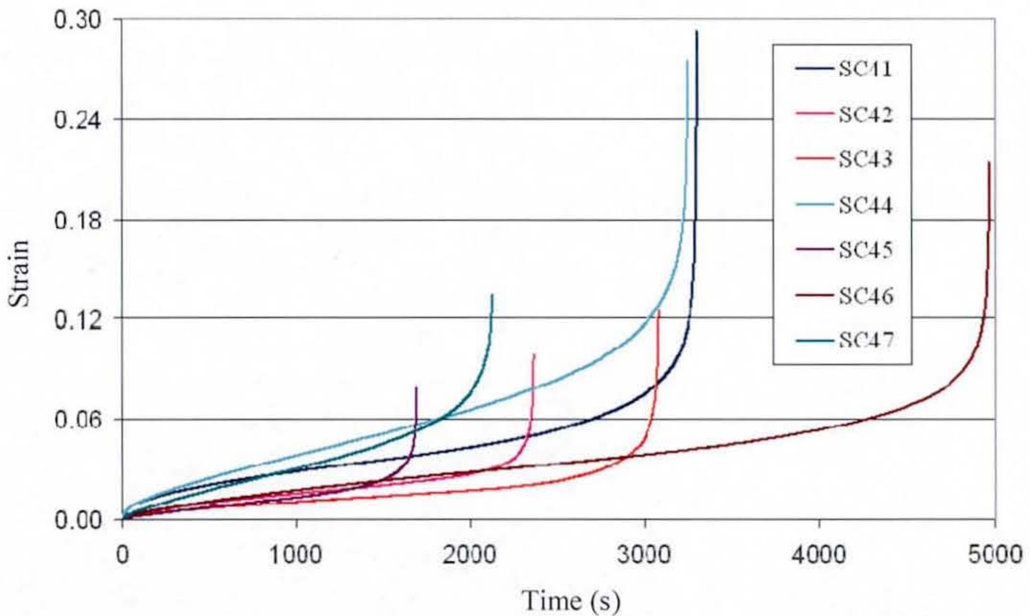


Fig. 7-2: Tensile creep curves at 26.7 MPa

A few voids were also observed in the specimens and examples of them are shown in Fig. 7-3. The presence of these voids reduces the effective volume of the solder joint and causes stress concentrations. Thus, the strength of the solder joint is reduced. For some of the weaker specimens most parts of solder joint microstructure contained Sn

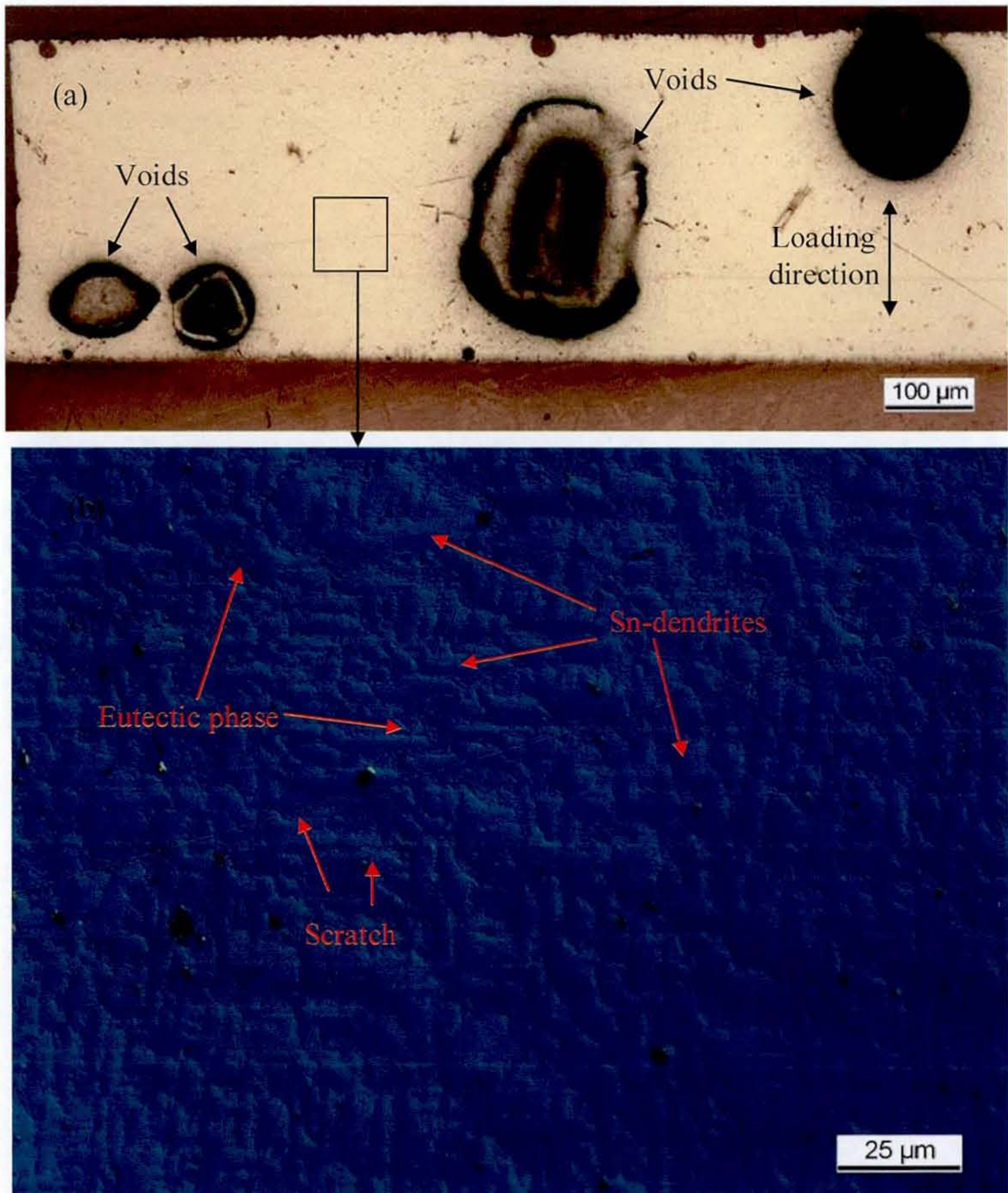


Fig. 7-3: Microstructure of weakest solder joint specimen SC13 in 16.7 MPa test: (a) voids in the solder joint; (b) detailed view of selected location

dendrites oriented perpendicular to the direction of load application. The stronger solder joints had fewer Sn-grains. Figure 7-5 presents the microstructure of one such solder joint where only 2 Sn-grains were observed for the entire width of the solder joint. The Sn dendrites in the vicinity of the grain boundary are almost in the same direction, but the dendrites in grain 1 are longer than those in grain 2. However, the Sn dendrites at both sides of the grain boundary are oriented approximately in the direction of loading, and fewer grain boundaries were present at which grain boundary deformation could take place. These results show that the microstructure of the solder joints plays a very important role in determining creep performance.

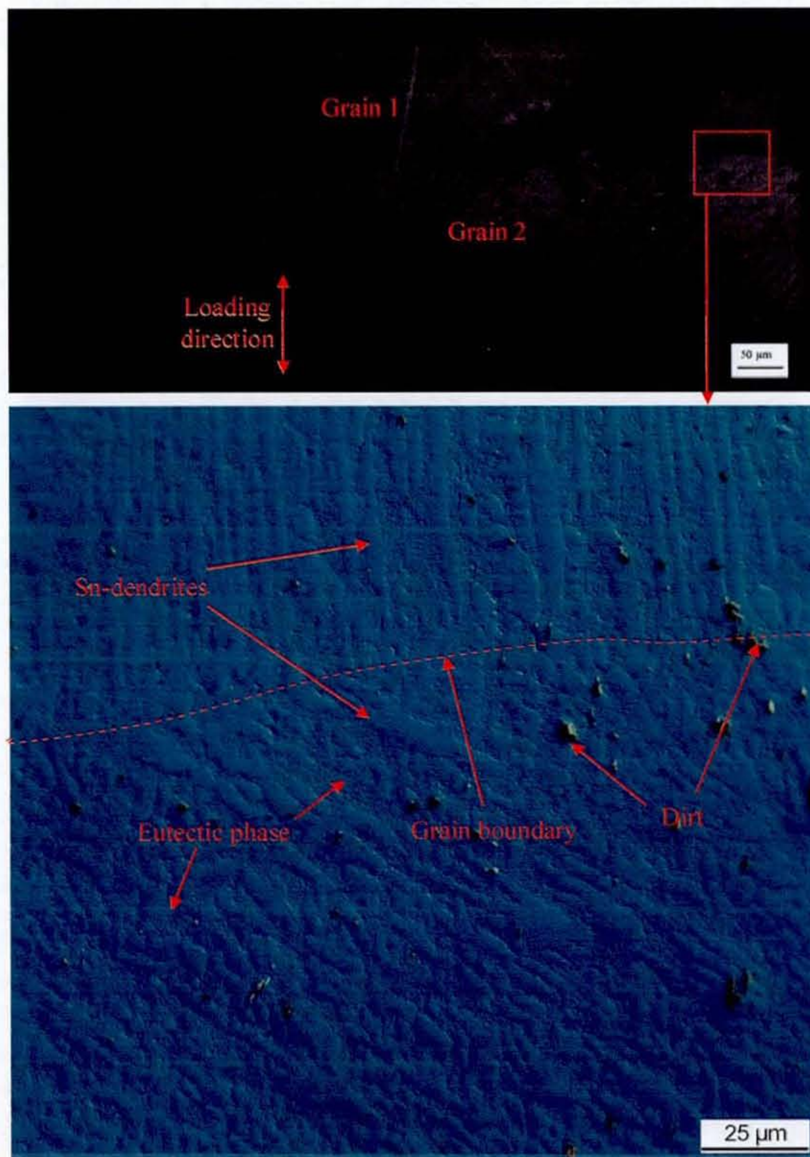


Fig. 7-4: Microstructure of weakest solder joint specimen SC44 in 26.7 MPa test: (a) grains; (b) microstructure at the grain boundary

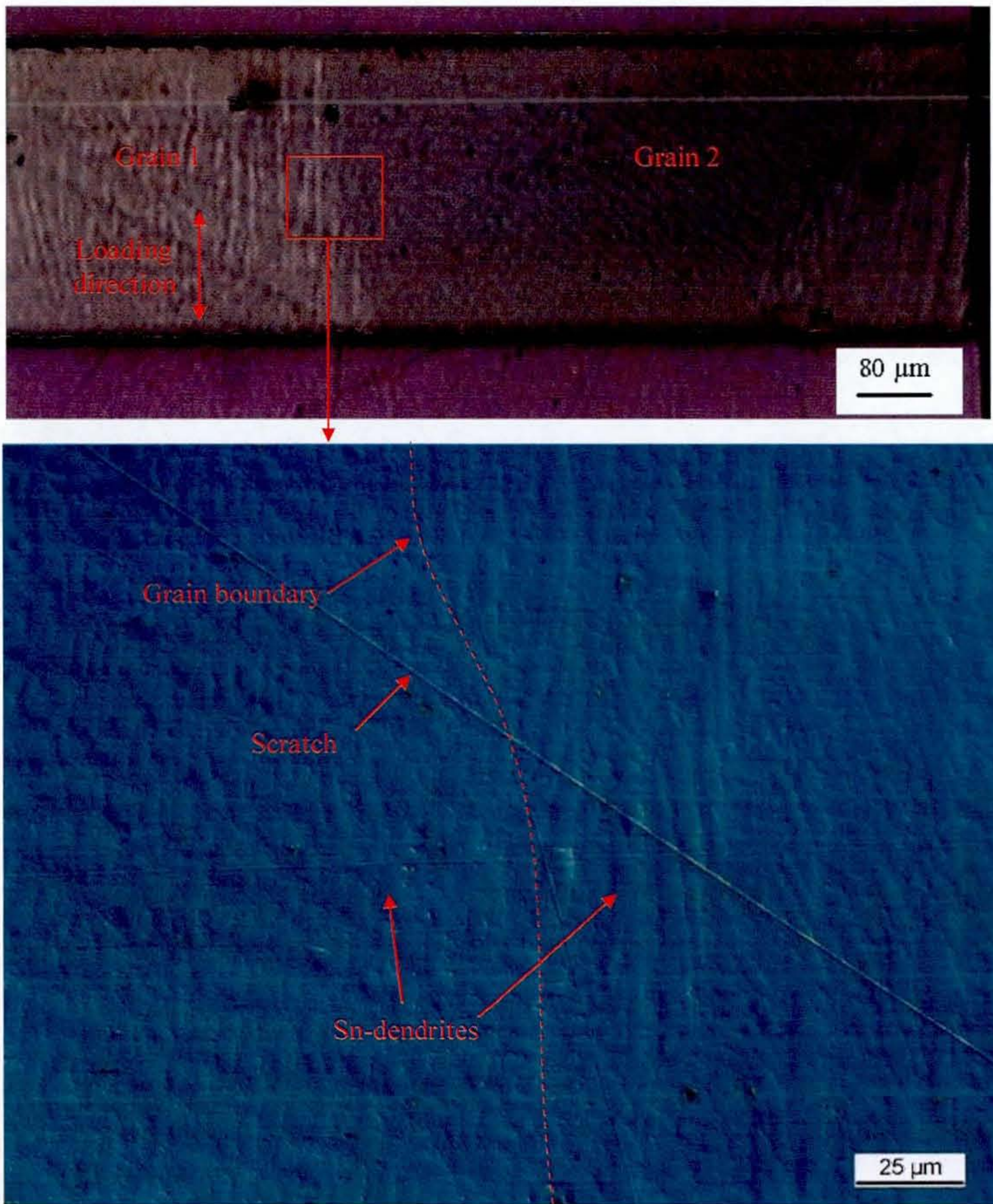


Fig. 7-5: Microstructure of strongest solder joint specimen SC43 in 26.7 MPa test: (a) grains; (b) microstructure at the grain boundary

Unlike for the stress-strain results, the creep curves for specific stresses have not been averaged. In contrast, creep curves for the strongest and weakest solder joint at each stress level were identified and the steady-state strain rates of these curves were studied against the tested stress levels. Adopting this method would cover the entire range of the creep data scatter. Figure 7-6 illustrates the calculation of the steady-state creep rate for the secondary stage of the creep curve. The slope of its linear part, which

lies between the primary and tertiary stages, is considered to be the steady-state strain rate. This slope was calculated for each creep curve.

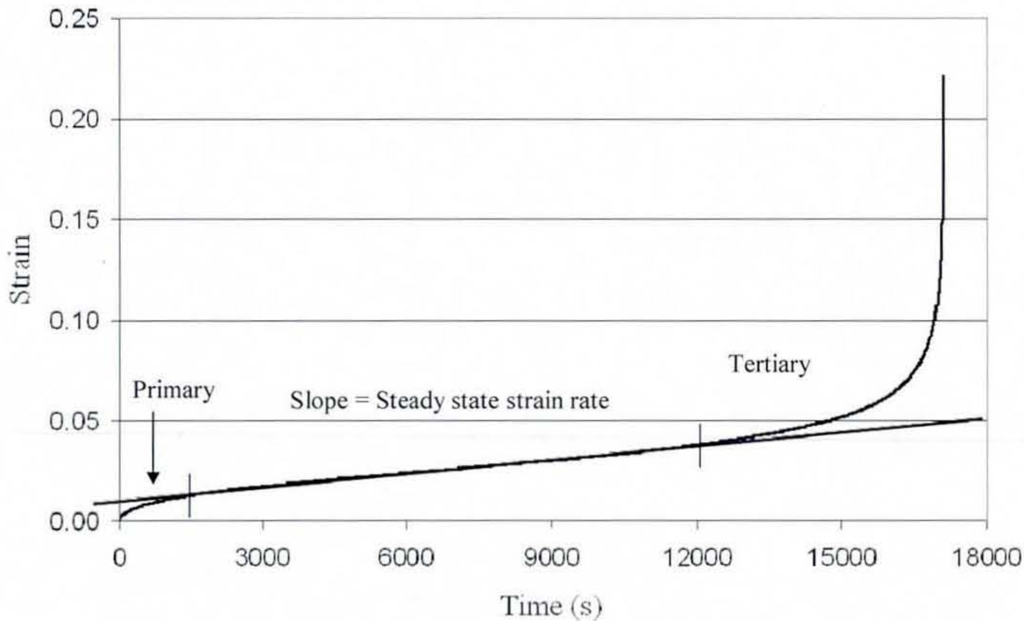


Fig. 7-6: Calculation of the steady-state strain rate during secondary creep

Since secondary creep is very important for the modelling of creep behaviour, a constitutive equation for the variation of steady state strain rate with the applied stress was fitted to the experimental data. For solder alloys, the hyperbolic sine constitutive law is most commonly used in creep modelling and its suitability was discussed in section 2.3.2 and is given by equation 2.35. This equation has been implemented in most commercial finite-element software. Therefore, the parameters required for reproducing the experimental data were calculated based on the experimental data by assuming a value for the activation energy, Q. A comparative study carried out by Clech on creep data for solder joints [44] showed that the activation energy for SnAgCu solders is between 63 kJ/mol and 99 kJ/mol. He also obtained an average value of Q as 72.93 kJ/mol for merged NPL (Sn3.8Ag0.7Cu), NTU (Sn3.8Ag0.7Cu) and UM (Sn3.9Ag0.6Cu) creep data. Since, in this research, the creep experiments were carried out only at room temperature, this value of activation energy was used whilst obtaining the remaining hyperbolic sine parameters, B_1, β and p, using non-linear curve fitting to best reproduce the experimental results. This was done in Microsoft Excel using an iterative procedure. Table 7-1 presents the calculated values of these parameters for the steady-state strain rate curves for both the weakest and

strongest joints. A comparison of the experimental steady-state strain rates with the strain rates reproduced using the fitted hyperbolic sine equation were made, and is presented in Fig. 7-7 for both weakest and strongest joints. The reproduced data for both types of joints match very well with the experimental data, except for the case of the weakest joint tested at 16.7 MPa. The higher number of Sn-grains than the other weakest joints could have resulted in higher experimental strain rate, which in turn lead to deviation from the reproduced data. However, this discrepancy did not significantly compromise the quality of predictions for the other stress levels. A sensitivity study was also carried out by varying the values of Q between 63 kJ/mol and 99 kJ/mol, and B_1 value was varied respectively, to reproduce the similar curve fit. Therefore, by using this equation, the steady-state strain rate can be calculated for different stresses, for which experimental creep data are not available.

Table 7-1: Parameters for hyperbolic sine constitutive equation for creep

Steady state strain rate	$B_1 \times 10^4$ (1/sec)	β (1/MPa)	p	Q (kJ/mol)
Weakest	3.28	0.092	5.3	72930
Strongest	1.64	0.089	4.9	72930

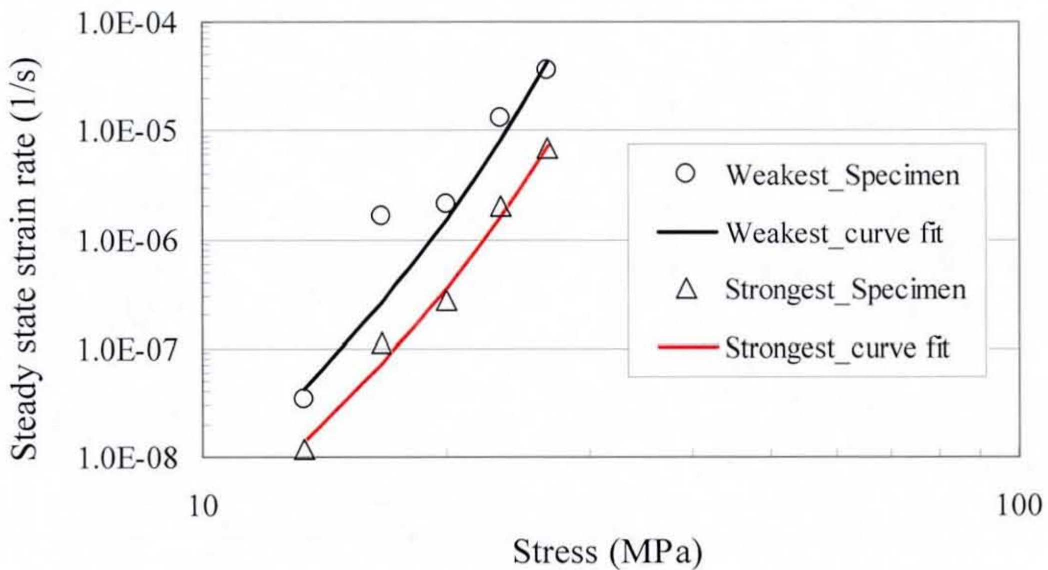


Fig. 7-7: Comparison of experimental data and fitted hyperbolic sine law for steady-state strain rate for the strongest and weakest joints tested

7.3 Shear Creep Testing of Small-Scale Solder Joints

This section discusses the experimental work carried out for obtaining the creep properties of small-scale solder joints under shear load.

7.3.1 Specimen Preparation

To determine the creep properties of Sn3.8Ag0.7Cu solder joints under a shearing load, a single lap joint was fabricated between two copper substrates. The fabrication method was adopted from that used by Duesk *et al* [14] but with a modification to the method of cutting the copper substrate. For fabrication, 99.99 % pure 1 mm thick copper sheet, as used for the tensile creep tests, was cut into 10.5 mm × 60 mm specimens. A slot was cut in the middle of each copper specimen using the same low speed saw, as used for the fabrication of tensile test specimen; which was shown in Fig. 6-14. A slot approximately 0.35 mm wide and approximately 40 mm long was obtained. One side of the slot was covered with high temperature tape to prevent the flow of solder paste out of the slot. Then a quantity of Sn3.8Ag0.7Cu solder paste approximately 3-4 times the volume of the slot was put in the copper specimen slot to ensure that the slot was full of solder after reflow. Finally the copper specimen with solder paste in the slot was placed in the T-TRACK reflow oven as shown in Fig. 6-6. The reflow profile used to fabricate the solder joint was the same as that used for the fabrication of the tensile test specimens, as illustrated in Fig. 6-15, i.e. with a maximum reflow temperature of 523 K and a cooling rate of 1.5 K/s. This cooling rate is similar to that usually used in surface mount applications. Then, the specimens were ground flat by hand followed by a final polish on 800 grit paper. The ground specimen is shown in Fig. 7-8 (a).

The specimens were finally cut from both sides, as shown in Fig. 7-8 (b), at a spacing of 7 mm using the same low speed saw. These two cuts separate the copper plate into two parts, joined only by a lap solder joint. By adopting this method, lap solder joints were fabricated avoiding joining of two separate copper pieces. This method is therefore advantageous in maintaining the parallelism between the two copper pieces, which would have been difficult if joining two separate copper pieces. The final dimensions of the specimen are 60 mm (length) ×10.5 mm (width) × 0.95 mm

(thickness) with solder joint dimensions of 7 mm (length) × 0.35 mm (gap) × 0.95 mm (thickness).

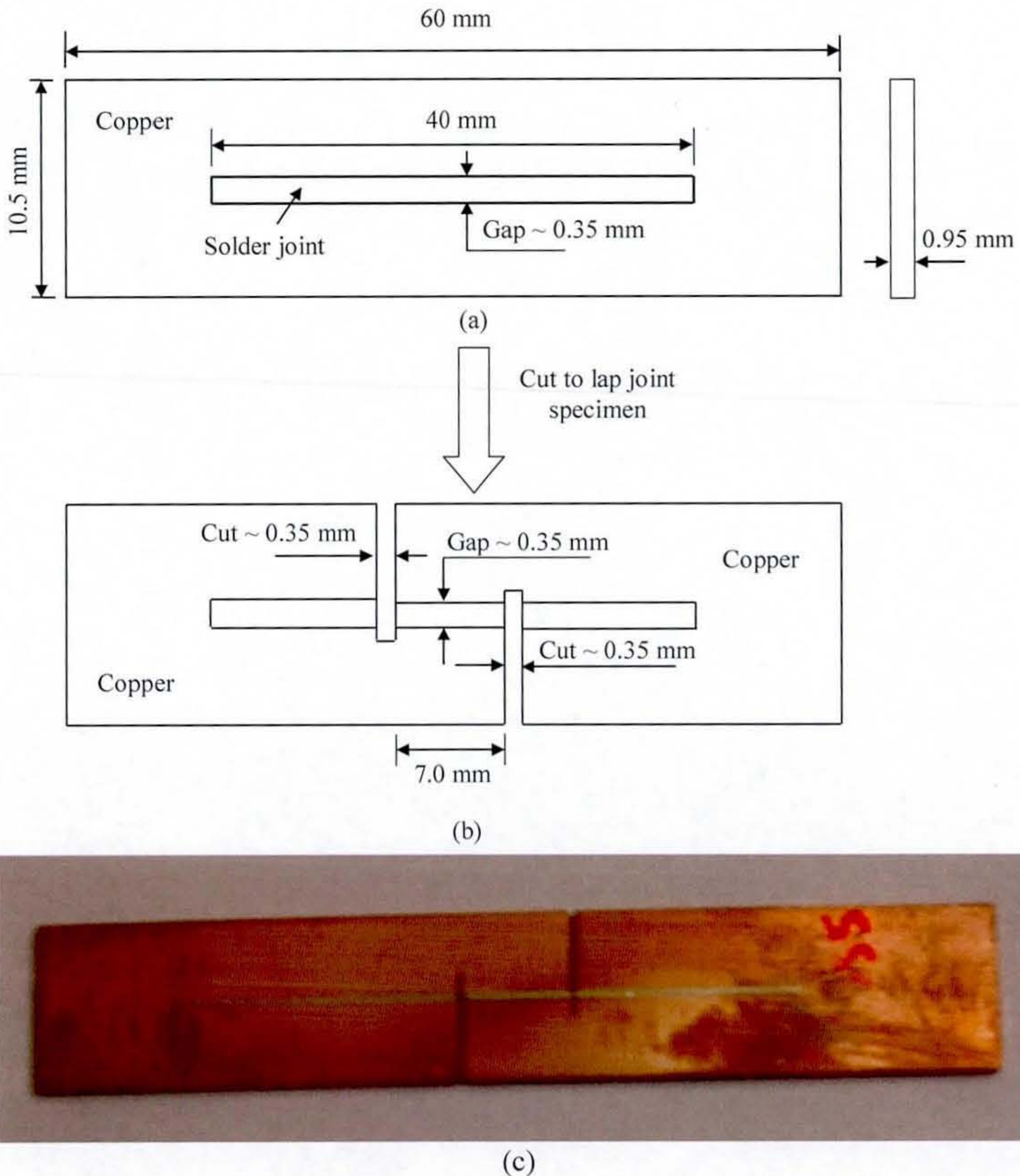


Fig. 7-8: Fabrication of lap solder joint: (a) copper specimen after formation of solder joint and grinding; (b) final shape of specimen; and (c) actual specimen after final polish

7.3.2 Creep Testing Method

The application of a shear load in the creep tests is shown in Fig. 7-9. Generally, the load application method was similar to that used in tensile creep tests, but, due to the fact that the load carrying cross sectional area of the solder joint is parallel to the

direction of the applied load, the solder joint is exposed to a simple shear load. Displacement measurement during the creep test was again done using the sensitive Instron extensometer. The test was also simulated using finite element analysis.

A 2-D finite element model of the solder joint specimen was built with the dimensions given in Fig. 7-10. Finite element modelling was performed using plane strain elements. One end of the model was fixed and a uniform displacement was applied at the other end, as illustrated in the Fig. 7-10. This represents the loading method used in the creep tests. The joint was modelled as having elasto-plastic material properties, while the copper substrate was modelled as linear elastic, due to its elastic response under the loading conditions used in the actual creep test.

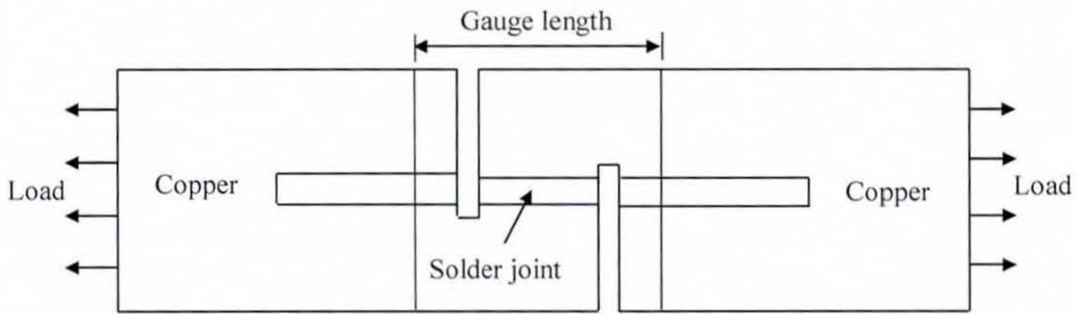


Fig. 7-9: Shear load application for the creep tests

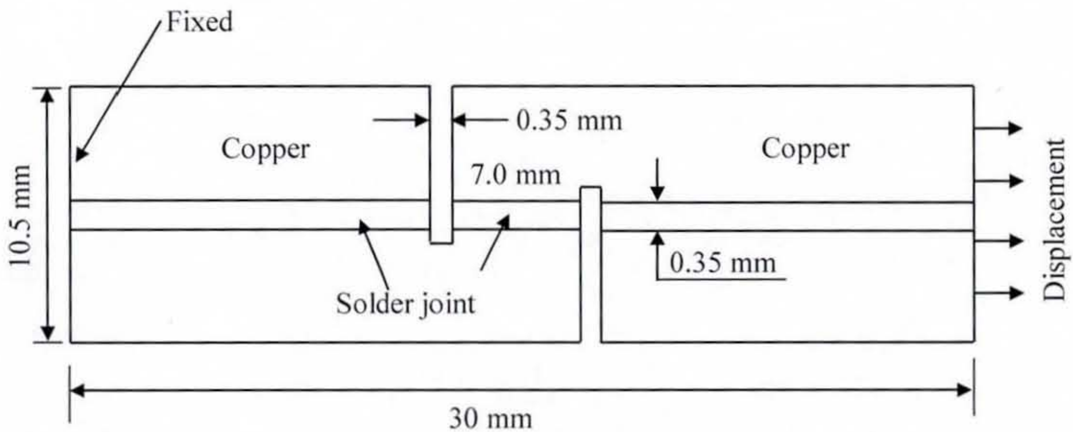


Fig. 7-10: Geometric and boundary conditions used in FEA

The displacement field in both the solder joint and copper were evaluated using FEA and the resulting UX displacement is presented in Fig. 7-11. The results confirmed

that during tensile loading of the copper bar the resultant shear strain is uniformly distributed through the solder. Even though the shear strain distribution in the copper parts is uniform, it is negligible compared to the distribution in the solder joint, as illustrated by Fig. 7-12 (a). This indicates that virtually all the strain appears in the solder joint. Figure 7-12 (b) shows the distribution of shear strain in the middle of the solder joint (along line 2). This distribution demonstrates that the shear strain is also uniform for most parts of the solder joint along the loading direction, except at the end due to the local distortion of elements. Therefore, these FEA results confirm that the solder joint deformation is essentially in simple shear. It is pertinent to note that, in reality; for components assembled onto substrates, both will tend to bend slightly i.e. the solder does not experience only simple shear, and there will be bending moments as depicted in Fig. 7-11 by the minimal, but real, change in the displacement. Thus, the displacement (δ_{ext}) recorded using the extensometer was considered to be the deformation of the solder joint and was used for the analysis of the results.

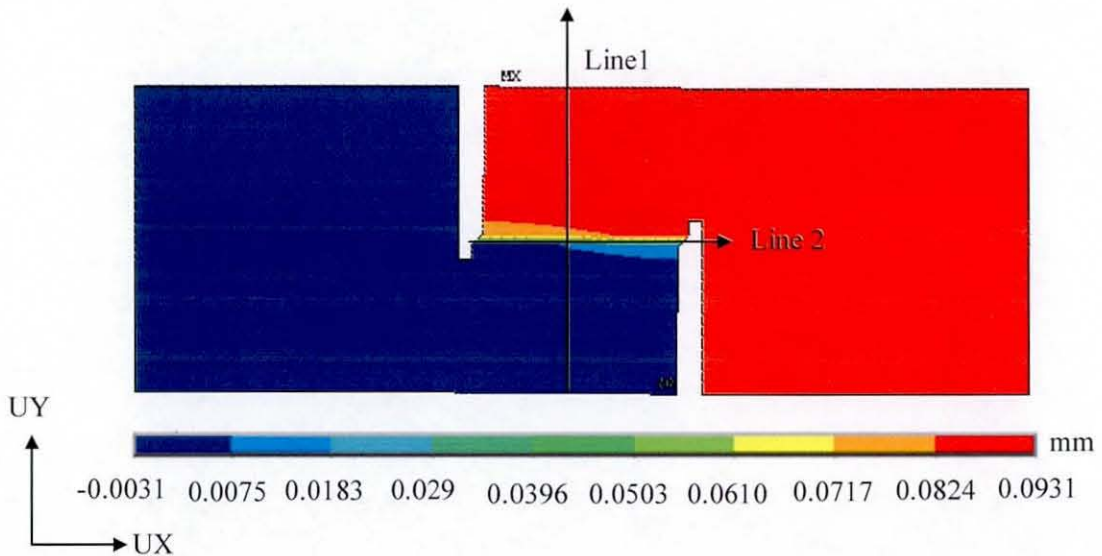
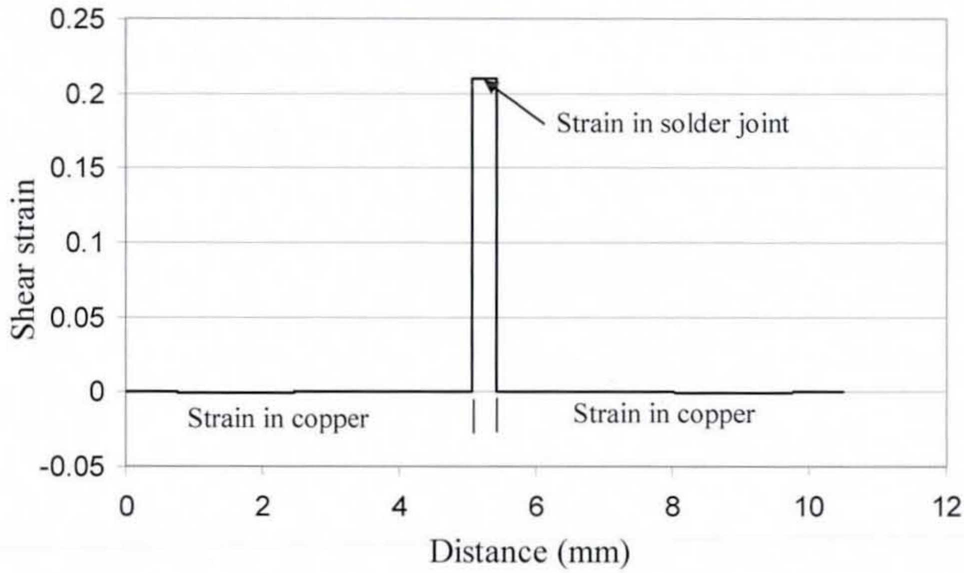
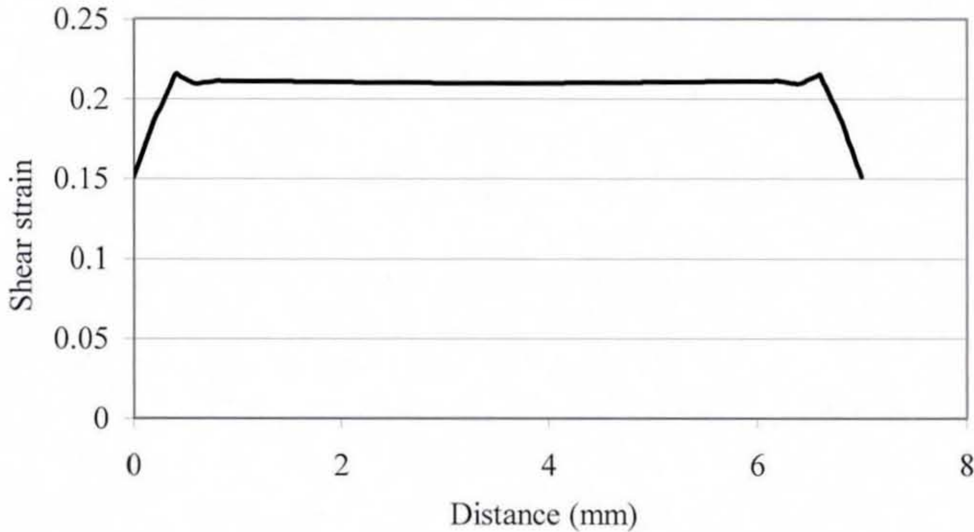


Fig. 7-11: FEA model of creep specimens showing direction and orientation of UX displacement



(a)



(b)

Fig. 7-12: Variation of local shear strain field in the creep specimen: (a) along line 1; (b) along line 2

In order to decide the stress levels for these tests, sample creep tests were carried out at stress levels 5 MPa, 7.5 MPa and 10 MPa. The time required for failure of solder joint was compared against that in the 26.7 MPa tensile creep tests. The lap solder joint at 5 MPa stress failed within about the same time range as observed for the 26.7 MPa tensile creep tests. Therefore, 5 MPa was taken as the highest stress level for the shear creep tests and other stress levels were selected at 10, 30, 50 and 70 percent of the highest stress level (5 MPa) i.e. 0.5 MPa, 1.5 MPa, 2.5 MPa and 3.5 MPa

respectively. All creep tests were carried out at room temperature, and a temperature of 295 ± 2 K was maintained throughout the experiments to avoid any effect of temperature. The shear creep tests were continued until either the failure of the specimen or at least 8 hrs. From the measured deformation (δ_{ext}) of the solder joint, the shear strain, γ, was calculated as:

$$\gamma = \frac{\delta_{ext}}{H_s} \qquad 7.1$$

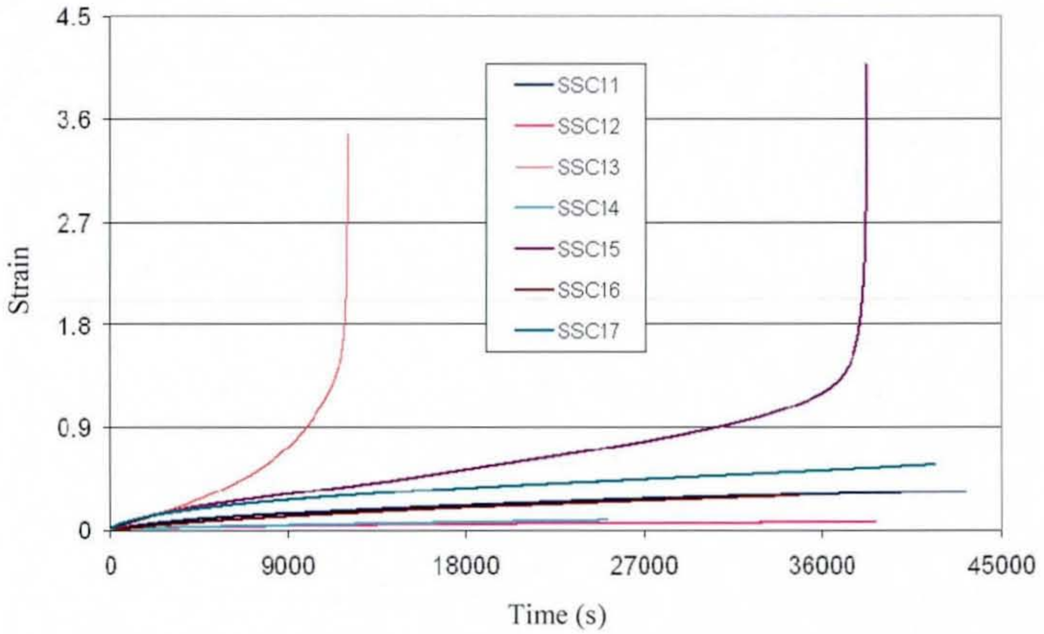
where H_s is the height of the solder joint equal to the gap in Fig.7-8. For every stress level 7 specimens were creep tested to ensure sufficiently accurate statistics, based on the study conducted on pure copper specimens that was discussed in section 6.2.3. In each creep test, the specimen was ramped to a specified stress with a displacement rate of 0.005 mm/s. This initial displacement rate was the same for all stress levels.

7.3.3 Results and Discussion

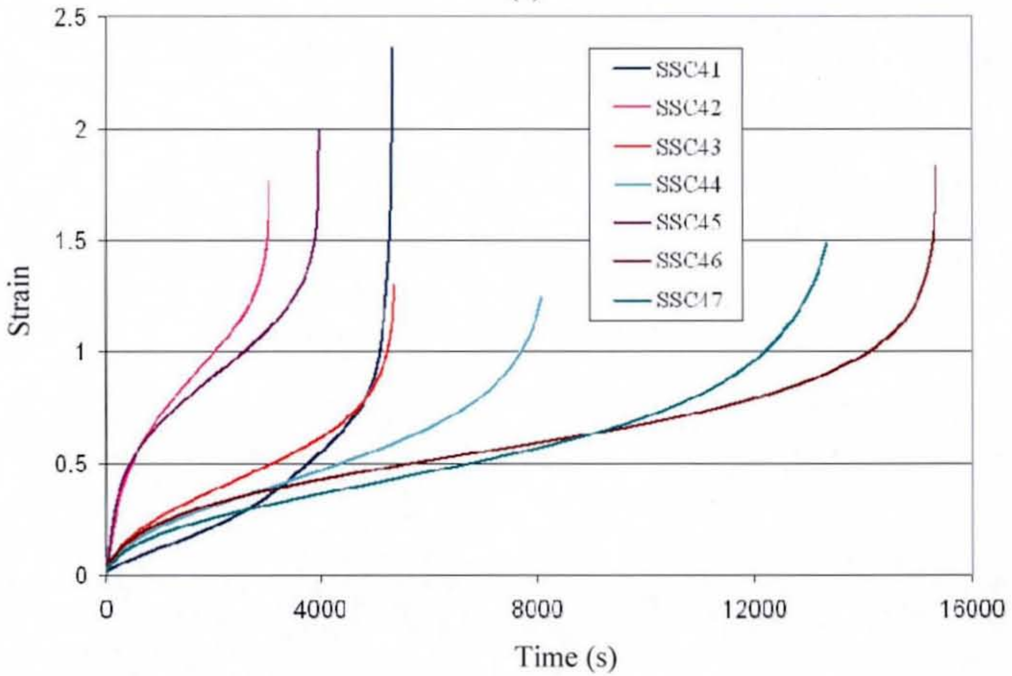
The shear creep curves at stresses of 1.5 MPa and 5.0 MPa are illustrated in Figs. 7-13 (a) and (b), respectively. The creep curves are presented only for these two stresses due to the similar variation and dispersion of creep data at all stress levels, but the creep curves for all stress levels were analysed. As commonly observed in a creep curve, three stages of creep are clearly distinguishable. The creep response of the solder joint for the applied stress demonstrates that the primary and secondary stages of creep are generally observed, while the tertiary stage depends on the applied stress or the quality and microstructure of the solder joint. It is evident from Fig. 7-13 that significant scatter in the creep behaviour is exhibited both in terms of creep strain accumulation and time to failure. The dispersion of the creep data was studied using the secondary/steady-state shear strain rate.

For each stress level the weakest and strongest samples were identified. Since the estimation of the steady-state strain rate was of primary importance, the secondary stage of creep was identified for each of these creep curves and the slope was calculated as explained in Section 7.2.2. The slope of this section of the curve is the steady-state shear strain rate. A comparison of these strain rates plotted against applied

stress on a logarithmic scale is shown in Fig. 7-14. An order of magnitude of difference in secondary creep strain is observed between the weakest and strongest solder joints, which is similar to the spread observed in the tensile creep tests.



(a)



(b)

Fig. 7-13: Scatter of shear creep curves for stress levels: (a) 1.5 MPa; (b) 5.0 MPa

The variation of the steady-state strain rate with applied shear stress was again fitted to the sine hyperbolic creep constitutive model, as discussed in section 2.3.2, using a non-linear curve fitting method. It was done using a combination of hand calculations and Microsoft Excel. The obtained parameters are presented in Table 7-2. The activation energy was again assumed to be 72.93 kJ/mol. Based on these parameters, a comparison of the experimental steady-state shear strain rates with the strain rates reproduced using the hyperbolic sine model were made, and is presented in Fig. 7-14 for both the weakest and strongest joints. The predicted behaviour matches very well with the experimental data, showing the solder joint creep behaviour can be very well represented by this model.

Table 7-2: Parameters for hyperbolic sine constitutive equation for creep under shear load

Steady state shear strain rate	$B_1 \times 10^8$ (1/sec)	β (1/MPa)	p	Q (kJ/mol)
Weakest	16.4	0.18	1.60	72930
Strongest	1.48	0.18	1.96	72930

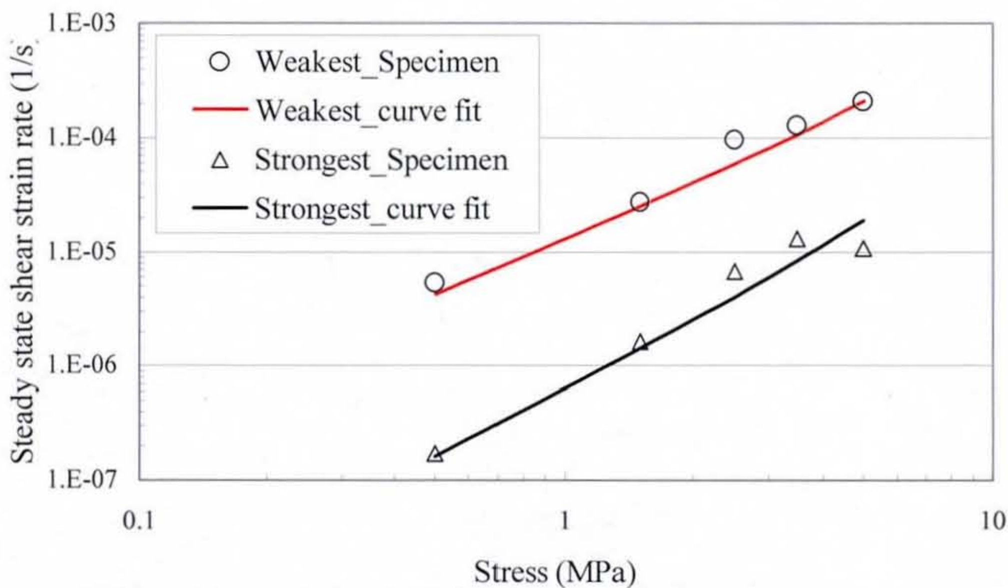


Fig. 7-14: Comparison of experimental and hyperbolic sine law creep data for the weakest and strongest solder joints

As for the tensile tests, to understand the dispersion in the creep data, the microstructure of the creep tested lap solder joints was studied. As before, the weakest (e.g. SSC13 and SSC42) and strongest (e.g. SSC12 and SSC46) samples for each stress level were identified and polished. The polishing methods used were discussed in section 6.5.2. The microstructural study included identification of Sn-grains, determination of Sn-dendrite orientation, and the number of voids in the solder joint. The observations from this microstructure study are very similar to those for the tensile stress-strain and creep tests. The weakest solder joints possessed either a higher number of Sn-grains or voids, unlike the strongest specimens which showed few, or sometimes only single, Sn-grain. The microstructures resembled those depicted in Figs. 7-3 and 7-5, respectively for the weakest and strongest joints. One distinctive observation made in the microstructure study of the shear creep tested specimens was the deformation of Sn-dendrites, which is illustrated in Fig. 7-15. Unlike the tensile specimens, the Sn-dendrites in the shear tested specimens had become mostly perpendicular to the applied load, which results in a lower strength in the shear direction. As the shear load was applied the Sn-dendrites deformed in the shear direction, as shown in Fig. 7-15. The microstructure investigation also showed that the intermetallic layer between the solder joint and the copper substrate was not affected by the shear load. This was evident from the failure of the solder joint always occurring at the interface between the solder and intermetallic layer. Microstructure study of SSC41 solder joint showed similar microstructure that of weakest solder joints, but its creep response was unlike the weakest joints with tertiary creep starting very early. This behaviour could be due to the worst combination of number of voids and Sn-grains in the solder joint.

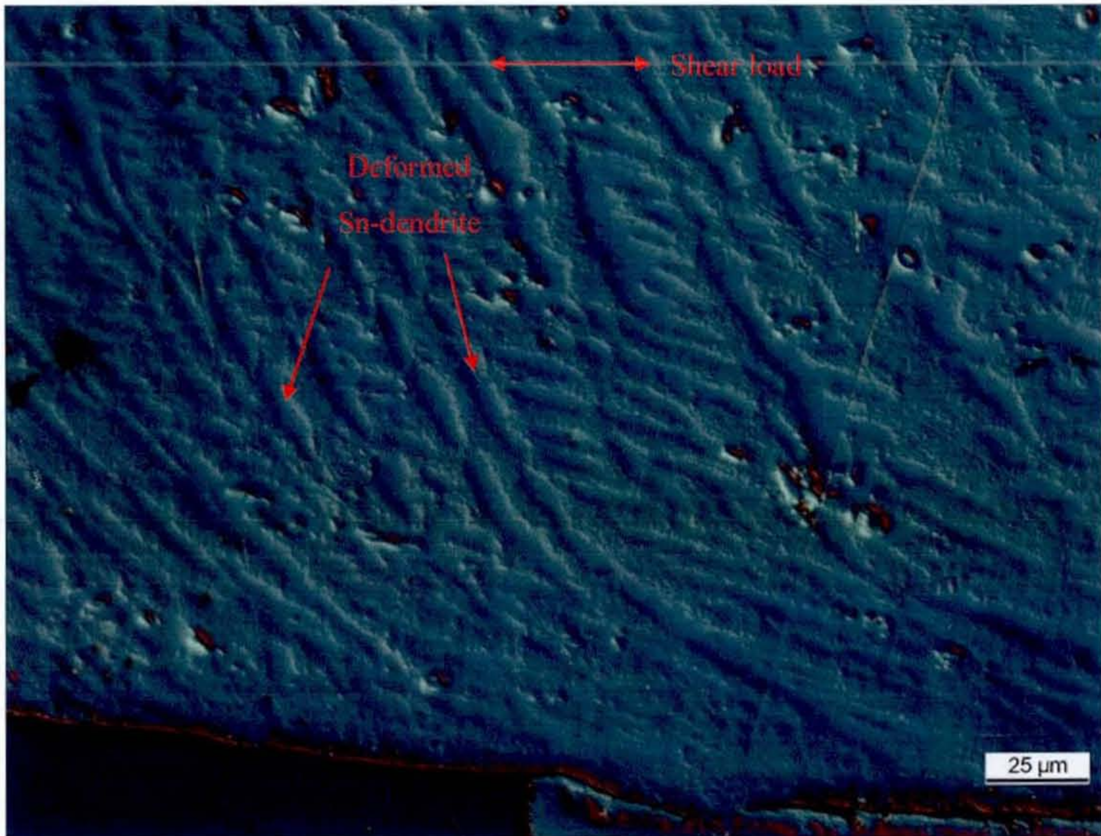


Fig. 7-15: Deformation of Sn-dendrites under shear loading

7.4 Tensile Creep Testing of Bulk Solder

After measuring the creep properties of small-scale solder joints under tensile and shear loading, creep tests were also performed on bulk solder samples with same alloy composition. As the tensile stress-strain results demonstrated that the solder joint stress-strain properties are very different from those of the bulk solder, creep tests were carried out for the latter to estimate the creep performance, for comparison with that for the solder joints under tensile and shear loads. This section discusses the experimental work carried out to obtain the creep properties of bulk solder.

7.4.1 Specimen Preparation and Creep Test Methodology

Sn3.8Ag0.7Cu bulk solder specimens for the creep tests were reflow-fabricated using the fabrication process explained in section 6.3.1. Dog-bone specimens with dimensions according to the ASTM standard for tensile testing were used, as shown in Fig. 6-8. The creep tests were conducted using the same Instron MicroTester machine

used in the solder joint tests. The displacement measured using the extensometer (δ_{ext}) gave the actual deformation of the bulk solder within the gauge length due to the absence of any substrate material. This displacement data was later used to calculate the creep rate of the bulk solder. As for the solder joint creep tests, the bulk specimens were also tested at constant stress. The stresses used were 5 MPa, 10 MPa, 15 MPa and 20 MPa i.e. 19, 38, 58 and 77 percent of the yield stress of 26 MPa, as discussed in section 6.3.2. At every stress level 7 specimens were tested and the tests lasted at least 8 hrs, to capture the secondary stage, or until the failure of the specimen.

7.4.2 Results and Discussion

The creep results for the bulk solder are presented in detail only for the tests at a stress of 5 MPa due to the similarity in the behaviour at the other stress levels. These strain-time results are given in Fig. 7-16. As expected, in the low-stress creep tests the bulk solder exhibited only primary and secondary creep for the chosen duration (8 hrs) of the tests. Unlike the bulk stress-strain curves, the creep curves showed a high dispersion, which is evident from Fig. 7-16. A similar spread between the creep curves was observed for the other stress levels i.e. 10 MPa, 15 MPa and 20 MPa. The dispersion of the creep data was studied in terms of the steady-state or secondary creep rate. Figure 7-17 demonstrates the variation of strain rate with applied stress for both weakest and strongest bulk samples. As observed in the case of solder joints, the steady-state strain rate increases with the stress level. The figure also demonstrates that the steady-state strain rates for the weakest and strongest joints are approximately separated by an order of magnitude throughout the stress range.

The data for the bulk sample steady-state strain rates was also fitted to the hyperbolic sine constitutive equation. The obtained parameters are presented in Table 7-3. The activation energy of bulk Sn3.8Ag0.7Cu solder was again assumed to be 72.93 kJ/mol. Using these parameters in the hyperbolic sine equation (Eq. 2.35), the steady-state strain rate from the experimental results was reproduced for both weakest and strongest samples. Figure 7-17 presents the comparison of both experimental data and curve fits for both weakest and strongest bulk solder samples.

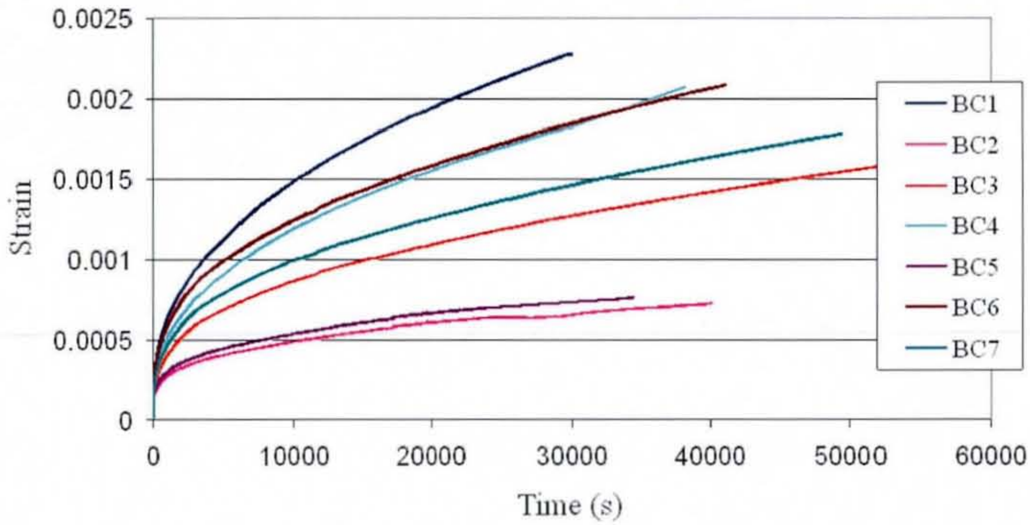


Fig. 7-16: Tensile creep results for bulk solder specimens at a stress of 5 MPa

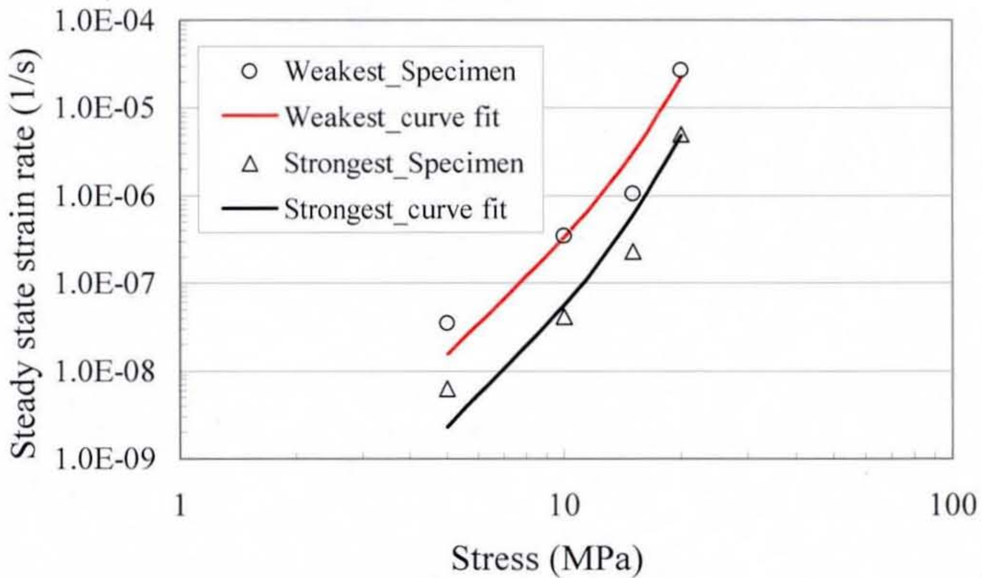


Fig. 7-17: Comparison of experimental creep data for bulk solder with the fitted hyperbolic sine model for weakest and strongest joints

Table 7-3: Fitted parameters for hyperbolic sine constitutive equation of creep for bulk solder

Steady state strain rate	$B_1 \times 10^5$ (1/sec)	β (1/MPa)	p	Q (kJ/mol)
Upper bound	16.4	0.098	3.80	72930
Lower bound	2.46	0.10	3.95	72930

A microstructural study of the creep-tested bulk specimens was carried out after identifying the weakest (e.g. BC1) and strongest (e.g. BC2) specimens. In spite of using the same fabrication process and testing conditions, the spread of the strain rates for the bulk solder is of an order of magnitude; however such large differences were not observed for the tensile tests/results. The material properties of metals and alloys are determined by the microstructure of the material. As discussed in chapter 3, the microstructural features that affect creep properties include: grain size, the distribution of the matrix and phases, dislocation line defects, and point defects such as vacancies and interstitial atoms. The bulk solder microstructure consists of Sn-grains, Sn dendrites, and β-Sn matrix. The presence of grain boundaries results in grain boundary sliding, which contributes to creep under constant load. There are also boundaries between the Sn dendrites and surrounding eutectic phase. These dendritic boundaries are also prone to sliding under load. However, tensile tests are generally carried out at much higher strain rates than creep tests, thus the time available for such deformation mechanisms is less. In addition, the orientation of grains with respect to the applied load is an important factor in the sliding of grain and dendritic boundaries. The distribution of Sn-grains in the weakest and strongest bulk solders were pretty much the same. However, the internal microstructure showed some differences in the distributions of Sn dendrites and the Sn-rich phase, along with the distribution of Ag_3Sn and Cu_6Sn_5 particles in them. The microstructure of the weakest (BC1) and the strongest (BC2) solder specimen is illustrated in Figs. 7-18 (a) and (b), respectively. It is evident from a comparison of their microstructures that the weakest specimen possessed fewer Sn dendrites than the strongest specimen. The Sn-rich phase present in the weakest specimen contained fine particles of Ag_3Sn and Cu_6Sn_5, while

comparatively larger Ag_3Sn and Cu_6Sn_5 particles were present in the Sn-matrix of the strongest specimen. These large Ag_3Sn and Cu_6Sn_5 particles are hard and strengthen the alloy [131]. These hard particles also serve as the most effective blocks for crack propagation [131]. This difference in microstructure between weakest and strongest specimen was observed at all stress levels and this could explain the spread in the creep behaviour for bulk solder.

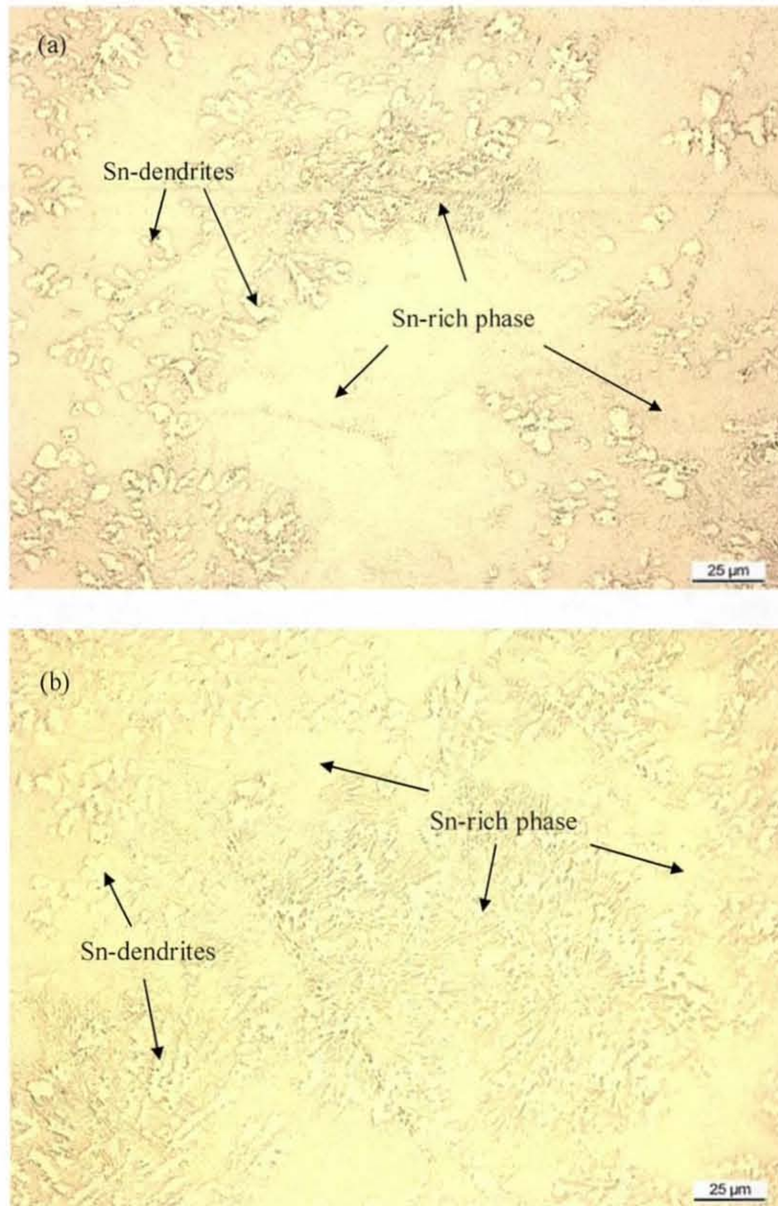


Fig. 7-18: Microstructure of the bulk solder specimen: (a) weakest (BC1); (b) strongest (BC2)

7.5 Comparative Study of Creep Properties

Having carried out creep tests on bulk solder and on small-scale solder joints in both tension and shear, a comparative study of the resulting steady-state creep data was performed. The experimentally obtained rates were fitted with the hyperbolic sine creep model. Then, a comparative study of the tensile and shear creep data for the solder joint and bulk solder was done with the help of the creep model fitted to the experimental results, due to the dissimilar stress levels used in the different creep tests. For the purpose of easy comparison, the steady-state shear strain rate, $\dot{\gamma}_s$, and corresponding shear stress, τ, were converted to an equivalent tensile steady state strain rate, $\dot{\varepsilon}_s$, and tensile stress, σ, using the von Mises transformations.

$$\dot{\varepsilon}_s = \left(\frac{1}{\sqrt{3}}\right)\dot{\gamma}_s \qquad 7.2$$

and:

$$\sigma = \sqrt{3}\tau \qquad 7.3$$

Figures 7-19 and 7-20 show a comparison of the fitted steady-state equivalent strain rate data against equivalent stress for the weakest and strongest specimens, respectively, under the three different testing conditions. A common feature in all three sets of creep data is the change in the slope of the curve as the stress increases. Due to this characteristic of the curve, the stress exponent p no longer remains constant and increases with the increase in the stress level. This is known as a power-law breakdown and therefore shows why a simple power law is inadequate to model the solder behaviour. However, the multiplier used with the hyperbolic sine law allows it to describe the creep behaviour over an extended range of applied stresses. It is evident from the variation of the steady-state strain rate that the tensile creep data for the tensile tested solder joints and bulk solder essentially have a similar slope, with stress exponent values between 3.8 and 5.3. However, the bulk solder possesses a lower creep resistance compared to that of the solder joints, as for a given stress the strain rate of the bulk solder is about two orders of magnitude higher than that of the tensile solder joint at low stress levels, decreasing to an order of magnitude at higher stress levels. The obtained value of the stress exponent p is within the expected range for solder alloys for which it generally lies between 3 and 17 [44].

Comparison of the shear and tensile creep data indicates that the solder joints under shear load were very much weaker, with the highest steady-state strain rates out of the three creep data sets. The slope of this curve - converted into tensile units - is also different from the tensile creep data shown in Figs. 7-19 and 7-20. The stress exponent value for the shear creep data varies between 1.6 and 1.96, which is lower than that for the tensile case. Such a difference in the stress exponent translated into big differences in the steady-state strain rates. For the solder joint, the difference between shear converted into an equivalent tensile and tensile strain rates is six orders of magnitude at low stress levels, decreasing to three orders of magnitude for higher stress levels. However, the difference in strain rates between the shear solder joint and bulk solder varies from five orders of magnitude at low stress levels to just one order of magnitude at higher stress levels.

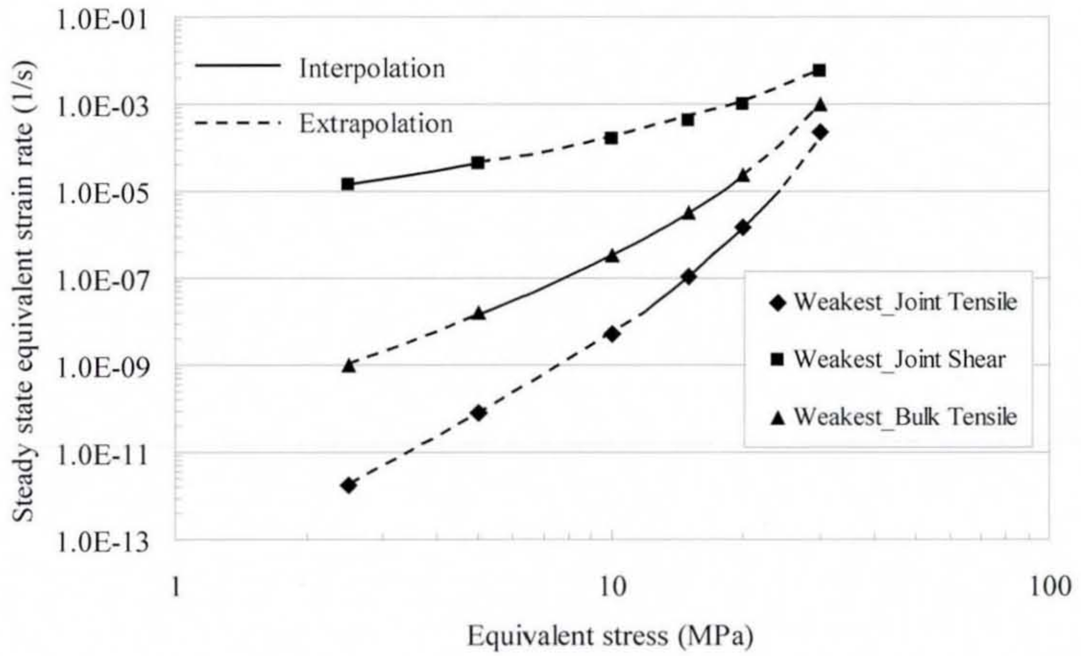
Thus, the comparison of creep data indicates that the creep resistance of the solder joint under tensile loading is higher than that of the bulk solder under a tensile load and of the lap solder joint under shear load. This is due to the higher tensile strength of the solder linked to its gap size and microstructure. This comparison signifies that the creep behaviour of the solder joint under tensile and shear loads is different, which means a simple von Mises transformation may not be sufficient. Even though the internal microstructure of the solder joints in both tensile and shear creep tests was essentially the same for both weakest and strongest specimens, the orientation of grains and Sn dendrites with respect to the applied load has a significant effect on the creep behaviour for the different types of load. Since the composition of the solder alloy was 95.5 % of Sn (tin), the anisotropy of the tin [19] could have contributed to the large difference between tensile and shear creep properties. For instance, due to the anisotropy of the Sn, the Young's modulus may vary by a factor of three with crystallographic direction [19]. In addition, during shear creep testing, shear deformation takes place in the solder between the stiffer intermetallic layers of Cu_6Sn_5 [132]; as a result hydrostatic does not develop in the solder joint, which eliminates the size effect.

It is clear from Figs. 7-19 (a) and (b) that the creep properties of the bulk solder lies between the solder joint creep data for tensile and shear load. It was shown in the tensile strength tests that the bulk solder has lower tensile properties than the solder

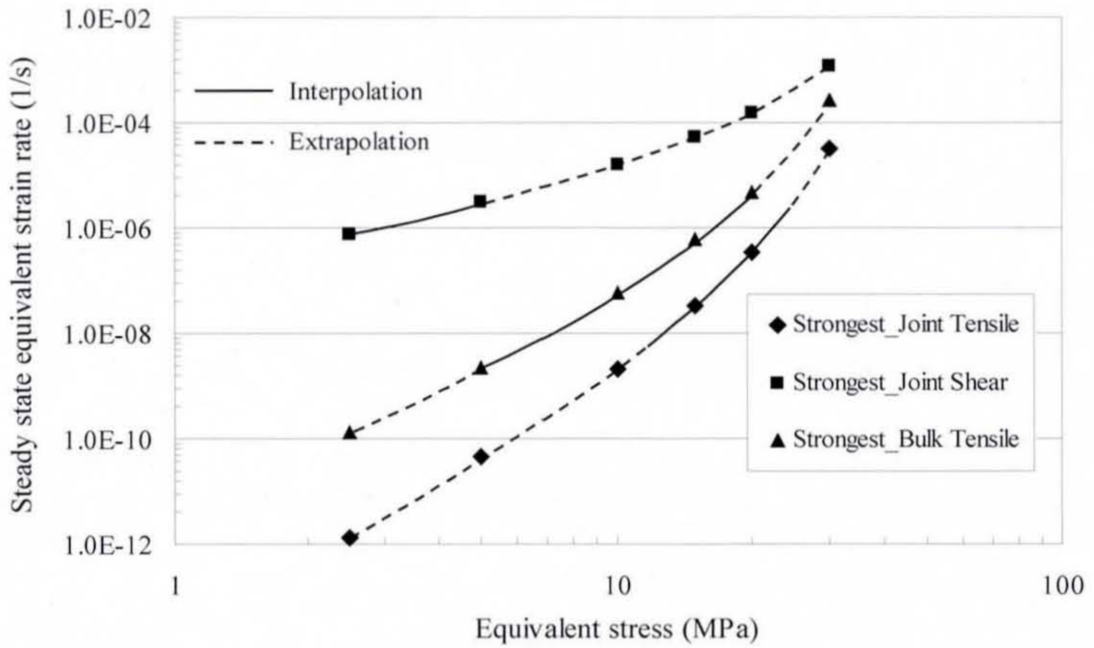
joint. Thus, it was obvious to expect a lower creep resistance for the bulk solder than the tensile solder joint. But, the dissimilarity between the bulk and shear creep data was an interesting outcome from the creep study. The equivalent steady-state creep rate for the solder joints in shear is higher than the tensile steady-state creep rate for the bulk solder. The difference between the microstructures of the solder joints and the bulk solder was discussed in section 6.5.2. Also, previous studies showed that the anisotropy of the tin could lead to a threefold variation in the Young's modulus depending on the crystallographic orientation [10-12]. Therefore, this difference in the creep performance confirms the anisotropic effect of the tin on the solder joint creep properties.

The equivalent steady-state strain rates for bulk/joint tensile and shear conditions for an equivalent stress of 15 MPa are presented in Table 7-4. From comparison of these data, the highest creep resistance was observed for the strongest small-scale solder joints under a tensile load, while the lowest creep resistance was observed for the weakest lap solder joints under shear load. Thus, these two creep behaviours represent the two extreme cases of creep. Therefore, in the FEA based reliability study of the solder joints in a surface mount device presented in chapter 8, the two different creep models are used based on the parameters belonging to these two extreme conditions.

The creep properties were also compared with those for similar alloys published by various researchers. The comparison of experimental steady state strain rate for both solder joint and bulk solder under tensile load with those published by Pang *et al.* [128] for Sn3.8Ag0.7Cu is presented in Fig. 7-20. The comparison shows good agreement between the author's creep data and the data reported by Pang *et al.* The author's small-scale solder joints showed a higher creep resistance, while less than an order of magnitude difference is observed between the two sets of bulk solder creep data. This could be due to the difference in the fabrication process wherein Pang *et al.* fabricated their specimen from the bulk solder bar.



(a)



(b)

Fig. 7-19: Comparison of steady-state strain rates for the three type of creep tests for: (a) weakest specimens; (b) strongest specimens

Table 7-4: Comparison of steady state strain rates at an equivalent stress of 15 MPa

Creep test condition	Steady state strain rate (1/s)	
	Weakest specimen	Strongest specimen
Lap shear solder joint	4.29×10^{-4}	5.19×10^{-5}
Tensile bulk solder	3.11×10^{-6}	5.94×10^{-7}
Tensile solder joint	1.08×10^{-7}	3.27×10^{-8}

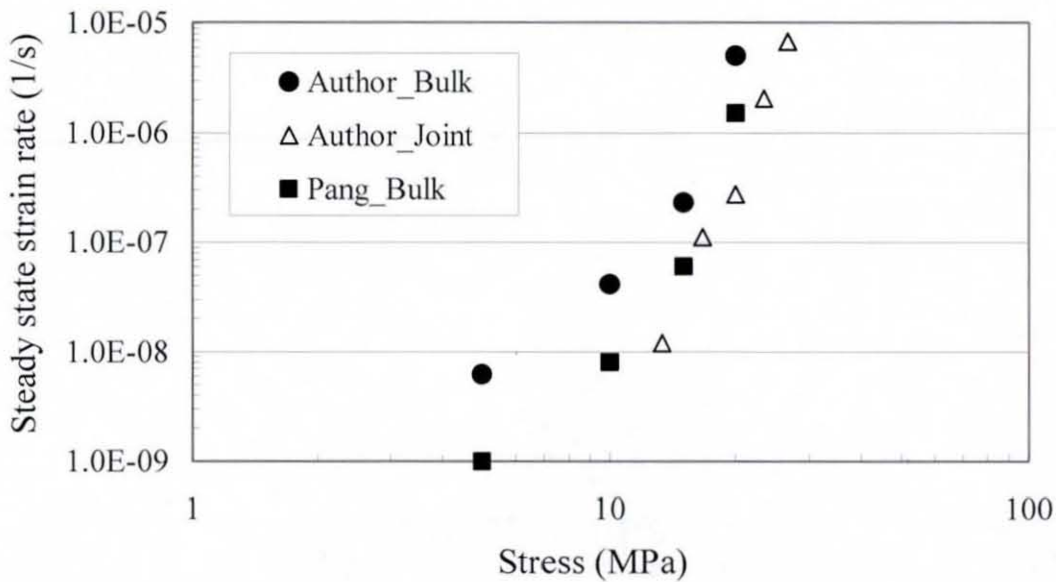


Fig. 7-20: Comparison of steady-state strain rates with those of Pang *et al.* [1]

The steady state creep data for the lap solder joints were also compared with those published by Dusek *et al.* for Sn3.8Ag0.7Cu [129] and by Zhang *et al.* for Sn3.9Ag0.6Cu [47], which are shown in Fig. 7-21. The author's predicted creep data show higher shear strain rates than the other studies. Unlike the author's fabrication process, Dusek *et al.* used water quenched cooling to fabricate the solder joints; therefore, the steady state strain rates are lower due to this fabrication process resulting in a finer microstructure and therefore higher creep resistance. The fabrication process used by Zhang *et al.* is unknown, but at higher stress levels the difference from the author's creep data decreases. The lap solder joints used by the author were 2.5 times longer than that tested by Dusek *et al.* and Zhang *et al.*, while the solder joint height at 0.35 mm was between those of Dusek *et al.* (0.4 mm) and Zhang *et al.* (0.18 mm). Thus, the comparison study indicates that the solder joint material data used in the

reliability study should be determined by employing the fabrication process used in the electronic packaging under reliability study.

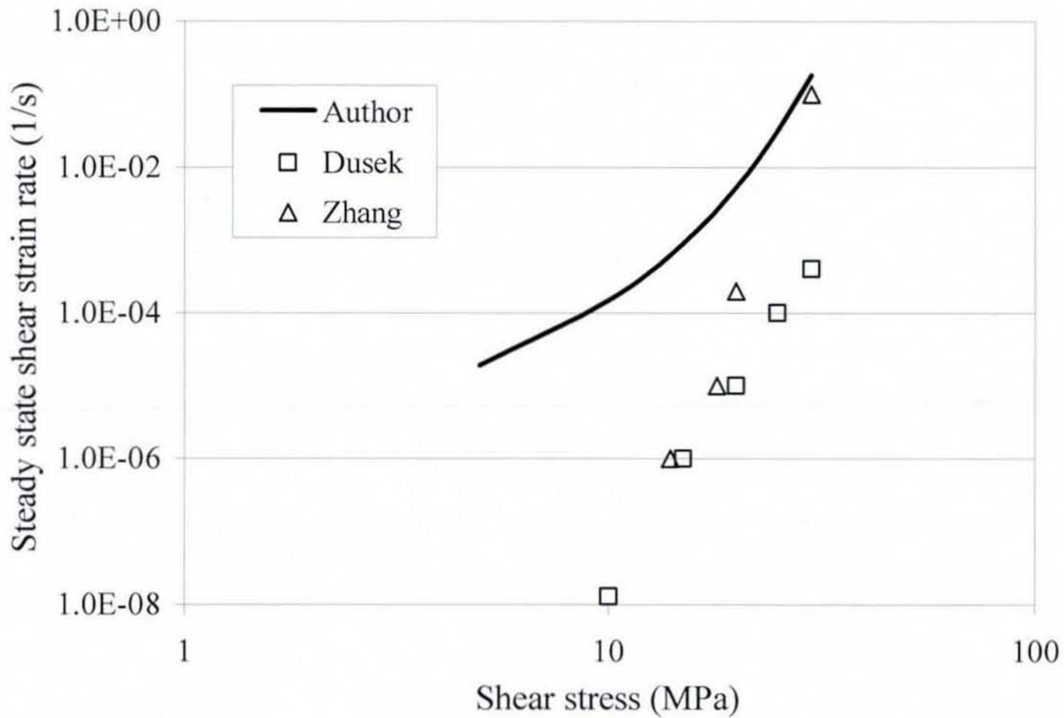


Fig. 7-21: Comparison of steady-state strain rates for lap solder joints with published data

7.6 Summary

In this chapter the methods for experimentally obtaining creep properties of solder joints under tensile and shear loads, and bulk solder under a tensile load were described and the results compared and discussed. The creep data for each type of loading condition showed significant dispersion, in spite of the use of same fabrication processes and testing conditions. The dispersion was as high as an order of magnitude, which was shown to be caused by the variations in the microstructure. The creep results comparison revealed that solder joints under tensile load have a higher creep resistance than the bulk solder under tensile creep and the solder joint under shear load. Another pertinent outcome of the experimental study was the dissimilarity in the tensile and shear converted into equivalent tensile creep data for the solder. Thus, obtaining creep data under any one type of load (tensile or shear) and using the von Mises transformation may not provide a realistic representation of the material behaviour. Therefore, determination of creep properties under both types of load is

sensible. The experimental steady-state creep data was a good fit to the hyperbolic sine creep equation, which can be conveniently used in the simulation of the solder joint creep behaviour.

8. Finite Element Simulation of Surface Mount Assembly

As discussed in chapter 4, finite element simulations have been widely used in reliability studies of solder joints due to their advantages over experimental reliability tests. The outcome of the simulation completely depends on the formulation and representation of the in-field conditions. The experimental studies presented in chapters 6 and 7 showed that the material properties of small-scale solder joints are significantly different from those of bulk solder. The actual operating conditions of a surface mount assembly are also different from the general assumption of uniform temperature distribution as discussed in chapter 5. Therefore, with the help of finite element simulations, the solder joint reliability is evaluated by considering the actual operating conditions and the solder joint material properties determined from experiments.

8.1 Introduction

As discussed in chapter 1, modern surface mount assemblies are the result of miniaturisation and cost reduction of electronic products. Some surface-mount components require high numbers of I/Os, and at the same time the size of solder joints has reduced in some cases to dimensions less than 100 μm. As electronic assemblies have miniaturised, manufacturing reliable products has become an increased concern to the industry. As discussed in chapter 4, the small solder fillets of surface mount components, such as chip resistors, must accommodate the strains due to mismatches between the thermal expansion of the component and the substrate. Consequently, when the electronic assembly/package is subjected to changes in temperature, a thermally driven strain-controlled operating regime is developed. The changes in the temperature could be due to powering on/off of packages as well as variations in ambient temperature. As discussed above, these thermal loads vary cyclically. The solder joints also experience creep, due to their high operating temperatures wherein the homologous temperature (T_h) could vary between 0.45 and 0.85. These operating temperatures generally cyclic, and therefore result in fatigue failure of the solder joint.

Although there are various standardised accelerated methods for assessing the reliability of solder joints in electronic applications, there are significant difficulties associated with solder joint reliability testing, such as the cost of designing and constructing test samples and the time necessary to obtain useful reliability data. Also, the tested configuration may not be exactly the one a customer is interested in. Therefore, with the help of finite element analysis, the required geometry can be simulated for the actual operating conditions and so the in service fatigue life of the solder joints assessed. Thus, by reducing the cost and time-to-market, customer requirements can be satisfied. In fact, IPC-9701 [82] permits the use of finite element analysis to predict the solder joint fatigue life for new products that are similar to those already tested. Thus, finite element analysis has become a very important tool for reliability studies of the solder joints of various shapes and sizes used in electronic assembly.

In this chapter, such numerical methods are used for the reliability assessment of lead-free solder joints. This is carried out using a model for the surface mount chip resistor assembly described in chapter 5. This component has solder joints susceptible to fatigue failure in operation. The use of suitable material models and representative temperature boundary conditions also play a vital role in such reliability studies. The experimental results presented in previous chapters demonstrated that the material properties of the solder joint are significantly different from those for the bulk solder. Also, the equivalent creep properties of solder joints under tensile and shear loads have been shown to be different. Based on these experimental outcomes, the stress-strain behaviour of the solder joint at relevant strain rates is captured for use in the simulation. Creep, a prominent deformation mechanism in solder joints, is modelled using constitutive equations, which are implemented in the commercial finite element software ANSYS.

In actual operation, the solder joints in surface mount chip resistors are expected to experience both plasticity and creep. Therefore, this problem was solved in two stages of modelling complexity, starting with inclusion of pure plasticity and culminating in combined plasticity and creep. In the initial simulations, elasto-plastic analysis of both 2D and 3D representations of the chip resistor assembly were carried out. This enabled a decision as to the kind of geometric model (2D or 3D) to be considered for the more

complex models. The final phase of simulations was carried out incorporating both plasticity and creep for two models with different thermal boundary conditions. In the first analysis the experimentally obtained temperature distribution in the chip resistor assembly was used as the thermal boundary conditions, and a comparison was made with a uniform temperature distribution. Finally, the fatigue life of the solder joint was estimated based on the finite element simulation results.

8.2 Geometric and FE Modelling of the 1206 Chip Resistor Assembly

2D and 3D representations of the chip resistor assembly were built for the finite element structural analysis. The geometries for the 2D and 3D chip resistor models used here for the structural analysis were the same as those used in the thermal analysis presented section 5.3. The dimensions used in the construction of both 2D and 3D models are shown in Fig. 5-11. Due to the symmetry of the structure only one half of the geometry was considered thereby assuming that the solder joints on either side of the symmetry plane behave identically.

For the analysis, the 2D geometry of the chip resistor assembly was discretised (meshed) using the ANSYS plane strain element PLANE 182. PLANE 182 is a 4-noded quadrilateral elements with two translational degrees of freedom, i.e. in the X and Y directions, at each node. Similarly, the 3D chip resistor geometry was modelled with the 8-noded hexahedral elements SOLID 185. This element has three translational degrees of freedom i.e in the X, Y and Z directions, at each node. While meshing the assembly, a fine-mesh pattern was adopted in and around the solder joint, which is the critical area in the assembly. The quality of the mesh was finalised based on error estimations carried out on both the 2D and 3D models. ANSYS has an in-built error approximation technique based on the Zienkiewicz and Zhu error approximation method [133]. In this method, the initial stress error contributed by each element at each node is calculated as follow:

$$\left\{\Delta\sigma_n^i\right\} = \left\{\sigma_n^a\right\} - \left\{\sigma_n^i\right\} \qquad 8.1$$

where $\left\{\Delta\sigma_n^i\right\}$ is a stress error vector at node n for element i, $\left\{\sigma_n^a\right\}$ is the averaged stress

vector at node n, and $\{\sigma_n^i\}$ is a stress vector for node n of element i. Then, stress bounds are estimated considering the above error and these are:

$$\sigma_j^{mnb} = \min\left(\sigma_{j,n}^{a} - \Delta\sigma_n\right) \qquad 8.2$$

$$\sigma_j^{mxb} = \max\left(\sigma_{j,n}^{a} + \Delta\sigma_n\right) \qquad 8.3$$

where σ_j^{mnb} is a nodal minimum of stress magnitude (SMNB); σ_j^{mxb} is a nodal maximum of stress magnitude (SMXB); j is a subscript to refer to either a particular stress component or a particular combined stress; $\sigma_{j,n}^{a}$ is the average stress level j at node n of elements attached to n; $\Delta\sigma_n$ is the root mean square of all $\Delta\sigma_i$ from elements connecting to node n; and $\Delta\sigma_i$ is the maximum absolute value of any component $\{\Delta\sigma_n^i\}$ for all of the nodes connecting to element i. Based on this method, error estimation was performed for the fillet region of the solder joint (Fig. 5-12) to decide whether the mesh quality for the structural analysis was sufficient. In this study a linear static analysis was conducted for increasingly refined mesh patterns and the maximum average stress (SMX) and its bound SMXB (σ_j^{mxb}) in the solder joint were studied. The quality of the mesh was considered to be sufficient when the ratio of SMXB and SMX was nearly the same for two consecutive mesh patterns. The resulting mesh used in the 2D and 3D FE models is illustrated in Figs. 5-12 and 5-17, respectively.

8.3 Elasto-Plastic Analysis

As mentioned before, the chip resistor solder joint will demonstrate elasticity, plasticity and creep behaviour due to its operating conditions. In reliability studies, plasticity and creep play a very important role, because these induce irreversible deformation in the solder joint. Therefore, this problem was tackled in two steps. In the first step, an elasto-plastic analysis of the 2D chip resistor assembly was conducted to understand the extent of plastic deformation taking place in the solder joint due to plasticity and to help understand what further improvements may be necessary when both plasticity and creep are taken into consideration. In the second step, both plasticity and creep behaviour of the solder joint were considered and this is discussed later. A similar elasto-plastic analysis was also conducted for the 3D geometry; which

was carried out to compare the 2D and 3D stresses and decide upon the kind of geometry to be used when both plasticity and creep are modelled. Therefore, in this section elasto-plastic analysis of the 2D and 3D chip resistor models is discussed.

8.3.1 Boundary Conditions

The boundary conditions for the models include prescriptions of displacements on the nodes at external sides or surfaces of the mesh. This is a vital step in the stress analysis since the stress field in the body is defined by these conditions. Thermal stresses are common in electronic packages, but the determination of thermal stresses in a package is not an easy task. Such electronic packaging assemblies are examples of composite structures that undergo thermal loadings and consist of at least two different materials. They may also be subjected to non-uniform temperature distributions during power cycling. The displacement components (*u*, *v* and *w*) everywhere inside the 3D electronic package are determined by solving the system of equations of thermoelasticity [29]:

$$\frac{\partial^2 u}{\partial x^2}+\frac{\partial^2 v}{\partial x \partial y}+\frac{\partial^2 w}{\partial x \partial z}+(1-2v)\nabla^2 u+\frac{X_x}{(\lambda+G)}=2(1+v)\alpha\frac{\partial T}{\partial x} \quad 8.4a$$

$$\frac{\partial^2 v}{\partial y^2}+\frac{\partial^2 u}{\partial x \partial y}+\frac{\partial^2 w}{\partial y \partial z}+(1-2v)\nabla^2 v+\frac{X_y}{(\lambda+G)}=2(1+v)\alpha\frac{\partial T}{\partial y} \quad 8.4b$$

$$\frac{\partial^2 w}{\partial z^2}+\frac{\partial^2 u}{\partial x \partial z}+\frac{\partial^2 v}{\partial y \partial z}+(1-2v)\nabla^2 w+\frac{X_z}{(\lambda+G)}=2(1+v)\alpha\frac{\partial T}{\partial z} \quad 8.4c$$

with the prescribed stress-displacement boundary conditions and with the calculated temperature distribution as an imposed loading condition. The thermal stresses and strains everywhere inside the package are then calculated using the following constitutive and kinematics equations [29]:

$$\sigma_{xx}=\frac{\lambda}{v}\left[(1-v)\frac{\partial u}{\partial x}+v\left(\frac{\partial v}{\partial y}+\frac{\partial w}{\partial z}\right)\right]-\beta_1(T-T_o) \quad 8.5a$$

$$\sigma_{yy}=\frac{\lambda}{v}\left[(1-v)\frac{\partial v}{\partial y}+v\left(\frac{\partial w}{\partial z}+\frac{\partial u}{\partial x}\right)\right]-\beta_1(T-T_o) \quad 8.5b$$

$$\sigma_{zz} = \frac{\lambda}{v}\left[(1-v)\frac{\partial w}{\partial z} + v\left(\frac{\partial u}{\partial x} + \frac{\partial v}{\partial y}\right)\right] - \beta_1 (T - T_o) \quad 8.5c$$

$$\tau_{xy} = G\left(\frac{\partial u}{\partial y} + \frac{\partial v}{\partial x}\right) \quad 8.5d$$

$$\tau_{yz} = G\left(\frac{\partial v}{\partial z} + \frac{\partial w}{\partial y}\right) \quad 8.5e$$

$$\tau_{zx} = G\left(\frac{\partial w}{\partial x} + \frac{\partial u}{\partial z}\right) \quad 8.5f$$

$$\varepsilon_x = \frac{\partial u}{\partial x} \quad 8.6a$$

$$\varepsilon_y = \frac{\partial v}{\partial y} \quad 8.6b$$

$$\varepsilon_z = \frac{\partial w}{\partial z} \quad 8.6c$$

$$\gamma_{xy} = \frac{\partial u}{\partial y} + \frac{\partial u}{\partial x} \quad 8.6d$$

$$\gamma_{yz} = \frac{\partial v}{\partial z} + \frac{\partial w}{\partial y} \quad 8.6e$$

$$\gamma_{zx} = \frac{\partial w}{\partial x} + \frac{\partial u}{\partial z} \quad 8.6f$$

where $\nabla^2 = \frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + \frac{\partial^2}{\partial z^2}$; T is the instantaneous absolute temperature; u, v, and w are the displacement components in the x-, y-, and z- directions, respectively; X_x, X_y and X_z are the body force components in x-, y-, and z- direction respectively; G is the shear modulus; σ_{xx}, σ_{yy}, and σ_{zz} are the normal stress components acting in x-, y-, and z- direction, respectively; τ_{xy} is the shear stress acting in the y-direction of the plane normal to the x-axis; τ_{yz} is the shear stress acting in the z-direction of the plane normal to the y-axis; τ_{zx} is the shear stress acting in the x-direction of the plane normal

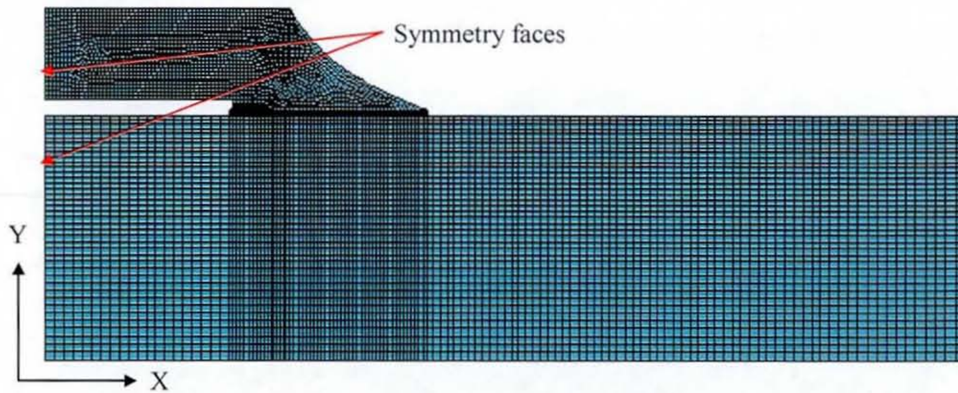
to the z-axis; ε_x, ε_y, and ε_z are the normal strains acting x-, y- and z- direction, respectively; γ_{xy} is the shear strain acting in the y-direction of the plane normal to the x-axis; γ_{yz} is the shear strain acting in the z-direction of the plane normal to the y-axis; and γ_{zx} is the shear strain acting in the x-direction of the plane normal to the z-axis.

In the current FEA, the boundary conditions were defined based on the physics of the chip resistor assembly. A deformation mechanism was explained in Fig. 4-1, where the electronic assembly expands and contracts about a central plane of symmetry. The displacement field is the same on either side of this plane as long as the loads are symmetric. Therefore, a symmetry boundary condition was applied at the symmetric plane faces of the chip resistor models to represent the structural symmetry of the assembly, which is shown in Fig. 8-1. It also prevents any rigid-body motion in the x-direction. For the 2D model the lowest node on the symmetry plane was also constrained in the y-direction to prevent rigid-body motion. For the 3D model, nodes in the lower edge of the symmetry plane were constrained in the y-direction to prevent rigid-body motion. Thus, these boundary conditions simulate the actual conditions of the chip resistor assembly in operation. The half symmetry for the 3D model was used in order to make a comparison of analysis results over the central symmetry plane (z = 0 plane) of the 3D model with those for the 2D plane strain model.

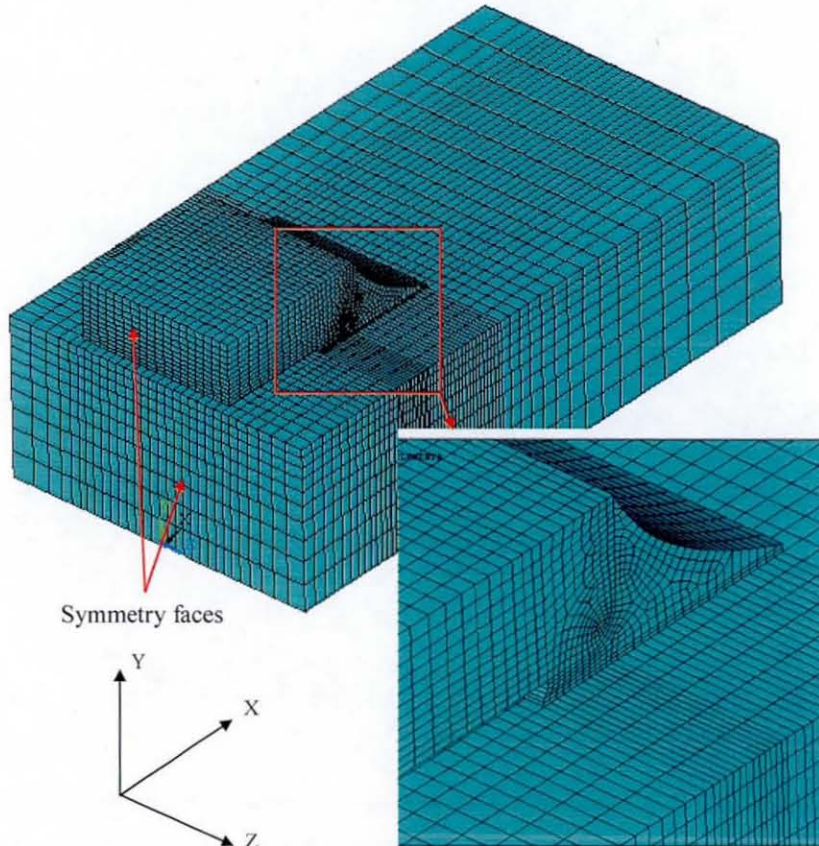
8.3.2 Thermal History

Most solder joint failures in electronic packaging are due to thermo-mechanical fatigue [6, 20, 69, 70, 91]. It has been time and again demonstrated that these failures are due to the cyclic temperature variations in service. Typically, it is common when using FEA to simulate this situation to idealise the entire package and PCB assembly as having a uniform temperature distribution, thus failing to capture any stresses due to spatial temperature gradients within the assembly. However, it has been proven in the experiments reported in Chapter 5 that the actual temperature distribution within the chip resistor assembly is non-uniform during power cycling at room temperature. Another aspect which is commonly neglected is the residual stresses and strains in the assembly after the reflow soldering process by which the solder joints are manufactured. Therefore, two thermal load cases (Cases A and B) were both used

including the reflow process; one with a uniform temperature distribution (Case A) over the assembly to represent traditional thermal cycling tests and the other applying the actual temperature distribution under power (Case B) discussed in chapter 5. These two thermal cases allow a comparative evaluation of the effect of a non-uniform temperature distribution on fatigue damage to the solder joint. The thermal histories used in these two elasto-plastic analyses are illustrated in Fig. 8-2 and 8-3.



(a)



(b)

Fig. 8-1: Boundary condition details for: (a) 2D FE model; (b) 3D FE model

The thermal history consists of cooling from the reflow process temperature to room temperature followed by two temperature cycles. Since plasticity is a time-independent material behaviour, no importance has been given to the rates of change of temperature while deciding the thermal history, and dwells at extreme temperatures were neglected for these plasticity only models. The reflow simulation in terms of cooling from the melting point of 490 K gives an estimate of the residual stresses induced in the solder joint when the temperature of the assembly is brought down to room temperature (294 K), which is represented by line PQ in Figs. 8-2 and 8-3. The two temperature cycles used are QRS and STU. As mentioned before, two cases of thermal boundary conditions were applied to the resistor assembly. These two thermal cases differ only in terms of the temperature distribution within the assembly at points R and T, i.e.:

Case A: In this case, a spatially uniform temperature distribution was assumed for the entire resistor assembly and throughout the time history as shown in Fig. 8-2. After cooling from the reflow process to room temperature the resistor assembly was ramped to a uniform temperature of 334.8 K from room temperature (lines QR and ST in Fig. 8-2). This is the maximum temperature observed in the chip resistor assembly when it is powered to full load at room temperature. This resembles traditional/unpowered thermal cycling test.

Case B: In this case, a non-uniform temperature distribution was applied to the chip resistor assembly at points R and T of the thermal history, as presented in Fig. 8-3. This means that when the chip resistor is powered to its maximum load at room temperature, a non-uniform temperature distribution is developed in the assembly that is taken into account in this case. This case represents the actual temperature distribution in the assembly due to power cycling. The full temperature distribution obtained from the thermal analysis (sections 5.3.1 and 5.3.2) was used in this case.

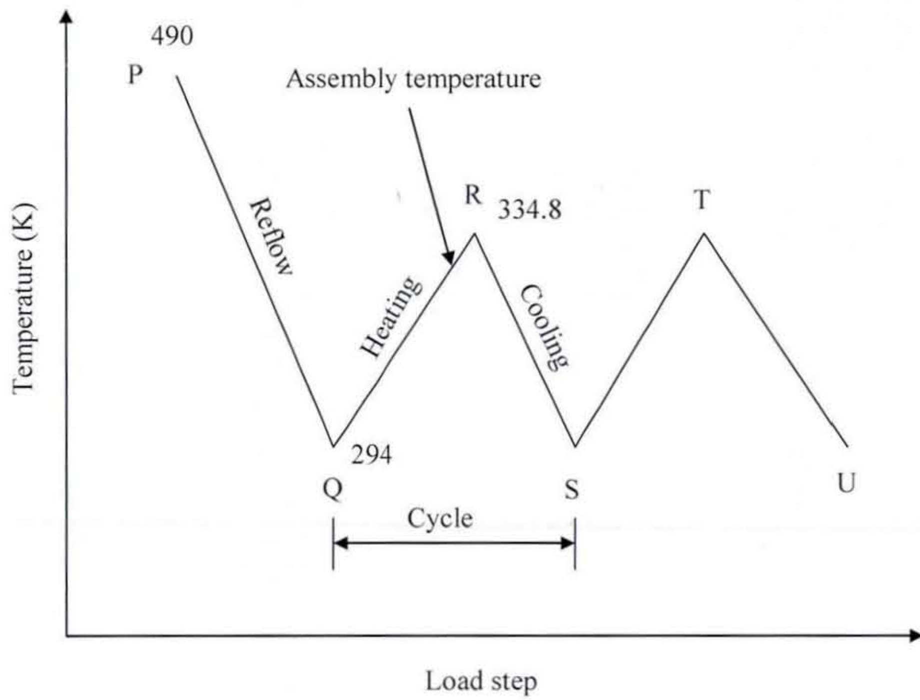


Fig. 8-2: Case A thermal history used in the elasto-plastic analysis

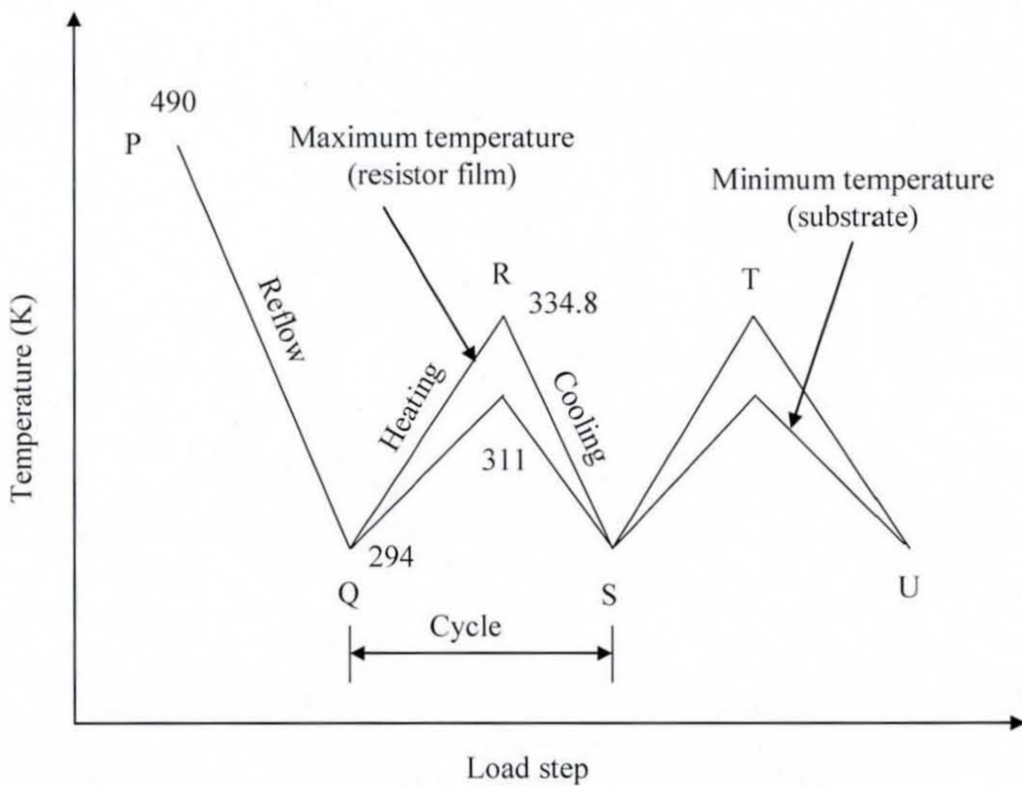


Fig. 8-3: Case B thermal history used in the elasto-plastic analysis

8.3.3 Material Properties

The chip resistor assembly consists of half the chip resistor itself, a solder joint, a copper pad and half the FR4 substrate. The chip resistor consists of several thin layers on an alumina substrate, as explained in Section 5.1.1. However, the thin layers were neglected in the simulations as these do not significantly influence the reliability of the solder joints. Therefore, the chip resistor was modelled using only the material properties of 96 % alumina, which is its substrate material. The selection of material properties for the other components of the assembly was straightforward. Properties of pure copper and FR4 were assigned to the copper pad and substrate respectively. All constituents, except the solder joint, were modelled with isotropic linear elastic material properties. Table 8-1 presents these material properties.

The solder joint was modelled using the non-linear isotropic stress-strain properties of Sn3.8Ag0.7Cu solder, ignoring the effect of voids, grains and their orientations. These properties were determined experimentally as discussed in chapter 6. As demonstrated there, the solder joint material properties are very different from those of the bulk solder. They also depend on the strain rate and it was shown that the non-linear component of the experimental stress-strain properties for the solder joint can be reproduced very well by the Johnson-Cook equation. In order to estimate the stress-strain properties for solder, the strain rate during the reflow process was calculated. In this calculation, the chip resistor assembly was assumed to be a multilayered structure with all layers the same length as shown in Fig. 8.4. Thus, the applied thermal strain on the solder joint due to the relative displacement between chip resistor and FR4 substrate can be calculated as:

$$\dot{\varepsilon}_{ts} = \Delta\dot{T}\left(\alpha_f - \alpha_{al}\right) \tag{8.7}$$

where $\dot{\varepsilon}_{ts}$ is the thermal strain rate in the solder joint, α_f is the CTE of FR4, α_{al} is the CTE of alumina and $\Delta\dot{T}$ is the cooling rate following reflow. This strain rate during cooling at a typical rate of 1.5 K/s was calculated to result in an approximate strain rate of $2.2\times10^{-5}\,\text{s}^{-1}$. Having calculated the strain rate, the required stress to produce this strain rate was calculated using the Johnson-Cook model:

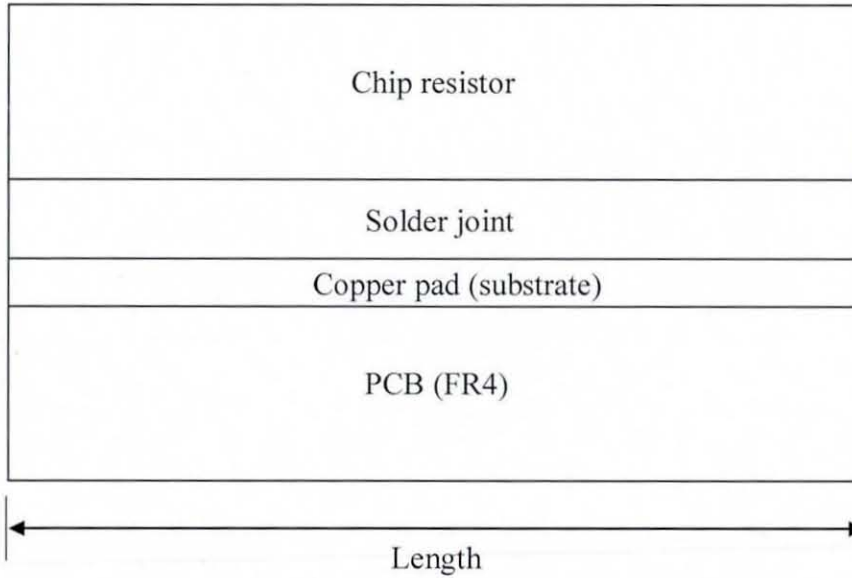


Fig. 8-4: Assumed multilayer chip resistor assembly

$$\sigma_e = (27 + 95\varepsilon_{ep}^{0.185})(1 + 0.0897 \ln \dot{\varepsilon}_{ep}^{*}) \quad 8.8$$

where ε_{ep} is equivalent plastic strain, $\dot{\varepsilon}_{ep}^{*} = \dfrac{\dot{\varepsilon}_{ep}\left(2.2\times10^{-5}\right)}{\dot{\varepsilon}_{o}\left(4.0\times10^{-3}\right)}$ is the dimensionless equivalent plastic strain rate. The Young's modulus E for this strain rate was calculated using the following relation:

$$E = 0.434 \ln(\dot{\varepsilon}) + 44.2 \quad 8.9$$

which is a fit to the Young's modulus *vs.* strain rate curve for the bulk solder. The Young's modulus for the bulk solder was used since its evaluation for the small-scale solder joints was difficult. The stress-strain curve was modelled using a multi-linear isotropic material model in ANSYS and is shown in Fig. 8-5. This elasto-plastic material model uses the von Mises yield criterion with isotropic hardening. Since the material properties of the solder joint were determined only for room temperature, any temperature dependence of its material properties was neglected. The other properties used for the solder joint are also presented in Table 8-1.

Table 8-1: Elastic material properties used in analysis [116, 134, 135]

Material	Young's modulus (GPa)	Poisson's ratio	Coefficient of thermal expansion (ppm/ °C)
Alumina	303	0.21	4.5
Copper	115	0.343	17.0
FR4	22	0.28	18.5
Solder	39.5	0.4	21.2

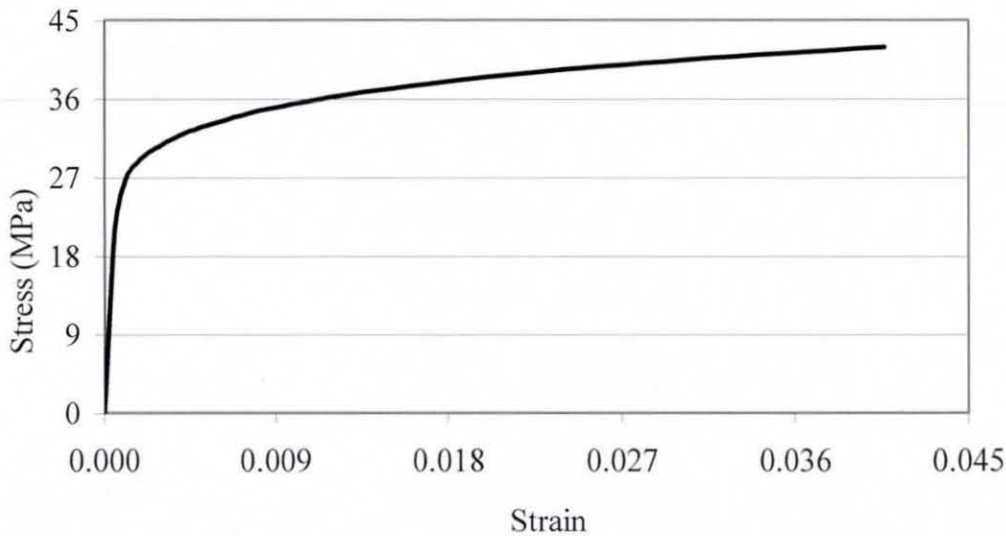


Fig. 8-5: Stress-strain curve used for the solder

8.3.4 Results and Discussion

At point P (load step 1) of the thermal history, the assembly temperature is 490 K, the melting temperature of the solder, so it is in a stress-free state. The reflow process is commonly used in surface mount soldering to create the solder joints. In this process the whole assembly passes through an oven where the maximum temperature is above the melting point of the solder alloy. Hence it is important to know the stresses induced in the solder joint due to cooling of the assembly to room temperature (line PQ in Fig. 8-2 and 8-3). When the assembly temperature decreases from the initial stress-free state to room temperature (294 K), it is subjected to thermal contraction in both translational (x and y) directions. In this process the alumina resistor body contracts less than the FR4 substrate, since it possesses a much lower CTE than the substrate resulting bending of the assembly as illustrated by the total displacement plot in Fig. 8-6. This mechanism induces primarily shear stress in the solder joint. Only

the results for the solder joint are discussed due to scope of the study and the stress levels in all of the other materials were well below their yield/fracture strength. This FE simulation of the reflow process predicts the level of residual stresses in the solder joint at its end. The distribution of both the equivalent and shear residual stresses at the end of cooling (from reflow, point Q in the thermal history) is illustrated in Fig. 8-7 (a) and (b), respectively. As shown in this figure, the maxima of both equivalent and shear residual stresses in the solder joint are at the same location at the interface between the solder joint and the chip resistor. But, the minimum stresses are at different locations on the free surface of the solder joint. The stresses at the end of the reflow can be termed as manufacturing induced stresses. The magnitude of the residual stress induced in the solder joint is above the yield stress of the Sn3.8Ag0.7Cu solder alloy at room temperature - 25 MPa. This causes plastic deformation of the solder joint due to reflow. Figures 8-7 (c) and (d) illustrate the distribution of equivalent and shear plastic strain at the end of reflow, and, as expected, the maximum plastic deformation is observed at the interface between the solder joint and chip resistor. The location of maximum stress and strain in the solder joint is the same. The von Mises transformations (Eq. 7.2 and 7.3) show the predominant contribution of shear stress and strain towards the equivalent stress and strain. This indicates the importance of shear stresses in this type of solder joint.

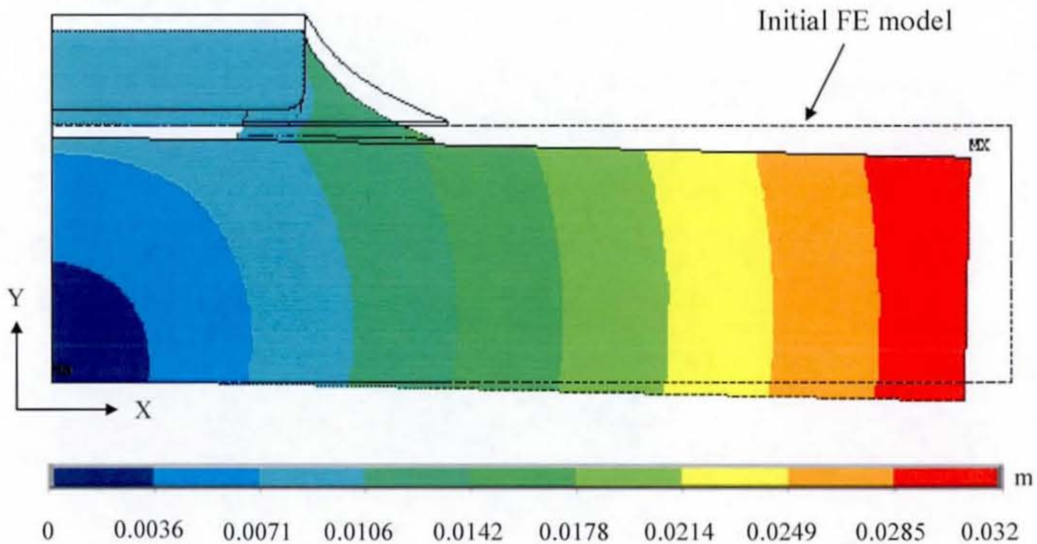


Fig. 8-6: Total displacement magnitude plot for the assembly at the end of reflow (point Q in Fig. 8-2 and 8-3)

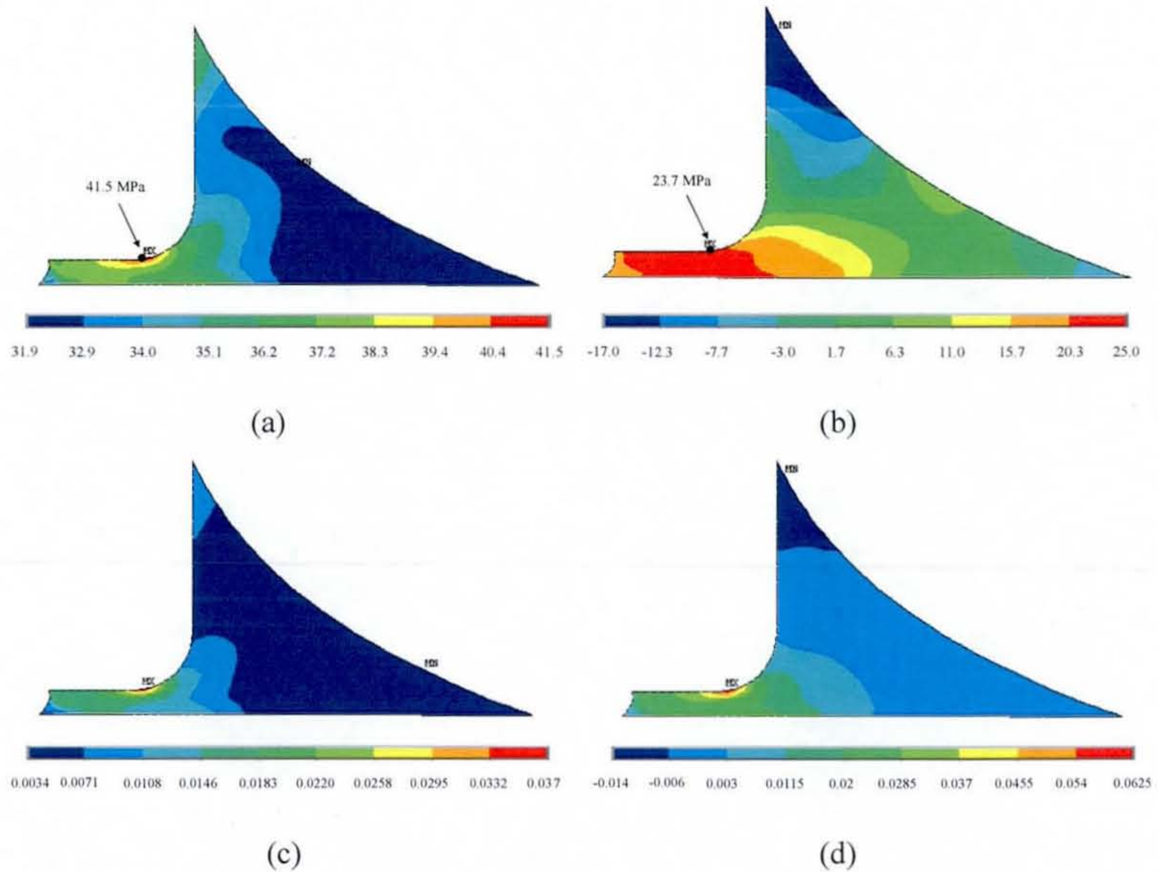


Fig. 8-7: Distribution of: (a) equivalent stress; (b) shear stress; (c) plastic equivalent strain; (d) plastic shear strain in 2D chip resistor assembly

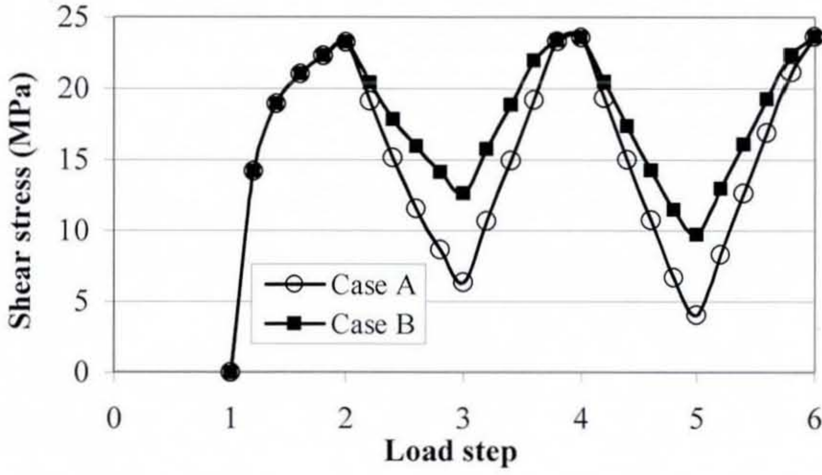
The evolution of stress and strain in the solder joint was studied considering the shear component as it is the major contributor. Figures 8-8 (a) and (b) illustrates the evolution of both shear stress and total shear strain, respectively throughout the whole of the loading sequence. The total shear strain is a summation of elastic and plastic shear strains. The maximum stress location, which is also the location of maximum strain, in the solder joint was considered for this study. This location also provides the maximum strain range for a stabilised cycle during cyclic thermal loading and therefore in the worst location for thermo-mechanical fatigue life estimation. As explained, point P (load step 1) is the stress-free state, and the induced shear stress increases as the temperature of the assembly decreases to room temperature (point Q, load step 2). Hereafter the assembly is subjected to the temperature cycles hence the fluctuation in the shear stress which is observed. The shear stress range during the two successive cycles after the reflow process was about the same. It is evident from Fig. 8-8 (b) that a significant plastic shear strain is induced during reflow soldering.

Significantly less plastic strain (less than 0.3%) was observed in each of the successive cycles compared to that observed at the end of reflow, indicating that the solder joint experiences little further plastic deformation during temperature cycling.

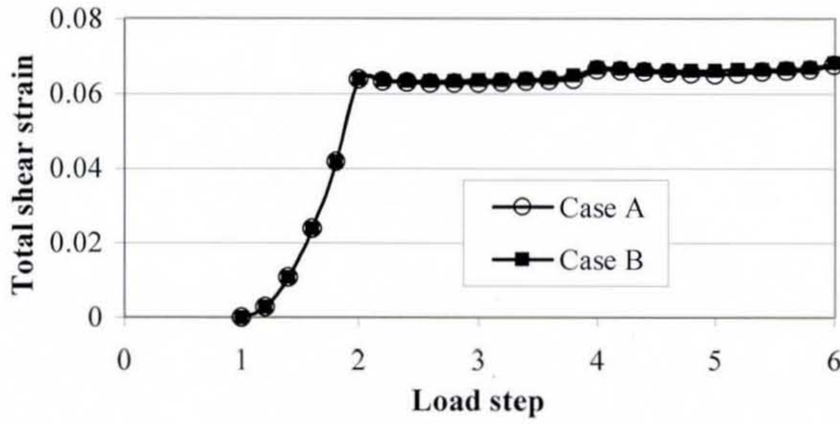
Figures 8-8 (a) and (b) also provide a comparison of evolution of shear stress and total shear strain, respectively, between Case A (unpowered) and Case B (powered) types of accounting for thermal conditions within the same thermal history. The evolution of the total shear strain is very much the same for both load cases. However, the shear stress evolution for Case A and Case B is rather different. As the thermal conditions approach point R or T, the differences between the shear stresses become prominent. In Case A, the whole assembly is at 334.8 K, unlike Case B, where the spatial temperature gradient is considered at point R (load step 3) or point T (load step 5). Due to the higher uniform temperature distribution in Case A, the relaxation of the assembly is higher from its plastically deformed state (point Q), which results in a greater reduction in the residual shear stress than is observed in Case B. The amount of the residual stress decrease in Case A is about 35 % greater than for Case B.

2D and 3D result comparison

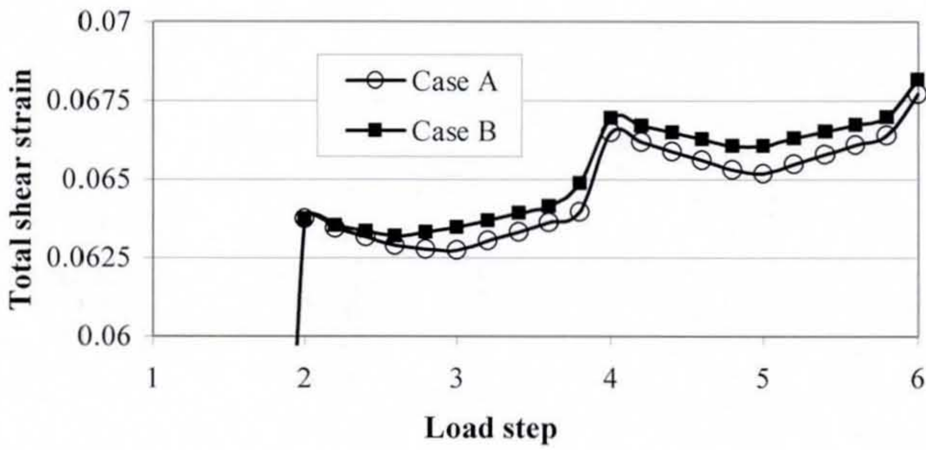
The elasto-plastic analysis for the chip resistor assembly was also carried out for the 3D mesh. Figures 8.9 (a) and (b) show the distribution of shear stress and plastic shear strain, respectively, in the 3D solder joint at the end of the reflow. The shear stress and strain distribution patterns are practically the same as those observed for the 2D model with the maximum magnitude observed in the same location (the interface between solder joint and chip resistor). A comparison of the evolution of shear stress and total shear strain in the 2D and 3D models made for the maximum shear stress location in the 2D model and the same location in the 3D model which is shown in Fig. 8-9 (a). These are illustrated in Figs. 8-10 (a) and (b). For Case B, this comparison demonstrates that the predicted stress in the 3D model is slightly higher than for the 2D model. The shear stress distributions in both models are nearly the same at R or T, as illustrated by Fig. 8-11, with difference of 3.1MPa at the same location between them.



(a)



(b)



(c)

Fig. 8-8: Evolution of: (a) shear stress; (b) total shear strain; (c) total shear strain on a bigger scale in the 2D chip resistor simulation

Comparison of the total shear strain evolution for the 2D and 3D models shows similar differences to those for the shear stresses. Due to slightly higher stress levels in the 3D solder joint model, the total shear strain prediction is also higher. The difference in predicted total shear strain between 2D and 3D models is about 10 % throughout the thermal history. As was also observed in the 2D analysis, hardly any plastic deformation was observed during the two successive temperature cycles in the 3D analysis. Thus, both models illustrate that the reflow process induces almost the entire plastic deformation taking place in the solder joint at the end of the analysis.

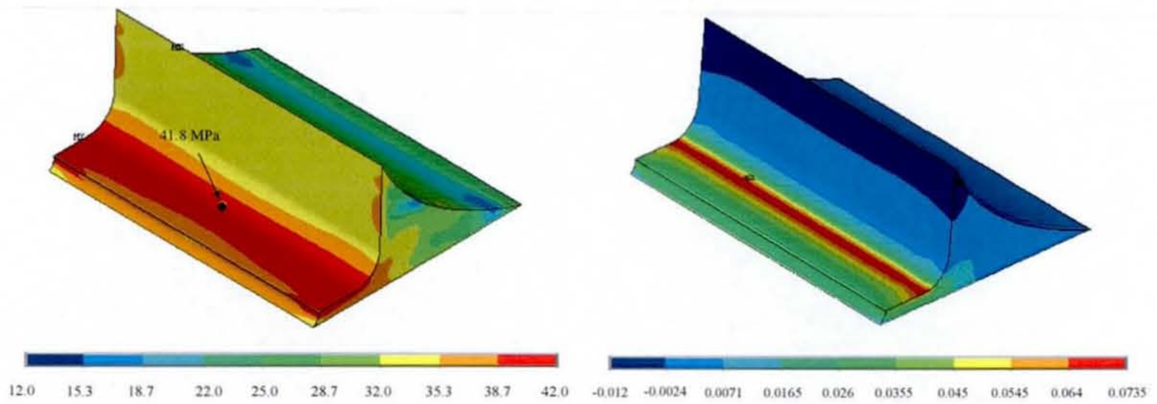
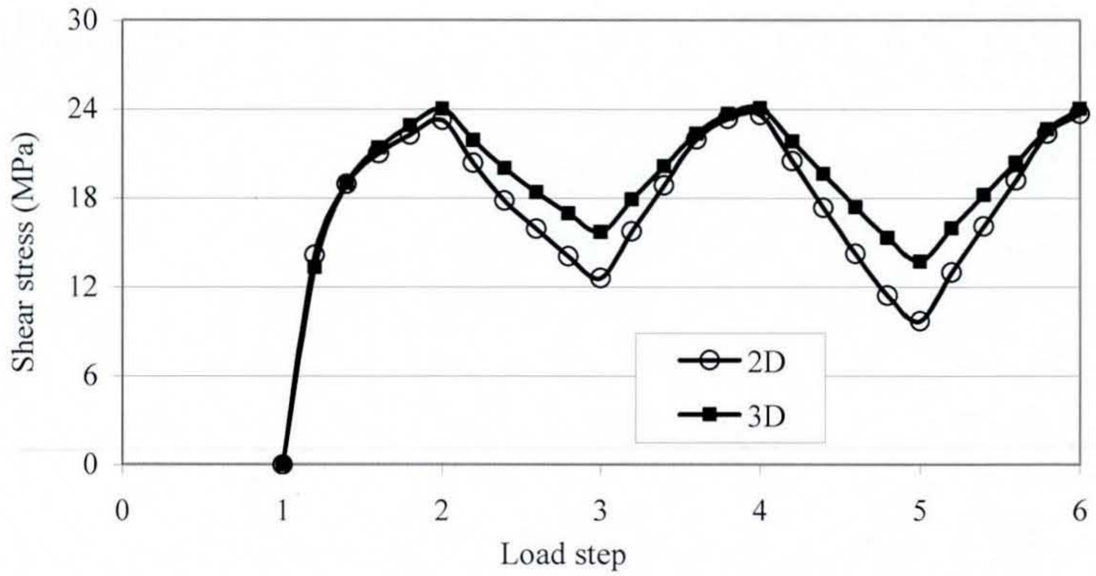
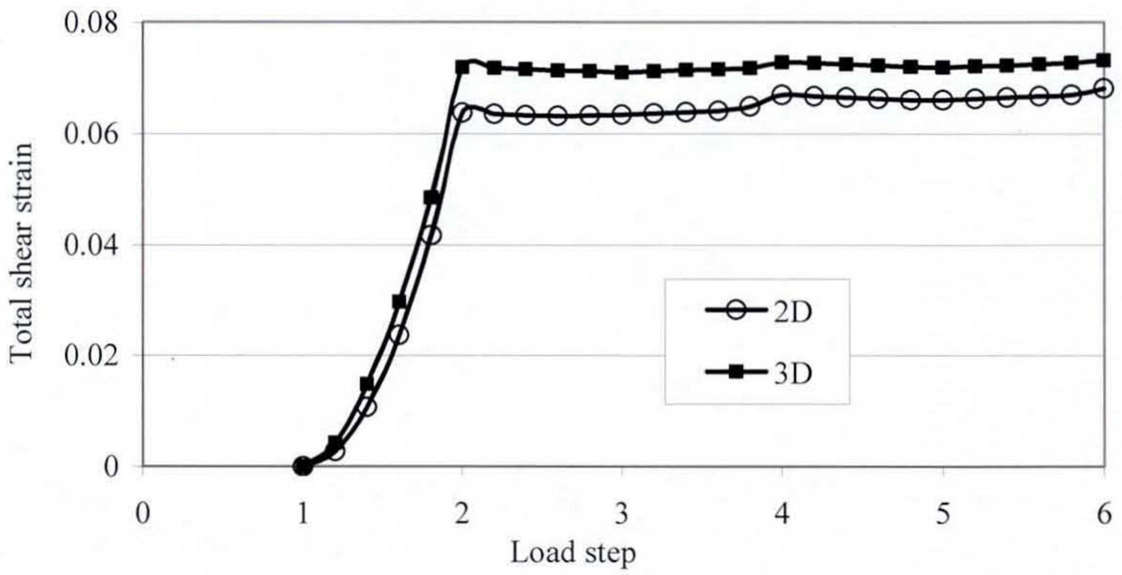


Fig. 8-9: Distribution of: (a) shear stress; and (b) plastic shear strain in the solder joint at point R of thermal history for 3D simulation

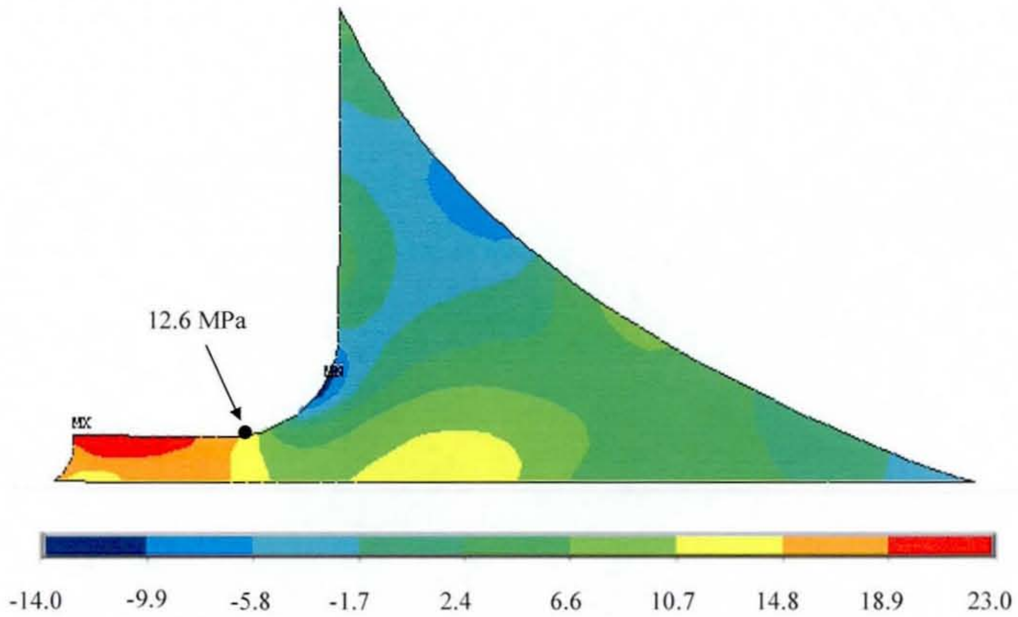


(a)

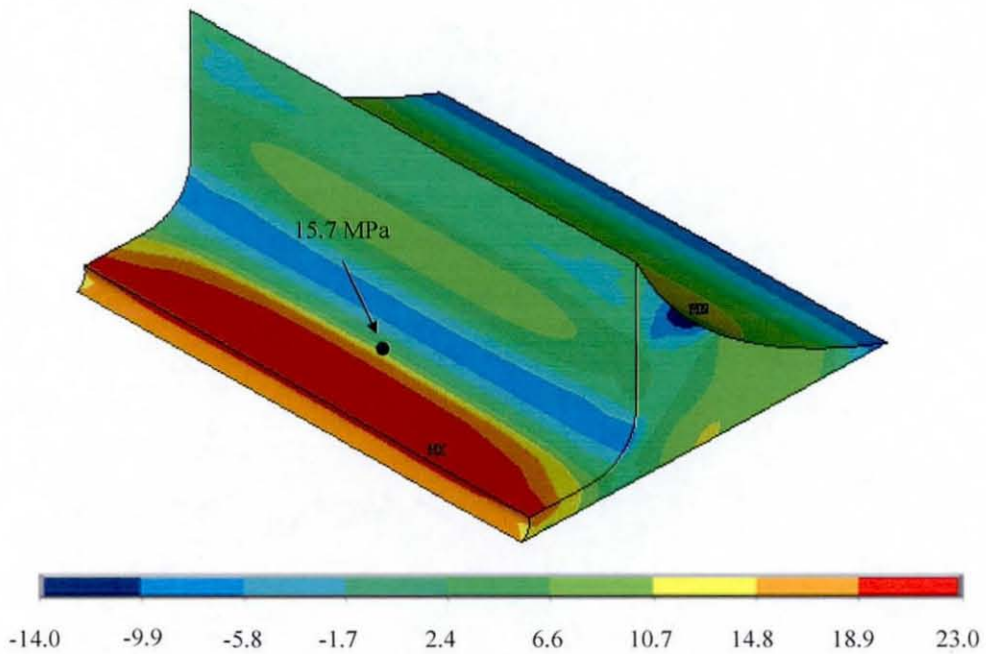


(b)

Fig. 8-10: (a) Comparison of shear stress; (b) total shear strain for the 2D and 3D chip resistor models



(a)



(b)

Fig. 8-11: Distribution of shear stress in the solder joint at the end of third load step (point R in Fig. 8-2 and 8-3) of thermal history for: (a) 2D model; (b) 3D model

Conclusions

The elasto-plastic analysis of the chip resistor assembly shows that a high level of residual stresses and strains are induced in the solder joint due to reflow soldering. It can cause significant plastic deformation of the solder joint. An important observation from the elasto-plastic analysis was that the solder joint was subjected to much smaller plastic deformations during the simulated temperature cycling after the reflow process. This indicates that the thermal history used in the simulation after the reflow process is not inducing stress levels in the solder joint which exceed the new yield stress of the solder material. The similar stress and strain predictions from the 2D and 3D models suggest that the problem can be adequately simulated using the 2D plane-strain element formulation and that the variation of temperature in the thickness direction (Z-direction) does not significantly alter the stress and strain pattern in the solder joint. Since solder alloys generally operate under conditions where significant creep is anticipated, further analysis of the chip resistor assembly was carried out using the 2D plane-strain formulation considering and including creep as well as plastic behaviour in the solder joint.

8.4 Creep Analysis

In order to achieve a more detailed understanding of the solder joint long term structural integrity, creep analysis of the 2D chip resistor assembly was carried out. The geometry used for this simulation was the one used in the previous elasto-plastic analysis, and the boundary conditions remained the same as explained in section 8.3.1. Inclusion of creep properties for the solder joint was the only addition to the previously described elasto-plastic model. Creep analysis of the resistor assembly was carried out for two different ambient conditions: one for power dissipation at room temperature and another for constant power dissipation within a varying ambient temperature. Each creep analysis consists of two thermal load cases. One load case represents the traditional thermal cycling test wherein an uniform temperature distribution is applied over the assembly, whilst the other load case represents the actual non-uniform temperature distribution. The comparison of the results of these two cases helps evaluate the effect of non-uniform temperature distributions on fatigue damage to solder joints. The details of these thermal cases are discussed in their respective sections.

8.4.1 Creep Material Properties

In the chip resistor model, only the solder joint is given creep deformation properties in addition to its elasto-plastic material properties. Thus, both plastic and creep behaviour in the solder joint were simultaneously modelled in the same simulation. The elasto-plastic material properties of the solder joint used in the FE analysis were discussed in Section 8.3.3. In the same section, the material properties of the other constituents of the chip resistor assembly were also presented. It is a common practice to characterise the creep response of solder joints solely with a steady-state constitutive equation. The frequently used equation for the steady-state creep rate of solder is a hyperbolic sine law, and it was demonstrated in the previous chapter that this creep law is a very good fit to the experimentally obtained steady-state strain rate. As discussed in section 7.5, the creep behaviour of the solder joint is different for tensile and shear loads. Thus, two creep models have been identified that represents the two extreme creep behaviours of the solder: one for highest creep strength (tensile creep data for the strongest small-scale solder joints), called creep model 1 and the other for the lowest creep strength (shear creep data for the weakest small-scale solder joints), called creep model 2. Creep model 1 is:

$$\dot{\varepsilon}_s = 1.64 \times 10^4 \left[\sinh 0.089\sigma\right]^{4.9} \exp\left(\frac{-8772}{T}\right) \qquad 8.10$$

and creep model 2 is:

$$\dot{\varepsilon}_s = 9.47 \times 10^8 \left[\sinh 0.104\sigma\right]^{1.6} \exp\left(\frac{-8772}{T}\right) \qquad 8.11$$

The hyperbolic sine creep model is readily available in ANSYS and the relevant parameters used are presented in Table 8-2. These parameters were established using a non-linear curve fitting method to the experimentally obtained steady-state creep data, which was discussed in chapter 7. The solder joint was assumed to be void free and isotropic.

Table 8-2: Hyperbolic sine creep model parameters used in the ANSYS simulations

Parameter	Definition	Value	
		Creep model 1	Creep model 2
C1 (s^{-1})	Constant (B_l)	1.64×10^{4}	9.47×10^{8}
C2 (MPa^{-1})	Stress multiplier (β)	0.089	0.104
C3	Stress exponent (p)	4.9	1.6
C4 (K^{-1})	Ratio Q/R	8772	8772

8.4.2 Creep Study for Power Dissipation Cycles at Room Temperature

This section presents the creep studies carried out for the same chip resistor assembly used previously in the elasto-plastic analysis for power dissipation at room temperature. These simulations are representative of power cycling at room temperature with the objective of demonstrating the effect of the non-uniform temperature distribution in the resistor assembly when it is powered on the solder joint fatigue life. Therefore, as discussed in section 8.3.2, two thermal load cases were considered in the creep study and these are discussed below.

8.4.2.1 Thermal History

Specification of the thermal history is critical for creep analysis since creep is the process of inelastic accrual of strain with respect to time under sustained loading. The thermal history applied was the same as that used in the elasto-plastic analysis, but with the consideration of time i.e. dwell duration at temperature extremes and a controlled rate of change of temperature. Two different ways of accounting for the temperature distribution in the chip resistor assembly were considered, Case A and Case B. The thermal histories used in Case A and Case B are shown in Fig. 8-12 (a) and (b) respectively, while Fig. 8-12 (c) illustrates the power condition used to obtain the temperature distribution in the chip resistor for Case B. Details of the thermal history are presented in Table 8-3. It consists of cooling from reflow, a one hour dwell at room temperature for stress relaxation to occur and then a temperature cycle. The cooling rate was 1.5 K/s whilst the ramps to the hot and cold dwell was based on the experimental measurement. The dwell times at temperature extremes were decided

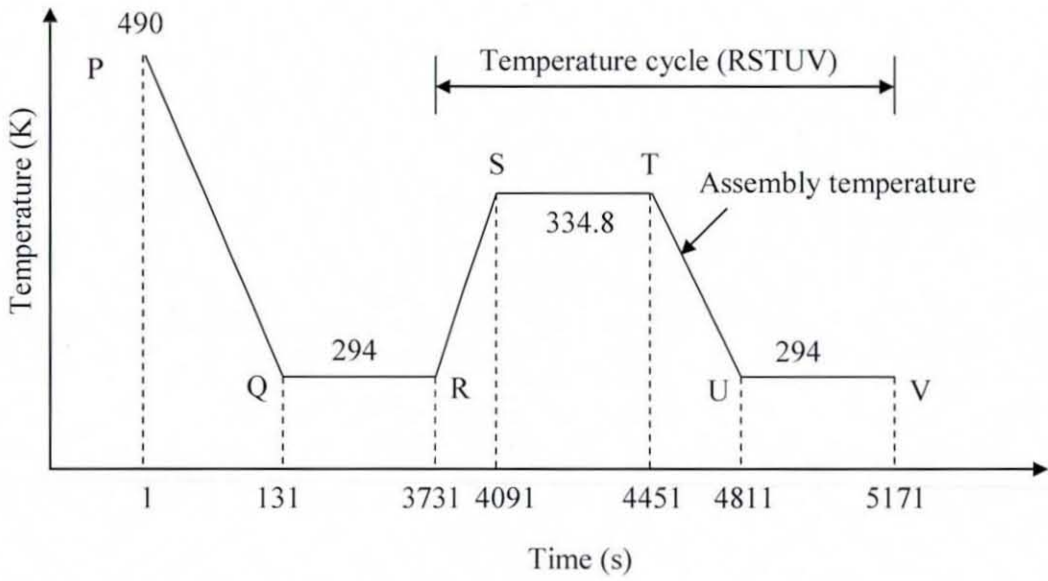
based on the temperature cycling studies carried out by other researchers [48, 80]. The two different ways of applying the temperature boundary conditions are discussed in more detail below:

Case A: This case is similar to Case A in the elasto-plastic analyses, but with the addition of ramps and dwells as detailed in Table 8-3. In this case, a spatially uniform temperature distribution was assumed for the entire resistor assembly during the hot dwell (line ST in Fig. 8-12 (a)) of the thermal history. During this dwell the entire chip resistor assembly was at 334.8 K. This is the maximum temperature observed in the chip resistor assembly when it was powered at full rated load at room temperature. This case represents the generally used idealisation of temperature cycling with a uniform temperature and thus resembles typical thermal cycling tests.

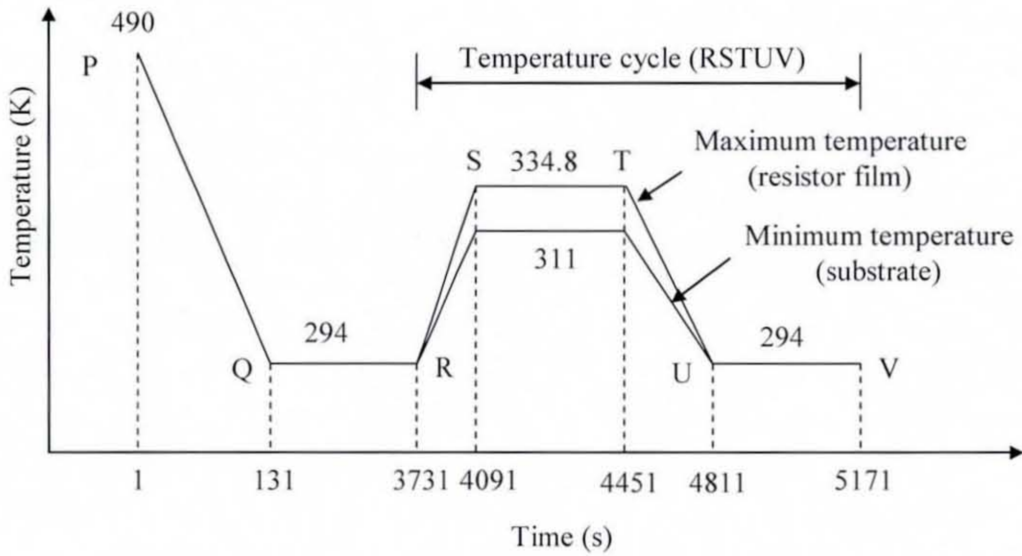
Case B: This load case is also similar to Case B in the elasto-plastic analyses. In this case a non-uniform spatial temperature distribution was progressively applied to the chip resistor assembly, as the temperature rose from room temperature to the hot dwell (line ST in Fig. 8-12 (b)) phase of the temperature cycle. Thus, Case B accounts for the actual non-uniform temperature distribution observed in the chip resistor assembly when it is powered at room temperature to its maximum load and represents power cycling at room temperature. The full temperature distribution obtained from the 2D thermal analysis of the chip resistor assembly at room temperature (as discussed in Section 5.3.1) was used.

Table 8-3: Details of the thermal history specified for the creep analysis

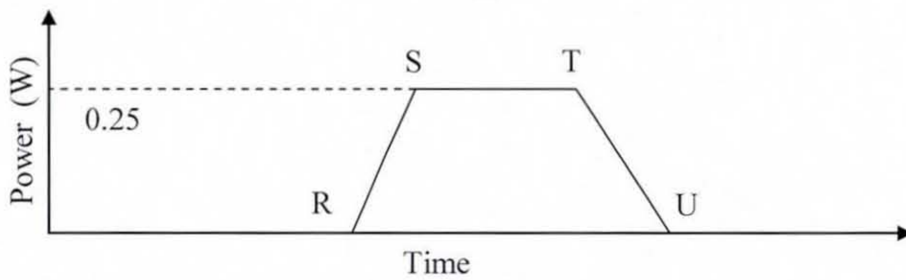
History step	Duration
Reflow process (PQ)	130 seconds
Dwell at room temperature (QR)	3600 seconds
Ramp to hot dwell (RS)	360 seconds
Hot dwell (ST)	360 seconds
Ramp to cold dwell (TU)	360 seconds
Cold dwell (UV)	360 seconds



(a)



(b)



(c)

Fig. 8-12: Thermal histories used for the creep simulation of power cycling at room temperature: (a) case A; (b) case B; (c) power dissipation

8.4.2.2 Results and Discussion

Creep Model 1

In this section the simulation results obtained when using the creep model 1 parameters (Eq. 8.10)) are discussed. In the finite element analysis, the chip resistor was subjected to 10 full temperature cycles after the post reflow dwell i.e. repetitions of the temperature cycle RSTUV in Figs. 8-12 (a) and (b). The stress and strain results from this simulation are presented only for the solder joint, since it is the principal area of interest in this work. Equivalent and shear thermal stresses in the solder joint were studied at the end of reflow and those stress distributions are illustrated in Fig. 8-13. As explained in the elasto-plastic analysis, shear stress is predominant in the solder joint and it contributes to most of the equivalent stress. The inclusion of creep properties resulted in a 3 MPa reduction of residual stress levels in the solder joint. The maximum and minimum stresses for both the equivalent and shear stress are observed at the same locations as those observed in the elasto-plastic analysis. Again the magnitude of the residual stress induced in the solder joint is above the initial yield stress of the Sn3.8Ag0.7Cu solder alloy at room temperature - 25 MPa. This causes plastic deformation of the solder joint during cooling from reflow temperatures.

As explained, shear stress is the dominant stress component and its evolution for both thermal load cases was studied at the maximum shear stress location in the solder joint. The shear stress evolution during the post reflow cooling, the dwell at room temperature, and the successive 10 temperature cycles is illustrated in Fig. 8-14. It demonstrates that the induced stress at the end of reflow diminishes by about 20 % due to creep relaxation during the dwell at room temperature. Its evolution is the same for both load cases until the end of the room temperature dwell, due to the thermal history being identical up to this point. The stress variations during the temperature cycle for both load cases are also similar. However, the stress range for Case A is higher than for Case B, due to the more rapid stress relaxation in the assembly during the hot dwell. The difference in the relaxation between Cases A and B is evident from the comparison of shear stress distributions at the beginning of the hot dwell (point S in Fig. 8-12 (a) and (b)) which is illustrated in Fig. 8-15 where lower stress levels are observed for Case A. Figure 8-14 also demonstrates that the distribution of stresses in the solder joint is similar during the cold dwells. It is also clear from the stress evolution results presented in Table 8-4 that the stress range has almost stabilised after

the 8th cycle. It can also be observed from the shear stress evolution that the maximum stress in the temperature cycles does not exceed maximum stress achieved in the first temperature cycle which is the same as the maximum residual stress. This indicates that after the first temperature cycle there is no further plastic deformation in the solder joint during successive temperature cycles and hence all of the irreversible deformation is only the result of creep.

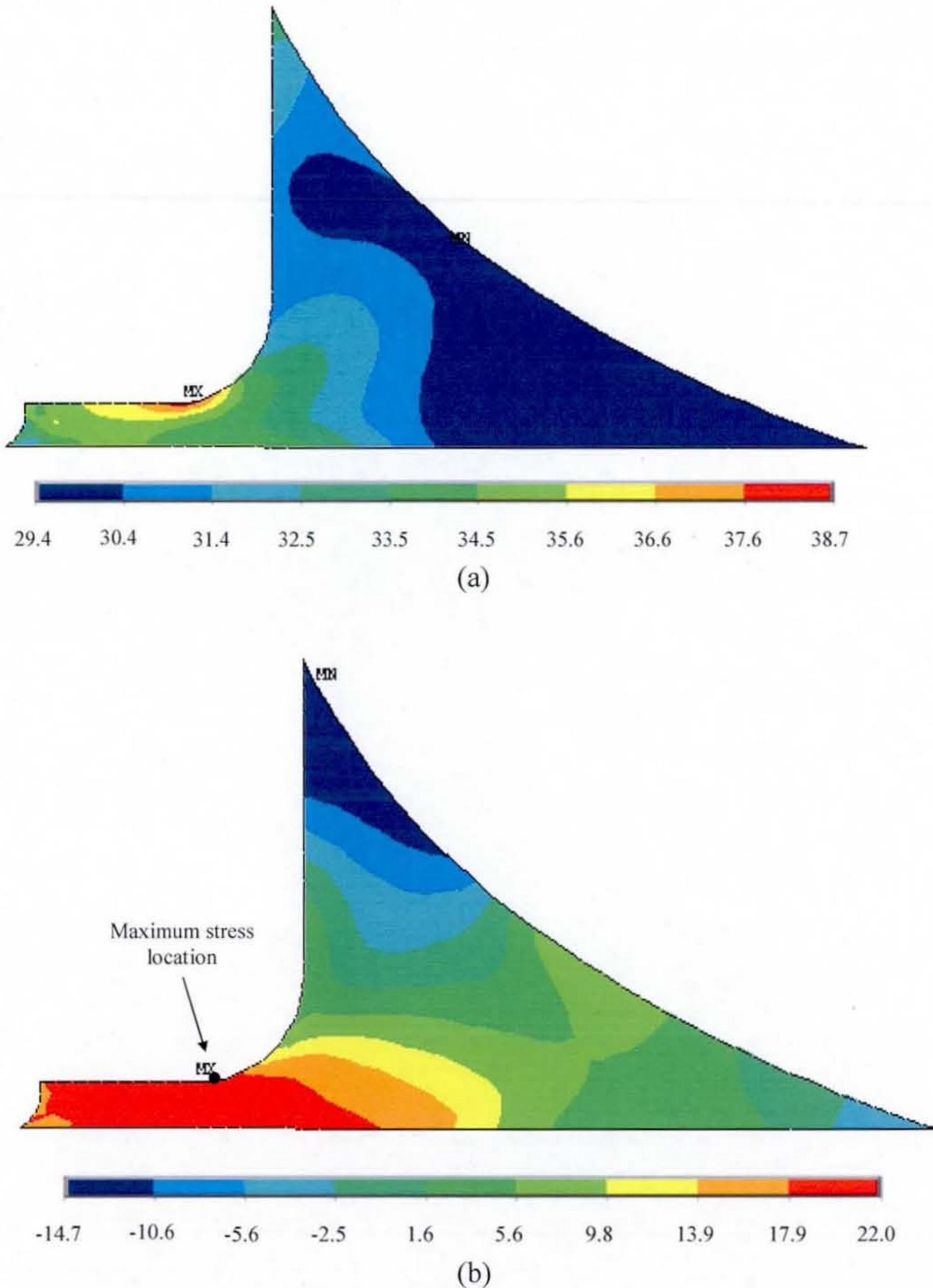


Fig. 8-13: Distribution of: (a) equivalent; (b) shear thermal stress (MPa) in the solder joint at the end of reflow (point Q in Fig. 8-12)

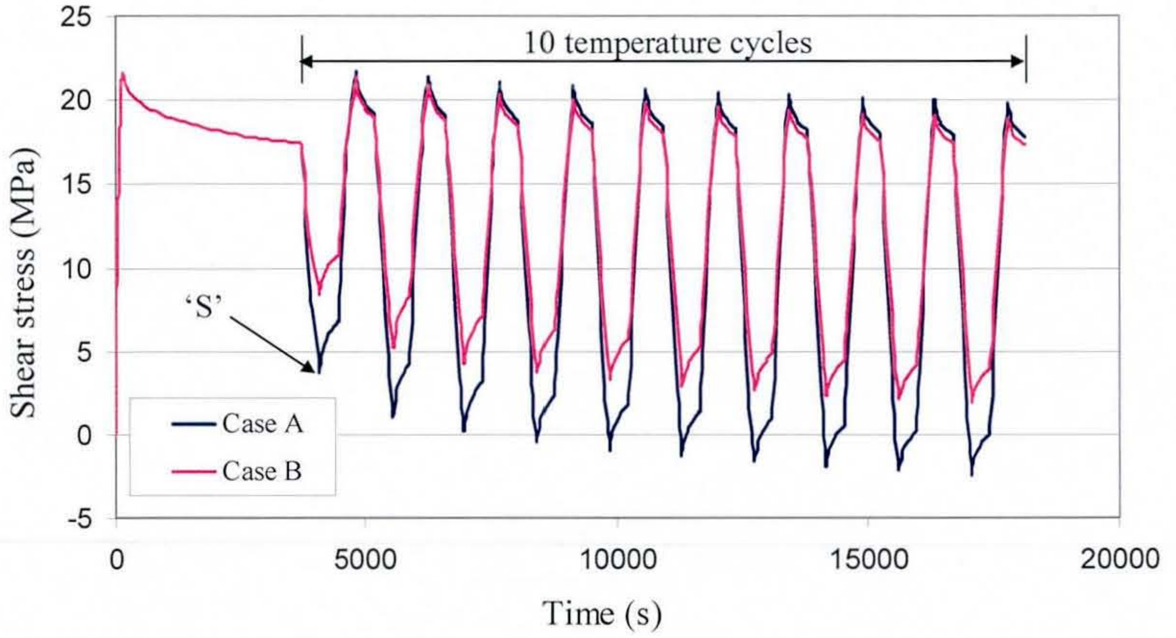


Fig. 8-14: Evolution of shear stress in the solder joint for creep model 1

Table 8-4: Stress range in the solder joint with creep model 1
and power dissipation cycling at room temperature

Cycle	Case A	Case B
	Shear stress range	Shear stress range
1	18.0	13.0
2	20.3	15.6
3	21.0	16.1
4	21.4	16.3
5	21.6	16.4
6	21.8	16.7
7	22.0	16.8
8	22.1	16.9
9	22.2	17.0
10	22.2	17.0

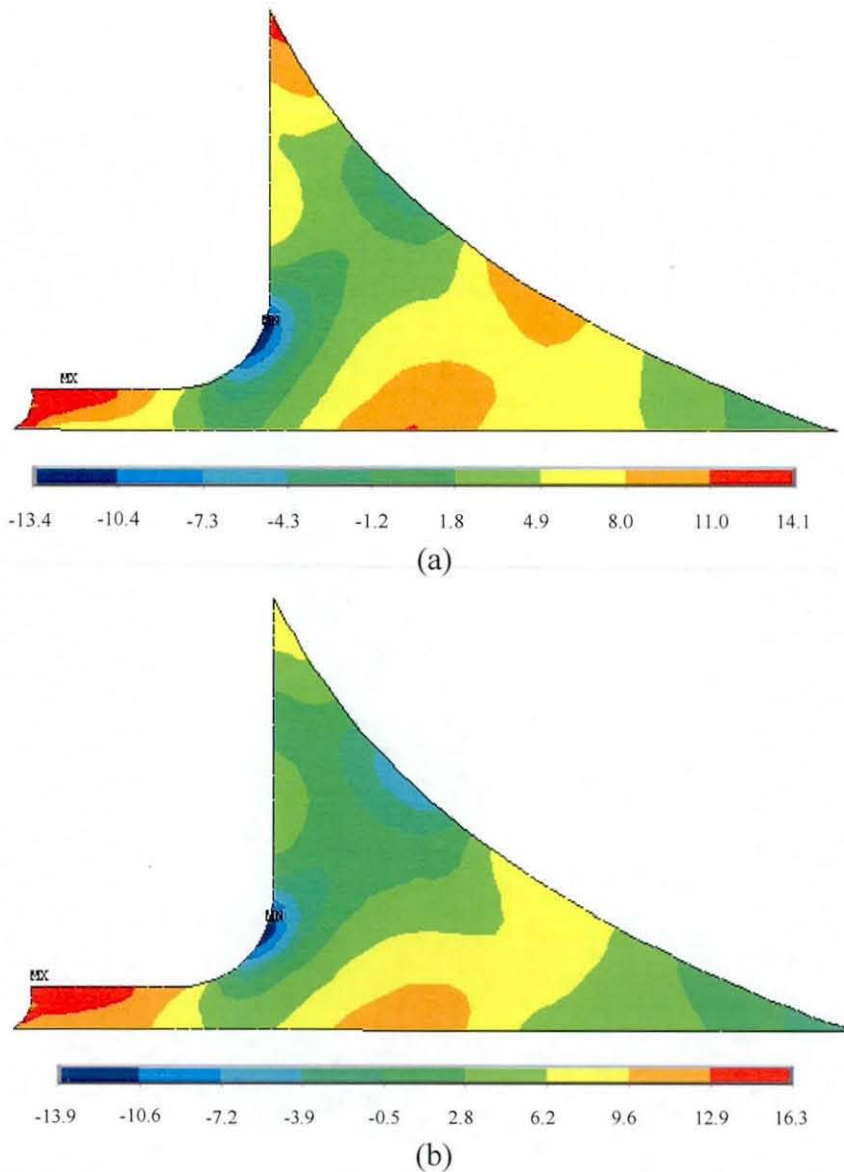


Fig. 8-15: Distribution of shear stress in the solder joint at the beginning of the first hot dwell: (a) Case A; (b) Case B

The evolution of accumulated inelastic strain in the solder joint was also studied for the entire thermal history. The total inelastic (plastic) strain is the sum of strains due to both plasticity and creep. Since the stress level induced in the solder joint at the end of reflow is in the plastic region, inelastic strain occurs. At the same time, time dependent deformation in the solder joint, due to creep, also contributes to the permanent strain. However, as explained earlier after the end of reflow, any further inelastic strain deformation in the solder joint is mainly due to creep. Figure 8-16 shows the evolution of accumulated inelastic strain at its maximum location, which is the maximum stress

location, in the solder joint for cases A and B. As expected, the accumulated inelastic (plastic) strain at the end of 10 temperature cycles is greater for Case A, due to its wider temperature cycling range. The reflow simulation contributed 59 % and 63 % of the total accumulated inelastic strain respectively for cases A and B, with the remainder due to the room temperature dwell and 10 temperature cycles. Each temperature cycle after the room temperature dwell results in an incremental increase in the levels of inelastic strain, which becomes constant after few cycles. The accumulation of inelastic strain for each temperature cycle was compared between Cases A and B, and is presented in Table 8-5. It decreases as the temperature cycle progresses, stabilising after 8 cycles. The stabilised cyclic inelastic strain is 45 % higher for Case A than for Case B, which is the effect of the non-uniform temperature distribution in the assembly during the hot dwell periods. This difference in stabilised inelastic strain range has a direct implication for the fatigue life of the solder joint, which is discussed later.

Table 8-5: Predicted inelastic strain range in the solder joint for power dissipation at room temperature for creep model 1

Cycle	Inelastic strain range	
	Case A	Case B
1	0.0039	0.0039
2	0.0029	0.0024
3	0.0025	0.0020
4	0.0022	0.0017
5	0.0020	0.0015
6	0.0019	0.0014
7	0.0018	0.0013
8	0.0017	0.0012
9	0.0016	0.0011
10	0.0016	0.0011

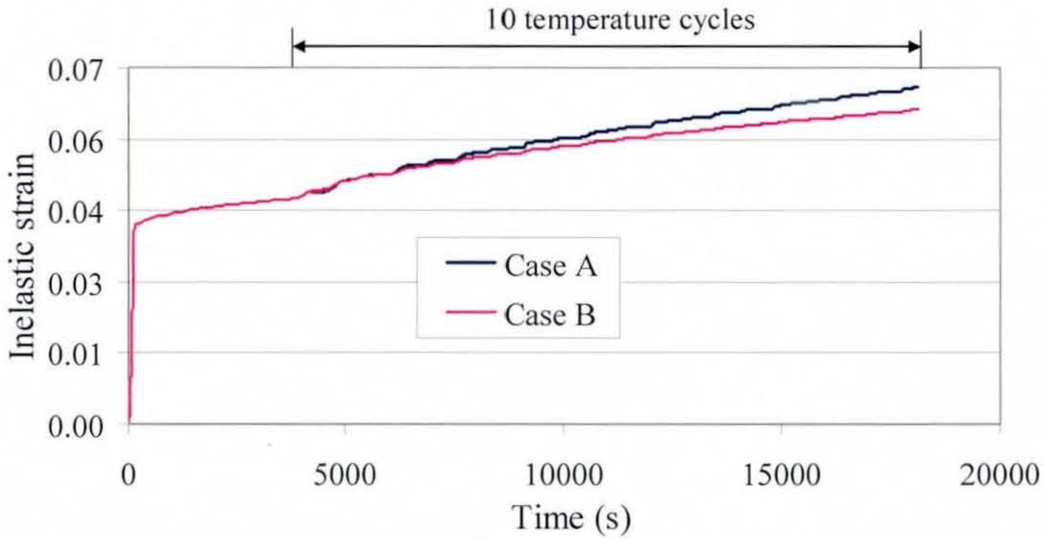
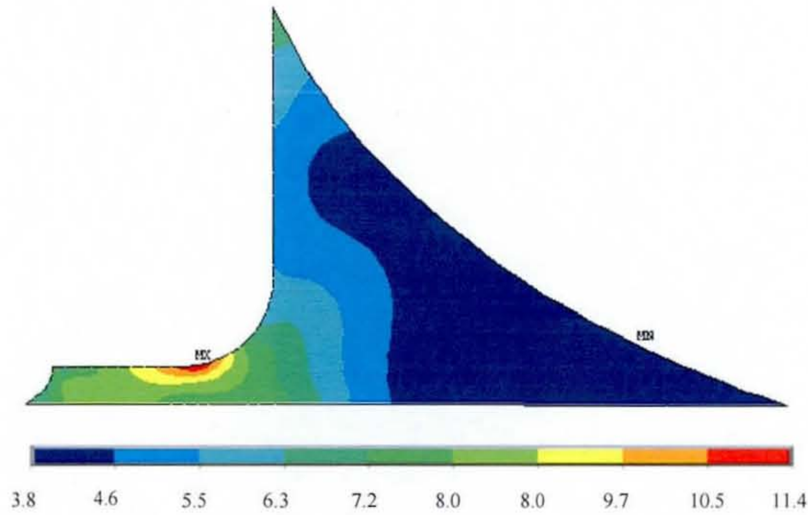


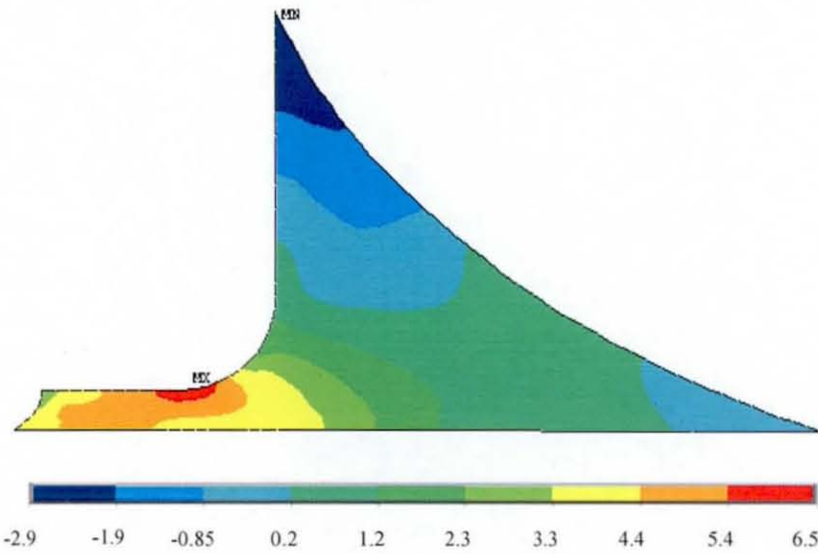
Fig. 8-16: Evolution of accumulated inelastic shear strain at the maximum stress location in the solder joint for creep model 1

Creep Model 2

In this finite element creep analysis of the chip resistor assembly, the solder joint was modelled using creep model 2 (Eq. (8.11)). The creep analysis again included 10 temperature cycles following the reflow process and dwell at room temperature. A study of stress and strain distributions and their evolution in the solder joint was performed, as for the previous creep analysis. The distribution of the equivalent and shear stress in the solder joint at the end of reflow is illustrated in Fig. 8-17. The distribution of both equivalent and shear stress is similar to that observed for creep model 1, with the maximum stress occurring at the same location in the solder joint as for model 1. However, the absolute levels of stress in the solder joint are lower due to the more rapid creep relaxation than in the previous creep model. These lower stress levels are well below the yield strength of the solder joint, and hence there was no plastic deformations due to cooling from reflow.



(a)



(b)

Fig. 8-17: Distribution of: (a) equivalent; (b) shear thermal stress in the solder joint at the end of reflow (point Q in Fig. 8-12)

As expected, shear stress is the dominant stress component in this creep analysis as for creep model 1, and its evolution for both thermal Cases A and B at the maximum stress location in the solder joint was studied. Figure 8-18 shows the evolution of shear stress for reflow, the dwell at room temperature and the 10 temperature cycles for both thermal cases. The more rapid creep relaxation at room temperature results in a greater decrease in the residual stresses, and as a result the solder joint is almost in a stress-free state, which is evident from Fig. 8-18. The shear stress evolution is the same for cases A and B until the end of the room temperature dwell, and the stress cycles during

the following temperature cycles were also similar. The shear stress range for Case A is marginally higher than that for Case B, due to the greater stress relaxation of the assembly at Case A's higher temperatures. The stress range for each cycle is constant for both cases throughout temperature cycling.

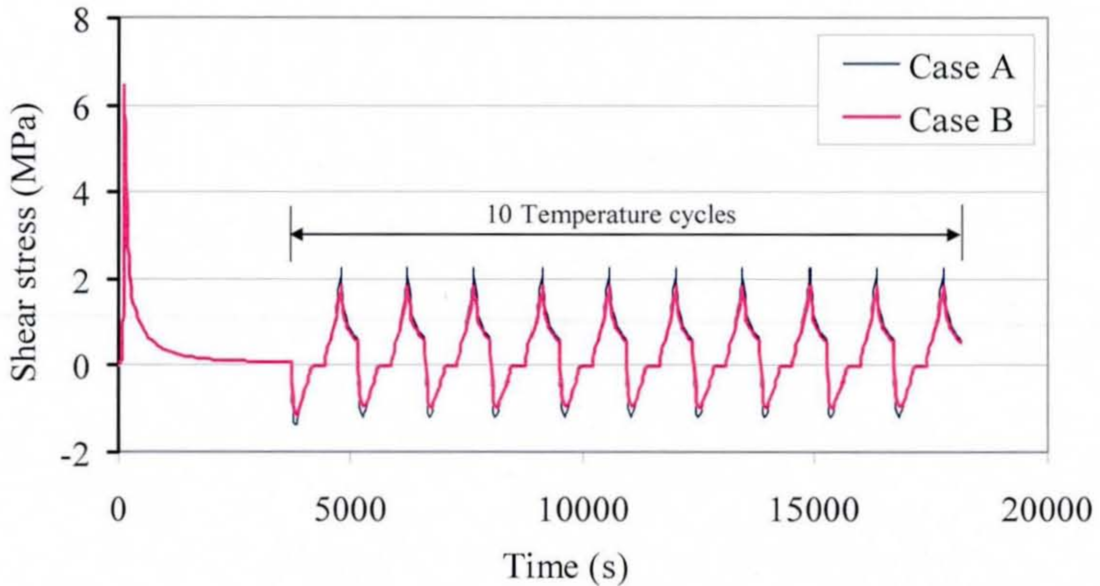


Fig. 8-18: Evolution of shear stress in the solder joint for power cycling at room temperature for creep model 2

The evolution of accumulated inelastic strain in the solder joint was again compared between cases A and B, and is shown in Fig. 8-19. In this creep analysis there was no plastic deformation observed because throughout the simulation the stress levels in the solder joint remained below its yield strength. Therefore, all of the inelastic strain in the solder joint was due to creep, unlike the previous creep model 1 simulations. The reflow simulation resulted in 18 % and 23 % of the total accumulated inelastic strain for case A and B respectively. As for creep model 1, the repeated temperature cycles resulted in incremental increase in inelastic strain. The accumulated inelastic (permanent) strain at the end of 10 temperature cycles is greatest for Case A, due to its higher temperatures. The inelastic strain for each temperature cycle is presented in Table 8-6 and it shows that the strain range stabilises after the first cycle for both cases. Again, the stabilised creep strain range is 45 % higher for Case A compared to Case B, which is the effect of the non-uniform temperature distribution in the assembly during the hot dwell periods. This difference in the stabilised inelastic strain has direct implications for the fatigue life of the solder joint. Knowing the stabilised

inelastic strain, the number of temperature cycles for achieving the inelastic strain resulted due to reflow was calculated to be 2 and 3 for cases A and B, respectively. The comparison of stabilised inelastic strain between creep models 1 and 2 illustrates the importance of the creep model used. Creep model 2, which represents the lowest creep resistance offered by the solder joints tested under shear load, resulted in the higher stabilised inelastic strain range. Its implications for the solder joint fatigue life are discussed in the following section.

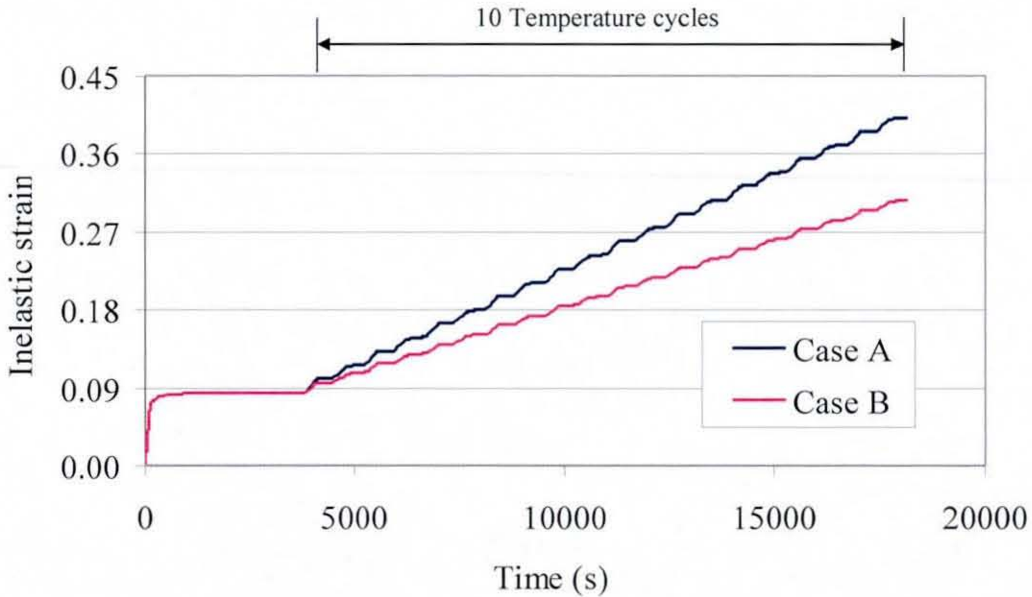


Fig. 8-19: Evolution of inelastic strain in the solder joint for power dissipation at room temperature for creep model 2

Table 8-6: Predicted inelastic strain in the solder joint for power dissipation at room temperature for creep model 2

Cycle	Inelastic strain range:	
	Case A	Case B
1	0.0331	0.0233
2	0.0319	0.0220
3	0.0319	0.0220
4	0.0319	0.0220
5	0.0319	0.0220
6	0.0319	0.0220
7	0.0319	0.0220
8	0.0319	0.0220
9	0.0319	0.0220
10	0.0319	0.0220

Fatigue Life Estimation

There are two parts in the estimation of fatigue life. These are: estimation of fatigue life consumed by reflow before temperature cycling and fatigue life estimation of post reflow thermal cycling. The life consumed by reflow was calculated considering the inelastic strain from the stabilised cycle. Thus the calculated fatigue life for both the creep models 1 and 2 are presented in Tables 7 and 8 respectively. In case of creep model 1, 24 and 36 thermal cycles were consumed by the reflow respectively for Cases A and B thermal conditions. However, with creep model 2 it is just 2 and 3 cycles for Cases A and B respectively.

As discussed in chapter 4, estimation of the fatigue life of solder joint for post reflow thermal cycles may be based on the strain range or strain energy calculated for the intact solder joint. Finite element analysis is generally used to calculate these values of strain or energy. These values are used as inputs to empirical expressions that are used for the life calculation. Examples of these expressions, including the Coffin-Manson equation, were discussed in section 4.4. In this research, to quantify the effects of both the non-uniform temperature distribution and the type of creep model on the fatigue life, the Coffin-Manson equation (Eq. (4.4)) was used. Various researchers have evaluated the parameters of the Coffin-Manson equation for different compositions of lead-free solder. In this research, the parameters obtained by Pang *et al.* [136] were used, which are for a solder joint composition of Sn3.8Ag0.7Cu using a failure criteria of 50 % load reduction in the solder. These parameters were derived from the experimentally obtained reliability data for a single lap shear joint. Their values of parameters r and C_2 were 0.913 and 26.3, respectively. Thus, the life prediction model for SnAgCu solder joints is:

$$N_f = \left(26.3\Delta\varepsilon_{in}\right)^{\frac{1}{0.913}} \quad 8.12$$

The inelastic strain ($\Delta\varepsilon_{in}$) used for assessment of the fatigue life was that for the stabilised temperature cycle predicted by the finite element analysis. The predicted respective stabilised inelastic strain and fatigue life for the different solder joint using Eq. (8.12) are presented in Tables 8-7 and 8-8. The predicted life has taken into account of the life consumed by the reflow. Load case B results in a higher predicted fatigue life for both creep models. Thus, consideration of the actual (non-uniform)

temperature distribution in the assembly resulted in a 50 % improvement in the predicted fatigue life for both creep models. The implication of the two different creep material models used in the creep analysis is very clear from the fatigue life estimation. The predicted fatigue life is higher (27 times) for creep model 1 than creep model 2 due to the lower stabilised inelastic strain, which is the result of the higher creep resistance predicted by creep model 1. The comparison of fatigue life consumed by reflow with that of post reflow sowed the effect of inelastic strain due to reflow on the fatigue life of solder joint is insignificant.

Table 8-7: Predicted fatigue life of the solder joint with Case A thermal condition for power cycling at room temperature

Creep model	Case A		
	Stabilised Inelastic strain	Consumed fatigue life by reflow (cycles)	Fatigue life (cycles)
1	0.0016	24	41430
2	0.0319	2	1561

Table 8-8: Predicted fatigue life of the solder joint with Case B thermal condition for power cycling at room temperature

Creep model	Case B		
	Stabilised Inelastic strain	Consumed fatigue life by reflow (cycles)	Fatigue life (cycles)
1	0.0011	36	62452
2	0.0220	3	2346

8.4.3 Creep Study for Constant Power Dissipation within a Varying Ambient Temperature

This section presents the creep analyses for the resistor assembly at a constant power dissipation within a varying ambient temperature. As discussed in section 5.1, in applications such as automotive, aerospace etc. the ambient temperature may vary significantly whilst an electronic assemblies constantly dissipates power. In these conditions the temperatures in the assembly are above the ambient temperature. However, both in actual thermal cycling tests and their simulation, it is usual practice that electronic assemblies are thermally cycled between two extreme ambient temperatures whilst neglecting the temperature gradients due to power dissipation. Therefore, this section demonstrates the effect of a non-uniform temperature distribution (thermal load Case D) for constant power dissipation within a varying ambient temperature by comparing it against a uniform temperature distribution (thermal load Case C).

8.4.3.1 Thermal History

To decide upon the thermal history, the chip resistor was assumed to be continuously dissipating power (at its de-rated level of, 0.15 W, due to its operating in an ambient temperature higher than 70 ^{o}C or 343 K) within an ambient temperature varying between 398 K and 218 K. Two approaches (cases C and D) to accounting for these thermal conditions were considered in this creep analysis. The thermal histories are similar to those used in the previous creep analysis, but with a wider ambient temperature range. The thermal histories used in cases C and D are shown in Fig. 8-20 (a) and (b) respectively, while Fig. 8-20 (c) illustrates the power dissipation used to obtain the temperature distribution in the chip resistor. The details of the thermal history are presented in Table 8-9, which is slightly different from the one used in the previous analysis with an additional ramp to the hot dwell temperature (line RS in Fig. 8-20 (a) and (b)) before starting the first temperature cycle. Addition of this ramp allows the same ramp rate as that used in the previous thermal history. The two different approaches to accounting for the temperature rise due to the power dissipation are discussed below:

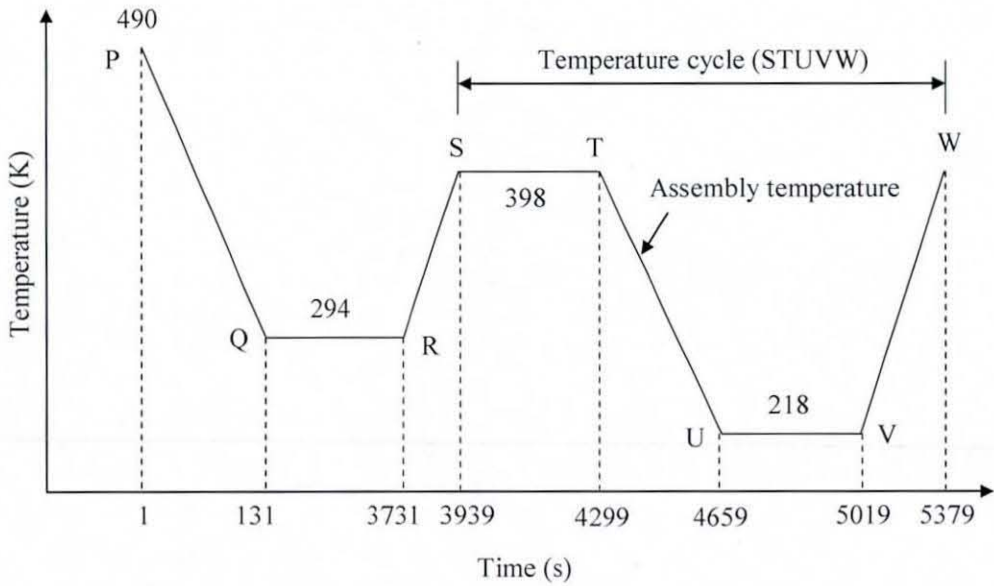
Case C: This case is similar to Case A in the previous creep analysis but with a wider temperature range. In this case, a spatially uniform temperature distribution was assumed for the entire resistor assembly during the hot dwell (line ST in Fig. 8.17 (a)) of the thermal history. During this dwell the entire chip resistor assembly was at 398 K, which is the maximum ambient temperature at which the chip resistor can be operated. When the temperature in the assembly was ramped down to a cold dwell (line UV in Fig. 8.17 (a)), the assembly was again assumed to be in the uniform temperature distribution state. The temperature during the cold dwell was 218 K, which is the minimum ambient temperature at which the chip resistor is designed to operate. Hence, this case represents the generally used idealisation of temperature cycling with a uniform temperature distribution and thus resembles typical thermal cycle tests with temperatures ranging between 398 K and 218 K.

Case D: This case represents the actual temperatures in the continuously power dissipating chip resistor assembly when the ambient temperature varies between 398 K and 218 K. Unlike Case C, a non-uniform temperature distribution was used during both hot and cold dwells (lines ST and UV, respectively, in Fig. 8-17 (b)) to take into account temperature gradients due to power dissipation. These non-uniform temperature distributions are taken from the thermal analysis of 2D assembly that was discussed in section 5.3.1.

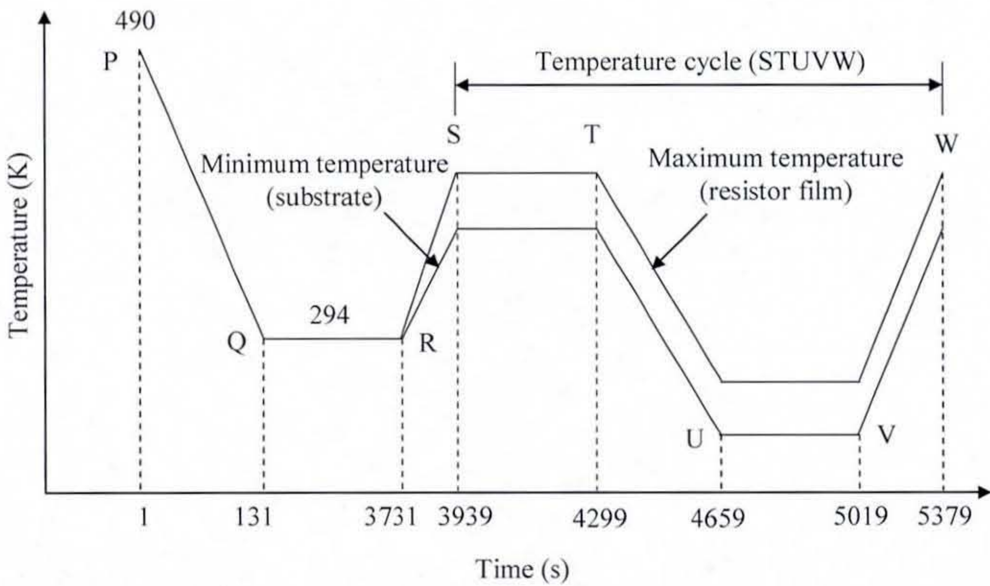
8.4.3.2 Results and Discussion

Creep Model 1

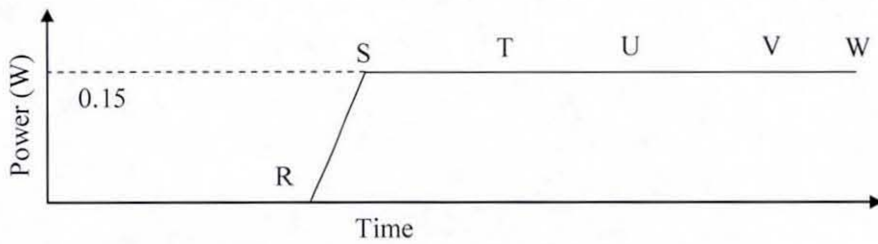
This analysis was carried out using creep model 1 (Eq. 8.10) for the solder joint. In this analysis, the chip resistor was subjected to 10 cycles of temperature cycle STUVW (Fig. 8-20 (a) and (b)) after the dwell at room temperature. The distribution and evolution of stresses in the solder joint was studied for the entire time range. Since the thermal history until the end of the room temperature dwell used in this creep analysis was the same as that used in the previous creep analyses, the stress distribution was the same as that discussed in section 8.4.2.2 up to this point.



(a)



(b)



(c)

Fig. 8-20: Thermal histories used for creep analyses for powered temperature cycling: (a) case C; (b) case D; (c) power dissipation

Table 8-9: Details of thermal history used for constant power dissipation within varying ambient temperatures

History step	Duration
Reflow process (PQ)	144 seconds
Dwell at room temperature (QR)	3600 seconds
Ramp to hot dwell (RS)	208 seconds
Hot dwell (ST)	360 seconds
Ramp to cold dwell (TU)	360 seconds
Cold dwell (UV)	360 seconds
Ramp to hot dwell (VW)	360 seconds

The evolution of shear stress in the solder was studied over the entire time range of the creep analysis at the maximum stress location in the solder (refer Fig. 8-13 (b)). Figure 8-21 demonstrates the evolution of shear stress at that location. The stress variation shows that the induced stress at the end of reflow diminishes due to creep relaxation during the room temperature dwell. Its evolution is the same for both cases C and D until the end of the dwell, due to them experiencing the same thermal history. The stress variation during the temperature cycle for both cases C and D is similar to cases A and B. However, it is clear from the stress evolution that due to the wider cyclic temperature range the maximum stress level induced in the solder joint during each cold dwell reaches the yield stress, which results in further plastic deformation of the solder joint. As presented in Table 8-10, the stress range for Case C is marginally higher than that for Case D, which is due to greater stress relaxation in the solder in Case C during the ramps from the cold dwell to the hot one. During the cold dwell (line UV in Fig. 8-20 (a) and (b)) for Case C, the homologous temperature (T_h) for the solder joint was about 0.44 and hence the creep in the solder joint was slow, resulting in a nearly constant stress in the solder joint during this period. A similar observation was made for Case D, even though the homologous temperature in the solder joint increased to about 0.49. It can also be seen from the stress results that the shear stress range had largely stabilised after the second temperature cycle.

The evolution of accumulated inelastic strain in the solder joint during the simulation was studied. Figure 8-22 illustrates the evolution of accumulated inelastic strain at the maximum inelastic strain range location (the maximum stress location) of the solder joint for cases C and D. With the incremental increase in the accumulated inelastic

strain for every temperature cycle, both cases C and D exhibit observation made in the earlier creep analyses. Due to the higher operating temperature, Case D results in higher inelastic strain accumulation at the end of the creep analysis. A comparison of the contributions of plastic and creep strain to the total inelastic strain for the simulated time range is presented in Figs. 8-23 (a) and (b) respectively for cases C and D. This comparison shows that the plastic strain increment due to plasticity is the same for each temperature cycle for both thermal cases. It is clear from these figures that the creep strain accumulation is greater for both cases. At the end of 10 cycles the plastic strain contribution is about 46 % for Case C while for Case D it contributes 36 % to the total accumulated inelastic strain. The accumulation of the inelastic strain for each temperature cycle was compared between cases C and D and it is presented in Table 8-11. Figure 8-24 shows the hysteresis loops for the shear stress-strain in Case C and it illustrates that the inelastic strain accumulation stabilised after the 6th temperature cycle for both cases. The stabilised cyclic accumulation of inelastic strain for Case D is 22 % higher than for Case C, which is a result of the non-uniform temperature distribution in the assembly and its effect on the fatigue life is discussed later in the section. Unlike the previous creep analyses, the inelastic strain due to reflow resulted in only 10 % and 9 % of the total accumulated inelastic strain respectively for cases C and D.

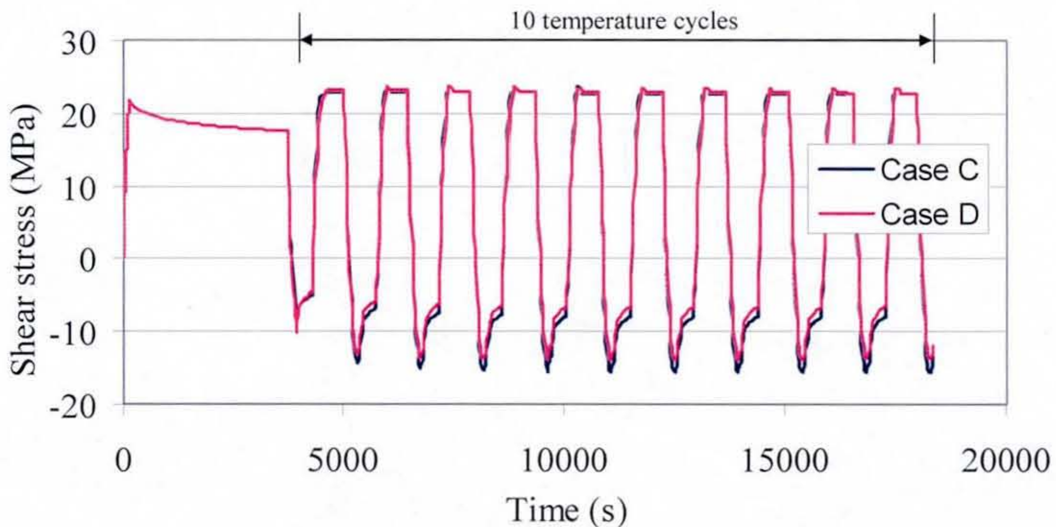


Fig. 8-21: Evolution of shear stress in the solder joint for creep model 2 over the entire simulation

Table 8-10: Predicted stress range in the solder joint using creep model 1 and constant power dissipation within a varying ambient temperature

Cycle	Shear stress range (MPa)	
	Case C	Case D
1	37.0	36.1
2	38.8	37.1
3	39.0	37.3
4	39.1	37.3
5	39.1	37.3
6	39.1	37.2
7	39.1	37.2
8	39.1	37.2
9	39.1	37.2
10	39.1	37.2

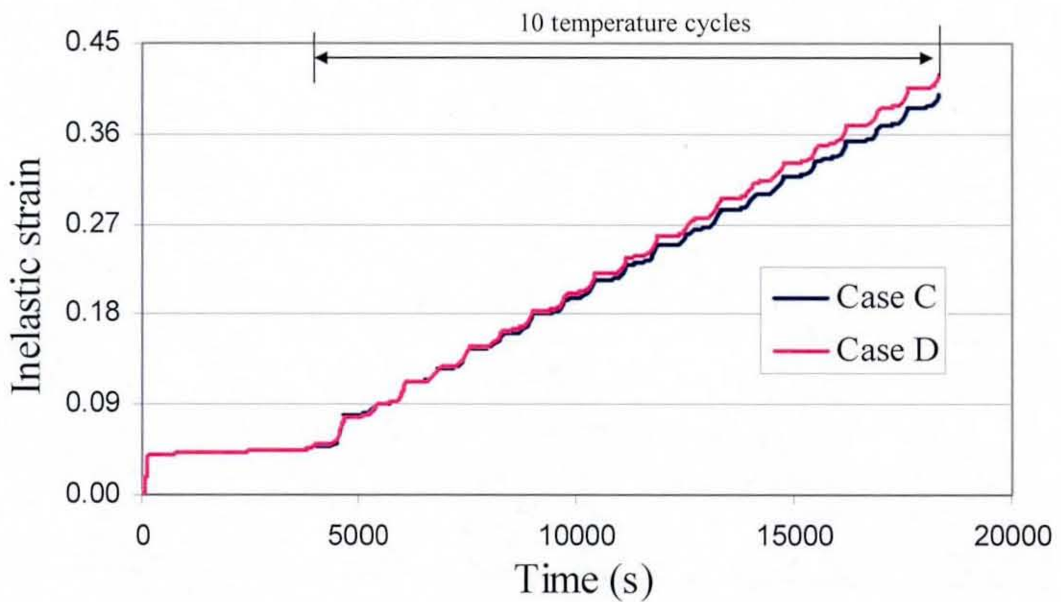
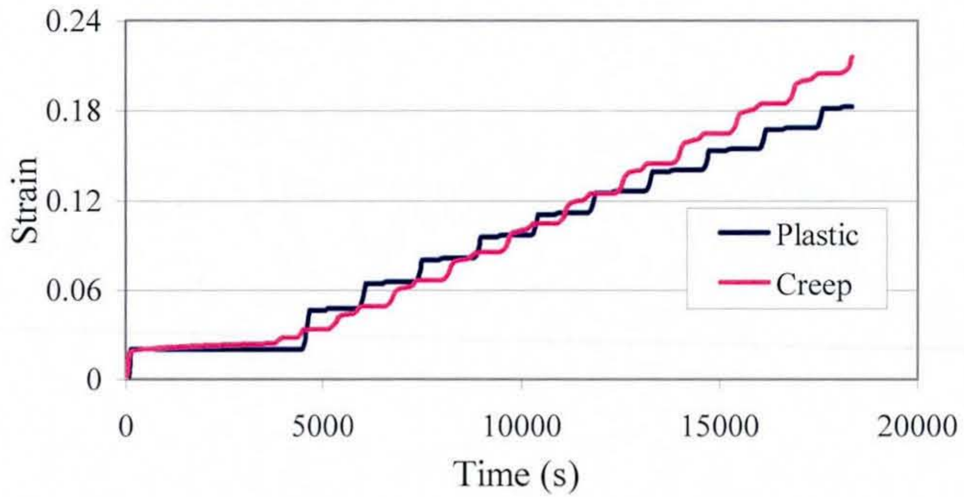
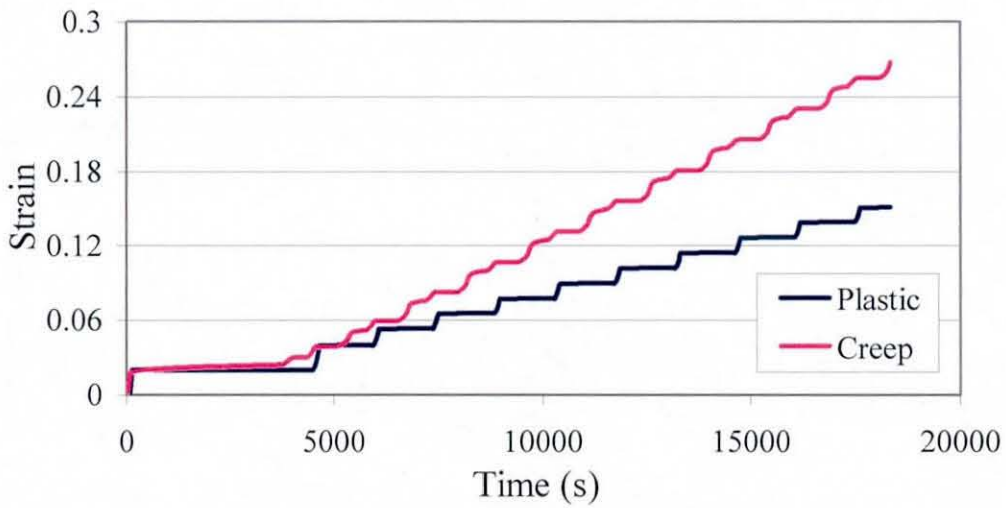


Fig. 8-22: Predicted evolution of accumulated inelastic strain in the solder joint using creep model 1 for constant power dissipation within a varying ambient temperature



(a)



(b)

Fig. 8-23: Evolution of plastic and creep strain in the solder joint using creep model 1 for constant power dissipation within a varying ambient temperature: (a) Case C; (b) Case D

Table 8-11: Predicted inelastic strain accumulation in the solder joint using creep model 1 for constant power dissipation within a varying ambient temperature

Cycle	Inelastic strain range	
	Case C	Case D
1	0.0137	0.0195
2	0.0167	0.0223
3	0.0182	0.0238
4	0.0192	0.0244
5	0.0198	0.0247
6	0.0200	0.0247
7	0.0202	0.0248
8	0.0202	0.0248
9	0.0202	0.0248
10	0.0202	0.0248

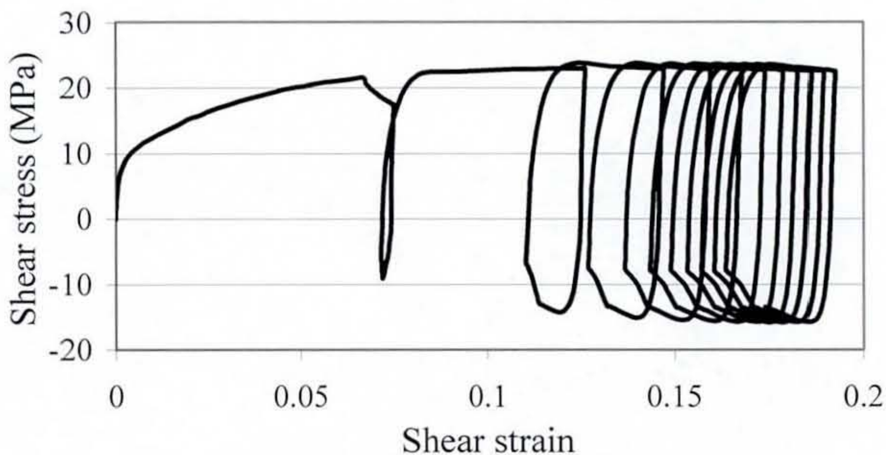


Fig. 8-24: Shear stress-strain hysteresis loop for thermal Case C using creep model 1

Creep Model 2

A simulation of the chip resistor assembly for the thermal histories explained in section 8.4.3.1 was also carried out employing creep model 2 (Eq. (8.11)). The resulting stress distribution in the solder joint until the end of the dwell at room temperature (point R in Fig. 8-20 (a) and (b)) is similar to that discussed in Section 8.4.2.2. The evolution of shear stress at the maximum stress location (Fig. 8-13 (b)) in the solder joint is illustrated in Fig. 8-25 for both cases C and D. The evolution of the shear stress until the end of cooling from reflow resembles that discussed above for

creep model 2 for power dissipation at room temperature (section 8.4.2.2). However, as occurred for creep model 1 for these loading conditions, the stress range is higher than in cases A and B and exceeds the initial residual stress level during each temperature cycle, causing additional plastic deformation. The stress evolution also showed that at the end of the hot ramp (line VW in Fig. 8-20 (a) and (b)) the stress in the solder joint become nearly zero. Therefore, the creep relaxation during the hot dwell is absent in both cases C and D. As observed in the simulation using creep model 1, the stress range is higher for Case C and is largely stabilised after the 7th temperature cycle for both thermal cases, as presented in Table 8-12. It is also clear from the shear stress-strain hysteresis loop presented in Fig. 8-26.

As for all other creep simulations, the accumulated inelastic strain exhibited incremental accumulation of strain in every temperature cycle which is shown in Fig. 8-27. The contribution of both plastic and creep strain to the inelastic strain was studied and its comparison in presented in Fig 28 (a) and (b) respectively for cases C and D. The plastic strain contributed about 2 % and 0.4 % to the accumulated inelastic strain at the end of 10 cycles for cases C and D respectively, which is much lower than the creep strain contributions of 98 % and 99.6 %. For the stabilised temperature cycle, Case D showed a higher inelastic strain accumulation than Case C, which is due to the wider cyclic temperature range. Table 8-13 presents the calculated inelastic strain for each temperature cycle. This is different to the room temperature load cases, where the strain per cycle initially increased as cycling progressed, but stabilised after 7 cycles. The stabilised inelastic strain range is 22 % higher for thermal Case D compared with Case C, since Case D includes the non-uniform distribution of temperature due to continuous heat dissipation. The implications of this for the fatigue life are discussed later. The inelastic strain due to reflow resulted in only 7 % and 6 % of the total accumulated inelastic strain respectively for cases C and D.

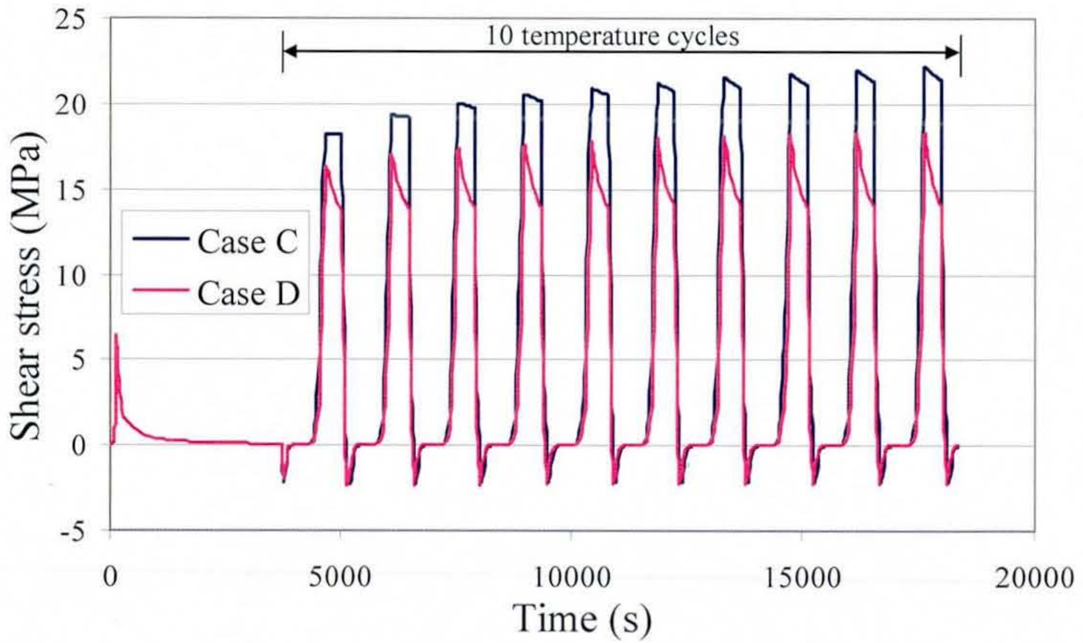


Fig. 8-25: Evolution of shear stress in the solder joint for creep model 2 over the entire simulation

Table 8-12: Stress range in the solder joint with creep model 2 and constant power dissipation within a varying ambient temperature

Cycle	Shear stress range (MPa)	
	Case C	Case D
1	20.5	18.6
2	21.6	19.3
3	22.2	19.6
4	22.7	19.8
5	23.1	20.0
6	23.4	20.2
7	23.6	20.4
8	23.9	20.4
9	24.2	20.5
10	24.2	20.6

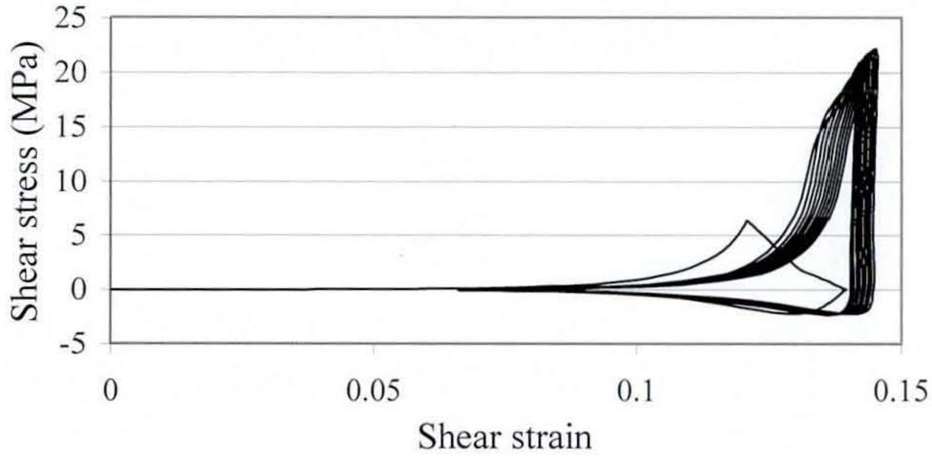


Fig. 8-26: Shear stress-strain hysteresis loop for thermal case C using creep model 2

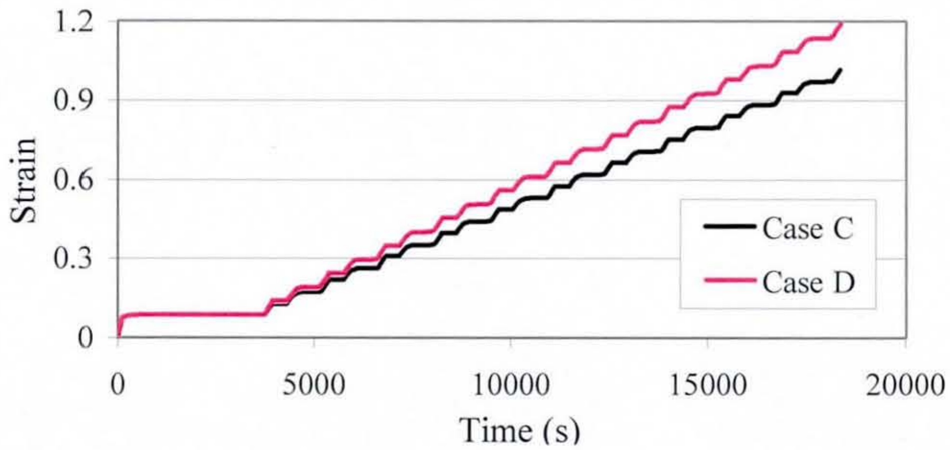
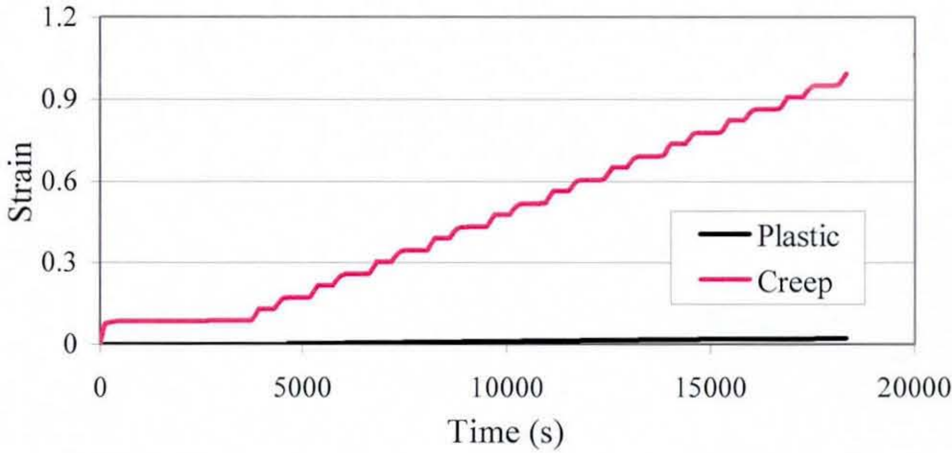


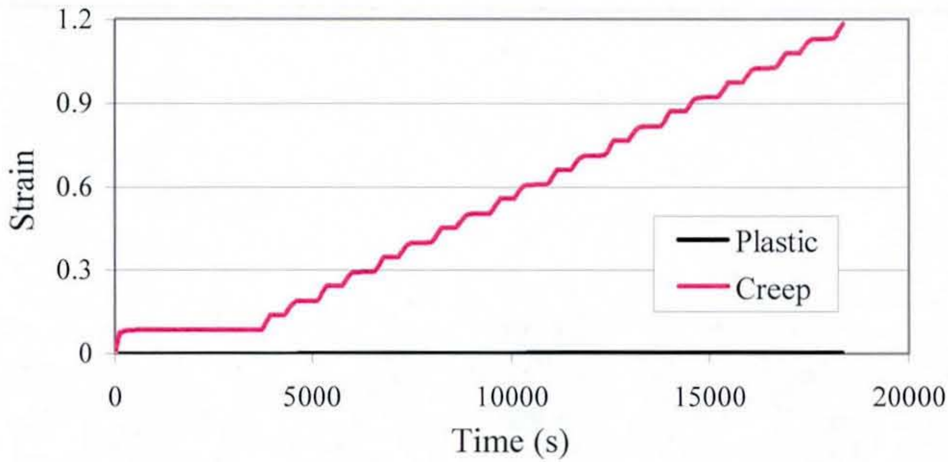
Fig. 8-27: Evolution of accumulated inelastic strain in the solder joint using creep model 2 for constant power dissipation within a varying ambient temperature

Table 8-13: Predicted inelastic strain accumulation in the solder joint using creep model 2 for constant power dissipation within a varying ambient temperature

Cycle	Inelastic strain range	
	Case C	Case D
1	0.0859	0.1043
2	0.0862	0.1046
3	0.0863	0.1047
4	0.0864	0.1048
5	0.0864	0.1048
6	0.0864	0.1048
7	0.0866	0.1049
8	0.0866	0.1049
9	0.0866	0.1049
10	0.0866	0.1049



(a)



(b)

Fig. 8-28: Evolution of plastic and creep strain in the solder joint using creep model 2 for constant power dissipation within a varying ambient temperature: (a) Case C; (b) Case D

Comparison of the results for creep models 1 and 2 for varying ambient temperature creep simulations shows the importance of selecting the appropriate creep model for the solder joint. Creep model 2, which was derived from the lowest measured creep resistance of the solder joints, resulted in a higher stabilised inelastic cyclic strain than for creep model 1. Comparison of the stabilised inelastic strain ranges between cases C and D shows the effect of considering the powered (non-uniform) temperature distribution in such simulations.

Fatigue Life Estimation

As for the room temperature creep analyses, the fatigue life was predicted for both reflow and post reflow thermal cycling. The predicted life is presented in Tables 14 and 15 respectively for Cases C and D. In case of creep model 1, just 2 thermal cycles were consumed by the reflow for both the thermal Cases C and D. However, with creep model 2 it is only one cycle.

The post reflow solder joint fatigue lives for Cases C and D were also estimated to identify the effects of the non-uniform temperature distribution and choice of creep model. The Coffin-Manson equation (Eq. (8.12)) and its constants used to predict the fatigue life were discussed in Section 8.4.2.2. The inelastic strain range was taken from the stabilised cycle. The predicted fatigue life of the solder joint based on Eq. (8.12) is presented in Table 8-14. Case D, which represents the non-uniform temperature distribution in the assembly, showed a lower fatigue life for both creep models (creep model 1 and 2). Thus, the consideration of the actual (non-uniform) temperature distribution in the assembly resulted in a 20 % decrease in the fatigue life for both creep models compared with the idealised (uniform) temperature distribution. The impact of the two different creep material models used in the creep analysis is also clear from the fatigue life comparison. The predicted fatigue life for creep model 2 in only 20 % of that for model 1 due to its lower creep resistance, which results in a higher stabilised inelastic cyclic strain. The comparison of fatigue life consumed by reflow with that of post reflow showed that the effect of inelastic strain due to reflow on the fatigue life of solder joint is insignificant.

Table 8-14: Predicted fatigue life of the solder joint with Case C thermal condition for constant power dissipation within a varying ambient temperature

Creep model	Case C		
	Stabilised Inelastic strain	Consumed fatigue life by reflow (cycles)	Fatigue life (cycles)
1	0.0202	2	2577
2	0.0866	2	522

Table 8-15: Predicted fatigue life of the solder joint with Case D thermal condition for constant power dissipation within a varying ambient temperature

Creep model	Case D		
	Stabilised Inelastic strain	Consumed fatigue life by reflow (cycles)	Fatigue life (cycles)
1	0.0247	1	2068
2	0.1049	1	423

8.5 Summary

The discussed finite element analyses included two different creep models and two thermal cases each for power dissipation at room temperature and within a varying ambient temperature. Both plasticity and creep behaviour in the solder joint were simulated. The following points summarise the outcome of these FE analyses:

1. The 2D and 3D simulations of the chip resistor assembly showed that the chip resistor assembly can adequately be modelled using the 2D plane strain formulation.

2. Plastic deformation in the solder joint during manufacturing depends on the material model, which is evident from the plastic strain results in the solder at the end of the reflow. There is no further plastic deformation during temperature cycling in the case of power dissipation at room temperature, however, the varying ambient conditions resulted in further plasticity due to wider temperature range during cycling.

3. The simulation including creep of the surface mount assembly showed the non-uniform temperature distribution thermal case (Case B) for power dissipation at room temperature resulted in a 45 % lower stabilised cyclic inelastic strain than for the traditional/unpowered uniform temperature distribution case (Case A). This difference in the stabilised inelastic strain improved the fatigue life of the solder joints by 50 %, as shown in Figs. 8-29 and 8-30.

4. Thermal Case D, which accounts for the non-uniform temperature distribution,

in the simulation of continuously heat-dissipating chip resistor assembly within a varying ambient temperature yielded 22 % higher stabilised inelastic cyclic strain than for the general uniform temperature distribution case (Case C). This, in turn, resulted in a 20 % lower prediction of fatigue life for the solder joints, as shown in Figs. 8-29 and 8-30. Therefore, the power dissipation must be treated case by case.

5. The two different creep material models, which represent the two potential extremes of the mechanical behaviour of the solder joints, showed a very significant effect on the stabilised inelastic strain and, therefore, on the fatigue life of the solder joint.

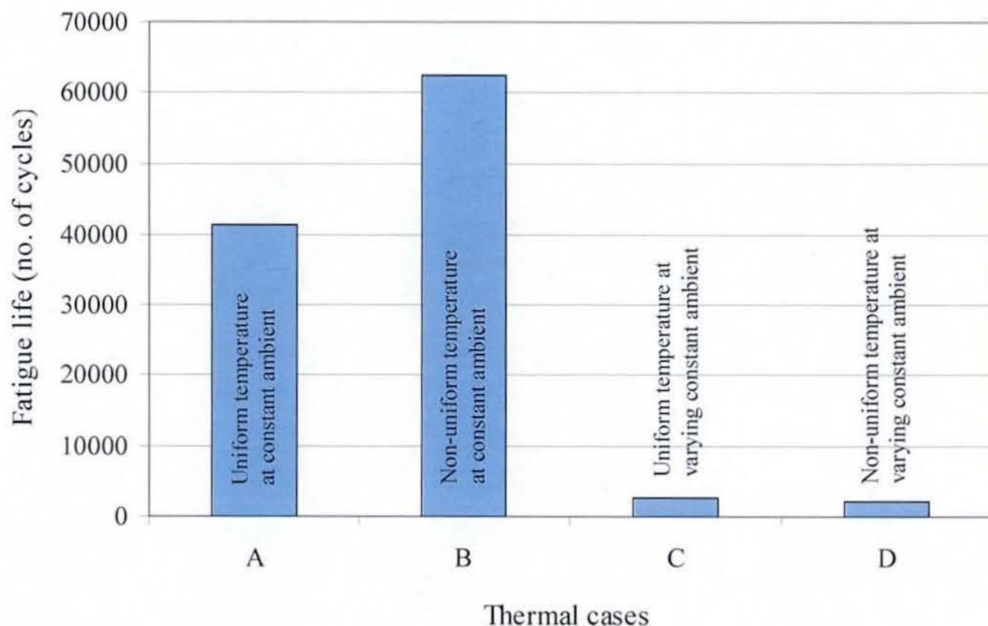


Fig. 8-29: Comparison of predicted fatigue life for creep model 1

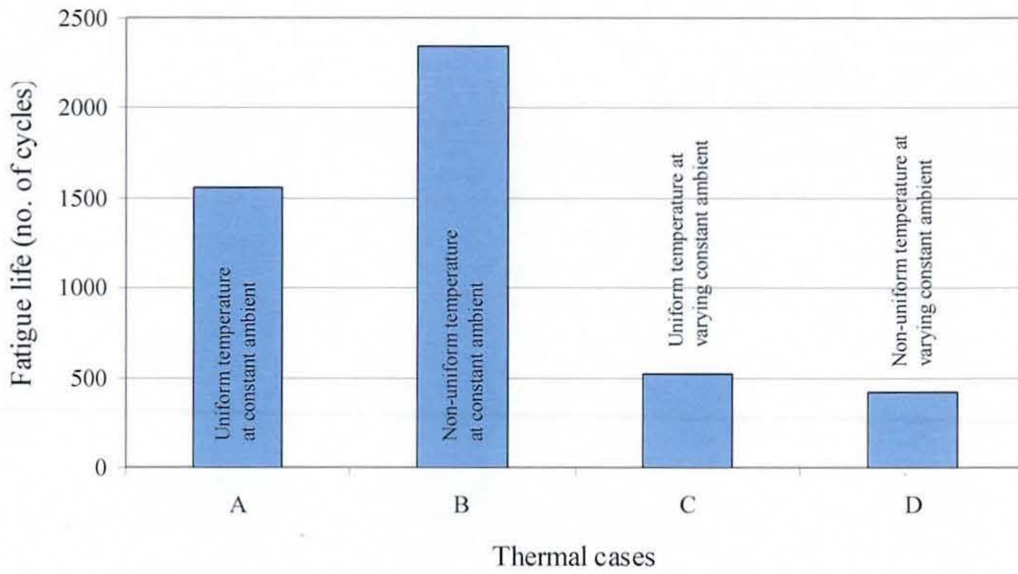


Fig. 8-30: Comparison of predicted fatigue life for creep model 2

9. Conclusions and Future Work

This thesis has focused on two important research novelties on the reliability in lead-free solder joints. First, the determination of the effect of size and microstructure on mechanical behaviour of small-scale Sn3.8Ag0.7Cu solder joints that are commensurate in scale and thermal history with the real application. Second, the effect of a realistic non-uniform temperature distribution in a surface mount assembly on the solder joint reliability considering different thermal cases. The above research novelties along with other results are discussed below:

Temperature Study for a Powered Surface Mount Assembly

1. In thermal cycling tests or FEA of electronic assemblies, it is generally assumed that the temperature within the assembly is uniform. However, the experimental study illustrated the non-uniform distribution of temperature in a typical surface mount assembly when powered, which clearly demonstrated the assumption of uniform temperature distribution is unlike the actual thermal conditions during operation. This study also provided quantitative data for use as boundary conditions in the subsequent stress analyses. Similar non-uniform temperature distributions can be expected in other electronic assemblies such as BGA, flip-chip etc. when these are powered.

Tensile Testing of Lead-Free Solder

1. The properties of a solder joint are greatly influenced by its microstructure and size. The solder joints manufactured for this work generally contained a finer microstructure than the reflowed bulk solder, which contributed to the increased strength of the solder joints compared with bulk solder. It has also been shown that the solder joints exhibit size effect whereby their tensile properties increase with reducing size. Hence, the solder joint exhibited significantly higher tensile properties than the bulk solder. Also, the contributions of size and microstructure effect on solder material properties were quantified with the help of FEA. Therefore, it has been shown that the use of tensile properties determined for a

bulk solder sample in FEA will not allow an accurate estimate of the solder joint reliability.

2. The stress-strain properties of the solder joints are dependent on the strain rate. The hardening behaviour of the solder joint increases with increasing load rates or strain rates, as demonstrated by the increased ultimate strength. As the load rate increases, the time available for processes such as grain boundary sliding, dynamic recovery and re- crystallisation decreases, thus the load required for the failure of the joint increases. The strain rate dependency of stress-strain properties in the solder joint was modelled effectively using the Johnson-Cook constitutive equation.
3. As the size of solder joints decreases the plastic deformation during tensile load is constrained by the elastic substrate on either side of the solder joint. In addition, the Poisson's effect is also observed on the free surface of the solder joint. These effects result in a complex 3D stress state in the solder joint in spite of the uniaxial loading. Therefore, the load required for the failure of the solder joint is increased.

Creep Testing of Lead-Free Solder

1. The experimentally determined creep behaviour illustrates that the creep resistance of small-scale solder joints under a tensile load is greater than that for the bulk solder and for solder joints in shear. This is again because of the effect of the finer solder joint microstructure and the joint size, which increases the yield and ultimate strengths of the solder joint and thereby affects the creep behaviour of the solder joint under tensile load.
2. The creep properties of the solder joints under shear load revealed the effect of anisotropic behaviour of Sn-grains in the solder joint on its material properties. Due to the BCT structure of the Sn-grains, their orientation with respect to the loading direction plays a very important role. The size effect is also eliminated in the shear creep, wherein the solder joint between the copper substrate is subjected to simple shear which avoids the constraining effect either due to the elastic copper substrate or due to Poisson's effect.
3. The study of tensile and shear creep properties showed the difference between the tensile creep and the shear creep properties converted to equivalent tensile

properties using the von Mises transformation. This highlights the use of von Mises transformation after determining the solder joint material properties under any one load type (either tensile or shear) to determine properties for other load types (either shear or tensile) is not an appropriate approach. Therefore, the separate determination of solder joint material properties separately in tensile and shear load is sensible.

4. An order of magnitude scatter in the tensile and creep properties was observed for the solder joints. This illustrates the effect of differences in the individual solder joint microstructures, such as the number of Sn-grains, orientation of Sn-dendrites, voids etc., on its material properties. The solder joint usually consists one or a few Sn-grains that are separated by grain boundaries. Grain boundaries are the weak locations in solder joint, and as the number of grain boundaries increases the strength of the solder joint decreases. Voids in the solder joint have similar effect.

Finite Element Analysis and Reliability

1. The finite element elasto-plastic analysis of a surface mount chip resistor assembly using with both 2D and 3D formulations showed similar results. Therefore, the 2D plane strain element formulation can be used to represent the physical behaviour of the chip component assembly which saves considerable computational time (67 %).
2. The FE analysis results for the chip resistor assembly demonstrate that the actual (non-uniform) temperature distribution significantly influences the estimated solder joint fatigue life depending on the application environment. For example, the use of a traditional uniform temperature distribution is conservative for power cycling within a room temperature environment, while for powered operation within a varying ambient temperature it is optimistic. Therefore, consideration of the potential effects of the actual temperature distribution is required to ensure FE analysis providing realistic life estimation. This approach can be extended to other types of surface mount assemblies to include the effect of non-uniform temperature distributions on their solder joint's fatigue life.
3. Due to the anisotropic behaviour of the solder joint microstructure, the creep behaviour under a tensile load is different from use of the von Mises conversion

of creep properties under a shear load. Since the material properties of solder joints directly affect their structural integrity, appropriate estimation of them for the solder joints manufactured using conditions used by the manufacturer is essential. Having obtained the material properties, the worst case can be identified and used for subsequent reliability studies of the solder joints.

9.1 Future Work

The research presented here has led to the identification of additional areas of further work, a number of which are discussed below:

1. This research focused on the determination of the solder joint material properties at room temperature and relied on published for extrapolation of these properties to other temperatures. Determine of the material properties at temperatures lower and higher than room temperature would provide a more robust material model.
2. As demonstrated by the research, at room temperature the higher tensile material properties of solder joints compared with bulk solder are contributed to by both differences in microstructure and the size effect. Research into the variation of this contribution of microstructure and size effect at different temperatures would allow for future study.
3. The thermal history used in the creep analysis assumed a linear cooling rate from the reflow temperature. However the actual cooling rate may follow an exponential function. Therefore, further studies can be carried out considering the actual cooling rate and its effect on creep damage.
4. The elasto-plastic material properties of the solder joint were modelled using a multi-linear isotropic hardening law which assumes that yield stress in tension and compression is the same, which is unlike actual material behaviour. Thus development of a user defined material model which includes both elasto-plastic material properties together with multi-linear kinematic hardening and creep material models would provide a scope for future work.
5. In this research, the solder was modelled as an isotropic material, which is unlike reality due to the anisotropic behaviour of Sn-grains. Therefore, further work could be carried out modelling solder joints containing multiple grains with different orientations and respective material properties inline with the work carried out by Gong *et al* [111].

References

[1] Lau, J. H., *Flip Chip Technologies*, McGraw-Hill, London, UK, 1996.

[2] Harper, C. A., *Electronic Packaging and Interconnection Handbook*, McGraw Hill, London, UK, 1991.

[3] Whalley, D. C., *An Investigation of Environmental Testing of Surface Mounted Components*, MPhil Thesis, Loughborough University, Loughborough, UK, 1988.

[4] Lea, C., *A Scientific Guide to Surface Mount Technology*. Electrochemical Publications Limited, Ayr, UK, 1988.

[5] Lee, N. -C., *Reflow Soldering Processes and Troubleshooting, SMT, BGA, CSP and Flip Chip Technologies*. Newnes, Boston, USA, 2001.

[6] Ganesan, S., Pecht, M., *Lead-Free Electronics*, John Wiley & Sons, New York, USA, 2006.

[7] Frear, D. R., Jang, J. W., Lin, J. K., Zhang, C., *A Metallurgical Study of Pb-free Solders for Flip Chip Interconnects*, Journal of Metals, vol. 53, pp. 28-32, 2001.

[8] Lee, N. -C., *The Next Generation of Solder for Electronics*, International Journal of Chip-Scale Electronics, 2004.

[9] Puttlitz, K. J., Kathleen, A. S., *Handbook of Lead-free Solder Technology for Microelectronic Assemblies,* Marcel Dekker, New York, USA, 2004.

[10] *Lead Exposure in Construction - Protective Clothing*, U.S. Department of Labour 1993.

[11] Matin, M. A., Vellinga, W. P., Geers, M. G. D., Thermo-mechanical Fatigue Damage Evolution in SAC Solder Joints, *Material Science and Engineering*, vol. A 445-446, pp. 73-85, 2007.

[12] Wu, C. M. L., Yu, D. Q., Law, C. M. T., Wang, L., The Properties of Sn-9Zn Lead-Free Solder Alloys Doped with Trace Rare Earth Elements, *Journal of Electronic Materials*, vol. 31, pp. 921-927, 2002.

[13] Wu, C. M. L., Yu, D. Q., Law, C. M. T., Wang, L., Properties of Lead-free Solder Alloys with Rare Earth Element Additions, *Materials Science and Engineering*, vol. R 44, pp. 1-44, 2004.

[14] Dusek, M., Hunt, C., *The Measurement of Creep Rates and Stress Relaxation for Micro Sized Lead-Free Solder Joints*, NPL Report, 2005 (DEPC MPR 021), Teddington, UK 2005.

[15] *Lead-Free Solder Project Final Report*, National Center for Manufacturing Sciences, USA, 1997.

[16] Suganuma, K., *Lead-free Soldering in Electronics Science, Technology, and Environmental Impact*, Marcel Dekker, New York, USA, 2004.

[17] Miric, A. Z., Grusd, A., Lead-Free Alloys, *Soldering & Surface Mount Technology*, vol. 10, pp. 19-25, 1998.

[18] *Lead-free Basics*, Kester, www.kester.com, 2005.

[19] Plumbridge, W. J., Long Term Mechancal Rliability with Lead-free Solders, *Soldering & Surface Mount Technology*, vol. 16, pp. 13-20, 2004.

[20] Shangguan, D., *Lead-Free Solder Interconnect Reliability*, ASM International, Materials Park, USA, 2005.

[21] Popov, E. P., *Mechanics of Materials*, Prentice Hall of India Private Limited, New Delhi, India, 1986.

[22] Boresi, A. P., Schmidt, R. J., *Advanced Mechanics of Materials*, John Willey & Sons, New York, USA, 2003.

[23] Dieter, G. E., *Mechanical Metallurgy*, McGraw-Hill Book Co., New York, USA, 1986.

[24] Timoshenko, S., *Strength of Materials, Part 1: Elementary Theory and Problems*, CBS Publishers & Distributors, New Delhi, India, 2002.

[25] *Standard Test Methods for Young's Modulus, Tangent Modulus, and Chord Modulus*, ASTM Standard E 111-04, West Conshohocken, USA, 2004.

[26] Timoshenko, S., *Strength of Materials, Part 2: Advanced Theory and Problems*, CBS Publishers & Distributors, New Delhi, India, 2000.

[27] *Standard Practice for Verification and Classification of Extensometer System*, ASTM E83-02, West Conshohocken, USA, 2002.

[28] Dunne, F., Petrinic, N., *Introduction to Computational Plasticity*, Oxford University Press, London, UK, 2005.

[29] Lau, J. H., *Thermal Stress and Strain in Microelectronics Packaging*, Van Nostrand Reinhold, New York, USA, 1993.

[30] Towashiraporn, T., Gall, K., Subbarayan, G., McIlvanie, B., Hunter, B. C., Love, D., Sullivan, B., Power Cycling Thermal Fatigue of Sn-Pb Solder joints

on a Chip Scale Package, *International Journal of Fatigue*, vol. 26, pp. 497-510, 2004.

[31] Ronnie, J. W., Sun, Y. F., Spalling Behaviour of Interfacial Intermetallic Compounds in Pb-free Solder Joints Subjected to Temperature Cycling Loading, *Acta Materialia*, vol. 56, pp. 242-249, 2008.

[32] Nemat-Nasser, S., *Plasticity: A Treatise on Finite Deformation of Heterogeneous Inelastic Materials*, Cambridge University Press, Cambridge, UK, 2004.

[33] Lemaitre, J., Chaboche, J. L., *Mechanics of Solid Materials*, Cambridge University Press, Cambridge, UK, 2002.

[34] Pang, J. H. L., Xiong, B. S., Mechanical Properties for 95.5Sn-3.8Ag-0.7Cu Lead-Free Solder Alloy, *IEEE Transactions on Component and Packaging Technologies*, vol. 28, pp. 830-840, 2005.

[35] Pang, J. H. L., Xiong, B. S., Neo, C. C., Zhang, X. R., Low, T. H, Bulk and Solder Joint Properties foe Lead-Free 95.5Sn-3.8Ag-0.7Cu Solder Alloy, *53rd Electronic Components and Technology Conference*, New Orleans, USA, pp. 673-679, 2003.

[36] Qiang, W., Lihua, L., Xuefan, C., Xiaohong, W., Experimental Determination and Modification of Anand Model Constants for Pb-free Material 95.5Sn4.0Ag0.5Cu, *Proc. 8th Int. Conf. on Thermal, Mechanical and Multiphysics Simulation and Experiments in Micro-Electronics and Micro-Systems, EuroSimE*, London, UK, pp. 308-316, 2007.

[37] Pang, J. H. L., Xiong, B. S., Che, F. X., Modeling Stress Strain Curves for Lead-Free 95.5Sn-3.8Ag-0.7Cu Solder, *Proc. 5th Int. Conf. on Thermal and Mechanical Simulation and Experiments in Micro-electronics and Micro-Systems, EuroSIME*, Brussels, Belgium, pp. 449-453, 2004.

[38] Xue-Bin, W., Temperature Distribution in Adiabatic Shear Band for Ductile Metal Based on Johnson-Cook and Gradient Plasticity Models, *Trans. Nonferrous Met. Soc. China*, vol. 16, pp. 333-338, 2006.

[39] Teng, X., Wierzbicki, T., Evaluation of Six Facture Models in High Velocity Perforation, *Engineering Fracture Mechanics*, vol. 73, pp. 1653-1678, 2006.

[40] Kajberg, J., Wikman, B., Viscoplastic Parameter Estimation by High Strain-rate Experiments and Inverse Modelling Speckle Measurements and High-

Speed Photography, *International Journal of Solids and Structures, Article in press,* vol. 44 pp. 145–164, 2007.

[41] Rule, W. K., Jones, S. E., A Revised Form for the Johnson-Cook Strength Model, *International Journal of Impact Engineering,* vol. 21, pp. 609-624, 1998.

[42] Weronsi, A., Hejwowski, T., *Thermal Fatigue of Metals*, Marcel Dekker, New York, USA, 1991.

[43] Gittus, J., *Creep, Viscoelasticity and Creep Fracture in Solids*, Applied Science Publishers Ltd., London, UK, 1975.

[44] Clech, J. -P., Comparative Analysis of Creep Data for Sn-Ag-Cu Solder Joints in Shear, *Micromaterials and Nanomaterials,* issue 3, pp. 144-154, 2004.

[45] Wiese, S., Meusel, E., Wolter, K. J., Microstructural Dependendence of Constitutive Properties of Eutectic SnAg and SnAgCu Solders, 53rd *Electronic Components and Technology Conference*, New Orleans, USA, pp. 197-206, 2003.

[46] Schubert, A., Dudek, R., Auerswald, E., Gollhardt, A., Michel, B., Reichl, H., Fatigue Life Models of SnAgCu and SnPb Solder Joints Evaluated by Experiements and Simulations, *53rd Electronic Components and Technology Conference*, New Orleans, USA, pp. 603-610, 2003.

[47] Zhang, Q., Dasgupta, A., Haswell, P., Viscoplastic Constitutive Properties and Energy-partioning Model of Lead-free Sn3.8Ag0.6Cu Solder Alloy, *53rd Electronic Components and Technology Conference*, New-Orleans, USA, pp. 1862-1868, 2003.

[48] Syed, A., Accumulated Creep Strain and Energy Density Based Thermal Fatigue Life Prediction Models for SnAgCu Solder Joints, *54th Electronic Components and Technology Conference*, Las Vegas, USA, pp. 737–746, 2004.

[49] Abtew, M., Selvaduray, G., Lead-free Solders in Microelectronics, *Materials Science and Engineering,* vol. Rep. 27, pp. 95–141, 2000.

[50] Suganuma, K., Advances in lead-free electronics soldering, *Current Opinion in Solid State and Materials Science,* vol. 5, pp. 55-64, 2001.

[51] Glazer, J., Microstructure and Mechanical Properties of Pb-free Solder Alloys for Low Cost Electronic Assembly: a review, *Journal of Electronic Materials,* vol. 23, pp. 693–699, 1994.

[52] Wu, C. M. L., Yu, D. Q., Law, C. M. T., Wang, L., Improvements of Microstructure, Wettability, Tensile and Creep Strength of Eutectic Sn–Ag Alloy by Doping with Rare Earth Elements, *Journal of Material Research,* vol. 31, pp. 3146–3154, 2002.

[53] Chada, S., Fournelle, R. A., Laub, W., Shangguan, D., Copper Substrate Dissolution in Eutectic Sn-Ag Solder and its Effect on Microstructure, *Journal of Electronic Materials,* vol. 29, pp. 1214-1221, 2000.

[54] Chada, S., Shangguan, D., *Envoronmental-Friendly Electronics: Lead-Free Technology*, Electrochemical Publications Ltd, Port Erin, UK, 2001.

[55] Sundelin, J. J., Nurmi, T. S., Lepisto, K. T., Ristolainen, O. E., Mechanical and Microstructural Properties of SnAgCu Solder Joints, *Materials Science and Engineering*, vol. A 420, pp. 55-62, 2006.

[56] Kang, S. K., Choi, W. K., Shih, D. Y., Lauro, P., Henderson, D. W., Gosselin, T., Leonard, D. N., Interfacial Reactions, Microstructure, and Mechanical Properties of Pb-free Solder Joints in PBGA Laminates, *52nd Electronic Component and Technology Conference*, San Diego, USA, pp. 146-153, 2002.

[57] Chuang, C.-M., Shih, P. -C., Lin, K. -L., Mechanical Strength of Sn-3.5Ag-Based Solders and Related Bondings, *Jounal of Electronic Materials,* vol. 33, pp. 1-6, 2004.

[58] Lehman, L. P., Athavale, S. N., Fullem, T. Z., Giamis, A. C., Kinyanjui, R. K., Lowenstein, M., Mather, K., Patel, R., Wang, J., Xing, Y., Zavalij, L., Borgesen, P., Cotts, E. J., Growth of Sn and Intermetallic Compunds in Sn-Ag-Cu Solder, *Jounal of Electronic Materials,* vol. 33, pp. 1429-1439, 2004.

[59] Telang, A. U., Bieler, T. R., Choi, S., Subramanian, K. N., Orientation Imaging Studies of Sn-based Electronic Solder Joints, *Journal of Material Research,* vol. 17, pp. 2294-2306, 2002.

[60] Bieler, T. R., Jiang, H., Influence of Sn Grain Size and Orientation on the Thermomechanical Response and Reliability of Pb-free Solder Joints, *57th Electronic Components and Technology Conference*, San Diego, CA, USA, pp. 1462-1467, 2006.

[61] Henderson, D. W., Gosselin, T., Sarkhel, A., Kang, S. K., Choi, W. -K., Shih, D. -Y., Goldsmith, C., Puttlitz, K. J., Ag3Sn Plate Formation in the Solidification of Near Ternary Eutectic Sn-Ag-Cu Alloys, *Journal of Material Research,* vol. 17, pp. 2775-2778, 2002.

[62] Kang, S. K., Choi, W. K., Shih, D. -Y., Henderson, D. W., Gosselin, T., Sarkhel, A., Goldsmith, C., Puttlitz, K. J., Formation of AgSn Plates in Sn-Ag-Cu Alloys and Optimization of their Alloy Composition, *53rd Electronic Component and Technology Conference*, New Orleans, USA, pp. 64-70, 2003.

[63] Liu, P. L., Shang, J. K., Influence of Microstructure on Fatigue Crack Growth Behavior of Sn-Ag Solder Interfaces, *Journal of Electronic Materials,* vol. 29, pp. 622-627, 2000.

[64] Moon, K.-W., Boettinger, W. J., Katter, U. R., Biancaniello, F. S., Handwerker, C. A., Experimental and Thermodynamic Assessment of Sn-Ag-Cu Solder Alloys, *Journal of Electronic Materials,* vol. 29, pp. 1122-1136, 2000.

[65] Yang, W., Messler, R. W., Felton, L. E., Microstructure Evolution of Eutectic Sn-Ag Solder Joints, *Journal of Electronic Materials,* vol. 23, pp. 765-772, 1994.

[66] Zheng, Y., Hillman, C., McCluskey, P., *Intermetallic Growth on PWBs Soldered with Sn-3.8Ag-0.7Cu*, University of Maryland, USA.

[67] Madeni, J., Liu, S., Siewert, T., Intermetallics Formation and Growth at the Interface of Tin-based Solder Alloys and Copper Substrates, *2nd International Brazing and Soldering Conference*, San Diego, USA, 2003.

[68] Choi, W. K., Lee, H. M., Effect of Soldering and Aging Time on Interfacial Microstructure and Growth of Intermetallic Compounds between Sn–3.5Ag Solder Alloy and Cu Substrate, *Journal of Electronic Materials,* vol. 29, pp. 1207-1213, 2000.

[69] Choi, S., Lee, J. G., Subramanian, K. N. Lucas, J. P., Bieler, T. R., Microstructural Characterization of Damage in Thermomechanically Fatigued Sn-Ag Based Solder Joints, *Journal of Electronic Materials,* vol. 31, pp. 292-297, 2002.

[70] Lee, J. G., Telang, A. U., Subramanian, K. N., Bieler, T. R., Modeling Thermomechanical Fatigue Behaviour of Sn-Ag Joints, *Journal of Electronic Materials,* vol. 31, pp. 1152-1159, 2002.

[71] Subramanian, K. N., Lee, J. G., *J. Mater Sci.: Mater in Electron.,* vol. 15, pp. 235-240, 2004.

[72] Lehman, L. P., Kinyanjui, r. K., Wang, J., Xing, Y., Zavalij, L., Borgesen, P., Cotts, E. J., Microstructure and Damage Evolution in Sn-Ag-Cu Solder joints,

55th Electronic Components and Technology Conference, Lake Buena Vista, Florida, USA, 2005.

[73] Dunford, S., Canumalla, S., Viswanadham, P., Intermetallic Morphology and Damage Evolution Under Thermomechanical Fatigue of Lead (Pb)-free Solder Interconnections, *54th Electronic Component and Technology Conference*, Las Vegas, USA, pp. 726-736, 2004.

[74] Clech, J.-P., *Lead-Free and Mixed Assembly Solder joint Reliability Trends*, EPSI Inc., Montclair, USA 2004.

[75] Engelmaier, W., *Solder Joints in Electronics: Design for Reliability*, Engelmaier Associates, L.C., Ormond Beach, USA 1983.

[76] Noda, N., Hetnarski, R. B., Tanigawa, Y., *Thermal Stresses*, Taylor & Francis, New York, USA, 2003.

[77] Shen, Y.-L., Thermo-mechanical Stresses in Copper Interconnects -A Modelling Analysis, *Microelectronic Engineering*, vol. 83, pp. 446-459, 2006.

[78] *Environmental Engineering Considerations and Laboratory Tests: Vibration*, MIL-STD-810F, Method 514.5, U. S. Department of defense, USA.

[79] *Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachment*, IPC-SM-785, 1992.

[80] Setty, K., Subbarayan, G., Nguyen, L., Powercycling Reliability, Failure Analysis and Acceleration Factors of Pb-free Solder Joints, *56th Electronic Components and Technology Conference*, Orlando, USA, pp. 907-915, 2005.

[81] Salmela, O., Comments on the IPC Surface Mount Attachment Reliability Guidelines, *Quality and Reliability Engineering International*, vol. 21, pp. 345-354, 2005.

[82] *Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments*, IPC-9701, 2002.

[83] Shine, M. C., Fox, L. R., Fatigue of Solder Joints in Surface Mount Devices, Low Cycle Fatigue, *ASTM Special Technical Publication 942*, pp. 588-610, 1987.

[84] Subrahmanyan, R., Wilcox, J. R., Li, C.-Y., A Damage Integral Approach to Thermal Fatigue of Solder joints, *IEEE Transactions Components Hybrids and Manufacturing Technology* vol. 12, pp. 480-491, 1989.

[85] Xunqing, S., Qianjin, Y., Zhiping, W., Dongji, X., Zhaofeng, S., New Creep Constitutive Relationship and Modified Energy-based Life Prediction Model

for Eutectic Alloys, Singapore Institute of Manufacturing and Technology, 2001.

[86] Darveaux, R., Banerji, K., Constitutive Relations for Tin-Based Solder joints, *44th Electronic Component and Technology Conference*, San Diego, USA, pp. 538-551, 1992.

[87] Coffin, L. F., Fatigue at High Temperature, Fatigue at Elevated Temperatures, *ASTM STP 520, American Soceity for Testing and Materials,* pp. 5-34, 1973.

[88] Manson, S. S., *Thermal Stress and Low Cycle Fatigue*. McGraw-Hill, New York, USA, 1966.

[89] Salmela, O., Andersson, K., Perttula, A., Sarkka, J., Tammenmaa, M., Re-calibration of Engelmaier's Model for Leadless, Lead-free Solder Attachments, *Quality and Reliability Engineering International,* vol. 23, pp. 415-429, 2006.

[90] Whalley, D. C., Chambers, D. J., Evaluation of SMD Solder Joints Using Finite Element Analysis, *7th European Hybrid Microelectronics Conference*, Hamburg, Germany, 1989.

[91] Gonzalez, M., Vandevelde, B., Beyne, E., Thermo-Mechanical Analysis of a Chip Scale Package (CSP) Using Lead-Free and Lead Containing Solder Materials, *iMAPS, Europe,* , Prague, Czech Republic, pp. 247-252, 2004.

[92] Pang, J. H. L., Chong, D. Y. R. , Flip Chip on Board Solder Joint Reliability Analysis Using 2-D and 3-D FEA Models, *IEEE Transactions on Advanced Packaging,* vol. 24, pp. 499-506, 2001.

[93] Zhang, L., Sitaraman, R., Patwardhan V., Nguyen, L., Kelkar, N., Solder Joint Reliability Model with Modified Darveaux's Equations for the Micro SMD Wafer Level-Chip Scale Package Family, *53rd Electronic Components and Technology Conference*, New-Orleans, USA, pp. 572-577, 2003.

[94] Pang, J. H. L., Seetoh, C. W., Wang, Z. P., CBGA Solder Joint Reliability Evaluation Based on Elastic-Plastic-Creep Analysis, *Journal of Electronic Packaging,* vol. 122, pp. 255-261, 2000.

[95] Lau, J. H., Pan, S. H., Creep Behaviors of Flip Chip on Board With 96.5Sn-3.5Ag and 100In Lead-Free Solder Joints, *The International Journal of Microcircuits and Electronic Packaging,* vol. 24, pp. 11-18, 2001.

[96] Tang, H., Basaran, C., A Damage Mechanics-Based Fatigue Life Prediction Model for Solder Joints, *Journal of Electronic Packaging,* vol. 125, pp. 120-125, 2003.

[97] Vandevelde, B., Gonzalez, M., Limaye, P., Ratchev, P., Beyne, E., Thermal Cycling Reliability of SnAgCu and SnPb Solder Joints: A Comparison for Several IC-Packages, *Microelectronics Reliability,* vol. 47, pp. 259-265, 2007.

[98] Kimura, S., Shimoyama, K., Yoneda, N., Nakao, K., Method of Producing a Chip Resistor, U. S. Patent, Matsushita Electric industrial Co. Ltd., Japan, 2001.

[99] Panasonic web page "www. Panasonic.com".

[100] Operating Manual, THERMO SENSORIK, GmbH, Germany.

[101] Holman, J. P., *Heat Transfer*, McGraw-Hill, London, UK, 1981.

[102] Fink, D. G., Beaty, H. W., *Standard Handbook for Electrical Engineers*, McGraw Hill, New York, USA, 1978.

[103] *Standard Test Methods for Calibration of Thermocouples by Comparison Techniques*, ASTM E220-86, West Conshohocken, USA, 1996.

[104] Cook, R. D., Malkus, D. S., Plesha, M. E., Witt, R. J., *Concepts and Applications of Finite Element Analysis*. John Wiley & Sons, New York, USA, 2002.

[105] *ANSYS Element Reference Manual*, Swanson Analysis System, Inc., Houston, USA.

[106] Siewert, T., Liu, S., Smith, D. R., Madeni, J. C., *Database for Solder Properties with Emphasis on New Lead-free Solders*, National Institute of Standards and Technology & Colorado School of Mines, Colorado, USA 2002.

[107] Zhou, T., Hundt, M., Villa, C., Bond, R., Lao, T., Thermal Study for Flip Chip on FR4 Boards, *47th Electronic Components and Technology Conference*, San Jose, USA, 1997.

[108] Qiang, X., Nguyen, L., Armstrong, W. D., Aging and Creep Behaviour of Sn3.9Ag0.6Cu Solder Alloy, *54th Electronic Components and Technology Conference*, Las Vegas, USA, pp. 1325-1332, 2004.

[109] Telang, A. U., Bieler, T. R., Orientation Imaging Microscopy of Lead-Free Sn-Ag Solder Joints, *Journal of the Minerals, Metals and Materials Society*, vol. 57, pp. 44-49, 2005.

[110] LaLonde, A., Emelander, D., Jeannette, J., Larson, C., Rietz, W., Swenson, D., Henderson, D. W., Quantitative Metallography of -Sn Dendrites in Sn-3.8Ag-0.7Cu Ball Grid Array Solder Balls via Electron Backscatter Diffraction

and Polarized Light Microscopy, *Journal of Electronic Materials,* vol. 33, pp. 1545-1549, 2004.

[111] Jong, G, *Microstructural Features and Mechanical Bahaviour of Lead Free Solders*, PhD Thesis, Loughborough University, Loughborough, UK, 2007.

[112] Saxton, H. J., West, A. J., Barrett, C. R., Deformation and Failure of Brazed Joints-Macroscopic Considerations, *Metallurgical Transactions,* vol. 2, pp. 999-1007, 1971.

[113] Zimprich, P., Betzwar-Kotas, A., Khatobo, G., Weiss, B., Ipser, H., Size effect in Small Scaled Lead-free Solder Joints, *Journal of Material Science,* vol. 19, pp. 383-388, 2008.

[114] West, A. J., Saxton, H. J., Tetelman, A. S., Barrett, C. R., Deformation and Failure of Thin Brazed Joints-Microscopic Considerations, *Metallurgical Transactions,* vol. 2, pp. 1009-1017, 1971.

[115] *Instron Help Manuals*, Instron, USA.

[116] Material property database: "www.matweb.com".

[117] Standard Practice for Probability Sampling of Materials, ASTM E 105-58, West Conshohocken, USA,1996.

[118] *Joint Industry Standard: Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*, IPC/JEDEC J-STD-020C, 2004.

[119] *Standard Test Methods for Tension Testing of Metallic Materials*, ASTM Standard E 8-04, West Conshohocken, USA, 2004.

[120] Socie, D. F., Marquis, G. B., *Multiaxial Fatigue*, Society of Automotive Engineers, Warrendale, USA, 2000.

[121] Ochoa, F., Deng, X., Chawla, N., Effects of Cooling Rate on Creep Behavior of a Sn-3.5Ag alloy, *Jornal of Electronic Materials,* vol. 33, pp. 1596-1607, 2004.

[122] Yeung, B., Jang, J-W., Correlation between Mechanical Tensile Properties and Microstructure of Eutectic Sn-3.5Ag solder, *Journal of Materials Science Letters,* vol. 21, pp. 723-726, 2002.

[123] Wiese, S., Meusel, E., Wolter, K.J., Microstructural Dependence of Constitutive Properties of Eutectic SnAg and SnAgCu Solders, *53rd Electronic Components and Technology Conference*, New Orleans, USA, pp. 197-206, 2003.

[124] Toux, T. L., Dusek, M., Hunt, C., *The Effect of Temperature on Microstructure of Lead-free Solder Joints*, NPL Report MATC(A) 157, Teddington, UK, 2003.

[125] Liu, C. Z., Chen, J., Nanoindentation of Lead-Free Solders in Microelectronic Packaging, *Materials Science and Engineering,* vol. A 448, pp. 340-344, 2007.

[126] Pang, J. H. L., Xiong, B. S., Mechanical Properties for 95.5Sn-3.8Ag-0.7Cu Lead-Free Solder Alloy, *IEEE Transactions on Components and Packaging Technologies*, pp. 830-840, 2005.

[127] Qiang, W., Lihua, L., Xuefan, C. and Xiaohong, W., Experimental Determination and Modification of Anand Model Constants for Pb-free Material 95.5Sn4.0Ag0.5Cu, *Proc. 8th Int. Conf. on Thermal, Mechanical and Multiphysics Simulation and Experiments in Micro-Electronics and Micro-Systems, EuroSimE*, London, UK, pp. 308-316, 2007.

[128] Pang, J. H. L., Xiong, B. S., Low, T. H., Creep and Fatigue Characterization of Lead Free 95.5Sn3.8Ag0.7Cu Solder, *54th Electronic Components and Technology Conference*, Las Vegas, USA, pp. 1333-1337, 2004.

[129] Dusek, M., Hunt, C., Measurement of Material Properties of Lead-free Solders for Modelling Requirements, *SMTA International Conference*, Chicago, USA, 2003.

[130] Morris, J. W., Song, H. G., Hua, F., Creep Properties of Sn-rich Solder Joints, *53rd Electronic Components and Technology Conference*, New-Orleans, USA, pp. 54-57, 2003.

[131] Hwang, J. S., Lead-Free Solder: the Sn/Ag/Cu System, *Surface Mount Technology,* pp. 18-21, 2000.

[132] Xu, L., Pang, J. H. L., Nanoindentation on SnAgCu Lead-free Solder Joints and Analysis, *Journal of Electronic Materials,* vol. 35, pp. 2107-2115, 2006.

[133] *ANSYS Theory Reference Manual*, Swanson Analysis System, Inc., Houston, USA, 2000.

[134] Chong, C. W., Xiaowu, Z. T., Chai, T. C., Board Level Solder Joint Life Prediction of Fine Pitch Large IC, *Electronics Packaging Technology Conference*, Singapore, pp. 302-306, 2006.

[135] Geffroy, P. -M., Mathias, J. -D., Silvain, J. -F., Heat Sink Material Selection in Electronic Devices by Computational Approach, *Advanced Engineering Materials,* vol. 10, pp. 400-405, 2008.

[136] Pang, J. H. L., Xiong, B. S., Low, T. H., Low Cycle Fatigue Models for Lead-Free Solders, *Thin Solid Films,* vol. 462-463, pp. 408-412, 2004.

Appendix 1: Load Levels and Creep Constant Estimation

A. Tensile creep test of small-scale solder joint

Average width (W) = 10.5 mm

Thickness of specimen (t) = 0.95 mm

Gap (g) = Average of 3 measurements

Area (A) = 9.975 mm^2

Load (P) = Stress (σ) $\times$ Area (A)

Strain in solder joint = $\frac{\delta_s}{g}$

Normal stress (MPa)	Load (N)
20	199.5
25	249.4
30	299.3
35	349.1
40	399.0

B. Shear creep test of small-scale solder joint

Length of solder joint (L) = 7.0 mm

Thickness of specimen (t) = 0.95 mm

Height of solder joint (H_s) = Average of 2 measurements

Area (A) = 6.65 mm^2

Load (P) = Shear stress (τ) $\times$ Area (A)

Shear strain in solder joint = $\frac{\delta_{ext}}{H_s}$

Shear stress (MPa)	Load (N)
0.5	3.3
1.5	10.0
2.5	16.6
3.5	23.2
5.0	33.3

C. Tensile creep test of bulk solder

Width of specimen (W) = 5.0 mm

Thickness of specimen (t) = 2.0 mm

Gauge length (L_g) = 10.0 mm

Area (A) = 10.0 mm^2

Load (P) = Stress (σ) $\times$ Area (A)

Shear strain in solder = $\dfrac{\delta_{ext}}{L_g}$

Normal stress (MPa)	Load (N)
5.0	50.0
10.0	100.0
15.0	150.0
20.0	200.0

D. Procedure for estimation of creep constants

Step 1: Fit an exponential trend line for the steady state strain rate ($\dot{\varepsilon}_s$) vs. stress (σ) graph on a logarithmic scale, which results:

$$\dot{\varepsilon}_s = B_3 e^{A_1 \sigma}$$

Step 2: Assume

$$B_3 = B_1 \exp\left[\frac{-Q}{RT}\right]$$

and

$$A_1 = \beta p$$

Step 3: Assuming the value of Q, the value of B_1 was found.

Step 4: Finally by iterating the values of β and p, a good fit to the experimental steady state strain rate ($\dot{\varepsilon}_s$) vs. stress (σ) was obtained using hyperbolic sine creep law.

ELSEVIER

Available online at www.sciencedirect.com

ScienceDirect

Computational Materials Science 43 (2008) 212–220

COMPUTATIONAL MATERIALS SCIENCE

www.elsevier.com/locate/commatsci

Finite element analysis of lead-free surface mount devices

Pradeep Hegde, Andrew R. Ochana, David. C. Whalley, Vadim. V. Silberschmidt *

Wolfson School of Mechanical and Manufacturing Engineering, Loughborough University, Leicestershire LE11 3TU, UK

Available online 17 September 2007

bstract

Transition to lead-free solder materials has raised concerns over the reliability of lead-free solder joints in the electronic industry. Soler joints provide electrical conduction and mechanical support for components and may operate over temperature extremes of −55 °C) 125 °C or greater. These temperatures are relatively high the melting point of the solder. A mismatch between coefficients of thermal xpansion of the component, solder and substrate, combined with thermal variations during service, results in thermal fatigue that is a ommon failure mechanism for solder joints in electronic products. So far most of the studies of this issue have considered uniform temerature distributions in the electronic assembly. The main objective of this paper is to investigate the effect of the experimentally bserved non-uniform temperature distribution in the electronic device on the structural response of solder joints in comparison with iat for a uniform temperature distribution.

) 2007 Elsevier B.V. All rights reserved.

ACS: 65.40.De; 85.40.Bh

eywords: Solder joint; Lead-free; Thermo-mechanical fatigue

. Introduction

Over many decades SnPb solder has been successfully sed by the electronic industry. However, the recent ban nposed on the use of lead in electronic devices has raised eliability concerns due to the introduction of considerably ess studied lead-free solders. Thermal stresses occur in a tructure when any portion of thermal expansion or conraction is constrained. Basically, there are two different ets of constraints, under which thermal stresses occur: xternal and internal [1]. Thermal stresses due to external onstraints are obvious. However, the notion of internal onstraints is less clear. A structure made of the material ıay be free to expand and yet have thermal stresses due ɔ a non-uniform temperature distribution. On the other and, a structure comprising components of different mateials can demonstrate thermal stresses even in the case of niform thermal conditions and absence of external constraints due to the difference in levels of coefficients of thermal expansion (CTEs). Usually electronic assemblies are manufactured from a range of materials with varying CTEs [2]. Since these assemblies experience temperature/power changes during their use (e.g. power consumption; switching equipment on/off; day/night temperature changes), the CTEs mismatch causes stresses in the assembly, which may then result in creep and stress relaxation with time.

The principle reliability hazard for surface mounting technology in microelectronics is fatigue cracking of the solder joints, caused by cyclic thermal stresses. Fig. 1 demonstrates a crack in a solder fillet caused by thermal cycling. Under service conditions, these devices may be subjected to a cyclic temperature range from −55 °C to 125 °C or more depending on their application. Under such cyclic thermal loading, stresses due to the thermal-expansion mismatches are difficult to avoid. Even with matched levels of CTEs there is a possibility for stress initiation in the package due to the spatial temperature variations in the assembly. In many designs the imposed stresses exceed the elastic limit of the solder and produce plastic deformation. Under these conditions eventual failure by

* Corresponding author. Tel.: +44 1509 227504; fax: +44 1509 227502. *E-mail address:* v.silberschmidt@lboro.ac.uk (Vadim. V. Silberschıidt).

927-0256/$ - see front matter © 2007 Elsevier B.V. All rights reserved.
oi:10.1016/j.commatsci.2007.07.046

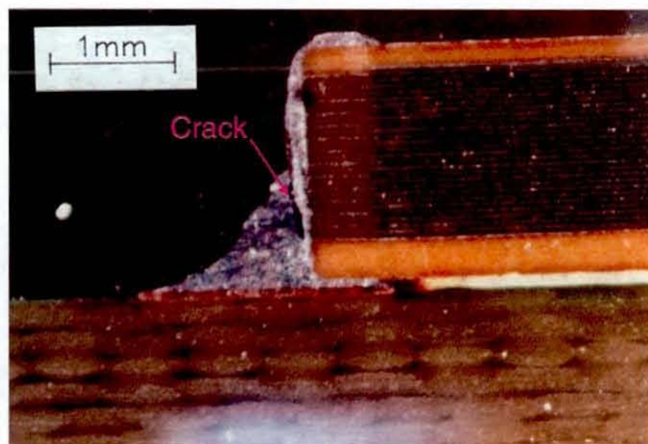


Fig. 1. Solder fillet cracking in −55 to +125 °C test on 1812 size ceramic capacitors.

low cycle fatigue can be expected. The fatigue lifetime, which is required in service, typically considerably exceeds the duration of reliability tests. This means that service reliability must be estimated using some sort of extrapolation. The situation becomes complex because of the relatively high temperatures involved. Low cycle fatigue at more than half the melting point of the solder will involve creep-fatigue interactions. Under these conditions, the number of cycles to failure depends on the cycle frequency and on the shape of a stress cycle [3].

Experimental evaluation of fatigue life consumes a considerable amount of time and is also expensive. Therefore, finite element analysis plays an important role in estimation of durability of solder joints. Within the framework of this approach a mathematical model is built, which incorporates both the constitutive equations and the actual geometry and different loading conditions can be simulated. So far, most of the finite element analyses in electronic assemblies have been conducted considering the spatially uniform thermal cycling, e.g. finite element simulation study of 5 × 4 chip scale packages (CSP) and flip chip solder joint reliability under isothermal cycling [4–6]. In this paper the effect of non-uniform temperature distribution on the structural behaviour of solder joints in a surface mount device is studied and compared with that of uniform thermal cycling.

2. Experimental procedure

A series of experiments were carried out to acquire the temperature distribution in an electronic assembly for power cycling condition, using an infrared (IR) Thermosensorik camera. It measures thermal radiation from the surface, which has a wavelength spectrum dependent on the temperature, structure and composition of the surface. The higher the temperature, the more radiation is emitted. This infrared radiation, not perceptible with naked eye, is made visible and measurable by infrared cameras. Analysing the infrared radiation it is possible to measure temperature as well as thermal conductivity, mechanical stress, material composition, defects and various kinds of inhomogeneities in the materials. IR-measuring technology is contactless and non-destructive and supplies information with a spatial and temporal resolution that is not achievable with other measuring techniques.

The Thermosensorik IR camera consists of a central processing unit with software and an IR detector head with a focal plane array (FPA) detector sensitive in the range 1–14 μm. An infrared microscopic lens MWIR 2.5×, with a focus distance of 21–22 mm was used for this experiment. The camera is interfaced with software to control real-time acquisition and analysis of the infrared data.

The specimens used were identical flip chip assemblies attached to either a copper or FR4 substrate. They were placed in a wind tunnel where they were subjected to either 0.4 W or 1.2 W power levels. They were also cooled by either free or forced convection (airflow rates of 5, 10 and 15 m/s were used).

2.1. Specimen description

The flip chip specimens were silicon-on-silicon multichip modules (MCMs) that matched the description of those used in a previous experiment [7]. Both MCMs consisted of a 3 mm × 3 mm × 0.5 mm *"heater"* chip that bore a large central resistive element (the heater) in addition to small aluminium tracks and 36 connection pads. The *"carrier"* chip was larger at 6 mm × 6 mm × 0.5 mm that included larger ball grid array pads allowing for external connections to be made, as well as the corresponding pads to match those on the heater chip. The heater chip was attached to the carrier chip so that a standoff height of 35 μm was achieved (without underfill). The MCMs were subsequently attached to the corresponding substrate by a thermally conductive adhesive pad. A schematic of the assembled specimen is shown in Fig. 2.

2.2. Experimental set up

The experimental setup consists of a thermal camera, fitted with the micro lens, is mounted on the tripod, the specimen is powered on for a few minutes to stabilise the temperature distribution in the specimen, then micro lens

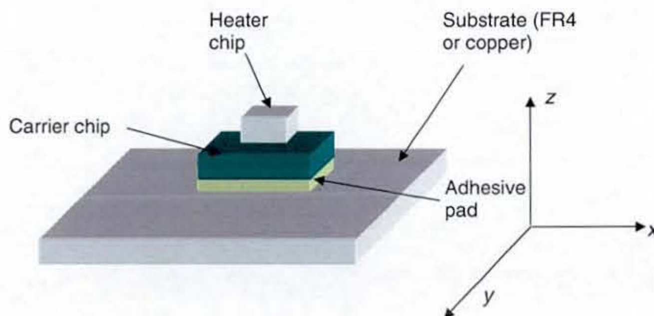


Fig. 2. Schematic of the flip chip specimens used.

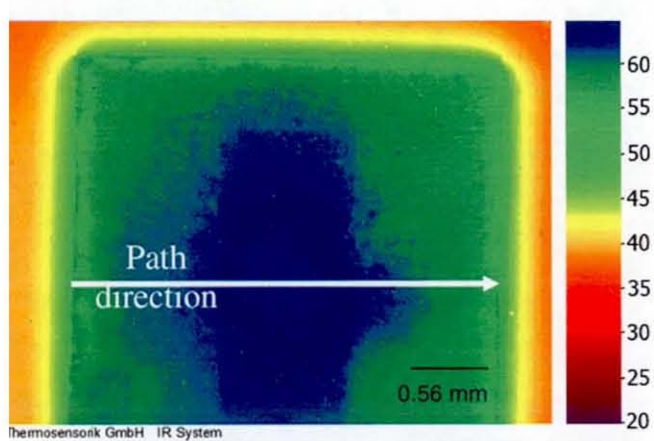
focused on the specimen and the temperature profile is ıptured.

3. Results and discussion

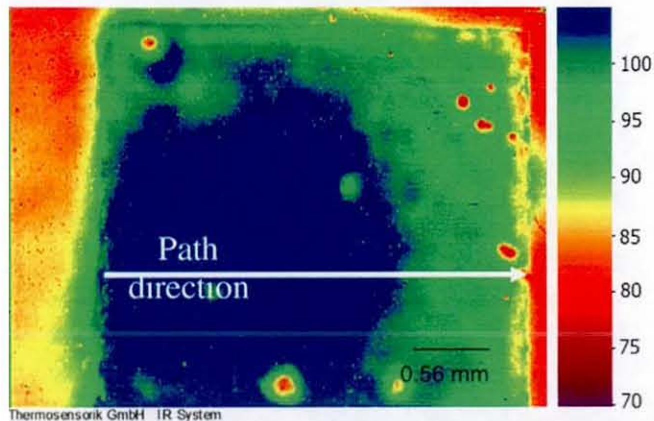
3.1. Free convection

The temperature distributions over the chip for 1.2 W ɔwer cycles are given in Figs. 3 and 4 for free convection; ıe path, which is used for temperature distribution analy-s, is also shown. These figures demonstrate the effect of ıe substrate on temperature distributions in the chip: the ɔpper substrate causes lower temperatures compared to ıe FR4 substrate.

Fig. 5 shows the temperature distribution cross the idth of the chip for both types of substrate. It is evident ıat these temperature distributions are non-uniform: the ıaximum temperature is observed at the centre of the chip, here there is a lower thermal mass, while its boundary has ıwer temperature. Another important result of this analy-s is that the FR4 substrate induces higher thermal gradi-ıts in the chip than copper substrate. This can be ‹plained by higher thermal conductivity of copper than R4.



ig. 3. Temperature distribution in chip with copper substrate for power ɪcle 1.2 W.



ig. 4. Temperature distribution in chip with FR4 substrate for power ɪcle 1.2 W.

2.3.2. Forced convection

Figs. 6 and 7 show temperature distributions in the chip for copper and FR4 substrates, respectively, under forced convection 5 m/s. Forced convection can be seen to reduce the temperatures in the chip by increasing the heat transfer

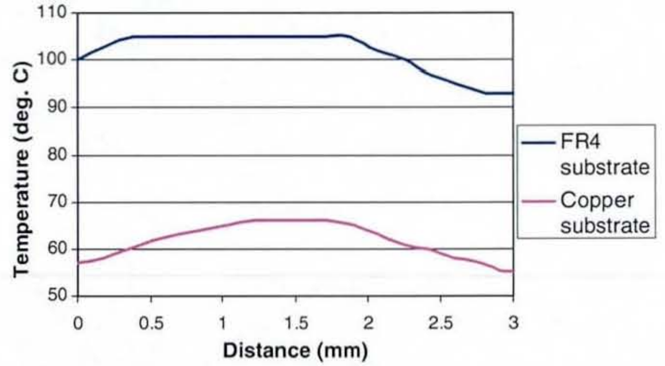


Fig. 5. Effect of substrate on temperature distribution in the chip for free convection.

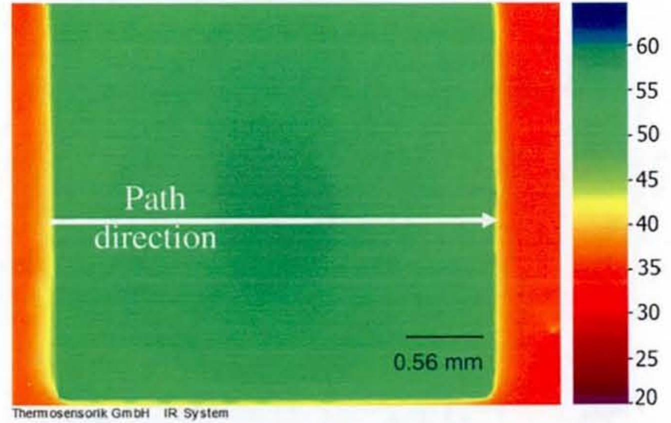


Fig. 6. Temperature distribution in chip with copper substrate for power cycle 1.2 W and forced convection 5 m/s.

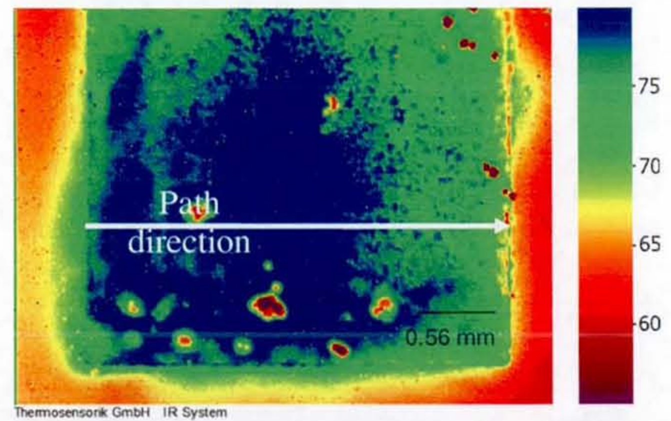


Fig. 7. Temperature distribution in chip with FR4 substrate for power cycle 1.2 W and forced convection 5 m/s.

rate. Similar experiments were carried out for forced convection at levels of 10 m/s and 15 m/s.

So, the experiments vividly show that the temperature distribution in a power dissipating electronic assembly is non-uniform. They justify the necessity to study the structural response of solder joints and assemblies for cases where there is a non-uniform temperature distribution. Even though the experiments are carried out only for flip chip specimens, similar temperature distributions can be expected to occur in assemblies manufactured using other packaging techniques (BGA, SMT etc.) due to the comparable thermal mass distribution (more thermal mass at the boundary than the centre of the chip). The thermal data, used below in finite element simulations of surface mount resistor, is based on these experiments (see Figs. 8 and 9).

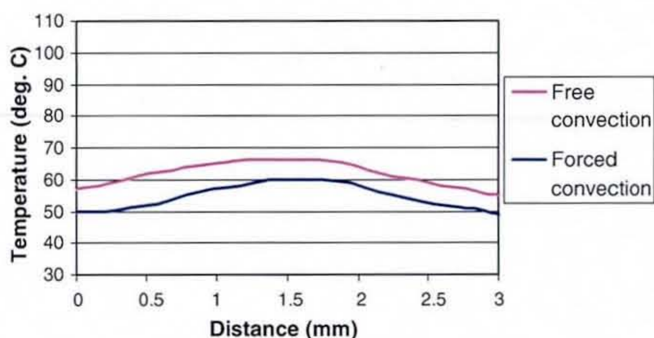


Fig. 8. Temperature distributions in chip with copper substrate for free and forced convection.

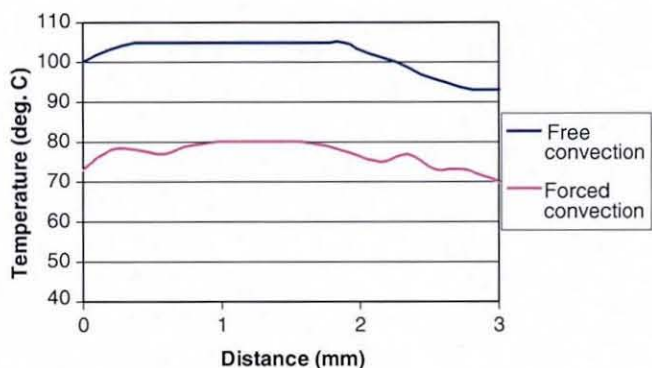


Fig. 9. Temperature distributions in chip with FR4 substrate for free and forced convection.

3. Finite element analysis

3.1. Geometry

The reliability of surface mounted devices (SMDs) has been extensively analysed by means of finite element simulations. Surface mounting is the technique of attaching components directly to a substrate without the through-hole leads of a more conventional technology. The origins of this technique have been traced to 1952, but it is only in recent years that advances in robotics have allowed mass production, based on it [8]. The geometry of a 1206 resistor has been here used to study the effect of non-uniform temperature distributions on the structural response. The geometric dimensions of different components of this resistor assembly are shown in Fig. 10. In this finite element study only one half of the resistor assembly is modelled thanks to its symmetry.

The commercial FEA software ANSYS was used for both finite element modeling and analysis. A 2D model was built using PLANE 182 element type, which is a 2D plane stress with thickness element. A 3D finite element model with hexahedral elements was also used in simulation to study specific feature of a 3D stress distribution. A fine mesh pattern is maintained in and around the solder joint – a critical area – to accurately capture variations in the stress level. Finite element models with detailed views of the critical area are presented in Figs. 11 and 12.

3.2. Material properties

Temperature-dependent material properties are used in the FEA. The component is modelled with properties of alumina (Al_2O_3), while the material data given in Table 1. for as-cast SnAgCu is used for solder joint, and high-conductivity copper is considered for the pad. The data

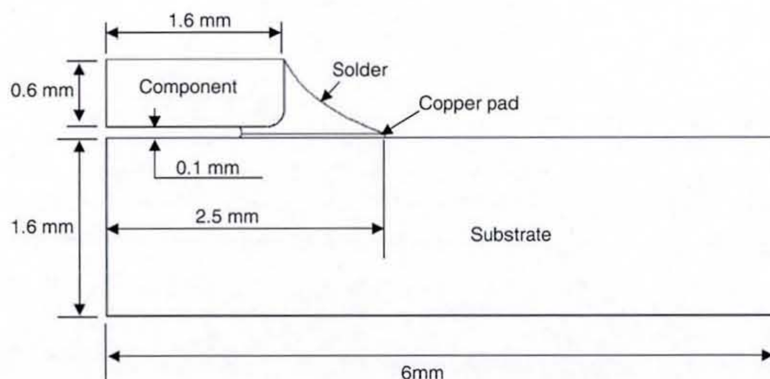


Fig. 10. Geometry of 1206 surface mount resistor.

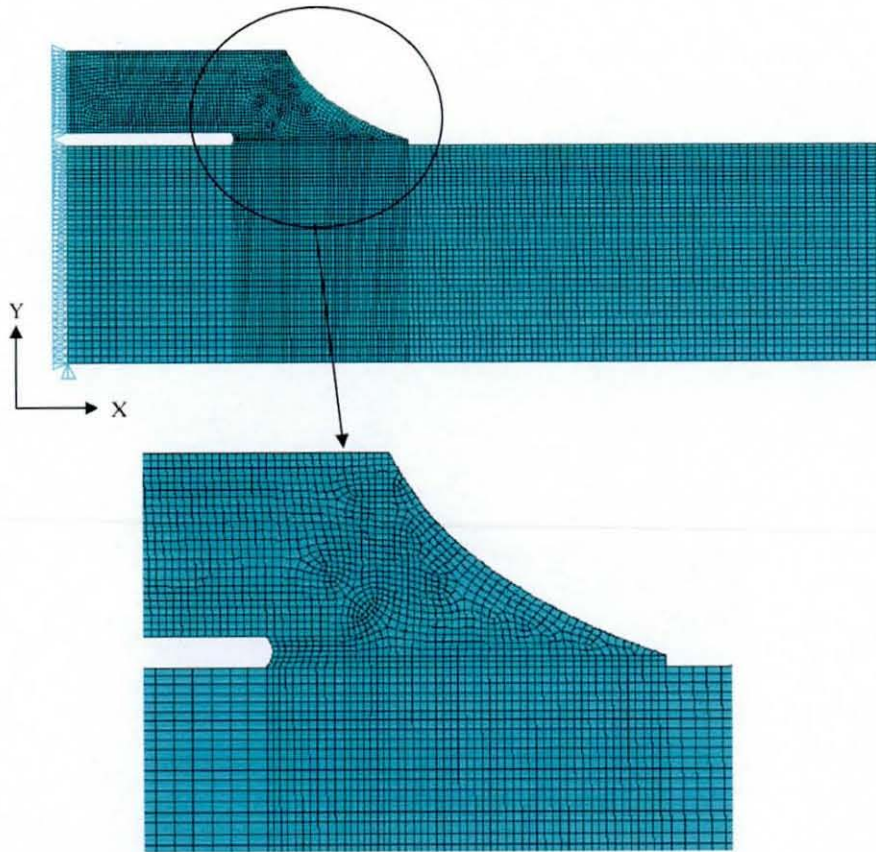


Fig. 11. 2D finite-element model of a 1206 resistor assembly.

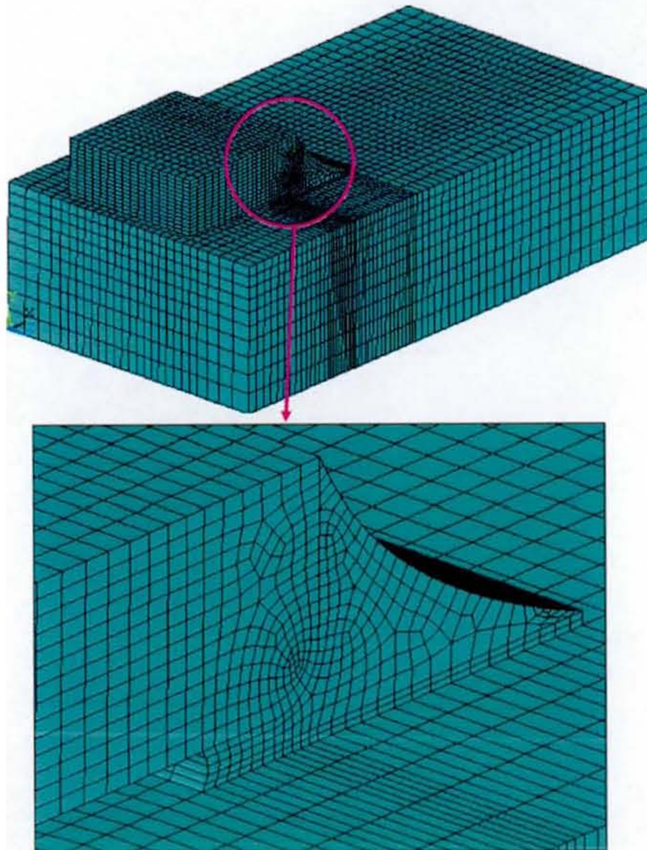


Fig. 12. 3D finite-element model of a 1206 resistor assembly.

for FR4 substrate is taken from [9,10]. The elasto-plastic analysis is carried out considering bilinear kinematic hardening (BKIN) model, which includes the Bauschinger effect due to thermal cycling.

3.3. Loads and boundary conditions

Since most chip resistors fail due to thermo-mechanical fatigue, only a thermal load is considered for FEA. The FE study was carried out considering three different thermal loading conditions in two steps. In the first step, elastic analysis was carried out to identify the limiting temperature at which stress levels in solder joint reach the yield limit. Secondly, an elasto-plastic analysis was performed to estimate the residual stress induced in the solder joint during cooling from reflow soldering temperature as well as inelastic strains due to thermal cycling, and to compare stresses and plastic strains for three different types of thermal cycling. The following three cases of thermal loads were used:

- Case A: Uniform temperatures ranging from +125 °C to −55 °C, where the entire resistor assembly is subjected to the same temperature.
- Case B: Uniform temperature for the component, solder joint and copper pad ranges from +125 °C to −55 °C, and the substrate's temperature (T_{sub}) varies according to the following relation:

Table 1
Material properties of SnAgCu

Temperature (°C)	Young's Modulus (MPa)	Yield Stress (MPa)	Hardening Modulus (MPa)	Poisson's ratio	CTE (ppm/°C)	Density (gm/cm³)
−50	57,300	45	5650	0.4	12.7	7.5
−25	55,800	41	5400	0.4	12.7	7.5
25	52,600	32	5200	0.4	21.2	7.5
75	49,300	21	4800	0.4	21.7	7.5
125	45,800	13	4450	0.4	23.0	7.5

$$T_{sub} = 0.18^{*}T_{comp} + 26.371, \quad (1)$$

where T_{comp} is the component's temperature.The substrate material is FR4, and Eq. (1) for temperature on the substrate is derived from the experimental data, described in the previous Section.

- Case C: In this case the temperature gradient in the whole assembly is considered. The gradient is obtained from the thermal analysis, for which temperature boundary conditions are derived from the experimental data. The following thermal boundary conditions are used for different zones, as shown in Fig. 13, for this thermal analysis:
- Zone 1: The temperature varies from +125 °C to −55 °C.
- Zone 2: This temperature boundary condition depends on temperature in Zone 1 boundary condition. The respective relationship is derived based on the experimental results for a specimen with a FR4 substrate and free-convection condition.

$$T_2 = 0.87^{*}T_1 + 4.7, \quad (2)$$

where, T_1 and T_2 are the temperatures of Zone 1 and Zone 2, respectively.

- Zone 3: The temperature in this zone, which is in the substrate, varies according to Eq. (1). The temperature gradient in the resistor depends on the temperature in Zone 1, which controls temperatures in Zone 2 and Zone 3. Thermal analysis is carried out for different temperature levels for Zone 1 to obtain the thermal data that is used in structural analysis. The thermal load history and time steps used in elasto-plastic analysis are shown in Fig. 14.

The symmetry boundary condition and single node constraint on the symmetry plane were used for restraining the rigid body motion in the X and Y directions, respectively.

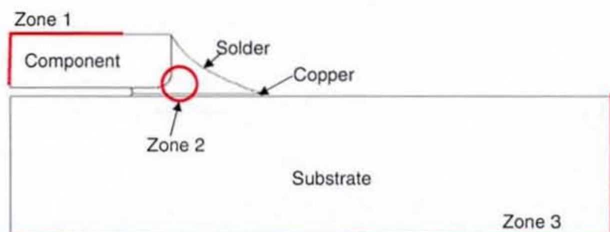


Fig. 13. Thermal zones of 1206 resistor.

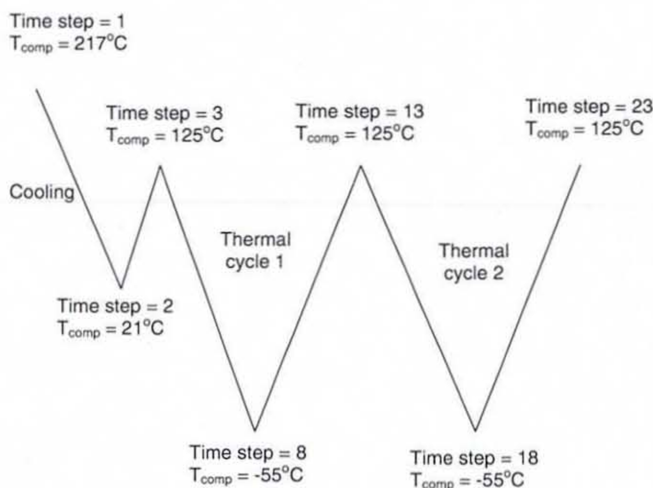


Fig. 14. Thermal load history and time step.

4. Results and discussion

4.1. Elastic analysis

A purely elastic finite-element analysis was performed for a component under thermal loading in the range from +125 °C to −55 °C to understand the level of stress induced in the solder joint and to estimate the area of applicability of this type of analysis. Plots of the equivalent stresses are presented for only one temperature step. Fig. 15 shows the distribution of equivalent stresses in the solder joint for three different thermal load cases when the component's temperature is +125 °C. It is evident that Case C results in lower stress levels than the other two cases. The difference in the maximum equivalent stress between cases B and C is significantly higher than that between cases A and C. Also there is a shift in the maximum stress location from case A to cases B and C. Similar observations are drawn for the case $T_{comp} = -55$ °C. The variation of the equivalent stress in the solder joint with temperature is studied for a single node (Node 551, Fig. 16(a)), located at the point with the maximum equivalent stress in case A. The obtained results (Fig. 16(b)) obviously demonstrate that the thermal load of Case C induces lower stresses in the solder joint compared to other two cases, with Case A resulting in the highest stress. The reason for this is that, in Case A the whole assembly is sub-

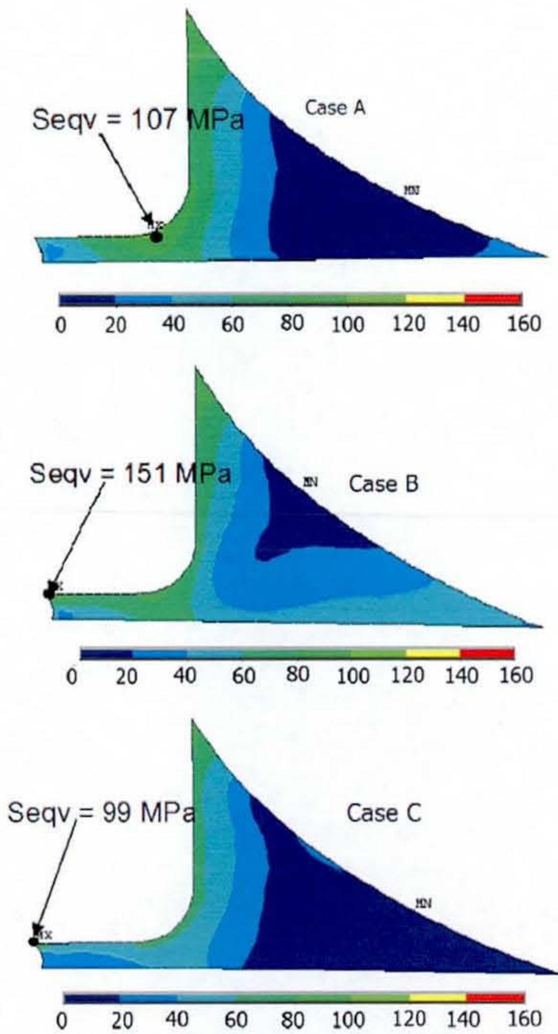


Fig. 15. Equivalent stresses (MPa) in solder joint (T_{comp} = 125 °C).

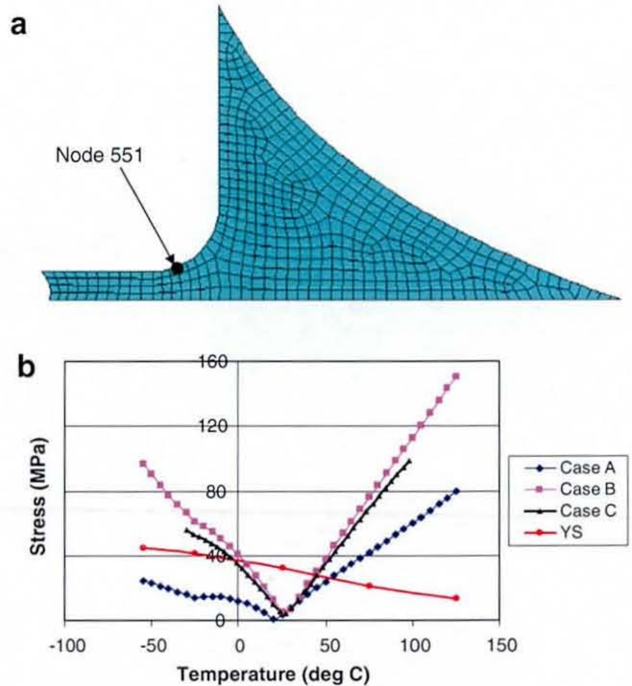


Fig. 16. Location of Node 551 (a) and evolution of equivalent stress with in this node (b).

ɔcted to the same temperature leading to its higher global leformation. On the other hand, case B and case C have ɔwer global deformation due to a low substrate tempera-ure and temperature gradient, respectively. The maximum quivalent stress is observed in the solder joint, when the omponent is at +125 °C for all three cases. The yield stress ne for the solder (denoted YS in Fig. 16(b)) is used to find ut the limiting temperature of the onset of plastic flow in he solder joint. In Case A 45 °C and −25 °C are limiting emperatures, while for cases B and C it is 50 °C.

.2. Elasto-plastic analysis

From this elastic stress analysis it is evident that ther-nally induced stresses in the solder joint exceed the elastic imit after a certain temperature excursion and confirms hat a non-linear analysis is required. Before subjecting he resistor assembly to thermal cycling, the reflow process vas simulated in order to determine the level of residual tresses induced in the solder joint by it. These manufactur-ing-induced stresses were then used as the initial stress state for the resistor assembly when subjected to two thermal cycles to study the evolution of plastic strains in the solder for the three different thermal load cases.

Fig. 17 shows the predicted distribution of residual equivalent stresses in the solder joint after cooling from the reflow temperature (217 °C, i.e. melting point of the solder) for both 2D and 3D elasto-plastic analysis. The solder fillet, area of stress concentration, is the location of the maximum residual stress. From comparison of these two elasto-plastic analyses, a location of the maximum equivalent stress is found to be the same but the obtained magnitude in the 3D analysis is 20% higher than that in the 2D stress analysis. Distributions of the maximum and minimum principal stresses are shown in Figs. 18 and 19, the maximum principal stress is dominant in the location of maximum equivalent stress. A comparison of the equivalent stress in cases of 2D and 3D simulations is performed for the entire thermal cycling with Case A thermal loading. Fig. 20 shows the variation for 2D and 3D stress for reflow and subsequent thermal cycles at the maximum residual stress's location. The equivalent stress variation is similar for both 2D and 3D analysis, with the difference in magnitude between them up to 8%. This study indicates that 2D finite element model provides a good approximation for the elasto-plastic analysis. Therefore, the 2D finite element model was used for remaining two thermal loading cases.

The reflow process also results in very high plastic deformation in the solder joint. The structural response of the solder joint to successive thermal cycles is presented in Fig. 21. The obtained results indicate that the stress and

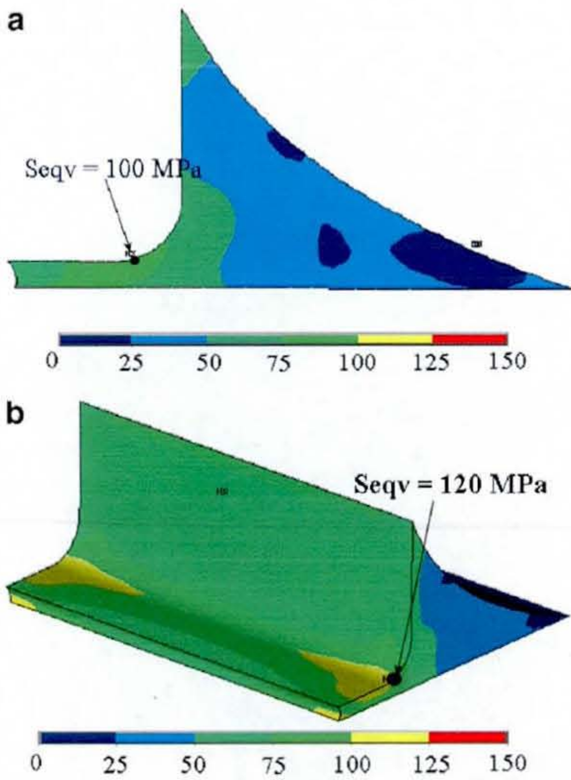


Fig. 17. Residual equivalent stress (MPa) in solder joint after reflow: (a) 2D simulations, (b) 3D simulations.

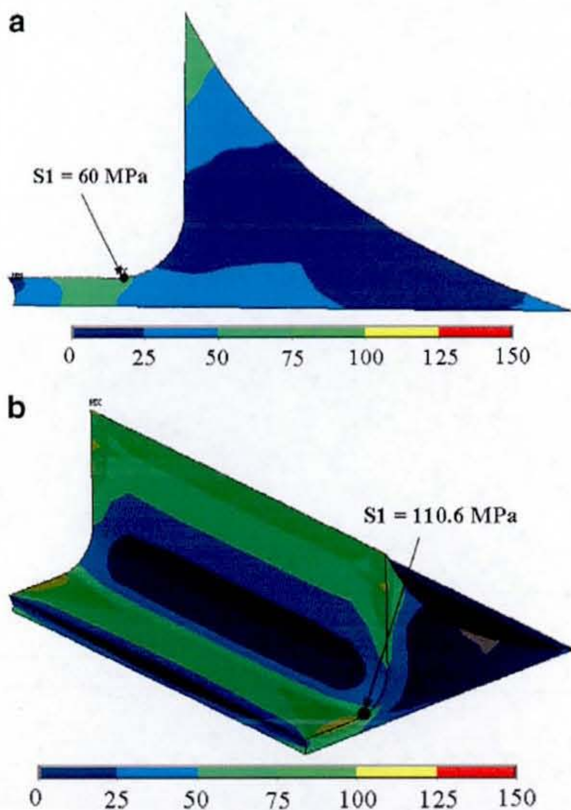


Fig. 18. Residual maximum principal stress (MPa) in solder joint after reflow: (a) 2D simulations, (b) 3D simulations.

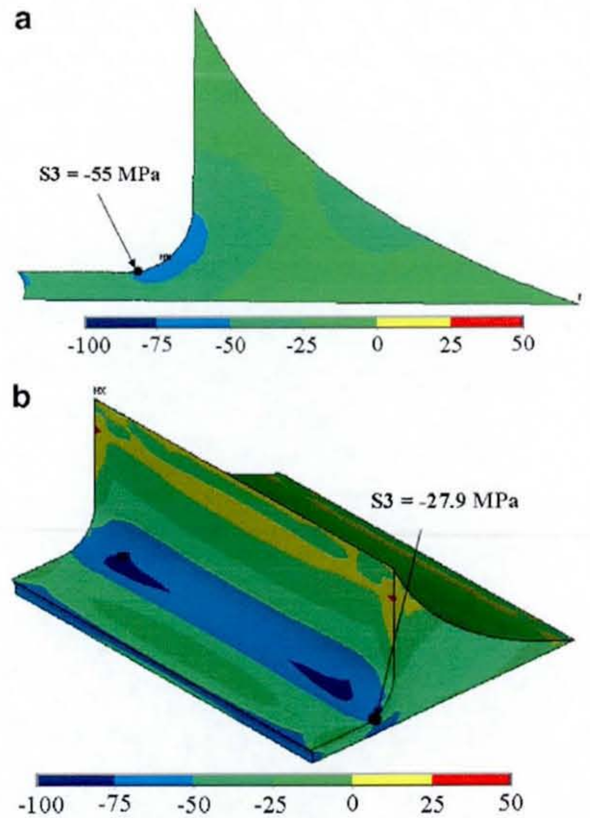


Fig. 19. Residual minimum principal stress (MPa) in solder joint after reflow: (a) 2D simulations, (b) 3D simulations.

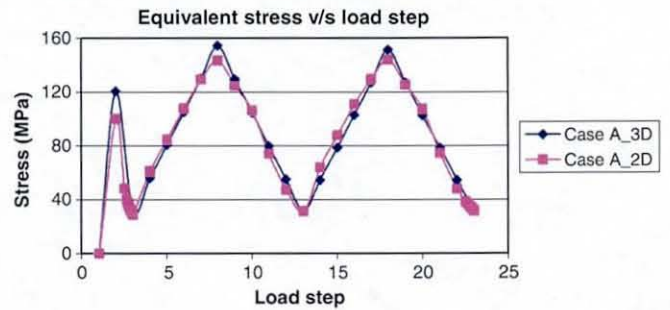
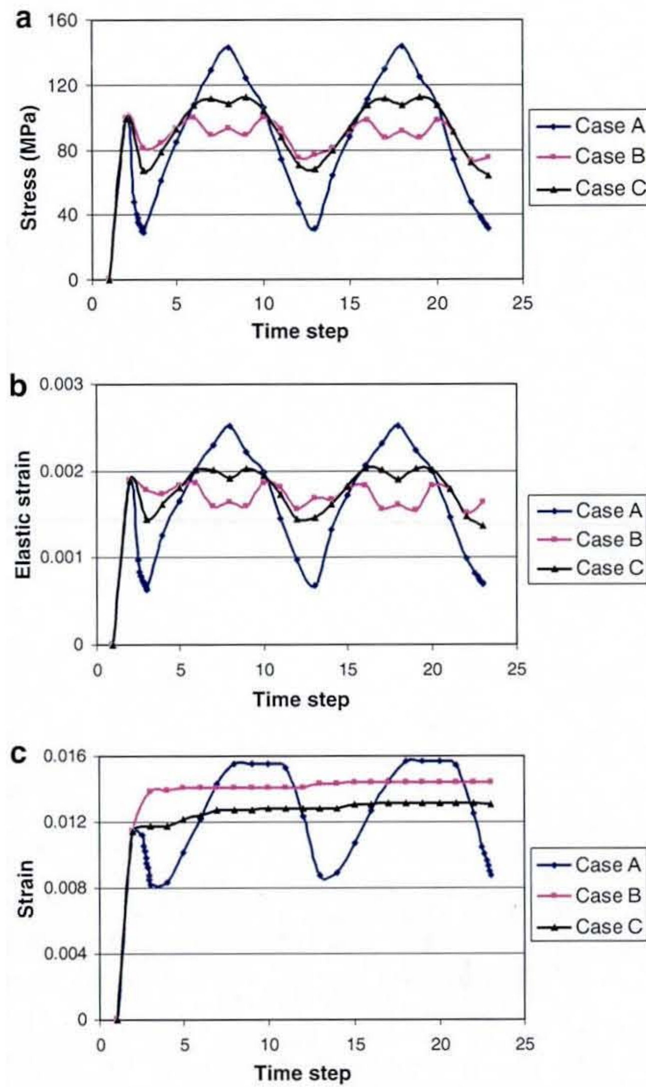


Fig. 20. Comparison of evolution of equivalent stress between 2D and 3D stress analysis.

strain ranges are constant for conditions of purely thermal cycling. In Case A the maximum stress range per cycle is induced, compared to the other two cases, while case B results in the minimum stress range, which is about 6.4 and 2.5 times smaller than that of Case A and C, respectively. Similarly, the elastic strain range per cycle is maximal for Case A and minimal for Case B. However, the range of equivalent plastic strain is quite different: their variations for Case A are similar to those of the equivalent stress/elastic strain and repeat with every thermal cycle. On the other hand, the levels of equivalent plastic strain for Cases B and C remain constant as, indicated in Fig. 21(c). Unlike Case A, Cases B and C show the increase



ig. 21. Evolution of equivalent stress (a), equivalent elastic strain (b) and quivalent plastic strain (c) with thermal cycling.

n the equivalent plastic strain despite the decrease in the tress level from residual stress state at the early stage of he first thermal cycle. This is due to the drastic decrease n the yield stress under heating from room temperature o +125 °C. It is obvious that the thermal loads of Case A and C lead to maximum and minimum equivalent plastic train in the solder joint. There is 8 and 16% decrease in the naximum plastic strain attained in thermal load Case B nd C, respectively, compared to Case A.

5. Conclusions

This finite element study of a surface mount resistor under non-uniform temperature loads allows us to draw the following conclusions:

Elastic and elasto-plastic finite-element studies show that the non-uniform temperature distribution in the electronic assembly causes different responses of the solder joint to thermal cycling.

From the three studied cases, Case C (non-uniform thermal loads in the assembly) predicts lower plastic strain compared to other cases.

It is clear from results of the elasto-plastic analysis that stress/strain range is constant for thermal cycling between +125 °C and −55 °C. The further analysis should incorporate the relaxational effects as well as possible deterioration of material properties due to damage accumulation.

The solder joint has internal residual stresses along with high plastic deformation due to reflow soldering before the start of a thermal cycling. Since solder alloys generally operate at higher homologous temperature, the future work will include the effect of viscous behaviour on solder joints during reflow as well as thermal and power cycling.

References

[1] J.H. Lau, Thermal Stress and Strain in Microelectronics Packaging, Van Nostrand Reinhold, New York, 1993.

[2] M. Dusek, M. Wickham, C. Hunt, Solder. Surf. Mount. Technol. 17 (2005) 22–31.

[3] H.J. Frost, R.T. Howard, IEEE. Trans. Compd. Packag. Technol. 13 (1990) 727–735.

[4] B. Vandevelde, M. Gonzalez, P. Limaye, P. Ratchev, J. Vanfleteren, E. Beyne, Lead Free Solder Joint Reliability Estimation by Finite Element Modeliing Advantages, Challenges and Limitations, IMEC, Leuven, Belgium. IPC 7th international conference on Lead-free electronic components and assemblies, Frankfurt, Germany, October 21–22, 2004.

[5] J.H.L. Pang, D.Y.R. Chong, T.H. Low, IEEE Trans. Compd. Packag. Technol. 24 (2001) 705–712.

[6] D.C. Hillman, Long-term Reliability of Pb-free Electronics, DfR Solutions. http://www.dfrsolutions.com.

[7] A.R. Ochana, D.A. Hutt, D.C. Whalley, F. Sarvar, A. Al-Habaibeh, Modelling of the power cycling performance of a Si on Si flip chip assembly. In: Proceedings of the 10th Intersociety Conference on Thermal and Thermochanical Phenomena in Electronics Systems, ITHERM 2006, San Diego, USA, 30th May 2006, pp. 243–250.

[8] R.F. Bonner, J.A. Asselta, F.W. Haining, IBM J. Res. Dev. 26 (1982) 297–309.

[9] Database for solder properties with emphasis on new lead-free solders http://www.boulder.nist.gov/div853/lead%20free/props01.html.

[10] Matweb material property database, http://www.matweb.com.

Creep Analysis of a Lead-free Surface Mount Device

Pradeep Hegde, David Whalley, Vadim. V. Silberschmidt
Wolfson School of Mechanical and Manufacturing Engineering, Loughborough University, Loughborough, Leicestershire, LE11 3TU, UK

Abstract

In this paper finite element analysis (FEA) is used to understand the effect of a non-uniform temperature distribution on the creep and fatigue behaviour of lead-free solder joints in an electronic assembly comprising of a chip resistor mounted on printed circuit board (PCB). Solder joints in surface mount devices (SMDs) operate over a temperature range as extreme as -55°C to 125°C, which is high compared to the melting temperature of solder alloys. Exposure of solder joints to these temperatures can result in thermo-mechanical fatigue. Eutectic or near- eutectic tin-lead alloys have previously been used as an interconnection material, but the ban imposed on the use of toxic materials in electronic products demands new lead-free solder materials. This paper presents the experiments carried out using a thermal camera to obtain the real temperature distribution in the electronic assembly. These temperature distributions were used in FEA of the chip resistor under temperature cycling conditions. Unlike accelerated tests for obtaining reliability data, FEA is quick and less expensive.

1. Introduction

The environmental impact of lead in electronic products is relatively low, but due to the size of the industry, is becoming a major concern all around the world. The stimulus for the "green movement" is market trend's and customers' perception. Therefore, manufacturers, suppliers and research institutes around the world are investing their efforts into developing lead-free soldering technologies to substitute for tin-lead solder alloys. In addition, researchers are also pondering the pressing need to find a high-performance solder alloy with improved mechanical properties and similar processing characteristics to tin-lead solders [1].

The reliability of lead-free solder joints is still a major concern due to their widespread application in the electronic industry only very recently and therefore there is not a great deal of material data or practical experience available. In this study a near-eutectic lead-free SnAgCu (SAC) solder alloy, with a melting temperature of 217°C, is considered because it is being widely adopted due to its excellent wetting and mechanical properties [2]. When the solder is subjected to a cyclic stress induced by thermal cycling, the reliability of the solder joint depends on its resistance to fatigue. Along with thermo-mechanical fatigue, solder joints are subjected to creep as they operate at high homologous temperatures (T_g, the ratio of absolute operating and melting temperature). In this study a solder joint is subjected to thermal cycles between -55°C and 125°C. This means that they operate between $T_g = 0.44$ and $T_g = 0.81$. It is well documented [3] that creep plays a very important role in deformation behaviour of materials at homologous temperatures close to and above 0.5 if the loading rate is slow enough for creep damage to occur. Since under actual service conditions, the temperature cycle duration is in the order of minutes to days and the homologous temperature is more than 0.5, solder joints formed using SnAgCu alloy are expected to deform primarily due to creep [3]. This is essentially the same as for SnPb solders, but much less is known about the creep fatigue response of Pb free alloys.

Research into the use of finite element analysis (FEA) has been widely carried out to understand the elasto-plastic and creep behaviour of solder joints exposed to uniform (isothermal) temperature cycling conditions [1,3,4,5]. Thermo-mechanical analysis of a chip scale package (CSP) assembled using both lead-free and lead containing solder materials [1] and thermal cycling analysis of flip-chip solder joint reliability [5] are examples. However, experimental studies show that the temperature distribution within an electronic assembly is non-uniform due to different heat dissipation rates in the constituents of the electronic assembly. In addition, the mass distribution within the electronic assembly results in a non-uniform distribution of temperature during rapid changes in ambient temperature or power dissipation. Therefore, this paper focuses on the use of FEA to investigate the effect of a non-uniform temperature distribution on the creep behaviour of SAC solder joints in surface mount devices and a comparison is made with that for an uniform temperature distribution. The finite element analysis is first used to estimate stresses/strains due to cooling from reflow and then three different thermal cycling conditions are applied.

2. Experimental analysis

2.1 Experimental set up

In order to establish an appropriate magnitude for the non-uniform temperature distribution in the electronic assembly, a series of experiments were carried out to acquire the temperature profile in a flip chip assembly under power cycling conditions, using an infrared (IR) camera. Although this flip chip is different to the component (chip resistor) modelled, the general size and interconnection joint distribution makes both flip chip and chip resistor assemblies roughly comparable and means the flip chip experimental results will provide an indication of the temperature gradients to be expected in the chip resistor. The camera measures thermal radiation from the surface, which has a wavelength spectrum and intensity dependent on its temperature, structure and

1-4244-1106-8/07/$25.00 ©2007 IEEE

8th. Int. Conf. on Thermal, Mechanical and Multiphysics Simulation and Experiments in Micro-Electronics and Micro-Systems, EuroSimE 2007

composition. The higher the temperature, the more the radiation emitted. This infrared radiation, not perceptible with the naked eye, is made visible and measurable by the infrared camera. By analysing this infrared radiation it is possible to measure temperature as well as, indirectly, the thermal conductivity, mechanical stresses, material compositions, defects such as pores and delamination, and various other kinds of inhomogeneities in the materials.

The IR camera used (Fig. 1) has an IR detector head with a focal plane array (FPA) detector sensitive in the range 1 μm – 14 μm. An infrared microscopic lens MWIR 2.5X, with a focus distance of 21-22 mm was used. The camera is interfaced with software to control real-time acquisition and analysis of the infrared data.

The specimens used were identical flip chip assemblies attached to either a copper or FR4 substrate. They were mounted vertically and powered at 1.2 W and cooled by free convection.

The flip chip specimens were silicon-on-silicon multi-chip modules (MCMs) the same as those used in a previously reported experiment [6]. Both MCMs consisted of a 3 mm × 3 mm × 0.5 mm "heater" chip that bore a large central resistive element (the heater) in addition to small aluminium tracks and 36 connection pads. The "carrier" chip was larger at 6 mm × 6 mm × 0.5 mm and included larger ball grid array type pads allowing for external connections to be made, as well as the corresponding pads to match those on the heater chip. The heater chip was attached to the carrier chip so that a standoff height of 35 μm was achieved (without underfill). The MCMs were subsequently attached to the corresponding substrate by a thermally conductive adhesive pad. A schematic of the assembled specimen is shown in Fig. 2.

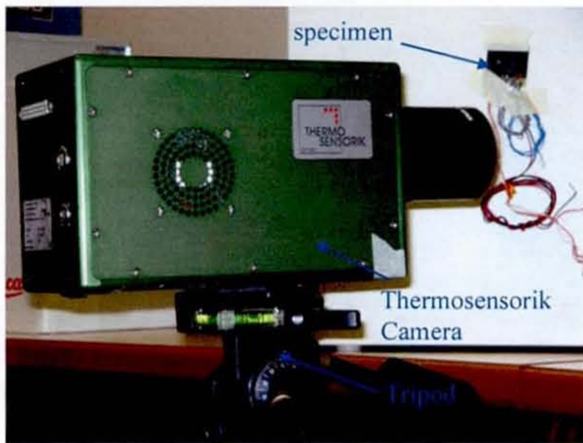


Figure 1 Experimental setup

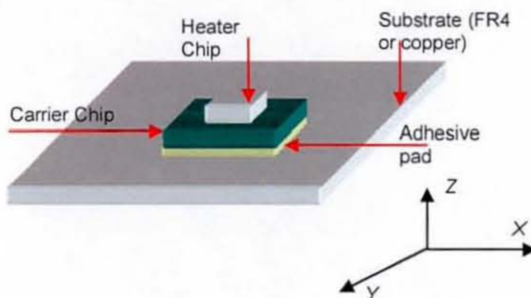


Figure 2 Schematic of flip chip specimens

Figure 1 shows the experimental setup, used for acquiring the temperature data for the flip chip assemblies. The camera, fitted with the micro lens, is mounted on the tripod, the specimen is powered on for few minutes to stabilise the temperature distribution in the specimen, then the lens is focused on the specimen and the temperature profile is captured.

2.2 Experimental results and discussion

The temperature distributions over the chip for a continuous 1.2 W power dissipation are given in Figs. 3 and 4 for free convection. The path used for subsequent temperature distribution analysis, is also shown. These figures demonstrate the effect of the substrate on the chip temperature distribution: the copper substrate results in lower temperatures compared to the FR4 substrate. From comparison of these two temperature profiles, the temperature distribution is symmetric on the chip with a

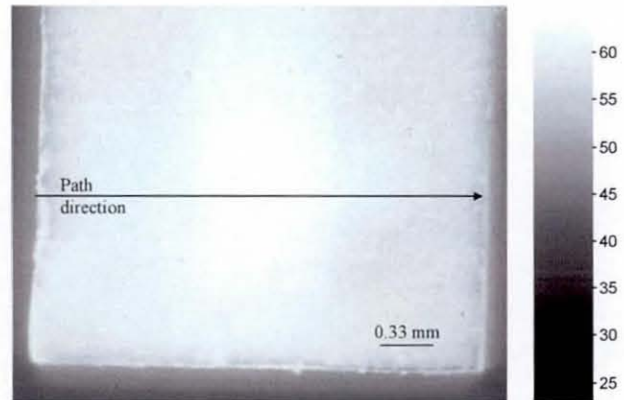


Figure 3 Temperature distributions in a chip mounted on a copper substrate at 1.2W

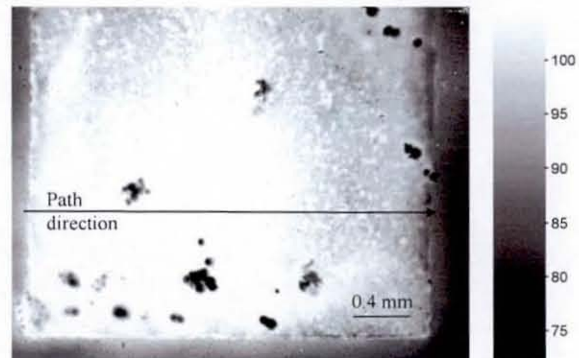


Figure 4 Temperature distributions in a chip mounted on FR4 substrate at 1.2 W

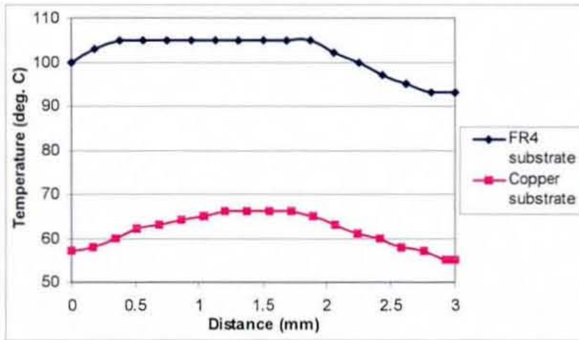


Figure 5 Effect of substrate on temperature distribution in the chip for free convection

copper substrate, while that for the chip with a FR4 substrate is asymmetric. The cool appearing patches may be attributed to non-uniform application of the black paint which is applied to ensure a higher uniform emissivity of the chip surface. Figure 5 shows the temperature distribution across the width of the chip for both types of substrate. It is evident that these temperature distributions are non-uniform: the maximum temperature is observed at the centre of the chip, where the heat is generated, while its boundary is at a lower temperature. Another important observation of this analysis is that the FR4 substrate induces higher thermal gradients in the chip than the copper substrate. This can be explained by the much higher thermal conductivity of copper compared with FR4. The experimental temperature distribution in the chip with a FR4 substrate is used as one of the thermal load cases for creep analysis, as it best represents typical operating conditions of the chip modelled in the finite element analysis.

3. Creep analysis

The geometry of a standard 1206 resistor chip was used for the creep analysis. Figure 6 shows the geometric dimensions of chip resistor modelled for finite element analysis. In the finite element modelling only one half of the geometry was used, due to the symmetry of the structure. The finite element model was created using 2D plane strain elements and a fine mesh pattern is maintained around the interface between component and solder. Figure 7 shows the mesh details.

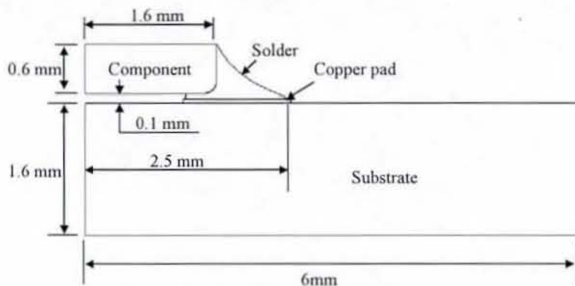


Figure 6 Geometry of 1206 chip resistor

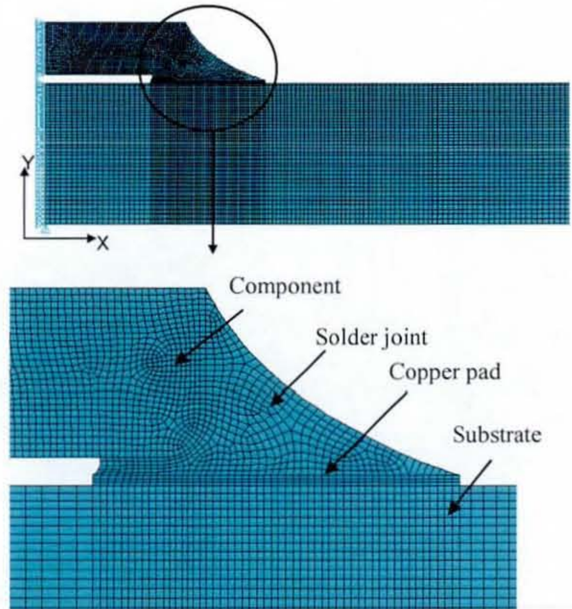


Figure 7 Finite Element Model of 1206 resistor

3.1 Creep constitutive equation

The solder joints of the 1206 resistor were modelled using the temperature-dependent material properties as shown in Table 1. A number of papers have been published [7, 8, 9] on the constitutive equation for creep deformation of SnAgCu alloys and they have identified two mechanisms for steady-state creep deformation. They attributed these to a dislocation climb controlled (low stress) and combined glide/climb (high stress) behaviour and have represented the steady-state creep behaviour using a double power law model. In this paper the creep

Temperature (°K)	Young's Modulus (MPa)	Poisson's ratio	CTE (ppm/°K)	Density (gm/cm³)
218	57300	0.4	12.7	7.5
248	55800	0.4	12.7	7.5
298	52600	0.4	21.2	7.5
248	49300	0.4	21.7	7.5
398	45800	0.4	23.0	7.5

Table 1 Elastic material properties for SnAgCu

model determined by Schubert et al. [7] is used for the steady-state creep behaviour. They also identified two regions for stress-strain rate behaviour, but postulated the high stress region as a power law break-down region, and chose the hyperbolic sine function to fit their creep data:

$$\dot{\varepsilon}_{cr} = A_1[\sinh(\alpha\sigma)]^n \exp\left[\frac{-H_1}{kT}\right] \quad (1)$$

Where A_1 = 277984 s^{-1}, α = 0.02447 MPa^{-1}, n = 6.41, $\frac{H_1}{k} = 6500$, $\dot{\varepsilon}_{cr}$ is steady state creep strain rate, σ is stress, T is absolute temperature.

Plasticity is also included along with creep in the finite element analysis. Plasticity is modelled with bilinear kinematic hardening (BKIN), which includes the Bauschinger effect due to thermal cycling. Table 2 gives the plastic material properties used for SnAgCu [10].

The material properties of 96% alumina (Al_2O_3) are used for the component body, whilst high-conductivity copper and FR4 material properties [10, 11] are used for pad and substrate respectively.

Temperature (ºK)	Yield stress (MPa)	Tangent modulus (MPa)
218	45	5700
248	41	5600
298	32	5260
348	21	4900
398	13	4600

Table 2 Plastic material properties of SnAgCu

3.2 Thermal cycling conditions

In the surface mount assembly process, the components are reflowed in an oven to create the solder joint and the assembly is then returned to room temperature. Therefore, creep analysis is carried out in two steps for three different temperature cycling conditions. In the first step, creep analysis is carried out for the reflow soldering process and relaxation for one hour at room temperature (assuming there is a one hour storage period before the resistor assembly is subjected to thermal cycling). The stress levels at the end of the reflow process give the manufacturing-induced stress in the solder joint, and similarly stress level at the end of relaxation gives the amount of stress after relaxation has taken place in the solder joint due to storage at room temperature. Below are the three different thermal cases used.

Case A: Uniform temperature ranging from 398°K (+125 °C) to 218°K (-55°C), where the entire resistor-substrate assembly is subjected to the same temperature.

Case B: Uniform temperature for the component, solder joint and copper pad ranging from 398°K (+125°C) to 218°K (-55°C), while the substrate's temperature (T_{sub}) is also uniform but varies according to the following relation:

$$T_{sub} = 0.18*T_{comp} + 299.4, \quad (2)$$

Where T_{comp} is the component's temperature. This equation is deduced from the previously described experimental results.

Case C: This case is more representative of real conditions where the temperature gradient from the experimental results is indirectly used in the thermal cycling. A thermal analysis was first carried out using temperature boundary conditions from the experimental results to obtain a continuously varying temperature distribution throughout the surface mount assembly. Figure 8 shows the different thermal zones within the resistor assembly used in the thermal analysis. Temperature boundary conditions were applied on the outer surface of the body at zone 1 and zone 3. In zone 2, a set of nodes was selected for temperature boundary condition application. The temperature boundary conditions in zone 2 (solder joint) and zone 3 (substrate) are based on the zone 1 (component) temperature. The

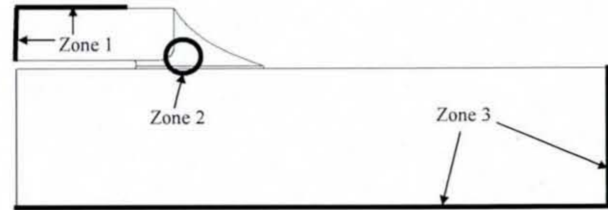


Figure 8 Temperature zones for thermal analysis

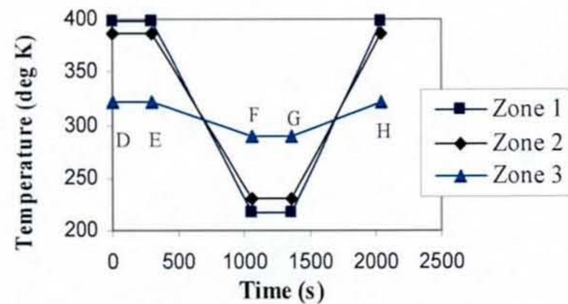


Figure 9 Temperature variations in zone 1, zone 2 and zone 3 in thermal analysis

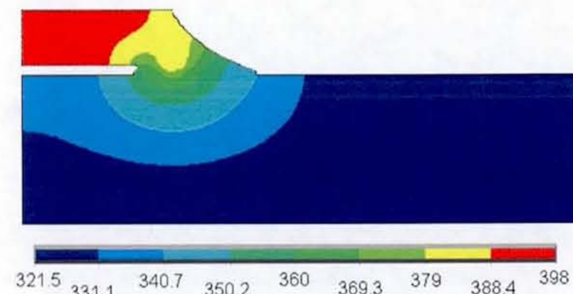


Figure 10 Temperature distribution in resistor assembly when component is at 398°K

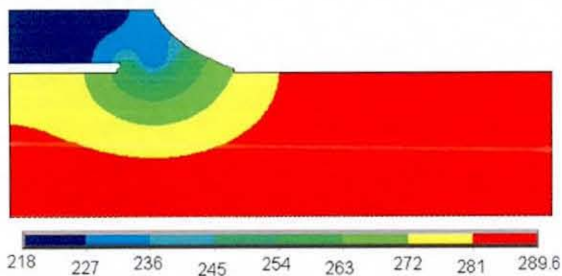


Figure 11 Temperature distribution in resistor assembly when component is at 218°K

relationship between the temperatures in zone1, zone2 and zone3 were deduced from the experimental results. Figure 9 shows the variation of temperature boundary conditions at different zones throughout the thermal cycle. Figures 10 and 11 give the temperature distribution in the 1206 resistor assembly after thermal analysis was carried out when the zone 1 (component) temperatures are 398°K and 218°K respectively. In Case C the resistor assembly is subjected to a thermal cycle between these two extreme temperature profiles.

Figure 12 shows the typical thermal cycle used in creep analysis. Line AB represents the reflow process, where a cooling rate of 4°C/s is used, and line BC represents storage of the resistor at room temperature for an hour. After an hour of storage at room temperature, the component temperature (T_{comp}) is ramped to 398°K (in Case A this is the whole assembly temperature) to start the thermal cycling. A complete thermal cycle starts at D and ends at H. In this thermal cycle there is a ramp of 12 minutes between temperature extremes (398°K and 218°K) and dwells of 5 minutes at the extreme temperatures.

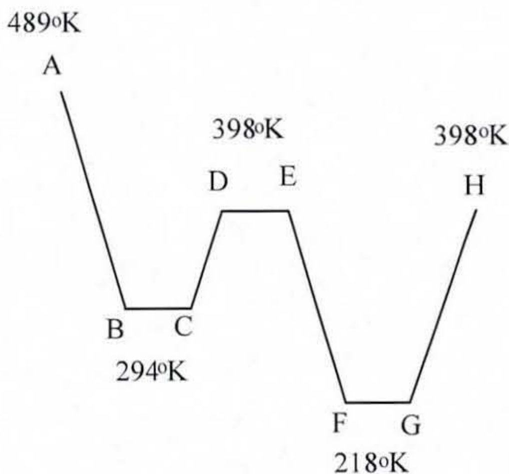


Figure 12 Thermal cycle used for creep analysis based on component temperature

4. Result and discussions

Finite element analysis of the chip resistor assembly was carried out for two thermal cycles and for the three different thermal loading cases described above. Figure 13 shows the shear stress distribution in the solder joint after the reflow process and also the location of maximum shear stress. The maximum shear stress of 25 MPa observed in the solder joint fillet, is mainly due to the mismatch of coefficients of thermal expansion (CTE)

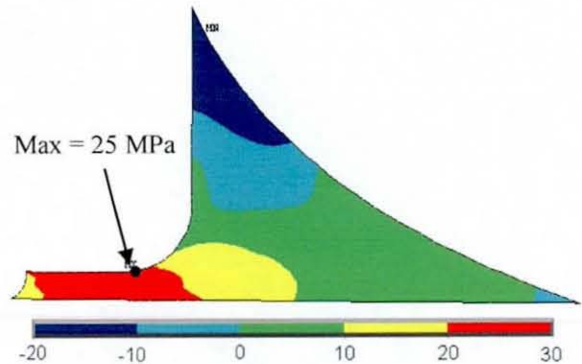


Figure 13 Distribution of shear stress in the solder joint at the end of reflow period (time = 48s)

between component (made from alumina), solder and substrate (made from FR4). This stress is well above the yield stress of SnAgCu solder alloy at room temperature. When the resistor assembly is stored at room temperature, this stress reduces by the solder joints undergoing creep strain. This process is called stress relaxation. The shear stress after stress relaxation for one hour at room temperature reduces to 12 MPa, as can be seen in Fig. 14, which is below the yield stress at room temperature of SnAgCu alloy. The shear stress evolution for the entire creep analysis is shown in Fig. 14, which includes reflow period, relaxation period and 2 thermal cycles, all for the peak stress location in Fig. 13. It is evident from the figure that the shear stress range is 35MPa for Case A and that for Cases B and C is only about 15 MPa. This shows that there is about a 60% reduction in the shear stress

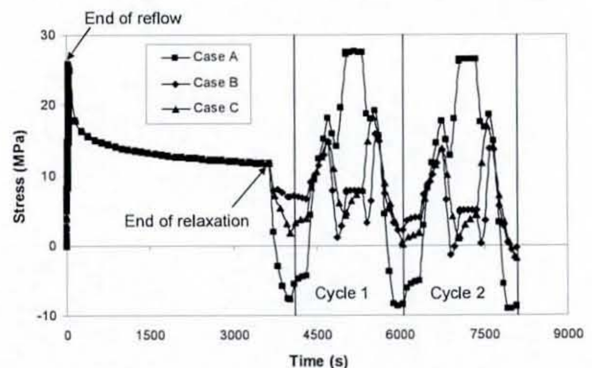


Figure 14 Distribution of shear stress in the solder fillet over time

range for Case B and C.

Accumulated inelastic strain due to thermal cycling is also studied for the solder joint. Figure 15 shows the worst case variation of inelastic strain over time at solder fillet. The total accumulated inelastic strain at the end of two thermal cycles was largest (9.5%) for Case A and smallest for Case C (7.2%). In Case B and Case C the total accumulated creep strain at the end of the thermal cycle is reduced by 13% and 28% respectively compared with case A. It can be observed from Fig. 15 that, even though most of the inelastic strain accumulation has taken place during the reflow and relaxation periods, this depends on parameters such as relaxation time, temperature and number of thermal cycles. In this particular analysis inelastic strain accumulation during the reflow and relaxation period accounts for 50%, 57% and 69% for Case A, Case B and Case C respectively. The

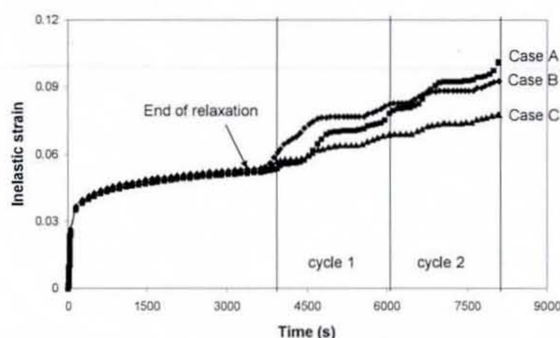


Figure 15 Accumulation of creep strain with time

amount of inelastic strain accumulation is reduced in thermal cycle 2 compared with that in thermal cycle 1. This reduction is only 3% for Case A compared with Cases B and C where it is 23% and 20% respectively. It is however expected that further reductions for subsequent cycles would be smaller.

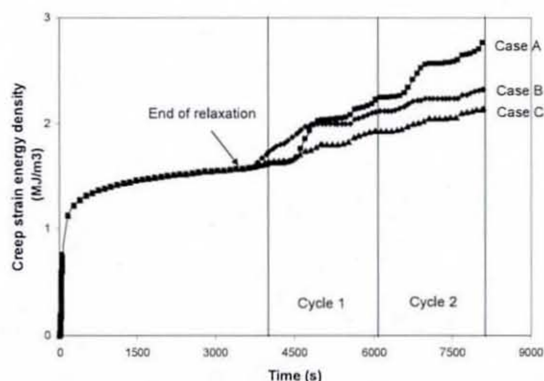


Figure 16 Accumulation of creep strain energy density in solder joint

Figure 16 demonstrates the density of creep strain energy dissipated in the solder joint during the analysis. This variation is quite similar to the variation of accumulated inelastic strain in the solder joint, with Case A having a higher density of creep strain energy dissipation (2.64 MJ/m^3) due to the higher inelastic strain accumulation and Case C having a lower density of creep strain energy dissipation (1.96 MJ/m^3).

The number of cycles to failure, N_f, for the solder joints were predicted based on the following Coffin-Manson based relationship [3]:

$$N_f = (C'\varepsilon_{acc})^{-1} \quad (3)$$

Where ε_{acc} = Accumulated inelastic strain per cycle and C' = inverse of creep ductility. The accumulated inelastic strain calculated for the 2nd thermal cycle was considered for these life calculations.

Table 3 gives the predicted lives for the three different thermal loading cases. From comparison of predicted lives for the three different thermal cases, there is more than 100% improvement in the life of the solder joint in case B and case C. Case C is predicted to have the longest life for the solder joint (i.e. 2456 cycles) out of the three cases.

Thermal cycling conditions	C' (inverse of creep ductility)	Acc. inelastic strain in 2nd cycle	Predicted lives (cycles)
Case A	0.0468	0.023	929
Case B	0.0468	0.0104	2054
Case C	0.0468	0.0087	2456

Table 3 Predicted life for chip resistor

5. Conclusions

The experimental results demonstrate a typical non-uniform temperature distribution in an electronic assembly. The finite element study carried out based on the experimental results is a preliminary study to understand the effect of a non-uniform temperature distribution on the fatigue behaviour of lead-free solder joints. Out of the three different thermal loading cases considered, Case C (non-uniform temperature distribution) is predicted to result in lower levels of shear stress, creep strain accumulation and creep strain energy density. However, the accumulation of creep strain and creep strain energy density depend on relaxation time, temperature and number of thermal cycles. Therefore, further creep studies are required considering various relaxation times, temperature and a greater number of thermal cycles. The inelastic strain based estimated lives

demonstrate the significant impact of non-uniform temperature distribution (case C) on fatigue life of solder joint in the chip resistor, case C predicting highest number of life cycles. However, the accumulated inelastic strain is from 2nd thermal cycle, which needs further creep analysis to establish the stabilised accumulated inelastic strain per cycle. The capture of thermal data for the actual components studied and a more accurate thermal model, taking into account the thermal mass distribution in the assembly, will be used to assess the interaction of power and thermal cycles on fatigue. Future analysis will also establish the relevant contributions of plastic and creep strains to fatigue damage and the life reduction attributable to post reflow stress relaxation.

References

1. Gonzalez, M., Vandevelde, B., Beyne, E., "Thermo-Mechanical Analysis of a Chip Scale Package (CSP) Using Lead Free and Lead Containing Solder Materials", *Proc 3rd European Microelectronics and Packaging Symposium*, Prague, Czech Republic, June. 2004.

2. Wu, C.M.L., Yu, D.Q., Law, C.M.T., Wang, L., "Properties of Lead-free Solder Alloys with Rare Earth Element Additions", Material Science and Engineering R 44 (2004) pp. 1-44.

3. Syed. A., "Accumulated Creep Strain and Energy Density Based Thermal Fatigue Life Prediction Models for SnAgCu Solder Joints", *Proc 54th Electronic Components and Technology Conf*, Las Vegas, USA, June. 2004, pp. 737-746.

4. Warde, J., Wallach, E.R., "The Prediction of Creep Damage in Surface Mount Components using Finite Element Modelling," NPL Report CMMT(A)218, March. 1999.

5. Pang, J.H.L., Chong, D.Y.R., Low, T.H., "Thermal Cycling Analysis of Flip-Chip Solder Joint Reliability," *IEEE Trans* Compn. and Packag. Technol. Vol. 24, No. 4 (2001), pp. 705-712.

6. Ochana, A.R., Hutt, D.A., Whalley, D.C., Sarvar, F., Al-Habaibeh, A., "Modelling of the Power Cycling Performance of a Si on Si Flip Chip Assembly," *Proc 10th Intersociety Conference on Thermal and Thermochanical Phenomena in Electronics Systems, ITHERM 2006*, San Diego, USA, May. 2006, pp. 243-250.

7. Schubert, A., Dudek, R., Auerswald, E., Gollbardt, A., Michel, B., Reichl, H., "Fatigue Life Models of SnAgCu and SnPb Solder Joints Evaluated by Experiments and Simulations," *Proc 53rd Electronic Components and Technology Conf*, New Orleans, LA, May. 2003, pp. 603-610.

8. Wiese, S., Meusel, E., Wolter, K.-J., "Microstructural Dependence of Constitutive Properties of Eutectic SnAg and SnAgCu Solders," *Proc 53rd Electronic Components and Technology Conf*, New Orleans, LA, May. 2003, pp. 197-206.

9. Morris, J.W., Song, H.G., Hua, F., "Creep Properties of Sn-rich Solder Joints," *Proc 53rd Electronic Components and Technology Conf*, New Orleans, LA, May. 2003, pp. 54-57.

10. Database for solder properties with emphasis on new lead-free solders http://www.boulder.nist.gov/div853/lead%20free/props01.html

11. Matweb material property database, www.matweb.com.

Journal of Thermal Stresses, 31: 1039–1055, 2008
Copyright © Taylor & Francis Group, LLC
ISSN: 0149-5739 print/1521-074X online
DOI: 10.1080/01495730802250763

Taylor & Francis
Taylor & Francis Group

3D STUDY OF THERMAL STRESSES IN LEAD-FREE SURFACE MOUNT DEVICES

Pradeep Hegde, David Whalley, and Vadim V. Silberschmidt
Wolfson School of Mechanical and Manufacturing Engineering, Loughborough University, Loughborough, Leicestershire, UK

The paper presents the study of non-uniform temperature distributions in a flip chip electronic assembly, and the use of these temperature distributions to analyse the thermal stresses in lead-free solder joints in surface mount devices. The thermal stresses in the solder joints are mainly due to the mismatch in the coefficients of thermal expansions between the component and substrate materials, and temperature gradient in the electronic assembly. The thermo-elasto-visco-plastic finite element analysis is carried out to investigate the extent of thermal stresses induced in solder joints between a surface mount component and a FR4 circuit board (substrate) under conditions of thermal cycling with the chip resistor operating at its full power condition. Three different cases of spatial temperature distributions are considered including one with an experimentally obtained non-uniform temperature distribution. A comparative study of thermal stresses is performed using a near-eutectic SnAgCu solder material for three different thermal cases.

Keywords: Creep; Lead-free solder; Surface mount device; Temperature distribution; Thermal stresses

Downloaded By: [Silberschmidt, Vadim V.] At: 09:56 29 September 2008

INTRODUCTION

Solder joints are commonly used in electronic packaging for mechanical support and electrical connection of components. Various technologies are used to create solder joints in electronic packaging depending on the type of electronic products being manufactured. Driven by a desire for miniaturization and increased circuit speed, a surface mount technology (SMT) has been widely adopted in electronic packaging. However, introduction of SMT also brought with it a new era of joints' failures. A major finding of electronic package failures is that the joint material does not demonstrate an adequate ability to sustain deformations due to cyclic variation of temperature during operation [1, 2].

The applications of electronic packages vary from entertainment to aerospace industries. In these applications, solder joints operate under severe temperature conditions compared to their melting temperature – the temperature can change between 218 K to 398 K. This cyclic variation of temperature makes solder joints prone to thermal stresses that can be caused by various reasons. For instance,

Received 20 March 2008; accepted 28 May 2008.
Address correspondence to V. V. Silberschmidt, Wolfson School of Mechanical and Manufacturing Engineering, Loughborough University, Leicestershire LE11 3TU, UK. E-mail: V.Silberschmidt@lboro.ac.uk

a body, restricted from its free expansion due to uniform change in temperature experiences thermal stresses as well as a component under a non-uniform change in temperature. Thermal stresses can also be induced due to the mismatch in the coefficient of thermal expansion (CTE) between different components of an assembly [3]. However, in electronic packaging, solder joints experience thermal stresses due to a combined effect of non-uniform temperature distributions in the package when it is powered and the mismatch in CTE between the component and substrate material.

The thermal strains in the electronic packaging are cyclic in nature due to the variation in the operating conditions such as powering on and off of the assembly, and cycling variations in the ambient temperature. Therefore, thermal fatigue is one of the major failures in the surface mount solder joints. The problem of fatigue in solder joints is linked to an intermittent character of heat generation during power cycling in the electronic components. The generated heat is dissipated by radiation, convection and conduction. The last mechanism results in the heat flow through the solder joint to the substrate, heating up both. Since the component and substrate materials have different CTEs they experience relative displacement due to expansion. Both the component and substrate are significantly stiffer than the solder joint, so the repeated relative displacements produce a cyclic stress in it and its eventual fatigue failure [1]. This problem has been worsened considerably by the introduction of leadless surface mount devices since the size of the solder joint is very small and there is less compliance between the component and substrate. For instance, leadless devices such as chip capacitors and resistors, as well as ceramic chip carriers, have only a solder fillet to relieve any induced thermal strains. Figure 1 demonstrates the solder joint's crack in the surface mount capacitor due to thermal cycling between 218 K to 398 K [4].

Downloaded By: [Silberschmidt, Vadim V.] At: 09:56 29 September 2008

Solder joints are also prone to creep due to high operating homologous temperatures (T_h, the ratio of operating and melting temperature in absolute scale). For most of the solder materials T_h is about 0.6 at the room temperature (RT). Working at such high T_h, the solder usually exhibits very complicated rate- and temperature-dependent mechanical behaviours such as viscous creep, stress

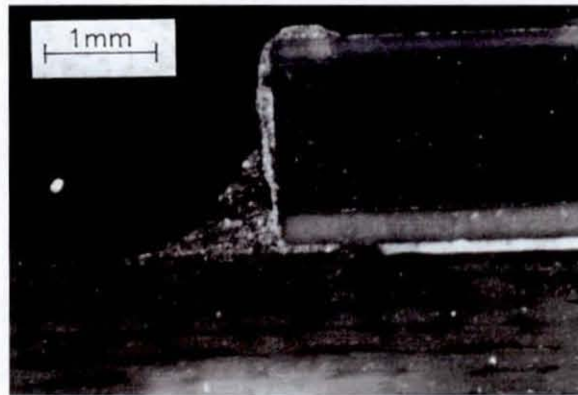


Figure 1 Solder fillet cracking in thermal cycling test between 218 K to 398 K on 1812 size ceramic capacitors [4].

relaxation, and plasticity [2, 4, 5]. This results in accumulation of creep damage alongside with thermo-mechanical damage. Predicting the reliability of solder joints under such conditions is complicated since they are at complex states of stress and strain [1, 3]. In addition, an exchange of lead-containing solder materials with lead-free ones added more concerns for the electronic industries with regard to manufacturing of reliable products. Eutectic or near-eutectic SnAgCu alloy used as possible replacement for well-established SnPb solder alloys are considerably less studied. However, the use of experimental techniques such as accelerated tests, for obtaining test data to assess the reliability of solder joints is both time-consuming and difficult to extrapolate to predict operational reliability.

Recently, numerical simulations based on finite element analysis became a tool to investigate the reliability of solder joints subjected to thermal cycling. Most simulations deal with reliability for conditions of thermal cycling and power cycling, usually, uniform temperature distributions in the assembly are considered linked to the variation in ambient operating conditions. Thermo-mechanical analysis of a chip-scale package (CSP), assembled using both lead-free and lead-containing solder materials [6], and thermal cycling analysis of flip-chip solder joint reliability [7] are typical examples. However, research into the effect of non-uniform temperature distributions in assemblies due to continuous heat dissipation by the chip resistor along with cyclic variation in the ambient temperature is insufficient. Hence, this paper focuses on effect of actual temperature distributions in the powered flip-chip electronic assembly and finite-element simulations using these temperature distributions for varying ambient temperature. The finite-element model accounts for both plasticity and the creep behaviour of a new lead-free SnAgCu solder alloy. A comparison of 3D evolution of thermal stresses in the solder joint is performed for three different thermal cases including the experimentally measured temperature distribution for powercycling.

Downloaded By: [Silberschmidt, Vadim V.] At: 09:56 29 September 2008

EXPERIMENTAL ANALYSIS

In order to obtain the temperature distribution in an electronic assembly, experiments were carried out with a flip-chip electronic assembly for power cycling condition, using an infrared (IR) Thermosensorik camera. An IR technique is a contactless temperature measurement technique where radiation emitted from a surface is captured by a thermal camera and processed for obtaining temperature distribution over that surface. Although the flip-chip assembly used in experiments is different from the component (chip resistor) modelled, the general size and joint distribution make both flip-chip and chip resistor assemblies comparable, allowing the flip-chip experimental results to provide an indication of the temperature gradients in the chip resistor.

Specimen Preparation

The flip-chip specimens were silicon-on-silicon multi-chip modules (MCMs) that matched the description of those used in a previous experiment [8]. Both MCMs consisted of a 3 mm × 3 mm × 0.5 mm "heater" chip that bore a large central resistive element (the heater) in addition to small aluminium tracks and 36 connection pads. The "carrier" chip was larger at 6 mm × 6 mm × 0.5 mm and

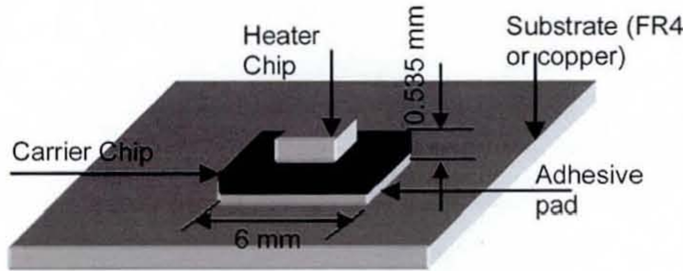


Figure 2 Schematic of specimens used in experiments.

Downloaded By: [Silberschmidt, Vadim V.] At: 09:56 29 September 2008

included larger ball grid array pads for external connections, as well as the corresponding pads to match those on the heater chip. The latter was attached to the carrier chip so that a standoff height of 35 μm (without underfill) was achieved. The MCMs were subsequently attached to the substrate by a thermally conductive adhesive pad. A schematic of the assembled specimen is shown in Figure 2.

The specimens were attached to either a copper or FR4 substrate and sprayed with matt black paint to achieve uniform emmissivity over the surface. The specimens were mounted vertically, powered at 1.2 W, and cooled by free convection. The camera, fitted with the micro lens, was mounted on the tripod, the specimen was powered on for few minutes to stabilize the temperature distribution in the specimen, then micro lens was focused on the specimen and the temperature distribution was captured.

EXPERIMENTAL RESULTS AND DISCUSSION

Experiments were carried out for two power dissipation conditions (0.44 W and 1.2 W) for two specimens, one with FR4 and another with copper as substrate

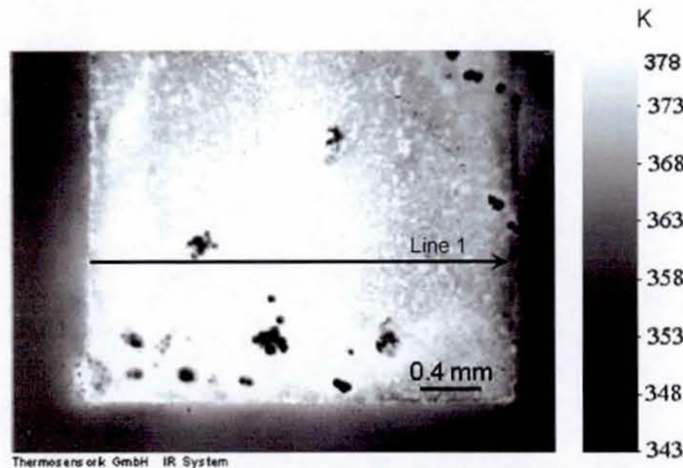


Figure 3 Temperature distribution (in K) in a chip mounted on FR4 substrate at 1.2 W.

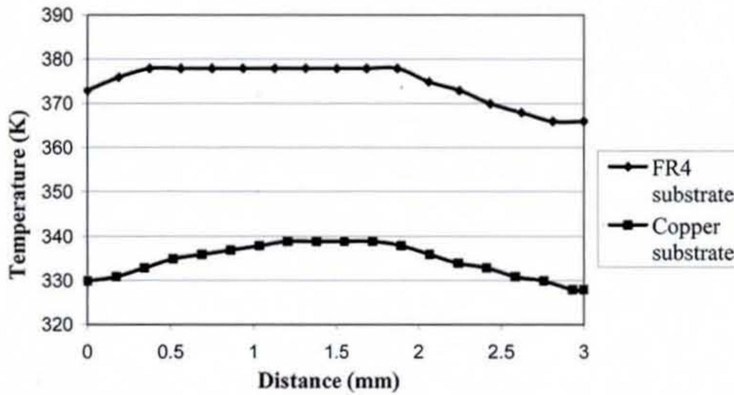


Figure 4 Effect of substrate on temperature distribution in the chip for free convection.

Downloaded By: [Silberschmidt, Vadim V.] At: 09:56 29 September 2008

materials [4]. These power dissipation conditions are selected to establish a relation between temperatures of the chip and substrate. The captured temperature distribution for continuous power dissipation of 1.2 W over a chip surface is given in Figure 3, along with the path used for temperature distribution analysis over the chip. Figure 4 shows the temperature distributions across the width of the chip for both substrates. The effect of the substrate material on the temperature distribution over the chip surface is very clear from the comparison of these temperature distributions.

Since copper is a better heat conductor than FR4, more heat is dissipated from the flip-chip assembly to the atmosphere, resulting in lower temperature magnitudes. For both specimens the maximum temperature is observed at the centre of the chip, where a heat-generating resistive element is situated. The distribution of the temperature over the chip surface is nearly symmetric for the chip mounted on copper substrate while that for the chip with a FR4 substrate is asymmetric. This may be due to the manufacturing deficiency with a skewed resistive element. The patches appearing cool in the image may be attributed to non-uniform application of black paint. From the variation of chip and substrate temperature with power dissipation, following relation is deduced,

$$T_{\text{sub}} = 0.18T_{\text{chip}} + 299.4 \tag{1}$$

where T_{chip} is chip temperature and T_{sub} is substrate temperature.

This experimental study confirms that, as expected, FR4 substrate induces a higher level of temperature in the flip-chip assembly. Also the average temperature gradient, which is a difference between maximum and minimum temperature in the assembly, is higher for specimen with FR4 as a substrate material. Therefore, the temperature distribution obtained for flip-chip assembly with FR4 substrate is used as temperature boundary conditions for thermal analysis, which is later used in structural analysis.

THERMAL ANALYSIS

Finite element analysis is broadly used to study various engineering problems such as new product design, improving the existing products, their reliability, in studies of new materials etc. Due to the legislation introduced across the world to remove the lead content from electronic products, reliability of the new generation of lead-free solders should be thoroughly tested before introduction into products. The finite element technique enables a researcher to simulate the various operating conditions of solder joints and study the structural behaviour such as thermo-mechanical, creep, and low cycle fatigue damage. In finite element analysis the structural problem is represented in terms of a mathematical model that is solved for field variables. In the present work, finite element analysis has been used to obtain the temperature distribution in the chip resistor assembly and study the structural response of solder joint for three different thermal cases.

Downloaded By: [Silberschmidt, Vadim V.] At: 09:56 29 September 2008

Finite Element Model

The finite element analysis, both thermal and structural, of a chip standard Panasonic 1206 resistor was implemented with commercial software ANSYS. The geometric dimensions of different components of this resistor assembly are shown in Figure 5. Due to the construction of the chip resistor assembly, which is symmetric, only one half of its geometry is shown for a side view (Fig. 5(a)) and considered for finite element modelling. A 3D finite element model is considered for the thermal stress study to capture the entire 3-dimensional distribution of the temperature and its effect on the thermal stress integrity of the solder joint.

Figure 6 shows the meshing used in the assembly as well as the critical region. Since the solder joint is our area of interest, a finer mesh pattern has been used there. The finite element model is built with 8-noded hexahedral elements. ANSYS employs an error approximation technique based on the Zienkiewicz-Zhu scheme. In this scheme, an initial stress error contributed by each element at each node is calculated as follows [9]:

$$\{\Delta\sigma_n^i\} = \{\sigma_n^a\} - \{\sigma_n^i\} \tag{2}$$

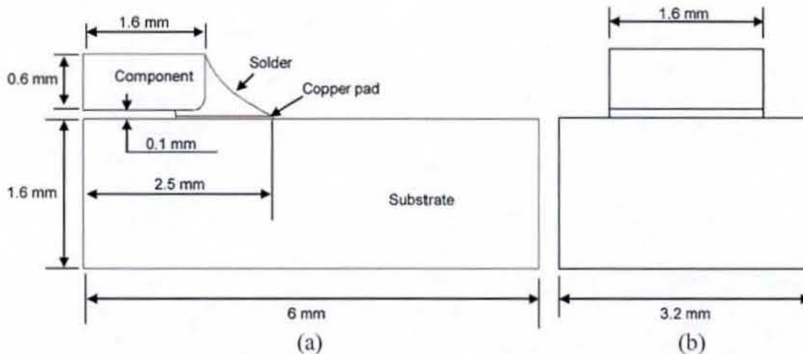


Figure 5 Geometrical details of chip resistor assembly: (a) side view and (b) front view.

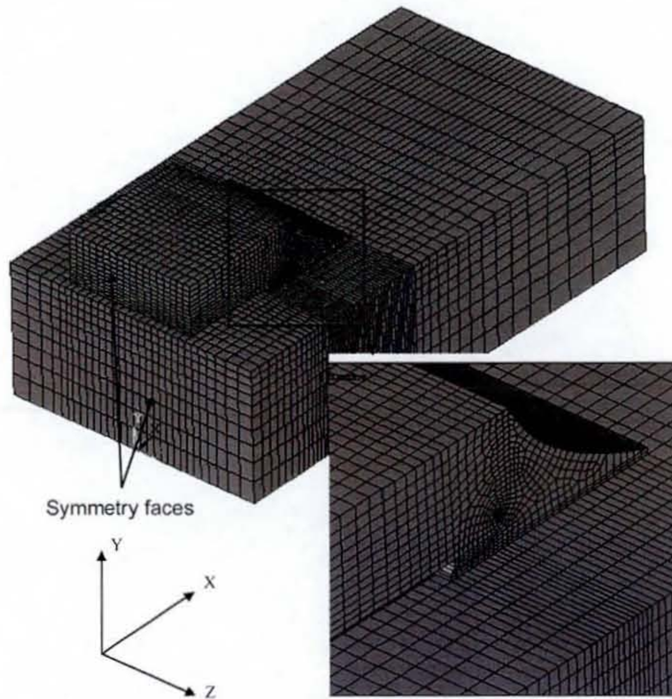


Figure 6 Meshing of chip resistor assembly.

Downloaded By: [Silberschmidt, Vadim V.] At: 09:56 29 September 2008

where $\{\Delta\sigma_n^i\}$ is the stress error vector at node n for element i, $\{\sigma_n^a\}$ is the averaged stress vector at node n, $\{\sigma_n^i\}$ is the stress vector of node n of element i.

Then, the stress bounds are estimated considering the above error:

$$\sigma_j^{mnb} = \min\left(\sigma_{j,n}^a - \Delta\sigma_n\right) \tag{3}$$

$$\sigma_j^{mxb} = \max\left(\sigma_{j,n}^a + \Delta\sigma_n\right) \tag{4}$$

where σ_j^{mnb} is the nodal minimum of stress quantity (SMNB), σ_j^{mxb} is the nodal maximum of stress quantity (SMXB).

An error estimation study was carried out at the fillet region of the solder joint to assess the mesh quality for the creep analysis. In this study a linear static analysis was conducted for different mesh patterns and related element dimensions, and the maximum nodal stress (SMX) in the fillet of solder joint was assessed together with its bound SMXB. The mesh was considered to be suitable with regard to convergence when the difference between the magnitudes of the ratio of SMXB and SMX for two consecutive iterations for the mesh pattern achieved the prescribed level. There are two main regimes of heat transfer in electronics packages with respective types of variations of thermal stresses – transient (power on/off) and steady-state (during operation). In both cases, for the theory of isotropic thermal stresses and strains, the temperature distribution $T(x, y, z, t)$ in the package is calculated by solving the heat conduction equation (with prescribed initial and

boundary conditions that are described next [10]):

$$\nabla^2 T = \frac{\rho C_v}{k}\frac{\partial T}{\partial t} - \frac{W}{k} \tag{5}$$

where $\nabla^2 = \frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + \frac{\partial^2}{\partial z^2}$; $T \equiv T(x, y, z, t)$ is instantaneous absolute temperature; C_v is heat capacity per unit mass; ρ is mass density; k is the heat conduction coefficient; W is heat generation per unit time per unit volume.

RESULT AND DISCUSSIONS

Thermal stresses are the major cause of concern in the reliability of solder joints, as they operate in high temperature conditions compared to their melting temperature. Hence it is important to model the exact thermal field corresponding to the in-field conditions for the structural analysis. The discussed experimental work gives only the surface temperature of the chip assembly. In order to obtain the internal temperature distribution in the chip resistor assembly a simple thermal analysis is carried out considering only a conduction heat transfer. For this thermal analysis surface temperatures obtained from the experiment are used as boundary conditions. The chip resistor can operate in the temperature range between 398 K and 218 K. Therefore, the maximum temperature a chip can achieve is 398 K when it is operating at its maximum power. Considering this chip temperature (T_{chip}), the substrate temperature (T_{sub}) was calculated using Eq. (1). The difference between temperatures of the substrate and chip gives the temperature gradient on the

Downloaded By: [Silberschmidt, Vadim V.] At: 09:56 29 September 2008

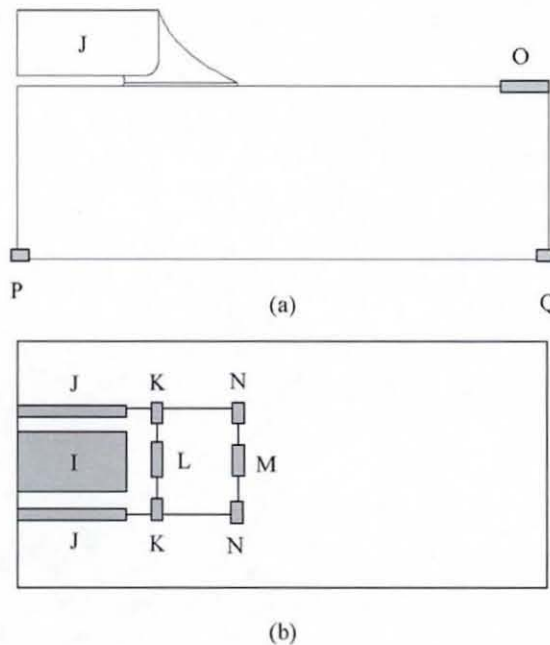


Figure 7 Zones of thermal boundary conditions: (a) side view and (b) top view.

Table 1 Temperature levels at different zones for two extreme ambient temperatures

Thermal zone	Boundary conditions at ambient temperature 398 K	Boundary conditions at ambient temperature 218 K
I	398	294.5
J	386	282.5
K	382	278.5
L	384	280.5
M	379	275.5
N	376	272.5
O	328	224.5
P	343	239.5
Q	321.5	218

Downloaded By: [Silberschmidt, Vadim V.] At: 09:56 29 September 2008

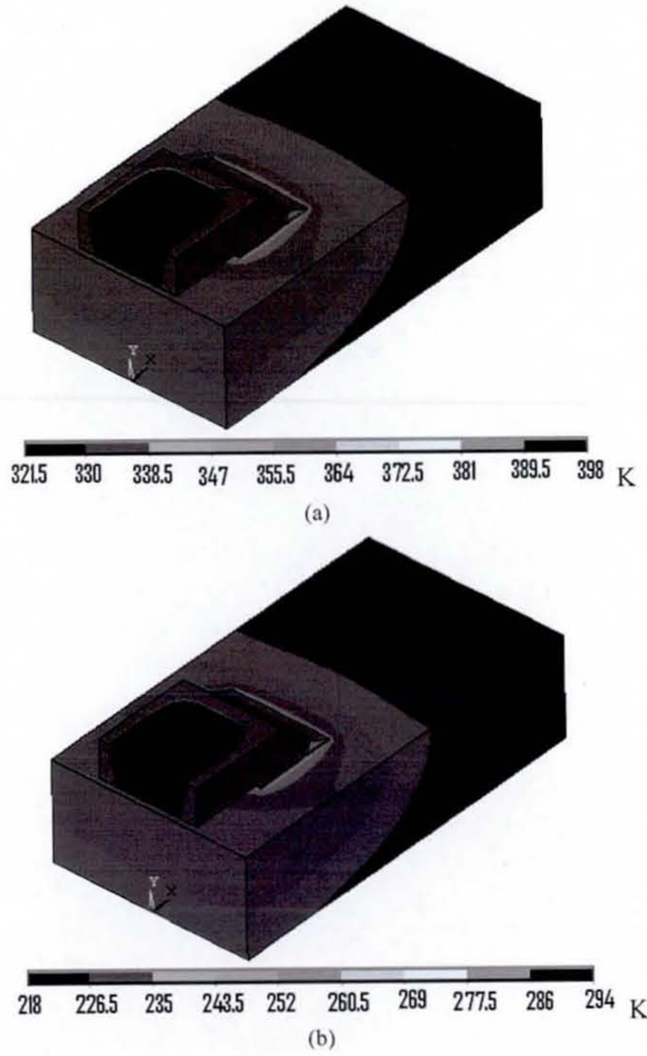
assembly when chip is operating at its maximum power condition. The thermal analysis was carried out for two extreme ambient temperatures 398 K and 218 K with maintaining the same temperature gradient in the assembly due to the fact that the chip resistor is continuously dissipating heat at its maximum power.

Figure 7 shows the thermal zones used for the application of boundary conditions based on the experimental measurements. Table 1 gives the temperature levels used for different zones of the resistor assembly for the ambient temperature 398 K and 218 K. For example, to apply the temperature boundary condition due to heat generated by resistive element, an area covered by it (zone I in Fig. 7) on the top surface of the component is selected. Similarly temperature zones are selected based on the temperature data collected from the experimental work and respective temperature distributions are applied. A linearly varying temperature is applied on the bottom surface of the substrate, which is between zone H and I to replicate the reality when chip resistor is powered on. The obtained temperature distributions after thermal analysis are shown in Figures 8(a) and (b) for ambient temperature 398 K and 218 K, respectively. These two temperature profiles are used in the subsequent structural analysis as parts of the thermal history.

THERMAL STRESS ANALYSIS

Material Properties

The chip resistor assembly consists of a chip component made of alumina, a solder joint, a copper pad and a FR4 substrate. Since the material properties of the solder alloy greatly varies with the temperature, temperature-dependent elasto-plastic material properties of Sn3.8Ag0.7Cu (SAC) alloy [11, 12] has been used for solder joint, which is given in Table 2. In this finite-element simulation, the solder material is modelled with the bilinear kinematic hardening (BKIN) material model. The model's name is derived from the way a stress-strain curve is modelled and the type of hardening rule used for the plastic flow. In the model, both elastic and plastic regions are represented by two straight lines with different slopes. The slope of the plastic part is linked to the tangent modulus, which is given in Table 2. The kinematic strain hardening is used to include the Bauschinger effect due to cyclically



Downloaded By: [Silberschmidt, Vadim V.] At: 09:56 29 September 2008

Figure 8 3D temperature distributions (in K) in chip resistor assembly at ambient temperature (a) 398 K and (b) 218 K.

Table 2 Material properties for SAC solder [11, 12, 19]

Temperature (K)	Young's modulus (MPa)	CTE (ppm/K)	Yield stress (MPa)	Tangent modulus (MPa)
298	44400	21.2	38	154
348	30700	21.7	30	134
423	18800	23.0	17	132

varying thermal loads. The material properties of 96% alumina (Al_2O_3) were used for the chip component body, while high-conductivity copper and FR4 material properties were used for pad and substrate, respectively.

There is a significant amount of research regarding the constitutive equations for creep deformation in both lead and lead-free solder materials. For instance, Wiese et al. [13] studied the creep behaviour of Sn4.0Ag0.5Cu for both bulk solder and flip chip solder joints. Their study identified two types of creep mechanisms for steady-state deformation linked to the climb-controlled (at low stresses) and combined glide/climb (at high stresses) dislocation behaviour. Similar studies were carried out by Schubert et al. [14] and Zhang et al. [15], and both identified two regimes of the stress-strain rate behaviour. Both modelled the steady-state creep rate with a classical hyperbolic sine creep law:

$$\dot{\varepsilon}_{cr} = A_1[\sinh(\alpha\sigma)]^n \exp\left(-\frac{Q}{RT}\right) \tag{6}$$

where constant $A_1 = 277984\,\mathrm{s}^{-1}$, a multiplier to equivalent stress $\alpha = 0.02447\,\mathrm{MPa}^{-1}$, a stress exponent $n = 6.41$, the activation energy $Q = 54041\,\mathrm{J/(K \cdot mole)}$, the gas constant $R = 8.314\,\mathrm{J/mol}$, $\dot{\varepsilon}_{cr}$ is a steady state creep strain rate, σ is the equivalent stress.

This law reduces to a power law in the low stress area ($\alpha\sigma < 0.8$) and to an exponential model in the high stress area ($\alpha\sigma > 1.2$) [16–18]. The hyperbolic sine creep model is adequate for most lead and lead-free solder materials, and it is used in the present study to simulate the viscous behaviour of the solder joint due to its high operating temperatures. The creep parameters, obtained by Schubert et al. for Sn3.8Ag0.7Cu solder material, are used in the creep analysis [14, 16].

Downloaded By: [Silberschmidt, Vadim V.] At: 09:56 29 September 2008

Thermal Loading and Boundary Conditions

To properly estimate the effect of the real spatially non-uniform temperature distributions on evolution of thermal stresses, three cases of thermal boundary conditions are applied to the resistor assembly in the finite element elasto-plastic and creep analysis. Each case represents a various type of accounting for thermal conditions within the same thermal history consisting of the reflow process and dwell at room temperature before thermal cycling. The reflow simulation in terms of cooling from the melting point gives an amount of residual stress induced in the solder joint when the temperature of the assembly brought down from 490 K to the room temperature. A typical thermal history used in thermal stress analysis is given in Figure 9, with duration of the total temperature cycle (DEFGH) 1320 sec. Point H in Figure 9 denotes the end of the first thermal cycle and the begin of the next one. All the subsequent cycles have the same thermal history as DEFGH. Following are the three different cases used in the finite element analysis of continuously heat dissipating chip with a varying ambient temperature during thermal cycles after reflow and the dwell at the room temperature.

Case A: In this case, spatially uniform temperature distributions are assumed the entire resistor assembly, e.g., during hot dwell (DE) the entire assembly is at 398 K, while during the cold dwell (FG) it is at 218 K.

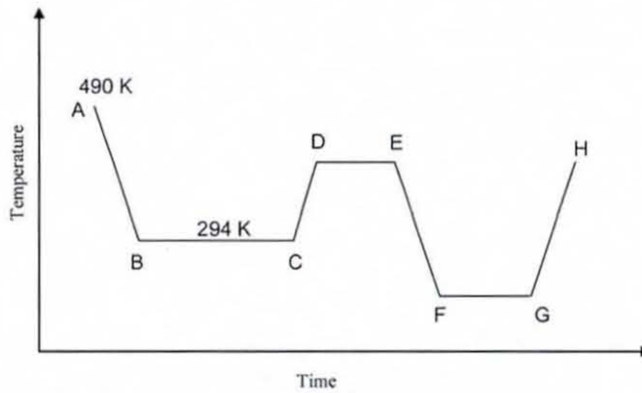


Figure 9 A typical thermal history used in thermal stress analysis: Cooling from 490 K (AB) – 48 sec; dwell at room temperature (BC) – 3600 sec; ramp CD – 300 sec; hot & cold dwell (DE, FG) – 300 sec; ramps EF & GH – 360 sec.

Downloaded By: [Silberschmidt, Vadim V.] At: 09:56 29 September 2008

Case B: In this case, Eq. (1) is used to obtain the temperature of the substrate in dependence of that on the component. For instance during hot the dwell (DE) a uniform temperature of 398 K is applied to the chip component, solder joint and copper pad, while the substrate's temperature is 321.5 K. During the cold dwell (FG) the chip component, solder joint and copper pad are at 294 K and the substrate temperature is 218 K. It is assumed that the assembly has the same temperature gradient as for the hot dwell due to continuous heat dissipation at its maximum power.

Case C: In Case C, the actual temperature gradient based on the thermal FE analysis for the chip resistor operating at its full load and the varying ambient temperature is considered. Hence, the temperature profile shown in Figure 8(a) is used for the hot dwell (DE) and the one in Figure 8(b) is used for the cold dwell (FG).

A symmetry boundary condition is applied on the symmetry faces (Fig. 6) of the assembly to represent the structural symmetry and to prevent a rigid body motion. The bottom nodes on the symmetry plane are also constrained to prevent the rigid body motion in the Y-direction.

RESULTS AND DISCUSSIONS

In our finite element analysis, the chip resistor is subjected to 5 temperature cycles (see Fig. 9). The results of simulations are presented only for the solder joint, since it is our area of interest. The reflow process is commonly used in surface mount devices to create solder joints. In this process the whole assembly passes through an oven where the maximum temperature is above the melting point of the lead-free solder alloy. Hence, it is important to know the stress induced in the solder joint due to cooling of the assembly in the reflow process from 390 K to room temperature. Different components of the thermal stresses in the solder joint are studied after the reflow and shown in Figure 10. The distributions of the thermal stresses show that

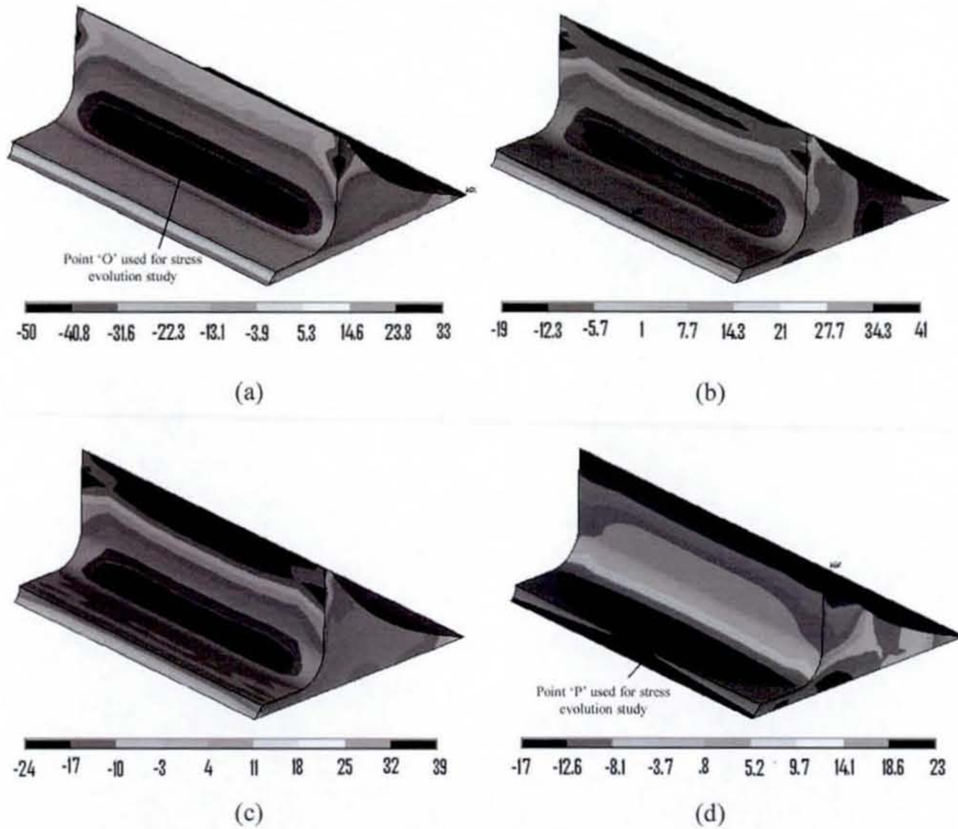


Figure 10 Distribution of thermal stresses in solder joint after reflow: (a) σ_{xx}; (b) σ_{yy}; (c) σ_{zz}; (d) σ_{xy}.

Downloaded By: [Silberschmidt, Vadim V.] At: 09:56 29 September 2008

the fillet of the solder joint is the area of stress concentration and the magnitude of the residual stress induced in the solder joint is above the yield stress of the SAC solder alloy at room temperature -38 MPa. As expected, σ_{xx} is the dominant stress component due to the contraction of the assembly with decrease in temperature, which also results in shear stress σ_{xy}. The variation of the component stress σ_{xx}, at location of stresses with maximum magnitude (compressive in this case) in the fillet (point 'O' in Fig. 10a), over the dwell at room temperature and temperature cycles was studied and is shown in Figure 11(a). The room-temperature dwell results in a relatively quick decrease of residual stresses during the first 10 min. due to the relaxation process. The latter decelerates after this initial stage of the dwell, resulting in 62% decline after first hour. The stress variation is presented only for 3 cycles due to a transition to a quasi-stable configuration after first four thermal cycles. The evolution of the component stress demonstrates the effect of three different thermal boundary conditions.

The magnitudes of stress are similar for Cases B and C; however Case A induces compressive stresses of higher magnitude than in B and C. Another important observation is that in the case of the uniform temperature distribution (Case A) the relaxation of stress at cold dwell is absent due to a lower homologous

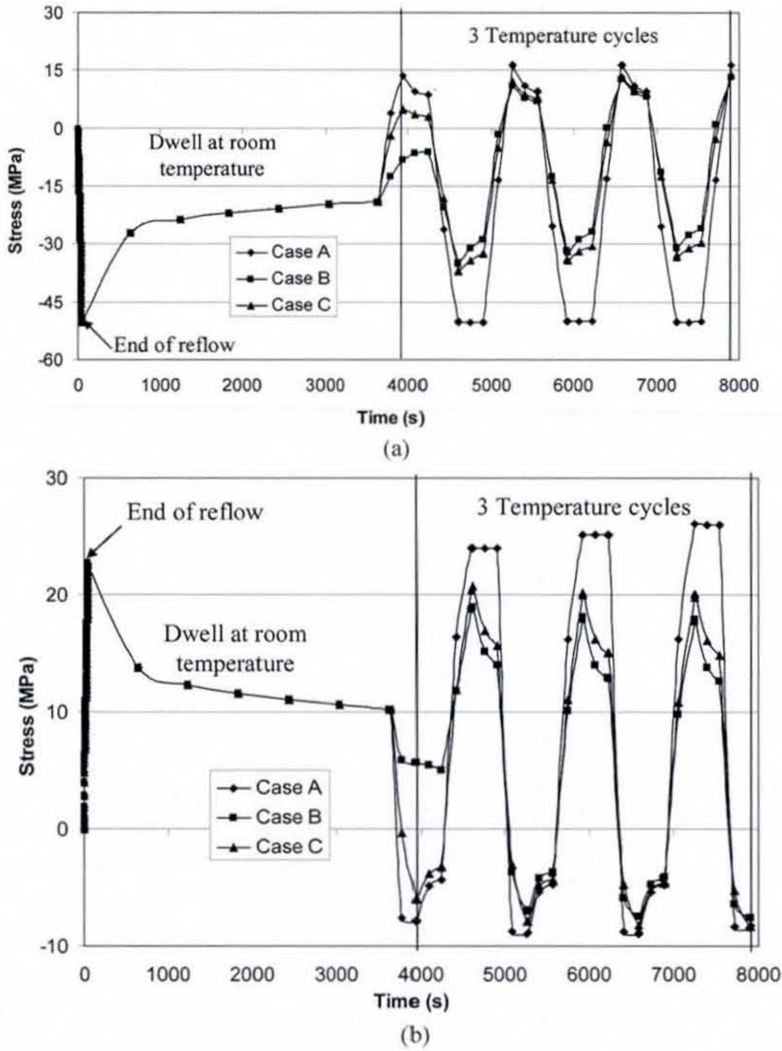


Figure 11 Evolution of (a) component stress σ_{xx} and (b) shear stress σ_{xy}.

Downloaded By: [Silberschmidt, Vadim V.] At: 09:56 29 September 2008

temperature ($T_h = 0.44$). But at hot dwell all three cases show comparable extents of relaxation due to higher T_h. As temperature cycling progresses the stress levels at hot dwell practically coincide for all three cases. The evolution of shear stresses in the solder joint is also studied for the maximum stress location in the fillet (point 'P' in Fig. 10(d)). Figure 11(b) demonstrates the variation of shear stresses for reflow, relaxation at room temperature and 3 temperature cycles. The general character and main features of the shear stress evolution are similar to those for the stress component σ_{xx}, with Case A exhibiting higher stress levels and Case C lower stress levels. Here also no relaxation of stress at cold dwell is observed in case of Case A, and stress levels converge for all three cases at hot dwell as the cycle progresses.

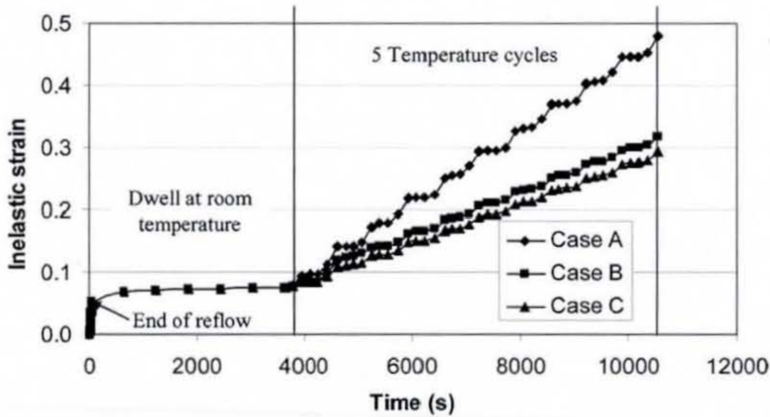


Figure 12 Accumulation of inelastic strain.

Downloaded By: [Silberschmidt, Vadim V.] At: 09:56 29 September 2008

Since the stress levels induced in the solder joint are in plastic region, they cause an irreversible strain in it. At the same time, deformation in the solder joint due to creep also contributes to the permanent strain. Therefore inelastic strain, caused by a combined effect of plasticity and creep, was calculated for the solder joint at point 'P' in the fillet. Figure 12 shows the evolution of inelastic strain for Cases A, B and C. All three cases correspond to thermal ratcheting after the reflow and dwell at room temperature: each thermal cycle results in the incremental increase in the levels of inelastic strains. As expected, the accumulated inelastic strain (permanent) strain at the end of 5 temperature cycles is maximum for Case A, while that in Case C is minimum.

The inelastic strain accumulation after five thermal cycles is 33% and 40% lower for Cases B and C, respectively, than that in Case A. In the latter case, there is no inelastic strain accumulation at cold dwell due to low homologous temperature, resulting in the absence of stress relaxation. In contrast the inelastic strain accumulation takes place for both hot and cold dwells in Cases B and C. However, the amount of accumulation is greater for cold dwell than that of hot dwell due to higher level of stress in the solder joint during cold dwell.

CONCLUSIONS

In this paper, the experimental work is aimed at determination of the temperature profiles in the working flip-chip assembly. It is demonstrated that the real spatial temperature distributions are not uniform, resulting in thermal gradients in the assembly. Finite element simulations are used to study the effect of non-uniformity as opposed to the standard assumption of uniform temperature distributions in microelectrinics components when they are powered. This is implemented in terms of three variants of thermal boundary conditions, linked to experimental results. Their effect on thermal stresses and inelastic strain accumulation in the surface-mount solder joint is studied. From the three cases considered, the non-uniform temperature distribution (Case C) in the resistor assembly demonstrates the lowest stress levels as well as inelastic strain

accumulation while the uniform temperature distribution (Case A) demonstrates the highest ones. Obviously, the common assumption of the uniform temperature field in powered component overestimates thermal ratcheting for the studied loading history. Therefore, it is very important to consider the actual temperature distribution rather than a uniform one in the finite-element simulation to study stress and strain conditions in the solder joint.

REFERENCES

1. C. Lea, *A Scientific Guide to Surface Mount Technology*, Electrochemical Publications Ltd, Isle of Man, UK, 1988.
2. Q. D. Yang, D. J. Shim, and S. M. Spearing, A Cohesive Zone Model for Low Cycle Fatigue Life Prediction of Solder Joints, *Microelectr. Engng.*, vol. 75, pp. 85–95, 2004.
3. N. Noda, R. B. Hetnarski, and Y. Tanigawa, *Thermal Stresses*, Taylor & Francis, New York, 2003.
4. P. Hegde, A. R. Ochana, D. C. Whalley, and V. V. Silberschmidt, Finite Element of Lead-free Surface Mount Devices, *Comput. Mater. Sci.*, vol. 43, pp. 212–220, 2008.
5. P. Hegde, D. C. Whalley, and V. V. Silberschmidt, Creep Damage Study at Powercycling of Lead-free Surface Mount Devices, *Comput. Mater. Sci.*, In press, 2008.
6. M. Gonzalez, B. Vandevelde, and E. Beyne, Thermo-Mechanical Analysis of a Chip Scale Package (CSP) Using Lead Free and Lead Containing Solder Materials, *Proc. 3rd European Microelectronics and Packaging Symposium*, Prague, Czech Republic, p. 247, 2004.
7. J. H. L. Pang, D. Y. R. Chong, and T. H. Low, Thermal Cycling Analysis of Flip-Chip Solder Joint Reliability, *IEEE Trans. Compn. Packag. Technol.* vol. 24, pp. 705–712, 2001.
8. A. R. Ochana, D. A. Hutt, D. C. Whalley, F. Sarvar, and A. Al-Habaibeh, Modelling of the Power Cycling Performance of a Si on Si Flip Chip Assembly, *Proc. 10th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronics Systems*, ITHERM, San Diego, CA, USA, p. 243, 2006.
9. *ANSYS Theory Reference Manual*, Swanson Analysis System, Inc., Houston, TX, USA, 2000.
10. J. H. Lau, *Thermal Stress and Strain in Microelectronics Packaging*, Van Nostrand Reinhold, New York, 1993.
11. W. Qiang, L. Lihua, C. Xuefan, and W. Xiaohong, Experimental Determination and Modification of Anand Model Constants for Pb-free Material 95.5Sn4.0Ag0.5Cu, *Proc. 8th Int. Conf. on Thermal, Mechanical and Multiphysics Simulation and Experiments in Micro-Electronics and Micro-Systems*, EuroSimE, London, UK, p. 308, 2007.
12. J. H. L. Pang and B. S. Xiaong, Mechanical Properties for 95.5Sn3.8Ag-0.7Cu Lead-free Solder Alloy, *IEEE Transactions Components and Packaging Technologies*, vol. 28, pp. 830–840, 2005.
13. S. Wiese, E. Meusel, and K. J. Wolter, Microstructural Dependendence of Constitutive Properties of Eutectic SnAg and SnAgCu Solders, *Proc. 53rd Electronic Components and Technology Conference*, New Orleans, LA, USA, p. 197, 2003.
14. A. Schubert, R. Dudek, E. Auerswald, A. Gollhardt, B. Michel, and H. Reichl, Fatigue Life Models of SnAgCu and SnPb Solder Joints Evaluated by Experiements and Simulations, *Proc. 53rd Electronic Components and Technology Conference*, New Orleans, USA, p. 603, 2003.
15. Q. Zhang, A. Dasgupta, and P. Haswell, Viscoplastic Constitutive Properties and Energy-Partioning Model of Lead-Free Sn3.9Ag0.6Cu Solder Alloy, *Proc. 53rd Electronic Components and Technology Conference*, New Orleans, LA, USA, p. 1862, 2003.

Downloaded By: [Silberschmidt, Vadim V.] At: 09:56 29 September 2008

16. A. Syed, Accumulated Creep Strain and Energy Density Based Thermal Fatigue Life Prediction Models for SnAgCu Solder Joints, *Proc. 54th Electronic Components and Technology Conference*, Las Vegas, NY, USA, p. 737, 2004.
17. J. P. Clech, Comparative Analysis of Creep Data for Sn-Ag-Cu Solder Joints in Shear, *Micromaterials and Nanomaterials*, pp. 144–154, 2004.
18. R. Darveaux and K. Banerji, Constitutive Relations for Tin-Based-Solder Joints, *IEEE Trans. Components, Packaging, and Manufacturing Technology*, vol. 15, pp. 538–551, 1992.
19. C. W. Chong, Z. T. Xiaowu, and T. C. Chai, Board Level Solder Joint Life Prediction of Fine Pitch Large IC, *Proc. Electronics Packaging Technology Conference*, Singapore, p. 302, June 2006.

Downloaded By: [Silberschmidt, Vadim V.] At: 09:56 29 September 2008

Thermo-mechanical Damage Accumulation during Power Cycling of Lead-Free Surface Mount Solder Joints

Pradeep Hegde, David C. Whalley, Vadim V. Silberschmidt
Wolfson School of Mechanical and Manufacturing Engineering, Loughborough University,
Loughborough, Leicestershire, LE11 3TU, UK
Email: p.hegde@lboro.ac.uk

Abstract

It is well known that in surface mount technology (SMT), thermal strains in electronic assemblies are induced in the solder joints by the mismatch between the coefficients of thermal expansion (CTE) of the components, substrate and solder, both during their processing and in service. Therefore, thermo-mechanical damage is likely to occur in the solder and the principle reliability hazard in SMT assemblies is the resulting fatigue cracking of the solder fillet, caused by cyclic thermal stresses. These stresses may be caused by both cyclic variations in power dissipation within equipment and by external environmental temperature changes. Most work reported to date has focused on the effects of environmental temperature changes, although for many types of equipment power cycling may result in significant stresses. The present paper describes the experimental determination of the actual temperature distribution in a chip resistor assembly when it is powered. The paper also discusses the significance of such experimentally determined non-uniform temperature distributions in electronic assemblies to fatigue damage accumulation due to both power cycling and to cyclic variations in the ambient temperature whilst the chip resistor is powered. This fatigue damage accumulation study is carried out using finite element analysis.

Introduction

The primary functions of solder joints in electronic assemblies are to achieve electrical connectivity and structural integrity, but structural integrity is a requirement for conductivity. The functional reliability of electronic products therefore depends on the structural reliability of the solder joints. Due to the ban imposed on use of SnPb solders in many electronic applications, most manufacturers have been forced to adopt lead-free solders. Eutectic and near eutectic SnAgCu solders have been widely adopted as replacements for the well established SnPb based solders. Any lead-free solder must have its reliability studied in the anticipated operational conditions before implementation in electronic products.

In typical applications, solder joints form a bridge between a substrate and the components. The difference in coefficient of thermal expansion (CTE) between the substrate and component may cause significant thermal stresses during operation. For the reliable functioning of electronic products, solder joints must accommodate the thermal strains caused in operation due to the mismatch in CTEs. The ability of solder to withstand considerable fatigue damage is critical for the reliable functioning of electronic products. Stronger solder materials that could resist these thermal stresses without fatigue damage could result in an unacceptable change in the failure mode, with failures occurring in the component or substrate rather than in the solder [1]. The most commonly used solders in electronic applications are Sn based. These are prone to thermal fatigue damage because the thermal anisotropy of the β-Sn phase causes intergranular fatigue damage upon thermal loading [2, 3].

Solder joints are subjected to thermo-mechanical fatigue damage during operation with the fluctuation of local temperature. The repeated heating and cooling of electronic devices induces cyclic strain in the solder joint resulting from the CTE mismatch between component and substrate. The operating temperature may vary between extremes as wide as 218K to 398K, depending on the application in which the electronic device is being used. This means typical lead-free solder joints, with melting points of around 217°C (490K), operate at homologous temperatures (T_h) of between 0.45 and 0.81, which is sufficient for rapid creep deformation to occur under moderate loads. Hence, studies of the fatigue damage in solders must consider creep behaviour. Experimental methods such as shear or mechanical shock tests which may be used for solder joint bond strength determination do not provide any information about their fatigue behaviour. Hence, thermal cycling tests are commonly used to determine the fatigue damage due to cyclic variations in temperature, but it is laborious and time-consuming. Therefore, finite element analysis has been employed in recent years to simulate the damage phenomenon with consideration of different field operating conditions. However, most of the reported finite element simulations of thermal fatigue damage in solders have been carried out considering thermal cycling, which is application of a changing, but uniform temperature distribution across the electronic assembly, which is contrary to the actual temperature distribution [4, 5]. In applications such as automotive, aerospace etc., the ambient temperature can vary significantly when the electronic devices are in operation. This type of situation is very difficult to include in accelerated life testing to understand its influence on the fatigue damage. However, in finite element analysis such varying operating conditions can be readily included.

978-1-4244-2814-4/08/$25.00 ©2008 IEEE

2nd Electronics Systemintegration Technology Conference
Greenwich, UK

In this paper, the temperature distribution in a chip resistor assembly is determined using infrared thermography. These temperature distributions are then used as boundary conditions in a finite element creep analysis to replicate the infield thermal conditions during power cycling. A comparison of the resulting creep damage is made between application of a uniform and non-uniform temperature distribution within the chip resistor. Finite element analysis is also carried out for cyclic variations of ambient temperature with the chip resistor continuously powered.

Experimental Work

Procedure

Infrared (IR) thermography was used to determine the temperature profile in a typical chip resistor for power cycling. A schematic diagram of the temperature measurement set up is shown in Fig. 1. The experimental set up consists of a Thermosensorik camera, a 1206 chip resistor assembled on to a FR4 substrate, and a power supply. The details and background on these thermography experiments are given in [6].

Figure 2 shows the construction of the chip resistor used in the experiment. The chip resistor consists of an alumina substrate on which a thick film resistive element is printed. The thick resistive element is covered with a polymer resin based protective coating. The alumina substrate is covered with a solderable electrode termination at the ends. The chip resistor is mounted on a 1.6 mm thick FR4 substrate which has 35μm thick copper tracks used for powering the chip resistor. The 1206 chip resistor is rated to operate in the temperature range between 218K and 428K with a maximum power dissipation of 0.25W up to an ambient temperature of 343K, reducing to 0W at 428K. The resistor is reflow soldered to the copper tracks using Sn3.8Ag0.7Cu (SAC) solder with a melting point of 490K. The resistor assembly was sprayed with a thin layer of a matt black paint to provide a uniform high emissivity temperature measurement surface. The experiment was carried out for two different loading conditions: (A) the full rated load (0.25W) and (B) a derated load (0.15W). The chip resistor was powered and, after the temperature distribution had stabilised, the temperature profile was captured with the IR camera.

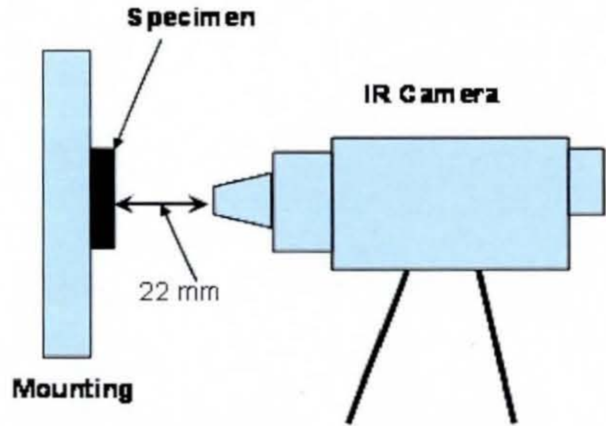


Fig. 1: Schematic diagram of experimental setup

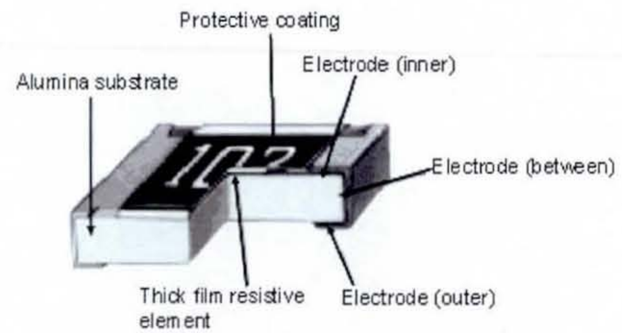


Fig. 2: Construction of a 1206 chip resistor [7]

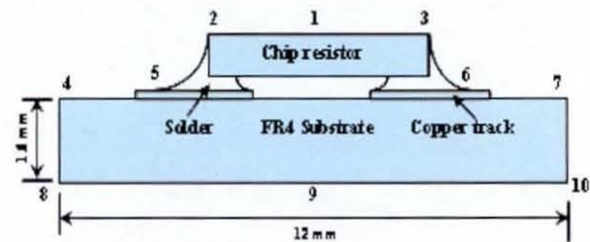
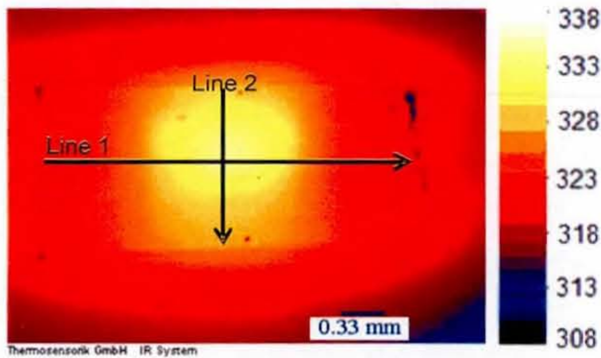


Fig. 3: Geometrical model of the chip resistor assembly

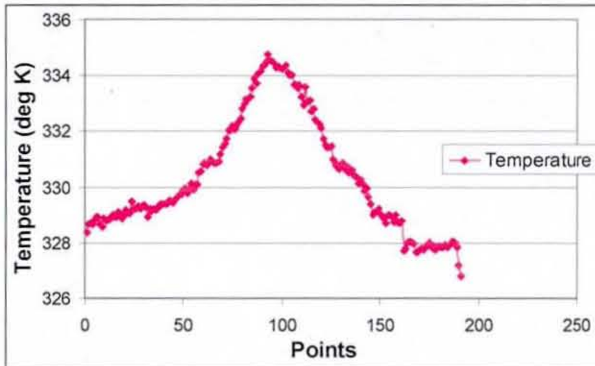
Results and Discussion

A. Full load (0.25W): The temperature distribution in the chip resistor at 0.25W is shown in Fig. 4(a). The maximum temperature of 334.5K was at the centre of the thick film resistive element, where the heat is generated, and decreased towards the boundaries of the chip. The temperature distribution was also evaluated across the length and width of the chip resistor. Figures 4(b) and (c) show the variation of temperature along lines 1 and line 2. The temperature distribution along line 1 is symmetrical, while that of line 2 is skewed towards one side. Manufacturing deficiencies wherein the heat generating resistive element is skewed towards one side may be the reason for the asymmetrical temperature distribution along line 2.

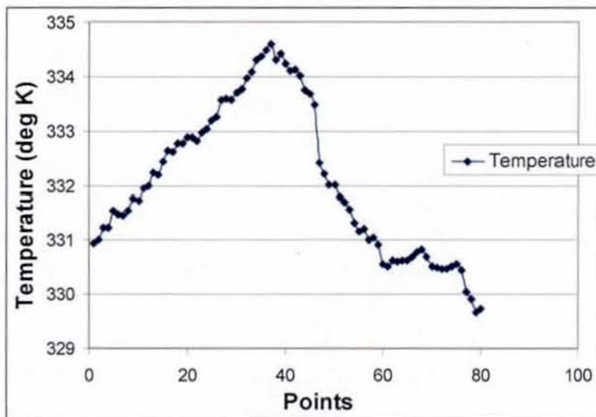
The temperature distribution obtained using the IR camera was validated by comparison with temperature measurements from thermocouples bonded to the sample at the locations indicated in Fig.3 on the central line. Calibrated K-type thermocouples with a wire diameter of 40 μm were used and these thermocouples were connected to a digital thermometer. Table 1 presents a comparison of the temperatures at these locations. The temperatures pretty well match for both measurement methods with a maximum discrepancy of 1K. The temperature gradient, which is the difference between the maximum and minimum temperature, in the chip resistor assembly is calculated to be 22.5K for the full load condition.



(a)



(b)



(c)

Fig. 4: Temperature distributions in the chip resistor: (a) over chip surface; (b) along line 1; (c) along line 2.

The full load experiment was repeated for a higher room temperature (297.5K) to understand its effect on the temperature gradient in the assembly. The temperature measurements for this condition are also shown in Table 1. The temperature distribution in the chip is similar to that observed at the lower room temperature (295K). The maximum temperatures in the chip increased marginally, while the temperature gradient in the assembly decreased by one degree. Again, the comparison of temperature between thermocouple and thermal camera measurement is good, with a maximum discrepancy of 3K at the chip centre. The drop in temperature gradient may not be significant; however, since the thermal strain in the solder joints is the direct effect of the temperature gradient in the assembly, and the temperature distribution at a room temperature of 295K was used in the subsequent finite element analysis.

Table 1 Measured temperature using thermocouples and thermal camera at full load (0.25W)

Location (Fig. 3)	Room Temperature 295K		Room Temperature 297.5K	
	Thermo-couple	Therma l Camera	Thermo - couple	Thermal Camera
1	333.5	334.5	335.5	338.5
2	329.0	328.0	330.0	328.0
3	327.0	327.0	329.5	326.0
4	312.0	311.0	317.5	316.5
5	326.0		328.0	
6	325.0		327.0	
7	312.0	311.0	317.0	316.0
8	311.0		314.0	
9	318.0		319.0	
10	311.0		314.0	

Thermal Finite Element Analysis

A 2D finite element thermal analysis was carried out, using the experimentally determined temperature distribution in the chip resistor as the boundary conditions, to obtain the full temperature distribution for use in the following creep analysis. Figure 5 (a) shows the temperature boundary conditions used at different locations on the assembly for thermal analysis. The locations of the boundary conditions are similar to those used for temperature measurement comparison. The symmetry plane is considered to be an adiabatic surface, i.e. without any temperature boundary conditions applied to it. A linearly varying temperature is applied only on the bottom surface of the substrate to replicate the experimental temperature distribution in the assembly. Material properties used for the thermal analysis are presented in Table 2. The obtained temperature distribution after thermal analysis is shown in Fig. 5(b).

Table 2 Material properties used in thermal analysis

Material	Density (gm/cm3)	Thermal conductivit y (W/mK)
Alumina	3.97	25
Solder (SAC)	7.5	60.32
Copper	8.96	400
FR4	1.96	0.3

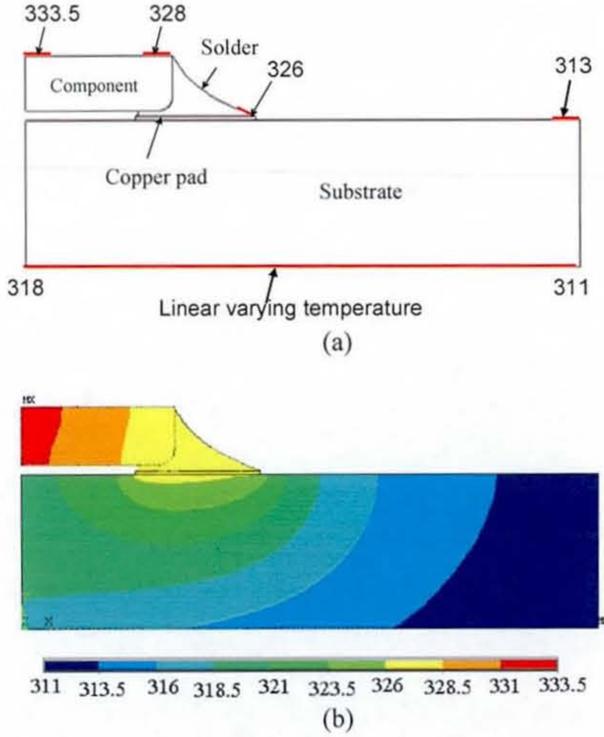


Fig. 5: Thermal analysis of chip resistor assembly at 0.25W: (a) temperature boundary conditions used; (b) predicted temperature distribution (K)

B. Derated load (0.15W): As the ambient temperature increases, the maximum allowable power dissipation in the chip resistor decreases. An experiment was carried out to establish the temperature distribution in the chip resistor while it is operating at an ambient temperature of 398K. At this temperature, the maximum load at which the 1206 chip resistor can be operated is 0.15W.

Figure 6(a) shows the temperature distribution in the chip resistor for the derated load of 0.15W, which resembles the temperature distribution for full load condition, but with a decrease in the magnitude of the temperature rise above ambient. The maximum temperature is again, as expected, observed at the centre of the chip and the variation of temperature along line 1 and line 2 is similar to that observed for full load. The thermal camera temperature measurements and those from the thermocouples again match very closely, as shown in Table 3. The temperature gradient observed in the assembly is 12.5K, which is proportional to the decrease in power input to the specimen.

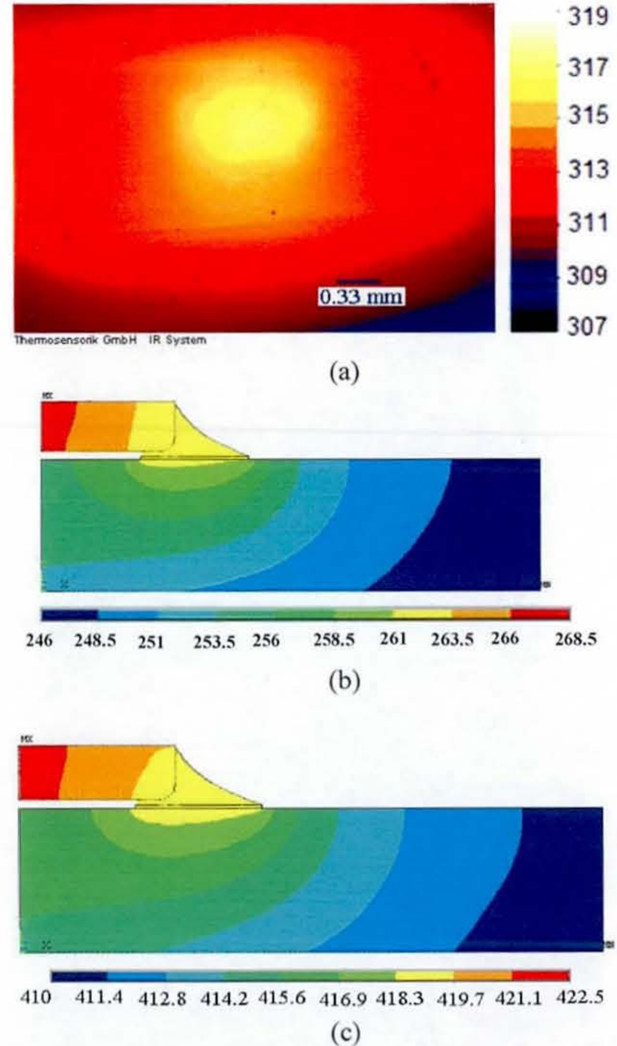


Fig. 6: Temperature distribution at 0.15W: (a) measured over chip surface (b) predicted for an ambient temperature of 218K; (c) predicted for an ambient temperature of 398K (K)

The thermal analysis was repeated for ambient temperatures of 218K and 398K, using both the full and derated load temperature distribution as boundary conditions respectively. This was carried out to establish the full temperature distribution in the assembly for continuously heat dissipating chip resistor with varying ambient temperatures between 218K and 398K. The locations (Fig. 5(a)) of the thermal boundary conditions are the same as used for the full load condition. Figures 6 (b) and (c) show the temperature distribution obtained after thermal analysis respectively for ambient temperatures of 218K and 398K, and these temperature profiles are later used in the cyclic creep analysis for variation of the ambient temperature between 218K and 398K with the chip resistor powered.

Table 3 Measured temperatures from thermocouples and thermal camera for derated load (0.15W)

Location (Fig. 3)	Room Temperature 295K	
	Thermo-couple	Thermal Camera
1	318.5	318.0
2	316.0	315.0
3	315.0	314.0
4	308.0	307.0
5	315.0	
6	314.0	
7	306.0	306.0
8	306.0	
9	312.0	
10	306.0	

Structural Finite Element Analysis

FE Model, Loads and Boundary Conditions

A 2D finite element (FE) model of the chip resistor assembly was built for the creep analysis. The FE modelling was done using plane strain elements, which have been shown to provide an accurate simulation of such chip resistor assemblies [9]. Only one-half of the geometry is considered in the finite element analysis, making use of the structure's symmetry. Figure 7 shows the quality of mesh used in the critical region of the solder joint of the chip assembly.

The majority of solder joints failures in electronic packaging are due to thermo-mechanical/creep fatigue. Therefore, only thermal loads are considered in the finite element analysis. The thermal history used in the power cycling simulation is detailed in Fig. 8. Creep analysis was carried out for three thermal loads:

Case 1: Non-uniform temperature distribution (Fig. 5(b)) in the chip resistor assembly at hot dwell (line DE in Fig. 8), which represent the power cycling simulation.

Case 2: Uniform temperature distribution in the chip assembly at hot dwell (DE) of the thermal history with the maximum temperature of 333.5K taken from the full load thermal simulation at room temperature. This represents the thermal cycling simulation.

Case 3: For the finite element creep analysis including cyclic variation of the ambient temperature with a continuously heat dissipating chip, the chip resistor assembly is cycled between the temperature profile obtained for ambient temperature 398K at hot dwell (line DE in Fig. 8) and 218K at cold dwell (line FG in Fig. 8).

A symmetry boundary condition is used to represent the structural symmetry of the assembly and to prevent rigid body motion in the X-direction. The lowest node on the symmetry plane is also constrained in the Y-direction to prevent rigid body motion.

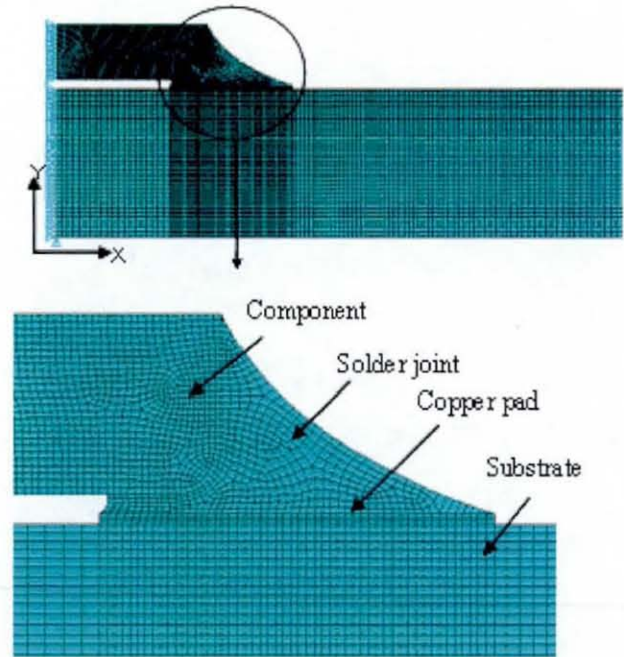


Fig. 7: Finite Element Model of 1206 resistor

Material Properties

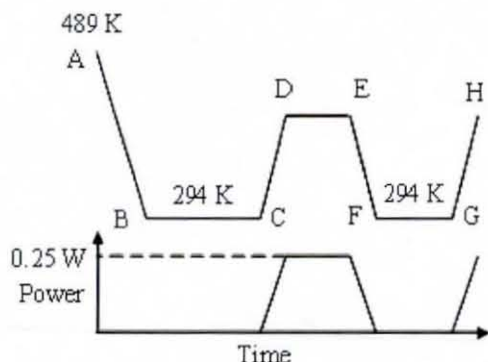
The finite element model consists of a component, solder joint, copper pad and substrate, which are modelled using published material properties for alumina, Sn3.8Ag0.7Cu, copper and FR4 respectively [8,9]. Since many material properties vary significantly with temperature, temperature-dependent material properties are used in the analysis. Most materials undergo rapid creep deformation at temperatures above $0.4T_h$. The solder, but none of the other materials in the assembly, operate well above 0.4Th ($0.55T_h$ and $0.68T_h$), therefore, a creep material model is introduced for the solder joint to capture the effect of creep and therefore allow estimation of fatigue damage during power cycling. Material properties for the SnAgCu solder joint are presented in Table 4 and a bilinear kinematic hardening (BKIN) material model is used for elasto-plastic modelling of the solder joint, which includes the Bauschinger effect due to cyclic loading. To reduce the model complexity and analysis time, only the solder joint is modelled using this elasto-plastic material model. The steady state creep behaviour of the SAC solder joint is modelled using the sine hyperbolic law:

$$\dot{\varepsilon}_{cr} = A[\sinh(\alpha\sigma)]^n \exp\left[\frac{-H}{RT}\right], \qquad (1)$$

where A = 277984, α = 0.02447, n = 6.41, H/R = 6500. $\dot{\varepsilon}_{cr}$ is a steady state-creep strain rate, σ is stress, T is absolute temperature [11].

Table 4 Material properties for SAC solder [8, 10]

Temperature (K)	Young's modulus (MPa)	CTE (ppm/K)	Yield Stress (MPa)	Tangent modulus (MPa)
298	32331	21.2	38	154
348	8285	21.7	30	134
423	6517	23.0	17	132



Cooling from 489 K (AB) = 48 sec

Dwell at room temperature (BC) = 3600 sec

Ramp DC = 300 sec

Ramp EF & GH = 360 sec

Hot & Cold dwell (DE, FG) = 300sec

Hot dwell peak temperature (DE) = 333.5 K

Temperature range = 39.5 K

Fig 8 Thermal history and power dissipation creep simulation

Results and Discussion

Case 1 & 2: This study is an extension to the work published in [8], where the same chip resistor assembly was cycled for five power cycles. The previous analysis work was performed with a similar set of boundary conditions, thermal history and material properties, but the stress-strain hysteresis loop had not stabilised after 5 power cycles resulting in a different strain range for each of the power cycles. Hence, the power cycling was continued for 10 cycles in this creep analysis. Since the solder joint is the main region of interest, a detailed study of stress and strain variation is carried out for the fillet of the solder joint, which is the location of both the maximum stress and strain.

The distribution of shear stress in the solder joint at the start of the hot dwell (point D in Fig. 8) and cold dwell (point F in Fig. 8) is shown in Fig. 9. It is clear from the stress distribution that both the thermal histories (Cases 1 & 2) predict similar stress variations in the solder joint. Evolution of shear stress in the solder joint is also studied and shown in Fig. 10. The figure shows the stress evolution for reflow, dwell at room temperature and two power cycles. Even though ten power cycles are simulated, the shear stress variation is shown only for two power cycles, since the stress cycle repeats for subsequent cycles due to thermal ratcheting. Simulation of reflow shows the considerable amount of residual shear stress (24 MPa) in the solder joint after reflow soldering.

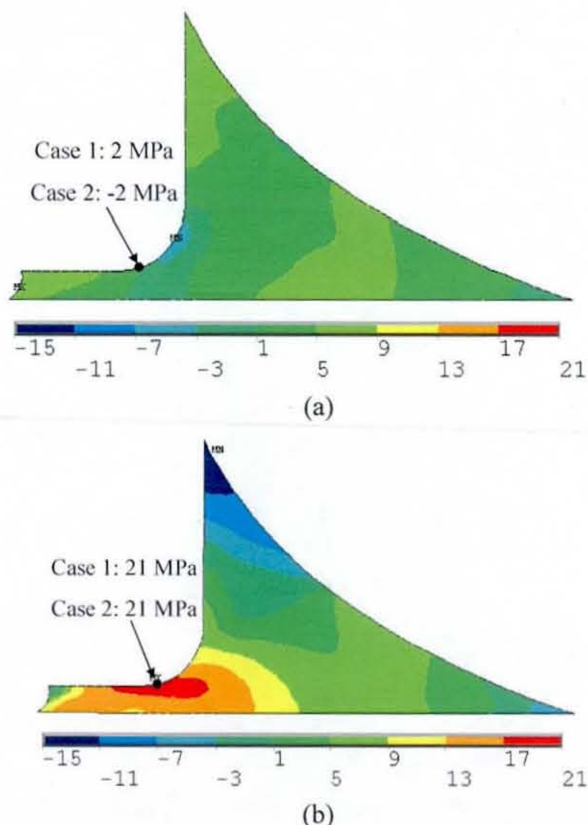


Fig. 9: Shear stress in solder joint: at point D (a) and F (b) of the thermal history (Fig. 9)

An hour dwell at room temperature, before the assembly is cycled, results in relaxation of the residual stress (reduction from 24 MPa at the end of reflow to 12 MPa) induced during manufacturing of the assembly. The maximum shear stress in each power cycle did not exceed the initial residual stress of 24 MPa, which indicates that stress levels induced in the solder joint during power cycling are within the new yield stress. The shear stress range was also studied and remained constant (24 MPa for Case 1 and 26 MPa for Case 2) over the power cycle, which is also evident from the stress evolution shown in Fig. 10.

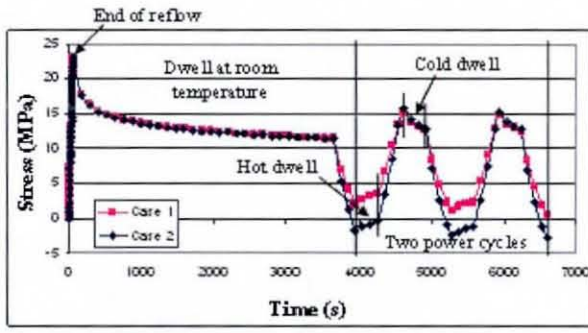


Fig. 10: Evolution of shear stress in the solder joint

The fatigue damage in the solder joint is studied by considering the inelastic strain accumulation during creep analysis. Figure 11 shows the accumulation of inelastic strain due to creep after reflow, dwell at room temperature and ten power cycles. The strain accumulation increases with time and Case 2 has a higher accumulation than Case 1. The difference in the inelastic strain accumulation at the end of ten power cycles is 5%.

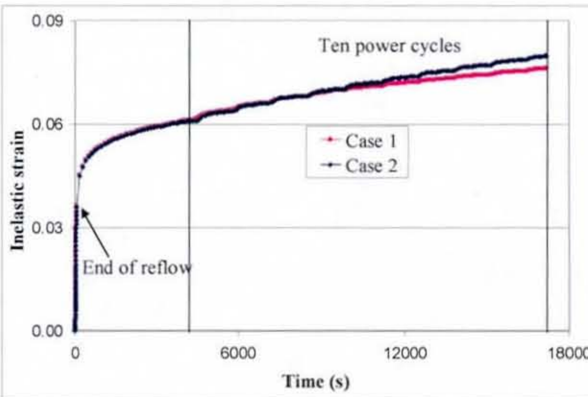


Fig. 11: Evolution of inelastic strain in solder joint

In fatigue life calculations using the strain based Coffin-Manson method, the inelastic strain range for a stabilised thermal/power cycle is used. Hence, the inelastic strain range for every power cycle is analysed. Table 5 shows the calculated inelastic strain range over each power cycle for both of the thermal histories (Cases 1 & 2). This shows an initial decrease in strain range as each cycle progresses, but unlike the authors previously reported creep study [9], the strain range reaches a constant value after the 9th power cycle, which shows the stabilisation of stress-strain hysteresis. Comparison of the inelastic strain range between cases 1 & 2 shows the importance of a non-uniform temperature distribution in the chip assembly. The uniform thermal history (Case 2) always shows a higher strain range than the non-uniform thermal history (Case 1). An inelastic strain range difference of 50% is observed at the end of the cycle stabilisation. This difference has a direct implication for the fatigue life on the solder joint.

Table 5 Inelastic strain range for power cycles

Power cycle	Inelastic strain range		% variation
	Case 1	Case 2	
1	0.0028	0.0028	0
2	0.0022	0.0024	9
3	0.0019	0.0022	16
4	0.0016	0.0020	25
5	0.0013	0.0019	46
6	0.0012	0.0018	50
7	0.0011	0.0017	42
8	0.0011	0.0016	45
9	0.0010	0.0015	50
10	0.0010	0.0015	50

Case 3: Finite element creep simulations were also carried out for powered chip resistor within an ambient temperature varying between 218K and 398K. The simulations were carried out for ten cycles and the shear stress variation is shown in Fig. 12. The shear stress distribution in the solder joint is similar to that in Fig. 9, but with slightly higher magnitude due to the higher thermal load. The stress variations were similar to Case 2 of power cycling, but also with increased magnitude.

The shear stress range and inelastic strain range for this simulation is tabulated in Table 6. The shear stress range is constant between cycles, which is similar to that for the Case 1 & 2 simulations. However, unlike the Case 1 & 2 simulations, the cyclic inelastic strain range increases initially and attains stabilisation earlier. The stabilised inelastic strain range is 38 and 25 fold higher than for Case 1 and Case 2 respectively, which is due to the higher range of cyclic temperature. This will greatly reduce the solder joint fatigue life.

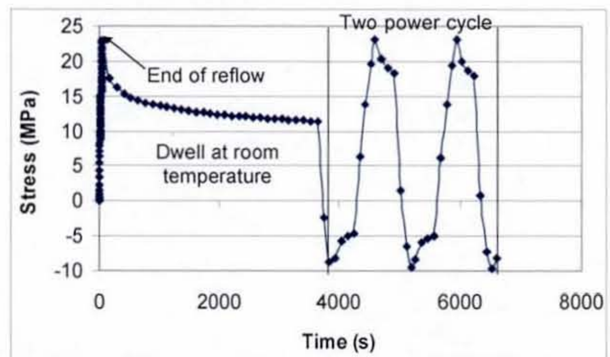


Fig. 12: Variation of maximum shear stress in the solder joint

Table 6 Inelastic strain range for cyclic variation of ambient temperature with chip resistor powered

Cycle	Shear stress range (MPa)	Inelastic strain range
1	32.6	0.0354
2	32.8	0.0363
3	32.9	0.0370
4	32.9	0.0375
5	32.9	0.0377
6	32.9	0.0379
7	32.8	0.0380
8	32.8	0.0380
9	32.8	0.0380
10	32.8	0.0380

Fatigue Life Estimation

The fatigue life for the solder joint was calculated based on the stabilised inelastic strain range. The commonly used Coffin-Manson relationship was used for the life estimation [11]:

$$N_f = (C'\varepsilon_{in})^{-1}, \quad (2)$$

where, N_f is the number of cycles to failure (fatigue life), C' is a constant, and ε_{in} is the accumulated inelastic strain range for a stabilised power cycle. For this study the value of C' used was 0.0468 [11]. Table 7 presents the calculated cyclic strain ranges used in fatigue life calculations, along with the predicted life for both power cycling and cyclic variation of ambient temperature with the chip resistor powered. As expected, there is a 50% improvement in the fatigue life of the solder joint with Case 1 in comparison with Case 2. However, in the case of cyclic variation of ambient temperatures, the fatigue life decreased drastically due to the higher level of stabilised cyclic inelastic strain.

Table 7 Predicted fatigue for solder joint

Thermal history		Inelastic strain range	Predicted fatigue life (cycles)
Power cycling	Case 1	0.0010	21367
	Case 2	0.0015	14245
Cyclic variation of ambient temperature		0.038	562

Conclusions

1. The experimental study shows that the temperature distribution in a powered electronic assembly is non-uniform, and consideration of a uniform temperature distribution for finite element analysis would result in an over estimation of the fatigue damage in the solder joints.
2. The creep study shows that the considerable amount of residual stress is induced in the solder joint by the reflow process but decays with dwell at room temperature. The stress cycle repeats with the subsequent power cycle because of thermal ratcheting.
3. The number of cycles before stabilisation of the stress-strain hysteresis loop in the power cycling analysis was 9, while for cyclic variation of ambient temperature analysis it was 7. This shows that the results of any simulations must be assessed on a case by case basis to ensure stabilisation has occurred.
4. Application of a non-uniform temperature distribution during the creep analysis results in a lower strain accumulation and a significant 50% difference in stabilized inelastic strain range has similar implication on the fatigue life calculation.
5. Creep analysis for cyclic ambient temperature variation significantly increases the stabilised strain range, which in turn affected the solder joint fatigue life.

The present study was carried out using published material properties for bulk Sn3.8Ag0.7Cu solder. In a future study, experimentally obtained material properties for solder within a joint will be used for modelling of both elasto-plastic and creep behaviour.

References

1. Dusek, M., and Hunt, C., "Crack Degradation Model Derived From Experimental Strain-Stress Data," *Proc. 8th Int. Conf. on Thermal, Mechanical and Multiphysics Simualtion and Experiments in Micro-Electronics and Micro-Systems,* EuroSIME 2007, London, pp. 297-302.
2. Erinc, M., Schreus, P.J.G. and Geers, M.G.D., "A Coupled Numerical and Experimental Study on Thermo-mechanical Fatigue in SnAgCu Solder Joints," *Proc. 8th Int. Conf. on Thermal, Mechanical and Multiphysics Simualtion and Experiments in Micro-Electronics and Micro-Systems, EuroSIME 2007*, London, pp. 707-712.
3. Telang, A.U., Bieler, T.R., Lucas, J.P., Subramanian, K.N., Lehman, L.P. Xing, Y. and Cotts, E.J. "Grain-boundary Character and Grain Growth in Bulk Tin and Bulk Lead-free Folder Alloys", *Journal of Electronic Materials*, Vol. 33, No.12,(2004) , pp. 1412-1423.
4. Warde, J. and Wallach, E.R., "The Prediction of Creep Damage in Surface Mount Components Using Finite Element Modelling," *NPL Report*

CMMT(A)218, Controller of HMSO, NPL, Teddington, UK, ISSN 1361-4061 March. 1999.

5. Gonzalez, M., Vandevelde, B. and Beyne, E., "Thermo-Mechanical Analysis of a Chip Scale Package (CSP) Using Lead Free and Lead Containing Solder Materials", *Proc. 3rd European Microelectronics and Packaging Symposium, iMAPS*, Prague, Czech Republic, June 2004, pp. 247-253.
6. Hegde, P., Ochana, A.R., Whalley, D.C. and Silberschmidt, V.V., "Finite Element Analysis of Lead-free Surface Mount Devices," *Computational Material Science*, article in press, September 2007.
7. Panasonic web page www.panasonic.com/industrial/components/pdf/001_er009_erj_1g_2g_3g_6g_8g_14_12_12z_1t_dne.pdf
8. Siewert, T., Liu, S., Smith, D. R., and Madeni, J. C., "Database for solder properties with emphasis on new lead-free solders", *National Institute of Standard and Technology & Colorado School of Mines*, Colorado, February 11, 2002.
9. Hegde, P., Whalley, D.C. and Silberschmidt, V.V., "Creep Damage Study at Powercyling of Lead-free Surface Mount Devices," *Computational Material Science*, article in press, 2008.
10. Qiang, W., Lihua, L., Xuefan, C. and Xiaohong, W., "Experimental Determination and Modification of Anand Model Constants for Pb-free Material 95.5Sn4.0Ag0.5Cu," *Proc. 8th Int. Conf. on Thermal, Mechanical and Multiphysics Simulation and Experiments in Micro-Electronics and Micro-Systems, EuroSimE* 2007, London, pp. 308-316.
11. Syed, A. "Accumulated Creep Strain and Energy Density Based Thermal Fatigue Life Prediction Models for SnAgCu Solder Joints," *Proc. 54th IEEE Electronic Components and Technology Conf*, Las Vegas, USA, June 2004, pp. 737-746.

Computational Materials Science xxx (2008) xxx–xxx

Contents lists available at ScienceDirect

Computational Materials Science

journal homepage: www.elsevier.com/locate/commatsci

Creep damage study at powercycling of lead-free surface mount device

Pradeep Hegde *, David C. Whalley, Vadim V. Silberschmidt

Wolfson School of Mechanical and Manufacturing Engineering, Loughborough University, Leicestershire LE11 3TU, UK

ARTICLE INFO

Article history:
Received 20 November 2007
Accepted 5 May 2008
Available online xxxx

PACS:
71.15.Dx
85.40.Bh

Keywords:
Powercycling
Lead-free solder
Creep analysis

ABSTRACT

Soldering is extensively used to assemble electronic components to printed circuit boards or chips to a substrate in microelectronic devices. These solder joints serve as mechanical, thermal and electrical interconnections, therefore, their integrity is a key reliability concern. However, newly introduced lead-free solders do not have a long history of applications in the industry and there is a lack of established material models of their behaviour over the wide temperature range experienced by electronics systems. Therefore, an extensive reliability study is required before introducing a new lead-free solder material in the electronic industries. Moreover, most of the solder materials have low melting temperatures, and are prone to creep in service. The cyclic temperature operating condition (powercycling) of the solder joint can result in the creep fatigue failure. Thus, a computational technique is used to investigate creep damage in solder joints. The present paper, deals with creep damage of lead-free solder joints for powercycling using finite element analysis with the consideration of experimentally observed non-uniform temperature distributions in the 1206 surface mount chip resistor. In addition, a comparison is made for inelastic strain accumulation and fatigue life for creep damage study for spatially uniform and non-uniform temperature powercycling.

© 2008 Elsevier B.V. All rights reserved.

1. Introduction

Solder joints provide both electrical connection and mechanical support to electronic devices, which makes them indispensable in electronic packaging. Tin-lead (SnPb) solders were first used for metal interconnections about 2000 years ago [1]. In electronic industry, eutectic or near-eutectic Pb-bearing solder alloys, which meet most of the requirements for a good solder material, are extensively used. Research to replace the well-established Pb-based solder alloys with new lead-free solder alloys has gained importance due to the introduction of legislation on removal of lead from all electronic products in most parts of the world. Although several commercial and experimental Sn-based Pb-free solder alloys exist, none can be considered as a full substitute to traditional Pb-based solders. This is due to a relatively low melting temperature of the latter as compared to new lead-free solders. Nevertheless, new solders need to possess the desirable material properties, reliability and manufacturability.

Solder joints used in the electronic packaging operate under high homologous temperatures (T_h, a ratio of operating temperature and melting temperature on absolute scale) compared to its melting temperature. The typical operating conditions of solder joints are powercycling, vibration and impact (e.g. due to drops) loading and changes in environmental temperature. Integrity of solder joints is critical for reliable functioning of electronic components. The dominant type of failure in solder joints is creep fatigue due cyclic variations of load. Therefore, it is imperative to study the reliability aspects of new Pb-free solder joints in electronic packages before its broad use in various electronic packing. Accelerated temperature cycling (ATC) is a well-established experimental test used to study the reliability in the electronic industry. In this test, electronic components are placed in a chamber, in which temperature is cycled between extreme magnitudes. During this test, at each instant, the oven operates quasi-statically, reaching a uniform temperature practically instantaneously.

The popularity of the accelerated thermal cycling is due to its simplicity in concept and operation. However, in recent years, there is an increasing debate on the applicability of thermal cycling tests for reliability studies since under the actual operating conditions, the heat is generated by a powered electronic device, and as a result, the package is under anisothermal conditions [2]. Thus, it is believed that powercycling accelerated tests, which result in uneven heating of electronic packages, represents service conditions more realistically. The typical temperature- and power-cycling tests are carried out in the range from −40 °C to 125 °C and 0 °C to 100 °C making both creep and fatigue a potential microscopic failure mechanism due to the high homologous temperature T_h, to which solder is exposed.

The present paper continues the previous work [3], where an elasto-plastic behaviour of the solder joint at thermal cycling was studied for assumed both uniform and non-uniform temperature

* Corresponding author.
E-mail address: v.silberschmidt@lboro.ac.uk (P. Hegde).

0927-0256/$ - see front matter © 2008 Elsevier B.V. All rights reserved.
doi:10.1016/j.commatsci.2008.05.005

Please cite this article in press as: P. Hegde et al., Comput. Mater. Sci. (2008), doi:10.1016/j.commatsci.2008.05.005

listributions in the 1206 chip resistor assembly. This paper focuses n a creep behaviour of solders under powercycling. Initially, the xperimental work carried out to establish the temperature distriutions for powering of the surface mount chip resistor, which is ctual representation of field use conditions, is described. These emperature distributions are used in the finite element creep nalysis to study the creep damage accumulation in the solder oint of 1206 chip resistor for five power cycles. Creep analysis is arried out for both uniform and non-uniform temperature distriutions (two cases of thermal loading) in the chip resistor that are xplained below. Finally, fatigue lives are calculated for both cases f thermal loading based on the Coffin–Manson approach and comarison is made between them.

2. Experimental

To assess the non-uniformity of temperature distributions in the 1206 chip resistor due to powercycling, a series of experiments are arried out to acquire the temperature field using an infrared (IR) Thermosensorik camera. The temperature measuring technique is imilar to the one described in [3]. Thermal radiation from the surace, which has a wavelength spectrum dependent on its temperaure, structure and composition of the surface, is measured in the xperiment. The higher the temperature, the more radiation is mitted; the temperature is measured by analysing thermal radiaion. Infrared-measuring technique is contactless and non-destrucive and supplies information with spatial and temporal resolutions hat are usually not achievable with other measuring techniques.

2.1. Specimen description

The construction of the studied 1206 chip resistor is shown in Fig. 1. It consists of a thick-film resistive element mounted on an alumina substrate. The resistive element is covered with protective coating. The ends of the alumina substrate are covered with electrodes, which are used to power the chip resistor. This 1206 chip resistor can operate in the temperature range between −55 °C and +125 °C. It has resistance 1.8 kΩ and the maximum power dissipation 0.25 W. As the ambient temperature increases, the power dissipation should be decreased to match the maximum power dissipation of the chip resistor. The required power supply to achieve the maximum power dissipation at room temperature is 21.3 V, which corresponds to the current with 0.01183 A.

The above described chip resistor is mounted on a FR4 substrate (width 3.2 mm) with 35 μm thick copper track (Fig. 2). The chip resistor is connected to the copper track with a lead-free eutectic Sn3.8Ag0.7Cu solder alloy. Electric connections are made to copper track for powering the chip resistor.

2.2. Experimental set up

The experimental setup, used for acquiring the temperature data for the chip resistor assembly, is presented in Fig. 3. The chip resistor is painted with a matt black paint and mounted on a wooden block, which is placed over a variable lab jack. The camera, fitted with an infrared micro lens, is mounted on the tripod (not shown in Fig. 3). The specimen is powered on for a few minutes to stabilise the temperature distribution in the specimen, then the micro lens is focused on the specimen and the temperature profile is captured. The experiment is carried out to capture the temperature profile in the chip resistor assembly for two different power conditions – 0.25 W and 0.15 W. The results are presented only for maximum power condition due its relevance for the numerical simulations presented in this paper.

2.3. Experimental results

A typical measured temperature distribution over the chip resistor is demonstrated in Fig. 4; it is evident that the maximum temperature 61.5 °C is at the centre of the chip where heat is generated due to resistance of the thick-film resistive element. This heat is conducted to other parts of the assembly. It is also observed that the temperature distribution decreases at the corners of the chip resistor, which is an indication of the temperature non-uniform distribution in the assembly. This is justified by Fig. 4b and c, demonstrating temperature distributions along two orthogonal lines. One of these distributions is more symmetric (Fig. 4b) than another; this is due to eccentricity of the resistive element's position along line 2.

The validation of the temperature distributions captured with the thermal camera is made by comparing it with the temperature obtained by means of thermo-couple measurements. A very fine thermo-couple with diameter of 40 μm is used for the latter to avoid heat dissipation through it. The thermo-couple was calibrated by measuring temperature of boiling water. The comparison of temperatures at different locations of chip resistor assembly is presented in Table 1; the locations considered for are given in

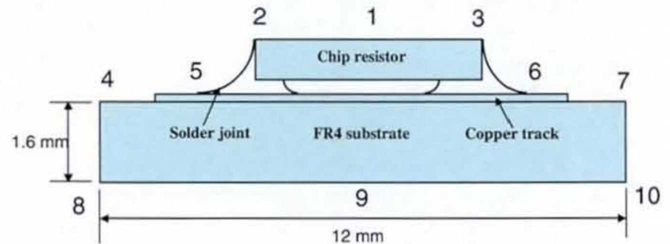


Fig. 2. Mounting of chip resistor on FR4 substrate.

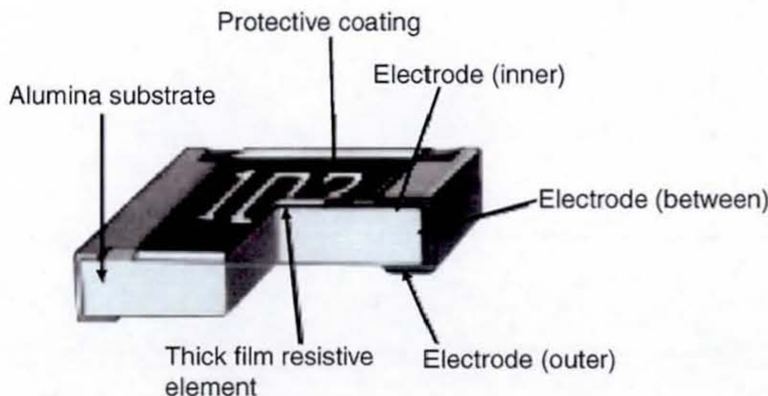


Fig. 1. Construction of a 1206 chip resistor.

Please cite this article in press as: P. Hegde et al., Comput. Mater. Sci. (2008), doi:10.1016/j.commatsci.2008.05.005

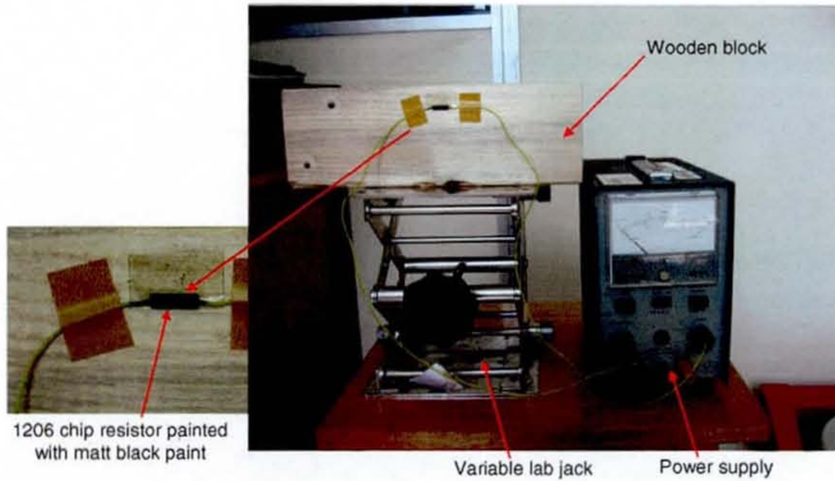


Fig. 3. Experimental setup (without infrared camera).

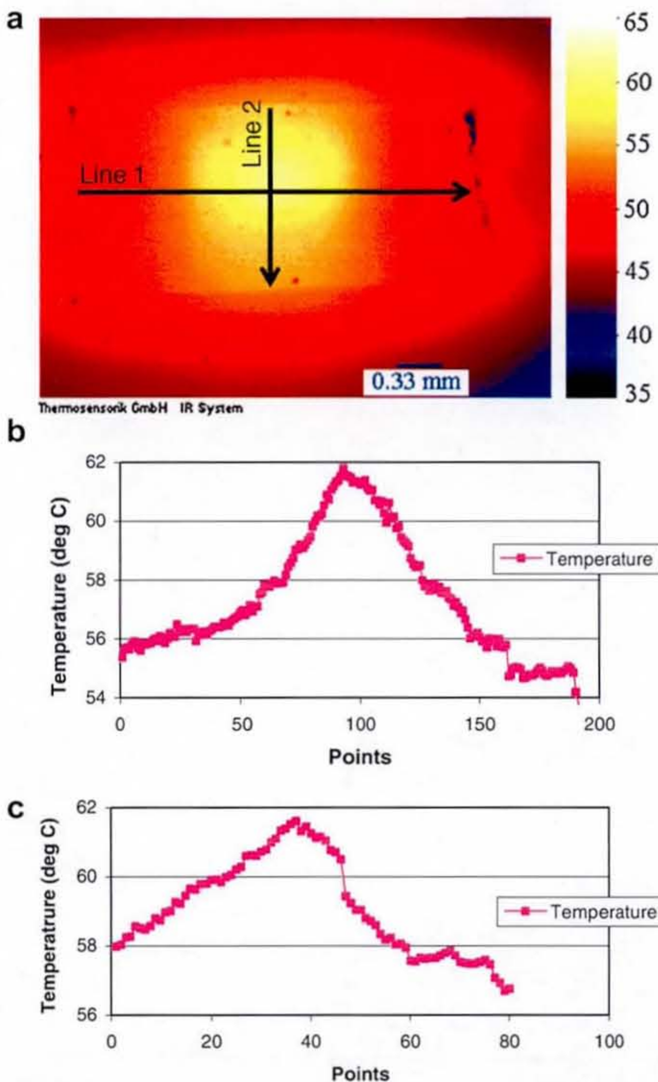


Fig. 4. Temperature distributions in chip resistor: (a) Over chip surface. (b) Along line 1. (c) Along line 2.

Fig. 2. A maximum temperature discrepancy 1.5 °C between two measuring techniques is observed at the centre of the chip, while at other locations it is about 1 °C. The temperature measurement

Table 1
Temperature magnitudes measured with thermocouple and thermal camera

Location (see Fig. 2)	Room temperature = 22° C		Room temperature = 24.5° C	
	Morning		Afternoon	
	Thermocouple	Thermal camera	Thermocouple	Thermal camera
1	60.5	61.5	62.5	65.5
2	56	55	57	55
3	54	54	56.5	53
4	39	38	44.5	43.5
5	53		55	
6	52		54	
7	39	38	44	43
8	38		41	
9	45		46	
10	38		41	

in the afternoon estimates a slightly higher temperature level (65.5 °C) due to the increase in the ambient temperature; the discrepancy is also higher here. However, the temperature gradient in the chip resistor assembly remains nearly the same (23.5 °C). The obtained temperature distribution is used as input information for finite element creep analysis.

3. Finite element analysis

The complexity of the studied structure makes the use of analytical techniques cumbersome and presupposes employment of numerical simulation tools. The finite element analysis is an obvious choice to solve a thermomechanical problem for a complex behaviour of the multi-material assembly exposed to non-trivial thermal boundary conditions. The use of numerical simulations can reduce the time and cost associated with the reliability study of solder joints, which otherwise include a time consuming and expensive experimental technique – ATC – used to assess the reliability of electronic product.

3.1. Geometry and material

Both 2D and 3D finite element models of the analysed assembly (see Fig. 2) are built to study the evolution of stresses and creep damage accumulation during powercycling. The geometry used for finite element analysis is the one used in the experiment. The geometric dimensions for both 2D and 3D are similar to those used in [3].

Please cite this article in press as: P. Hegde et al., Comput. Mater. Sci. (2008), doi:10.1016/j.commatsci.2008.05.005

able 2
laterial properties of Sn3.8Ag0.7Cu [4]

emperature (K)	Young's modulus (MPa)	Poisson's ratio	CTE (ppm)	Density (gm/cm^3)	Yield stress (MPa)	Tangent modulus (MPa)
98	32331	0.4	21.2	7.5	38	154
48	8285	0.4	21.7	7.5	30	134
23	6517	0.4	23.0	7.5	17	132

Since material properties vary with temperature, temperature-lependent material parameters are introduced into the FEA. The naterial properties used to model a ceramic component, copper pad and FR4 are the same as in [3]. The undertaken studies showed hat powercycling induces stress levels in solder joints beyond vield and temperature ranges between $0.55T_h$ and $0.68T_h$. When he operating temperature is more than $0.4T_h$, most of the materi-ils undergo creep deformation. Therefore, the creep material mod-el is introduced for the solder joint to capture the effect of creep damage during powercycling. Material properties for the SnAgCu solder joint are shown in Table 2 [4], and a bilinear kinematic hard-ening material model is used for elasto-plastic modelling of the solder joint, which includes the Bauschinger effect due to cyclic oading. To reduce the complexity and analysis time, only the SnAgCu solder joint is modelled with the elasto-plastic material behaviour. Its creep behaviour is described by the hyperbolic sine aw used for the steady-state creep:

$$\dot{\varepsilon}_{cr} = A\sinh(\alpha\sigma)^n \exp\left[\frac{-H}{RT}\right], \quad (1)$$

where $A = 277984$, $\alpha = 0.02447$, $n = 6.41$, $H/R = 6500$. $\dot{\varepsilon}_{cr}$ is a steady state-creep strain rate, σ is a stress level, T is absolute temperature [5].

3.2. Element selection and meshing

2D finite element modelling is implemented with plane strain elements to better represent the field problem and compared with the 3D formulation. Only one-half of the geometry is modelled to make use of the symmetry of the structure. The commercial FEA software package ANSYS is used for both finite element modelling and analysis. A 2D model is built with 4-noded PLANE182 elements with the plane strain option. The 2D finite element model contains 8058 elements with finer mesh at the solder joint area that is the region of interest. The 3D finite element model is built with 8-noded SOLID 45 element, and there are 33,017 elements in this model.

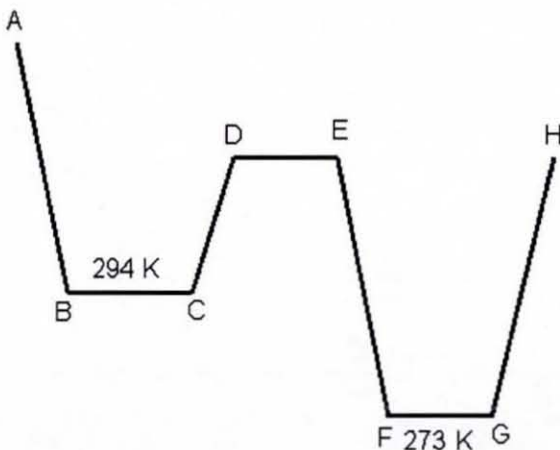


Fig. 5. Thermal profile used in powercycling: Reflow (AB) – 48 s; Dwell at room temperature (BC) – 3600 s; Ramp (EF, GH) – 360 s; Cold dwell (FG) – 300 s; Peak temperatures of power cycle (D and E) – 333.5 °C; Temperature range of power cycle 60.5 °C.

3.3. Loads and boundary conditions

In the present creep analysis, only a thermal load is considered, which is a major cause for creep fatigue failures in solder joints. The thermal load for the 1206 chip resistor assembly is applied through powercycling. Research has been carried out to decide upon the dwell time used in the powercycling. Since most of the creep damage accumulation takes place during the hot dwell [2]. The longer hot dwell results in higher accumulation of inelastic strain and a shorter fatigue life. In contrast, shorter dwells do not allow a sufficient time for creep damage and result in a higher fatigue life. Further, according to previous research, the fatigue life is most sensitive to the hot dwell time that ranges between 5 and 10 min. Effect of hot dwell time on creep damage accumulation is insignificant when it is beyond 10 min [2]. Therefore, it is critical to select the proper dwell time in the powercycling to accurately represent the test condition. In the present powercycling used for creep analysis, 5 min hot and cold dwell time is used with total cycle time of 22 min.. Details of temperature changes during the power cycle used in our simulations are given in Fig. 5.

Most commonly, creep analysis for powercycling is carried out considering a uniform temperature distribution in the chip resistor. This does not accurately represent the temperature distribution in the assembly when it is powered. Therefore, in the present creep analysis two different thermal profiles are used for powercycling: a non-uniform temperature distribution in the chip resistor assembly at hot dwell (Thermal load case 1) and a uniform temperature at hot dwell with the temperature corresponding to the maximum one at the measured distribution when the chip resistor is powered on to its full power (Thermal load case 2). This enables us to compare the creep damage accumulated in the solder joint due to two assumed boundary conditions. The temperature in both thermal profile changes between 273 K and 333.5 K (which is the maximum temperature in the chip resistor assembly when chip resistor is powered to its maximum load). Fig. 5 shows the power cycle used in creep analysis. Before the chip resistor assembly is subjected to powercycling, reflow (line AB) and a one-hour dwell period at room temperature (line BC) is simulated for creep. CD represents the ramp from room temperature to the hot dwell with a 5 min dwell (line DE). Then the temperature is ramped down (line EF) to the cold dwell (0 °C) with 6 min ramp. After 5 min of the cold dwell (line FG), temperature is again ramped up (line GH) for the hot dwell to start powercycling again.

The structural boundary condition employed for creep analysis is similar to the one in [3] – a symmetry boundary condition is used for the finite element model to represent the symmetry and restrain the rigid body motion. In addition, a bottom node in the symmetry plane is also restrained in the vertical direction.

4. Results and discussion

4.1. Thermal analysis

A thermal analysis is carried out to obtain the temperature distribution for the 1206 chip resistor assembly when the resistor is powered on to its maximum power condition (0.25 W) at room temperature. The temperature distribution obtained from our

Please cite this article in press as: P. Hegde et al., Comput. Mater. Sci. (2008), doi:10.1016/j.commatsci.2008.05.005

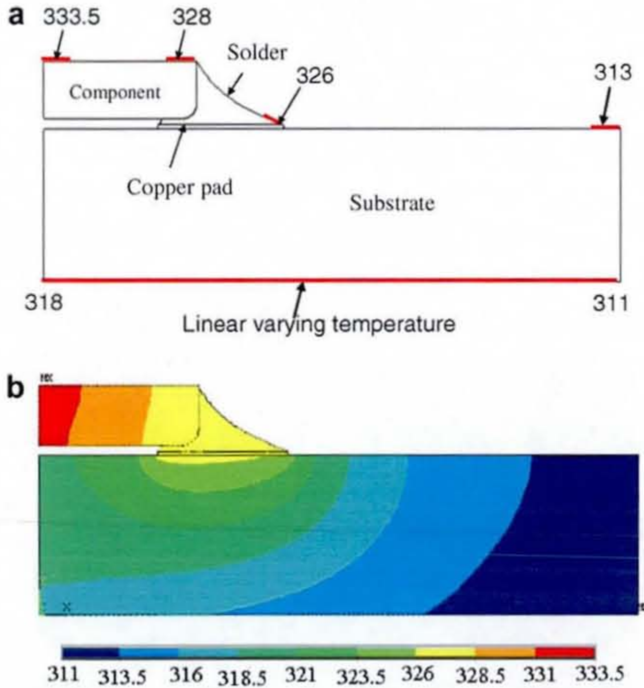


Fig. 6. Thermal analysis for chip resistor assembly: (a) Temperature boundary conditions. (b) Calculated temperature distribution (in K).

experimental work is used as the boundary condition for the finite element thermal analysis. Fig. 6a demonstrates the temperature boundary condition used for thermal analysis, while Fig. 6b shows the temperature distribution in the chip assembly for maximum power condition. This is the temperature distribution used at the hot dwell of the power cycle in thermal load case 1.

4.2. Structural analysis

4.2.1. Comparison of 2D and 3D finite element simulation

A comparative study is implemented to decide on the type of finite element modelling–2D or 3D–for creep analysis. This study is carried out for the thermal profile with a uniform temperature distribution in the chip assembly. A creep analysis is conducted for both 2D and 3D models with similar loads and boundary conditions for three power cycles. The obtained distribution of shear stresses in the solder joint at the end of the dwell (point C in the thermal profile, Fig. 5) at room temperature is shown in Fig. 7. From comparison of 3D and 2D stress distributions, it is obvious that the stress magnitudes (between −6 MPa and 12 MPa) and positions of their extreme levels match very closely in both models.

Evolution of shear creep strain and stress is also studied for both 3D and 2D models over the dwell period at room temperature and three subsequent power cycles. The shear stresses calculated at a maximum stress location in the solder joint's fillet are compared in Fig. 8a. It is obvious that both schemes provide very close results over the cycle time, except for a slight discrepancy during the beginning of the dwell period. The evolution of shear creep strain over the dwell and subsequent power cycles is depicted in Fig. 8b for both types of dimensions. It is obvious from the graph that levels of shear creep are particularly the same in the initial period (till 285 s); thereafter a difference between the graphs appears. However, this difference between 3D and 2D models narrows as the powercycling progresses, changing from 6% in the first power cycle to 3% in the third power cycle. This indicates that 2D finite element simulations pretty well match 3D simulations, and further creep analysis can be carried out using the 2D model to reduce the computational time.

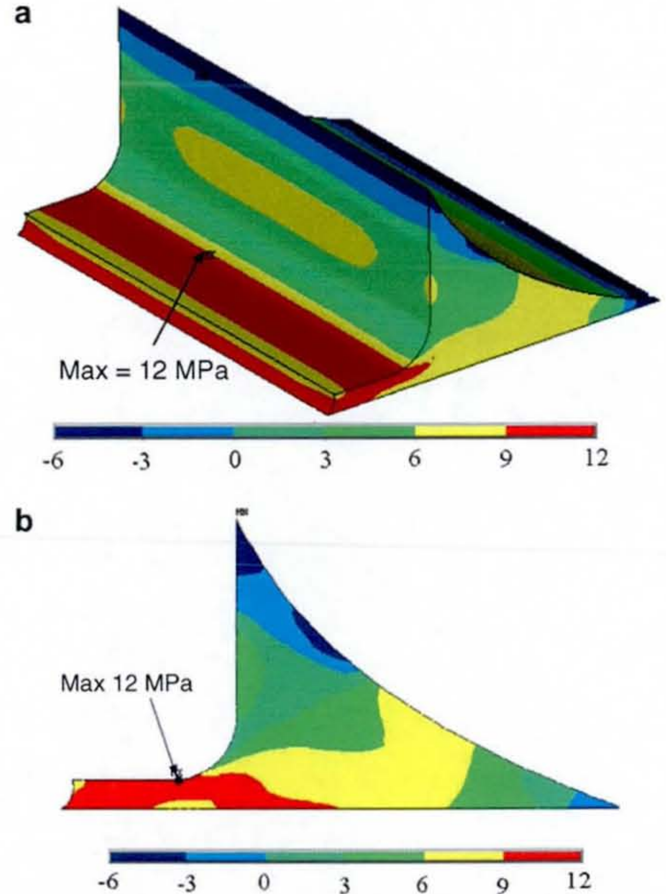


Fig. 7. Distribution of shear stresses in 3D (a) and 2D (b) after dwell at room temperature.

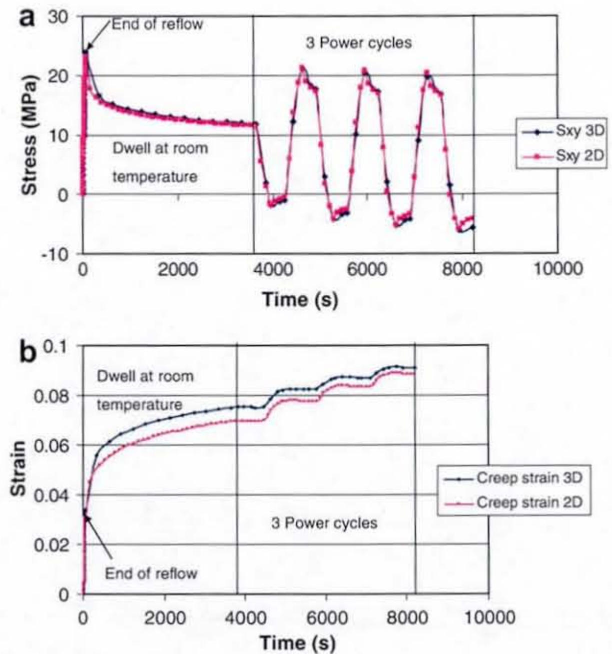


Fig. 8. Evolution of shear stresses (a) and shear strains (b) in 2D and 3D creep analysis.

Please cite this article in press as: P. Hegde et al., Comput. Mater. Sci. (2008), doi:10.1016/j.commatsci.2008.05.005

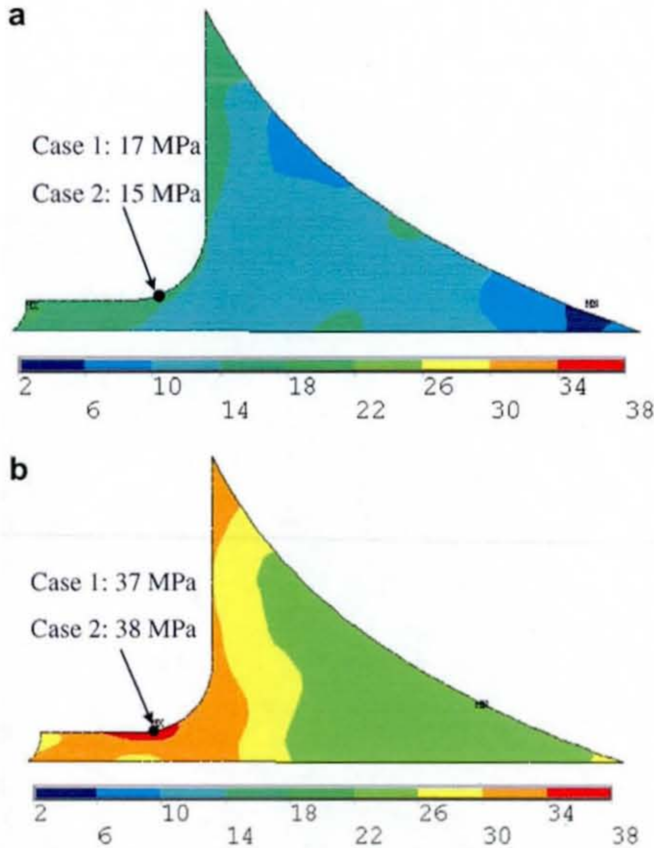


Fig. 9. Equivalent stresses in solder joint: at point D (a) and F (b) of the thermal profile (Fig. 5).

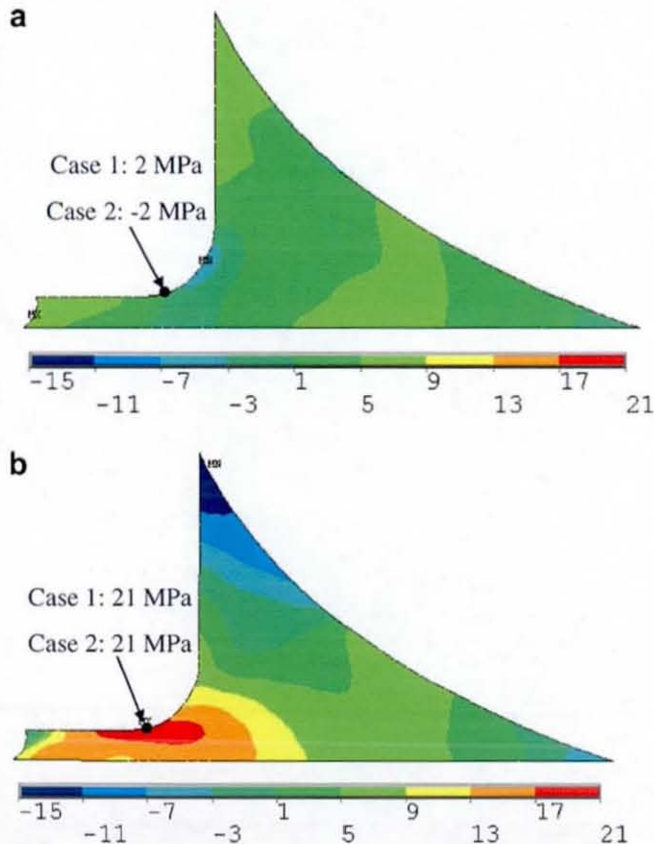


Fig. 10. Shear stresses in solder joint: at point D (a) and F (b) of the thermal profile (Fig. 5).

4.2.2. Creep analysis

A detailed creep analysis of the 1206 chip resistor assembly is carried out for five power cycles with two different thermal conditions corresponding to thermal load cases 1 and 2. The calculated distribution of the equivalent stress in the fillet of the solder joint at the start of the power cycle (location D in the thermal profile) is shown in Fig. 9a. There is no significant difference in the stress distributions between non-uniform and uniform thermal load cases with the respective maximum stresses 15 MPa and 17 MPa. A similar observation can be made for the stress distribution at the start of the cold dwell (point F in the thermal profile, Fig. 5). However, it is evident from Fig. 9b that the level of stresses in the solder joint is higher for the cold dwell compared to that for the hot dwell due to higher thermal strain. Fig. 10 presents the shear stress distributions for the same moment of the thermal history. The analysis of stress distributions in the solder joint demonstrates that the solder fillet is the area of stress concentration that is the potential location for crack initiation.

A study of evolution for both equivalent and shear stresses for the location of the maximum stress in the solder joint's fillet over five power cycles is carried out for two thermal loading cases. In addition, the stress range in each power cycle is calculated and compared for these two cases. Figs. 11 and 12 illustrate the variation of equivalent and shear stresses, respectively, in the solder joint's fillet over the dwell at room temperature and five power cycles. Both the maximum equivalent stress (42 MPa) and the maximum shear stress (24 MPa) are observed at the end of reflow. The magnitudes of both stresses decrease with relaxation representing the dwell at room temperature. The stress variation shows that stress cycles practically do not change the shape; there is a decrease in the magnitude for the lowest point; the decline of the

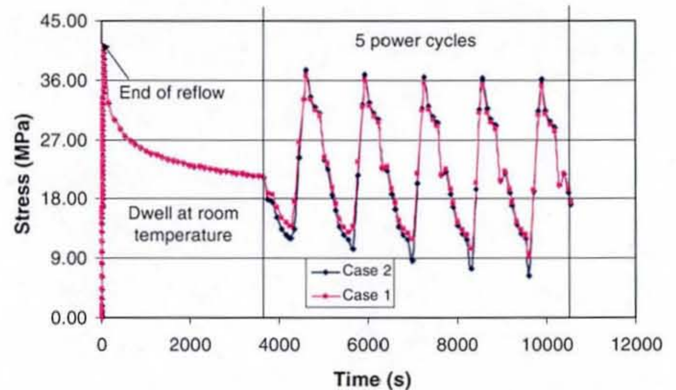


Fig. 11. Evolution of equivalent stress in solder joint's fillet (Fig 10).

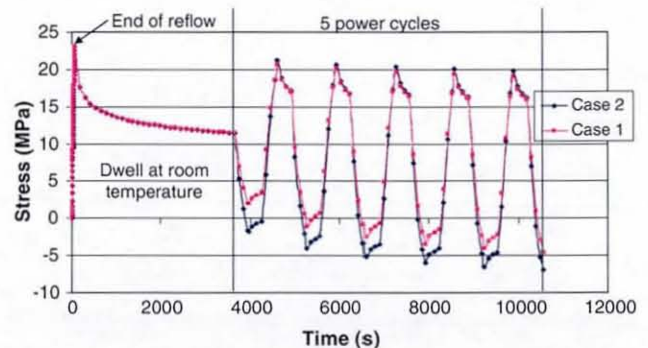


Fig. 12. Evolution of shear stress in solder joint's fillet (Fig 10).

Please cite this article in press as: P. Hegde et al., Comput. Mater. Sci. (2008), doi:10.1016/j.commatsci.2008.05.005

Table 3
Range of equivalent stress in power cycles

Cycle	Range of equivalent stress (MPa)		Difference (%)
	Thermal load case 1	Thermal load case 2	
1	22.8	25.5	11.8
2	23.0	26.5	15.2
3	23.8	27.9	17.2
4	24.8	28.9	16.5
5	25.6	29.6	15.6

Table 4
Range of shear stress in power cycles

Cycle	Range of shear stress (MPa)		Difference (%)
	Thermal load case 1	Thermal load case 2	
1	21.8	25.3	16.1
2	22.6	25.9	14.6
3	23.1	26.2	13.4
4	23.4	26.5	17.2
5	23.7	26.8	13.1

maximum value with power cycle is significantly less pronounced. Differences between the stress ranges for cases 1 and 2 of thermal loading were studied, and results are presented in Tables 3 and 4. From this study, it is clear that stress range is nearly constant (24 MPa for the non-uniform temperature distribution case and 27.5 MPa for the uniform one) and the uniform temperature distribution case always results in the higher level of the stress range for both equivalent and shear stresses.

A study on creep strain accumulation is also conducted to find out the extent of creep damage caused by powercycling in the solder joint. It was shown in our previous work [3] that the critical temperatures corresponding to the onset of plastic flow are well within the range of thermal cycling of solder joints (presupposing the account for plastic strain component). In the conducted creep analysis accounting for the elasto-plastic material behaviour of SAC solder, the inelastic strain in the solder joint is calculated. This is due to both plastic and creep deformation. Evolution of this strain in the fillet of the solder joint is demonstrated in Fig. 13 for powercycling. It is obvious that accumulation of inelastic strain increases with time due creep. The inelastic strain contribution due to plasticity ceases at the end of reflow (point B in the thermal profile, Fig. 5) since the magnitudes of stresses induced in the solder joint in subsequent power cycles do not exceed the level attained at the end of reflow. The comparison of inelastic strains for cases 1 and 2 indicates that strain accumulation is always higher in case of the uniform temperature distribution. The inelastic strain range for each power cycle is given in Table 5. Interestingly, this strain

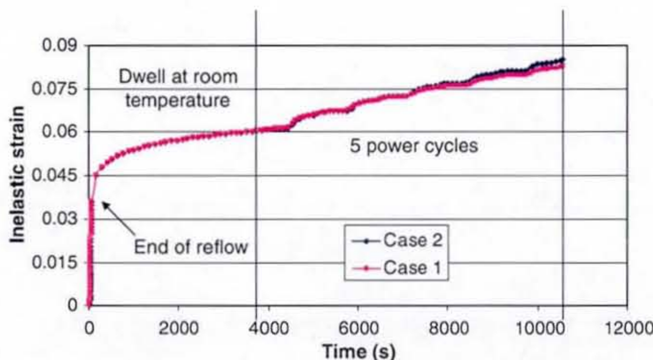


Fig. 13. Evolution of inelastic strain in solder joint's fillet (Fig 10).

Table 5
Range of inelastic strain in power cycles

Cycle	Range of inelastic strain		Difference (%)
	Thermal load case 1	Thermal load case 2	
1	0.00622	0.00625	0.42
2	0.00467	0.00512	9.52
3	0.00402	0.00462	14.97
4	0.00363	0.00433	19.17
5	0.00337	0.00414	22.80

range is almost the same in the first power cycle for both cases. This range decreases as powercycling progresses, an indication for the stabilisation of the stress–strain hysteresis loop after few power cycles. The difference in inelastic strain ranges between cases 1 and 2 increases from 0.42% in the first power cycle to 22.8% in the fifth power cycle. This difference has a direct effect on the corresponding fatigue lives.

4.2.3. Fatigue life estimation

There are various methods to calculate the fatigue life of solder joints. One among the most commonly used is the strain-range based Coffin–Manson method. The following Coffin–Manson equation [5] is used to calculate the fatigue life based on the inelastic strain range obtained from the creep analysis:

$$N_f = (C'\varepsilon_{acc})^{-1}, \tag{2}$$

where N_f is the number of cycles to failure (fatigue life), $C' = 0.0468$ [5], ε_{acc} is the accumulated inelastic strain range per cycle. Fatigue life for both cases is calculated based on the strain range in the fifth power cycle (see Table 5). The calculated fatigue life of case 1—6341 cycles—is 23% higher than that for case 2 (5161 cycles). This indicates that consideration of the non-uniform temperature distribution has a significant effect on the estimate of the fatigue life of solder joints.

5. Conclusions

The finite-element creep study of a surface mount resistor under non-uniform temperature loads allows us to draw the following conclusions:

1. The experimental study of the chip resistor shows that the temperature distribution in the assembly is not uniform under the condition of powering.
2. An assumption of the uniform temperature distribution in the chip resistor assembly overestimates the inelastic strain accumulation. This overestimation results in the lower predicted fatigue life compared to the case of the non-uniform temperature distribution.
3. Accumulation of plastic strain in the solder joint ceases after the reflow making creep the main source of the inelastic deformation in the joint.
4. The range of inelastic strain stabilises with the increase in the number of power cycles.

The next stage of finite element analysis of reliability of lead-free surface mount assemblies will be linked with direct introduction of interfacial crack initiation and growth, which will be implemented using cohesive zone elements at the interfaces.

References

[1] C.M.L. Wu, D.Q. Yu, C.M.T. Law, L. Wang, Materials Science and Engineering Reports 44 (2004) 1–44.

Please cite this article in press as: P. Hegde et al., Comput. Mater. Sci. (2008), doi:10.1016/j.commatsci.2008.05.005

[2] K. Setty, G. Subbarayan, L. Nguyen, Electronics Components and Technology Conference (2005) 907–915.

[3] P. Hegde, A.R. Ochana, D.C. Whalley, V.V. Silberschmidt, Finite element analysis of lead-free surface mount devices, Computational Material Science 43 (2008) 212–220.

[4] W. Qiang, L. Lihua, C. Xuefan, W. Xiaohong, Experimental determination and modification of Anand model constants for Pb-free material 95.5Sn4.0Ag0.5Cu, in: Proceedings of the 8th International Conference on Thermal, Mechanical and Multiphysics Simulation and Experiments in Micro-Electronics and Micro-Systems, EuroSimE 2007, pp. 308–316.

[5] A. Syed, Accumulated creep strain and energy density based thermal fatigue life prediction models for SnAgCu solder joints, in: Proceedings of the 54th Electronic Components and Technology Conference, Las Vegas, USA, June, 2004, pp. 737–746.

Please cite this article in press as: P. Hegde et al., Comput. Mater. Sci. (2008), doi:10.1016/j.commatsci.2008.05.005