Characterization of CdTe Photovoltaic Films and Devices with Over 18% Efficiency Fabricated Using Scalable Sublimation Processes

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Abstract

Sublimated thin film CdTe photovoltaic devices with conversion efficiencies over 18% and a fill-factor greater than 79% have been repeatedly obtained using high-rate fabrication processes on commercial soda-lime glass substrates used in CdTe modules. Four major improvements to the device have enabled an increase in efficiency from a baseline of approximately 12% to 18.7%: 1) A sputtered multilayer metal-oxide anti-reflection layer; 2) total replacement of the CdS window layer with a higher bandgap sputtered $Mg_xZn_{1-x}O$ (MZO) window layer; 3) deposition of the CdTe layer at a higher thickness and substrate temperature; and 4) an evaporated tellurium back-contact. This work describes the effect of these changes on the device performance and film microstructural characteristics using various methods. Multiple devices with comparable high efficiency have been fabricated and demonstrated using methods described in this study, yielding some of the highest efficiencies for CdTe polycrystalline thin-film photovoltaics.

Thin film CdTe photovoltaics have consistently demonstrated the lowest cost solar electricity generation, particularly for utility scale applications. CdTe is a *p*-type absorber that has a bandgap of 1.5 eV which is nearly optimal for photovoltaic conversion. Approximately 2 μm is sufficient to absorb most of the visible solar spectrum.[1,2] CdTe films are typically deposited on glass substrates using low-cost hardware and high-rate deposition processes[3,4,5] reducing production costs. Typical crystalline silicon photovoltaics require wafers that are 150-200 microns thick and use a more complex and capital-intensive fabrication process.[3]

The low-cost manufacturing of thin-film CdTe PV has enabled agreement for a record low cost power purchase agreement of ¢3.8/kWh for a 100 MW field,[6] which is significantly lower than the average cost of electricity in the U.S. of ¢11/kWh.[7] With recent improvements, research-scale small devices have record efficiencies of 22.1%,[8] while modules with up to 18.6%[9] efficiency have been produced. The leading CdTe PV manufacturer, First Solar Inc., has increased average production module efficiency from 13.5% in the first quarter of 2014[10] to 16.7% in the first quarter of 2017.[11] Further improving the efficiency without substantial increase in production cost will reduce the levelized cost of energy for CdTe photovoltaics.[12,13]

Maintaining the dual requirement of high efficiency and low cost requires the use of film deposition techniques suitable for mass production of millions of solar modules per year. The vapor deposition methods used for this study, including sublimation, evaporation, and sputter deposition, have been used in large scale manufacturing for solar and other industries. Commercially available 3.2-mm soda-lime glass with a fluorine-doped tin-oxide (FTO) transparent conducting layer is a standard substrate for thin-film PV manufacturing, including for CdTe, due to its sufficient strength, reliability, and low cost. Using processes suitable for large scale manufacturing, the authors have explored new materials and process modifications to systematically reduce conversion losses in devices fabricated on low cost glass substrates. This has resulted in an 18.3% efficient device which has been externally certified by ILX Lightwave (Newport).[14] These independent measurements correspond closely to internal measurements performed at Colorado State University. The performance results have been repeatedly replicated. To the

authors' knowledge, this is the highest efficiency device for which the complete structure has been reported in detail. A detailed materials characterization protocol was used to guide the process optimization. Methods include transmission electron microscopy (TEM) and energy dispersive X-ray spectroscopy (TEM-EDS) for elemental distribution, and grazing incidence X-ray diffraction (GIXRD) for grain orientation and film texture. Electrical characterization includes current density-voltage (J-V) measurements to derive device efficiency parameters and spectral response measurements.

Device Structure for Improved Efficiency

Thin film CdTe device structure and processing improvements were characterized to understand their impact on performance and microstructure. At the start of the study, baseline device efficiency was typically 12%, with the device's structure shown in Figure 1a. At the conclusion of this study, the devicestructure had been significantly modified, as shown in Figure 1b. This improved structure, combined with elevated CdTe absorber deposition temperatures, resulted in the increased device performance of over 18%.

Baseline Device and Film Growth

The devices were fabricated using a vacuum deposition system at Colorado State University (CSU) capable of performing processes in-line to fabricate a nearly complete CdTe solar cell.[15] The baseline device (Figure 1a) fabrication process begins with the preheating of the substrate, followed by 130 nm of *n*-type CdS and 2.4 µm of CdTe deposition at a substrate temperature of 440ºC and 445ºC, respectively.[15] The substrate is TEC 12D soda-lime glass produced by NSG. The glass is coated with fluorine doped tin oxide (FTO) followed by an un-doped, high resistivity transparent (HRT) tin oxide layer. After CdTe deposition, sublimation of a $CdCl_2$ layer and an annealing treatment at approximately 400ºC comprise the passivation process for the CdTe absorber. The substrate is then removed from the in-line vacuum chamber, rinsed with deionized water, and heated again under vacuum to approximately 200ºC. A small amount of CuCl is sublimed onto the CdTe and annealed at 200ºC to form the device back contact. The back electrode of this device consists of carbon- and nickel-containing acrylic paints.

Improving Device Response at Low Wavelengths

Cadmium sulfide has been traditionally used with CdTe as an *n*-type window layer. CdS is a strong absorber of light above its bandgap of 2.4 eV, and thus the light absorbed within this layer cannot reach the CdTe absorber layer.[16] Photogenerated carriers from CdS are not collected and the light absorbed in this layer is wasted, limiting J_{SC} in the baseline devices. Use of HRT layers has been studied to enable the use of thinner CdS layers to decrease above bandgap absorption, but some CdS is still needed to maintain voltage.[16]

The CdS *n*-type window layer is a strong absorber of blue light, which causes lack of absorption in the CdTe absorber. Using a more transparent window layer would lead to greater absorption of light in the CdTe absorber layer, leading to higher current generation. Magnesium zinc oxide (MZO) has a high bandgap of 3.7 eV, which greatly reduces parasitic window layer absorption. ZnO alloyed with MgO to form a HRT layer has been studied by Kephart, *et al.*[17] In addition to increased ultraviolet transmission, MZO provides a band-alignment more suitable for CdTe.[16,17] The $Mg_xZn_{1-x}O$ with a composition of x=0.23 may be used without an *n*-type CdS window layer to achieve higher J_{SC}, as well as V_{OC}. These films are deposited by RF sputtering and are typically 100 nm thick. An initial study of devices using MZO window layers demonstrated devices with 15.5% efficiency with improved J_{SC} and V_{OC} relative to CdS devices.[18]

Optimization of CdTe Growth on MZO

Increasing substrate temperatures during growth generally improves grain structure and film quality. Increasing substrate temperature during deposition of CdTe on CdS window layers produced an improvement in fill-factors.[19] However, the re-sublimation of the CdS window layer restricts further increase in the CdTe deposition temperatures. In addition to the increased transparency and favorable band alignment, MZO is thermally stable at high substrate temperatures and does not re-sublime. This

enables deposition of CdTe films at substrate temperatures over 610ºC–significantly higher than can be achieved with CdS. Higher temperature deposition leads to larger CdTe grains, a higher fill-factor, and thus higher efficiency. This is attributed to fewer grain boundaries, which reduces recombination in the absorber. Additionally, the optimal thickness of the large-grain CdTe absorber layer is greater than for the baseline devices.

Increasing the CdTe absorber thickness beyond the baseline device of 2.4 µm impacts the device performance. The effect of increasing CdTe absorber thickness on MZO/CdTe devices is shown in Figure 2a and 2b. Increasing the absorber thickness improved the fill-factor and J_{SC} of the devices while maintaining the V_{OC}. The carrier lifetime measured by time resolved photoluminescence (TRPL) increases with increased CdTe thickness, as shown in Figure 2a. This suggests that interfaces at the back of the device act as recombination regions. As the thickness is increased, the back interface is moved away from the junction, improving its lifetime. Though the lifetime continues to increase for CdTe layers thicker than 3 µm, the thicker layers were more difficult to passivate with the $CdCl_2$ process. A local optimum of around 3 µm was experimentally identified.

Microstructural Characterization

Cross-sectional high resolution transmission electron microscopy (HRTEM) is performed on devices to better understand the interaction between the MZO and CdTe. Microscopic elemental distribution within the film stack is mapped using EDS. A representative TEM micrograph is shown in Figure 5. When deposited at relative high temperatures and subjected to the $CdCl_2$ treatments, there is S diffusion into the CdTe.[20] Some inter diffusion is beneficial to reduce defects at the CdS/CdTe interface. Figure 3 shows the TEM analysis on completed devices (but without the painted electrode layers). The interface between CdTe and 100 nm MZO is continuous and uniform with a homogenous and conformal coverage over the TCO (Figure 3b and 3c). CdS has a mismatch of 10% with CdTe and is known to intermix with the CdTe during high temperature deposition and $CdCl_2$ activation.[21] MZO has a greater mismatch with CdTe.[18] EDS maps of these high efficiency devices show no signs of MZO diffusing into the CdTe layer within the detection limits of the technique (Figure 3e). In addition, the HRTEM image shows an abrupt

interface between MZO and CdTe that reinforces minimal intermixing and diffusion between these layers (Figure 3a and 3d). Films deposited at a higher substrate temperature (~610ºC) exhibit a large CdTe grain size compared to films deposited at a relatively lower substrate temperature.[22,23] The CdTe layer deposited here had an approximate thickness of ~3 µm, and the CdTe grains grow from the MZO layer to the back surface as a continuous grain with no horizontal intercepting grain boundaries.

Other studies have shown Cl decorating CdTe grain boundaries and the CdS/CdTe interface after $CdCl_2$ passivation treatment using EDS maps.[24] Using an Electron Energy Loss Spectroscopy (EELS) line scan,[25] Li *et al.* reported a Cl rich region of 1-2 nm at the CdTe/CdTe grain boundary. It was also reported that grain boundaries have enhanced carrier collection after $CdCl_2$ passivation treatment, suggesting that $CdCl_2$ plays a more critical role than just promoting recrystallization.[25] Abbas *et al.* also found that excessive accumulation of Cl at interfaces and grain boundaries has a detrimental effect on CdTe device performance.[26] Much lower concentrations of Cl are detected using EDS in CdTe films deposited at high temperature on MZO in comparison with those on CdS. Good device performance with such minimal Cl at the suggests that the amount of Cl required for enhanced carrier collection at grain boundaries is minimal.

GIXRD was used to compare the grain texture of baseline CdTe films with those deposited using the new, high-temperature process conditions before and after $CdCl_2$ passivation. At higher 2θ angles, peaks from K_{a2} are observed as a doublet peak. For lattice parameter calculation, 2θ values from the first three high intensity peaks were taken into consideration and compared to the standard (Supplementary Table 1). In all cases, the change in the lattice parameter with respect to the standard value is insignificant, suggesting no thermal stresses generated after the $CdCl_2$ treatment.

There is an increase in the peak intensities in the samples treated with cadmium chloride (Figure 4) indicating improved crystalline quality. To evaluate the preferred orientation (P_{hkl}) of a particular plane in the films, the intensities from the individual and the standard peaks were substituted in the texture coefficient formula:[27]

$$P_{hkl} = \frac{I_{hkl}}{I_{o,hkl}} / \frac{1}{n}\sum_{i=1}^{n}\frac{I_{hkl}}{I_{o,hkl}}$$

(Where I_{hkl} is the measured intensity, $I_{o,hkl}$ is the intensity corresponding to the particular plane in the JCPDS card, and *n* are the number of the peaks considered.) As-deposited CdTe (baseline or HT) has a larger texture coefficient, which indicates a strong preferred orientation along {111} plane. After the $CdCl_2$ treatment in the baseline films, the texture coefficient along {111} drops significantly closer to unity. There is an increase in the texture coefficient along {511} plane, indicating that the preferred orientation has changed. In the films processed at high temperature, the texture coefficient is still larger than unity after the $CdCl_2$ treatment, which suggests that the preferred orientation has not changed significantly.

The full width half maximum (FWHM) of the diffracted peaks provides information about the crystalline quality of the films. For the analysis, the FWHM was measured at the diffracted peaks of the films treated and not treated with $CdCl_2$. From the graph, it can be observed that after $CdCl_2$ treatment there is a decrease in the peak width, which suggests that the crystalline quality of the CdTe has increased. No strong correlation was observed between the $CdCl_2$ treated samples fabricated at high temperature and baseline process conditions.

Tellurium Back Contact

Several materials, such as Au,[28] ZnTe,[30,31] and Sb_2Te_3,[29,32–34] frequently doped with Cu have been studied as back (hole) contacts to CdTe PV devices. Although reasonable contacts can be made to CdTe using Cu doping, the device performance is quite sensitive to the precise quantity of Cu and subtle process variations.[35] As an alternate to Cu, a Te-rich back contact for CdTe photovoltaics has been studied by Niles *et al.*, Xia *et al.*, and Kraft *et al.*, among others.[36–38] Niles *et al.* describes vacuum evaporated Te as an alternative to chemical etching to avoid the use of acids and the shunting of the device.[36] In addition, Te can be deposited in a highly controlled manner with minimal complexity. Xia *et al.*[37] found that Cu_xTe, formed from a tellurium back-contact in combination with Cu, had a major impact on improving the fill-factor of CdTe thin-film devices. In this study, the presence of a 20 nm Te layer

with Cu at the back surface appeared to form an ohmic contact that caused a substantial reduction in the recombination current, resulting in an improved fill-factor for these devices.[37,38]

To improve the performance of our devices, elemental Te contacts were investigated. Evaporation of a 20 to 100 nm tellurium layer on the Cu-doped back surface of the CdTe, prior to the electrode application, was investigated. 20-25 nm of Te film at the back surface was found to be advantageous, substantially increasing the fill-factor and slightly improving V_{OC}. Further increasing the thickness of Te did not provide any additional benefit. Devices using the Te contact processed without intentional Cu demonstrated over 16% efficiency.[14] The J-V measurements performed at -75 ºC on the Te contacted devices resulted in good fill-factors and no rollover behavior in the fourth power quadrant.

Antireflection Coating Development

Soda-lime glass has a refractive index of 1.51 and an average front-surface reflection of 4.1%. The addition of an effective and robust anti-reflection (AR) coating can reduce this value to below 1.5% and allow more light to reach the CdTe absorber, increasing J_{SC} by approximately 1 mA/cm^2 for typical devices. In order to realize these benefits, a 4-layer Ta_2O_5/SiO_2 based AR coating was developed. The AR stack is based on the Reichert design used by Kaminski *et al.*[39] and has a total thickness of 200 nm.

The calculated ideal AR coating increased reflection for photon energies below the bandgap and for high photon energies where the photon flux is low. In the intermediate range, there is a strong reduction in front-surface reflection. To compare the modeled AR coating with the effect in the actual device, reflection was measured on the highest-efficiency device and a comparable device made without AR coating. The actual difference in reflection agrees well with the modeled difference (Figure 5), with a slight shift to longer wavelengths and interference fringes due to the transparent conductive and window layers. The estimated loss in J_{SC} due to reflection for the AM1.5 global spectrum is 2.7 mA/cm^2 without the coating and 1.6 mA/cm^2 with the coating.

High Efficiency Device Fabrication

High-efficiency devices incorporating all improvements have been fabricated. The device structure is shown in Figure 1b. The substrate is TEC10, a product similar to TEC12D but without a HRT

layer, which is not needed with the MZO window layer, and a slightly lower sheet resistance. This is a commercial 3.2-mm substrate with approximately 400 nm of FTO deposited by the manufacturer. Deposition of the MZO window layer was performed using radio-frequency (RF) sputter deposition and a 100 nm film was deposited on the FTO.[18] Thereafter, a 3.0 µm CdTe film was deposited using sublimation, followed by a $CdCl_2$ passivation treatment. After rinsing the residual $CdCl_2$ film, CuCl was used to deposit a thin-film of Cu on the CdTe surface via a sublimation process,[15,40] and a 20 nm Te film was deposited at room temperature using evaporation to form the back-contact. Following the Te deposition, carbon and nickel paints were deposited. Further details regarding the film deposition method and device fabrication can be found in the methods section.

Figure 6 shows the effect of the different improvements on the J-V and external quantum efficiency (EQE). Comparing the baselines device with the 2.7 µm high temp CdTe (HT CdTe) device shows that replacing the CdS with the MZO significantly improves the device current. The EQE graph shows that the CdS absorption losses below 500 nm are eliminated. The better band alignment of the MZO, combined with improved film quality from the high temperature deposition, results in an increased V_{OC} and fill-factor. The third device with the 3.0 µm absorber shows the effect of the optimized AR stack on device current—the increased thickness further increased the voltage. The increase in J_{SC} can be attributed to increase in absorption at wavelengths greater than 700 nm with increase in absorber thickness, as can be seen in the quantum efficiency plot in Figure 6b. When the EQE data for increasing thicknesses are plotted against each other, there appears to be a shift of the CdTe band-edge, suggesting greater carrier collection with greater absorber thickness. Increasing absorber thickness also leads to an increase in the fill-factor up to 3.5 µm absorber thicknesses. This increase in fill-factor may be the result of moving the back surface of the device away from the depletion region, resulting in a longer carrier lifetime (Figure 2a) and reduced recombination.

The highest efficiency for devices without AR coatings was measured to be 17.9%, as shown in Figure 6. Reduced reflection losses resulted in higher absorption, leading to improved J_{SC}. Such a device

yielded the highest efficiency of 18.7%. A similar device from the same substrate was certified by ILX Lightwave, Newport with a measured efficiency of 18.3% and a V_{OC} of 863 mV, J_{SC} of 26.8 mA, and fill-factor of 79.2% (Figure 7).[14]

Table 1 shows the performance of the best devices within this study. The average measured fill-factor for these devices was 79.5%, while the average J_{SC} was observed to be 26.9 mA/cm^2. Initial MZO/CdTe devices had a V_{OC} of 837 mV, fill-factor of 72.6%, and J_{SC} of 25.2 mA/cm^2.[18] The highest V_{OC} observed within this study was measured to be 863 mV, and the increase from the previous study was attributed to CdTe deposited at a higher substrate temperature (610ºC), resulting in larger CdTe grains and fewer grain boundaries. The J-V plot in Figure 6a shows an excellent fill-factor, and higher absorption can be confirmed from the EQE plot shown in Figure 6b. EQE also shows greater absorption at wavelengths lower than 400 nm, suggesting higher charge collection in the absorber with use of MZO and a multilayer AR coating.

Discussion and Conclusions

We have conducted a comprehensive study of sublimated polycrystalline CdTe thin-film photovoltaics with an efficiency exceeding 18%. This demonstrates that the inherent simplicity and low-cost manufacturing of CdTe devices is compatible with high efficiency. Sublimated CdTe photovoltaic devices with efficiencies up to 18.7% are reported here with the highest measured fill-factor of 80.5%, J_{SC} of 27.1 mA/cm^2, and V_{OC} of 863 mV. These improvements have been achieved through several process modifications.

Eliminating the CdS window and using MZO enables sublimation of CdTe at temperatures over 600ºC. Higher substrate temperatures at the start of CdTe sublimation produces larger CdTe grains. The sublimated films were about 3 μm thick. The CdTe grains appear to grow continuously from the MZO/CdTe interface to the CdTe back surface. It has been consistently observed that larger grain size correspond to higher device efficiency (supplementary Figure 1). In addition, using thicker CdTe films would suggest that back-surface recombination is reduced, since the back surface is situated further from

the CdTe absorber bulk. In the reported study, we show that tellurium deposited using evaporation at room temperature enhances device performance, and that evaporation allows the deposition of Te to be controlled and uniform (supplementary Figure 2). Reduced recombination in the bulk, as well as reduced back-surface recombination, results in a high fill-factor, suggesting higher device quality.

For epitaxial-grown films the interface between absorber and underlying layer must be closely matched to reduce defects and fabricate good devices. However, CdTe is cubic while MZO is hexagonal, and the HRTEM images show an abrupt interface between them. EDS maps show no signs of diffusion of MZO into the CdTe absorber layer. This suggests that improving the quality of this interface can further improve device performance.

Using MZO provides an added advantage of eliminating the CdS window layer. MZO also increases the optical bandgap of the layer that leads to better ultraviolet transmission. This reduces losses from the absorption of photons in the CdS layer, allowing for a greater generation of photo-current and leading to a higher J_{SC}. Adding a Ta_2O_5/SiO_2 multilayer AR coating further reduces reflection losses, improving J_{SC}.

The GIXRD studies confirmed that as-deposited CdTe (baseline or high temperature) has a strong preferred orientation along {111} plane. After the $CdCl_2$ treatment on the high-temperature deposited CdTe, the preferred orientation along {111} plane was maintained. The FWHM comparisons indicate an increase in the crystalline quality of CdTe after the $CdCl_2$ treatment.

Methods

$Mg_{0.23}Zn_{0.77}O$ Buffer Layer Deposition

The thin films are deposited on NSG TEC 10 soda lime glass coated with fluorine-doped tin oxide (FTO), a transparent conducting oxide (TCO). 100 nm $Mg_{0.23}Zn_{0.77}O$ films are deposited using RF planar sputter deposition process. The process gas pressure is set at 5 mTorr with a composition of 1% oxygen in argon. The target has a composition of 11 wt% MgO with 89% ZnO and a diameter of 10 cm. The substrates are not heated during the sputter deposition.[18]

Antireflection Coating Deposition

A 4-layer antireflection coating is deposited on the uncoated soda-lime glass side of the TEC 10 substrate using ion beam sputter deposition in a Veeco SPECTOR system. This film is of the Reichert design[41] and is based on the coating reported by Kaminski *et al.*[39] The design uses smooth metal-oxide layers of a precise thickness to provide destructive interference over a wide range of wavelengths and angles of incidence. In this case, Ta_2O_5 is used for the high-index layer, and SiO_2 is used for the low-index layer. Refractive indices for the two oxide materials are measured using variable angle spectroscopic ellipsometry (VASE); thickness results are verified with profilometry. A program is written in MATLAB which calculates the front-surface reflectance of the structure using the transfer-matrix method. This reflectance is multiplied by the photon flux at each wavelength for the AM1.5G spectrum, and a global optimization is performed to minimize the calculated loss in J_{SC} due to reflection. Reflection measurements are performed using an integrating sphere at 8° from normal.

System for CdTe, $CdCl_2$, and CuCl Deposition

CdTe thin-films deposition, $CdCl_2$ passivation treatment and CuCl contact formation are carried out using an optimized sublimation deposition process using a single vacuum chamber with multiple sublimation sources called the Advanced Research Deposition System (ARDS).[15] This deposition system enables deposition of multiple subsequent films without breaking vacuum and thus avoiding surface contamination between deposited layers. The ARDS is comprised of a main deposition chamber and a

load lock chamber separated by a gate valve.[15] The main deposition chamber consists of nine process stations, such as preheating, CdS, CdTe, $CdCl_2$, $CdCl_2$ activation, CuCl, annealing and controlled cooling. The load lock chamber allows the introduction of the substrate into the primary chamber without the need of venting for each substrate. A CAD (Computer Aided Design) model of a typical sublimation source used in ARDS is shown in supplementary images. The ARDS primary chamber is vented only to replenish the deposition material and for occasional preventative maintenance. The substrate is introduced into the primary sublimation chamber through the load lock using a magnetic transfer arm custom-designed for this application. The temperature of each deposition source, the sequence of deposition, and dwell time in each source (up to as little as one second) can be programed using LabView programs custom-designed for ARDS at Colorado State University. ARDS can be used to fabricate 9-12 substrates per working day that can produce up to 25 photovoltaic devices on each substrate. The primary sublimation chamber pressure is maintained at 40 mTorr using a diffusion pump, and ultrahigh purity N_2 is used as the process gas. The load lock chamber is pumped to process pressure using a mechanical pump.

CdTe Thin-Film Deposition

Devices described in this study are fabricated on $Mg_{0.23}Zn_{0.77}O$ films using a continuous vacuum process in a conventional superstrate configuration.[15,23] The CdTe sublimation source has a bottom heater to heat the material for sublimation. A top heater positioned above the substrate enables the substrate to be maintained at the desired temperature. A graphite vapor source containing CdTe is heated to 555ºC ± 3ºC bottom heater and 360ºC top heater, while the substrate is preheated to ~610ºC in a separate heater before introducing the hot substrate into the sublimation source. These temperatures and time-set points are determined after several empirical experimental iterations to achieve the desired thickness of CdTe films. The thickness of the CdTe films is maintained at ~3.0 μm.

$CdCl_2$ Passivation Treatment

After the deposition of the CdTe film, the substrate is then passed over a $CdCl_2$ source for the $CdCl_2$ deposition and activation process immediately after CdTe deposition, without breaking vacuum. An approximately 4 μm $CdCl_2$ film is sublimated on CdTe, where the $CdCl_2$ bottom source temperature is maintained at 447ºC while the top heater—to maintain substrate temperature—is set at 387ºC. This deposition takes 180 seconds, after which $CdCl_2$ activation is carried out for another 180 seconds, wherein both top and bottom heater temperatures are maintained at 400ºC.[19] The cadmium chloride passivation treatment is carried out in an N_2 atmosphere. After $CdCl_2$ activation for 180 seconds the substrate is transferred to a cooling station for 300 seconds, which has only a top heater maintained at 435ºC. This station does not possess a bottom heater. Following cooling, the substrate is removed from the ARDS and rinsed using deionized water.

CuCl Treatment

Copper chloride in controlled quantities has been known to be critical for the formation of back contacts and bulk doping of CdTe photovoltaic films.[40] For the Cu treatment of CdTe film with $CdCl_2$ passivation is reintroduced into the ARDS and heated for 85 seconds using a heating source set at 330ºC. Following the preheating step, the substrate is introduced into the CuCl sublimation source, where the bottom source temperature is set at 190C and the top heater for the substrate is set at 170ºC. CuCl sublimation is performed for 110 seconds and then the film is annealed in another process station within the ARDS at 200ºC top and bottom source temperatures for 220 seconds.

Te Back Contact Deposition

The 20 nm tellurium back contact is deposited using a Cooke Vacuum Products physical vapor deposition (PVD) system: model MK VII – FR. 99.999% pure tellurium pieces used for deposition are obtained from Sigma-Aldrich Corporation. Tellurium pieces are placed in a molybdenum evaporation boat coated with alumina. Acoustic impedance for deposition is set at 9.81 g cm^{-2} s^{-1}. During deposition, the electric current is set between 70 A and 90 A to achieve a steady deposition rate of 5-10 Å/s. The deposition rate and thickness are measured using a quartz crystal monitor and monitored via an external

digital display. A sliding shutter between the deposition boat and the substrate allows for the abrupt start and termination of Te deposition on the substrate. This shutter is manually operated from outside the vacuum chamber. The pressure during Te deposition is maintained at 10^{-5} Torr or less. The substrate is not heated during Te deposition.

Carbon and Nickel Back Electrode Fabrication

Following the deposition of the 20 nm Te back contact layer, the films are ready to be coated with carbon and nickel paint to form the back electrode. Carbon (graphite) paint in a polymer matrix that is diluted using methyl ethyl ketone (MEK) is sprayed on the Te surface to a thickness of about 50 µm. This paint is allowed to dry for 2-5 minutes, after which similar nickel paint is sprayed. The nickel paint is made from fine nickel particles suspended in a polymer binder diluted with methyl ethyl ketone. The thickness of this nickel paint is about 100 µm. The painted surface is allowed to dry for 6-8 hours.

Delineation and Photovoltaic Device Fabrication

Once the paint is completely dry, the films are delineated into 25 square devices on each substrate, with each square device measuring approximately 0.65 cm^2. Delineation is carried out by masking the painted surface of the film and blasting the unmasked regions, thus exposing the TCO in the unmasked areas. Blasting is performed using plastic media to avoid damage to the glass and the TCO. A thin line of indium is soldered in the regions between the cells that have TCO exposed to from the front electrode contact.

Electrical Characterization

Electrical measurements are performed with a Model 10600 solar simulator from ABET Technologies using a high-pressure xenon arc lamp with an AM1.5 filter. Current density v/s voltage curves were generated based on electrical measurements performed using the Keithley 2420 SourceMeter controlled by a LabView program. The J_{SC} density was calibrated to cells measured by NREL. The device areas are measured using a webcam that takes an image of a backlit solar cell and counts the pixels below a certain brightness. Both the light intensity and area are calibrated before each set of measurements. The

cells are contacted by a fixture of spring-loaded pins that provide 4-point connection and collect current from all around the front contact of the device.

Scanning Electron Microscopy

A Jeol JSM-6500F Field Emission Gun Scanning Electron Microscope (FEG-SEM) is used for microstructural analysis of the cadmium telluride solar cell stacks, as well as for the individual layers which make up a cell. The FEG-SEM is generally used to look at the surface of the depositions using an in-lens detector, which requires a short working distance as it detects low energy secondary electrons coming from the surface of the sample. A high acceleration voltage of 20 kV with an aperture of 30 μm is used. Energy Dispersive X-ray (EDX) analysis is also carried out in the FEG-SEM using a 20 kV acceleration voltage and 60 μm aperture to give both quantitative and qualitative chemical analysis with a Thermo Noran energy-dispersive spectrophotometer (EDS).

Transmission Electron Microscopy (TEM) and Energy Dispersive X-ray Spectroscopy (EDS)

TEM is carried out using a Jeol JEM 2000FX equipped with an Oxford Instruments 30 mm^2 EDX detector and a Gatan Erlangshen ES500W digital camera above the phosphor screen. The TEM provides a clearer view of the grain structure than most other electron based techniques, as the electrons pass through the sample and are detected on the other side, giving a small interaction volume. As the sample is ultra-thin, EDX can also be carried out at a higher resolution, making the detection of any inter-diffusion between layers possible. The TEM sample dimensions are relatively small in comparison to SEM samples. A normal size would be 5 μm – 10 μm in length. This means that the sample's extraction location must be chosen with care. If a sample is not homogenous, several TEM samples must be produced at different locations to be able to observe any variation.

Scanning Transmission Electron Microscopy (STEM) is carried out in a FEI Tecnai F20 (S)TEM equipped with Gatan Bright and Dark field STEM detectors, a Fischione High Angle Annular Dark Field (HAADF) STEM detector, a Gatan Enfina Electron Energy Loss Spectrometer, and an Oxford Instruments X-Max 80mm^2 windowless energy-dispersive spectrometer (EDX). STEM imaging is

performed at 200 kV with a camera length of 100 mm and condenser aperture size of 70 μm using a spot size of seven. HAADF images are collected in conjunction with STEM bright field images. HAADF imaging gives a unique perspective, as the higher the atomic weight of the material, the more the electrons passing through the sample will be detected. Therefore, the amount of signal collected will depend on the atomic weights of the sample, providing atomic weight contrast in the image.

The (S)TEM system is equipped with a Silicon Drift Detector (SDD), allowing high spatial resolution Energy Dispersive X-ray (EDX) measurements and chemical mapping. This is largely used for mapping the diffusion of elements such as chlorine and sulphur in the cadmium telluride matrix. Point analysis is also useful, as quantification of elements can be acquired with a sensitivity of ~0.5 at% for light elements such as chlorine. EDX spectra are collected for 120 seconds. Maps are collected using the largest condenser aperture (150 μm) with the largest spot size. This allows for a high number of counts. The dead time is controlled by changing the process time; each frame took approximately 120 seconds to collect. Maps are collected from in periods from ten minutes to one hour with no discernible sample drift.

Focused Ion Beam (Dual Beam) TEM Specimen Fabrication

High quality TEM samples are prepared using an FEI Nova 600 Nanolab dual-beam system, where a standard in-situ lift-out procedure is used. This involved depositing a layer of platinum onto the sample surface above the area to be analyzed, using the ion beam with a current of 0.5 nA. A typical area of 20 μm by 2 μm is covered, with a thickness of 2 μm. An SEM image showing the sample after it is deposited is shown in Figure 4.1A. If the top 50 nm of the sample is required for analysis, then a layer of electron beam deposited platinum (using a voltage of 5 kV and current of 1.1 nA) is deposited before the ion beam platinum. Electron beam platinum is advantageous in that it does not implant ions into the sample surface; however, the deposition of platinum with the electron beam is too slow to use for the whole platinum layer thickness. Two staircase trenches are then cut on either side of the platinum layer which are approximately 25 μm x 15 μm; the depth depends on the sample etching rate, but it is usually of the order of less than 10 μm using an ion beam current of 20 nA, as shown in Figure 4.1B. After the formation of the trenches a few micrometers from the platinum, a cleaning cross section is used at the

lower current of 7 nA to clean up to the platinum, leaving a sample of approximately 1 micrometer thick, shown in Figure 4.1C. Once this is done, the sample is tilted to 7º and a U-shaped cut is formed, leaving a small uncut part to support the sample shown in Figure 4.1D. The omniprobe is then inserted and welded onto the platinum protective layer, with the platinum at 50 pA shown in Figure 4.1D, and the final support of the TEM sample to the bulk sample is then disconnected using a 1 nA beam. Once this is done, the sample should be free and lifted out on the needle by lowering the stage. The next step is to attach the TEM sample to a copper grid and detach it from the omniprobe using a platinum weld at 50 pA and ion beam at 1 nA, respectively.

Once the sample is attached to the copper grid it can be further thinned down to approximately 100 nm, as shown in Figure 4.1F. This is achieved by milling the sample with the ion beam, starting at 1 nA with the sample tilted 0.7º either side of 52º. The sample is milled until it is 500 nm thick. The ion beam current is then reduced to 0.5 nA, and the end 10 μm of the sample is milled on each side until the sample is 200 nm thick. The current is further reduced to 0.3 nA and the end 5 μm is thinned to 150 nm. Finally, the last 5 μm of the sample is thinned using a 100 pA current until the thickness is ~100 nm.

X-ray Diffraction

Glancing angle X-ray diffraction is conducted using a Bruker D8 Discovery system. The Cu Kα radiation is 1.54060 Aº and the grazing incident angle is 2º degrees. The scintillator detector is scanned from 10º degrees to 80º degrees with a step size of 0.05º degrees and scan speed of 1º/min. The measured peaks were fitted using a Pearson VII function in a R programming script (reference) and compared with JCPDS card #00-015-0770 for Cadmium Telluride.

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The references are not consistent. Sometimes et al is used but in others all the authors are named. Sometimes & is used and sometimes not. All capitals are used for one paper title. Needs to be made consistent.

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Author Contribution

The investigation of higher sublimation temperatures was initiated by Kurt L. Barth. The idea of using a higher temperature deposition for CdTe, along with the $Mg_{0.23}Zn_{0.77}O$ buffer layer, was proposed by Amit H. Munshi and Kurt L. Barth. Fabrication of devices and some material's characterization for this study was performed by Amit H. Munshi. TEM imaging and EDS mapping was performed by Ali Abbas and analyzed by Ali Abbas and John M. Walls. Electrical characterization of finished devices was performed by Amit Munshi. Jason Kephart was responsible for the development of the Ta_2O_5/SiO_2 antireflection coating, as well as the $Mg_{0.23}Zn_{0.77}O$ buffer layer. XRD data was collected and analyzed by Tushar M. Shimpi. The manuscript was mainly written by Amit H. Munshi, Jason M. Kephart, Kurt L. Barth, and Tushar M. Shimpi. Walajabad S. Sampath is the principle investigator leading the entire project.

Competing interests

The authors declare no competing financial interests.

Figures:

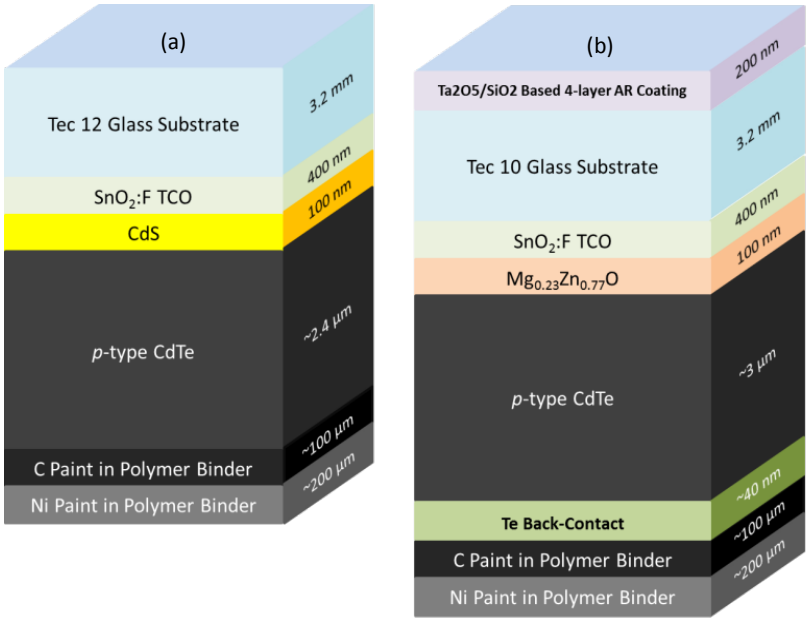


Figure 1| Schematic of (a) CdS/CdTe baseline device (b) device with changes incorporated to achieve high efficiency (not to scale).

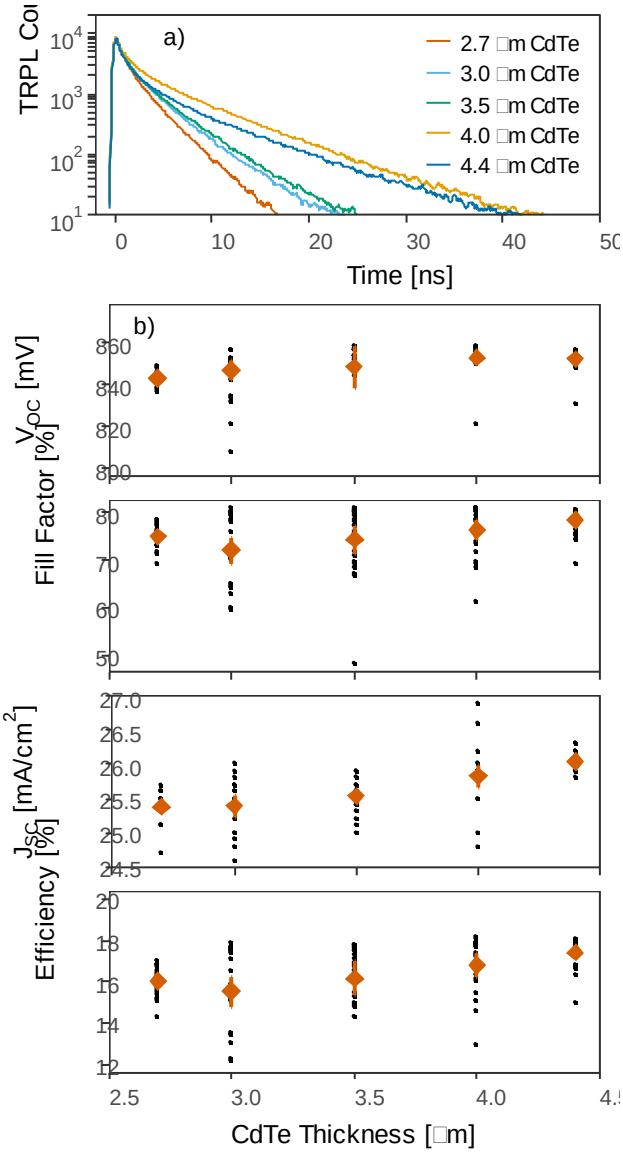


Figure 2|Effect of varying absorber thickness (a) TRPL measurement showing improved carrier lifetime with increasing absorber thickness **(b)** performance parameters of devices with varying absorber thickness.

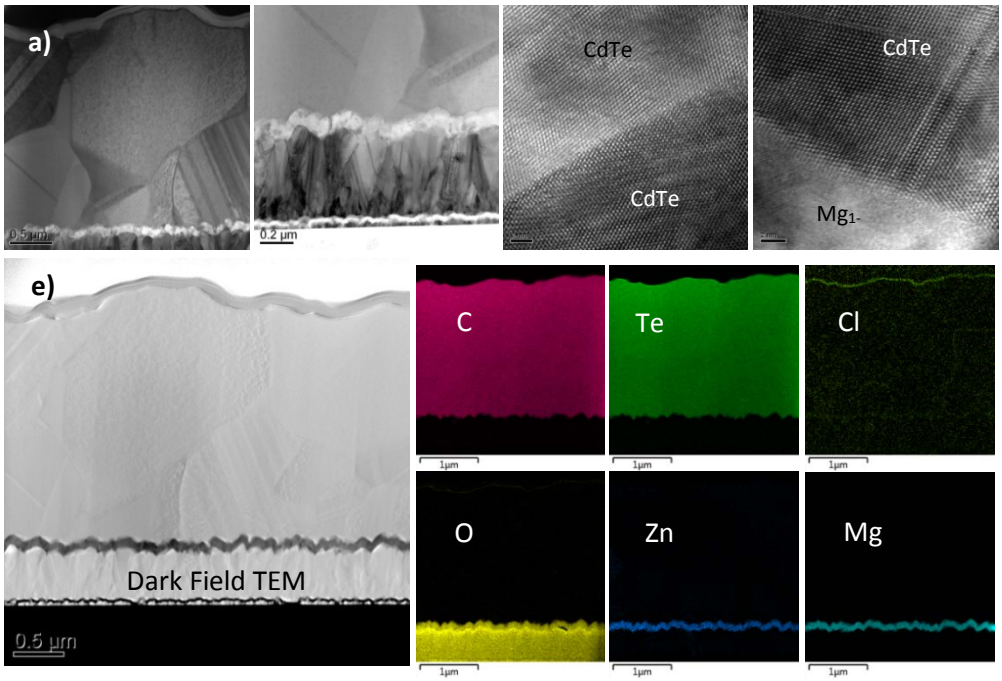


Figure 3|Microscopic analysis. (a)TEM image TCO/$Mg_{0.23}Zn_{0.77}O$/CdTe/Te film stack **(b)** high magnification TEM image of TCO/ $Mg_{0.23}Zn_{0.77}O$ and $Mg_{0.23}Zn_{0.77}O$/CdTe interface showing conformal coverage of $Mg_{0.23}Zn_{0.77}O$ **(c)** HRTEM image of CdTe grain boundary showing no apparent signs of line or bulk defects **(d)** HRTEM image of $Mg_{0.23}Zn_{0.77}O$/CdTe interface showing abrupt interface with minimal intermixing **(e)** EDS elemental map of TCO/$Mg_{0.23}Zn_{0.77}O$/CdTe/Te film stack showing no diffusion of materials within detection limits.

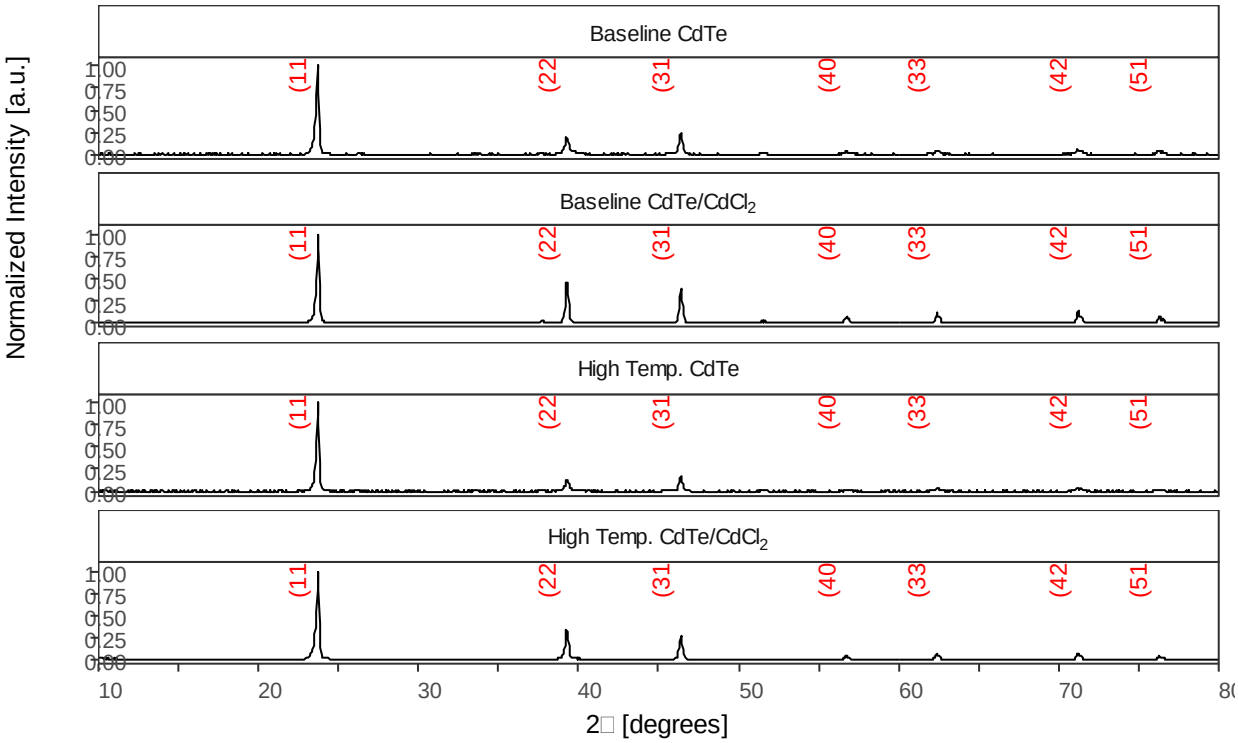


Figure 4| XRD analysis of film orientation. XRD Peak intensities showing increased {111} orientation and less randomization of CdTe films sublimated at higher temperature on $Mg_{0.23}Zn_{0.77}O$ buffer before and after $CdCl_2$ passivation treatment.

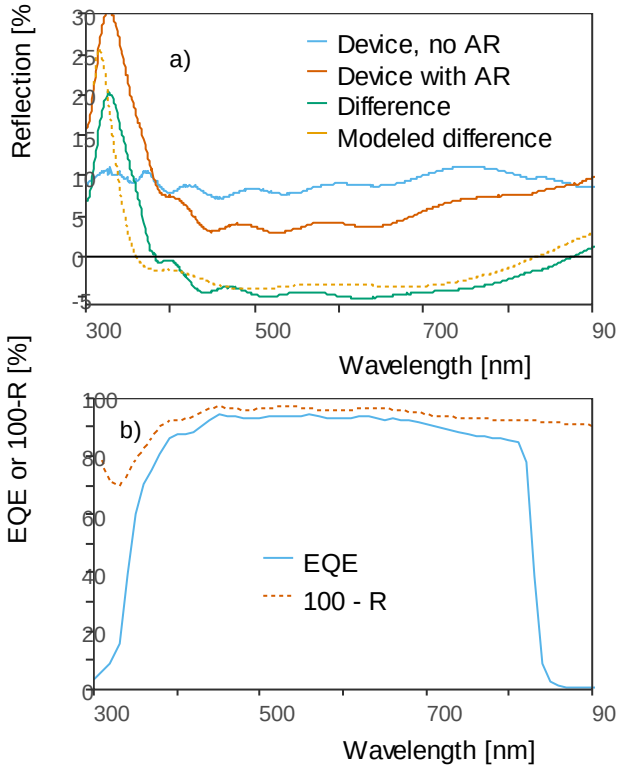


Figure 5|AR Coating (a) Reflection vs wavelength comparing modeled against actual difference in reflection and **(b)** external quantum efficiency for AR coating used in this study.

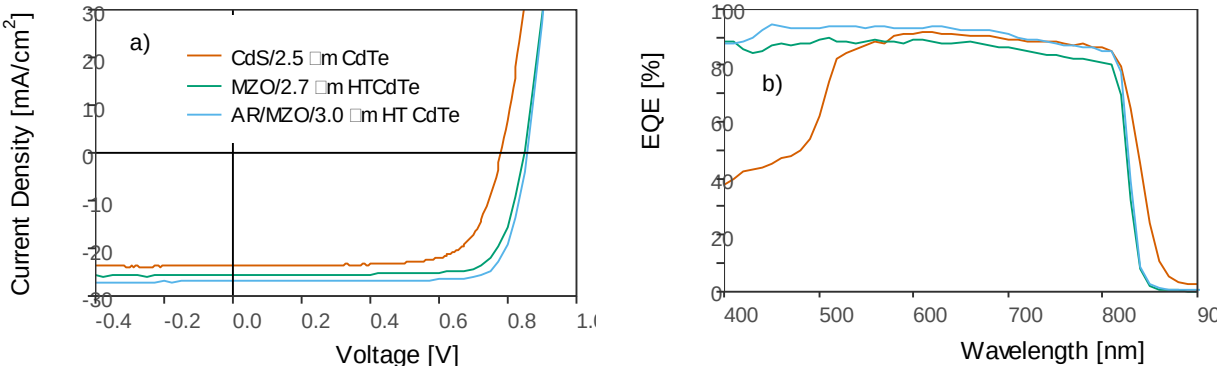


Figure 6| J-V (a) and EQE (b) comparing performance of CdS/CdTe baseline device, MZO/CdTe high temperature (HT) device and high efficiency high temperature (HT) device with AR coating

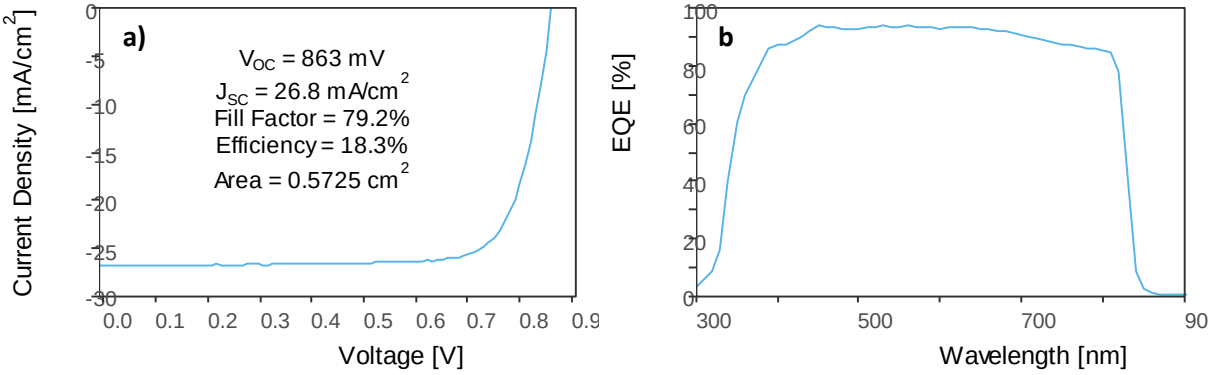


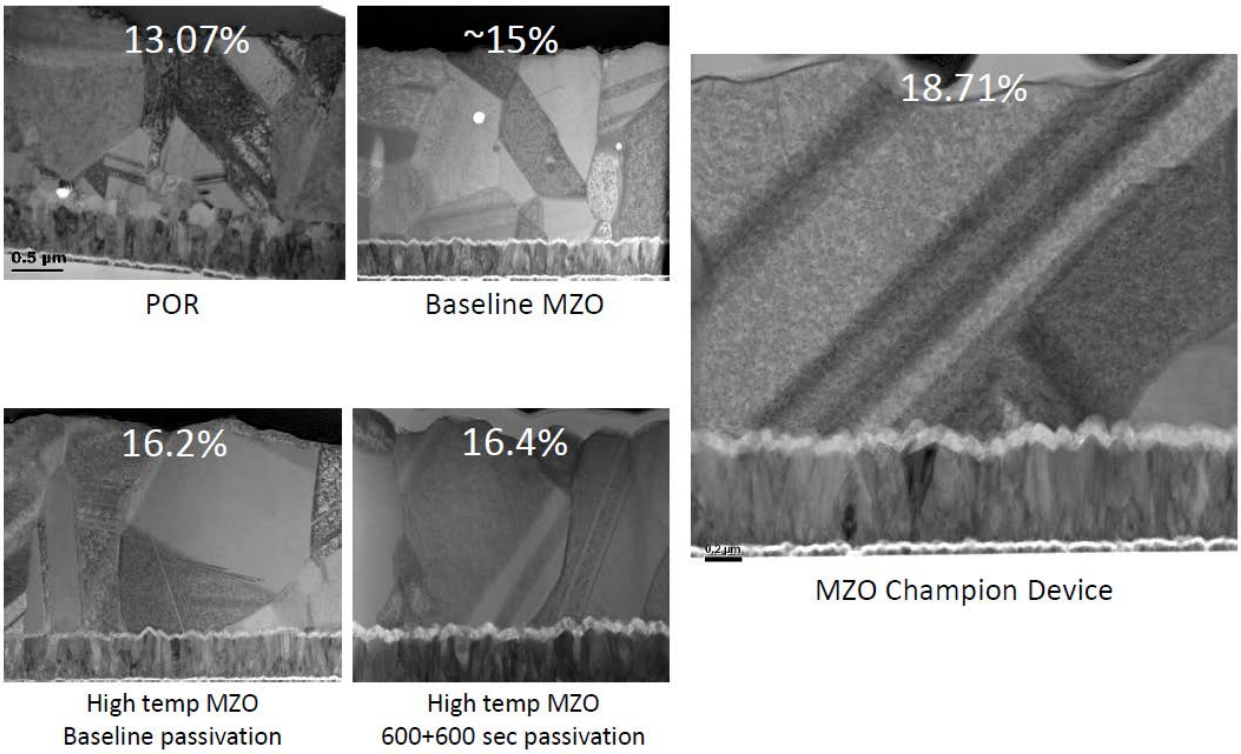
Figure 7| ILX Lightwave certified results. (a) J-V Curve **(b)** and External quantum efficiency for device structure under investigation

Table 1| Best performing devices measured within the presented study

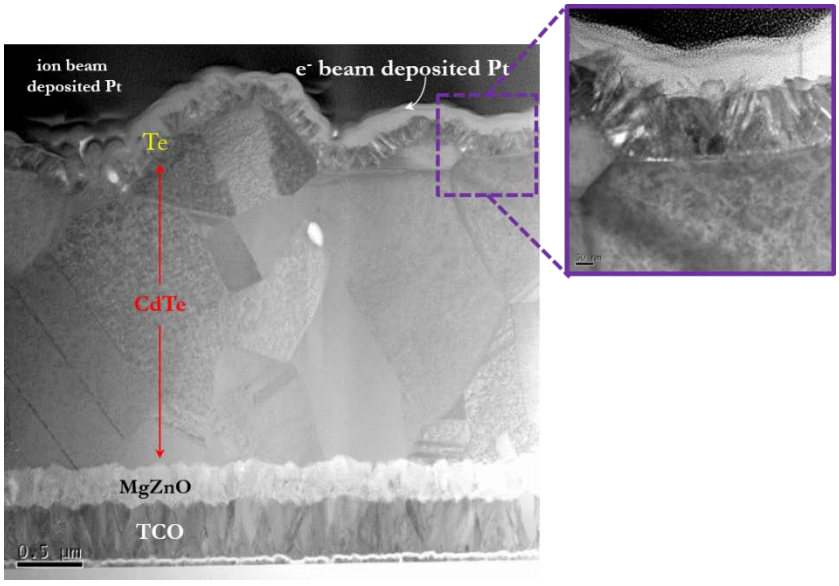
	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	Efficiency (%)	Cell Area (cm^2)
1A	858	27.1	80.5	18.71	0.661
1B*	863	26.8	79.2	18.30	0.573**
2	856	27.0	80.1	18.55	0.669
3	856	27.1	79.7	18.46	0.665
4	857	27.0	76.6	18.40	0.666
5	858	26.9	80.5	18.61	0.667
6	858	27.0	80.2	18.59	0.665

*Sample 1B is certified performance for sample 1A by ILX Lightwave, Newport, CA on a masked area**.

Supplementary Figures



Supplementary Figure 1| Cross-section HRTEM images of CdTe films showing the effect to larger CdTe grain size on device efficiency.



Supplementary Figure 2| Cross-section HRTEM images of CdTe uniform coverage of Te on CdTe surface

Supplementary Table 1| For lattice parameter calculation, 2θ values from the first three high intensity peaks

2Θ	*Lattice Parameter (Å)*	*% change wrt standard value*
Baseline (No $CdCl_2$)		
23.735	6.487	0.09%
39.257	6.485	0.13%
46.408	6.484	0.05%
Baseline ($CdCl_2$)		
23.762	6.480	-0.02%
39.275	6.482	0.09%
46.404	6.484	0.06%
HT (No $CdCl_2$)		
23.748	6.484	0.04%
39.266	6.484	0.11%
46.409	6.483	0.05%
HT ($CdCl_2$)		
23.754	6.482	0.02%
39.275	6.482	0.09%
46.450	6.478	-0.04%