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Temporal Evolution of Electric Field Distribution and Energy Dissipation in a Metallized Polymer Film Capacitor under DC, AC, or Nonsinusoidal Voltage Stresses

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Abstract

Temporal evolution of electric field distribution and its resulting energy dissipation in a metallized polymer film capacitor is an important indicator of the scale of breakdown discharges within the capacitor unit when it is subjected to an external voltage stress. To gain an understanding of the dependence of breakdown discharges on the characteristics of the external voltage, an equivalent circuit model is developed to simulate the dynamics of the field distribution under three different types of voltage stresses, namely DC, AC, and non-sinusoidal. Pattern of the electrode segmentation is taken into account by means of an effective surface resistance. Also included are the effects of the number of electrode segments cross a given length. Electric field distribution and its temporal evolution are computed and the peak electric field is calculated to provide an indication of the likelihood of surface flashover between two adjacent current gates. In addition, electric energy dissipation is calculated to assess potential temperature rise within the capacitor and so its implication on uncoupling of distant current gates. These calculations are repeated for different values of surface resistance and segmentation number such that certain guidelines for capacitor design can be drawn.

1. Introduction:

For metallized polymer film capacitors used in power systems, electric field distribution and the associated energy dissipation within a capacitor unit is an important indicator of the scale of breakdown events. This in turn illustrates the level of energy density that can be achieved with specific capacitor designs. Some of the aforementioned issues have been addressed experimentally[1], albeit costly and sometimes difficult, for instance to yield the electric field distribution. To aid this, it is highly desirable to develop appropriate theoretical tools.

In this paper, an equivalent circuit model is developed to simulate dynamics of the electric field distribution under three different types of voltage stresses, namely DC, AC, and non-sinusoidal. Numerical computations based such a model are then used to assess peak electric field on the surface of metallized polymer films and energy dissipation associated to ohmic losses for different values of key system parameters.

Subsequently possible guidelines for capacitor design drawn from these numerical studies will be discussed.

2. Circuit model of film capacitors:

A power film capacitor typically consists of a few thousand flattened polymer layers stacked together and immersed in an impregnation medium (silicon oil or insulating gas) in the packaging case unit[2]. As shown in figure 1, each flattened polymer layer is coated on one side with a thin metallic film, which has one of its side edges connected to an electrode terminal and the other insulated with a side margin. These side margins are arranged to be on alternating sides of the stacked polymer layers such that the metallic coatings are connected alternatively to two external electrode terminals[3]. A rigorous simulation requires simultaneous computation of electrostatic field, fast transients, thermal evolution, and discharge ignition and dynamics in three dimensions[4]. This is formidable and will take many progressive steps of improvement in their physical and numerical models.

Figure 1 A Section of a typical film capacitor.

As a first step, we consider a simplified capacitor configuration consisting of a single polymeric layer to allow a one-dimensional simulation of the electrostatic and electromagnetic fields in a film capacitor. The presence of the impregnation medium and the case unit is ignored. Also neglected are thermal effects. This 1D model permits an efficient computation routinely repeatable on a power PC and provides insights for model improvement of film capacitors.

Furthermore we assume that the polymeric film is deposited on both sides each with a thin metallic coating which is then connected to an external voltage. Thus the top and bottom metallic films act as the electrodes for the single-layer film capacitor. The electrode materials are however assumed to be resistive rather than perfectly conductive. This allows them to be described by means of surface resistors in equivalent lumped circuit models of film capacitors.

Electrode coatings in power capacitors are usually segmented and their segmentation can usually be decomposed into inter-connected square segments each having the same mosaic design[1][5]. This allows us to describe each one of them using a lumped surface resistor of identical resistance. As a result, a two-dimensional network of identical lumped resistors may be used to describe one electrode layer.

Based on the above model, a horizontal stripe of the capacitor electrode coating with a width equal to the size of one electrode segment can be divided by an array of identical segments. As there are two electrode coatings, each on one side of the polymer film, they are modelled by two parallel arrays of series-connected identical resistors, each having the same surface resistance, R_s , as shown in figure 2. To account for the presence of the polymeric film, a series of shunt capacitors are also added to connect the two arrays of lumped resistors.

Figure 2 An equivalent lumped circuit model for a single layer film capacitor.

In figure 2, R_{end} represents the resistance from the electrode edge to the external voltage source, which in the case of practical film capacitors is the resistance from the edge of the metallic coating, through the end-spray, to one terminal of the voltage source. Resistance of capacitor's external connection is usually much lower than the surface resistance of the electrode. If the surface resistors of the first and the last mosaic elements are absorbed into the two end resistors, respectively, in the circuit of figure 2, R_{end} may be approximated by R_s .

It should be mentioned that the equivalent circuit of figure 2 only models one stripe of a single-layer film capacitor. Nevertheless since this is a one-dimensional model, the remaining part of the single-layer film capacitor of area $W \times L$ may be considered as being charged up by separate but identical voltage sources. Their behaviours should therefore be at least very similar to that of the single-layer film capacitor, especially the eventual field distribution.

For numerical examples discussed here, the length of the capacitor stripe is fixed to 15cm and divided by m divisions to form an array of m square segments. Thus lumped resistors used in figure 2 take the value of the surface resistance of one segment. Depending on the mosaic pattern used, the surface resistance is between 5Ω and 200Ω although surface resistance as high as $1k\Omega$ has been considered[3][5][6]. Note that large surface resistance may lead to large electric energy dissipation on the electrode coatings. Thus a small nominal surface resistance of $R_s = 50\Omega$ is assumed,

although the effects of different surface resistance will be assessed using numerical examples. On the other hand, the capacitance of each shunt capacitor depends on the number of segmentations in the length of L . Assuming all individual shunt capacitors have the same capacitance, we have

$$C_m = \epsilon_0 \epsilon_r (L/m) \times (L/m) / d \quad (1)$$

where d is the film thickness and ϵ_r is its relative permittivity. We choose $d = 10\mu m$ and $\epsilon_r = 2.3$. Thus

$$C_m = 4.5799 \times 10^{-8} / m^2. \quad (2)$$

3. Results for DC stresses:

A set of circuit equations is formulated for the circuit in figure 2 and a computer program is subsequently developed to simulate the evolution of electric field distribution in a single-layer film capacitor. Typically this program takes a few minutes of CPU time on a power PC to complete the simulation of charging processes in a power capacitor of given parameters. Figure 3 is a plot of capacitor voltage against, x , the distance from the left-hand edge of the capacitor along its electrode surface, at $t = 0.1 \tau_0$ where τ_0 is the time constant of the circuit in figure 2.

Figure 3 Spatial distribution of normalised capacitor voltage at $t = 0.1 \tau_0$.

Figure 3 suggests that during the charging processes capacitor voltage has a spatial distribution and therefore there exists a finite surface electric field. The maximum surface electric field occurs at the edge of capacitor electrode coating. Also if there are more mosaic segments over a given electrode length, this surface electric field tend to be larger. When the capacitor is fully charged, capacitor voltage will become the same across the electrode surface and so the surface electric field decreases to zero.

Surface electric field at the capacitor edge reaches its peak at the beginning of the discharge processes. Figure 4 is a plot of the peak surface electric field as a function of segmentation number. As it is shown, the peak surface electric field can reach $283V/cm$, well below the breakdown field of around $3kV/mm$ in air[7]. However experiments done with contaminated glass and porcelain suggest that a surface electric field as low as

300V/cm can assist an initially small spark surface discharge to become an elongated surface flashover discharge and cause the insulator to fail[8]. Given that the mosaic pattern may enhance surface electric field considerably, a surface field of 283V/cm for the $m=17$ case implies field assisted elongation of surface discharges can be an important issue for film capacitors.

Figure 4 Peak electric field reached for different segmentation number.

Figure 5 Temporal evolution of power dissipated on electrode at various surface resistance

The establishment of surface electric field leads to power dissipation on the capacitor electrode. A quantitative evaluation of dissipated heat is important to estimate thermally assisted uncoupling of distant current gates[1]. In figure 5, the power dissipated on the two electrode coatings is plotted as a function of time for different values of surface resistance for $m = 17$. It is shown that low surface resistance leads to a large instantaneous dissipation power with a rapid decrease from its peak value. On the other hand, large surface resistance results in a comparatively low peak value of the instantaneous power but gradual reduction from the peak power. In other words, a low level of surface resistance leads to strong and short power dissipation whereas large surface resistance results in gentle and lengthy power dissipation.

The time-averaged impact of the power dissipation in figure 5 may be appreciated by means of the eventual energy density. It is found that the energy density is independent of surface resistance. Also as the segment number increases from $m = 5$ to $m = 17$ the energy density is found to reduce monotonically from 0.644mJ/cm^2 to 0.637mJ/cm^2 , a reduction of 1.1%. This implies that for film capacitors with large segment

number the induced temperature rise is only slightly less than that with small segment number.

4. Results with AC stress:

When stressed with an AC voltage, an originally unchanged capacitor undergoes an initial charging process before arriving at its steady state. Depending on the time constant of the circuit, this initial charging process usually completes within the first cycle of the applied voltage for frequencies significantly below $1/\tau_0$. For cases studied here, $\tau_0 = 0.46\text{ms}$ and so the above assumption is true for frequencies up to 200kHz. Figure 6 shows the surface electric field at $x = L/2$ against time for different signal frequencies.

Figure 6 Temporal evolution of the surface electric field at different source frequencies.

Surface electric field reaches its peak periodically in response to the externally applied sinusoidal voltage. Similar to the DC case, the peak surface field is at its highest at the edge of the capacitor film. Figure 7 is a plot of the peak surface electric field at the capacitor edge as a function of frequency for $R_s = 50\Omega$ with different segmentation numbers. It is clear that the surface field is proportional to the frequency with a proportionality coefficient of approximately 2.14mV/cm/Hz and this proportionality is independent of segment number. However it increases linearly as the surface resistance is increased.

Figure 7 Peak surface field against source frequency.

Finite surface field suggests power dissipation on electrode surface. Figure 8 shows the dissipated power density against time, which exhibits an initial charging process before the steady-state sinusoidal oscillation is reached. More interestingly is that the dissipated power is

much higher at larger source frequencies. As the source frequency increases from 50Hz to 10kHz by a factor of 200, the peak power density increases from 0.2mW/cm² to 8W/cm², a factor of 40,000. Thus the dissipated power is proportional to the square of source frequency. This is consistent with the finding of figure 7 where the surface electric field is shown to be proportional to the frequency.

Figure 8 Temporal evolution of dissipated power density at different source frequency.

5. Results with non-sinusoidal stress:

Non-sinusoidal signals considered here consist of a DC voltage and an impulse perturbation voltage, ie,

$$V_s = V_0 + V_m \exp(-t^2 / \tau^2) \quad (3)$$

For all numerical examples discussed here, $V_0 = 2.5\text{kV}$. Figure 9 shows the surface electric field at the middle of the capacitor film as a function of time for $V_m/V_0 = 0.15$ and $m = 17$. As it can be seen, the electric field is generally not large. The largest surface field is around 14V/cm for the $\tau = 0.5\mu\text{s}$ case, and in general the narrower the initial impulse perturbation voltage the larger the surface electric field.

Figure 9 Evolution of the surface electric field

The maximum peak surface field occurs at the edge of the electrode film, and it is found to be in linear proportion to V_m/V_0 . Also the largest peak field is reached around 90V/cm for the $\tau = 0.5\mu\text{s}$ case at $V_m/V_0 = 0.5$ for $m = 17$. This should be compared to the DC case of figure 4 where the peak surface field at an applied voltage of 2.5kV is around 280V/cm for $m = 17$. Thus proportionally the surface field is higher in the DC case than the non-sinusoidal case.

The eventual dissipated energy density is shown in figure 10 as a function of the perturbation voltage. Interestingly the $\tau = 2\mu\text{s}$ case results in the largest energy

density. This is because the total energy associated with the impulse perturbation is large when the pulse duration is large. Consequently it is clear that an impulse voltage perturbation of long duration induces low peak surface electric field but results in large dissipated energy density. It is worth noting that these two aspects are related to the onset of breakdown and thermal effects respectively.

Figure 10 Dissipated electric energy density as a function of the perturbation voltage.

6. Conclusion:

An equivalent circuit model has been developed for metallized film capacitors used in power systems. Based on a simplified film capacitor model, surface electric field and associated dissipated power has been calculated for different external voltage conditions, namely DC, AC, and non-sinusoidal stresses. It has been established that segmentation number and surface resistance influence the level of surface electric field and dissipated power, especially for DC cases. For AC and non-sinusoidal cases however, the source frequency and impulse duration can also affect significantly the surface electric field and dissipated power density.

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