Polycrystalline CdSeTe/CdTe Absorber Cells with 28 mA/cm^2 Short-Circuit Current

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***Abstract* — An 800-nm CdSeTe layer was added to the CdTe absorber used in high-efficiency CdTe cells to increase the current and produce an increase in efficiency. The CdSeTe layer employed had a band gap near 1.41 eV, compared to 1.5 eV for CdTe. This lower band-gap allowed a current increase from approximately 26 to over 28 mA/cm^2. Voltage same as earlier demonstrated high efficiency CdTe-only device was maintained. The fill-factor was not significantly affected. Improving the short-circuit current and maintaining the open-circuit voltage lead to device efficiency over 19%. QE implied that the approximately half the current was generated in the CdSeTe layer and half in the CdTe. Cross-section STEM and EDS showed good grain structure throughout and diffusion of Se into the CdTe layer was observed. To the best of authors' knowledge this is the highest efficiency polycrystalline CdTe photovoltaic device demonstrated amongst universities and national labs.**

I. Introduction

Thin-film CdTe photovoltaic panels have demonstrated very low cost of photovoltaic electricity generation, particularly for utility scale applications [1]. With improvements in fabrication processes, research scale small devices have recorded efficiencies as high as 22.1% [2] while commercial modules have achieved upto 18.6% [3]. The average production efficiency of such modules has increased from 13.5% to 16.2% between 2014 and 2016 [4], [5].

Improving the efficiency of photovoltaics without substantially increasing the manufacturing cost is key to further reductions in the cost/Wp of photovoltaic modules for commercial applications. One way of increasing the efficiency of thin-film photovoltaic devices is to improve the short-circuit current. This can be achieved in several ways including the use of more transparent window-layers, anti-reflection coatings and a more transparent glass/TCO substrate. The authors have previously demonstrated 18.7% efficiency for polycrystalline thin-film CdTe devices using higher deposition temperatures, a Te layer in the back contact, and the use of anti-reflection coating[6][7]. This study demonstrates the use of a CdSeTe/CdTe absorber structure to further improve short-circuit current for II-VI photovoltaic devices.

Lowering the band-gap of the absorber material can increase the photon fraction above the band-gap of the material leading to improved short-circuit current. Previous studies using these alloys for this purpose [8][9] have shown promise for the use of CdSeTe in PV cells. This study demonstrates the results from utilization of $CdSe_{1-x}Te_x$/CdTe absorber structure to improve the short-circuit current and thus improve the overall efficiency.

II. Experimental Details

The cells used in the study were deposited on NSG TEC 10 soda lime glass coated with fluorine-doped tin oxide (FTO), a transparent conducting oxide (TCO). A $Mg_xZn_{1-x}O$ (MZO) buffer layer instead of the more common CdS was deposited using RF sputter deposition. CdSeTe films were sublimated using an optimized deposition process followed by sublimation of the CdTe layer. The $CdSe_xTe_{1-x}$ (CdSeTe) and CdTe depositions were followed by $CdCl_2$ passivation, performed in-line without breaking vacuum [10]. The substrate was heated to about 540ºC before starting the sublimation of CdSeTe. The temperature of the substrate was measured in-situ using a pyrometer located outside the preheating station.

The CdSeTe vapor source was heated to 575ºC and CdSeTe films of 800 nm thickness were deposited. The CdSeTe composition used for this study had 20% Se in the source material. Band-gap of as-deposited film was measured to be 1.41 eV using transmission measurements and Tauc Plot. After deposition of CdSeTe, the sample was moved to the CdTe sublimation vapor source and a film ~3.4 µm thick was deposited. The CdTe sublimation source temperature was maintained at 555ºC. $CdCl_2$ treatment is known to promote grain growth in CdTe films[11]–[14]. An aggressive $CdCl_2$ passivation treatment was performed for CdSeTe/CdTe films to promote inter-diffusion between these layers and avoid an abrupt interface. In addition to this, $CdCl_2$ treatment also is known to passivate the grain boundaries that leads to higher device performance[15]. For $CdCl_2$ passivation treatment, after deposition of CdSeTe and CdTe layers the substrate was transferred to the $CdCl_2$ treatment station without breaking vacuum. The $CdCl_2$ deposition source was maintained at

450ºC while the substrate heater for this source was maintained at 425ºC. The passivation treatment was performed for 600 seconds. This temperature gradient was maintained to ensure a thin film of $CdCl_2$ got deposited on the substrate. After the $CdCl_2$ treatment, the film was allowed to cool under vacuum for 180 seconds and then removed from the deposition chamber. After removing the film from the deposition chamber, the films were rinsed with deionized water to remove residual $CdCl_2$ from the surface and surfaced dried using ultra-high purity N_2 gas.

Thereafter, the films were heated to ~140ºC, and CuCl was deposited on the film surface for 110 seconds[16]. The CuCl deposition source was maintained at 200ºC while the substrate heater for the CuCl station was maintained at 170ºC. This was followed by 220 seconds of annealing at 220ºC in continued vacuum to form a Cu back contact. A 20-nm Te film was evaporated to improve the back-contact[17]. Carbon and nickel paint in a polymer binder where then sprayed on these films to form the back electrode.

Figure 1 shows a schematic of the full device structure. The individual cells were delineated using a mask and bead blasting using plastic medium to fabricate 16 small scale devices on the substrate. The devices each had an area of ~1 cm^2. The area of the aperture after masking the best performing device was measured to be 0.777 cm^2.

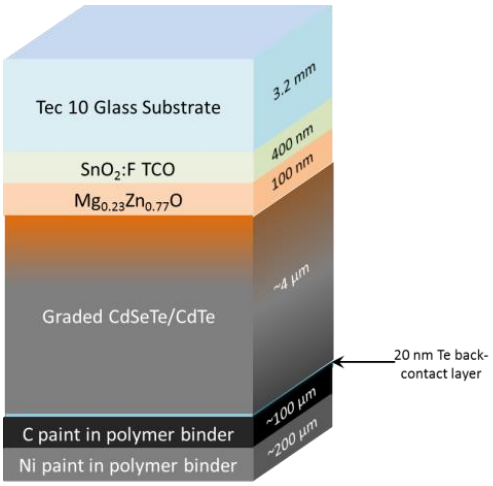

Fig. 1. Schematic of the CdSeTe/CdTe graded absorber device. (not to scale).

III. Performance

Figure 2 shows the current-density vs voltage comparison of a high efficiency device with CdTe absorber, with and without anti-reflection coating, earlier demonstrated by the authors. These high efficiency CdTe devices are compared to the device with CdSeTe/CdTe absorber described in section II. Table I shows the performance parameters of these 3 devices. The device with 19.1% efficiency demonstrated here is the highest efficiency polycrystalline CdTe device demonstrated by any academic institution to the best of authors' knowledge.

With the addition of Se alloy at the front of the device, a higher J_{SC} is achieved. This is due to the formation of a lower band-gap absorber layer at the front interface leading to higher absorption. The band-gap measured for this ~800 nm CdSeTe layer was 1.41 eV before device completion. Current density of 28.4 mA/cm^2 was measured for this cell. This was over 1 mA/cm^2 higher than the current density measured for the high efficiency CdTe device with anti-reflection coating.

TABLE I
Electrical Performance of High Performing Devices Showing Improvement in Efficiency Through Improved Absorption and Increase in Short-Circuit Current

Device Structure	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	% η
CdTe without AR	860	26.3	78.9%	17.9%
CdTe with AR	858	27.1	80.5%	18.7%
CdSeTe/CdTe without AR	854	28.4	79.1%	19.1%

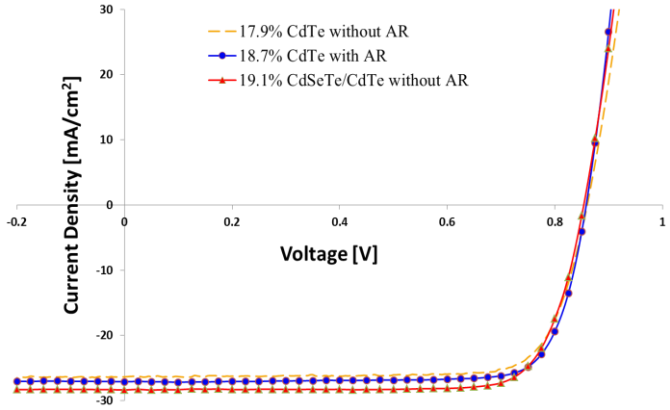

Fig. 2. J-V graph comparing the performance of a CdSeTe/CdTe device against a CdTe reference device

The external quantum efficiency (EQE) of the CdSeTe/CdTe and high efficiency device without anti-reflection coating (Fig. 3) was essentially identical below 700 nm, and after correction for reflection, the internal quantum efficiency in both cases was very close to unity. Above 700 nm, there appeared to be two differences between the CdTe device without anti-reflection coating and the CdSeTe/CdTe. The QE of the CdTe-only absorber showed a slight decrease below the band-gap cut-off, presumably due to reduced collection caused by higher recombination. Above 700 nm the response in CdSeTe/CdTe device was seen to be substantially higher and this device was found to absorb wavelengths above 850 nm up to about 900 nm.

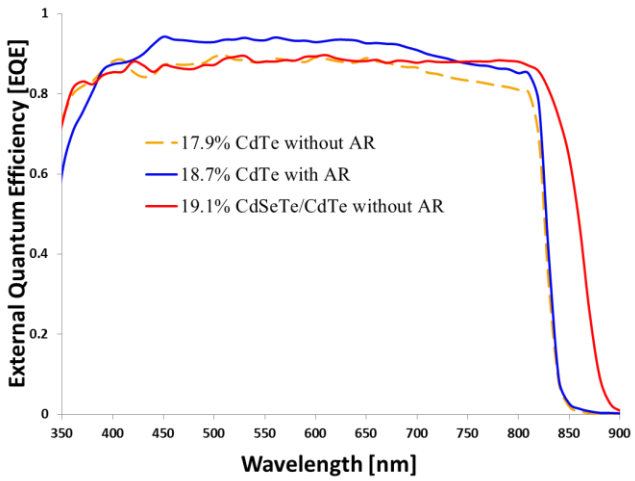

Fig. 3. Comparison of the quantum efficiency for CdSeTe/CdTe devices against high efficiency CdTe device.

The second difference above the CdTe cutoff clearly showed current contribution from the CdSeTe layer and was consistent with its 0.1-eV reduction in band-gap. The slant in that part of the curve followed directly from absorption of approximately half of the longer wavelength photons in the CdSeTe layer. The CdTe device with anti-reflection coating demonstrated increased response between 400 nm and 850 nm that resulted in higher J_{SC} (27.1 mA/cm^2) for this device. However, this improvement was still lower than the device with CdSeTe/CdTe absorber. This suggests large portion of the higher wavelength light was effectively utilized with the use of lower bang-gap CdSeTe. It is eminent that including an anti-reflection coating with the CdSeTe/CdTe absorber would lead to further improvement in short-circuit current.

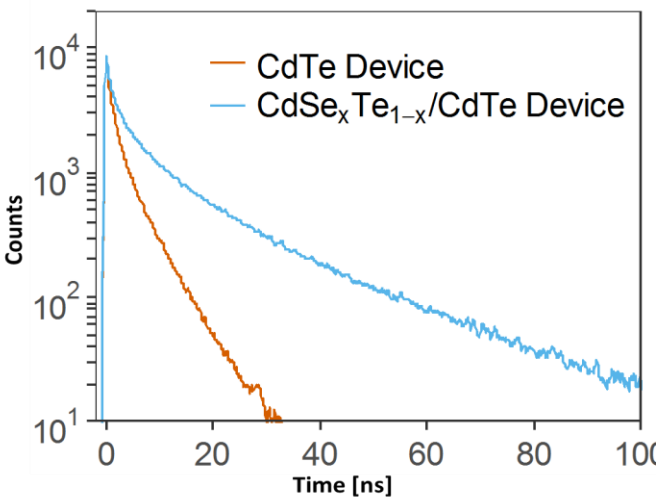

Fig. 4. Time-Resolved Photoluminescence (TRPL) measurement showing improved carrier lifetime with CdSeTe in the absorber.

Time-Resolved Photoluminescence (TRPL) measurements were performed for the high efficiency device with CdSeTe/CdTe absorber and compared to a high efficiency CdTe-only device. About 4-times higher carrier life-time of 21.9 ns was measured for the devices with CdSeTe/CdTe absorber as compared to CdTe-only absorber that demonstrated a carrier life-time of 5.5 ns. Carrier life-time as high as ~39 ns has been measured in similar devices with CdSeTe/CdTe absorber within this study. The cause of this improvement in carrier life-time is understood to be due to improved quality of the front interface between MgZnO and CdSeTe. Presence of lower band-gap CdSeTe adjacent to high band-gap MgZnO appears to produce a better band-alignment to give higher carrier life-time. In addition to this, presence of a higher band-gap CdTe at the back of CdSeTe maybe producing an effect similar to electron reflector [7], [18]–[20] which maybe partly responsible improvement in carrier life-time. The suggested electron reflection-like behavior of CdTe for CdSeTe requires further verification.

IV. Materials Characterization

In-depth microstructure characterization of the CdTe film was carried out using Transmission Electron Microscopy (TEM) and High Resolution Transmission Electron Microscopy (HRTEM). TEM samples were prepared using Focused Ion Beam (FIB) milling using dual beam FEI Nova 600 Nanolab. A standard in-situ lift out method was used to prepare the cross section sample through the film stack into the glass substrate. A platinum overlay was deposited on the top of the film to define the area of interest on surface of the sample, homogenize the final thinning of the samples and to avoid damage to the CdTe film surface from the ion beam. STEM bright-field images and high resolution TEM images were collected using a FEI Tecnai F20 (S)TEM operating at 200 kV Cross-section (S)TEM images and corresponding EDS maps revealed the grain-structure and elemental distribution for these devices. The (S)TEM image showed large CdTe

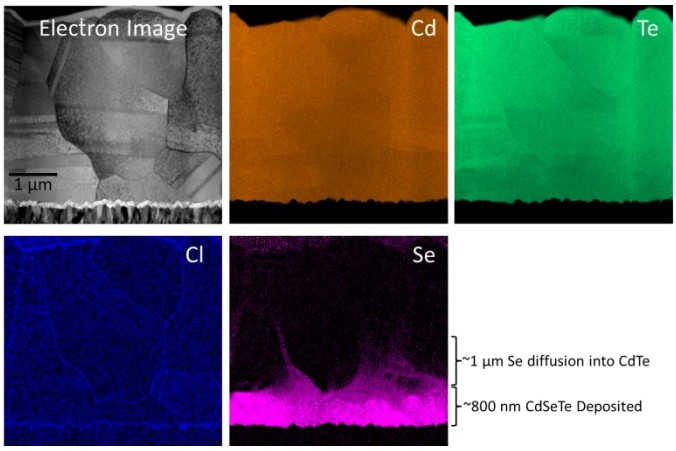

Fig. 5. A Cross-section STEM image with EDS maps for Cd, Te and Se along with over layered image showing distribution of elements in the thin-film CdSeTe/CdTe device.

grain. No stacking faults were present in the CdSeTe/CdTe absorber layer, although twin boundaries are visible. Coverage of CdSeTe/CdTe appears to be conformal over MgZnO buffer layer and no voids or abnormalities were observed in the

growth of the absorber layer. A 100 nm thick MgZnO buffer layer was deposited on the substrate prior to deposition of the CdSeTe layer. This MgZnO layer appeared to be preserved through the fabrication process and no diffusion of Mg, Zn and O into the absorber was detected within the limits of EDS. There appeared to be an abrupt interface between MgZnO and CdSeTe layer further reinforcing diffusion between these layers to be negligible, if any.

Authors in another study had shown that presence of grain boundaries that are perpendicular to the path of charges has a detrimental effect on device performance[6], [14]. Similarly, large grains in the absorber that grow along the thickness of the absorber correspond to better device performance. Improvement in device performance from such grain structure with large grains and fewer grain boundaries had a substantial positive impact on fill-factor. This behavior was observed with these CdSeTe/CdTe films as well. TEM cross-section shows large grains covering most of the thickness of the film. These devices demonstrate fill-factor over 79%. However, few grain boundaries that were formed perpendicular to the direction of charge conduction are observed. Reducing area of such grain boundaries may result in higher fill-factor and thus better device performance.

The EDS elemental maps (figure 5) showed that Cd and Te were retained in the absorber film. The Se concentration at the glass side of the film appears to be high up to a thickness of ~800 nm and it diffused up to about 1 µm into the following CdTe. EDS elemental map also showed Cl distinctly decorating the CdSeTe/CdTe absorber grain boundaries and CdSeTe/MgZnO interface. It had been demonstrated in the by Lee *et al* that Cl at the grain boundaries in CdTe films plays an important role in electronic performance of the devices[15]. This appeared to hold true for CdSeTe/CdTe devices. There appeared to be Cl present is some of the MgZnO grain

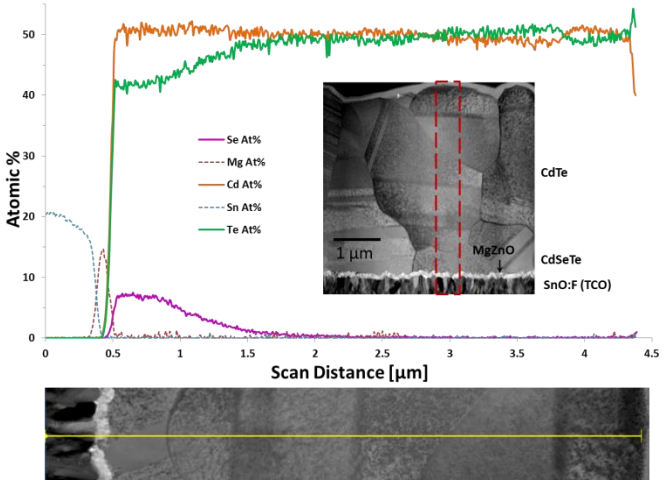

Fig. 6. A Cross-section EDS line-scan showing profile of Cd, Se, Te, Mg and Sn along the depth of thin-film CdSeTe/CdTe device. TEM image shows region where the scan has been performed.

boundaries but no such presence of Cl was detected at the interface of MgZnO and SnO:F (TCO). In addition, TEM images and EDS maps did not show Se being confined to certain grains closer to CdSeTe/MgZnO interface. Se was found to be present in grains that were graded from CdSeTe to CdTe. This suggested the growth of CdTe was epitaxial over CdSeTe that further helped in avoiding formation of an abrupt interface between CdSeTe and CdTe.

EDS line scan along the thickness of the absorber was performed that is shown in Figure 6. Region of the TEM cross section where the line scan was performed can also be seen in the figure. EDS line scan confirms the observation from the EDS elemental map that there was no substantial inter-diffusion between the MgZnO and CdSeTe layers. However, it reaffirmed higher concentration of Se in the first ~800 nm of the absorber and its gradual diffusion into the CdTe layer over next 1.5 µm – 2 µm. This helped in formation of a graded interface between the CdSeTe and CdTe layers which was believed to be advantageous for photovoltaic device performance.

V. Discussion

The external quantum efficiency indicated an improved absorption of light at higher wavelengths however, the effective band-gap of this material was still measured to be ~1.45 eV. Lowering the band-gap further to achieve higher short-circuit current density while maintaining higher voltage as well as fill-factor would be the logical next steps to achieve higher conversion efficiency. External quantum efficiency comparison showed that improving absorption between 700 nm and 900 nm wavelengths using lower band-gap CdSeTe has a greater impact on short-circuit current generation than increasing absorption between 400 nm and 850 nm using anti-reflection coating.

The elemental maps suggest that the process of grading the absorber material with Se was successful. Better grading of the absorber may be achieved by further optimization of $CdCl_2$ passivation treatment that may prove to be advantageous for device performance. Higher fill-factors may be achieved using more optimized $CdCl_2$ passivation treatment that would allow growth of larger grains in absorber that may lead to higher fill-factor and thus higher conversion efficiency.

Authors have currently been able to only maintain the open-circuit voltage when compared to earlier demonstrated high efficiency devices. However, TRPL results in this study showed about 4 times higher carrier life-time. This provides a basis to improve open-circuit voltage of the devices. Passivation of the front interface as well as reducing the back-surface recombination for such devices with CdSeTe/CdTe absorber may be necessary to achieve higher open-circuit voltage.

VI. Conclusions

To best of authors' knowledge, device performance demonstrated here is amongst the highest efficiency CdTe based photovoltaic device demonstrated by any university or national lab. Improvement in short-circuit current density of photovoltaic devices by using CdSeTe has been successfully demonstrated. Further refinement of the process is necessary to exploit the full potential of using Se in the absorber material. Long and high temperature $CdCl_2$ passivation treatment leads to the diffusion of Se into the CdTe film. However, this does not negatively affect the MgZnO buffer layer and the interfaces remain intact. External quantum efficiency measurements showed that the improvement in short-circuit current is due to improved absorption. From external quantum efficiency comparison it is evident that including an anti-reflection coating to the device demonstrated here would lead to devices with short-circuit current greater than 29 mA/cm^2. This along with improved fill-factor using more optimized $CdCl_2$ passivation treatment may be necessary to achieve device efficiencies in excess of 20%. High carrier life-time measured using TRPL provide basis for improving the open-circuit voltage that has been a major deficit with CdTe based photovoltaics. CdSeTe material used for fabrication of these devices contained 20% Se, however, from EDS line scan it can be observed that much lower i.e. ~8% is incorporated into the film. CdSeTe material with much higher Se composition may be necessary to further achieve higher absorption as well as further improve carrier life-time.

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