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***Stray Inductance Effects and Protection  
in  
GTO Thyristor circuits***

*by*  
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***A Doctoral Thesis  
Submitted in partial fulfilment of the requirements for the award  
of  
Doctor of Philosophy of the Loughborough University of Technology***

***JUNE 1990***

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## ACKNOWLEDGEMENTS

*I wish to express my deepest gratitude to my supervisor Dr. J K Hall for his guidance and assistance throughout the period of this research and for painstakingly proof-reading the text of this thesis.*

*I am indebted to my parents, brothers, brothers-in-law and sisters for their endurance and support throughout my research.*

*I wish also to thank Dr. C D Manning, Dr. C R Fitton, Mr. K Gregory and all my friends, especially Mr. A H Esuri, and colleagues in the Department of Electronic and Electrical Engineering for the rewarding discussions we had.*

*Also, I would like to acknowledge my appreciation to all the assistance provided by Mrs. M Cook, Mr. G Harris and Mr. D Thomas in the Computer Centre of the Loughborough University of Technology during my typing of this thesis.*

*Finally, gratitudes are due to my wife and daughter for their endurance and patience during the long hours of preoccupation in my studies.*

## ABSTRACT

*The recently developed gate turn-off thyristor is now becoming well established as the first choice switching device in high power converters for applications such as uninterruptible power supplies, frequency changers, and AC and some DC variable speed motor drives. The special operating features of these devices in conventional circuit configurations are investigated.*

*The GTO thyristor physical behaviour and operating characteristics are first described and supported by measurements made at turn-off currents of up to 600A on a specially constructed test circuit. From this, it is shown that, owing to the extremely fast rates of fall of anode current at turn-off, voltage overshoot effects caused by the stray circuit inductances are highly dangerous to the device, and effective snubbing is essential.*

*A detailed study of these stray inductance effects in constructed DC chopper and H-bridge inverter circuits follows. The circuits are modelled to include these strays, with appropriate mathematical analysis and computer simulation, to determine which stray inductances are the most influential in causing GTO thyristor voltage stress.*

*The different switching patterns are considered for the H-bridge to provide quasi-square and various pulse width modulated (PWM) output voltage waveforms, and the detailed current transfer paths in the various circuit devices and snubber components defined and mathematically analysed in each case. Practical switching effects of diode reverse recovery and GTO mismatched switching times are demonstrated and possible damaging conditions revealed.*

*All analytical and computed results are supported by experimental measurements.*

*A GTO thyristor will be damaged by attempting to turn-off an over-current, and satisfactory protection against this is essential. Conventional fusing is usually inadequate, and a better method is to use a fast active system utilising either a crowbar and fuse, or rapid direct gate turn-off. Both methods are investigated and experimental results provided.*



*It is concluded that, with appropriate circuit layout and component choice, the unavoidable stray inductance effects can be limited to manageable levels. The most severe effects are caused by the DC source inductance which is the most difficult to minimise. Others within the power circuit, if kept small, will have a marginal effect. Fast over-current protection is achievable.*

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## LIST OF PRINCIPAL SYMBOLS

$A - K$	=	<i>anode - cathode</i>
$BP$	=	<i>back - porch</i>
$C_s$	=	<i>snubber capacitor</i>
$D_s$	=	<i>snubber diode</i>
$di_G/dt$	=	<i>rate of rise of negative gate current</i>
$E_d$	=	<i>DC supply voltage</i>
$ESL$	=	<i>equivalent series inductance</i>
$ESR$	=	<i>equivalent series resistance</i>
$f$	=	<i>frequency of operation</i>
$h$	=	<i>integration step - length</i>
$i_{a1}$	=	<i>GTO A1 branch current</i>
$I_{A1}$	=	<i>GTO A1 anode current</i>
$i_{a2}$	=	<i>GTO A2 branch current</i>
$I_{A2}$	=	<i>GTO A2 anode current</i>
$i_{b1}$	=	<i>GTO B1 branch current</i>
$I_{B1}$	=	<i>GTO B1 anode current</i>
$i_{b2}$	=	<i>GTO B2 branch current</i>
$I_{B2}$	=	<i>GTO B2 anode current</i>
$i_{ca1}$	=	<i>A1 snubber capacitor current</i>
$i_{ca2}$	=	<i>A2 snubber capacitor current</i>
$i_{cb1}$	=	<i>B1 snubber capacitor current</i>
$i_{cb2}$	=	<i>B2 snubber capacitor current</i>
$i_f$	=	<i>instantaneous freewheeling current</i>
$I_f$	=	<i>peak freewheeling current</i>
$I_{GP}$	=	<i>peak negative gate current</i>
$I_H$	=	<i>holding current</i>
$i_l$	=	<i>instantaneous load current</i>
$I_l$	=	<i>peak load current</i>



$I_L$	=	<i>latching current</i>
$I_R$	=	<i>reverse current</i>
$I_{ra1}$	=	<i>A1 snubber diode reverse recovery current</i>
$I_{ra2}$	=	<i>A2 snubber diode reverse recovery current</i>
$I_{ra1pk}$	=	<i>A1 snubber diode peak reverse recovery current</i>
$I_{ra2pk}$	=	<i>A2 snubber diode peak reverse recovery current</i>
$I_{rb1}$	=	<i>B1 snubber diode reverse recovery current</i>
$I_{rb2}$	=	<i>B2 snubber diode reverse recovery current</i>
$I_{rb1pk}$	=	<i>B1 snubber diode peak reverse recovery current</i>
$I_{rb2pk}$	=	<i>B2 snubber diode peak reverse recovery current</i>
$I_{rp}$	=	<i>snubber diode peak reverse recovery current</i>
$i_s$	=	<i>instantaneous snubber current</i>
$I_s$	=	<i>peak snubber current</i>
$i_t$	=	<i>instantaneous tail current</i>
$I_t$	=	<i>peak tail current</i>
$i_T$	=	<i>instantaneous anode current</i>
$I_T$	=	<i>peak anode current</i>
$I_{TCM}$	=	<i>maximum repetitive controllable on - state current</i>
$I_{TCSM}$	=	<i>maximum non - repetitive controllable on - state current</i>
$I_{TSM}$	=	<i>maximum non - repetitive surge current</i>
$I_{OP}$	=	<i>initial - on pulse</i>
$L_d$	=	<i>supply inductance</i>
$L_g$	=	<i>gate circuit inductance</i>
$L_l$	=	<i>load inductance</i>
$L_s$	=	<i>snubber circuit inductance</i>
$NB$	=	<i>negative bias</i>
$p$	=	<i>differential operator d/dt</i>
$R$	=	<i>load resistance</i>
$R_s$	=	<i>snubber resistance</i>
$t_c$	=	<i>near constant current charging time</i>

$t_f$	= <sup>current</sup> GTO fall time
$t_{os}$	= oscillatory overshoot voltage time
$t_{rr}$	= snubber diode reverse recovery time
$t_s$	= GTO storage time
$t_t$	= tail current decay time
$t_{us}$	= voltage undershoot time
$v_{a1}$	= A1 instantaneous anode - cathode voltage
$v_{a2}$	= A2 instantaneous anode - cathode voltage
$v_{b1}$	= B1 instantaneous anode - cathode voltage
$v_{b2}$	= B2 instantaneous anode - cathode voltage
$v_c$	= instantaneous snubber capacitor voltage
$V_c$	= peak snubber capacitor voltage
$v_{ca1}$	= instantaneous A1 snubber capacitor voltage
$v_{ca2}$	= instantaneous A2 snubber capacitor voltage
$v_{cb1}$	= instantaneous B1 snubber capacitor voltage
$v_{cb2}$	= instantaneous B2 snubber capacitor voltage
$v_{co}$	= instantaneous snubber capacitor voltage during the anode current fall
$V_{co}$	= peak snubber capacitor accumulated voltage after the anode current fall
$v_{ds}$	= instantaneous forward recovery voltage of the snubber diode
$V_{ds}$	= peak forward recovery voltage of the snubber diode
$V_{g-k}$	= breakdown voltage of the GTO gate - cathode junction
$V_{GR}$	= gate reverse bias voltage
$v_l$	= instantaneous load voltage
$V_l$	= peak load voltage
$V_{NB}$	= gate negative bias voltage during GTO forward blocking state
$v_{os}$	= instantaneous oscillatory overshoot voltage
$V_{os}$	= peak oscillatory overshoot voltage
$V_{pk}$	= peak GTO voltage ( $E_d + V_{os}$ )
$v_{sp}$	= instantaneous spike voltage

$V_{sp}$  = *peak spike voltage*

$V_T$  = *GTO on - state voltage*

$v_{us}$  = *instantaneous undershoot voltage*

$V_{us}$  = *peak undershoot voltage*

$\delta$  = *GTO duty cycle*

$\omega$  = *angular frequency*

# CHAPTER 1

## INTRODUCTION

### 1.1 Background

*The gate turn-off thyristor (GTO) is a member of the diverse family of four layer (pnpn) power switching devices. The earliest four layer switches were silicon controlled rectifiers (SCRs) or thyristors, the former title coming from their function, and the latter by analogy with the gas-filled thyatron valve, which they largely replaced.*

*Thyristors are relatively simple devices to construct and to model mathematically, involving a top metallisation (cathode side) which has only one centre gate connection. Other techniques use interdigitation and an amplifying gate.*

*The main advantages of thyristors include their ruggedness (ability to withstand high surge voltages and currents), the small amount of gate power needed to turn them on and the lower conduction drop than the mercury valves that they replaced. The main disadvantage, along with the valves, lies in the lack of any effective means of turn-off, except by starving them of anode current for a specified time (about  $100\mu\text{S}$  [1]). Thus their use is mainly limited to phase-control applications, usually directly connected to the AC lines supply, where they can be naturally turned off (commutated) as the supply crosses zero.*

*An advance on the line-commutated thyristor is the family of fast, or inverter type thyristors. In these, the silicon crystal is usually doped with gold atoms. This reduces the life time of the charge plasma in the n-base of the thyristor, so that the time for which the thyristor must be starved of anode current to turn it off (turn-off time) is reduced to some tens of microseconds. It now becomes reasonable to turn off the thyristor using forced commutation employing auxiliary components to induce a current zero and reverse bias across the thyristor. The device may thus be used to switch power from a DC supply, or produce AC from DC (by inverter), or for DC voltage control (by chopper). Because of the still relatively long commutation times of these devices and the losses in the auxiliary circuits, the switching frequency is limited.*

*More recently has appeared a substantially greater improved device, the asymmetric thyristor (ASCR). The conventional thyristor, with two high-voltage blocking pn*



*junctions, can sustain high voltage in both directions. The ASCR trades off its reverse voltage blocking capability for something more useful in inverter and chopper circuits, a thinner piece of silicon for the same forward blocking voltage. The ASCR can therefore only be used in applications where there is no requirement for large reverse voltages. This saving in crystal thickness can be utilised in one of two ways. If the amount of gold doping is kept the same as in a fast turn-off thyristor, the commutation time remains of the order of tens of microseconds, but the on-state voltage drop is considerably reduced, giving a saving in on-state dissipation and a larger current surge rating. If however, the gold level is substantially increased, the on-state voltage drop is increased to the previous level, but the turn-off commutation time will be dramatically reduced to a few microseconds. This greatly eases the problem of turning off the ASCR as the energy required to be stored in the auxiliary commutation components is relatively small.*

*The ASCRs are capable of switching at tens of kilohertz and the device is becoming popular for pulse-width modulated (PWM) inverters with switching frequencies of several kilohertz.*

*Physicists and device designers, turning their attention to the family of four-layer devices, realised that the thyristor cannot be turned off from the gate because of the high internal loop gain of the pnp-npn transistor pair. If the regenerative loop gain could be carefully controlled, and if the gate series resistance could be made sufficiently small to all active parts of the chip, then it would be possible to construct a four-layer device which could be turned off from the gate. Because of the promise held out by this device to be a rugged, high voltage, high current power switch, yet economical in silicon content, much work was undertaken to develop a practical device. The answer proved to lie in several directions simultaneously, and has become possible with recent advances in semiconductor-device-fabrication technology.*

*The GTO switch was introduced commercially in the early 1960's [2] and has since continued to develop and advance in the power electronics field, especially during the 1970's with the introduction of the fine pattern processing technology of integrated circuits for LSI devices.*

*The uniqueness of the GTO lies in its self-extinction capability which eliminates the needs for a forced commutating circuit. The device properties, in many respects, lie between those of the thyristor and transistor, and it is now the favoured switching device in high power conversion applications.*

*The power handling capability of the GTO, which was regarded as being difficult to increase, has now been extended, and GTOs from 1200V, 20A types up to 4500V, 3000A types are presently available, with devices of about 4500V-5000V capable of interrupting currents of up to 4000A [2] soon to be realised.*

## **1.2 Objectives**

*The objectives of this research are:*

- a ) To provide an understanding of the physical behaviour and operating characteristics of the GTO thyristor.*
- b ) To assess the special problems of their implementation in DC choppers and DC-AC inverters.*
- c ) To investigate GTO over-voltage and over-current protection requirements and methods.*
- d ) To conduct an in-depth study of the effects of stray circuit inductances on the induced GTO over-voltages during all possible switching modes in the DC chopper and H-bridge inverter.*
- e ) To mathematically model the circuit behaviour allowing for lumped stray inductances and GTO snubber networks as current transfers between the active devices during the various possible switching patterns.*
- f ) To determine the relative importance of the various circuit path stray inductances in generating transient over-voltages, and the implications for circuit layout and component choice.*

## **1.3 Method of Approach**

*The approach adopted in this work has been to first investigate the principles of operation and characteristics of the GTO thyristor in general and one IR type 160PFT100 GTO in particular. This is presented in Chapter 2 which also evaluates the design and construction of a suitable gate drive circuit for the latter. Recommendations for the snubber circuit design are presented, and experimental measurements provided.*



*Chapter 3 deals with the mathematical analysis of the transient behaviour of the GTO thyristor and its snubber at turn-off in a conventional DC chopper circuit with resistive and resistive-inductive loads. Results are predicted using Laplace analysis and computer based numerical techniques, and compared with experimental results.*

*The investigation is then extended in Chapters 4 and 5 to an H-bridge employing GTOs capable of controlling 200A as the main switching elements. Chapter 4 is concerned with the mathematical models of the H-bridge operating in the quasi-square mode, whereas Chapter 5 assesses those for a pulse-width modulated output voltage. Allowance is made for the practical switching effects of diode reverse recovery and mismatch of device switching times.*

*Comprehensive consideration is given to the GTO over-current protection. Detection and current interruption systems that provide suitable protection are covered in Chapter 6. Again supporting practical results from designed and constructed systems are presented.*

*Chapter 7 gives the overall conclusions together with suggestions for further work.*

## **CHAPTER 2**

### **CHARACTERISTICS AND OPERATION OF THE GTO THYRISTOR**

#### **2.1 Introduction**

*The gate turn-off (GTO) thyristor is one of the most versatile switching devices yet developed, having ideal advantages; high blocking voltage, high peak and surge current capabilities and high power gain. It incorporates the advantages of both the conventional thyristor and the high-power bipolar transistor, and its turn-on and turn-off can be achieved by changing over only the polarity of the gate current. The negative gate current required for turn-off is only a fraction of the anode current lasting only for a few microseconds at a voltage no greater than the gate-cathode reverse breakdown voltage.*

*This chapter describes the characteristics and operation of the GTO thyristor and presents the characteristics of the International Rectifier type 160PFT100 GTO rated at 160A average, 1kV and having a 600A turn-off capability. In particular, it shows how these devices should be applied for safe operation.*

#### **2.2 Comparison Between the GTO and Conventional Thyristor**

*The argument for using GTO thyristors are overwhelming:*

- a) Self turn-off is provided by reversely biasing the gate, thus eliminating the need for the external commutation circuit, for applications in DC fed circuits where natural commutation is not possible;*
- b) A reduction in cost, weight, volume and acoustic and electromagnetic noise results;*
- c) Faster turn-off results, permitting the use of higher switching frequencies;*

*These benefits are achieved at the expense of a more complex GTO gate drive circuit. However, the cost and size of this is very small compared with the cost and size of the forced commutation components of the conventional thyristor.*

#### **2.3 Comparison Between the GTO Thyristor and the Bipolar Transistor**

*The GTO possesses significant advantages over the bipolar transistor, although for applications in the lower current and voltage ranges, the transistor is still favoured.*

*The GTO has the following advantages:*

- a) Higher blocking voltage and high ratio of peak controllable current to average current;
- b) Higher continuous current ratings;
- c) Higher surge current capability;
- d) The power consumed to drive the GTO is lower, a high gate drive throughout conduction not being necessary;

## 2.4 GTO Basic Principle of Operation

The cell structure of the GTO thyristor, being a four layer pnpn device, is basically similar to that of the conventional thyristor. The operation may be explained in terms of the two-transistor model of the thyristor.

### 2.4.1 Two-transistor model

The two transistor model is shown in Figure 2.1. The turn-on is initiated by emission of electrons across junction J3 into the npn transistor base when the gate-cathode junction is positively biased. This effectively turns on the npn transistor layer of the thyristor. These are attracted across the depletion layer of blocking junction J2, inducing a corresponding hole emission across J1.

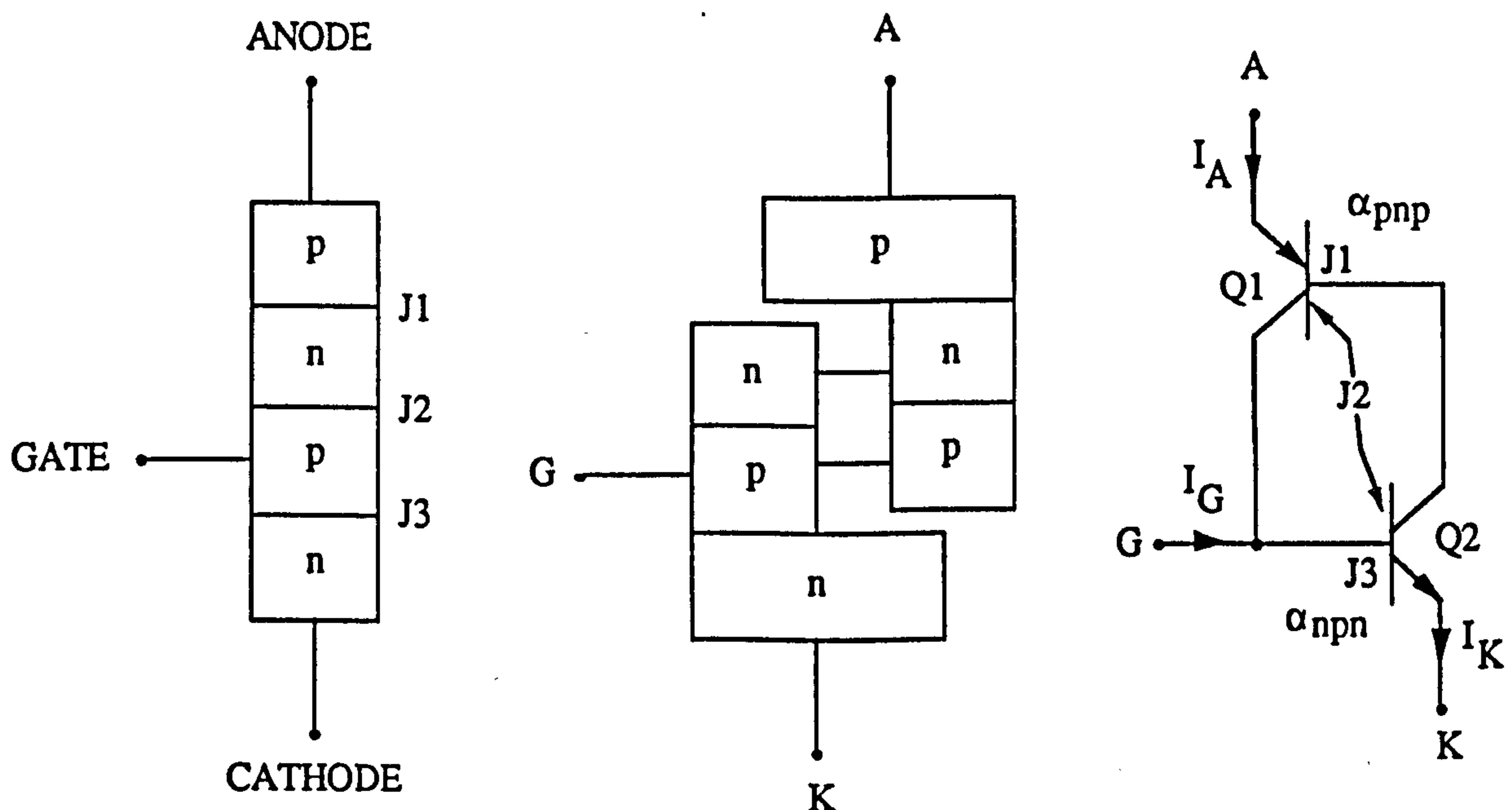


Figure 2.1 Two-transistor model of a thyristor

A regenerative arrangement therefore occurs in which the collector current of one



transistor supplies the base drive for the other. Latching of the thyristor occurs when both transistors saturate; the thyristor then conducts irrespective of the gate signal. The condition for turn-on is [3]:

$$\alpha_{npn} + \alpha_{pnp} > 1 \quad (2.1)$$

where  $\alpha_{npn}$  and  $\alpha_{pnp}$  are respectively the npn and pnp transistors common base current gains

Turn-off is obtained by extracting sufficient charge from the gate region to interrupt the positive feedback loop between the transistor sections of the device causing the loop gain to fall to a point where the regenerative action ceases.

#### 2.4.2 Turn-off gain

With reference to Figure 2.1, to sustain the npn transistor on, the base current required is  $(1 - \alpha_{npn})I_K$ , which is provided by the pnp transistor. The GTO turns off if:

$$\alpha_{pnp} I_A + I_G < (1 - \alpha_{npn})I_K \quad (2.2)$$

where  $(\alpha_{pnp} I_A + I_G)$  is the npn transistor actual base current; this yields (Appendix IV)

$$\frac{I_T}{I_G} = \frac{\alpha_{npn}}{(\alpha_{npn} + \alpha_{pnp} - 1)} \quad (2.3)$$

This ratio is the GTO thyristor turn-off gain. The equation implies that in order to obtain a high turn-off gain, the  $\alpha_{npn}$  should be large whereas  $\alpha_{pnp}$  should be small. This is incompatible with other requirements, as shown later, and a compromise is then essential.

#### 2.4.3 Maximum controllable on-state current

During the turn-off process, the p-base material present in the path between the gate terminal and the preceding plasma front possesses significant resistance ( $R_B$ ). The gate current flowing in this resistance will therefore produce a voltage drop in the p-base.

*This voltage drop may drive the gate-cathode (n-emitter/p-base) junction, being reversed biased, into reverse avalanche (breakdown) as the current flow increases. However, a limit to the amount of this gate current prior to the junction break-down is given by [3] [4]:*

$$I_G = \frac{4V_{GK}}{R_B} \quad (2.4)$$

*and*

$$R_B \text{ (the p-base resistance)} = \frac{\rho S}{W_p L} \quad (2.5)$$

*where*       $V_{GK}$  *is the break-down voltage of the gate-cathode junction*  
                *$\rho$  is the p-base resistivity*  
                *$S$  is the cathode (emitter) width*  
                *$L$  is the cathode (emitter) length*  
                *$W_p$  is the p-base width*

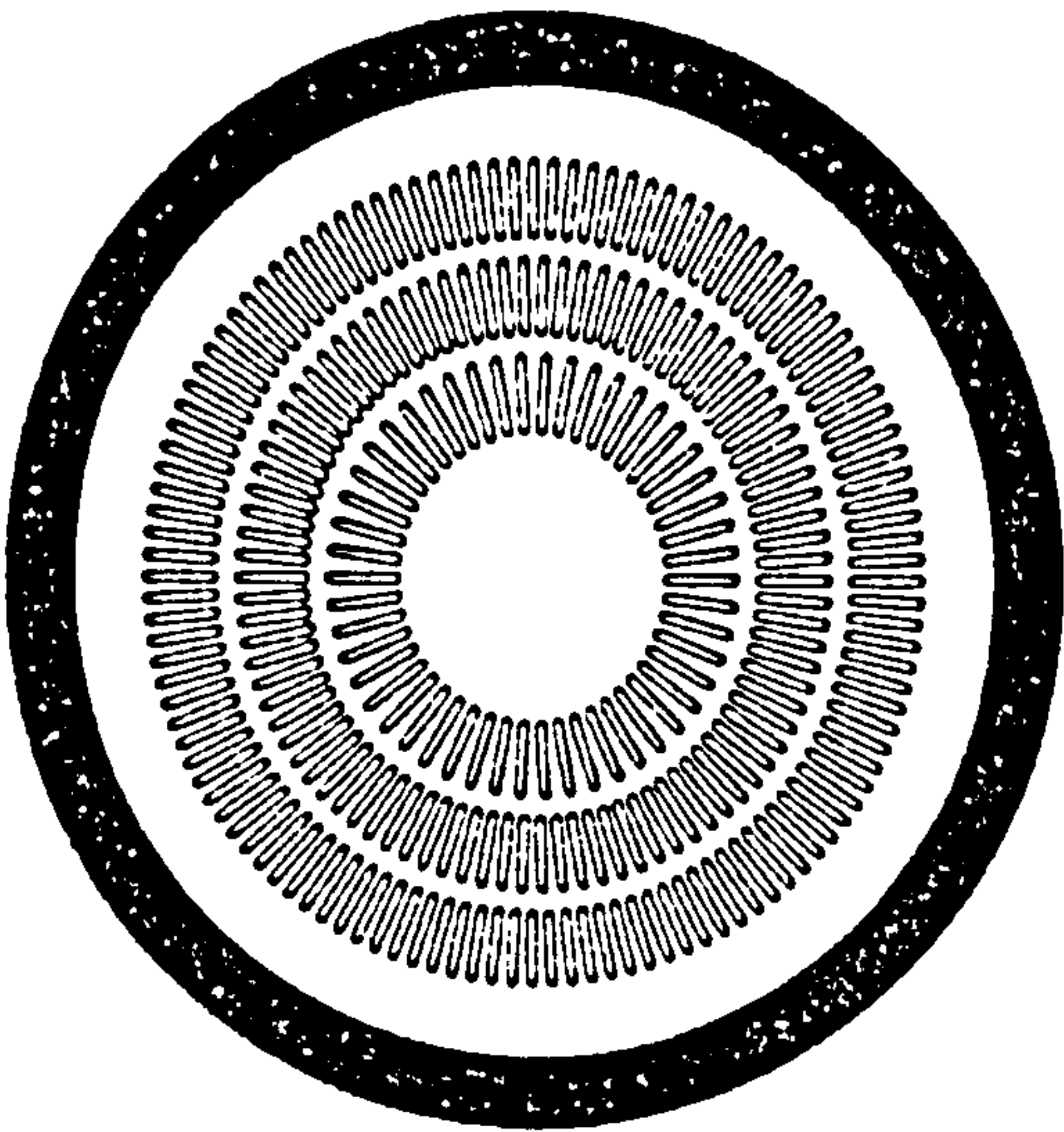
*The maximum current which can be drawn from the GTO gate is therefore a function of  $R_B$  and  $V_{GK}$ . The maximum anode current which may be controlled can then be indicated by combining equations 2.4 and IV.5 (Appendix IV), as follows;*

$$I_{TCM} < - \frac{4V_{GK}}{R_B} \cdot \frac{\alpha_{npn}}{(\alpha_{npn} + \alpha_{pnp} - 1)} \quad (2.6)$$

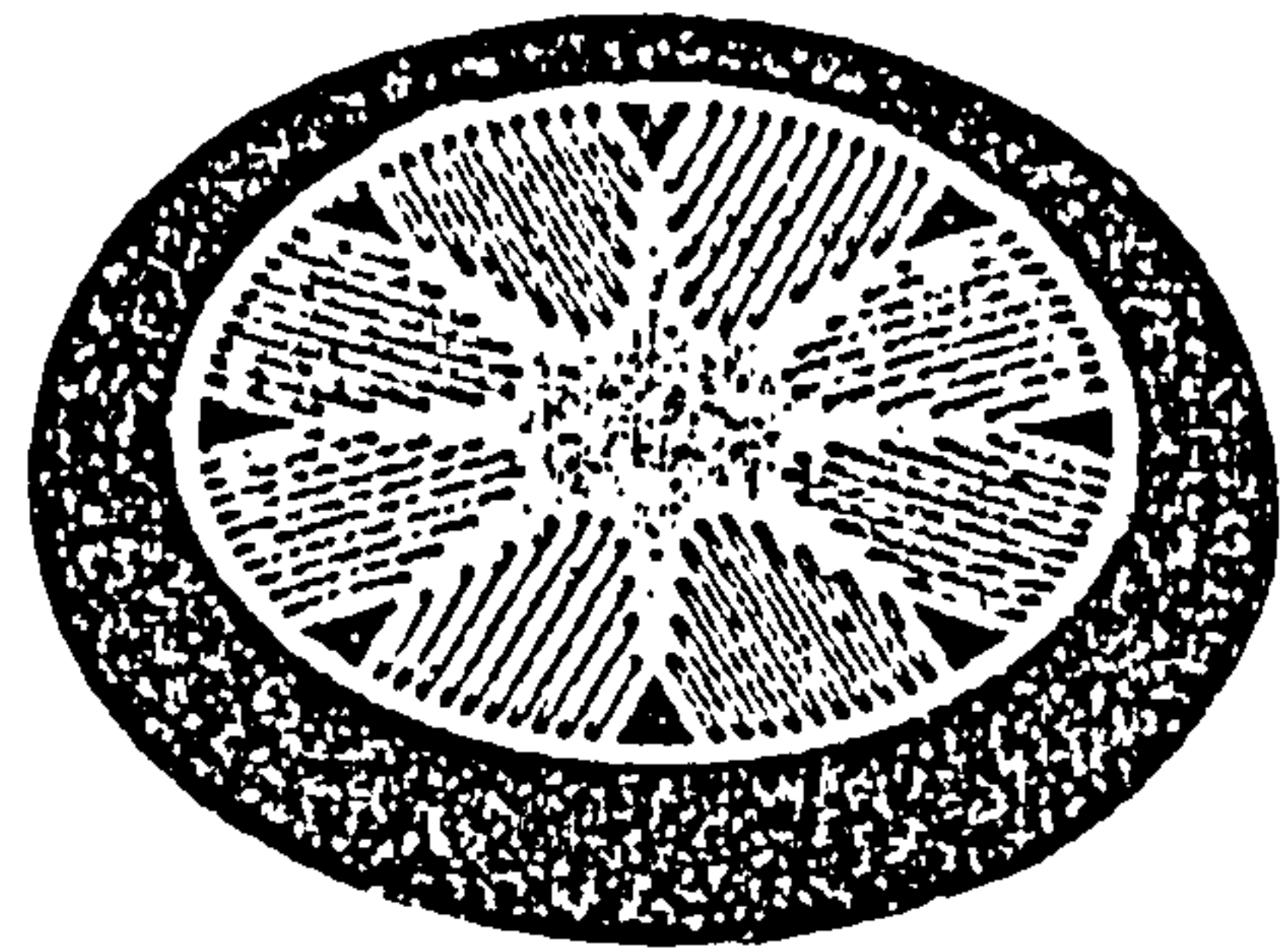
*The requirements of low p-base resistance and high gate-cathode breakdown voltage are conflicting. If a high junction breakdown voltage is achieved by lightly doping the p-base, the lateral resistance will be high. Furthermore, if a wide p-base is considered,  $R_B$  will be low but the  $\alpha_{npn}$ , hence the turn-off gain, will be low.*

*This conflict is overcome by the interdigitation of the gate and cathode regions; the cathode emitter area is subdivided into many elongated thin strips that are fully encompassed by a gate region, Figure 2.2. The main advantage of this arrangement is that the lowest value of p-base resistance  $R_B$  is obtained.*





(a) 2500V, 1800A GTO type



(b) 1200V, 600A 160PFT100 GTO

Figure 2.2 Gate-cathode structure of the GTO thyristor

#### 2.4.4 GTO cathode structure

*The cathode (n-emitter) pattern geometry is one of the important design parameters for achieving a high controllable on-state current capability. Referring to Figure 2.2, the length of the cathode finger is controlled by the voltage drop in the gate metallization that occurs at turn-off and the achievement of an acceptable value of current density at on-state and turn-off, whereas the width is limited by the maximum controllable on-state current and the on and off state voltages. It is desirable to reduce the width in a manner which makes it possible to increase the average forward current combined with an acceptable value of off-state voltage.*

*The gate region is etched below the level of the cathode element, which in fact is an island, as shown diagrammatically in Figure 2.3. This mesa construction permits a good voltage isolation between the cathode and gate regions, whilst a reliable electrical and thermal contact may be made to the cathode islands using a compression-bond technique. The high power GTO therefore effectively consists of a number of smaller GTOs connected in parallel, all integrated into a single piece of silicon. The disadvantages of this construction are that the amount of gate current required for turn-on becomes high, and due to the small ratio of the cathode to total device areas, the device thermal resistance is increased.*



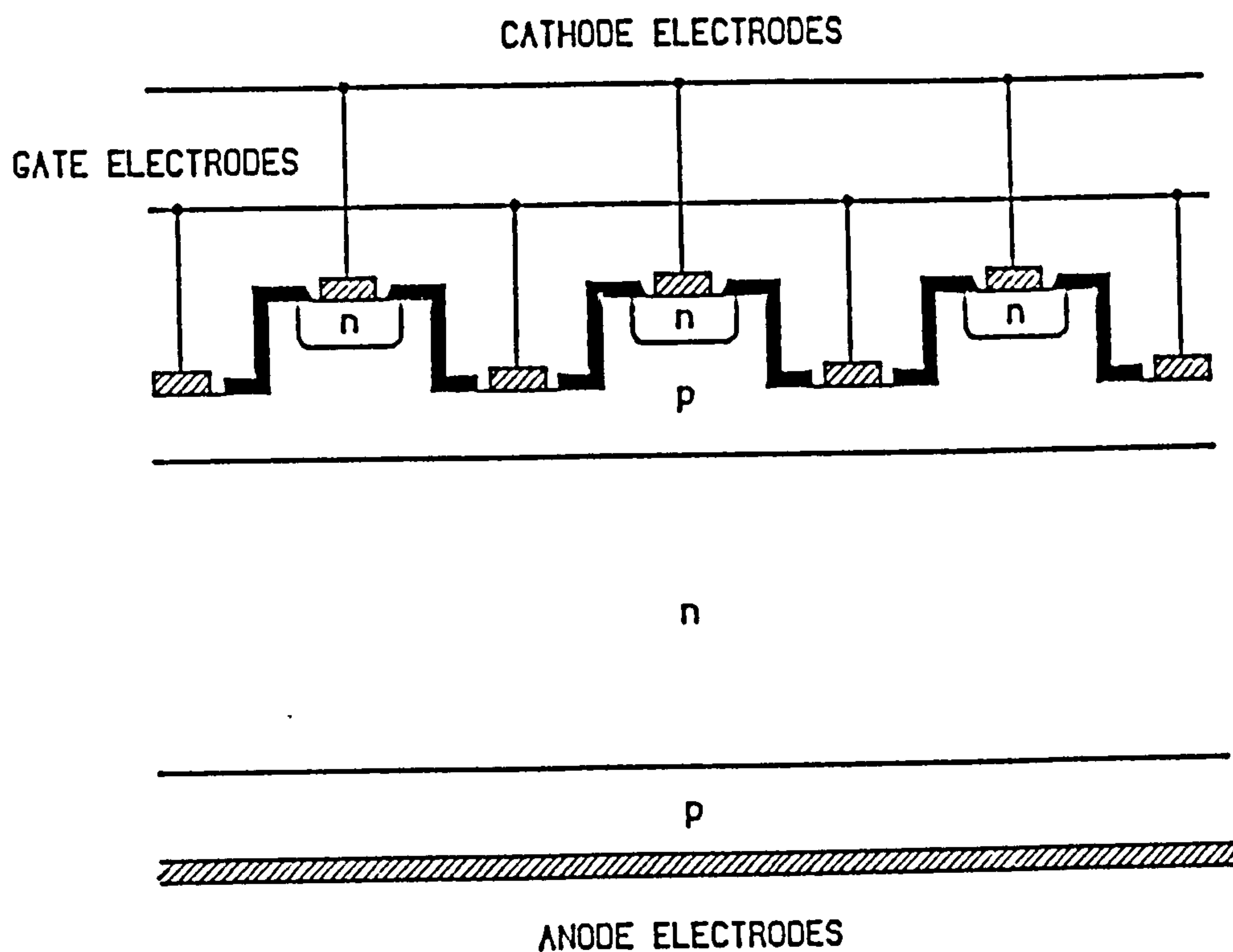


Figure 2.3 Cross-section of the gate-cathode junction assembly

#### 2.4.5 Plasma pinching

At turn-off, the GTO gate is reversed biased with respect to the cathode; the extraction of holes from the p-base results in a pinching of the hole-electron plasma that carries the current between the anode and cathode regions. This is illustrated schematically in Figure 2.4.

Turn-off is initiated at the edge of the cathode region next to the gate which introduces reverse bias as holes flowing in the p-base from the anode to the cathode element are swept out from the gate. As more charge carriers are extracted, which increases the resistance  $R_B$ , the conducting channel is constricted further until only the very centre region of the cathode finger remains conducting and forward biased. This causes a current crowding effect as the anode current during this period, the GTO storage time (sub-section 2.6.2, (b) (ii)), remaining unchanged. Hole extraction continues until the positive feedback loop between the npn and pnp transistor sections is interrupted. The anode current rapidly collapses, the J3 junction centre then reverse biases and the GTO regains the forward voltage blocking ability at junction J2.

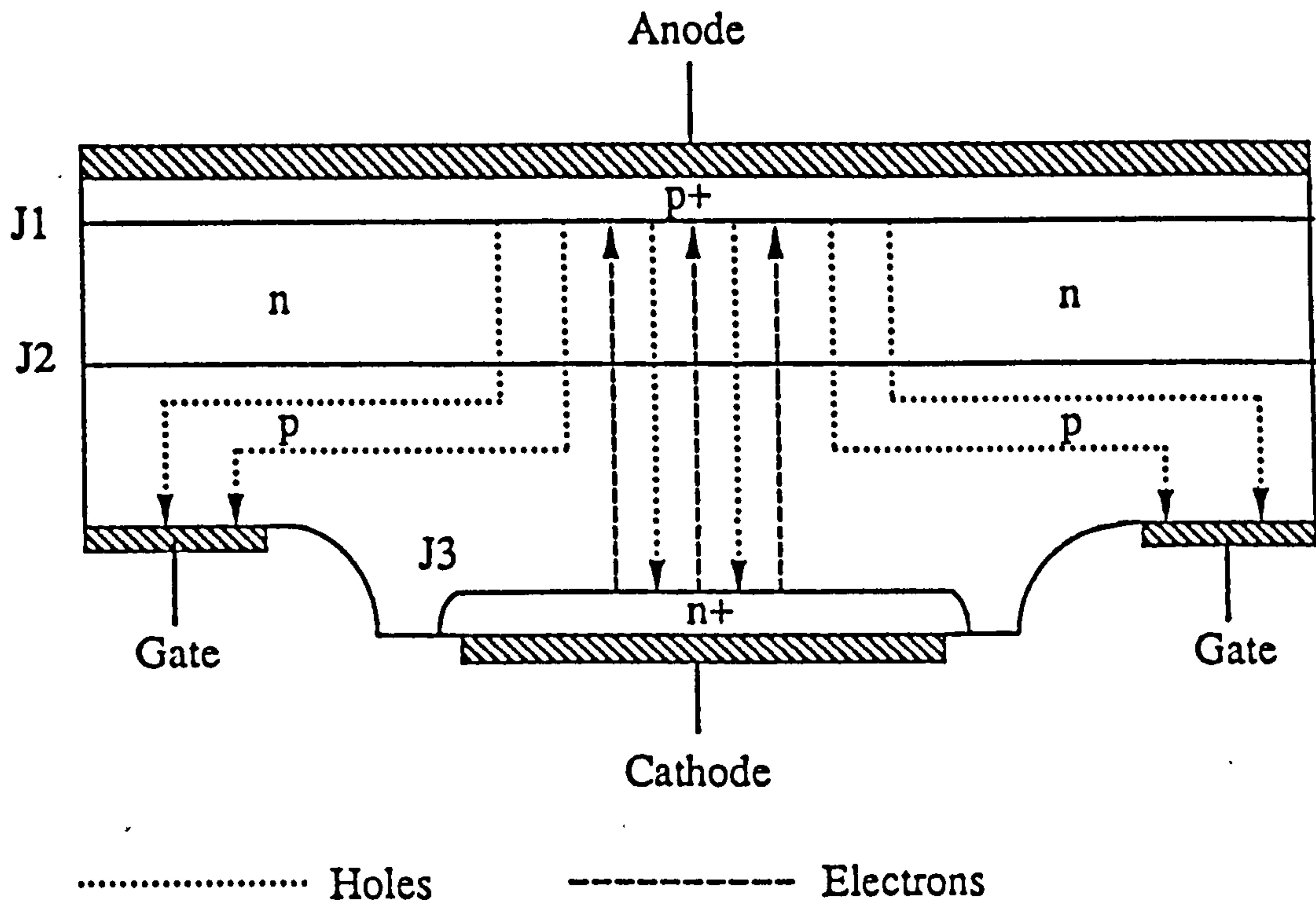


Figure 2.4 Plasma pinching on turn-off

## 2.5 Minority Carrier Lifetime Control

High turn-off gain, hence controllable current, may be achieved by a low value of the common-base current gain in the pnp section of the GTO. This value can be expressed by [4]:

$$\alpha_{pnp} = \alpha_T \gamma \quad (2.7)$$

where  $\alpha_T$  is the transport factor, defined as the ratio of the hole current from the p-emitter to the total emitter current  
 $\gamma$  is the emitter injection efficiency, defined as the ratio of the hole current reaching the collector to the total emitted hole current into the base.

Therefore reduced  $\alpha_{pnp}$  may be obtained by an increase in the width of the n-base with

low minority-carrier lifetime to reduce  $\alpha_T$ , or a reduction in the thickness of the p-emitter to decrease  $\gamma$ .

A common feature of the GTO which naturally lowers  $\alpha_{pnp}$ , is the wide n-base to give the device its forward blocking capability.

Also, it is important to provide some mechanism to remove or eliminate the charge trapped in the n-base region after turn-off. However, the value of  $\alpha_{pnp}$  must be kept low. Two common techniques are adopted, these being:

**a ) Shorted-anode emitter technique**

Figure 2.5(b) shows the basic structure with anode emitter short circuits. This contains resistive shunts of n-regions bypassing the p-emitter to create a discharge path for the charge trapped in the n-base after turn-off. This approach reduces  $\alpha_{pnp}$  as it lowers the p-emitter anode injection efficiency  $\gamma$ .

The anode shorted technique has several merits such as low on-state losses, higher surge current capability and low leakage current. The adverse effects are; the more complex fabrication process and the very low reverse voltage blocking capability (typically 15V-20V), which is limited to that of the gate-cathode junction J3, J1 being shorted.

It is found that values of anode short resistance  $R_a$  corresponds to the n-material sheet resistance of less than  $10\Omega.\text{cm}^2$  [3] will produce a good turn-off characteristics.

**b ) Heavy metal doping technique**

This is illustrated in Figure 2.5(a). The n-base region is doped with a metal such as gold. This produces recombination centres, and hence reduces minority carrier lifetime. Also,  $\alpha_{pnp}$  is controlled by the reduction in  $\alpha_T$ .

With this technique, in addition to the ease of the fabrication process, the device reverse voltage blocking capability is enhanced. The GTO can, in fact, have symmetrical forward and reverse voltage withstand. As demonstrated in Figure 2.5(a), junction J1 is complete and blocks the reverse voltage. However, this approach results in a high on-state voltage drop and high leakage current.



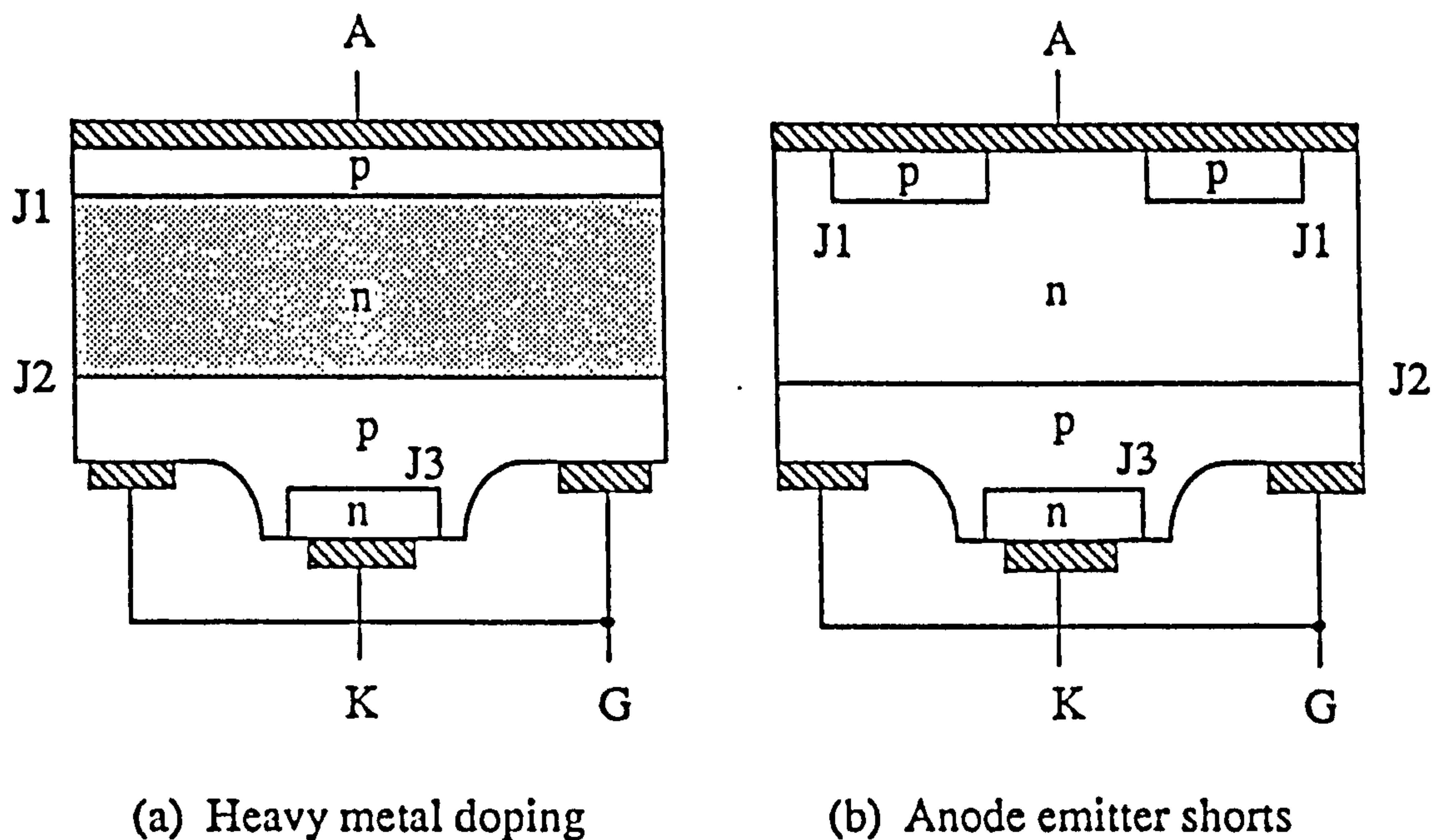


Figure 2.5 Carrier lifetime reduction techniques

## 2.6 GTO Thyristor Characteristics

The GTO voltage-current characteristics which indicates the two stable operating regions of the device is shown in Figure 2.6. These regions correspond to the forward on and off states of the GTO.

With no gate current, only a small leakage current flows between the anode and cathode. However, if the anode voltage exceeds the break-over value, the GTO then switches into forward conduction. With normal operation, the device turns on once the anode current has exceeded the latching level  $I_L$ , but may switch off if the current is reduced below the holding current value in the absence of gate drive.

With negative gate current applied for turn-off, the GTO reverts from the forward on-state region to the forward off-state region.

### 2.6.1 Static characteristics

#### a) Forward blocking capability ( $V_{DRM}$ )

Forward break-over by sufficient anode voltage is likely to occur if the anode-cathode

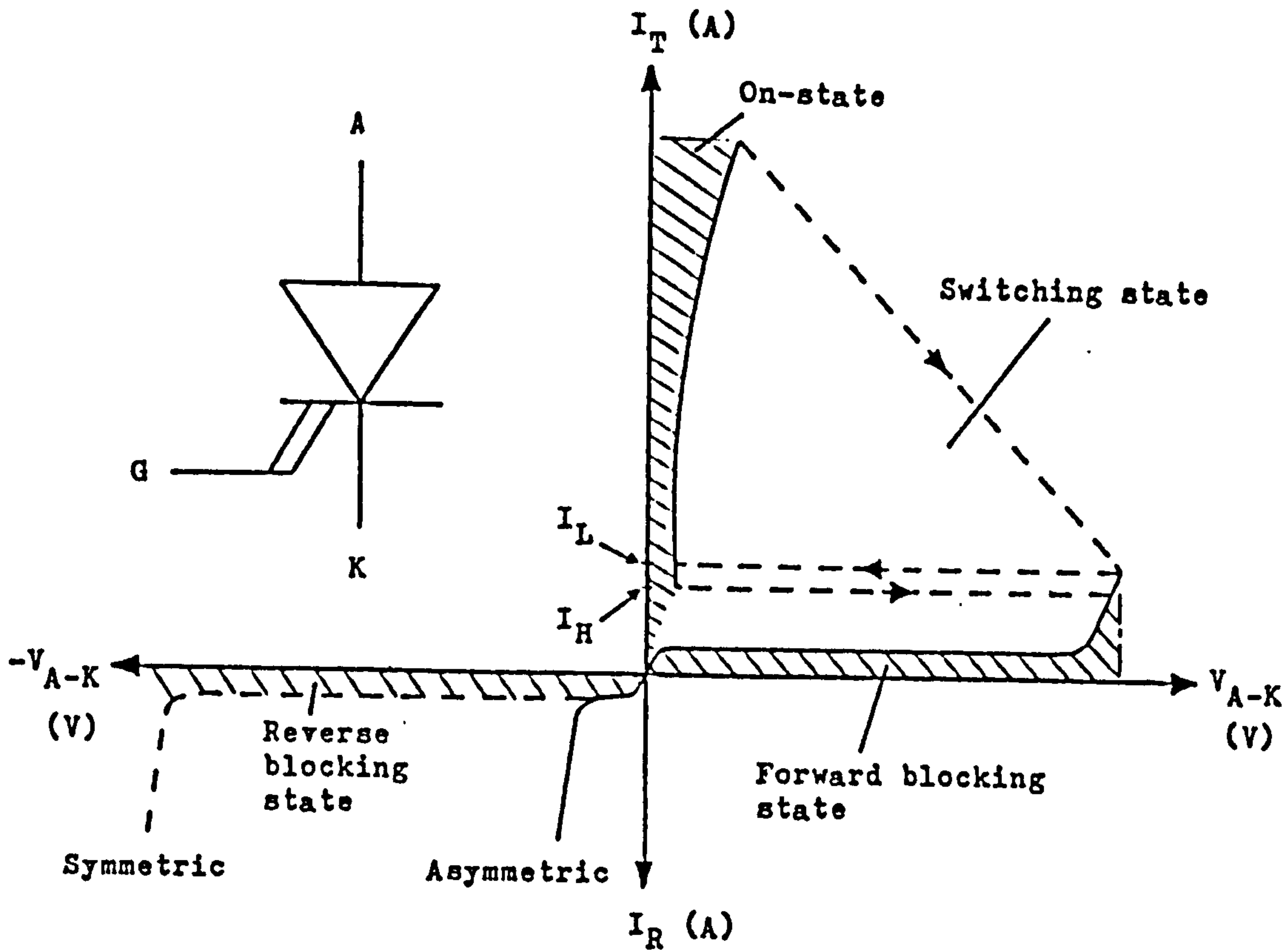


Figure 2.6 Symbol and voltage-current characteristics of the GTO thyristor

leakage current becomes high enough to initiate the regenerative action to turn-on. The forward blocking capability of the GTO thyristor therefore, may be enhanced if this leakage current is diverted out at the gate. This is achieved effectively by reverse biasing the gate-cathode junction during the GTO forward blocking period. The gate reverse bias voltage  $V_{GR}$  may be;

$$0 < V_{GR} < V_{g-k}$$

where  $V_{g-k}$  is the gate-cathode break-down voltage (approximately 20V)

Turn-on of the GTO thyristor by forward break-over may result in the destruction of the device. The full load current may be concentrated in a few cathode islands that are

the first to conduct, the others then being prevented from turn-on as the GTO voltage is immediately reduced by the turn-on of the former.

**b) Reverse blocking capability ( $V_{RRM}$ )**

The construction of the GTO thyristor determines if the device can block high reverse voltage as explained in section 2.5. A high reverse blocking capability can be an advantage for the GTO in some application such as current fed inverters and controlled rectifiers.

**c) Latching current ( $I_L$ )**

Due to the cathode structure, the GTO thyristor may be considered to consist of many small GTOs in parallel. The latching of one cathode finger will reduce the whole device voltage and the GTO may be said to be turned on, although it only carries a small portion of the load current. However, the agreed definition for the latching current is the minimum current required to latch all the cathode islands of the GTO thyristor into conduction.

Moreover, when the GTO anode current is less than  $I_L$ , the device behaviour will be similar to that of the transistor.

**d) Holding current ( $I_H$ )**

This is the minimum anode current required to maintain the GTO in the conduction state irrespective of the gate current. Some of the cathode islands, if the GTO anode current falls to a value below the holding current, may be unlatched. These will remain in the off state should the anode current increase again, and as current cannot spread throughout the device, results in high current concentration in those islands remaining in conduction. Therefore, a possibility of permanent damage to the device arises. However, this problem can be avoided when, during the GTO conduction period, a continuous gate current (back-porch) is maintained to prevent individual cathode fingers from unlatching.

**e) On-state voltage drop ( $V_{TM}$ )**

The forward voltage drop of the GTO thyristor will be influenced by the junction temperature and by the presence of the back-porch current at the gate. Without continuous gate drive, the voltage drop is higher at low values of anode current, as



demonstrated in Figure 2.7 [6]. This is caused by the unlatching of some of the cathode regions with the current density increasing in those already turned on.

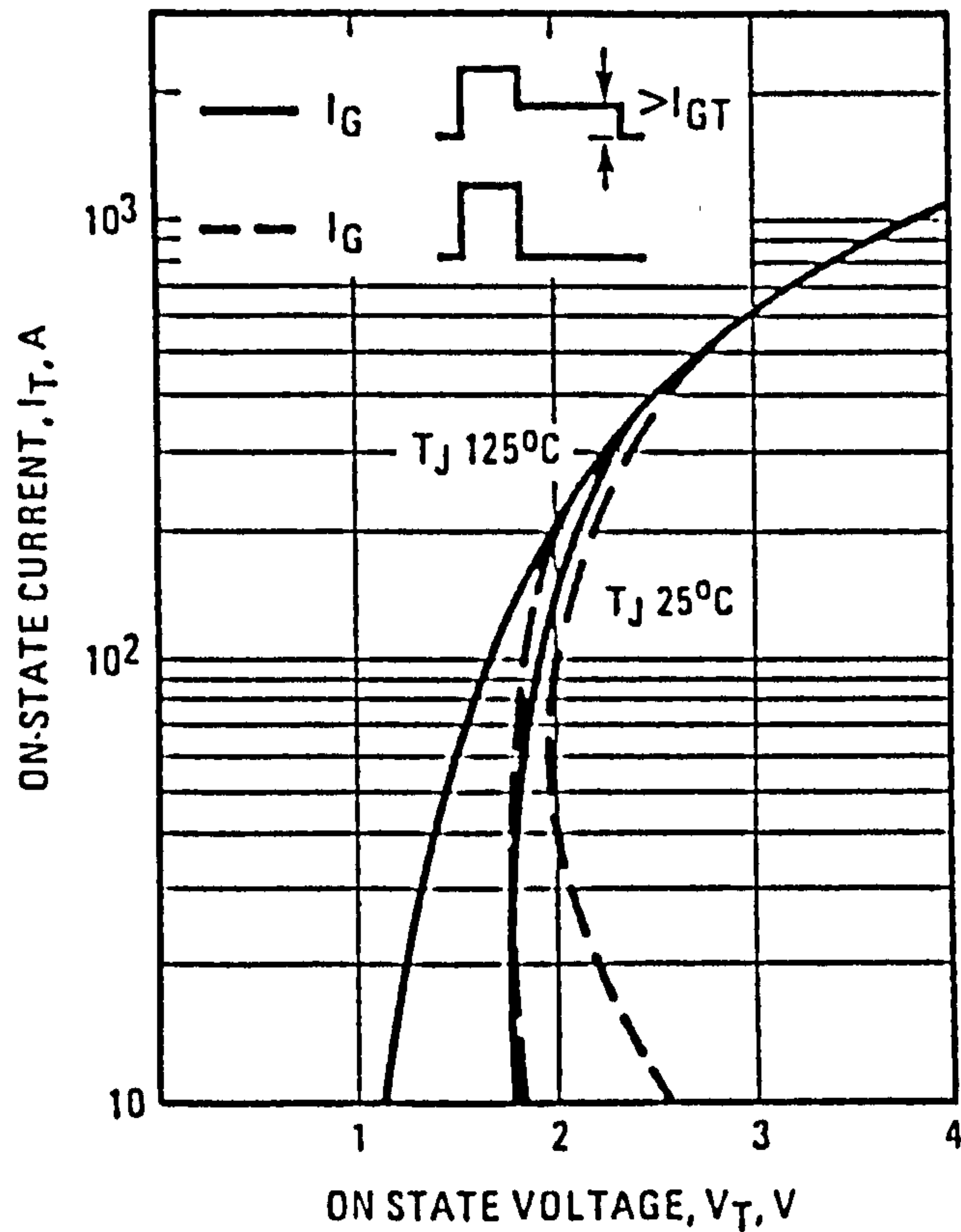


Figure 2.7 On-state voltage as a function of on-state current for the 160PFT100 GTO [6]

## 2.6.2 Dynamic characteristics

### a) Turn-on

The typical voltage and current waveforms of the GTO thyristor at turn-on and turn-off are represented schematically in Figure 2.8.

#### 1) Initial-on gate current pulse ( $I_{GM}$ )

The GTO turn-on is initiated by the application of a current pulse to the gate. This, due to the highly interdigitated structure of the GTO gate-cathode, should be of a large value with short rise time to ensure a rapid turn-on of all the partial areas of the GTO pellet structure and a good current sharing between the cathode fingers. The initial-on pulse is sustained for a duration  $t_{FG}$  which is long enough to ensure the complete turn-on.

The minimum value of  $t_{FG}$  is at least twice the gate delay time  $t_d$  [5]. The parameters

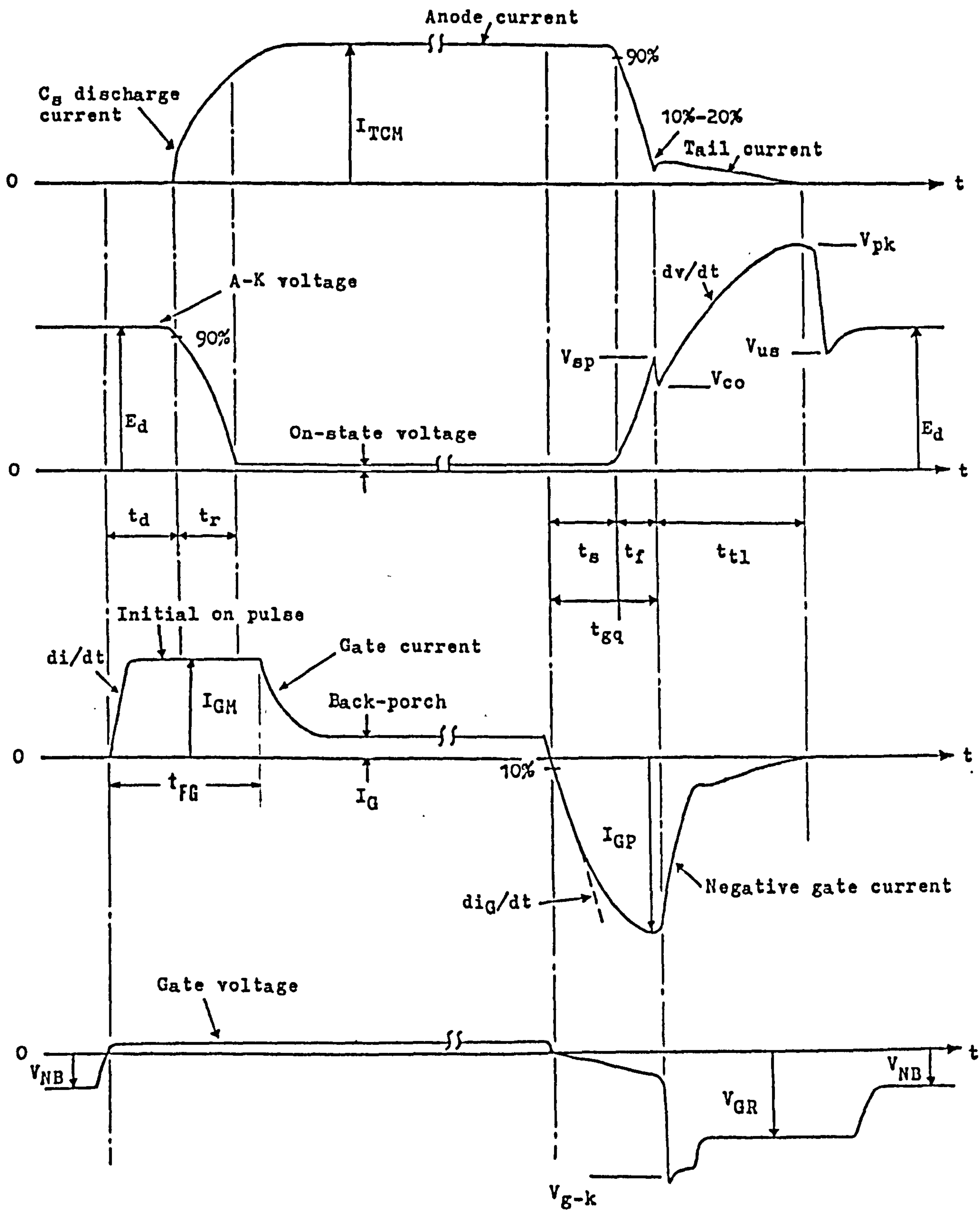


Figure 2.8 Switching condition for the GTO thyristor

$I_{GM}$ ,  $di/dt$  and  $t_{FG}$  (Figure 2.8) may have to be varied slightly depending on the environment temperature.

### *ii) Back-porch current ( $I_G$ )*

After the initial gate current pulse, the current level may be reduced to a much lower value (approximately 10%-20% of  $I_{GM}$ , depending on the environment temperature), which is maintained for the whole duration of the GTO forward conduction state. This, commonly known as the back-porch current, is required to ensure that all the cathode islands remain latched whatever subsequent variations might occur in the device anode current.

### *iii) Rate of rise of anode current( $di_T/dt$ )*

With the conventional thyristor, the relatively low rate of plasma spreading during initial turn-on limits the initial conducting capability of the device and necessitates a  $di/dt$  limitation of the anode current. With the GTO thyristor, owing to its fine interdigitated structure, turn-on is very rapid, assuming adequate gate drive. Conduction is initiated at multiple places across the gate-cathode area, and the plasma spreading across each cathode element is extremely fast. Therefore initial conduction occurs over a large proportion of the cathode area and hence restriction on  $di/dt$  of anode current by external protection is not usually required and is adequately controlled by the device self and the external stray inductances.

### *iv) Minimum on-state time ( $t_{on}$ )*

To avoid endangering the GTO, a minimum on-state duration  $t_{on}$  should be maintained before turn-off is attempted to ensure that all the cathode regions are in full conduction. Otherwise, at turn-off the poor load current sharing between the cathode islands results in very high current densities in those elements which are turned on, and the rise in their temperature gives the risk of their failure to turn off and the complete destruction of the device.

Furthermore, the time required for the complete discharge of the snubber capacitor into the GTO at turn-on, must be incorporated in the minimum on-time limit. If this is incomplete, the rise of the anode-cathode blocking voltage will be unrestrained until it is greater than that of the capacitor. This increases the GTO turn-off losses and the possibility of GTO re-triggering and damage due to the excessive initial  $dv/dt$ . The effect is illustrated in Figure 2.9.



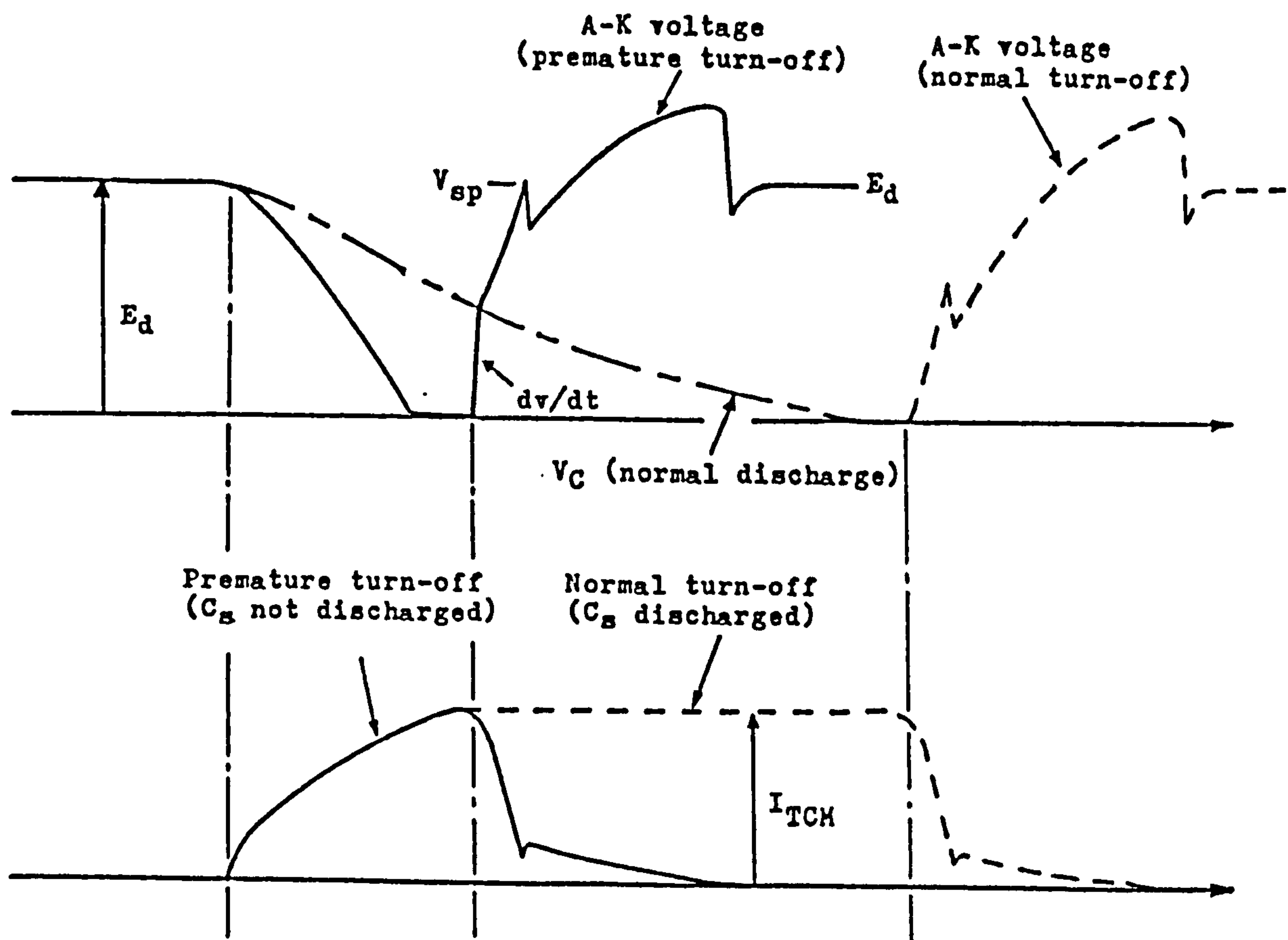


Figure 2.9 Waveforms at GTO turn-off when the snubber capacitor is not fully discharged during turn-on time

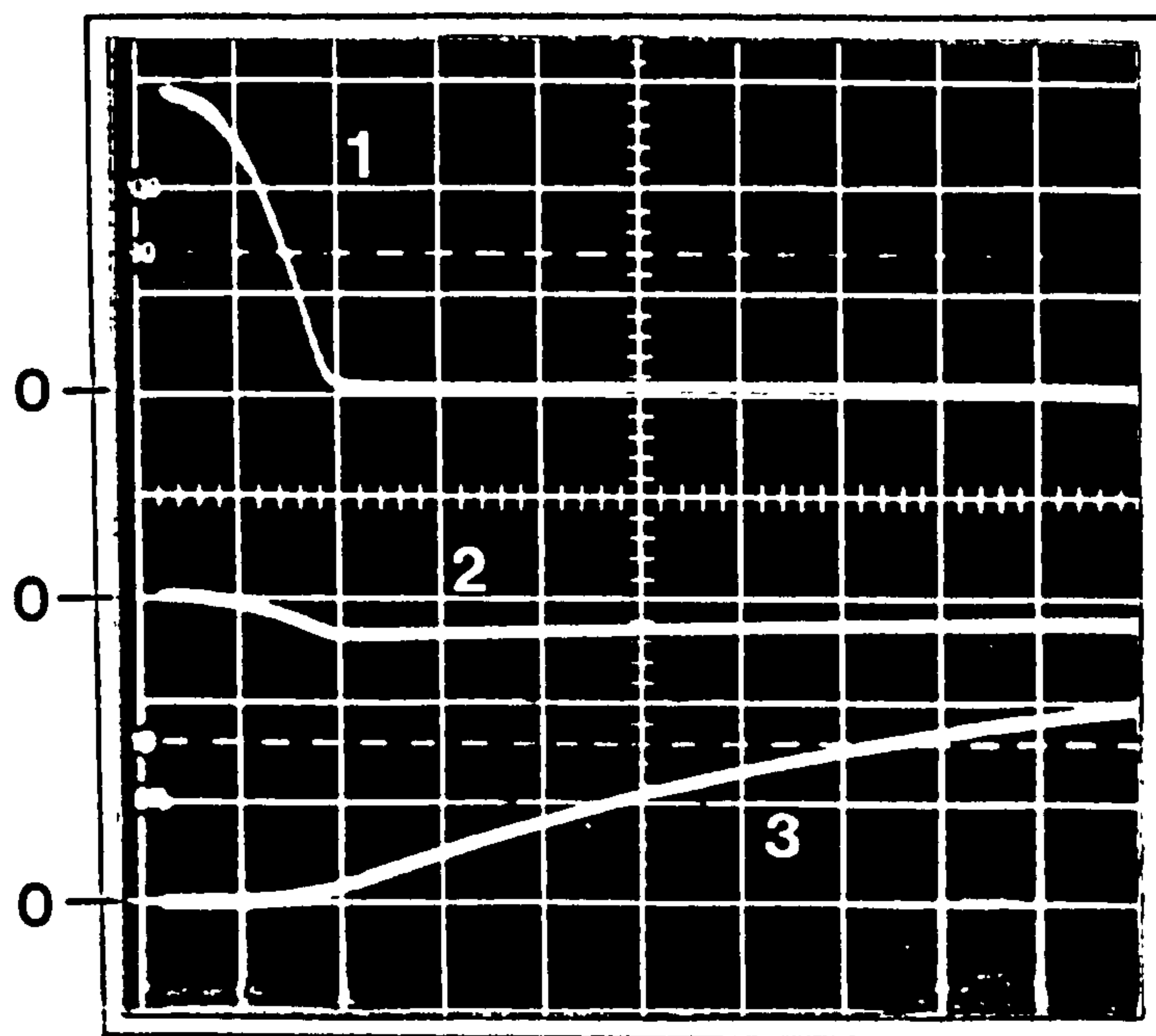
#### v ) GTO turn-on losses

Maximum GTO turn-on losses occur with resistive loads and negligible anode current  $di/dt$  limitation from stray inductances. It is then good practice to include a small inductor to lengthen the current rise time as illustrated in Figure 2.10. This may be accompanied by its own freewheeling diode, otherwise turn-off losses are increased due to increased stored energy producing a higher overshoot of the snubber capacitor voltage, as explained in the next section.

The turn-on losses will include those incurred by the snubber circuit discharge current.

#### b ) Turn-off

The typical waveforms at the GTO turn-off are included in Figure 2.8 with experimental waveforms in the oscillograms of Figure 2.11.



(1) A-K Voltage (100V/div.)  
 (2) Snubber Discharge Current (50A/div.)  
 (3) Anode Current (load + snubber) (200A/div.)

Time Scale : 2 $\mu$ S/div.

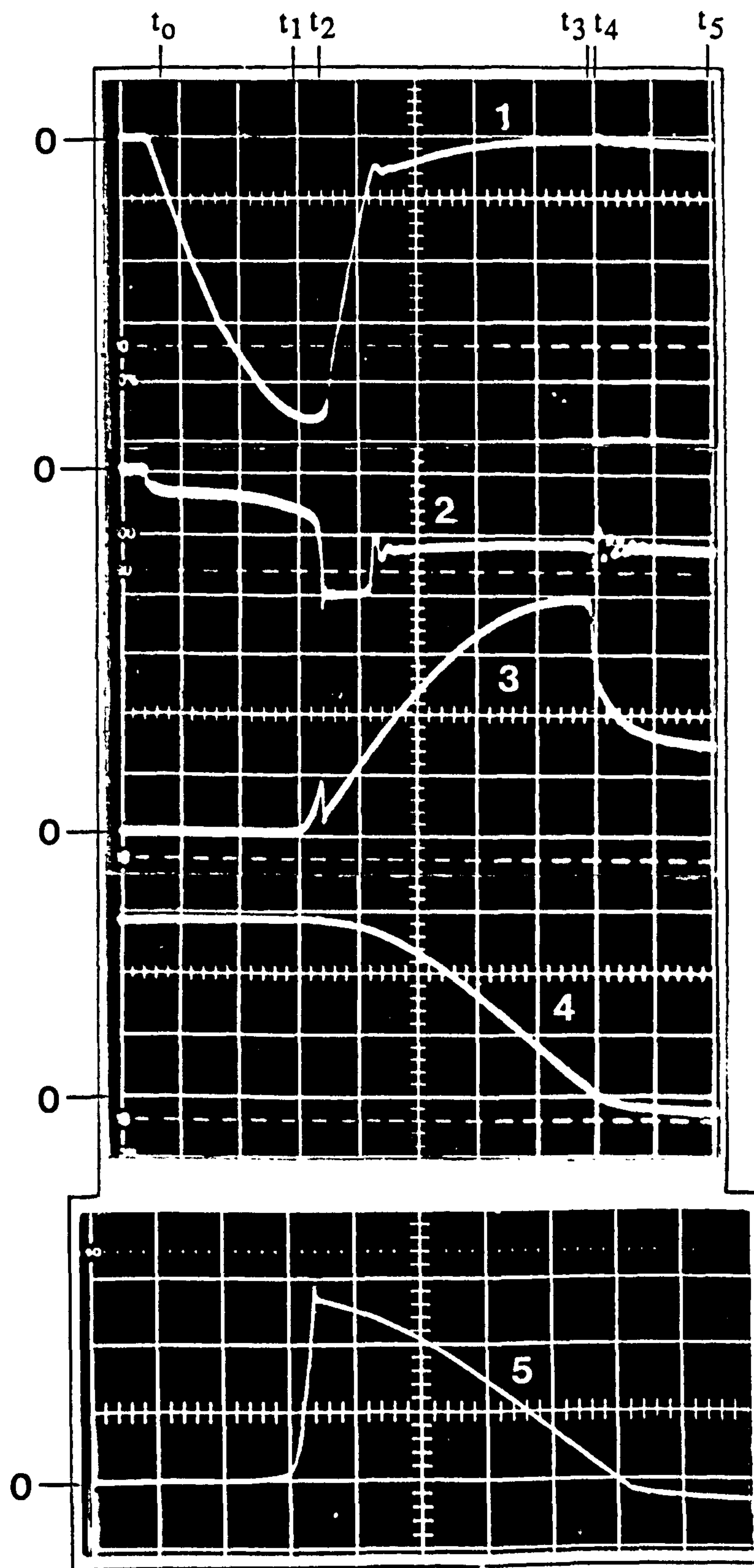
Figure 2.10 Anode voltage and current during GTO turn-on (160PFT100)

### 1) turn-off time intervals

Referring to Figure 2.11, the turn-off phases are:

$t_0 - t_1$ : At  $t_0$ , the turn-off of the GTO is initiated by the application of a negative voltage pulse to the gate, the magnitude of which is limited by the break-down voltage of the gate-cathode junction. The extracted negative current then rises at a rate dictated effectively by the gate circuit inductance and the value of the negative voltage source applied. The gate voltage develops a small negative potential caused by the increase of the p-base resistance as the plasma-pinching action continuous.

This phase, known as the storage time  $t_s$ , during which no variations occur to the anode voltage and current, ends at  $t_1$  where the anode current has fallen to 90% of its peak value.



- |                                  |             |
|----------------------------------|-------------|
| (1) Gate Current                 | (20A/div.)  |
| (2) Gate-Cathode Voltage         | (10V/div.)  |
| (3) A-K Voltage                  | (200V/div.) |
| (4) Load Current (anode+snubber) | (200A/div.) |
| (5) Snubber Current              | (200A/div.) |

Time Scale : 2 $\mu$ S/div.

Figure 2.11 Typical turn-off performance of the 160PFT100 GTO thyristor



$t_1 - t_2$ : This is the anode current fall time  $t_f$ . By time  $t_1$ , sufficient current is extracted from the GTO gate to interrupt the regenerative action of the pnp and npn sections of the device. The anode current fall is extremely fast, coinciding with the peak gate current, and the anode current diverts correspondingly quickly into the snubber circuit resulting in the parasitic inductance of the GTO to snubber loop (Figure 2.12), inducing a voltage spike (Figures 2.8 and 2.11) which must not exceed about 1/3 of the rated blocking voltage [7], but is best kept to a minimum. The voltage spike generated due to the finite turn-on time of the snubber diode will also contribute to the former spike.

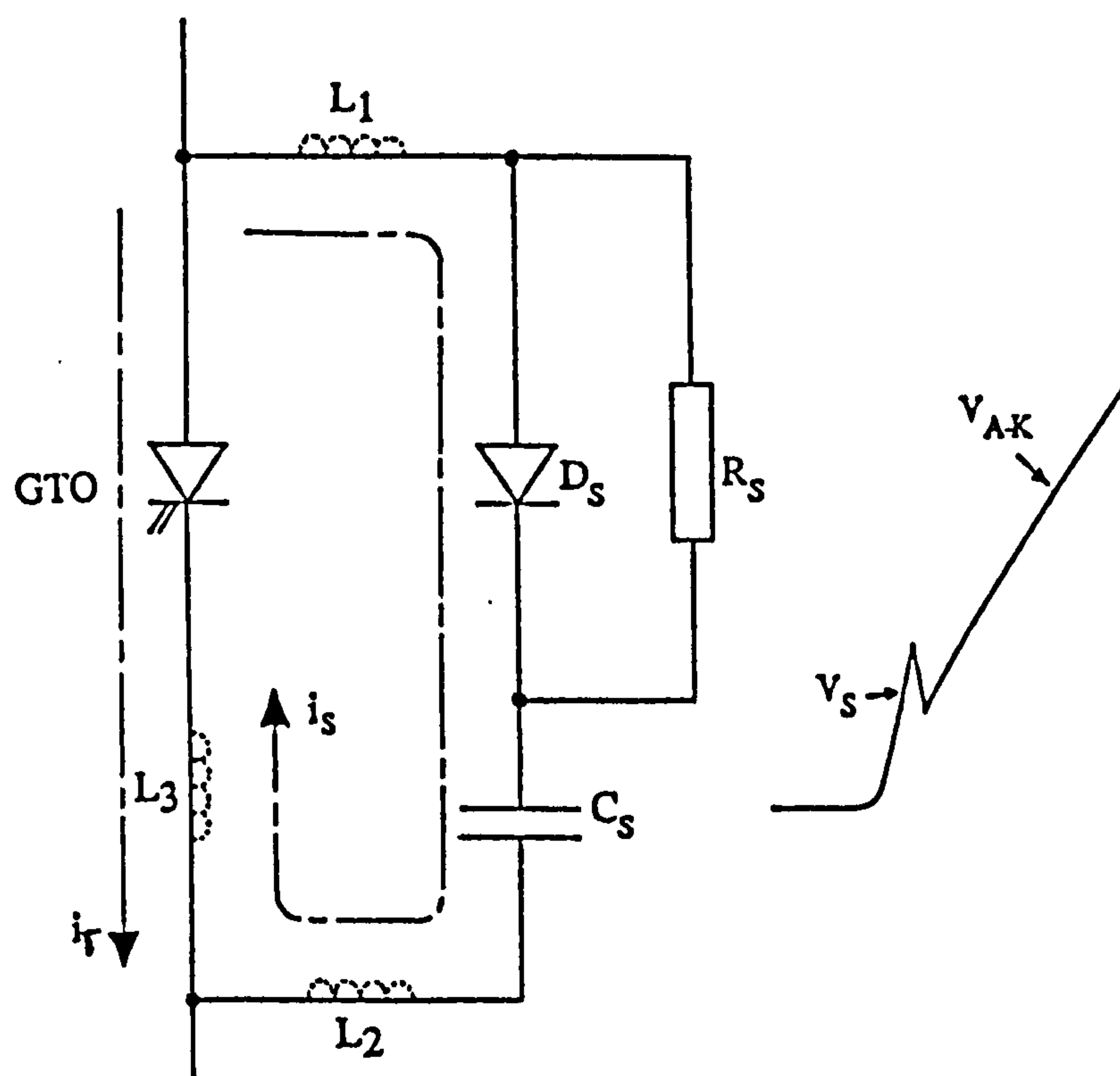


Figure 2.12 Effect of Parasitic inductances in the snubber circuit  
 $L_1$ ,  $L_2$  and  $L_3$  are stray inductances

At the end of anode current fall,  $t_2$ , the voltage spike collapses to the accumulated voltage across the snubber capacitor, with the GTO now virtually blocking current.

The reversed biased gate-cathode junction is driven into avalanche breakdown, due to

the rapid fall of the gate current in the gate circuit inductance  $L_g$ .

$t_2 - t_3$ : At  $t_2$ , the anode current has fallen to a small tail current level. This tail, the peak value of which is usually 10%-20% of the anode current, is due to the remaining residual charge trapped in the n-base section in the vicinity of the anode p-emitter. In general, the value of the tail current depends on the constructional technique of the GTO. Devices with emitter-shorts have lower tail current. The tail current decays to zero during this phase.

Voltage builds up across the GTO thyristor as the diverted anode current charges the snubber capacitor during its fall to zero, Figure 2.11. Correspondingly, the GTO voltage rises further with a quarter cycle of oscillation to a peak overshoot, when the stored inductive energy in the anode circuit discharges into the snubber capacitor.

Following the dissipation of the stored energy in the gate circuit inductances into the gate-cathode, the gate-cathode voltage falls to the voltage of the applied negative source.

At the end of the anode current fall, the gate current decays with a rate controlled by the gate circuit inductance  $L_g$ , the gate-cathode junction break-down voltage  $V_{g-k}$  and the applied negative gate voltage  $V_{GR}$  [12], i.e.

$$\frac{di_G}{dt} = \frac{(V_{g-k} - V_{GR})}{L_g} \quad (2.8)$$

The gate and anode tail currents will equalize following the recovery of the gate-cathode junction.

$t_3 - t_4$ : The oscillatory snubber capacitor current now continues into the negative (discharge) half-cycle as the snubber diode undergoes reverse recovery. The capacitor voltage then slightly reduces.

$t_4 - t_5$ : Upon snubber diode reverse recovery, the capacitor current transfers to the snubber resistor fairly rapidly at a rate determined by the reverse recovery snap-off of the diode. This is seen as a sudden voltage collapse across the GTO (Figures 2.8 and 2.11) and possible undershoot of the blocking voltage, Figures 2.8 and 2.28, due to the sudden negative IR drop. The subsequent  $dv/dt$  as the device voltage rises following the



*undershoot must be considered; this could be dangerous as it is not limited by the capacitor and may lead to a spurious turn-on.*

*The undesirable perturbation of the gate voltage and therefore current (Figure 2.11, traces 2 and 1) are due to the anode-gate and gate-cathode stray capacitances coupling the sudden voltage drop into the gate-cathode junction. Thereafter, the anode circuit L-C oscillation is damped by the snubber resistor, and the GTO voltage adjusts to the supply voltage value  $E_d$ .*

### *ii) Turn-off time ( $t_{gq}$ )*

*The turn-off time of the GTO, which comprises the storage and fall times ( $t_s + t_f$ ), is a function of the interrupted anode current, the junction temperature and the rate of rise of the negative gate current  $di_G/dt$  at turn-off. The effect of the different values of anode current on the turn-off time is demonstrated in Figure 2.13(a).*

*Shorter storage and (slightly) fall times are produced by increasing  $di_G/dt$  rates. As the total charge extracted remains constant [10], fast extraction of sufficient charge  $Q$  required to interrupt the regenerative action of the GTO will lead to higher peak negative gate current (Figure 2.13(b)), resulting in lower turn-off gain. Moreover, with faster turn-off times, the charge trapped in the n-base after turn-off is higher, leading to a larger, but not longer, tail current and hence higher losses during the tail time.*

*The effects of varying  $di_G/dt$  on turn-off time and gain are illustrated in Figure 2.13(c).*

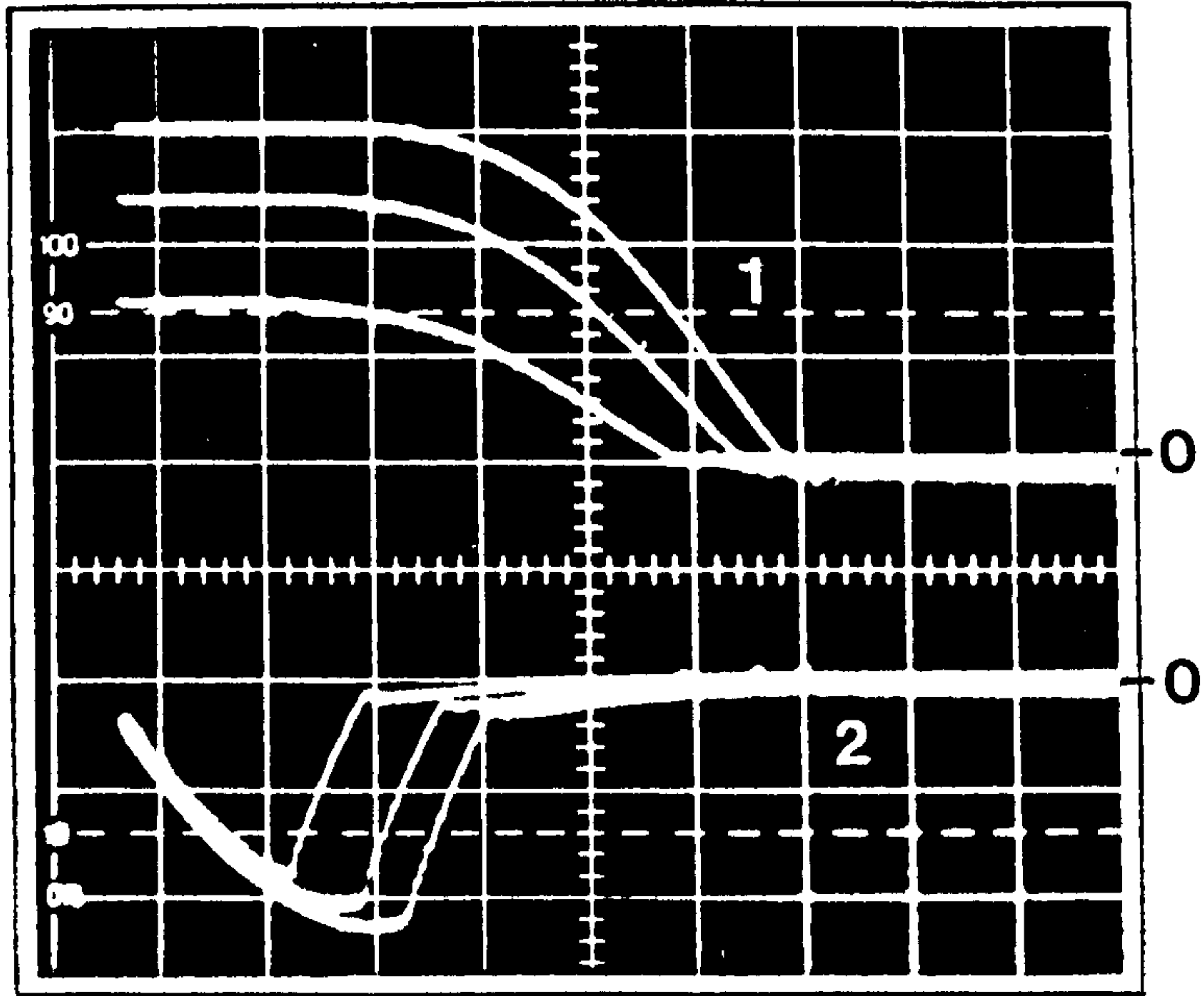
### *iii) Negative gate bias (NB) following turn-off*

*The applied turn-off negative voltage pulse  $V_{GR}$  may be reduced after the tail time to a value down to about 2V, to enhance the  $dv/dt$  and forward blocking voltage withstand capabilities of the GTO thyristor.*

### *iv) Critical turn-off*

*Reliable operation of the GTO depends greatly on providing safe switching conditions by adequate snubbing and gate drive. Referring to equation 2.8, it can be seen that a value of the negative applied gate voltage  $V_{GR}$  near to that of the gate-cathode break-down voltage*

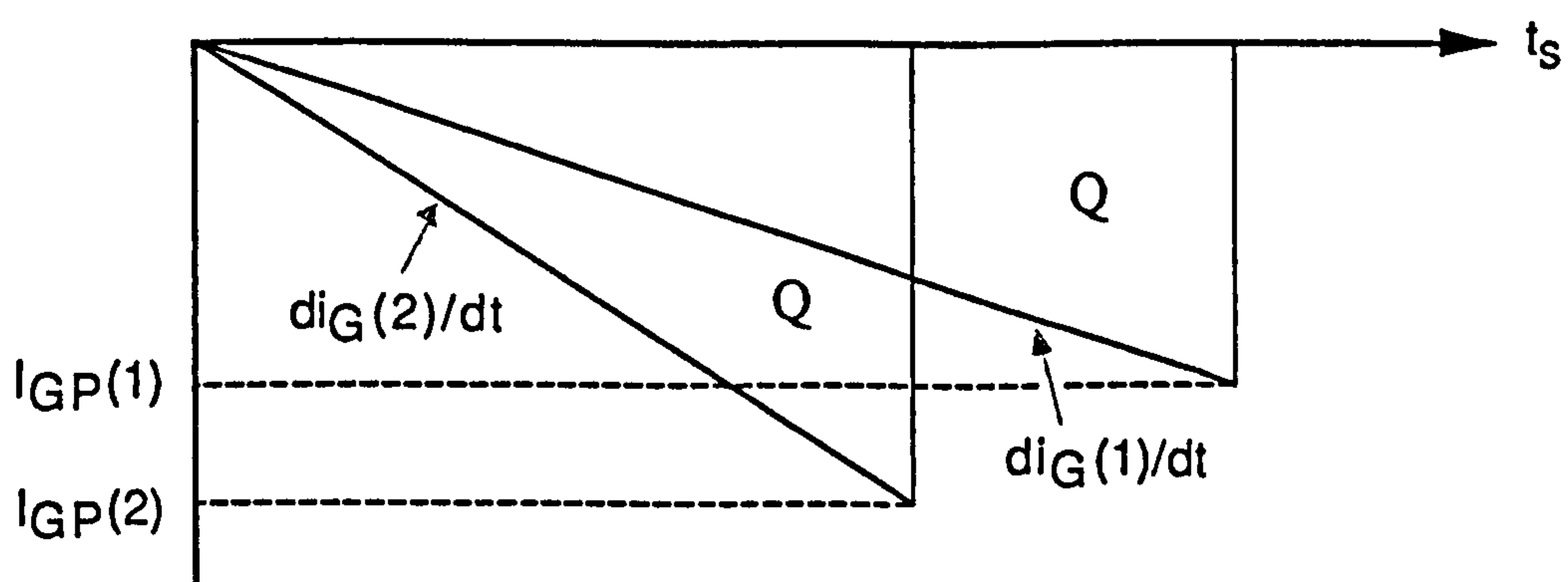




(a) Dependency of storage time ( $t_s$ ) on the values of anode current  $I_T$  (160PFT100)

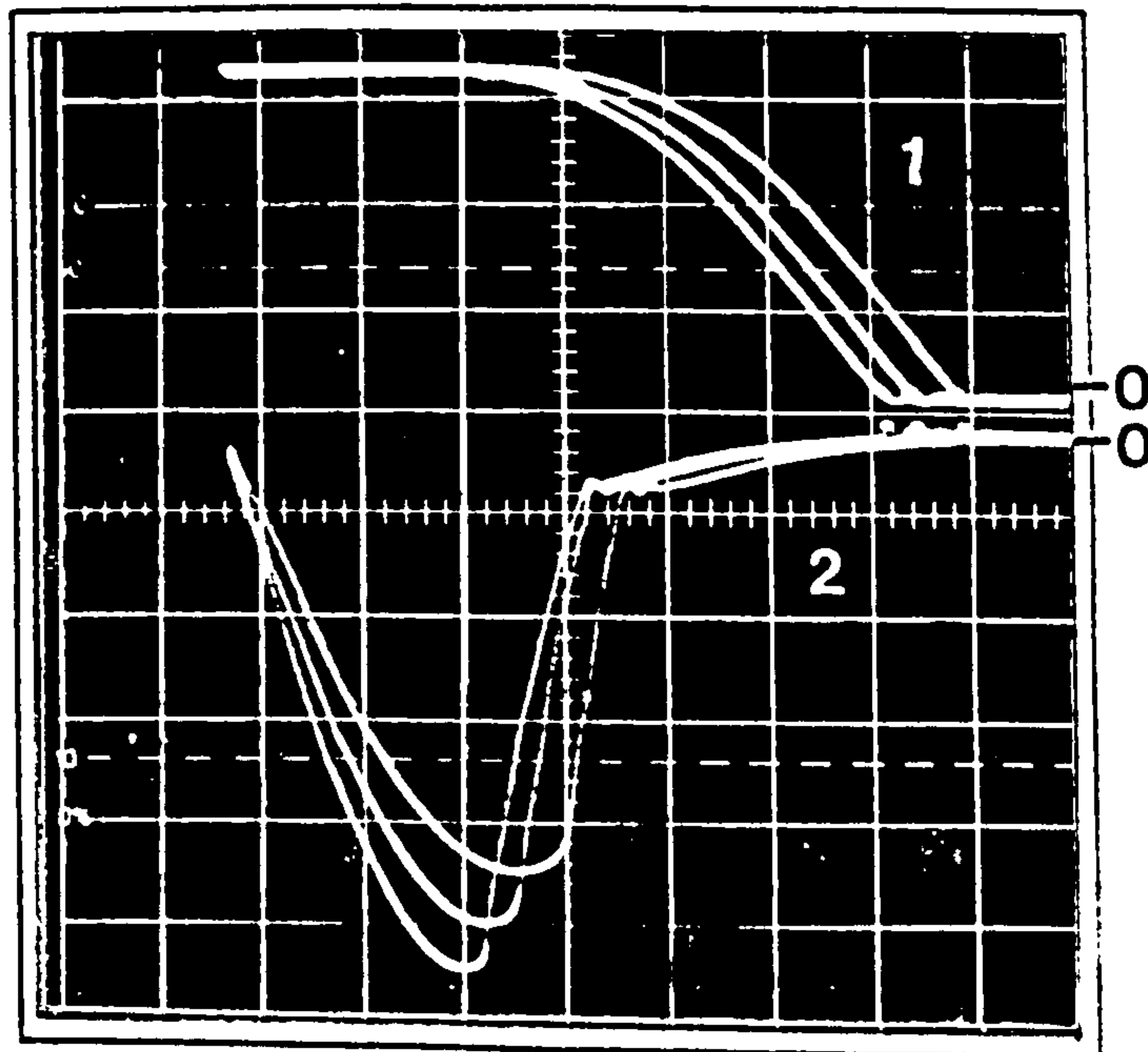
(1) Load Current (anode + snubber) (200A/div.)  
 (2) Gate Current (50A/div.)

Time Scale :  $2\mu\text{S}/\text{div.}$



(b) Effect of  $di_G/dt$  on storage time  $t_s$

Figure 2.13 Effect of varying  $di_G/dt$  at turn-off



(c) Dependency of storage time ( $t_s$ ) and turn-off gain on  $di_G/dt$  (160PFT100)

(1) Load Current (anode + snubber) (200A/div.)  
 (2) Gate Current (20A/div.)

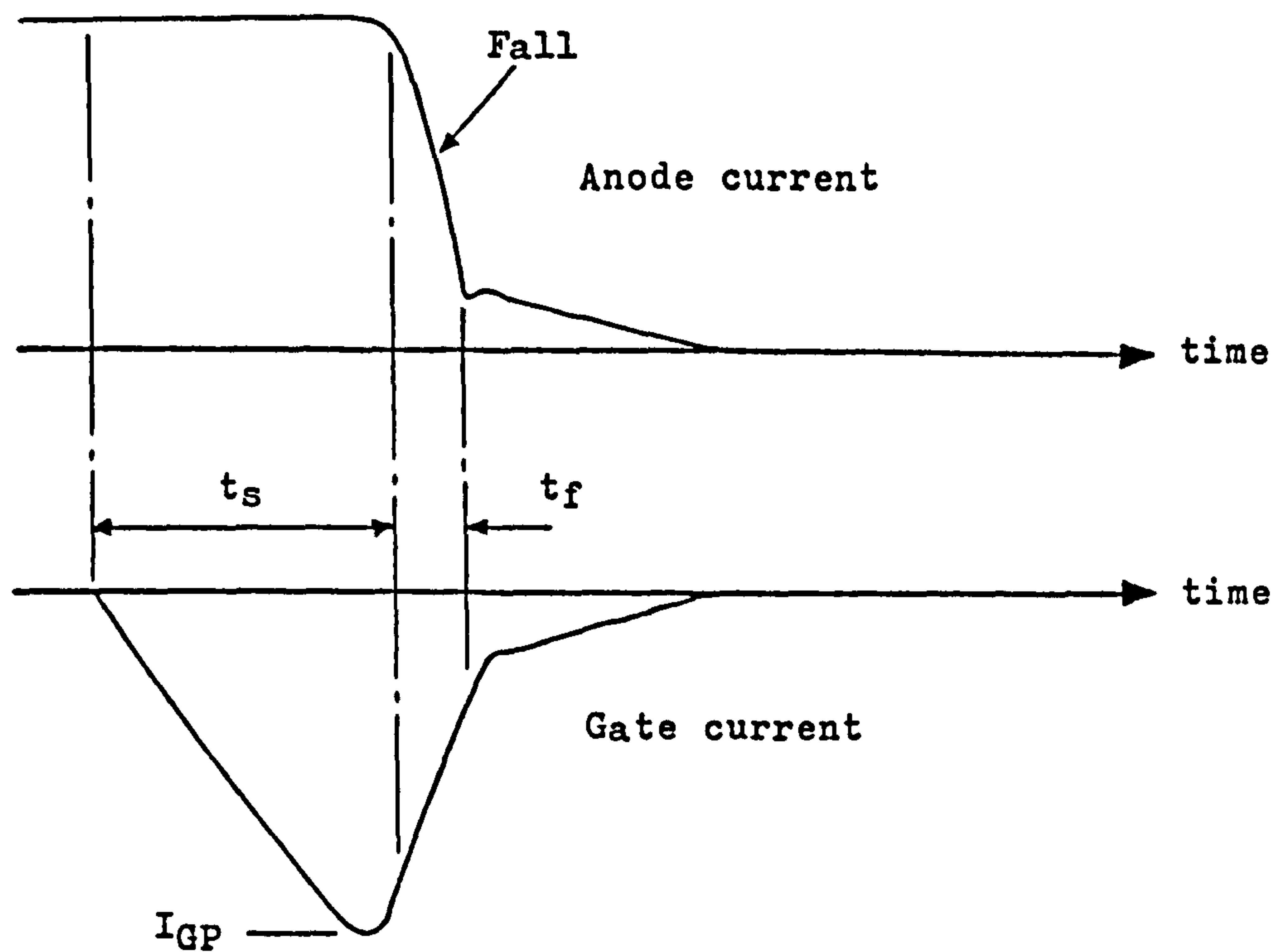
Time Scale : 2 $\mu$ S/div.

Figure 2.13 Effect of varying  $di_G/dt$  at turn-off

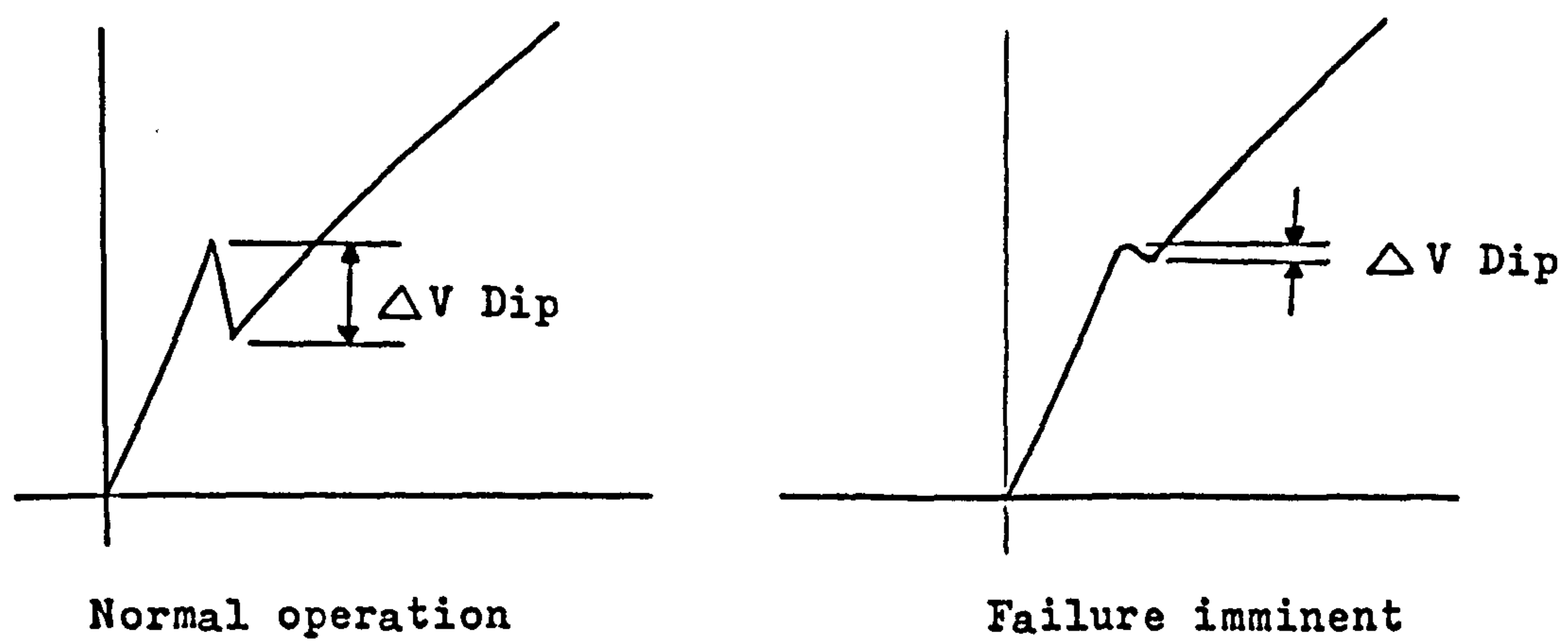
$V_{g-k}$  will result in a very slow rate of decay of the negative gate current. This increases the gate losses and at high values of controllable on-state current operations, it might be dangerous.

Critical turn-off condition may also be indicated by early commencement of the negative gate current decay during the storage time of the GTO [8]. This effect is illustrated schematically in Figure 2.14(a), whereas Figure 2.11 presents the turn-off waveforms under normal operating conditions.

Another observation which indicates critical turn-off is a reduced voltage spike caused



(a) Critical turn-off when gate current commences to decay during the storage time ( $t_s$ )



(b) Critical turn-off when lower dip during the voltage spike

Figure 2.14 Detecting critical turn-off



by unrealistic decrease in the fall rate of anode current [9], as shown in Figure 2.14(b).

**v ) Minimum off time ( $t_{off}$ )**

Turn-on must not be attempted too soon; at least until the snubber capacitor has acquired the supply voltage value following the overshoot, otherwise internal localised losses in the cathode elements that are still in conduction may be excessive, due to their high current concentration, and device permanent damage is imminent. Snubber losses will also increase due to the network higher discharge current.

**vi ) Turn-off losses**

The turn-off losses comprise two components. These occur during the anode current fall and the tail current times. Due to the longer duration and higher voltage level of the latter, although a much lower tail current flows, the loss is more significant than that of the former. It also increases further with high rates of rise of gate current  $di_G/dt$ , as the amplitude of the tail current is increased, but reduces with slower rise of the re-blocking voltage  $dv/dt$ .

The fall time loss, slightly affected by  $di_G/dt$  for a given value of controllable anode current, has high values of instantaneous power. However, the energy loss is not high owing to the very short fall time.

The total turn-off losses of the GTO are greatly dependent on the snubber circuit. Its loss contributes to the overall circuit switching losses, but removes much switching loss from the GTO.

**2.7 Rate of Rise of Anode Voltage ( $dv/dt$ )**

Like the conventional thyristor, the GTO can be triggered into conduction by a high  $dv/dt$ . The safe limit of the  $dv/dt$  that the device can tolerate varies according to its operating conditions. Destruction of the GTO may occur if it is triggered on by  $dv/dt$  because all the cathode islands do not respond equally, resulting in the anode current being concentrated in a few cathode fingers causing a thermal runaway.

For static  $dv/dt$ , applied when device blocking, this has values similar to the conventional thyristor. For example, the IR 160PFT100 GTO has a  $dv/dt$  rating of about  $1kV/\mu S$ .

*For  $dv/dt$  applied on at turn-off; the forward blocking voltage across the GTO is applied immediately after current ceases to flow (neglecting tail current). However, with the conventional thyristor forward recovery time must be allowed after turn-off, to eliminate the residual current carriers, before the re-application of  $dv/dt$ . Hence, the re-applied  $dv/dt$  withstand for a GTO tends to be lower than that of the conventional thyristor, and therefore snubbing is essential.*

*Furthermore, the very high  $dv/dt$  of the spike voltage during the GTO anode current fall can be tolerated if the amplitude of this voltage spike is kept low by keeping the snubber inductance to a minimum.*

## **2.8 Snubber Circuit Design**

*An in-depth investigation of the polarised snubber circuit (Figure 2.12) operation is reported in Chapter 3. Sub-section 2.6.2 describes the basic operation and now the main features of the design of the polarised snubber for GTOs will be covered.*

### **2.8.1 Snubber diode ( $D_s$ )**

#### **a) Requirements**

*The diode should;*

- i) Be able to carry, as a peak value, about 90% of the maximum current to be interrupted  $I_{TCM}$  by the GTO thyristor. This is the peak snubber current  $I_s$ ;*
- ii) Have a fast reverse recovery;*
- iii) Have a repetitive peak voltage rating at least equal to the maximum drop across the snubber resistor  $R_s$  following reverse recovery;*
- iv) Possess a good forward recovery characteristics; this and (ii) are incompatible in one device*

#### **b) Current rating**

*In addition to point (i), the low duty cycle necessitates an RMS current rating of approximately (Appendix V):*

$$I_{DRMS} = \frac{I_s}{2} \sqrt{\frac{\pi}{\omega T}} \quad (2.9)$$

#### **c) Voltage rating**

*Simplifying the reverse recovery waveform for design purposes, assume the worst*



condition of snap-off of diode reverse recovery current, as shown in Figure 2.15. The reverse recovery time  $t_{rr}$  of the diode must be known. Then, neglecting losses, the fall of the capacitor voltage from its peak value during  $t_{rr}$  is (Appendix v):

$$\Delta V_1 = (V_{pk} - E_d)(1 - \cos \omega t_{rr}) \quad (2.10)$$

where  $\omega = (L/C_s)^{1/2}$   
 $C_s$  = the snubber capacitance  
 $L$  = the oscillatory current path effective stray inductance

If the total removed reverse recovery charge  $Q_r$  is also known, it is simpler to use:

$$\Delta V_1 = \frac{Q_r}{C_s} \quad (2.11)$$

The peak reverse recovery current  $I_{rp}$  is (Appendix v):

$$I_{rp} = (V_{pk} - E_d)(C_s/L)^{1/2} \sin \omega t_{rr} \quad (2.12)$$

or if a perfectly triangular waveshape is adopted

$$I_{rp} = \frac{2Q_r}{t_{rr}} \quad (2.13)$$

With  $I_{rp}$  diverted into  $R_s$ , the voltage drop is:

$$\Delta V_2 = I_{rp} R_s \quad (2.14)$$

$\Delta V_2$  provides the first estimate of the peak voltage felt across  $D_s$ . The criterion for the GTO voltage to remain positive is;

$$\Delta V_1 + \Delta V_2 < V_{PK} \quad (2.15)$$



The criterion for no undershoot is;

$$\Delta V_1 + \Delta V_2 < V_{PK} - E_d \quad (2.16)$$

Upon current transfer into  $R_s$ , the remaining capacitor voltage is  $(V_{PK} - \Delta V_1)$ , this being the second estimated value.

The higher of the two estimates must be used. With slow recovery diodes, equation 2.14 is likely to give the highest required voltage rating, since  $I_{rp}$  will be high. With fast recovery diodes,  $\Delta V_1 \rightarrow 0$  and  $D_s$  should then have a voltage rating equal to  $V_{PK}$ , i.e. that of the GTO.

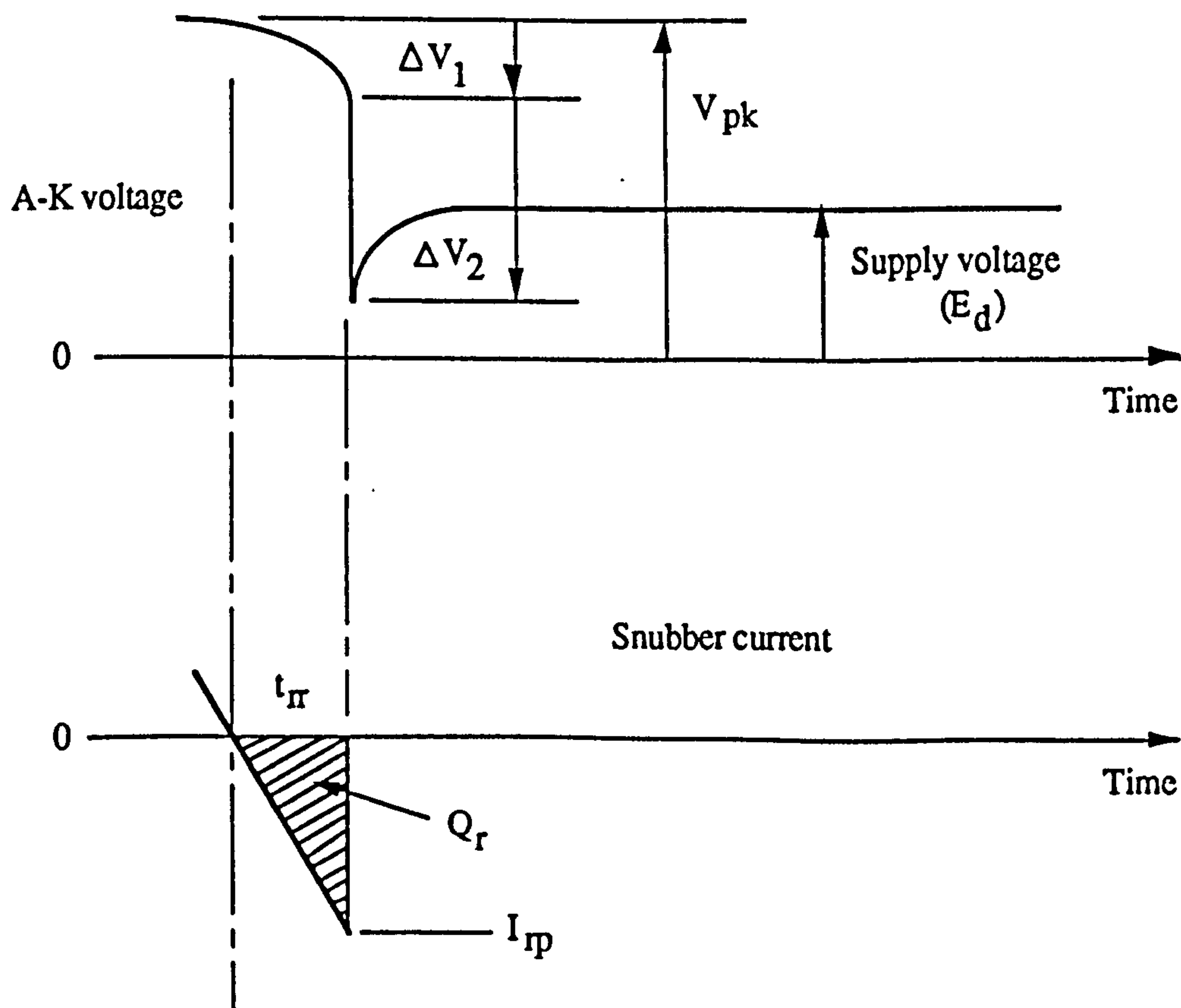


Figure 2.15 Instantaneous snap-off of the snubber diode reverse recovery current

## **2.8.2 Snubber capacitor ( $C_s$ )**

### **a ) Requirements**

*The capacitor must:*

- i ) Limit the  $dv/dt$  of the rising blocking voltage to less than the rated value of the device;*
- ii ) Limit the overshoot voltage to give a peak GTO voltage  $V_{PK}$  which is always below the device voltage rating;*
- iii ) Have a low self inductance and resistance so that its contribution to the snubber-GTO loop impedance is low;*

### **b ) Capacitance value**

*The maximum allowable GTO  $dv/dt$  data for the voltage rise immediately following the voltage spike at turn-off must be known, hence the value of  $C_s$  can be obtained from  $[dv/dt]_{max} = I_s / C_s$ . Manufacturers often recommend snubber capacitor values, based simply on the  $dv/dt$  limiting requirement when turning off maximum rated anode current.*

*In order to restrict voltage overshoot, and thereby allow the use of a lower voltage rated device, the capacitor size may need to be increased above such a recommended value. The value of  $C_s$  may be checked for overshoot using equation 3.18. The practical difficulties lie in estimating the effective path inductance  $L$  since it is usually a stray, and the effective damping resistance  $R$  at the frequency of oscillation  $\omega$ .*

### **c ) Voltage rating**

*The snubber capacitor must have a repetitive peak voltage rating of greater than the peak voltage  $V_{PK}$  applied to the GTO, which implies that it should be equal to or greater than that of the GTO.*

## **2.8.3 Snubber resistor ( $R_s$ )**

### **a ) Requirements**

*The resistor must:*

- i ) Limit the discharge current from the snubber capacitor  $C_s$  into the GTO at turn-on;*

- ii) Dampen the oscillation of  $C_s$  with the stray series inductance after the transfer of reverse current from diode  $D_s$  upon its reverse recovery.*
- iii) Have a low enough value to restrict the  $IR_s$  drop due to the transferred diode reverse recovery current such that, at worst, the voltage remains just positive and, at best, gives no undershoot.*
- iv) Have an adequate power handling capability.*

### **b) Resistance value**

*The ohmic value of  $R_s$  may be calculated by  $R_s = E_d / I_{DM}$ , where  $I_{DM}$  is the maximum snubber discharge current allowable at GTO turn-on, to satisfy point (i). It must then be checked against point (ii) using  $R_s = 2(L/C_s)^{1/2}$  and point (iii) using equation 2.14.*

### **c) Power rating**

*The resistor, having the diode in parallel, only conducts current flowing upwards from the snubber capacitor when it discharges. The two occasions per cycle for this are:*

- i) At GTO turn-on when (neglecting the device small dissipation) the energy loss is  $(C_s E_d^2)/2$  ( $E_d$  being the supply DC voltage).*
- ii) After current transfer from the reverse recovery diode  $D_s$  when, taking  $\Delta V_1 = 0$  with a fast recovery diode and overcritical damping, the capacitor  $C_s$  voltage falls from  $V_{PK}$  to  $E_d$  giving an associated energy loss  $C_s [(V_{PK} - E_d)^2]/2$  in  $R_s$ . The total energy loss per cycle in  $R_s$  is therefore;*

$$E_{RS} = \frac{1}{2} C_s \left[ E_d^2 + (V_{pk} - E_d)^2 \right] \quad (2.17)$$

*and the required power rating is;*

$$P_{RS} = E_{RS} f \quad (2.18)$$

*where  $f$  is the operating frequency*

## **2.9 Overall Switching Losses**

*At low frequencies (say lower than 1kHz), the total GTO switching and snubber losses*



are likely to be small. However, at high frequencies, particularly if the rate of rise of anode voltage is high, the turn-off losses and hence overall losses need to be evaluated.

Reducing  $dv/dt$  requires a large snubber capacitance which has the detrimental effect of adding to the GTO turn-on loss and the snubber resistor power rating. If assuming, for example, circuit operation at a frequency  $f=1.5\text{kHz}$ ,  $E_d=400\text{V}$  and  $C_s=4\mu\text{F}$ , then using  $(C_s E_d^2 f)/2$ , the snubber power loss at GTO turn-on is about 480W.

## 2.10 Effect of Temperature

The increase of junction temperature marginally increases the GTO forward conduction drop and also produces a small increase in storage time [10][11], but otherwise has imperceptible influence on turn-on and off performance.

## 2.11 Principles of GTO Gate Drive Circuitry

The GTO gate drive circuit, shown schematically in Figure 2.16, must be designed to satisfactorily turn the GTO both on and off. In general the on-drive circuit should operate as a current source, supplying a fast-rise gate current to rapidly turn-on the GTO. A voltage source is to produce the reverse turn-off voltage and must be limited to avoid prolonged breakdown of the gate-cathode junction.

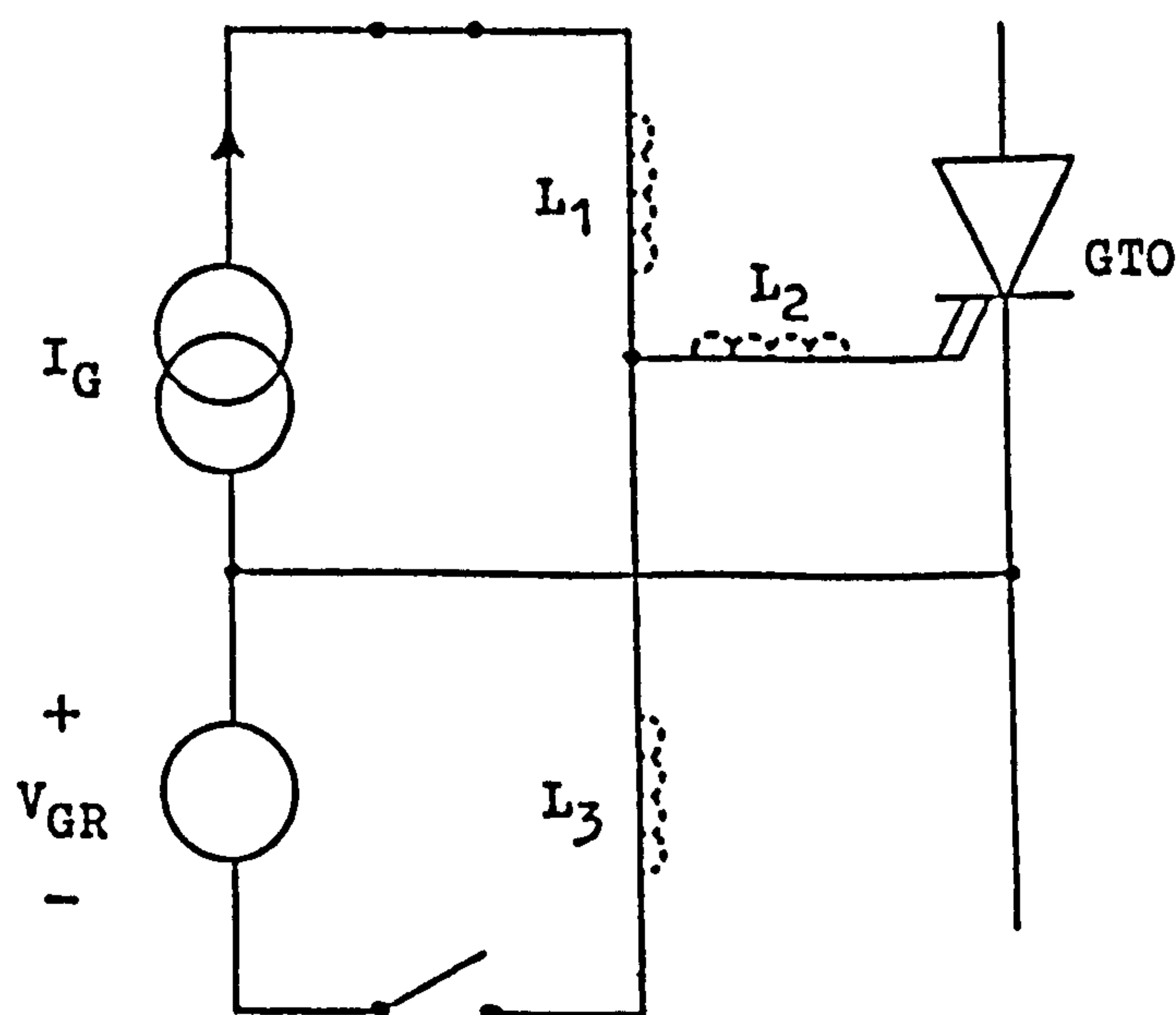


Figure 2.16 GTO gate drive circuit  
 $L_1$ ,  $L_2$  and  $L_3$  are stray inductances

For fast rise times, FETs should be used for final drive switching devices, and gate circuit inductances should be minimised.

## 2.12 Experimental Investigation

This section describes the tests performed on the International Rectifier 160PFT100 GTO thyristor. The test circuit is given together with a range of selected results. Although other characteristics are briefly mentioned, the main emphasis is given to the turn-off process.

### 2.12.1 Test circuit

The GTO is tested in the simple Class A chopper circuit giving a pulsed output to a resistive load as shown in Figure 2.17. The high blocking voltage is obtained using a variac-controlled rectifier, supplied from 415V three phase AC, 60A, mains. To keep within the laboratory power supply limit when controlling GTO peak rated current, the device is operated at a low duty cycle. The considerable electrolytic capacitor bank is needed to provide the peak controllable on-state current and present a low source impedance.

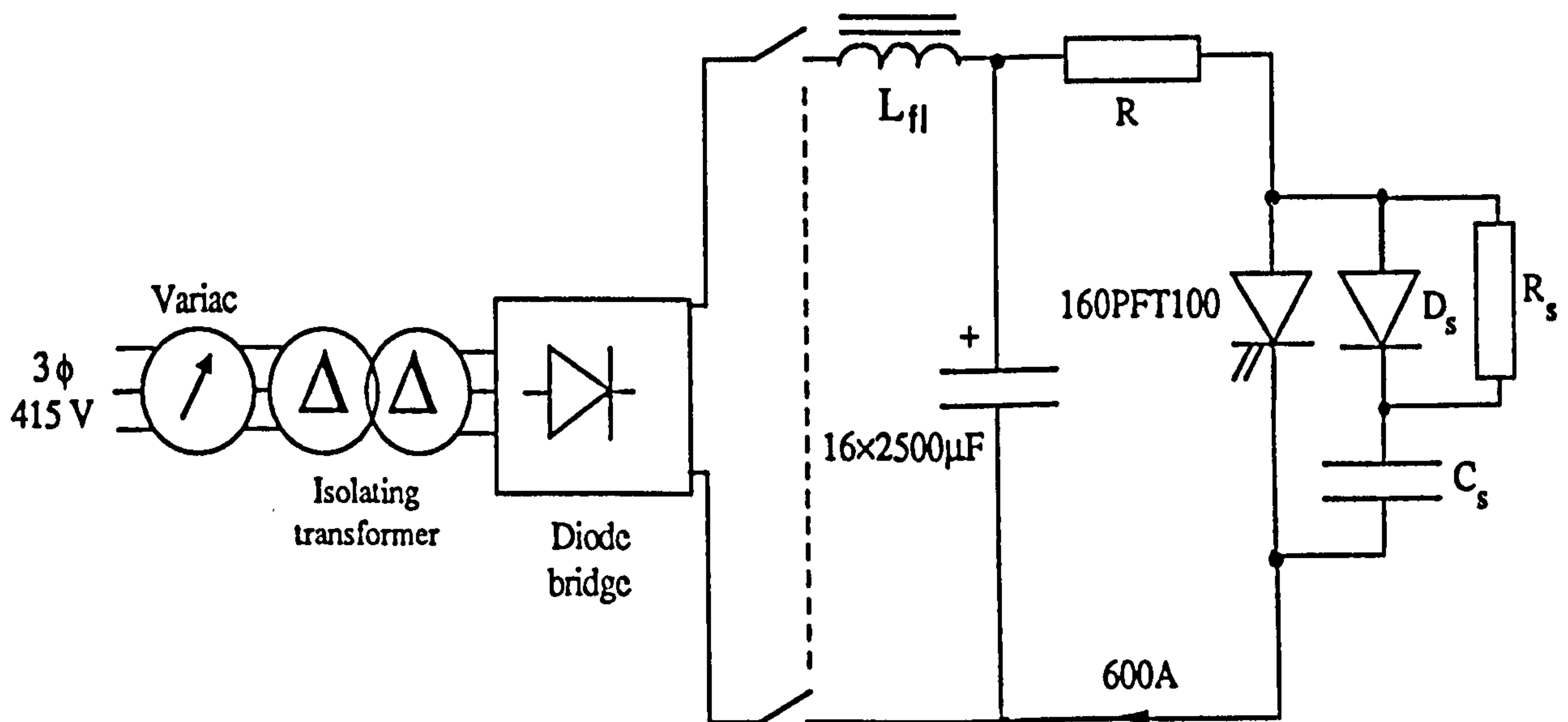


Figure 2.17 GTO test circuit

*Experimental tests are performed with the following circuit conditions, unless quoted otherwise:*

**a ) Power circuit**

<i>Supply DC voltage (<math>E_d</math>)</i>	<i>= 300V</i>
<i>Operating (switching) frequency (<math>f</math>)</i>	<i>= 100Hz</i>
<i>Duty Cycle (<math>\delta</math>)</i>	<i>= 7%</i>
<i>Load resistance (<math>R</math>)</i>	<i>= <math>0.5\Omega</math></i>
<i>Load inductances (<math>L_l</math>)</i>	<i>= <math>100\mu H</math></i>
<i>Snubber resistance (<math>R_s</math>)</i>	<i>= <math>8\Omega</math></i>
<i>Snubber capacitance (<math>C_s</math>)</i>	<i>= <math>4\mu F</math></i>

**b ) Gate drive circuit**

<i>Initial-on current pulse</i>	<i>= 11A with <math>8A/\mu S</math> rise; sustained for <math>14\mu S</math></i>
<i>Back-porch current (BP)</i>	<i>= 2A</i>
<i>Negative turn-off voltage pulse</i>	<i>= 12V sustained for <math>75\mu S</math></i>
<i>Negative bias (NB)</i>	<i>= 4V</i>

**2.12.2 Control signals**

*Figure 2.18 shows the complete logic circuit for providing the GTO gate control signals. IC1 is connected as an astable multivibrator, the switching frequency being determined by C1, R1 and Pt1 which can be adjusted between 50Hz and 1kHz.*

*The leading edge of IC1 output Q1 then triggers the two monostables of IC2, the outputs Q2 and Q3 of which are associated respectively with the initial-on and the back-porch signals. The duration of the initial-on pulse may be set by the external RC circuitry C2, R2 and Pt2 to any value between  $10\mu S$  and  $20\mu S$ , whereas C3, R3 and Pt3 control the range of the back-porch signal from 5% to 90% duty cycle.*

*However, the trailing edge of the back-porch logic pulse is then employed to generate the off Q4 and negative bias Q5 signals by triggering the monostables of IC3. The off signal may be adjusted for a duration of  $20\mu S$  to  $100\mu S$  by C4, R4, and Pt4.*

*Furthermore, the leading edge of the complement of the initial-on signal Q2 is used to clear the negative bias signal as the GTO turns on again. Figure 2.19 shows the observed control circuitry outputs.*



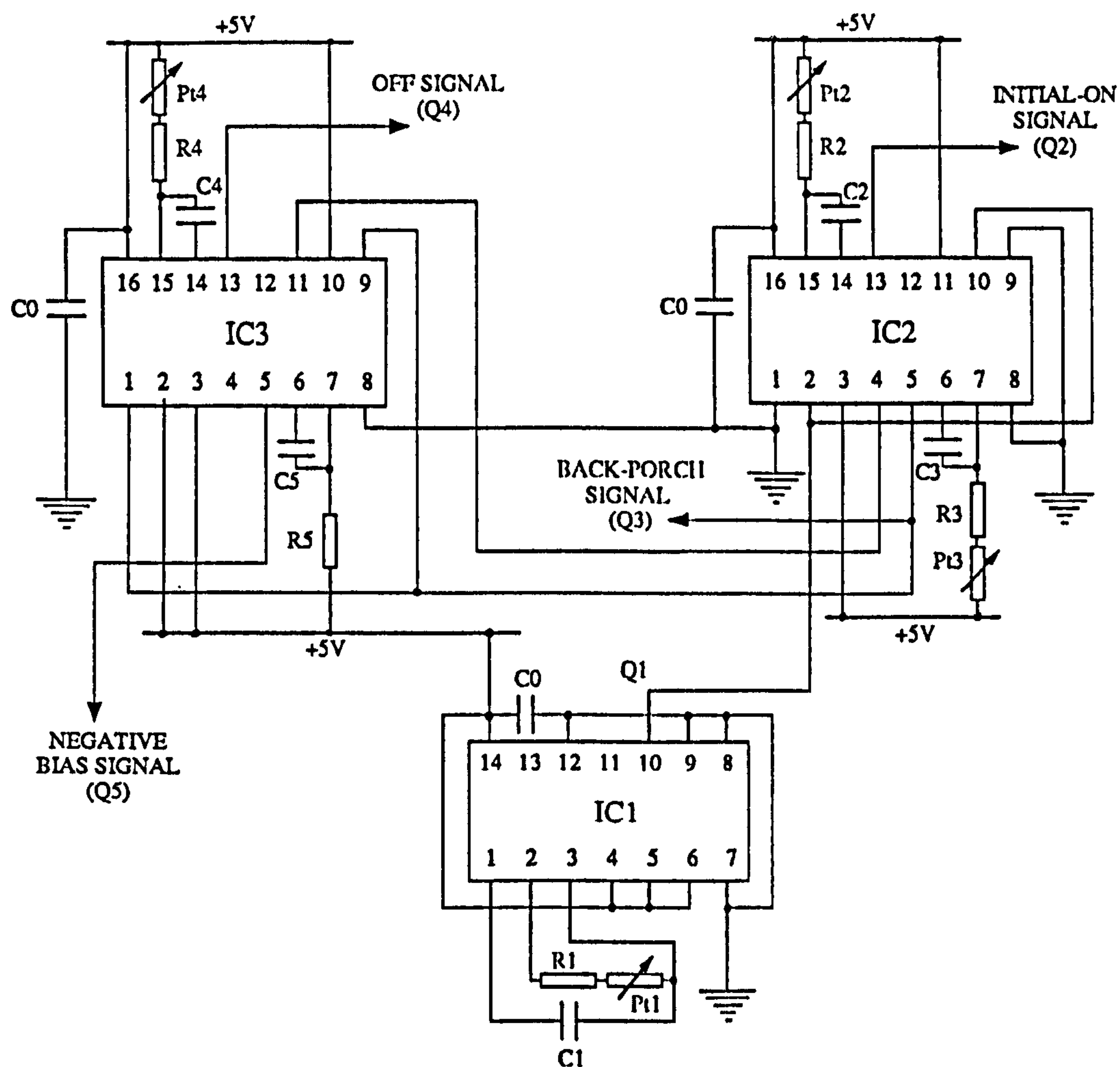
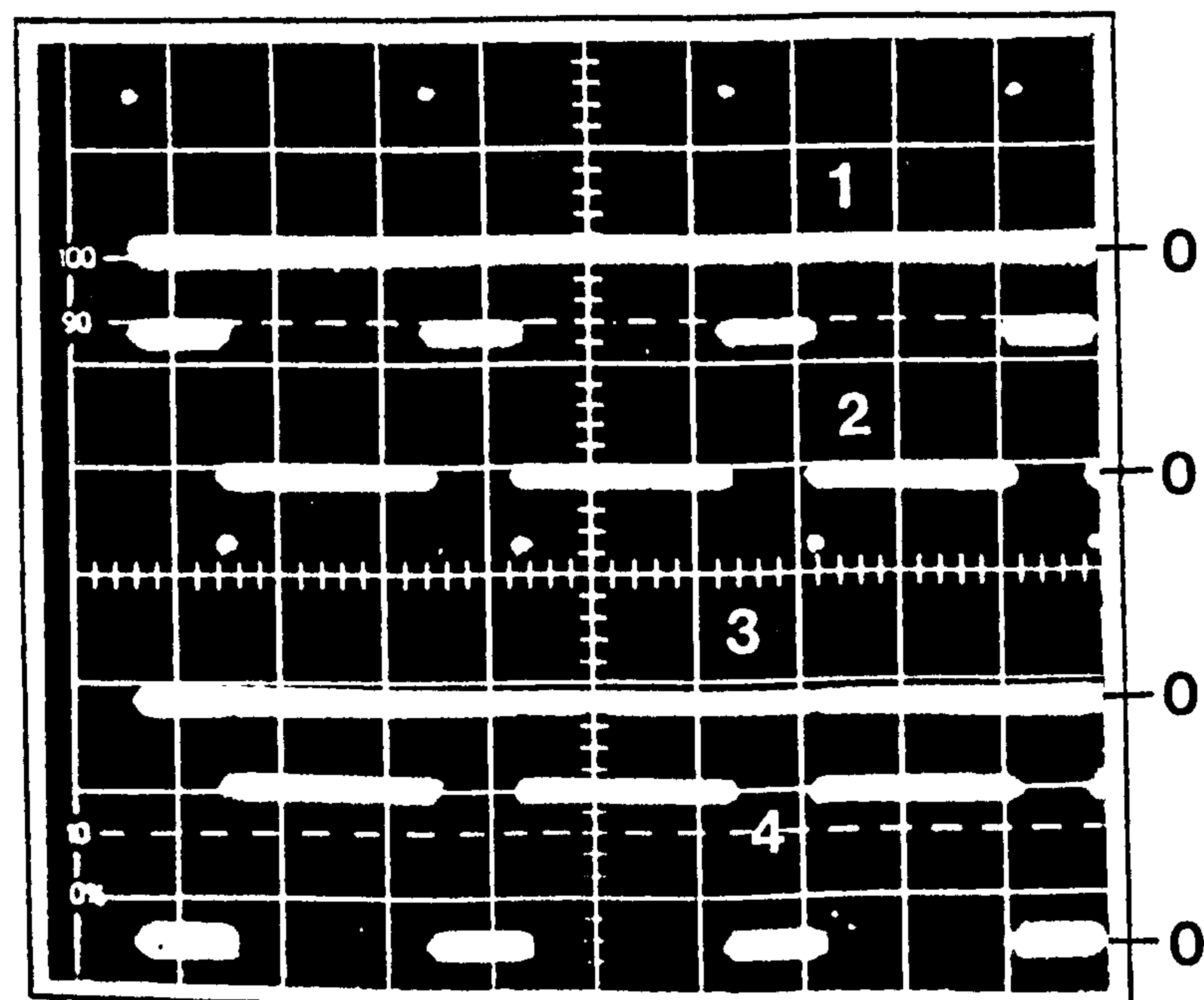


Figure 2.18 Control logic circuit



- (1) Initial on-pulse signal (2V/div.)
- (2) Back-porch signal (2V/div.)
- (3) Off-pulse signal (2V/div.)
- (4) Negative bias signal (2V/div.)

Time Scale : 2mS/div.

Figure 2.19 The control signals

### **2.12.3 Gate drive circuit**

*The gate drive circuit, shown in Figure 2.20, is capable of providing an initial turn-on current pulse of up to 15A, adjustable back-porch level (0-4A), adjustable turn-off voltage drive (10V-15V), a negative bias level of 4V and overall, the ability to control a GTO repetitive anode current up to 1000A.*

*The output terminals of the control logic circuitry and the inputs of the gate drive are electrically isolated by means of opto-isolators ICs 1 and 2. The negative rail of the turn-on drive and positive rail of the turn-off drive are common, as in Figure 2.16. The 5V power supplies for the opto-isolators are produced from the main supply rails by dropping the excess voltage with the aid of TR1 and ZD1, and TR2 and ZD2.*

*The outputs of the opto-isolator IC1 (3.5V high-to-low) to the on-drive circuit (initial-on and back-porch), are applied to TR4 and TR5 which invert and amplify the pulses to a maximum of 15V and 7V respectively; the power supply to TR5/7/9 is dropped to about 7V by TR3 and ZD3 (Figure 2.20), thus providing a lower voltage for the back-porch drive.*

*The combinations TR6, D1 and TR8, and TR7, D2 and TR9 are to ensure that no GTO on gate drive current is provided when the output of IC1 is high (GTO in the off state). The output of the OR gate (D3 in conjunction with D4) is applied to the MOSFET TR10, which is switched hard for the duration of the initial-on pulse producing a current pulse, Figure 2.21, limited by  $R_G$  and the MOSFET static on-state resistance  $R_{DS}$  ( $0.14\Omega$  for IRF530). The continuing back-porch pulse, being of lower voltage, biases TR10 to a lower current level. D9 is employed to aid in reverse biasing TR10 during the off period of the GTO. This reverse bias voltage is limited to 12V by ZD4.*

*The turn-off and negative bias control signals are executed in the same manner as those of the initial-on and back-porch pulses. The output of the OR gate (D7 and D8) is applied to the gates of the parallel MOSFETs TR11/12/13, which connect the negative voltage pulse followed by the negative bias, Figure 2.21, directly to the GTO gate.*

*ZD5 and ZD6 are to limit the positive gate-source voltage of TR10 and TR11/12/13 to 10V respectively. The  $48000\mu F$  high grade electrolytic capacitor  $C_S$  is employed to sink the current extracted from the GTO gate at turn-off.*

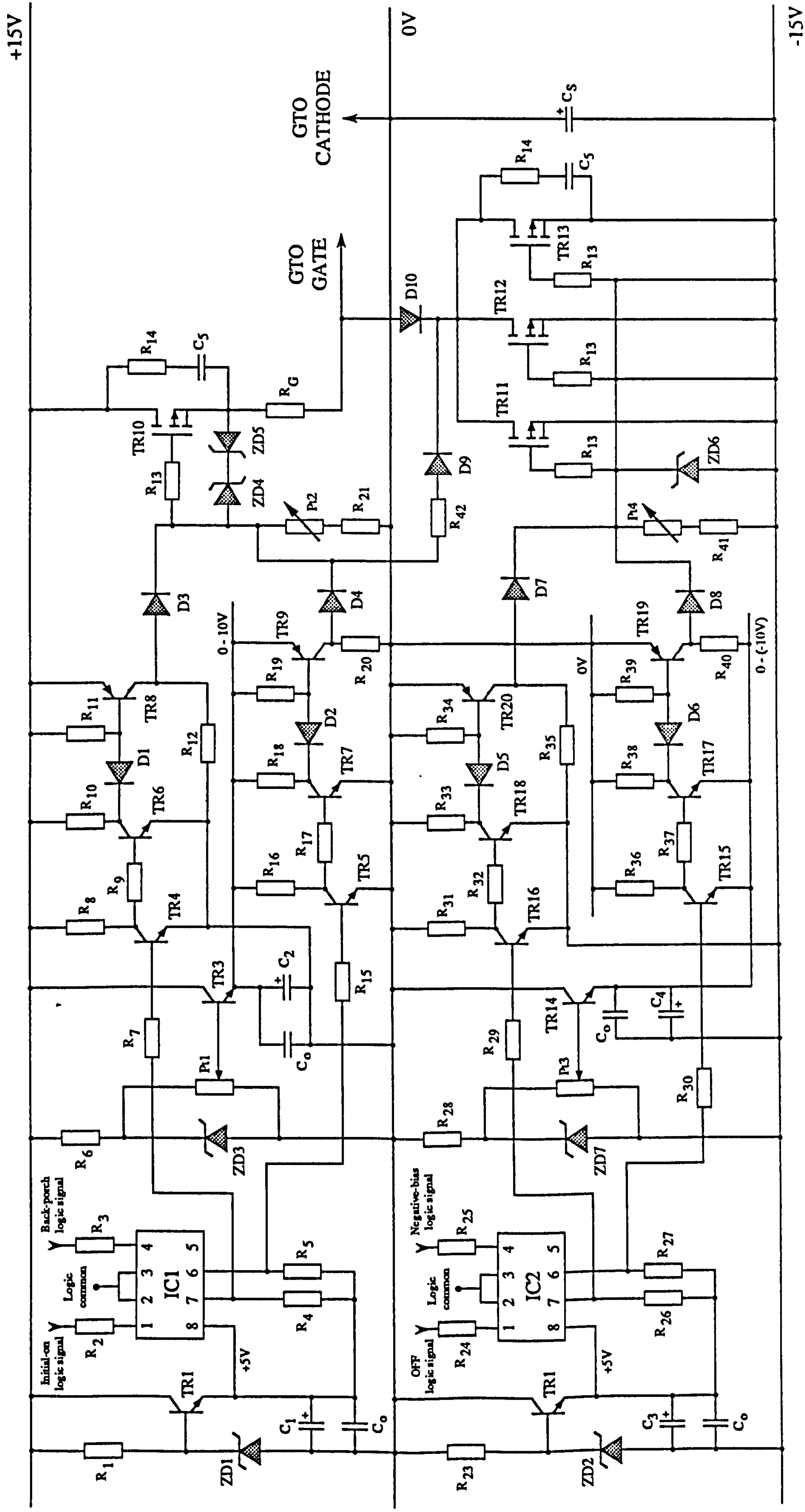
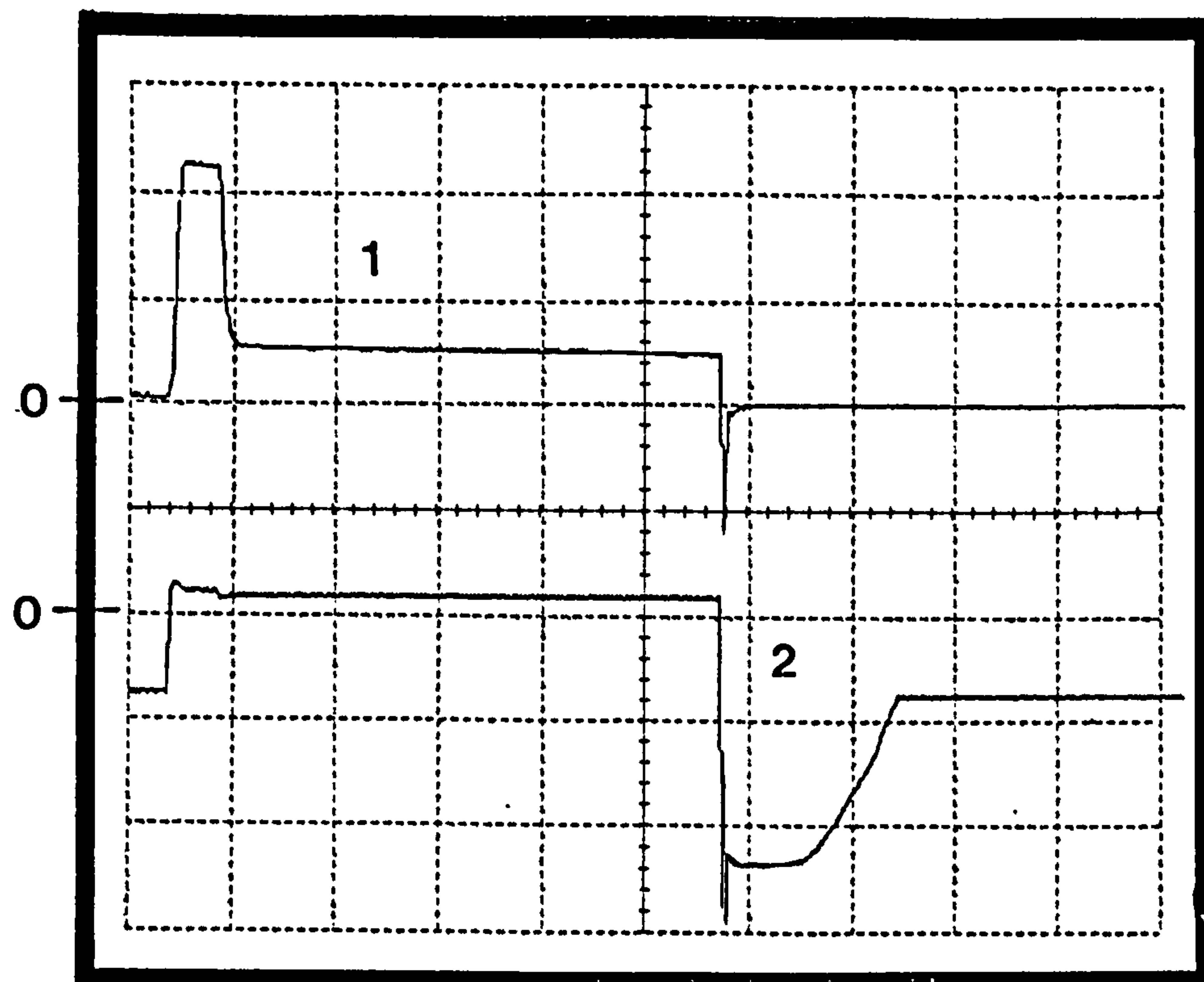


Figure 2.20 GTO gate drive circuit





(1) Gate Current (5A/div.)  
 (2) Gate Voltage (5V/div.)

Time Scale: 50µs/div.

Figure 2.21 The 160PFT100 gate current and voltage waveforms

#### 2.12.4 Drive circuit power supplies

*The mean positive gate current, and hence the current drawn from the positive power supply, depends on the frequency of operation and the duty cycle. At large duty cycles at low frequencies, the influence of the initial gate drive current peak becomes negligible.*

*The gate drive circuit requires a dual power supply of 15V and -15V, Figure 2.22. This provides a mean on-state gate current of up to 4A, and the required mean turn-off current of about 150mA; the gate reverse conduction duty cycle being extremely low.*

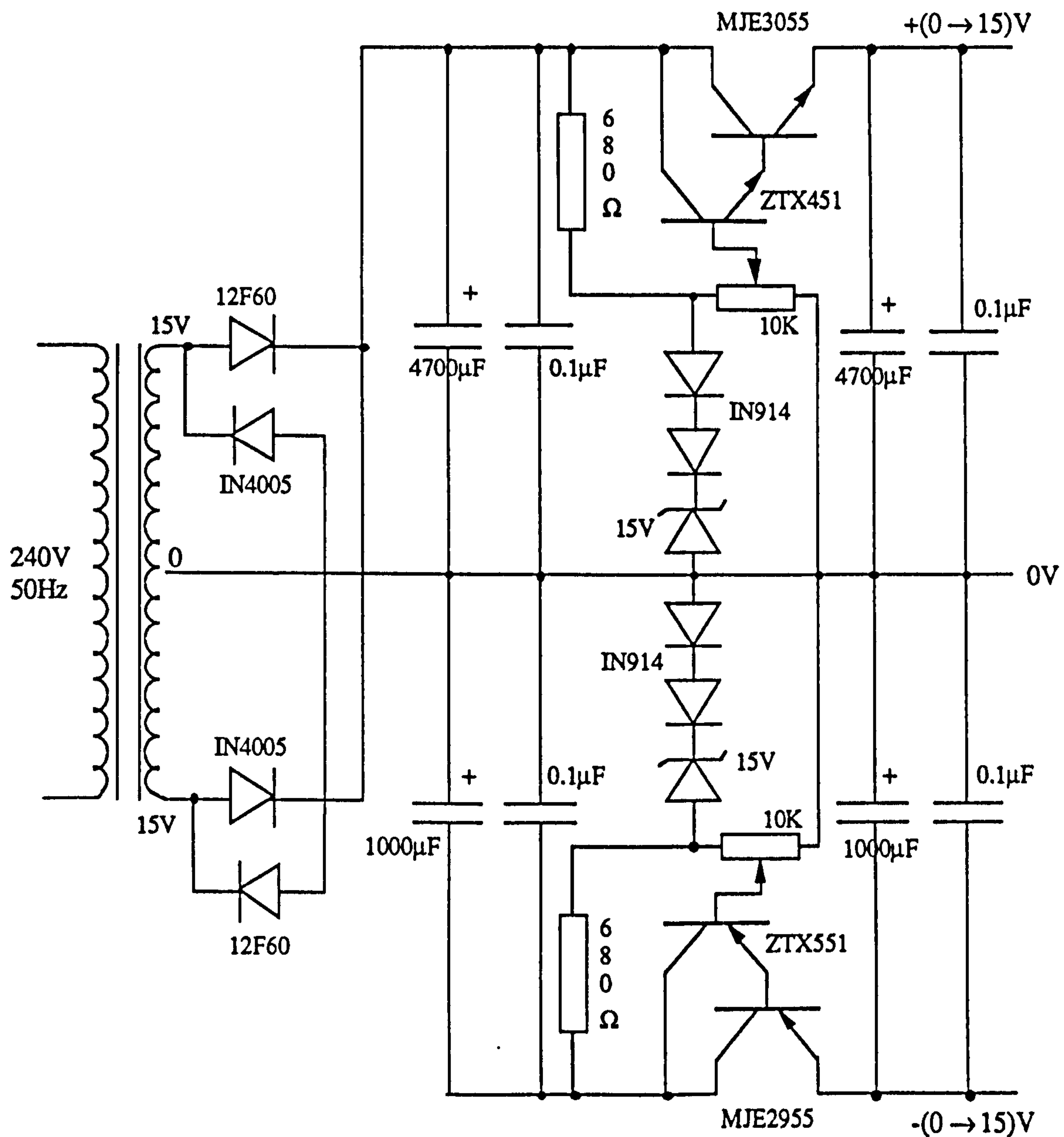


Figure 2.22 Drive circuit power supplies

### 2.13 Results

*a ) The rate of rise of the negative gate current pulse is substantially independent of the anode current being interrupted, it is controlled by the applied negative gate voltage and the gate circuit stray inductances, Figure 2.13(c).*

*b ) The negative peak gate current is dependent upon the anode current being interrupted (for a given  $di_G/dt$ ), increasing with it (Figure 2.13(a)) but not linearly (Figure 2.23).*

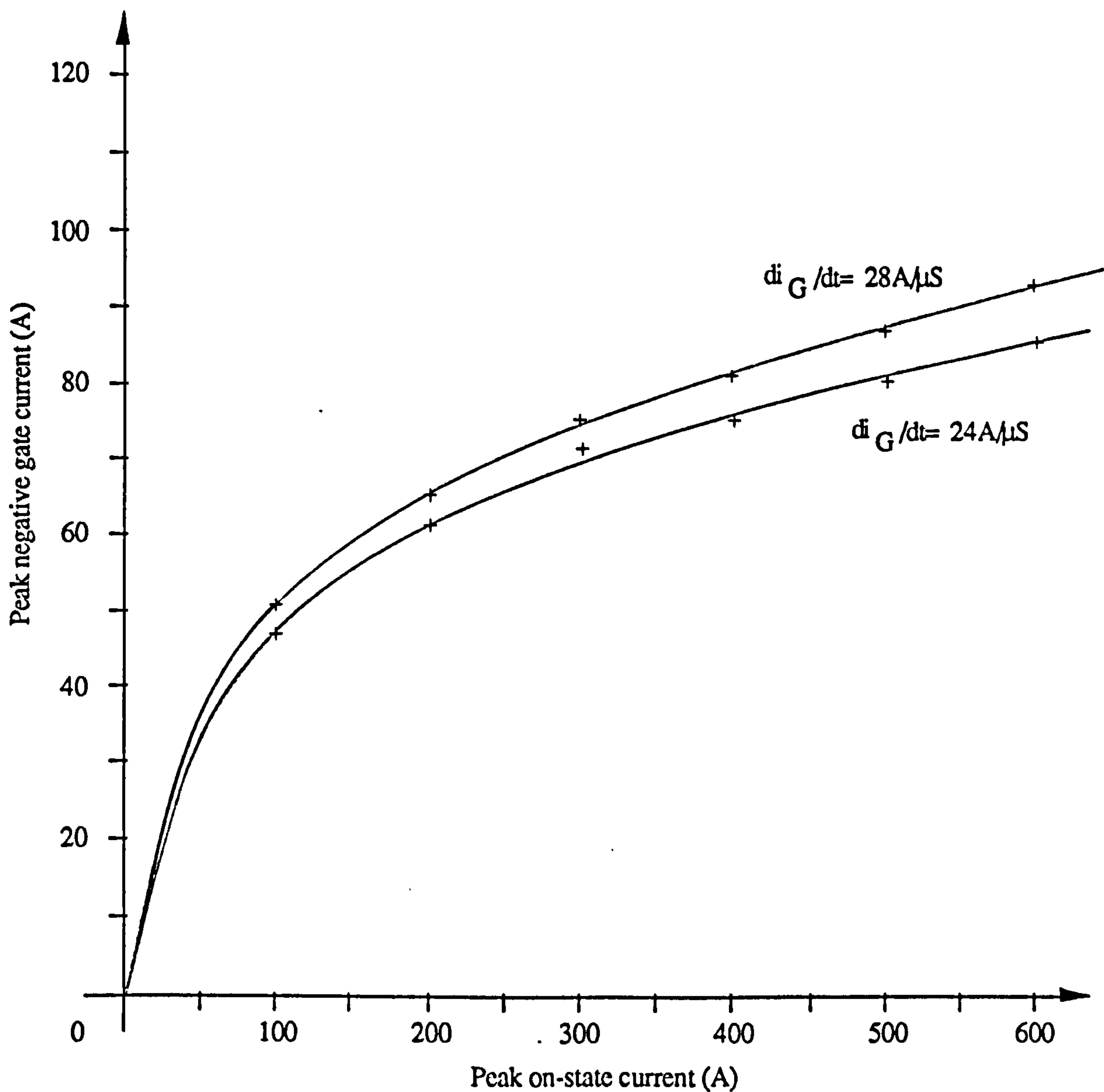


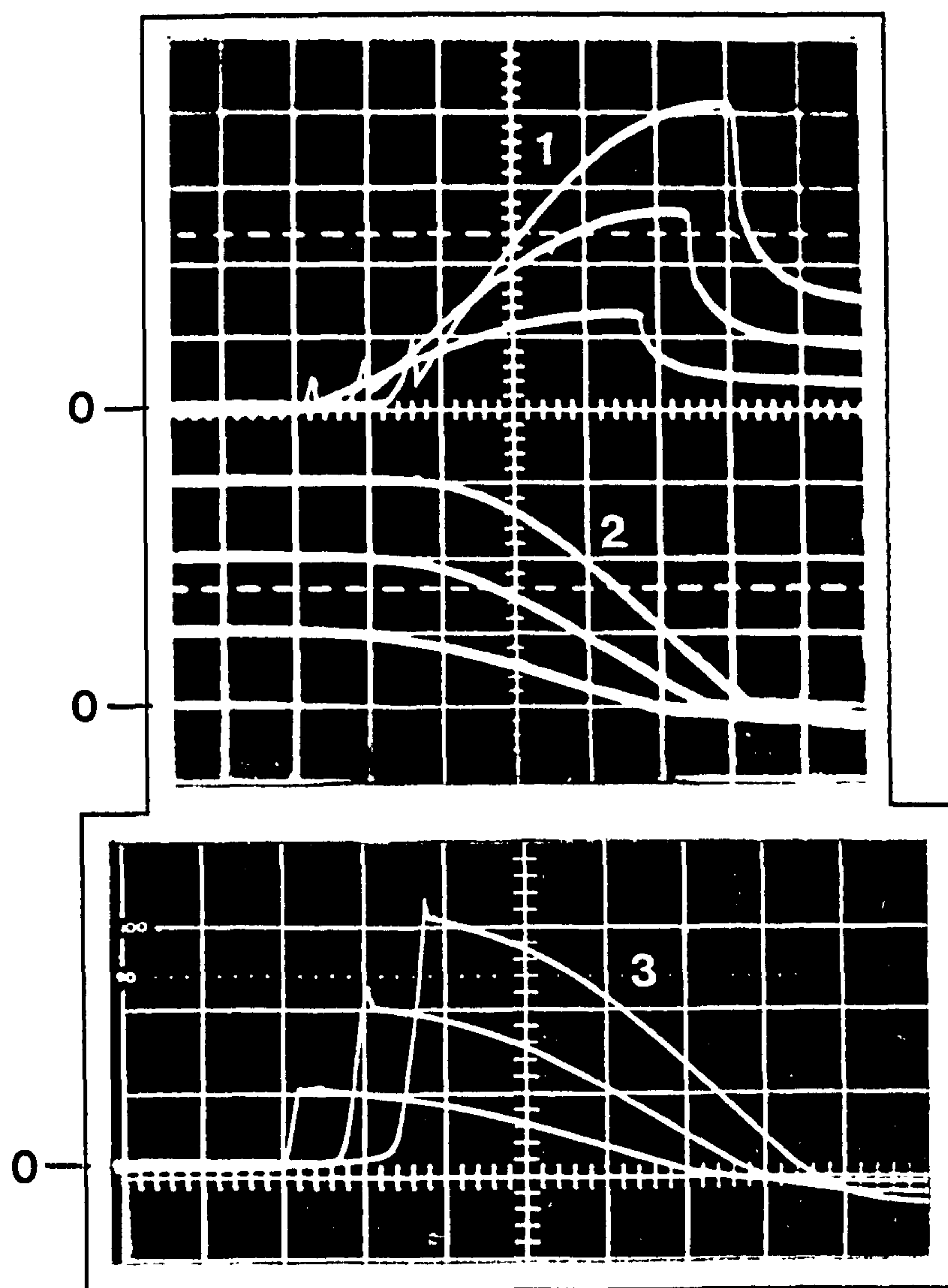
Figure 2.23 Variation of negative gate current with on-state current (160PFT100)

*c ) The anode current being interrupted does not commence its fall until the peak of the negative gate current pulse is reached (or almost); it then reduces rapidly to the 'tail', Figure 2.11.*

*d ) During the rapid fall of anode current, a voltage spike is induced across the GTO due to the GTO-snubber circuit loop stray inductances (Figure 2.11).*

*e ) The voltage spike, snubber capacitor accumulated voltage during the spike and oscillatory overshoot voltage amplitudes increase with anode current being turned off, Figure 2.24(a) and (b).*



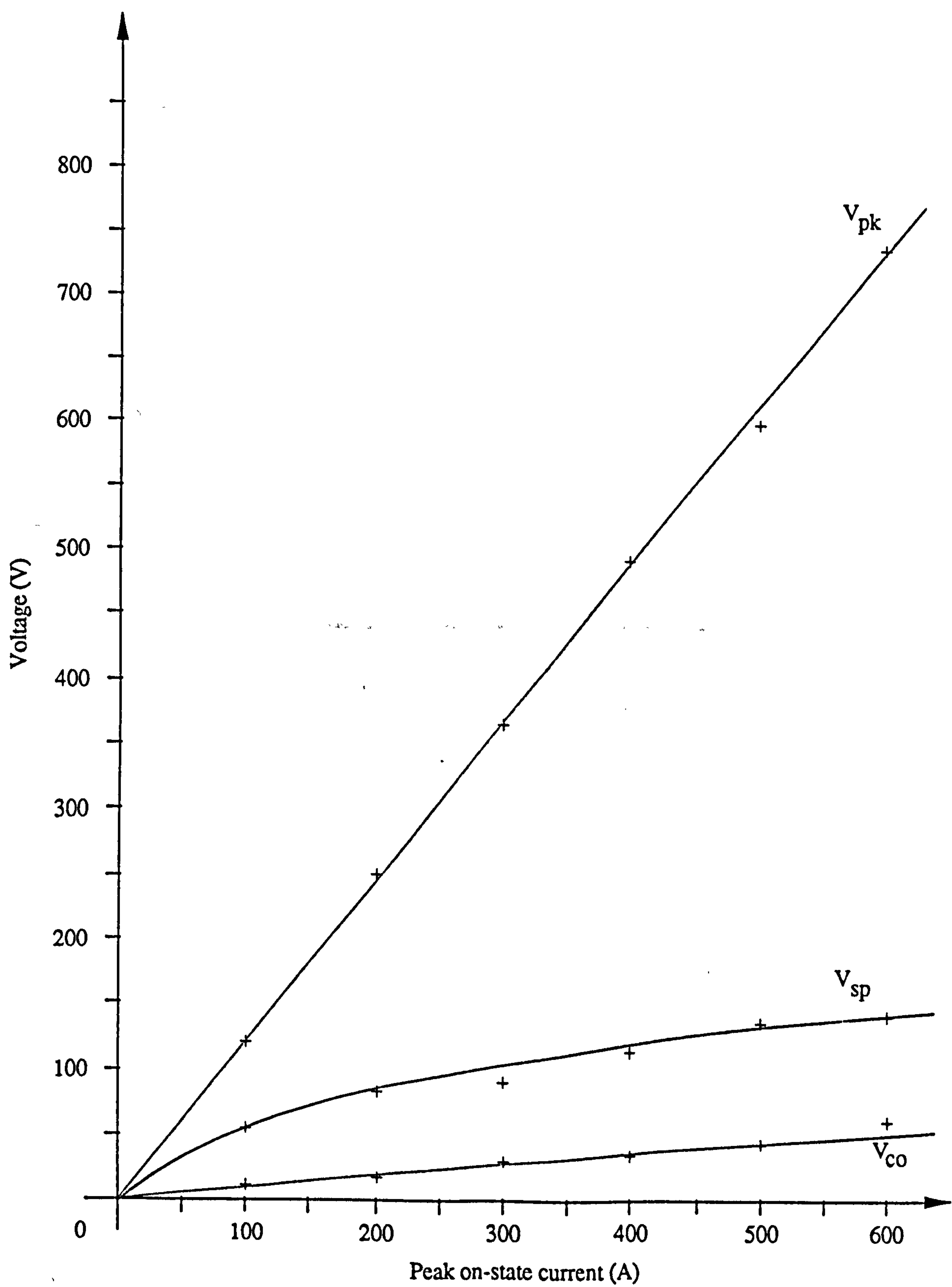


(a) Waveforms

- |                                  |             |
|----------------------------------|-------------|
| (1) A-K Voltage                  | (200V/div.) |
| (2) Load Current (anode+snubber) | (200A/div.) |
| (3) Snubber Current              | (200A/div.) |

Time Scale: 2μS/div.

Figure 2.24 Effect of interrupted anode current on the GTO A-K voltages (160PFT100)



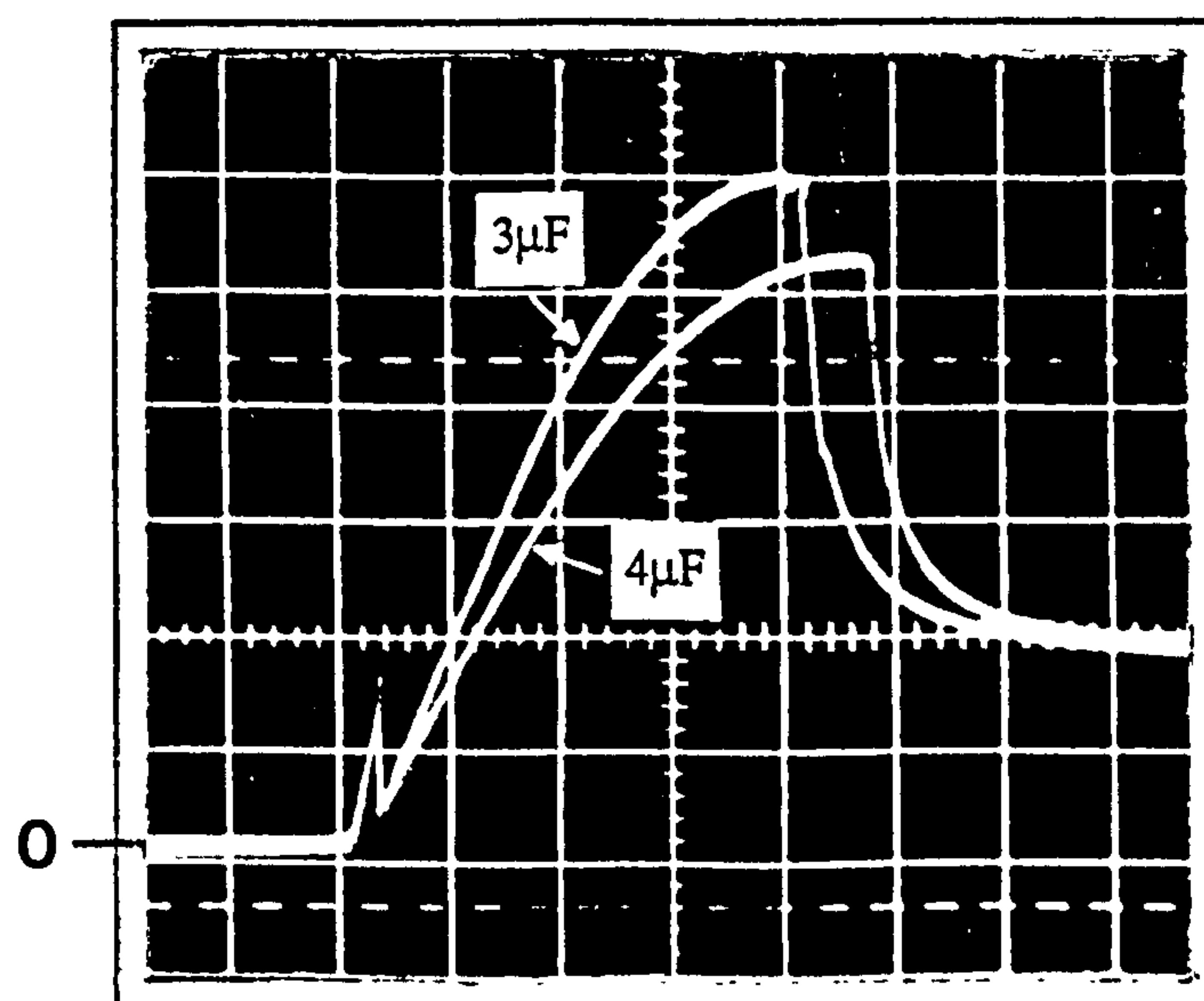
(b) Variation of the spike, snubber capacitor accumulated and peak voltages with on-state current

Figure 2.24 Effect of interrupted anode current on the GTO A-K voltages (160PFT100)

*f ) The rapid GTO controlled fall of negative gate current produces a reverse 20V avalanche of the GTO gate-cathode junction due to the gate circuit  $L_g di/dt$ , Figure 2.11.*

*g ) As the GTO anode current falls, the main device current is diverted into the snubber circuit whose capacitance charges through the series stray inductances with one quarter cycle of oscillation giving the voltage overshoot. Figures 2.11 and 2.24(a) demonstrate this.*

*h ) The rate of rise  $dv/dt$  and the amplitude of the oscillatory overshoot is reduced and its duration increased by increasing the snubber capacitance value as illustrated in Figure 2.25(a) and (b).*



(a)

A-K Voltage

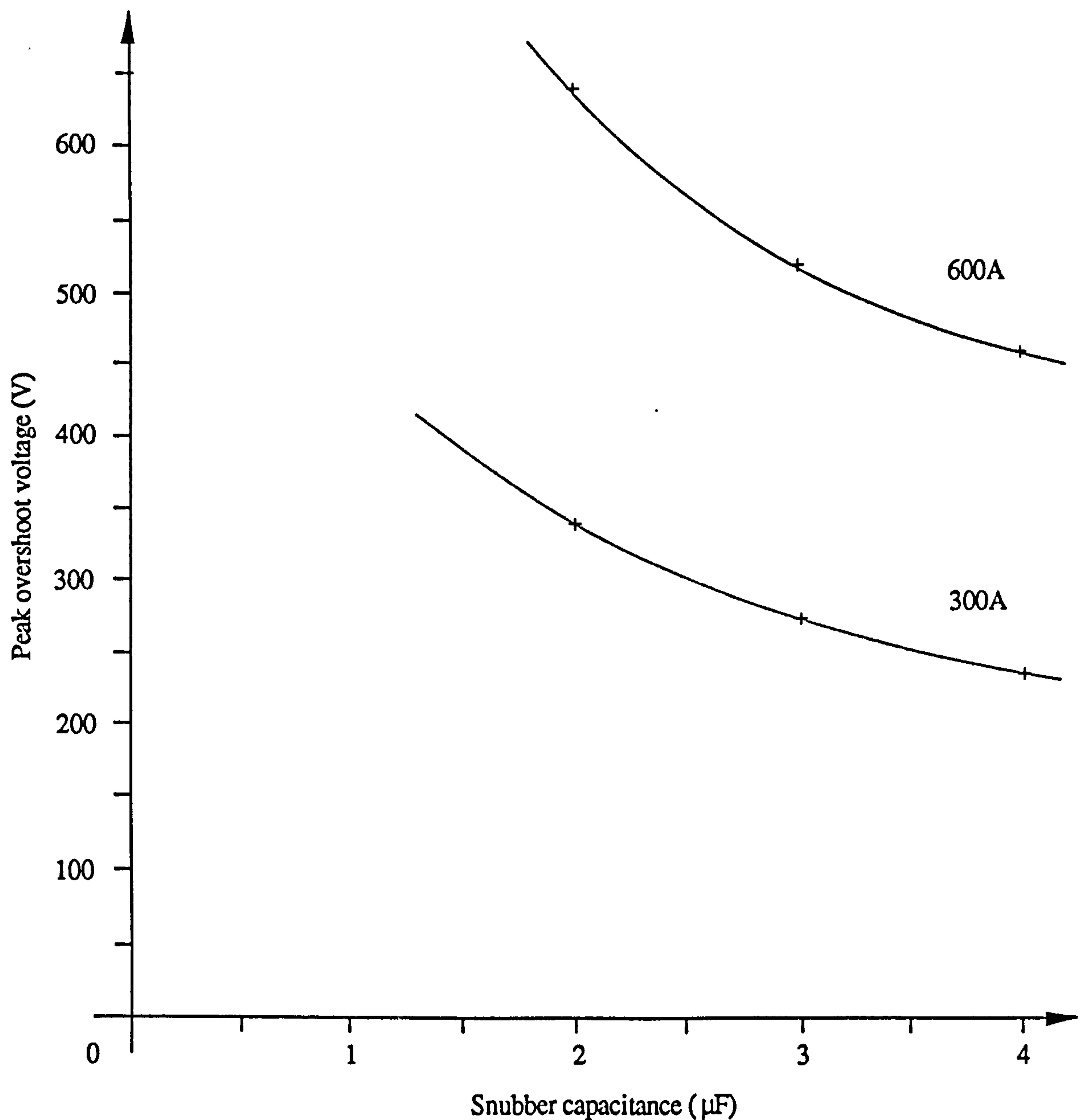
(100V/div.)

Time Scale: 2μS/div.

Anode Current= 400A

Figure 2.25 Effect of varying the snubber capacitance on the GTO A-K voltage (160PFT100)





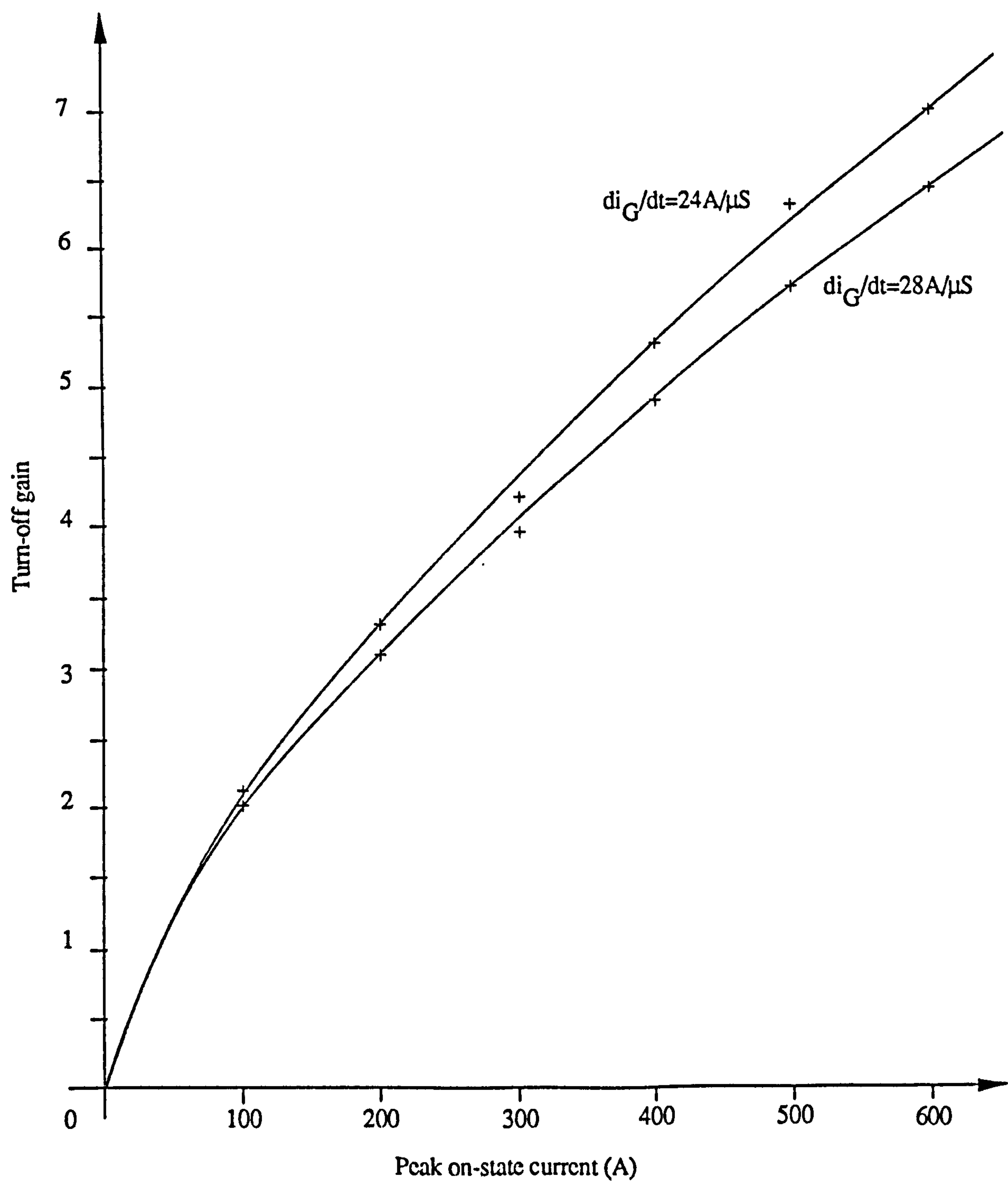
(b)

Figure 2.25 Effect of varying the snubber capacitance on the GTO A-K voltage (160PFT100)

*i ) The sudden collapse of the blocking voltage from the oscillation peak is due to the  $IR_s$  drop after the snubber diode reverse recovery. When this is complete, the further discharge through the snubber circuit resistor is damped (figure 2.11).*

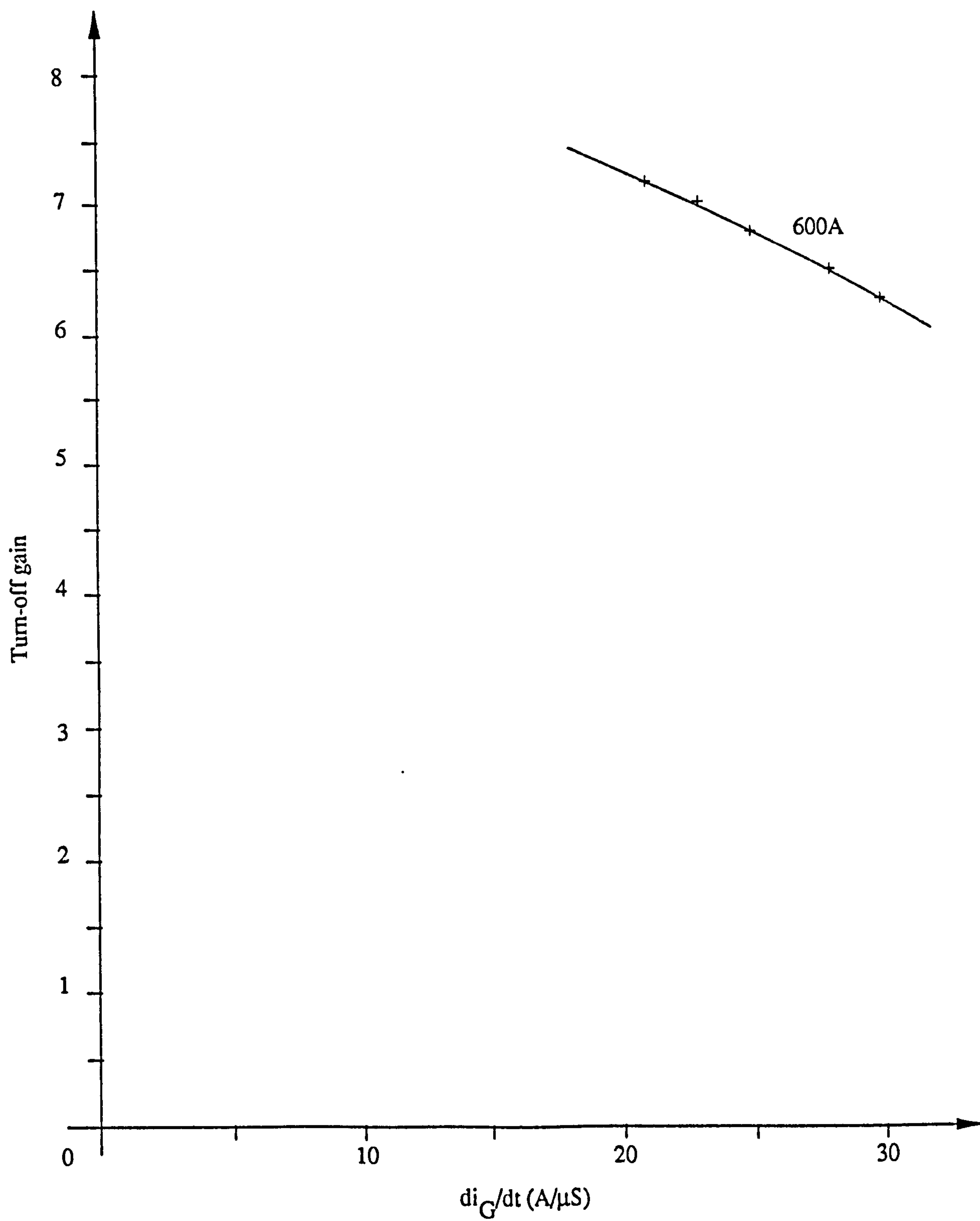
*j ) A turn-off gain ( $I_T/I_{GP}$ ) of 5 is often quoted as typical. However, this may be misconstrued since the gain is very much dependent upon the triangular negative gate current pulse peak (Figure 2.26(a)).*

Figure 2.26(b) demonstrates that a gain of 5 is only attainable when interrupting around maximum rated current with low  $di_G/dt$  values, the peak gate current then being relatively low.



(a) Variation of turn-off gain with on-state current

Figure 2.26 Effect of on-state current and  $di_G/dt$  on turn-off gain (160PFT100)



(b) Variation of turn-off gain with  $di_G/dt$

Figure 2.26 Effect of on-state current and  $di_G/dt$  on turn-off gain (160PFT100)



k ) For fast turn-off, the gate must be driven hard, that is the peak negative gate current must be high to extract the internal charge as quickly as possible. This requires a high  $di_G/dt$  which gives a low storage time  $t_s$  (Figure 2.13(c)). The short fall time  $t_f$  is marginally reduced at higher negative gate currents, giving lower turn-off time ( $t_s+t_f$ ), Figure 2.27. Thus, for fast turn-off, a low turn-off gain results; this is unfortunate.

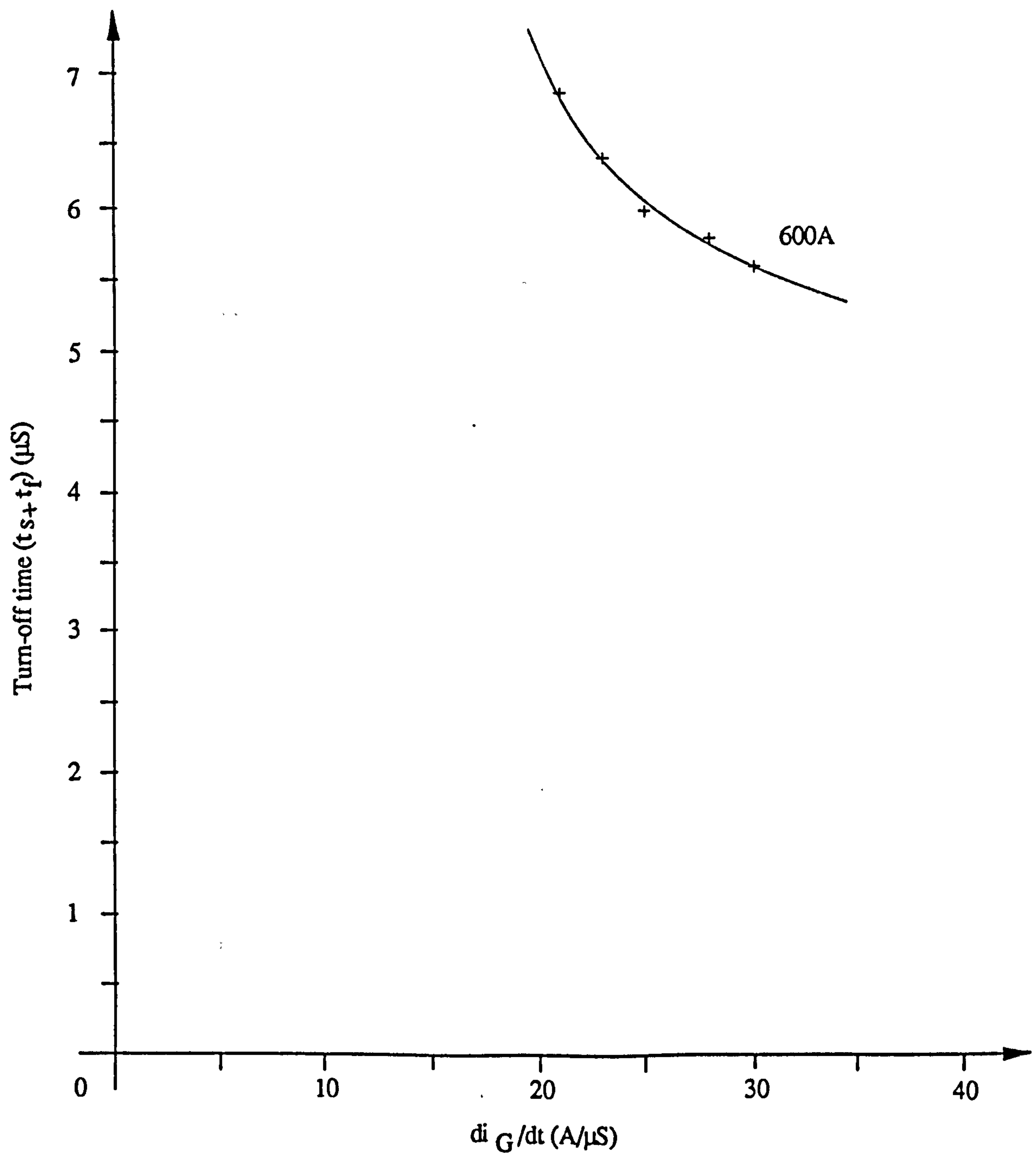
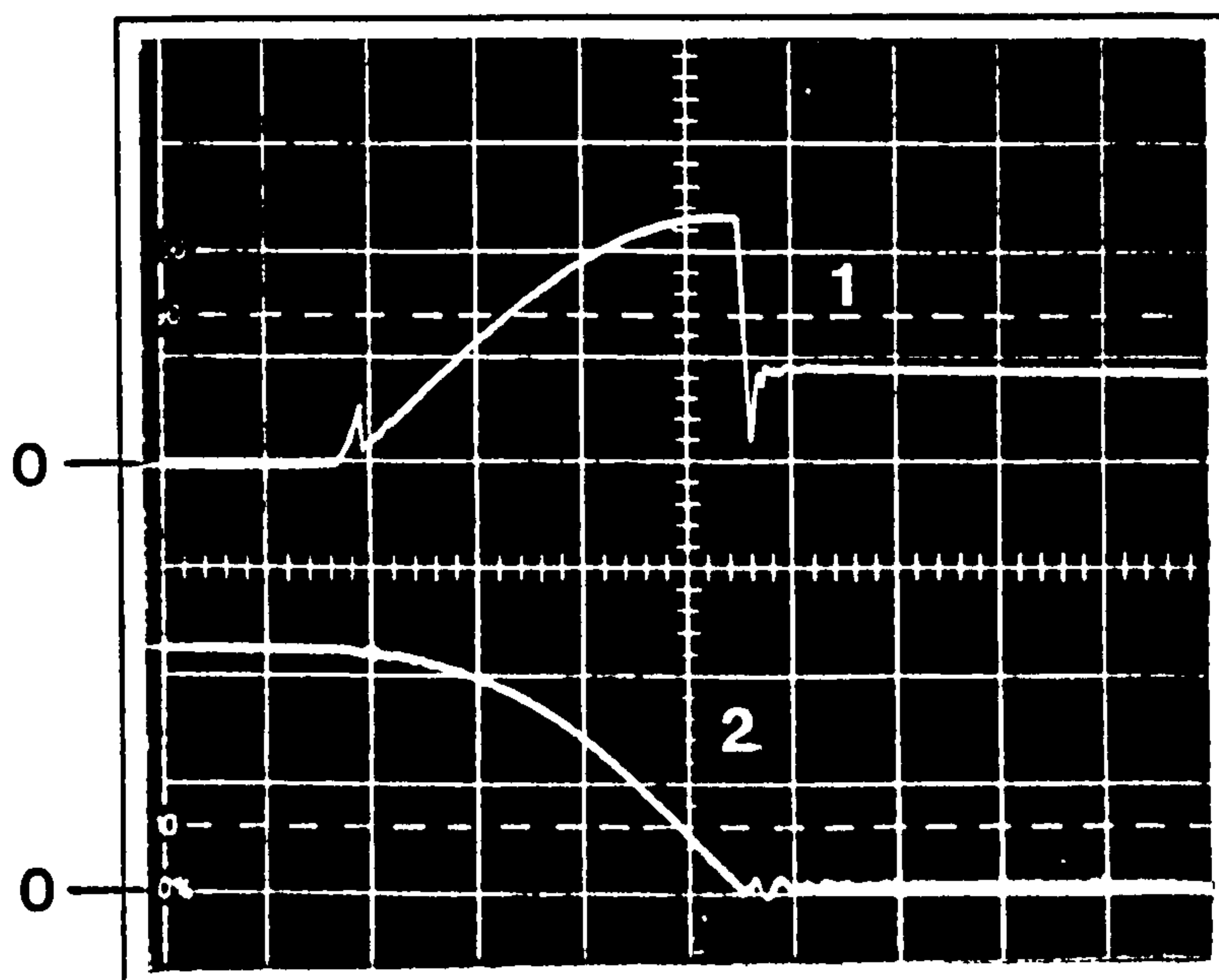


Figure 2.27 Variation of turn-off time with  $di_G/dt$  (160PFT100)

1 ) If the snubber diode reverse recovery is slow, the GTO voltage upon its collapse from the peak overshoot value, due to the  $IR_s$  drop, will undershoot the supply voltage, Figure 2.28, even down to zero or a negative value with high values of snubber resistance. The subsequent  $dv/dt$  as the voltage rises to the steady blocking voltage may be dangerous.



(1) Anode-Cathode Voltage (200V/div.)  
 (2) Load Current (100A/div.)

Time Scale: 2 $\mu$ S/div.

Figure 2.28  $dv/dt$  following the undershoot of the anode voltage (160PFT100)

## 2.14 Conclusions

The GTO behaviour and characteristics are described and supported by measurements made at anode currents of up to full current on a device rated at 600A using a specially constructed test circuit. Requirements of the snubber circuit have been identified and its design presented.

The gate drive circuit can be employed over a wide range of switching frequencies and duty cycle, and is capable of controlling a GTO peak anode current of up to 1kA.

*It is during the actual current interruption process that turn-off failure is most likely, and this will result in permanent damage to the GTO. Limitation of the voltage spike peak at this time and the internal switching losses generated within the device, is vital.*

*The test results give a wide perspective on GTO thyristor switching behaviour and performance, and generally confirm the theory presented earlier.*



## CHAPTER 3

### Stray Inductance Effects in the DC Chopper Circuit

#### 3.1 Introduction

*It is generally necessary to connect a snubber circuit across the GTO thyristor to absorb the energy of the circuit inductances and limit the resulting voltage overshoot and rate of rise ( $dv/dt$ ), during the turn-off interval. The difficulties of coping with the induced voltage transients produced by high rates of change of current when switching GTO thyristors are formidable. As the stray inductances are directly dependent on the power circuit configuration, the layout of the power components and their interconnection is of the utmost importance. The stray inductance within the gate drive circuit is also important.*

*In this chapter, a detailed analysis and computer simulation model are presented to show the relative importance of the various lumped circuit path stray inductances in generating these overshoot voltages in the DC step-down chopper circuit with resistive and resistive-inductive loads. GTO thyristor peak currents of up to 600 A are switched.*

#### 3.2 Approach for Circuit Modelling

*This section outlines some of the available methods for analysing transient and/or steady-state performance of electrical circuits, and presents the one adopted in this thesis.*

*Basically, the equations representing the behaviour of the circuit at defined time intervals (the state equations), are produced using any of several methods that utilise Ohm's law and Kirchhoff's voltage and current laws, these then being solved by an appropriate technique.*

*The above laws may be combined to produce circuit theorems such as Norton's, Thevenin's and Superposition.*

##### 3.2.1 Network analysis techniques

*The following distinct approaches for network analysis are, in general, applied to electrical circuits having (b) branches and (n) nodes. If a set of (n-1) simultaneous equations are obtained in which the variables are voltages, this is known as nodal analysis. If a set of (b-n+1) simultaneous equations are obtained in which the variables*

*are currents, this is known as mesh analysis. Networks known as non-planar [23] (where a planar circuit is one which can be drawn in the plane such that there is no element crosses over another) cannot be treated with mesh analysis; however a similar approach, loop analysis, can be used in which the variables are again currents.*

*Finally, there is branch current analysis where a set of (b) equations may be solved for the branch currents. The approach which gives fewest equations is often chosen.*

*The equations defining the circuit usually change with time. The simple chopper circuit has, for one time interval, a maximum of six branches and four nodes involved; this produces 3, 3 and 6 equations by utilising the above approaches respectively. More complex circuits need more equations, and in all cases mesh analysis needs fewer equations than nodal and branch current analysis. Hence, the former is used throughout this work.*

### **3.2.2 Solution of circuit equations**

*Having obtained the state equations, the best method for their solution is needed. Energy storage elements, inductors and/or capacitors, if present in the circuit, lead to a set of first or second order differential equations. These may be solved analytically by the Laplace transformation or by numerical methods. The Laplace method allows standard transformations, and the inverse, to be used for many time domain functions such as step, ramp and sinusoid. The technique becomes very complex as the number of branches and energy storage elements in a circuit topology increases. A numerical method using a digital computer becomes essential for all but the simplest circuits.*

*Solutions using numerical techniques can use either a multi-step or single-step method or both. The former, such as those of Milne, Adams and Adams-Moulton [21], uses information computed about the function and its derivative from the previous steps, as well as the last, to construct a polynomial that approximates to the function, and extrapolates this into the next interval. The construction of the polynomial is eased by the use of equal step-lengths (h).*

*The single-step method, such as Euler, modified Euler and Runge-Kutta [21], uses only the information computed from the last step, thus allowing the next calculation to be performed with a different step-length. These methods are ideal to a solution where the initial conditions are available. When the electrical circuit changes state, the new set of*



equations take the results from the last calculated step as the initial condition for the new circuit topology.

A single-step method is chosen in this thesis, as the circuits being modelled incorporate different conduction patterns per cycle. Although a multi-step technique in conjunction with a single-step method at the start of each new conduction pattern could have been used, the choice of a single-step method achieves a faster overall solution. The highest accuracy is obtained by the 4th order Runge-Kutta method, where the truncated solution error is proportional to the step-length to the power of five ( $h^5$ ), whence for those of Euler and modified Euler methods, is proportional to the square of the step-length ( $h^2$ ) [24].

For the 4th order Runge-Kutta method, the algorithm is:

$$y_{n+1} = y_n + \frac{1}{6} ( K_1 + 2K_2 + 2K_3 + K_4 ) \quad (3.1)$$

where

$$K_1 = hf(x_n, y_n)$$

$$K_2 = hf(x_n + \frac{h}{2}, y_n + \frac{K_1}{2})$$

$$K_3 = hf(x_n + \frac{h}{2}, y_n + \frac{K_2}{2})$$

$$K_4 = hf(x_n + h, y_n + K_3)$$

and  $h$  is the integration step-length.

Summarising the technique, an electrical circuit with energy storage elements can be described by a set of first order differential equations whose variables (voltages and currents), are called the state variables. These state equations can be written as a single matrix state equation of the form:

$$\frac{dX(t)}{dt} = AX(t) + Bw(t) \quad (3.2)$$



where  $X(t)$  is the state vector,  $w(t)$  results from the input and  $A$  and  $B$  are some coefficient.

The integration step-length ( $h$ ) is selected using a trial and error method. A value is chosen and tried, then if half this value, when used in the same program, produces nearly identical results, the first is used. In this thesis, the values used range between 1-15ns. The following simplifying assumptions are made for the chopper circuit modelling, the general computation flow diagram of which is shown in Figure 3.1.

- a) The switching device itself is taken as a non-ideal switch but having the terminal characteristics representing the GTO thyristor in the circuit;
- b) Diode reverse recovery is allowed for, the 'snap-off' of reverse current being instantaneous;
- c) Mutual inductive coupling effects are neglected.

### 3.3 GTO Thyristor Turn-Off in a Chopper with Resistive Load

#### 3.3.1 Turn-off time intervals

The GTO thyristor turn-off waveforms are shown, sketched in Figure 3.3 for a chopper with resistive load (Figure 3.2(a)), the various time intervals being indicated. The equivalent circuits and their corresponding state equations, appropriate to the GTO thyristor current fall time ( $t_f$ ), voltage overshoot time ( $t_{os}$ ), snubber diode reverse recovery time ( $t_{rr}$ ) and voltage undershoot time ( $t_{us}$ ), are shown in Figure 3.4(a), (b), (c) and (d) respectively. This section gives the important results related to each time interval.

#### a) Storage time ( $t_s$ )

Here, charge is being removed by the <sup>negative gate</sup> rising  $i_A$  current prior to the commencement of the anode current fall. The snubber circuit is shorted by the conducting GTO thyristor.

#### b) Fall time ( $t_f$ )

During the rapid anode current fall, with assumed loop currents  $i_T$  and  $i_s$  flowing (Figure 3.4(a)), rising current  $i_s$  opposes the  $i_T$  in the GTO until at the end of the fall

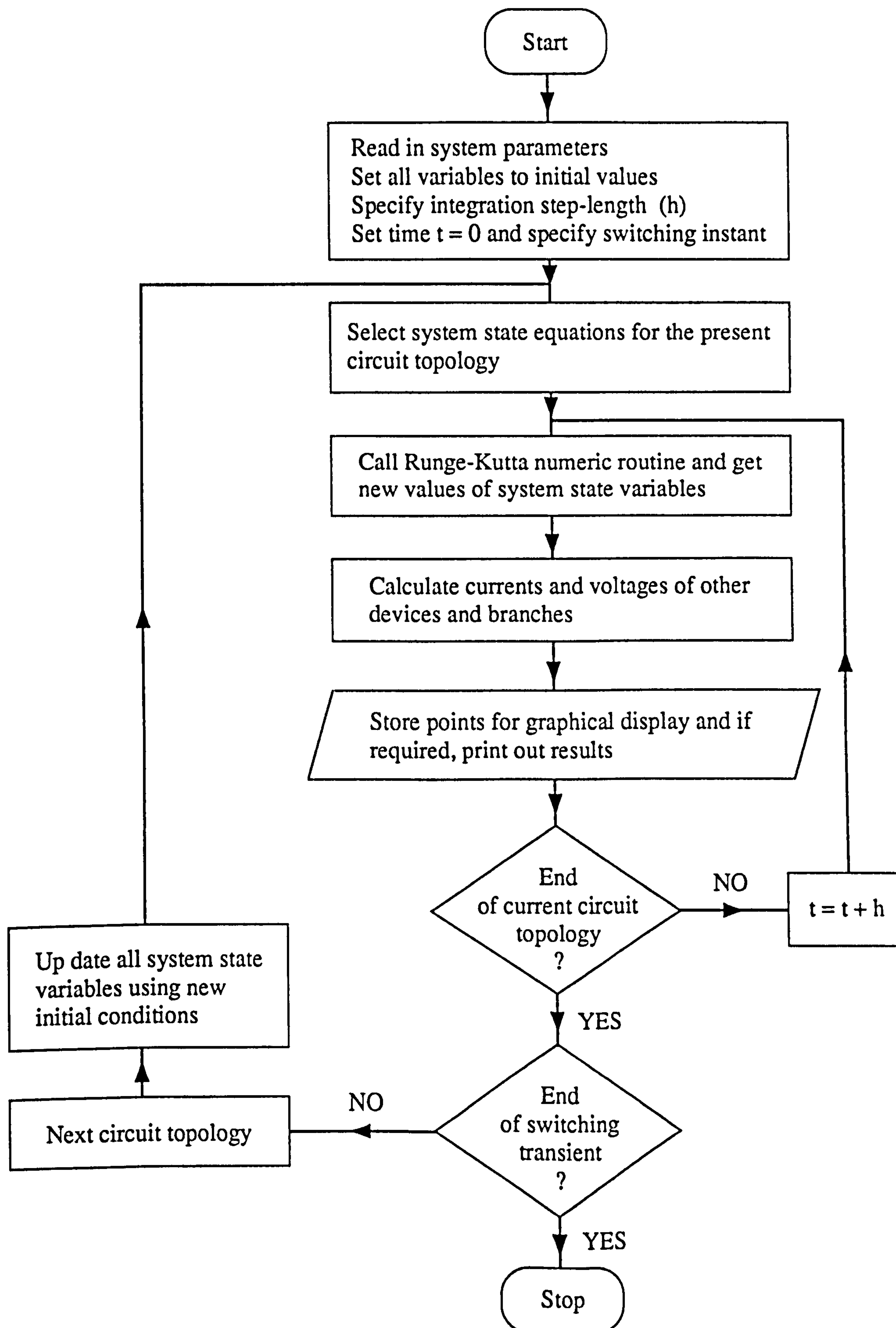
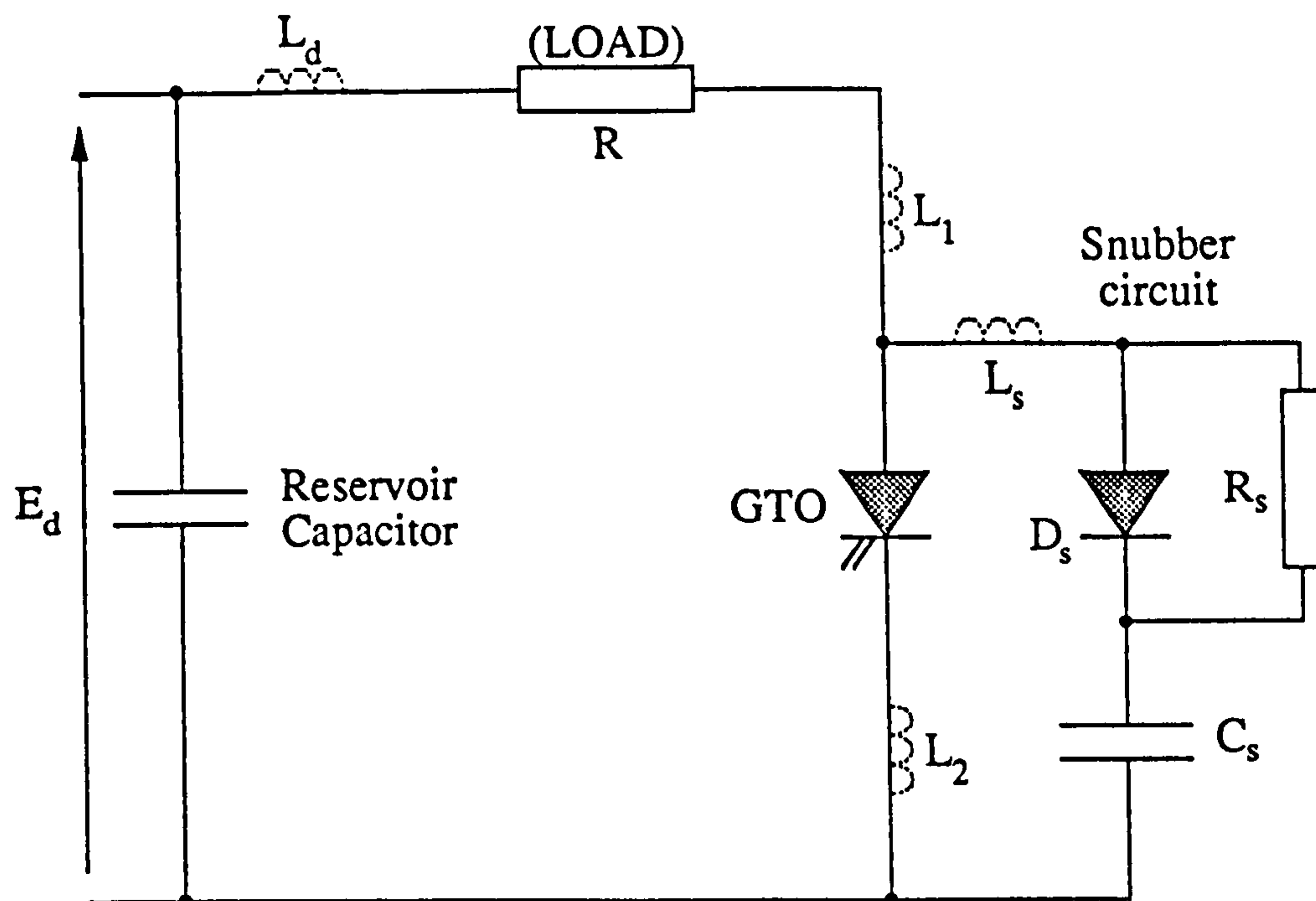
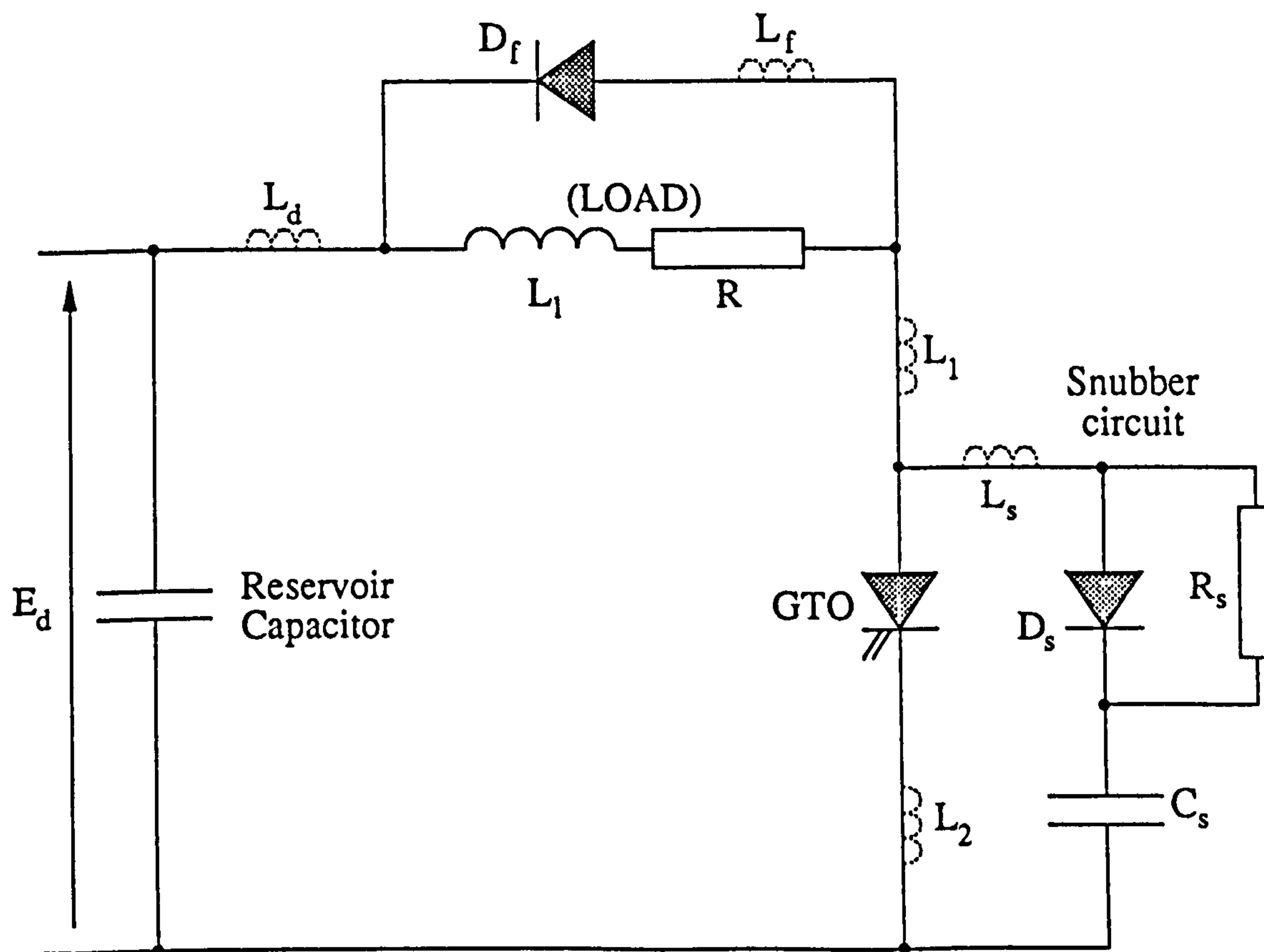


Figure 3.1 The general flow chart for the numerical analysis



(a) Chopper with resistive load



(b) Chopper with inductive load

Figure 3.2 Chopper circuits with stray inductances shown in dashed lines



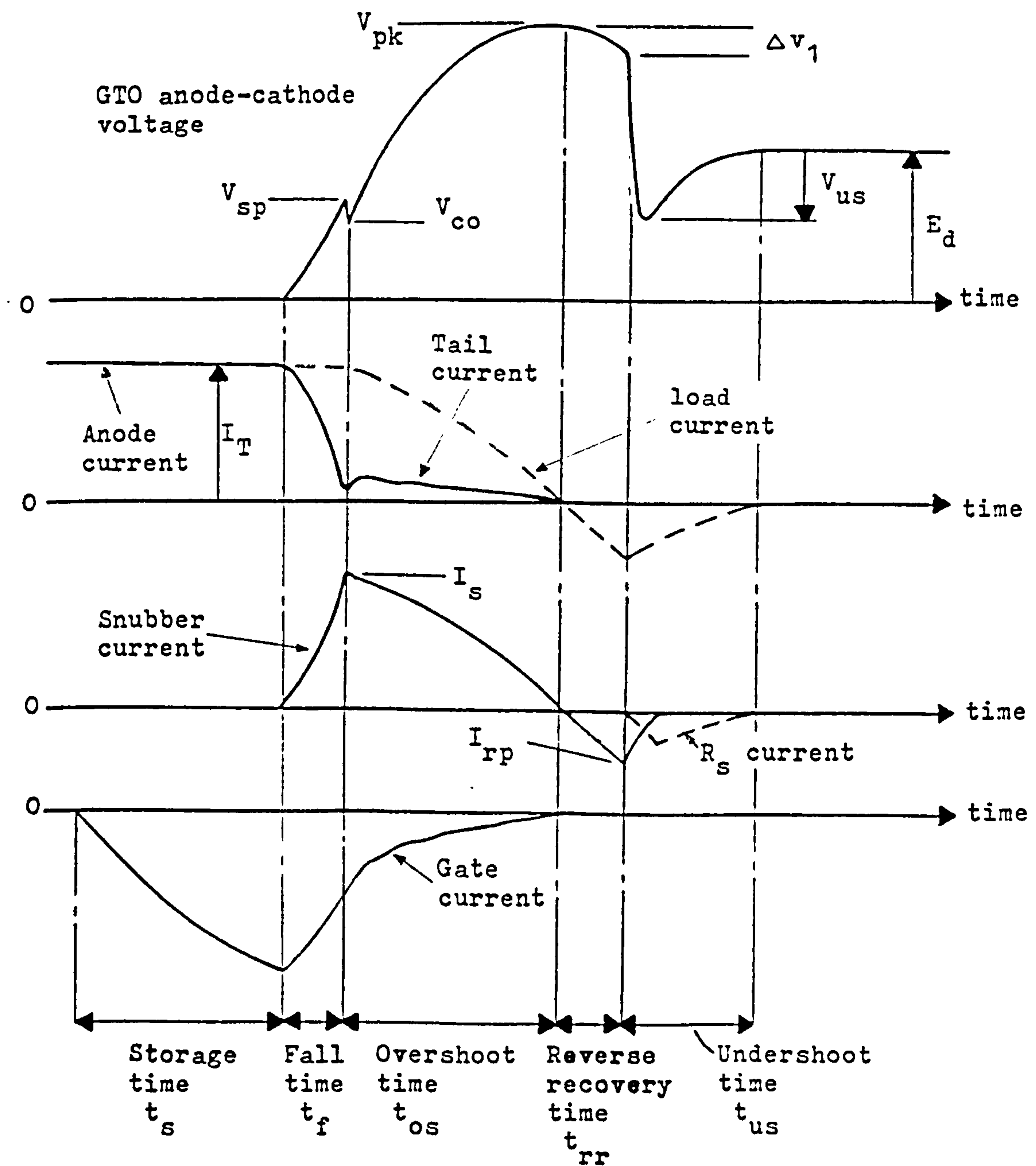
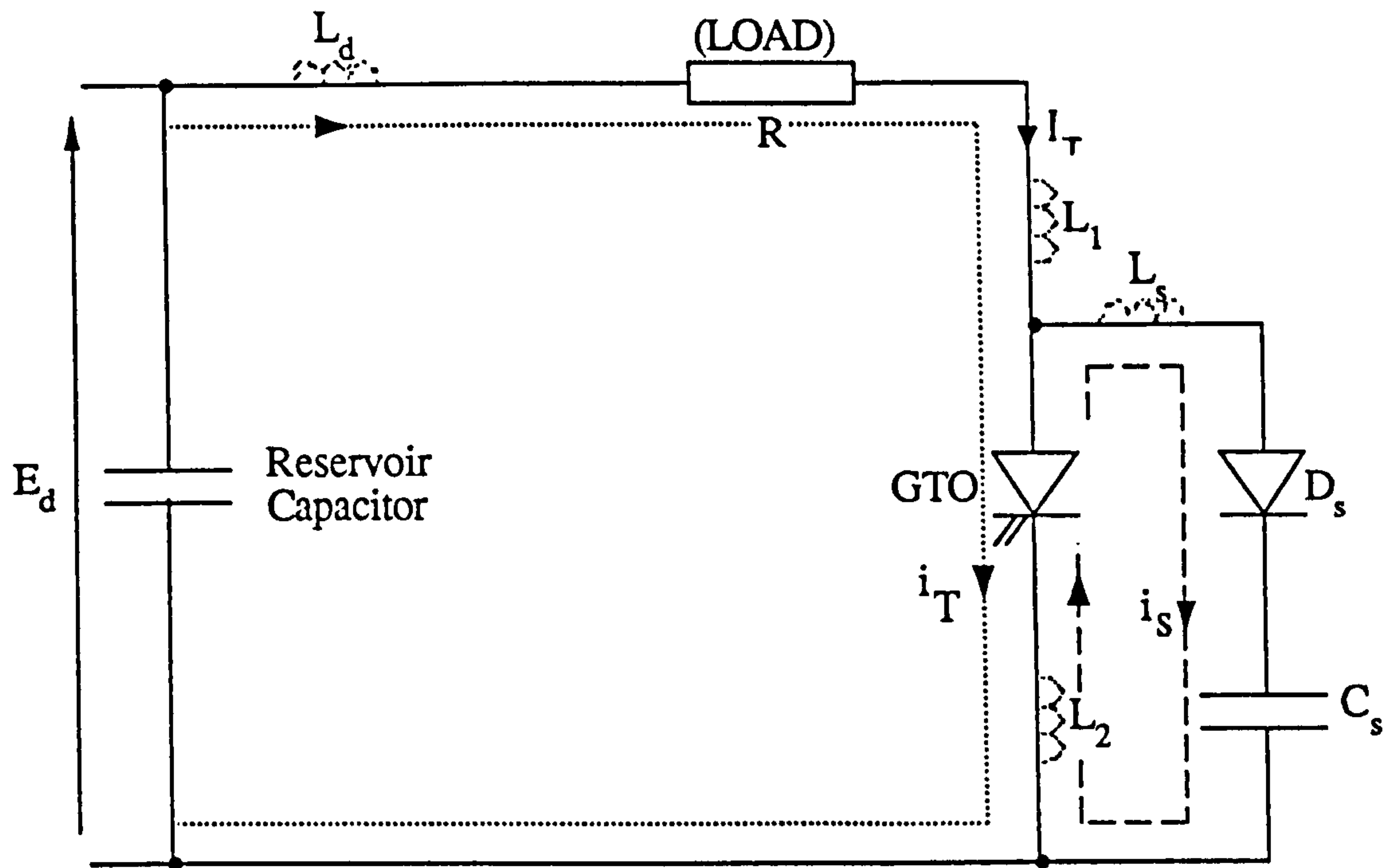


Figure 3.3 Sketched waveforms at GTO thyristor turn-off in chopper with resistive load



The anode current fall with time ( $t$ ) is represented by equation (3.11), but the tail current is not neglected, i.e.

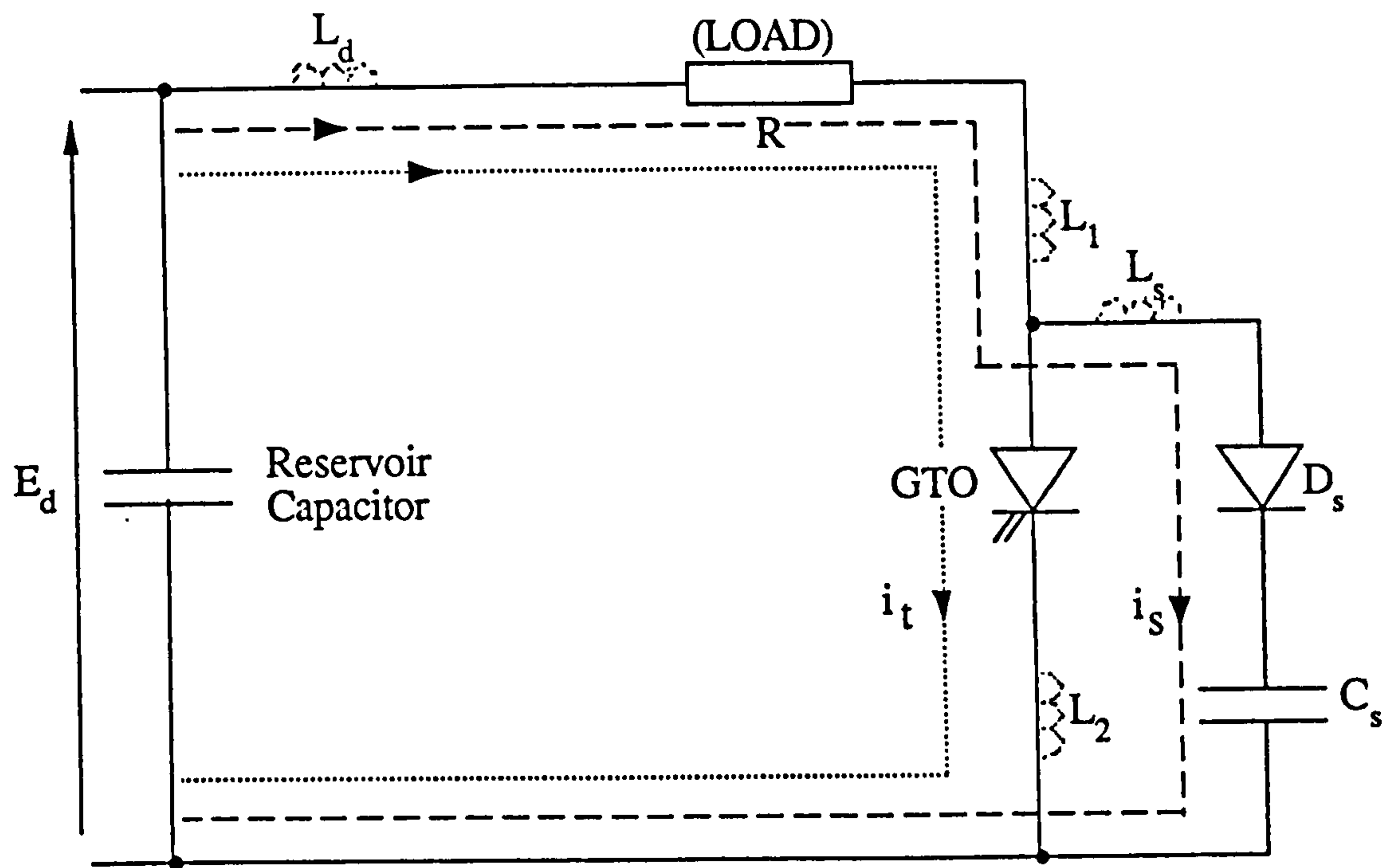
$$i_T = I_T \left( 1 - \frac{t^2}{T_0^2} \right)$$

$$T_0 = \frac{t_f}{\sqrt{1 - \left( \frac{I_T}{I_t} \right)}}$$

and  $i_s = I_T - i_T$

(a) During fall time ( $t_f$ )

Figure 3.4 Equivalent circuits and state equations of the GTO turn-off time intervals in chopper with resistive load.



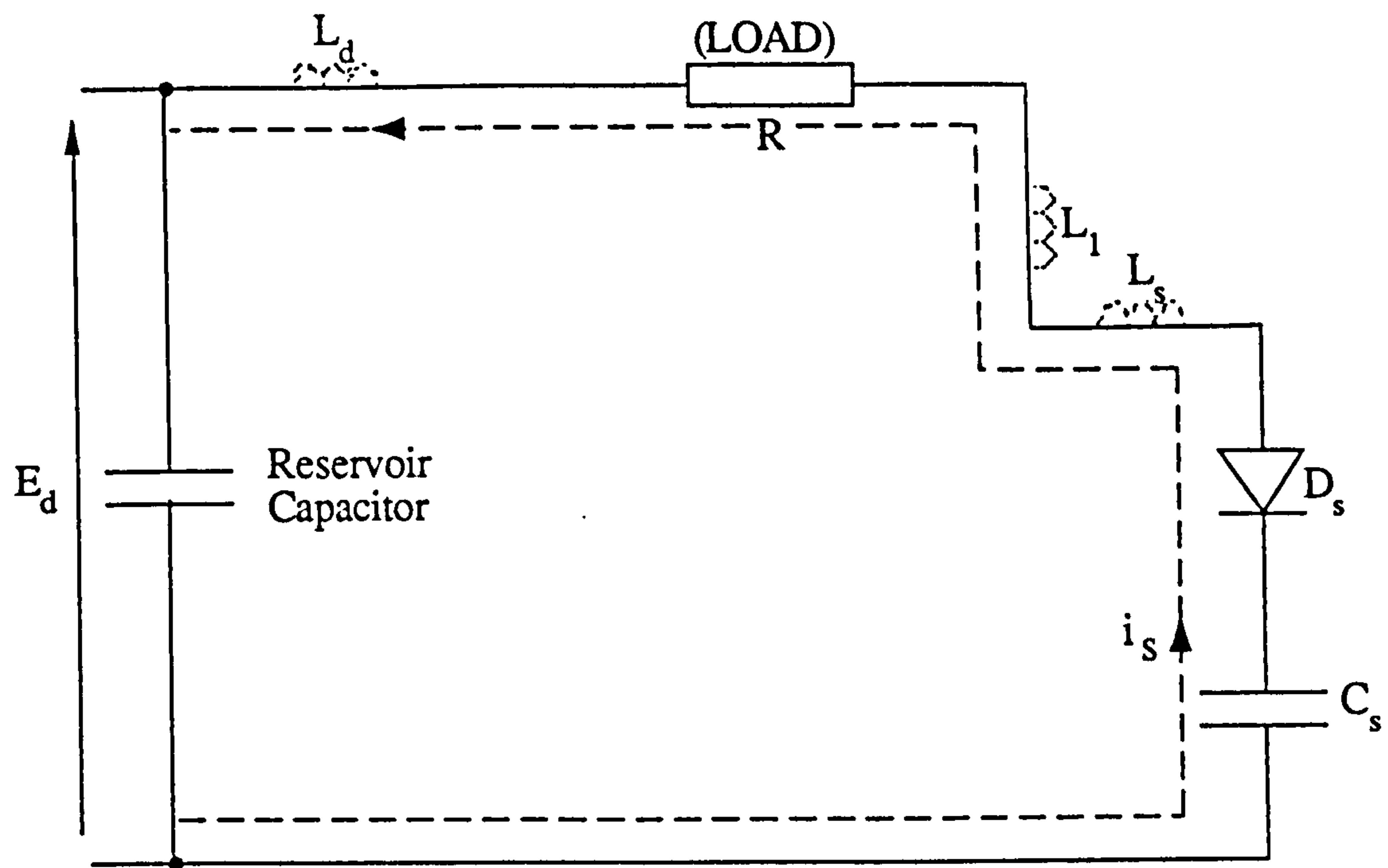
$$\begin{bmatrix} p i_s \\ p i_t \\ p v_c \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & -\frac{R}{L} & -\frac{1}{L} \\ 0 & 0 & 0 \\ \frac{1}{C_s} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_s \\ i_t \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{E_d t_{os} + 0.2 L_T L_4}{t_{os} L} \\ -0.2 \frac{L_T}{t_{os}} \\ 0 \end{bmatrix}$$

$$t_{os} \approx \frac{\pi}{2} \sqrt{LC_s}$$

(b) During voltage overshoot time ( $t_{os}$ )

Figure 3.4 Equivalent circuits and state equations of the GTO turn-off time intervals in chopper with resistive load.

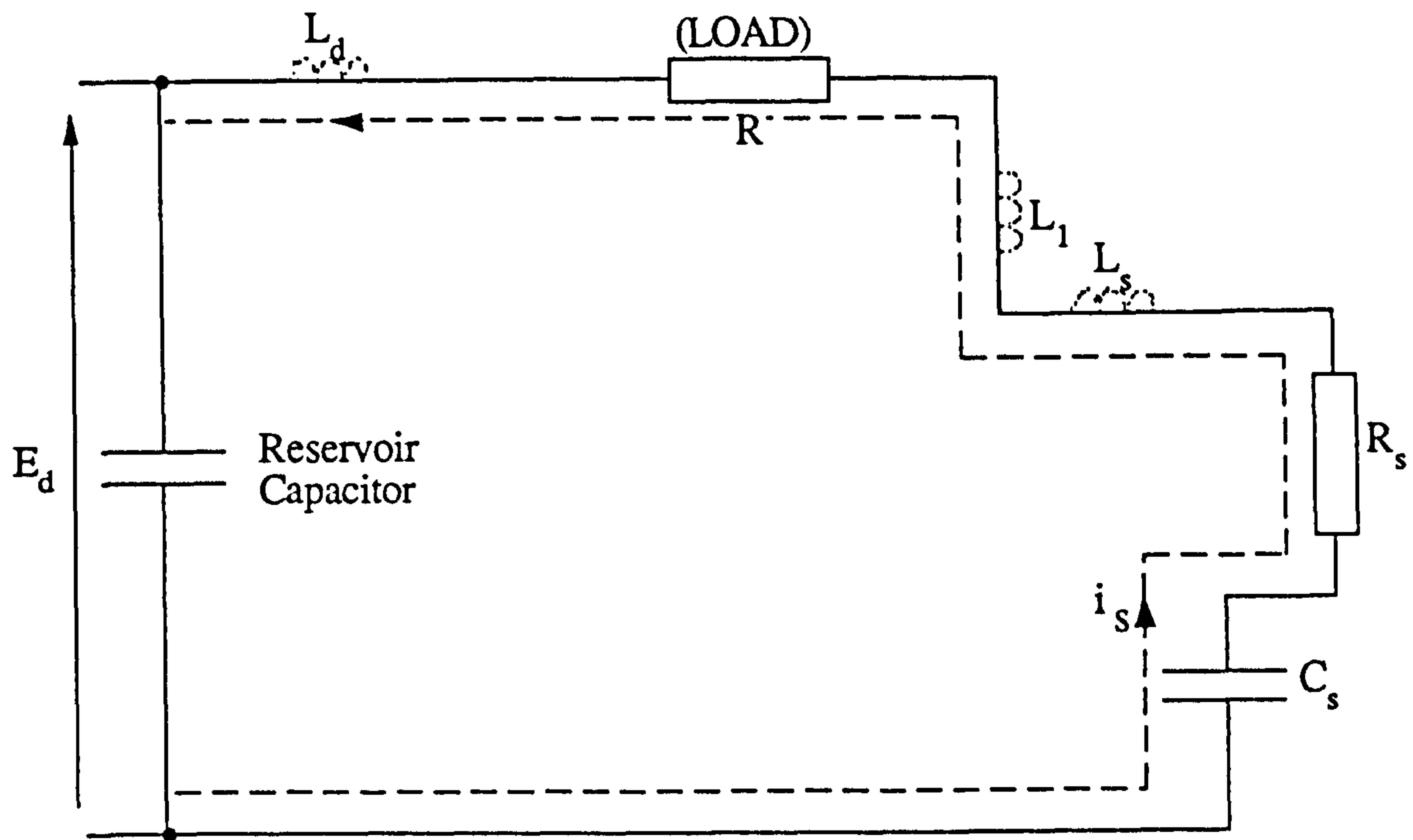




$$\begin{bmatrix} p i_s \\ p v_c \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & \frac{1}{L} \\ \frac{1}{C_s} & 0 \end{bmatrix} \begin{bmatrix} i_s \\ v_c \end{bmatrix} + \begin{bmatrix} -\frac{E_d}{L} \\ 0 \end{bmatrix}$$

(c) During snubber diode reverse recovery time ( $t_{rr}$ )

Figure 3.4 Equivalent circuits and state equations of the GTO turn-off time intervals in chopper with resistive load.



$$\begin{bmatrix} p i_s \\ p v_c \end{bmatrix} = \begin{bmatrix} -\frac{(R + R_s)}{L} & \frac{1}{L} \\ \frac{1}{C_s} & 0 \end{bmatrix} \begin{bmatrix} i_s \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{E_d}{L} \\ 0 \end{bmatrix}$$

(d) During voltage undershoot time ( $t_{us}$ )

Figure 3.4 Equivalent circuits and state equations of the GTO turn-off time intervals in chopper with resistive load.

time it has risen to approximately the  $I_T$  value, completely cancelling it apart from the small tail current, which has a maximum value of about 10% to 20% of the interrupted current before decaying. The remaining (say 90%) of the load current is diverted into the snubber. This interval is less than  $1\mu S$ , and if it is assumed that the DC source current remains constant for this time, then the rising rate of  $i_s$  is equal to the falling GTO current rate. The falling GTO current has the rough shape of the first quarter of a cosine curve [14,15,18]. Letting this be

$$i_T = I_T \cos \omega t \quad (3.3)$$

where  $I_T$  is the maximum interrupted current, then

$$i_s = I_T - i_T = I_T(1 - \cos \omega t) \quad (3.4)$$

Also

$$\frac{di_s}{dt} = I_T \omega \sin \omega t \quad (3.5)$$

and

$$\int_0^t i_s dt = I_T \left[ t - \frac{1}{\omega} \sin \omega t \right]_0^t \quad (3.6)$$

The induced voltage spike is produced by the rising  $i_s$  current, flowing through the snubber loop stray inductance plus the accumulated voltage across the snubber capacitor  $C_s$ . Also, as the forward recovery voltage ( $V_{ds}$ ) across the snubber diode contributes to the voltage spike, then:

$$v_{sp} = (L_2 + L_s) \frac{di_s}{dt} + \frac{1}{C_s} \int i_s dt + v_{ds} \quad (3.7)$$

If desired,  $V_{ds}$  may be modelled approximately by an induced voltage transient across a small inductance, whose value can be estimated from  $V_{ds}/(di_s/dt)$ , where  $V_{ds}$  is a measured value.

Using equations 3.5 and 3.6 in 3.7 gives



$$v_{sp} = (L_2 + L_s) I_T \omega \sin \omega t + \frac{I_T}{C_s} \left( t - \frac{\sin \omega t}{\omega} \right) + v_{ds} \quad (3.8)$$

where  $\omega = 2\pi/T$ , with  $T = 4 t_f$  giving  $\omega = \pi/2 t_f$ .

Theoretically, the maximum  $di_s/dt$  occurs when  $t = t_f$ , and  $\sin \omega t = 1$ . In practice, the spike voltage occurs when  $t = 0.8t_f$  approximately, giving  $\sin \omega t = 0.95$ . The peak capacitor current is  $0.9I_T$ . The peak spike voltage is therefore, with these empirical approximations:

$$V_{sp} = 1.4 (L_2 + L_s) \frac{I_T}{t_f} + 0.18 \frac{I_T t_f}{C_s} + V_{ds} \quad (3.9)$$

When the spike collapses,  $t = t_f$  and the accumulated voltage across  $C_s$  is:

$$\begin{aligned} v_{co} &= \frac{1}{C_s} \int_0^{t_f} i_s dt \\ &= \frac{0.3 I_T t_f}{C_s} \end{aligned} \quad (3.10)$$

Possibly a more accurate representation of the GTO thyristor current is the empirical approximate relationship [16].

$$i_T = I_T \left( 1 - \frac{t^2}{t_f^2} \right) \quad (3.11)$$

$$i_s = I_T - i_T = I_T \frac{t^2}{t_f^2} \quad (3.12)$$

Deriving the equivalent relationships to those above:

$$\frac{di_s}{dt} = 2 I_T \frac{t}{t_f^2} \quad (3.13)$$

and

$$\int_0^t i_s dt = \frac{I_T t^3}{3 t_f^2} \quad (3.14)$$

Therefore, for  $t = 0.8 t_f$  and peak  $i_s = 0.9 I_T$

$$V_{sp} = 1.6 (L_2 + L_3) \frac{I_T}{t_f} + 0.15 \frac{I_T t_f}{C_s} + V_{ds} \quad (3.15)$$

For  $t = t_f$

$$V_{co} = \frac{0.3 I_T t_f}{C_s}$$

as equation (3.10)

### c) Voltage overshoot time ( $t_{os}$ )

The anode current is now diverted into the snubber circuit and falls in a cosinusoidal form as  $C_s$  is charged oscillatorily from  $V_{co}$  to a peak value  $V_{pk}$  which overshoots the DC supply voltage due to the stored energy in the stray inductances in the charging current path ( $L_d + L_1 + L_s$ ), Figure 3.4(b). The charging current is given by (Appendix I).

$$i_s = I_s \sqrt{1 + \tan^2 \alpha} e^{-bt} \cos(\omega t - \alpha) \quad (3.16)$$

where

$$b = \frac{R}{2L}, \omega^2 = \frac{1}{LC_s} - b^2, \tan \alpha = \left( \frac{E_d - V_{co}}{I_s \omega L} - \frac{b}{\omega} \right)$$

and the effective inductance  $L = L_d + L_1 + L_s$ .

The initial snubber current,  $I_s$ , is about 90% of the interrupted anode current  $I_T$  owing to the tail current. The overshoot oscillation time  $t_{os}$  is obtained when  $i_s = 0$ , that is

$$\cos (\omega t_{os} - \alpha) = 0$$

giving

$$\omega t_{os} = \frac{\pi}{2} + \alpha \quad (3.17)$$

The peak capacitor voltage is given when  $t = t_{os}$ , by

$$V_{pk} = I_s \sqrt{1 + \tan^2 \alpha} \sqrt{\frac{L}{C}} [e^{-bt_{os}} \sin (\omega t_{os} - \alpha - \beta) + \sin (\alpha + \beta)] + V_{co} \quad (3.18)$$

where  $\tan \beta = b/\omega$

Alternatively, the peak voltage can be obtained from the energy consideration [14,15,18] (Appendix I):

$$\frac{1}{2} C_s V_{pk}^2 = \frac{1}{2} L I_s^2 + \frac{1}{2} C_s V_{co}^2 + \frac{2}{\pi} E_d I_s t_{os} - \frac{1}{2} I_s^2 R t_{os} \quad (3.19)$$

where very approximately,  $\omega t_{os} = \pi/2$ , and the derivation of the equation is based on this assumption.

#### d) Snubber diode reverse recovery time ( $t_{rr}$ )

After the current zero, the snubber capacitor commences to discharge from its peak voltage back into the DC supply. Initially, this is through the snubber diode  $D_s$  reverse recovery; when completed, the reverse current will have risen to  $I_{rp}$ . If the diode is assumed to snap off instantaneously,  $I_{rp}$  is diverted into the snubber resistor  $R_s$ . It immediately falls, and the voltage across the GTO thyristor, given instantaneously by

$$V_{GTO} = V_c - i_s R_s$$

experiences a sudden reduction and possible undershoot with respect to the steady blocking voltage  $E_d$ . The subsequent  $dv/dt$ , as the GTO voltage rises to  $E_d$ , can be excessive [17] with the risk of parasitic GTO turn-on. Also, the undershoot may have a greater amplitude than  $E_d$ , giving a dangerous negative bias across the GTO thyristor unless clipped by an antiparallel diode.

The perturbation of the gate voltage and current, due to the gate-cathode junction stray capacitance, after the sudden fall of the GTO thyristor anode-cathode voltage, Figure 3.5, is undesirable as it could lead to misfiring if an adequate negative gate voltage is not applied. To minimise these effects:

- i)  $I_{rp}$  should be as low as possible, i.e. a fast but soft recovery snubber circuit diode is needed, this may conflict with the requirement for fast turn-on [9] in order to minimise the diode's forward recovery contribution  $V_{ds}$  to the voltage spike during  $t_f$  (equations 3.9 and 3.15).
- ii) The snubber circuit resistor should be as low as possible.

#### e) Voltage undershoot time ( $t_{us}$ )

If possible, it is best to ensure that voltage undershoot does not occur at all. For this, the two conditions given above must be met and ringing between  $C_s$  and the stray inductances must be at least critically damped.  $R_s$  must be sufficient to limit the discharge from  $C_s$  into the GTO thyristor at turn-on to a safe value, which will require a few ohms. This should then be increased if needed to give the required damping.

The snubber time constant ( $R_s C_s$ ) for the capacitor discharge into the GTO thyristor must be considerably less than the shortest GTO conduction period, thus allowing a complete discharge before GTO turn-off is attempted.

Now, with these conditions satisfied, the GTO voltage is

$$V_{GTO} = V_c - i_s R_s$$

and from Appendix I, with the effect of the stray inductances being negligible,



$$i_s = \frac{(V_{pk} - E_d)}{R_T} \exp \left( -\frac{t}{C_s R_T} \right) \quad (3.20)$$

$$v_c = (V_{pk} - E_d) \exp \left( -\frac{t}{C_s R_T} \right) + E_d \quad (3.21)$$

where  $R_T = R + R_s$  then

$$v_{GTO} = \frac{R}{R_T} (V_{pk} - E_d) \exp \left( -\frac{t}{C_s R_T} \right) + E_d \quad (3.22)$$

Again, the GTO voltage will be lower if  $R_s$  is high but this will not matter as there is no undershoot, Figure 3.5.

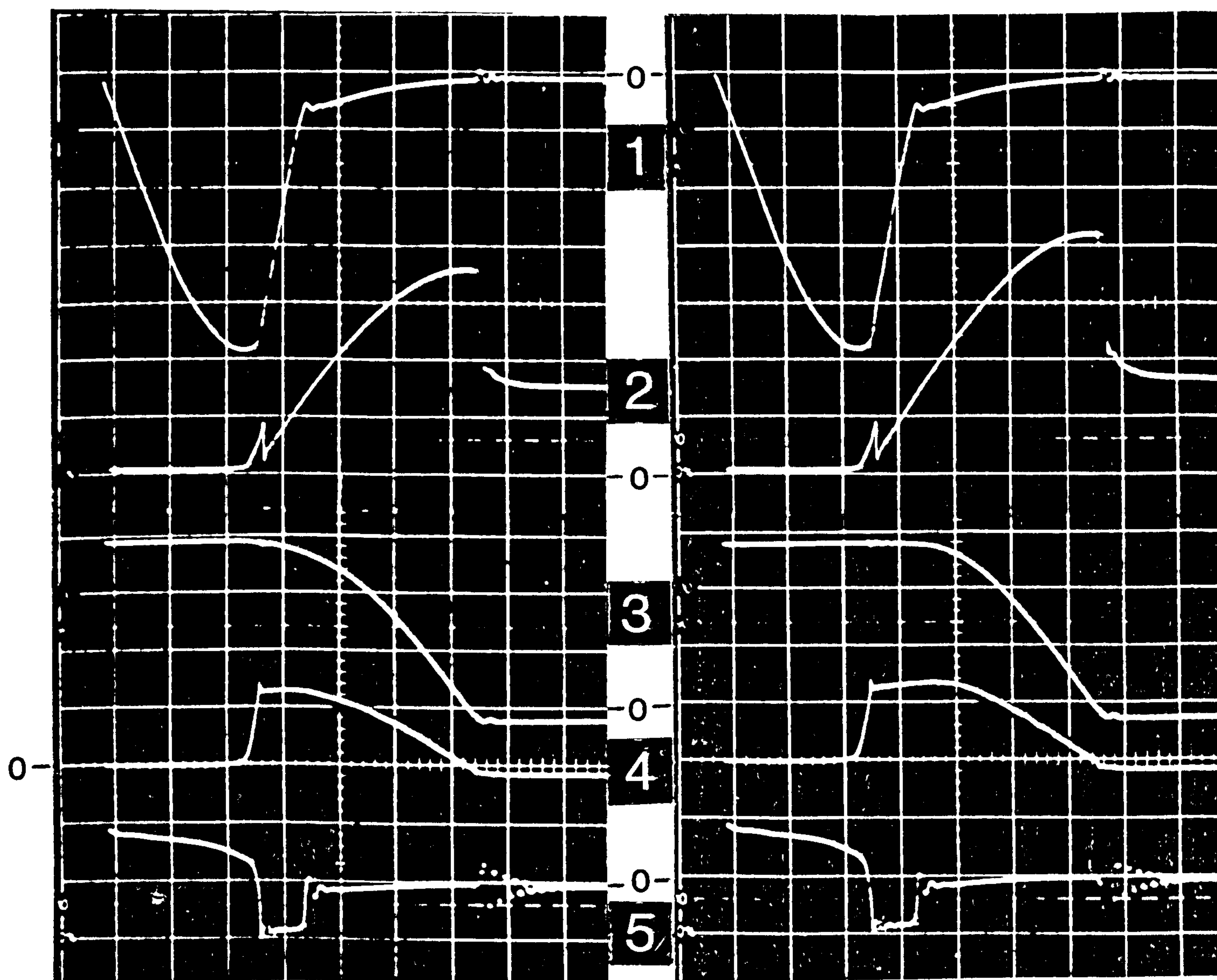
Points to note are that, although a fast recovery diode is used, there is a fairly sudden drop of voltage from  $V_{pk}$  due to the diversion of  $I_{rp}$  into  $R_s$  (from which  $I_{rp}$  can be estimated) before the exponential decay of voltage to the supply value  $E_d$ ; and, the fast recovery diode ensures little drop of voltage below  $V_{pk}$  before the diversion of current into  $R_s$  (i.e.  $\Delta V_r$  in Figure 3.3 is not noticeable).

### 3.3.2 Verifying Experimental Results

In order to verify the foregoing, a sample of predicted and measured results is given in Table 3.1 and Figure 3.6. The latter shows computed waveforms at the GTO thyristor turn-off in the chopper circuit. The stray inductances are difficult to predict, and have been measured where possible with a digital bridge at 1kHz, together with the load path resistance ( $R$ ).

Data:

Path inductance ( $L$ ) = ( $L_d + L_1 + L_s$ )	= 6.7 $\mu$ H	measured
Path resistance ( $R$ )	= 0.52 $\Omega$	measured
Snubber capacitance ( $C_s$ )	= 4 $\mu$ F (4X1 $\mu$ F nominal in parallel)	
Snubber resistance ( $R_s$ )	= 8 $\Omega$ (6X47 $\Omega$ nominal in parallel)	
Supply voltage ( $E_d$ )	= 312V	from CRO
Interrupted current ( $I_T$ )	= 600A	from CRO



(a) Resistive Load

(b) Inductive Load

(1) Gate Current	20A/div.
(2) GTO Voltage	200V/div.
(3) GTO + Snubber Current	200A/div.
(4) Snubber Current	400A/div.
(5) Gate Voltage	10V/div.

Time Scale: 2 $\mu$ S/div.

Figure 3.5 Waveforms at GTO thyristor turning-off 600A in choppers with resistive and inductive loads

Peak snubber current ( $I_s$ )	= 520A	from CRO
Snubber loop inductance ( $L_2 + L_s$ )	= 0.1 $\mu$ H	from CRO
Fall time (spike width) ( $t_f$ )	= 0.8 $\mu$ S	from CRO
Snubber diode forward recovery voltage ( $V_{ds}$ )	= 34V	from CRO

Quantity	Equation used	Calculated from equation	Computed value	Experimental value
Peak spike voltage ( $V_{sp}$ )	(3.15)	172V	175V	180V
Capacitor accumulated voltage ( $V_{co}$ )	(3.10)	36V	42V	50V
Overshoot time ( $t_{os}$ )	(3.17)	9.3 $\mu$ s	7.7 $\mu$ s	7.4 $\mu$ s
Overshoot time ( $t_{os} = \pi/2\omega$ )		8.3 $\mu$ s	7.7 $\mu$ s	7.4 $\mu$ s
Peak GTO voltage ( $V_{pk}$ )	(3.18)	788V	760V	720V
Peak GTO voltage ( $V_{pk}$ ) (with $t_{os} = \pi/2\omega$ )	(3.19)	786V	760V	720V
Peak GTO voltage ( $V_{pk}$ ) (with $t_{os}$ from eq. 3.8)	(3.19)	797V	760V	720V
Voltage across GTO at reverse recovery of the snubber diode	(3.22)	329V	220V	370V

Table 3.1 Calculated, computed and measured values for GTO turn-off in a chopper with resistive load

The correlation between predicted and measured results is good. The GTO snubber loop inductance is not measurable so a reasonable value is used, which relies to some extent



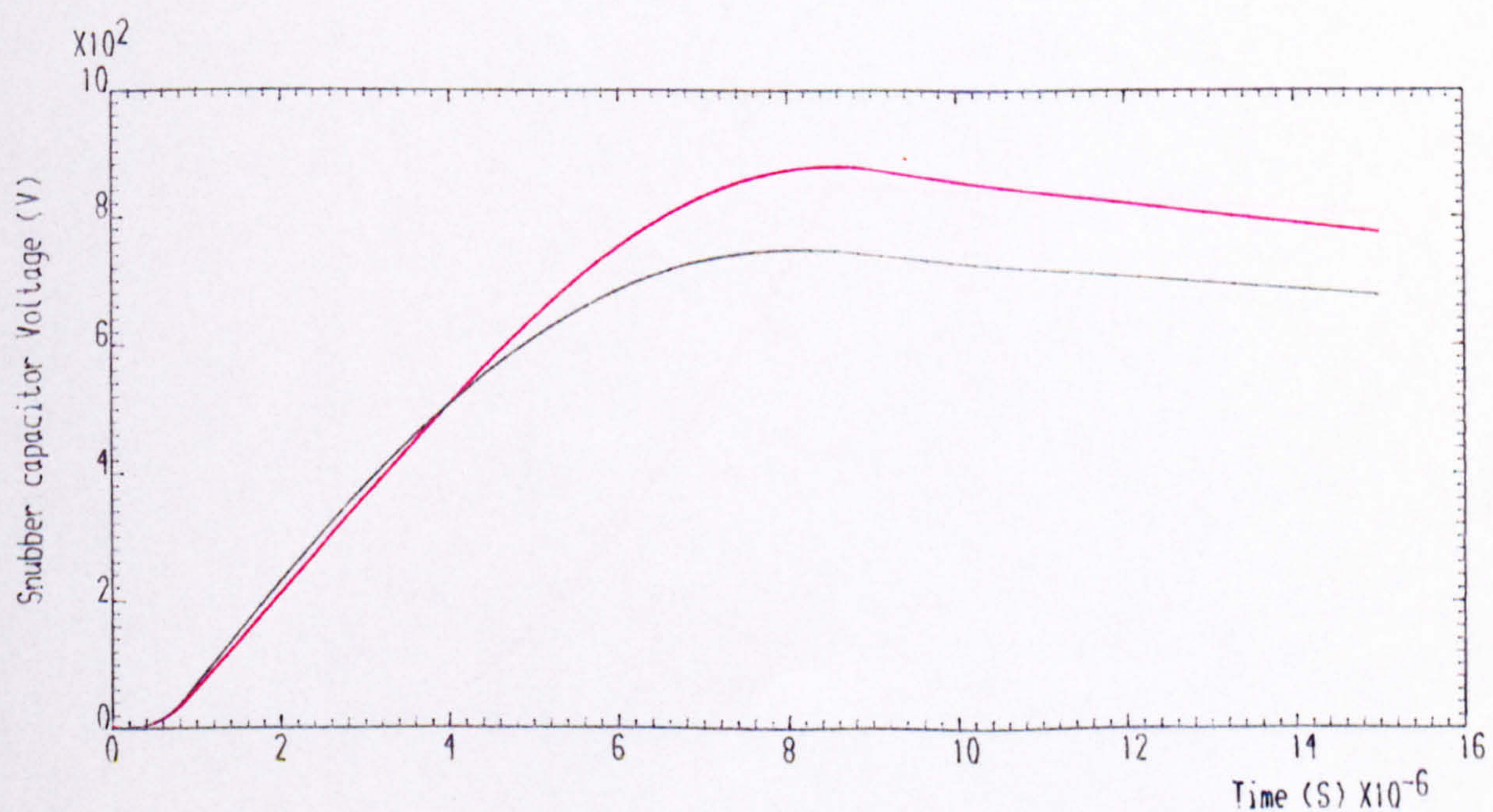
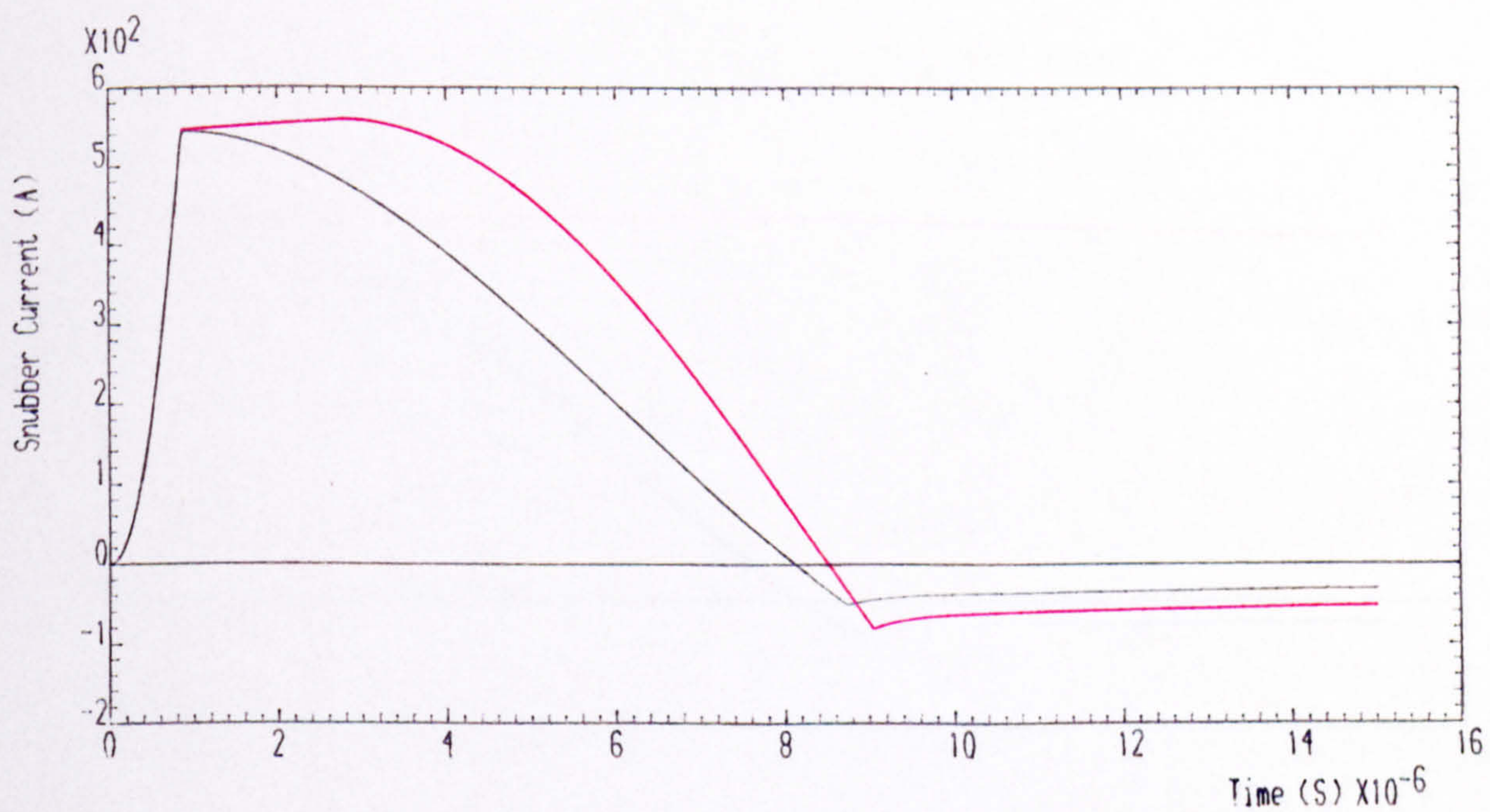
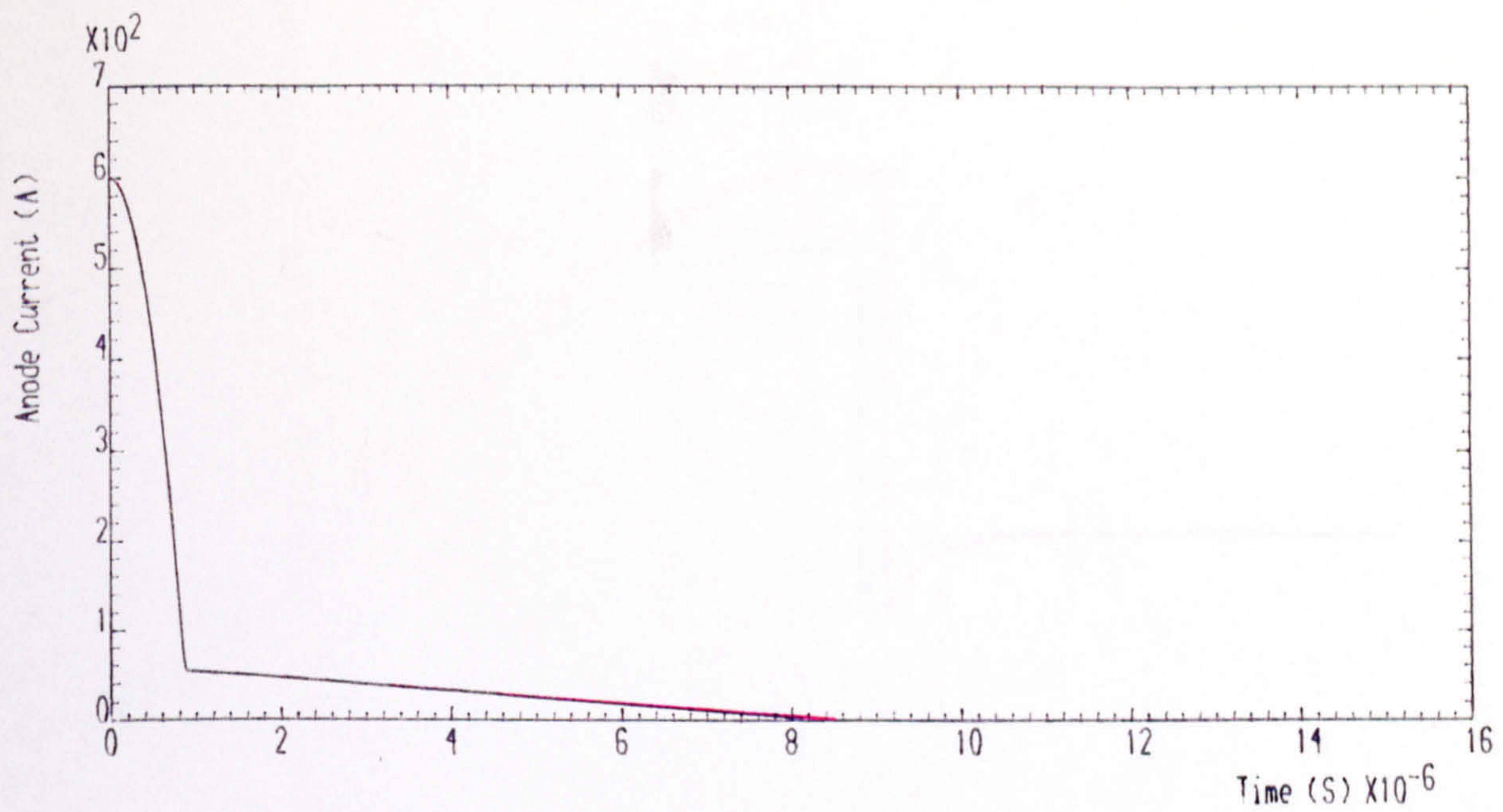


Figure 3.6 Computed waveforms at GTO thyristor turning off 600A (Black and Red traces are for R and R-L loads respectively) CONTINUED ..



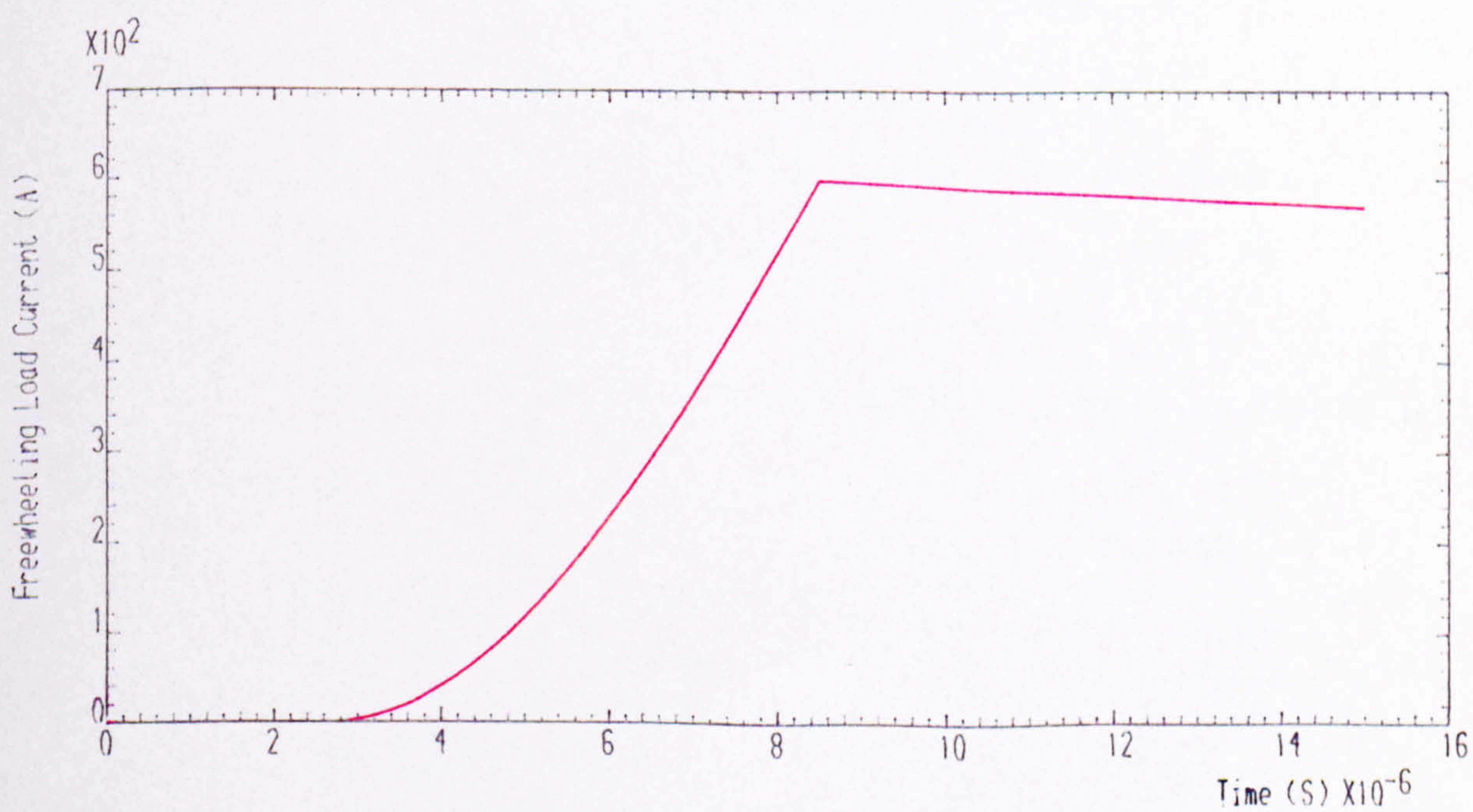
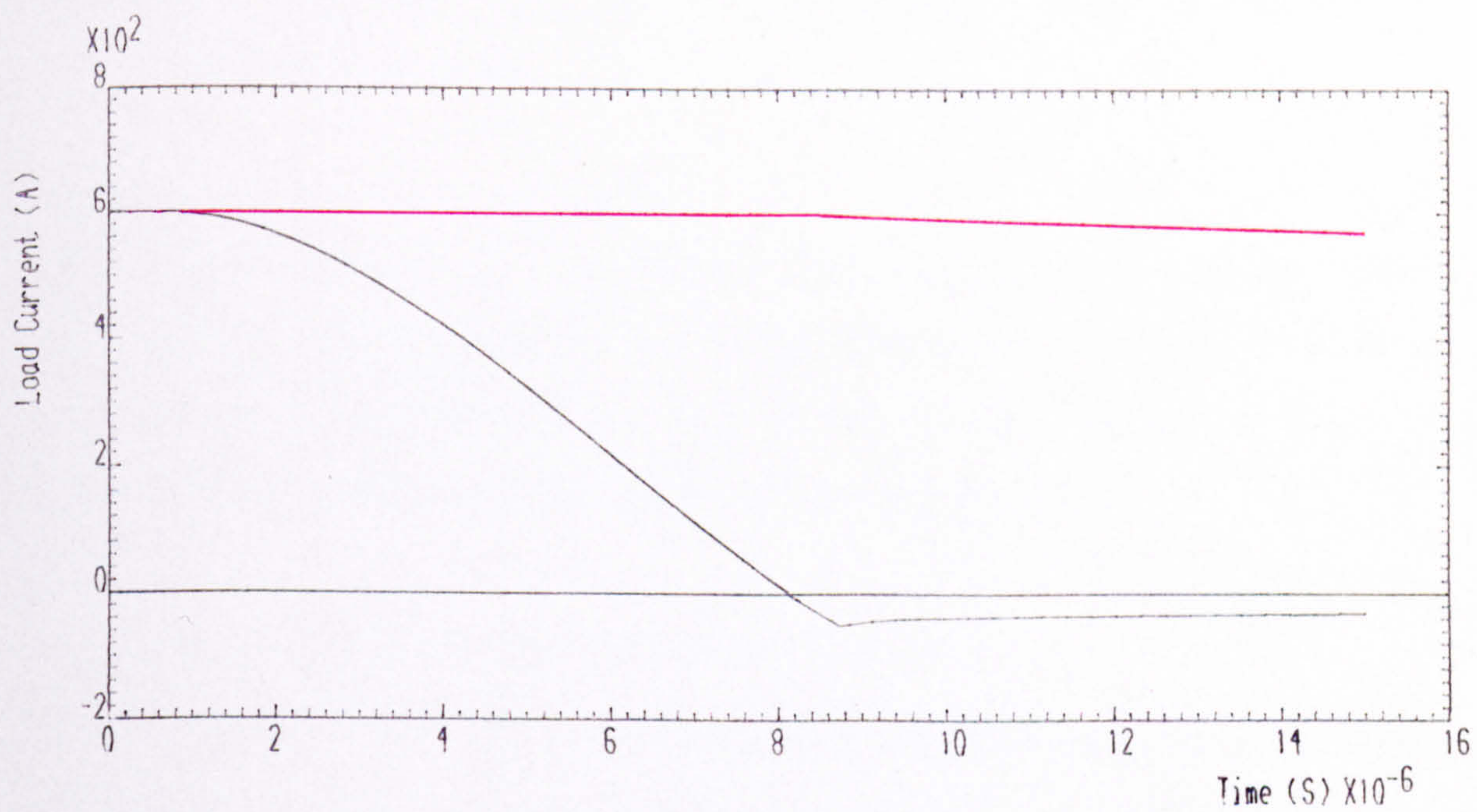
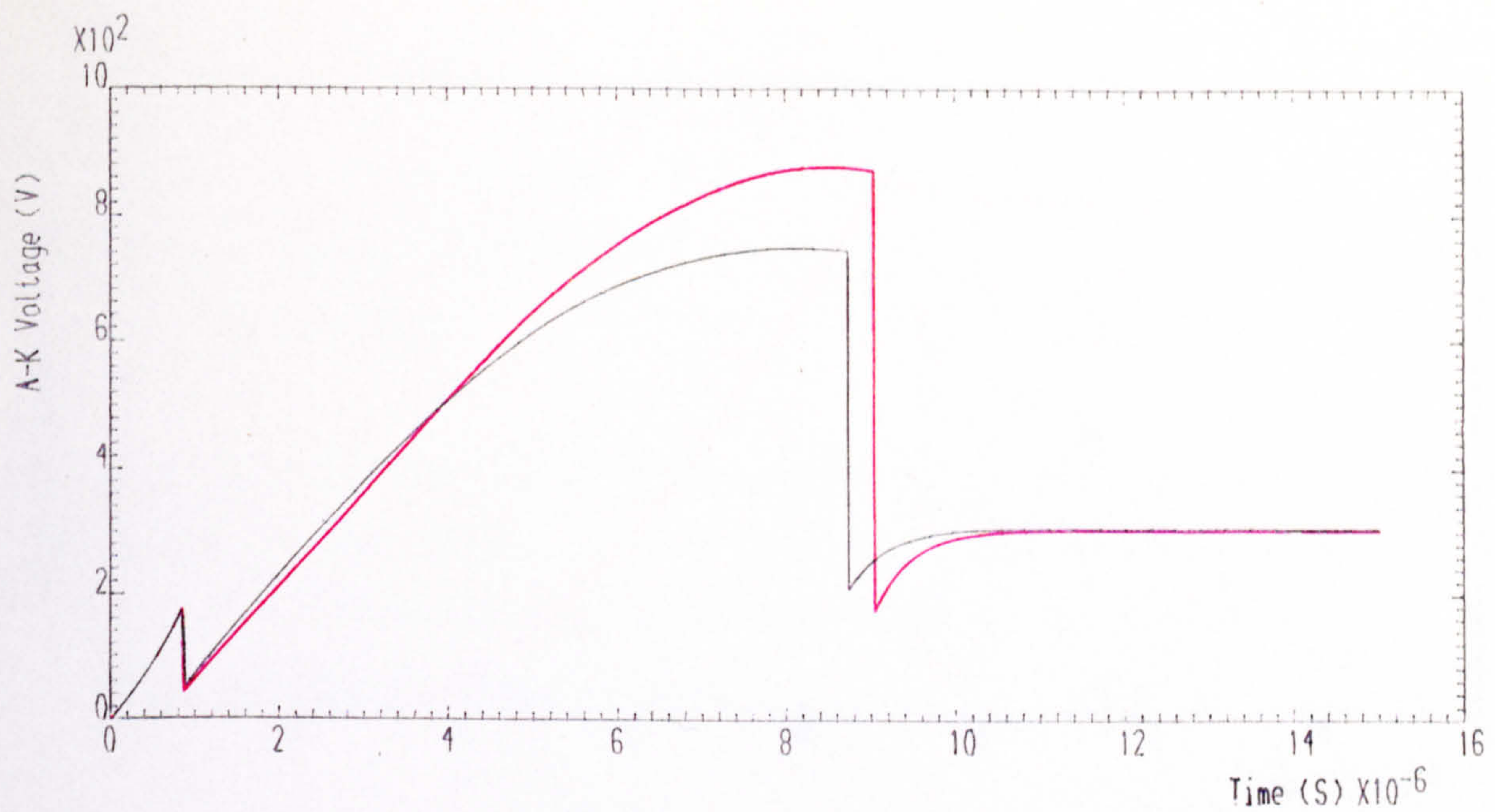


Figure 3.6 Computed waveforms at GTO thyristor turning off 600A (Black and Red traces are for R and R-L loads respectively)

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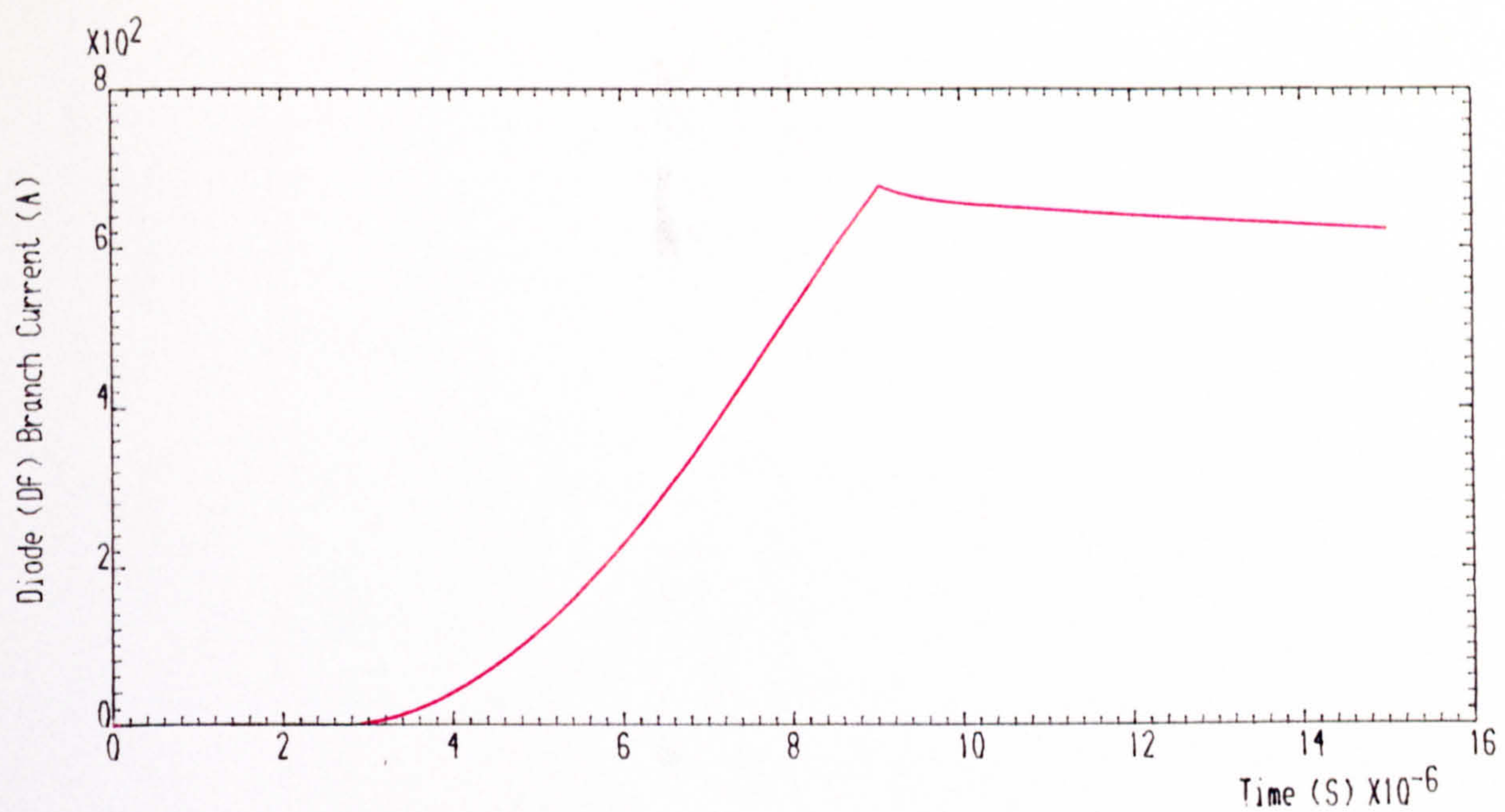


Figure 3.6 Computed waveforms at GTO thyristor turning off 600A (Black and Red traces are for R and R-L loads respectively) End ..



on the spike voltage observed. The calculated and computed voltage peaks are expected to be slightly higher than those measured since wiring resistance is neglected in the derivation of the state equations. The overshoot analysis is completely verified, and the calculated energy method is shown to give accurate results if  $t_{os}$  is estimated from the simple relationships.

The computed and observed waveforms compare, in general, very well. The assumption of snubber diode reverse recovery snap-off gives rise to differences, this being particularly demonstrated in Figures 3.5 and 3.6 where the computed voltage undershoot did not occur experimentally.

### 3.4 GTO Thyristor Turn-Off In a Chopper with Inductive Load and Freewheeling Path

#### 3.4.1 Turn-off time intervals

The turn-off process with an inductive load, Figure 3.2(b), although similar to that with resistive load, contains some important differences. However, referring to Figures 3.7 and 3.5, the storage time,  $t_s$ , and the fall time,  $t_f$ , intervals are identical for both types of load. The succeeding intervals are described below.

##### a) Near constant current charging time ( $t_c$ )

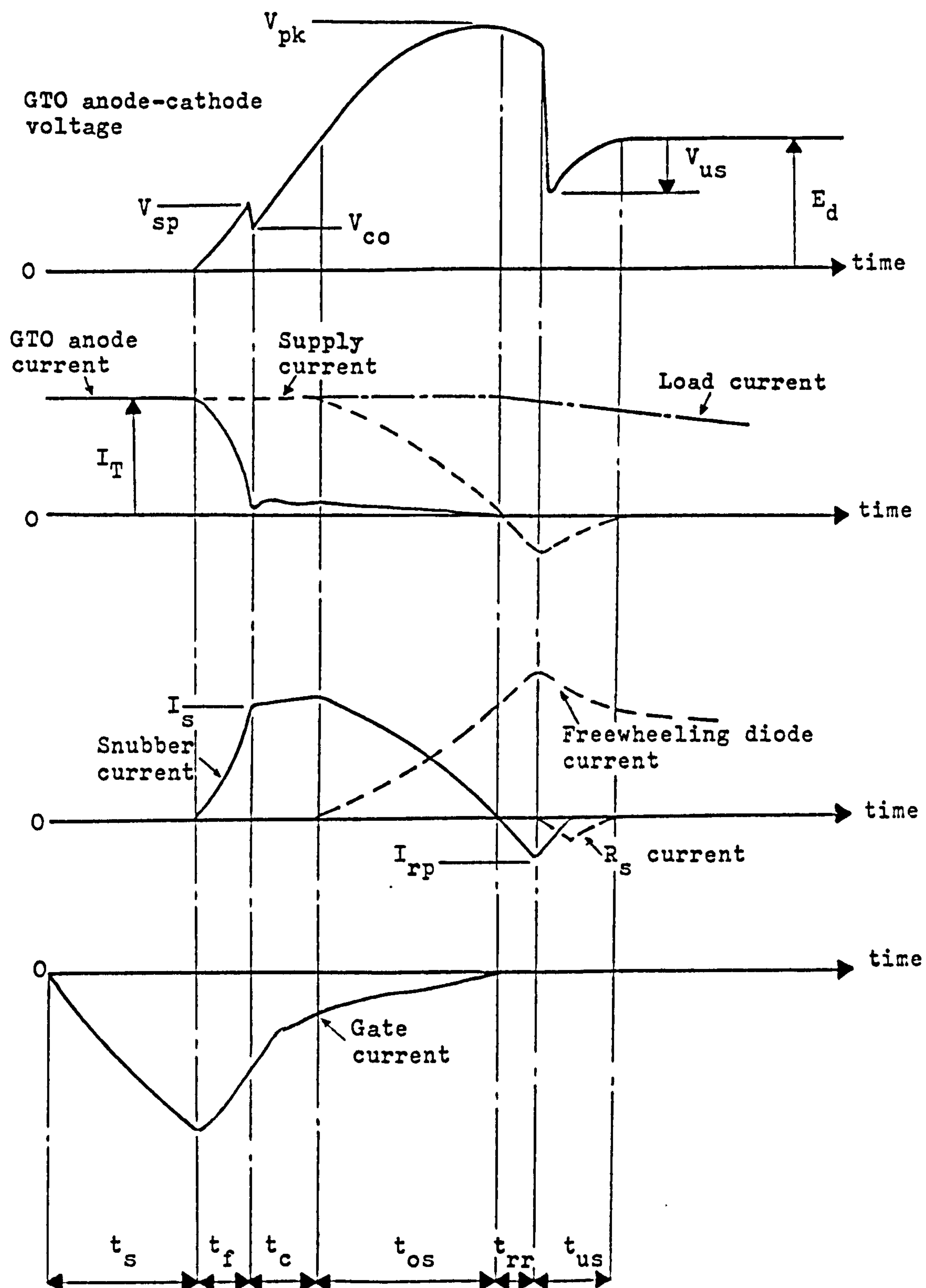
The freewheeling diode,  $D_f$ , does not become forward biased until the snubber capacitor is charged to value slightly higher than the supply voltage,  $E_d$ . Assuming the load inductance,  $L_l$ , is high relative to the strays ( $L_d$ ,  $L_f$ ,  $L_l$  and  $L_s$ ), and allowing for the small GTO tail current present, the almost constant capacitor current gives a virtually linear voltage rise from  $V_{co}$  to beyond  $E_d$ .

Now if, for simplicity, the GTO tail current is neglected, thus the charging current is the interrupted current,  $I_T$  then:

$$v_c = \frac{1}{C_s} \int_0^{t_c} I_T dt$$

giving





$t_s$	Storage time	$t_{os}$	Overshoot time
$t_f$	Fall time	$t_{rr}$	Reverse recovery time
$t_c$	Near constant current charging time	$t_{us}$	Undershoot time

Figure 3.7 Sketched waveforms at GTO thyristor turn-off in chopper with inductive load

$$t_c = \frac{C_s (E_d - V_{co})}{I_T} \quad (3.23)$$

since the load current is assumed constant over this short interval.

**b) Overshoot time ( $t_{os}$ )**

The overshoot time is now measured for the voltage rise from  $E_d$  to  $V_{pk}$  instead of  $V_{co}$  to  $V_{pk}$  as before. During this time, the snubber current falls to zero and concurrently, the load current, assumed constant, diverts into the freewheeling path, being totally freewheeling at the snubber current zero instant. From Appendix II, the capacitor charging current, neglecting the small lead resistance losses, is given by:

$$i_s = I_T \cos \omega t$$

where  $\omega^2 = 1/LC_s$  and  $L$  is the effective path stray inductance  $= (L_d + L_1 + L_s + L_f)$ .

Bearing no resistive term, this is simpler than for resistive load. Peak capacitor voltage is reached when  $i_s = 0$  and then  $\omega t_{os} = \pi/2$ , giving

$$t_{os} = \frac{\pi}{2} \sqrt{LC_s} \quad (3.24)$$

and the peak capacitor voltage

$$V_{pk} = I_T \sqrt{\frac{L}{C_s}} + E_d \quad (3.25)$$

As  $t_{os}$  is now easily calculated, energy considerations (Appendix II) give  $V_{pk}$  from

$$\frac{1}{2} C_s V_{pk}^2 = \frac{1}{2} (L_d + L_1 + L_3 - 3 L_f) I_T^2 + \frac{1}{2} C_s E_d^2 + \frac{2}{\pi} E_d I_T t_{os} \quad (3.26)$$

**c) Snubber diode reverse recovery time ( $t_{rr}$ )**

The snubber diode reverse recovery is essentially the same as with the resistive load.

However, the capacitor discharge path back into the source is through the freewheeling path of inductance  $(L_d + L_1 + L_s + L_f)$ , not the load, and its resistance is the very small connector value (neglected in the analysis). The peak reverse recovery current  $I_{rp}$  will thus be rather higher, although this depends on the falling  $di_s/dt$  prior to diode reverse conduction which, in turn, is indicated by the overshoot time controlled by the stray inductance values. For a greater  $I_{rp}$ , the sudden drop of voltage ( $I_{rp} R_s$ ) from the peak value,  $V_{pk}$ , will be greater.

#### **d) GTO undershoot time ( $t_{us}$ )**

The reasoning relating to the prevention of undershoot and the overdamping of the capacitor discharge oscillation is as for a resistive load. Equation (3.22) applies with the circuit resistance,  $R$ , now being the very small path resistance through the freewheeling branch. After the sudden fall of voltage, the time constant of the voltage exponential decay will be smaller than that with a resistive load.

### **3.4.2 Verifying experimental results**

With data measured as before;

Path inductance through freewheeling

branch $(L_d + L_1 + L_s + L_f)$	= 4.6 $\mu$ H	measured
----------------------------------	---------------	----------

Path inductance through load

$(L_d + L_1 + L_s + L_f)$	= 68.8 $\mu$ H	measured
---------------------------	----------------	----------

Freewheeling path inductance ( $L_f$ )	= 0.8 $\mu$ H	measured
--	---------------	----------

Remaining $(L_d + L_1 + L_s)$	= 3.8 $\mu$ H (= 4.6 - 0.8) $\mu$ H	
-------------------------------	-------------------------------------	--

Path resistance through load $R$	= 0.54 $\Omega$	measured
----------------------------------	-----------------	----------

Path resistance through freewheeling

branch	= 0.02 $\Omega$	measured
--------	-----------------	----------

Supply voltage ( $E_d$ )	= 320V	from CRO
--------------------------	--------	----------

Interrupted current ( $I_T$ )	= 600A	from CRO
-------------------------------	--------	----------

Snubber loop inductance ( $L_2 + L_s$ )	= 0.1 $\mu$ H	estimated
---	---------------	-----------

Fall time (spike width) ( $t_f$ )	= 0.8 $\mu$ S	from CRO
-----------------------------------	---------------	----------

Snubber diode forward recovery voltage	= 34V	from CRO
--	-------	----------

A set of the computer simulated waveforms at the GTO thyristor turn-off is shown in Figure 3.6. The equivalent circuits for the various time intervals and their associated



state matrices are given in Figure 3.8. The interval corresponding to  $t_f$  is as that of the resistive load shown in Figure 3.4(a), and is not repeated. Table 3.2 compares calculated, computed and experimental results and again good correlation is demonstrated, particularly between the latter two.

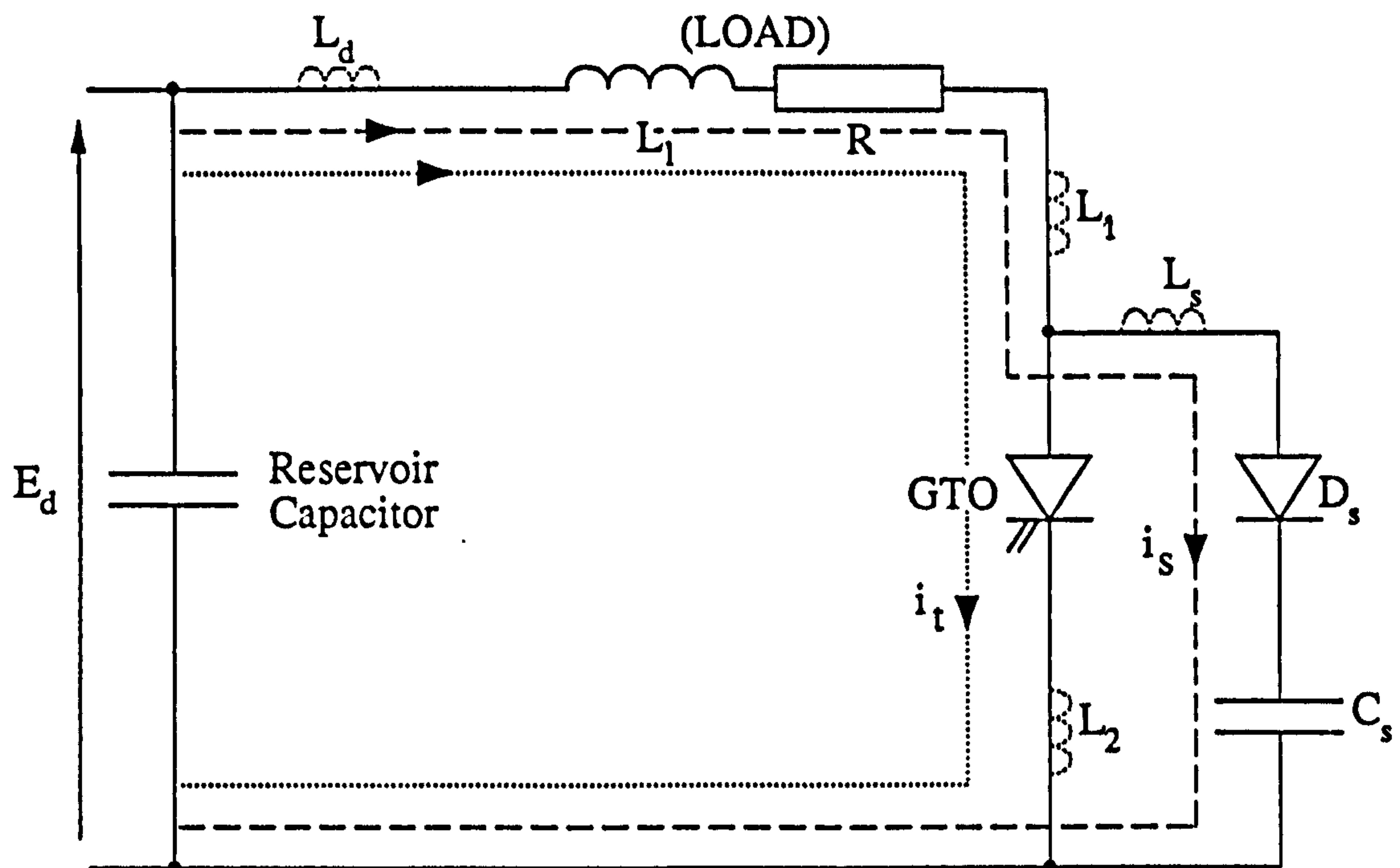
Quantity	Equation used	Calculated from equation	Computed value	Experimental value
Peak spike voltage ( $V_{sp}$ )	(3.15)	172V	175V	180V
Capacitor accumulated voltage ( $V_{co}$ )	(3.10)	36V	42V	50V
Near constant current charging time ( $t_c$ )	(3.23)	1.9 $\mu$ s	1.6 $\mu$ s	1.7 $\mu$ s
Overshoot time ( $t_{os}$ )	(3.24)	6.7 $\mu$ s	6.5 $\mu$ s	6.3 $\mu$ s
Peak GTO voltage ( $V_{pk}$ )	(3.25)	963V	880V	840V
Peak GTO voltage ( $V_{pk}$ )	(3.26)	790V	880V	840V

Table 3.2 Calculated, computed and measured values for GTO turn-off in the chopper with inductive-resistive load

### 3.5 Comparison of GTO Turn-Off with Resistive and Inductive Loads

Comparison of turn-off with the two types of load is made from the evidence of plotted experimental results, Figure 3.9, and the oscillograms of Figure 3.5(a) and (b). Owing to the laboratory supply and device switching loss limitations, a relatively low chopping frequency of 100Hz and low duty cycle of 6% were used. The load current flow with inductive load was discontinuous. The following points emerge:

1) The voltage spike  $V_{sp}$  induced during the GTO current fall time by the rising current in the very small GTO snubber loop inductance is independent of the type of load, as is the accumulated capacitor voltage  $V_{co}$  present at the end of the spike.



$$\begin{bmatrix} p i_s \\ p i_t \\ p v_c \end{bmatrix} = \begin{bmatrix} -\frac{R}{L_4} & -\frac{R}{L_4} & -\frac{1}{L_4} \\ 0 & 0 & 0 \\ \frac{1}{C_s} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_s \\ i_t \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{E_d t_t + 0.2 L_T L_5}{t_t L_4} \\ -0.2 \frac{I_T}{t_t} \\ 0 \end{bmatrix}$$

where  $t_t = t_c + t_{os}$  ;

$$t_c = \frac{C_s (E_d - V_{co})}{I_T} ;$$

$$t_{os} = \frac{\pi}{2} \sqrt{LC_s} ;$$

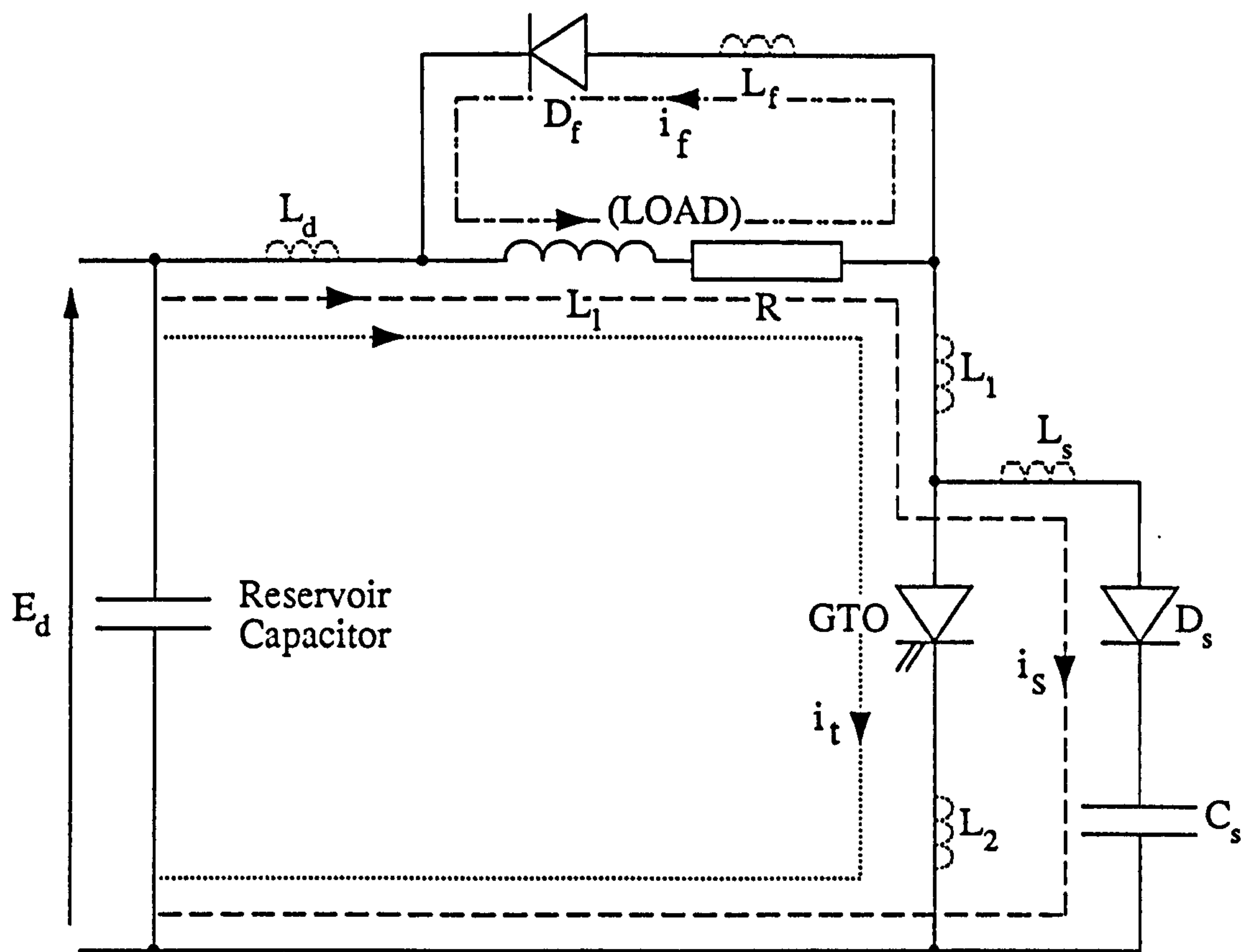
$$L = L_d + L_{df} + L_1 + L_s ;$$

$$L_4 = L_d + L_1 + L_1 + L_s ;$$

$$L_5 = L_d + L_1 + L_1 ;$$

(a) During the constant current charging time ( $t_c$ )

Figure 3.8 Equivalent circuits and state equations of the GTO turn-off time intervals in chopper with inductive load.



$$\begin{bmatrix} p i_s \\ p i_t \\ p i_f \\ p v_c \end{bmatrix} = \begin{bmatrix} -\frac{RL_f}{L_8^2} & -\frac{RL_f}{L_8^2} & -\frac{RL_f}{L_8^2} & -\frac{L_6}{L_8^2} \\ 0 & 0 & 0 & 0 \\ -\frac{RL_7}{L_8^2} & -\frac{RL_7}{L_8^2} & -\frac{RL_7}{L_8^2} & -\frac{L_1}{L_8^2} \\ \frac{1}{C_s} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_s \\ i_t \\ i_f \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{E_d t_t L_6 - 0.2 I_T L_9^2}{t_t L_8^2} \\ -0.2 \frac{I_T}{t_t} \\ \frac{-E_d t_t L_1 + 0.2 I_T L_{10}^2}{t_t L_8^2} \\ 0 \end{bmatrix}$$

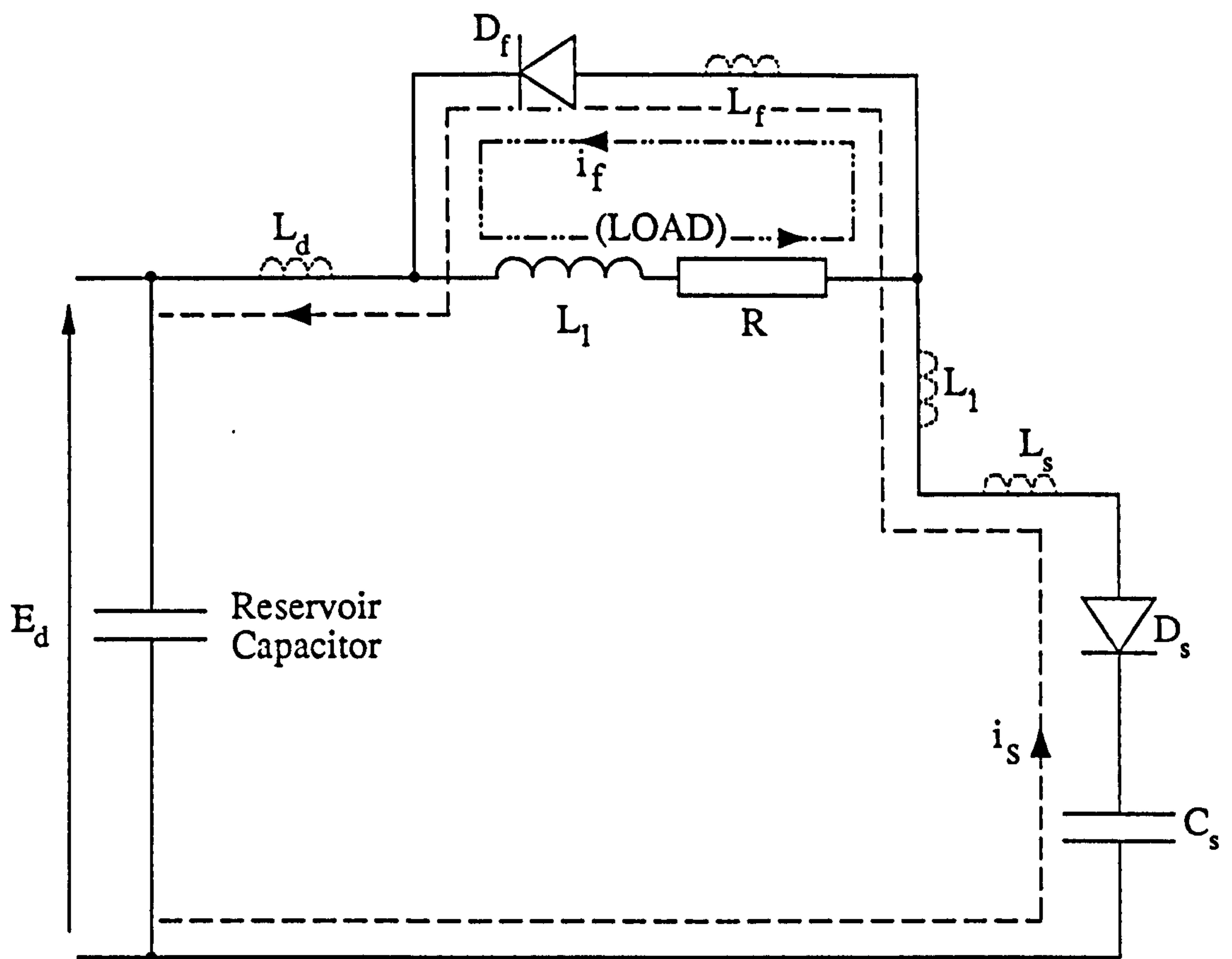
where

$$\begin{aligned}
 L_6 &= L_1 + L_{df} ; \\
 L_7 &= L_d + L_1 + L_s ; \\
 L_8^2 &= (L_1^2 - L_5 L_6) ; \\
 L_{10}^2 &= L_1 L_5 ;
 \end{aligned}$$

(b) During the oscillatory overshoot time ( $t_{os}$ )

Figure 3.8 Equivalent circuits and state equations of the GTO turn-off time intervals in chopper with inductive load.



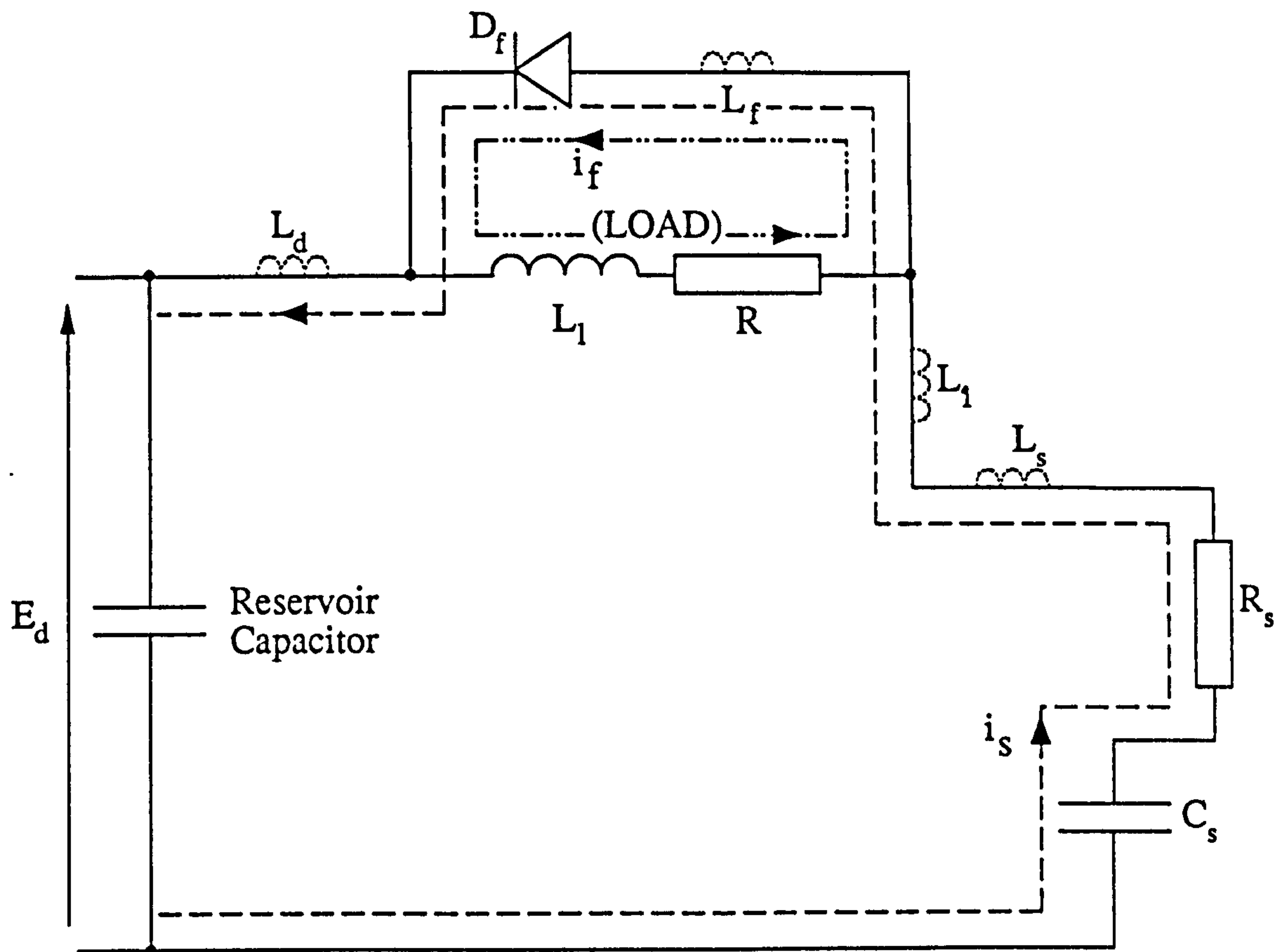


$$\begin{bmatrix} p i_s \\ p i_f \\ p v_c \end{bmatrix} = \begin{bmatrix} 0 & -\frac{RL_f}{L_{12}^2} & -\frac{L_6}{L_{12}^2} \\ 0 & -\frac{RL}{L_{12}^2} & -\frac{L_f}{L_{12}^2} \\ \frac{1}{C_s} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_s \\ i_f \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{E_d L_6}{L_{12}^2} \\ \frac{E_d L_f}{L_{12}^2} \\ 0 \end{bmatrix}$$

where  $L_{12}^2 = (LL_6 - L_f^2)$  ;

(c) During snubber diode reverse recovery time ( $t_{rr}$ )

Figure 3.8 Equivalent circuits and state equations of the GTO turn-off time intervals in chopper with inductive load.



$$\begin{bmatrix} p i_s \\ p i_f \\ p v_c \end{bmatrix} = \begin{bmatrix} -\frac{R_s L_6}{L_{12}^2} & -\frac{R L_f}{L_{12}^2} & -\frac{L_6}{L_{12}^2} \\ -\frac{R_s L_f}{L_{12}^2} & -\frac{R L}{L_{12}^2} & -\frac{L_f}{L_{12}^2} \\ \frac{1}{C_s} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_s \\ i_f \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{E_d L_6}{L_{12}^2} \\ \frac{E_d L_f}{L_{12}^2} \\ 0 \end{bmatrix}$$

(d) During voltage undershoot time ( $t_{us}$ )

Figure 3.8 Equivalent circuits and state equations of the GTO turn-off time intervals in chopper with inductive load.

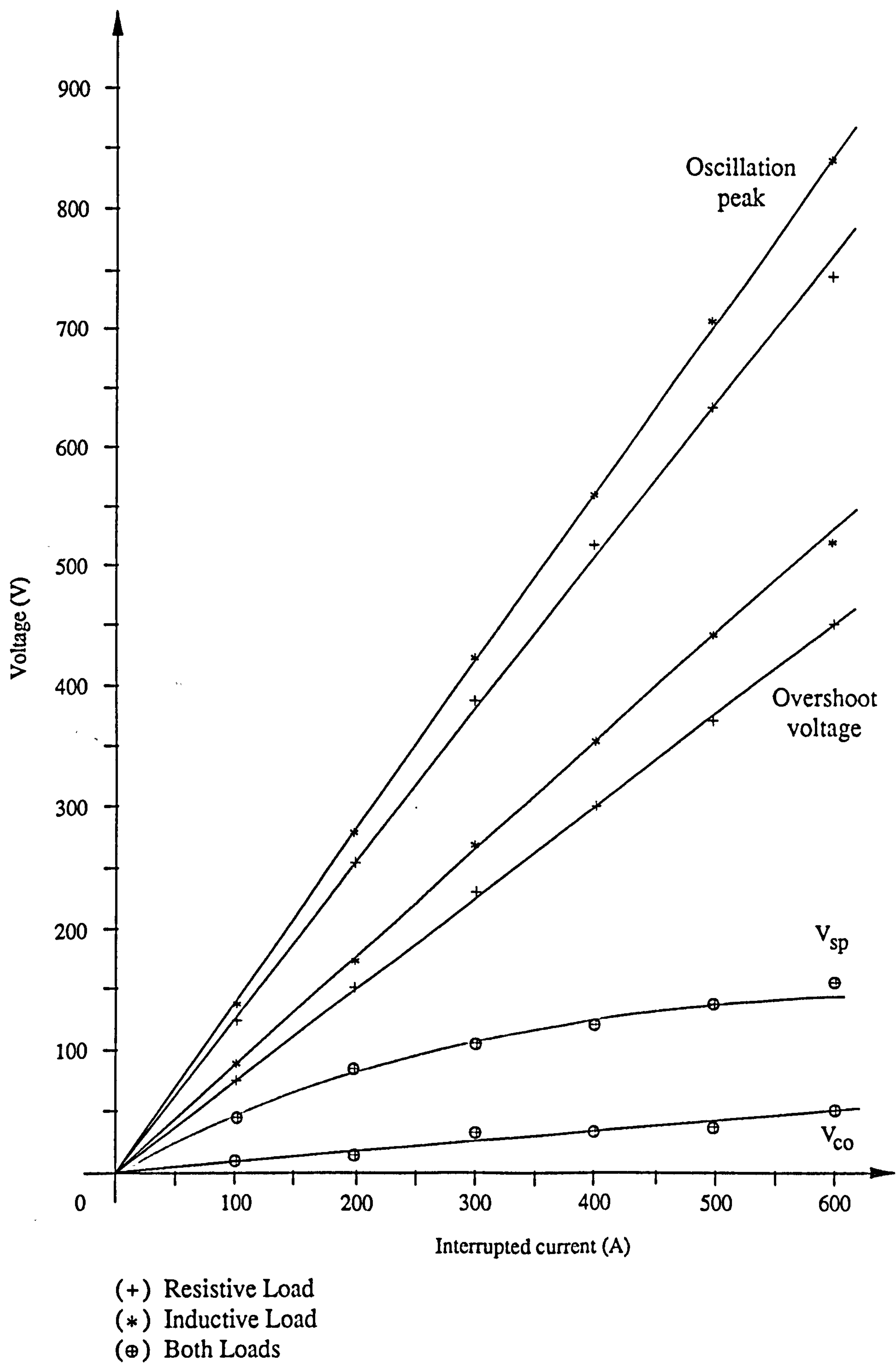


Figure 3.9 Measured voltage components at GTO turning off 600A in chopper circuit



*ii) With resistive load, the capacitor charging current commences its fall immediately after the  $V_{co}$  instant; with inductive load, the current is virtually constant until the capacitor voltage reaches  $E_d$ , thereafter it commences its fall.*

*iii) As a result of (ii), comparison of the oscillograms shows a virtually linear rise of GTO thyristor voltage from  $V_{co}$  to the supply voltage level  $E_d$  (time interval  $t_c$ ) for the inductive load, whereas it is sinusoidal for the resistive load. This is emphasised by Figure 3.6.*

*iv) The overshoot voltage ( $V_{pk} - E_d$ ) and peak voltage  $V_{pk}$  are higher with the inductive load as the damping effect of the load resistance is absent with the freewheeling path present. The effect would be more marked if the stray inductance ( $L_d + L_1 + L_s + L_f$ ) had not been comparatively low.*

*v) The rate of snubber diode current rise is greater for the inductive load, giving a higher reverse recovery current peak  $I_{rp}$  which, when diverted into the snubber resistor  $R_s$  will cause a greater sudden drop of GTO voltage from the peak value. This is also coupled to the gate voltage.*

*vi) The voltage oscillatory overshoot time is measured from  $V_{co}$  with the resistive load (depending on  $L_d + L_1 + L_s$ ) and from  $E_d$  for the inductive load (depending on  $L_d + L_1 + L_s + L_f$ ). It would be expected that the latter be longer but the oscillograms indicate the opposite. This is due to much of ( $L_d + L_1 + L_s$ ) stray inductance ( $6.7\mu H$ ) being in the load and the ( $L_d + L_1 + L_s + L_f$ ) ( $4.6\mu H$ ) being smaller due to  $L_f$  paralleling much of the stray  $L_1$ , which is effectively lowered.*

*vii) The plotted results (Figure 3.9) confirm what may be interpreted from the equations, that  $V_{sp}$ ,  $V_{co}$  and  $V_{pk}$  voltages are all proportional to the interrupted current  $I_T$ .*

### **3.6 Circuit Layout Consideration to Minimising Stray Inductances Effect**

*The overriding theme in circuit layout for transient over-voltage limitation is to minimise the stray inductances.*

### **3.6.1 Gate drive circuit**

- a) The gate drive should be as close as possible to the GTO.*
- b) The gate and cathode control leads should be a short twisted pair or coaxial.*
- c) The gate pulse energy storage capacitor(s) should have low internal equivalent series inductance (ESL).*

### **3.6.2 Chopper circuit**

- a) The usual technique of using short length, large rectangular cross-section conductors, with go and return DC rails close together (to obtain the benefit of cancelling mutual inductance effects), should be used.*
- b) The freewheeling diode should be connected across the GTO thyristor anode and supply positive so that the stray lead inductance to the perhaps remote load is incorporated in the load inductance.*
- c) The supply reservoir capacitor should be connected right across the input terminals to give low supply  $L_{\Lambda}^{\text{lead}}$  inductance, and its ESL should be as low as possible, as both contribute to  $L_d$ . Electrolytic capacitors have desirably high capacitance, but also relatively high ESL compared with other types. A number of paralleled units should be used.*
- d) The snubber capacitors should have the lowest possible ESL. Typical types are the metallised polypropylene capacitors, the ESL of which, ranges between 30-100nH. Again, paralleling is a useful technique.*
- e) The snubber circuit should be mounted as near as possible to the GTO thyristor terminals.*

### **3.7 Conclusions**

*A comprehensive treatment of the GTO thyristor chopper has been investigated for resistive and resistive-inductive loads. In particular, methods of determining the amplitudes and duration of the transient voltages appearing across the GTO thyristor at turn-off have been defined in terms of the stray circuit inductances and the snubber capacitance value, and the various circuit resistance where appropriate. Lead resistance has been ignored. It is difficult if not impossible to predict the stray wiring inductances accurately, although they can usually be measured after construction. The stray inductance circuit modelling has been limited to self inductances, mutual magnetic coupling being ignored. This may not be justified at very high currents, but is shown to be adequate for the peak currents of 600A used here.*

*The computer simulation satisfactorily models the circuit behaviour under switching conditions when representative GTO thyristor and diode terminal characteristics are used. These are somewhat approximated, for example by using a linear fall of GTO tail current and instantaneous snap-off of diode reverse recovery. It was not intended to model the GTO thyristor by active and passive components, such as by using the SPICE software. A separate small scale exercise in this respect did not prove satisfactory in the time available.*



## CHAPTER 4

### Stray Inductance Effects in the H-Bridge with a Quasi-Square AC Output Voltage

#### 4.1 Introduction

*The voltage overshoots produced at GTO thyristor switching, due to the stored energy in the stray inductances, must be limited to an acceptable value in relation to the GTO thyristor voltage rating. The widely used circuit of the H-bridge is considered, it being capable of operating as a four-quadrant DC chopper, or a single-phase inverter, with the current paths at commutation being dependent on the switching pattern employed.*

*In this chapter, computer simulated and experimental results are presented which demonstrate the relative importance of the various lumped circuit path stray inductances in generating these overshoot voltages as current transfers between the active devices during commutation. The limitation of over-voltages is again accomplished by the passive snubbers connected across the GTO thyristors.*

*The implications of circuit layout are considered.*

#### 4.2 Basic Inverter Operation

*Figure 4.1 shows the bridge circuit with stray inductances included. If the load is resistive, and all stray inductances are negligibly small, the alternate gating of GTO pairs A1, A2 and B1, B2 for 180° of the inverter output voltage will place the DC supply in alternate polarities across the load, giving a square waveform (Figure 4.2(a)).*

*With an inductive load, the current reversals are exponential, although the voltage is still square as in Figure 4.2(b).*

*Considering the end of the positive half-cycle, the load current is positive and almost constant when GTOs A1 and A2 are turned off and B1 and B2 are gated for conduction. However, the inductive load current, which cannot reverse instantaneously, transfers to diodes D3 and D4 with the stored inductive energy of the load being returned or fed back to the supply until the load current falls to zero. On load current reversal, GTOs B1 and B2 conduct and power is again fed from the supply to the load, the reversed load current now growing exponentially. As the instant of the feedback current zero can be at any*

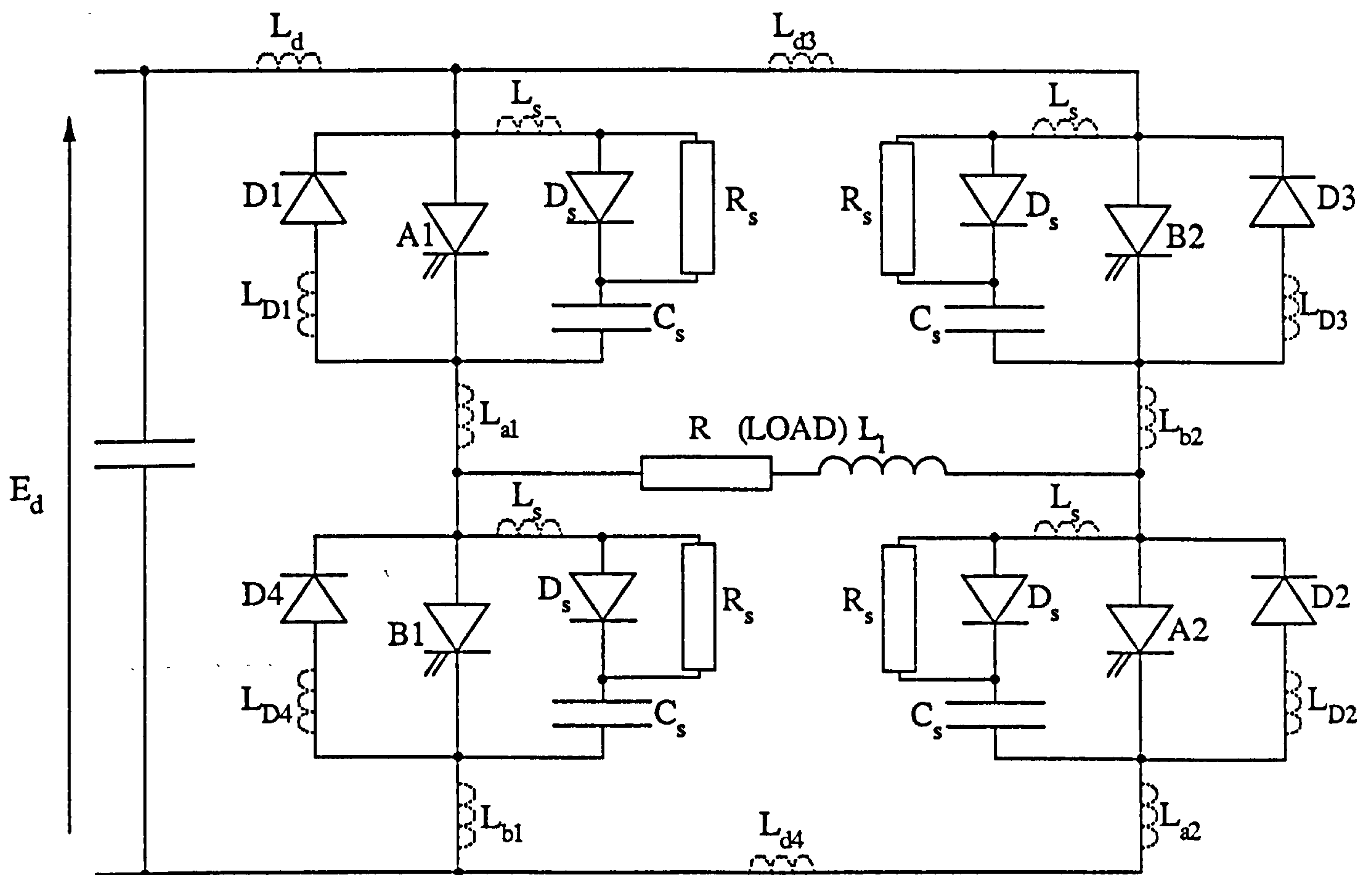
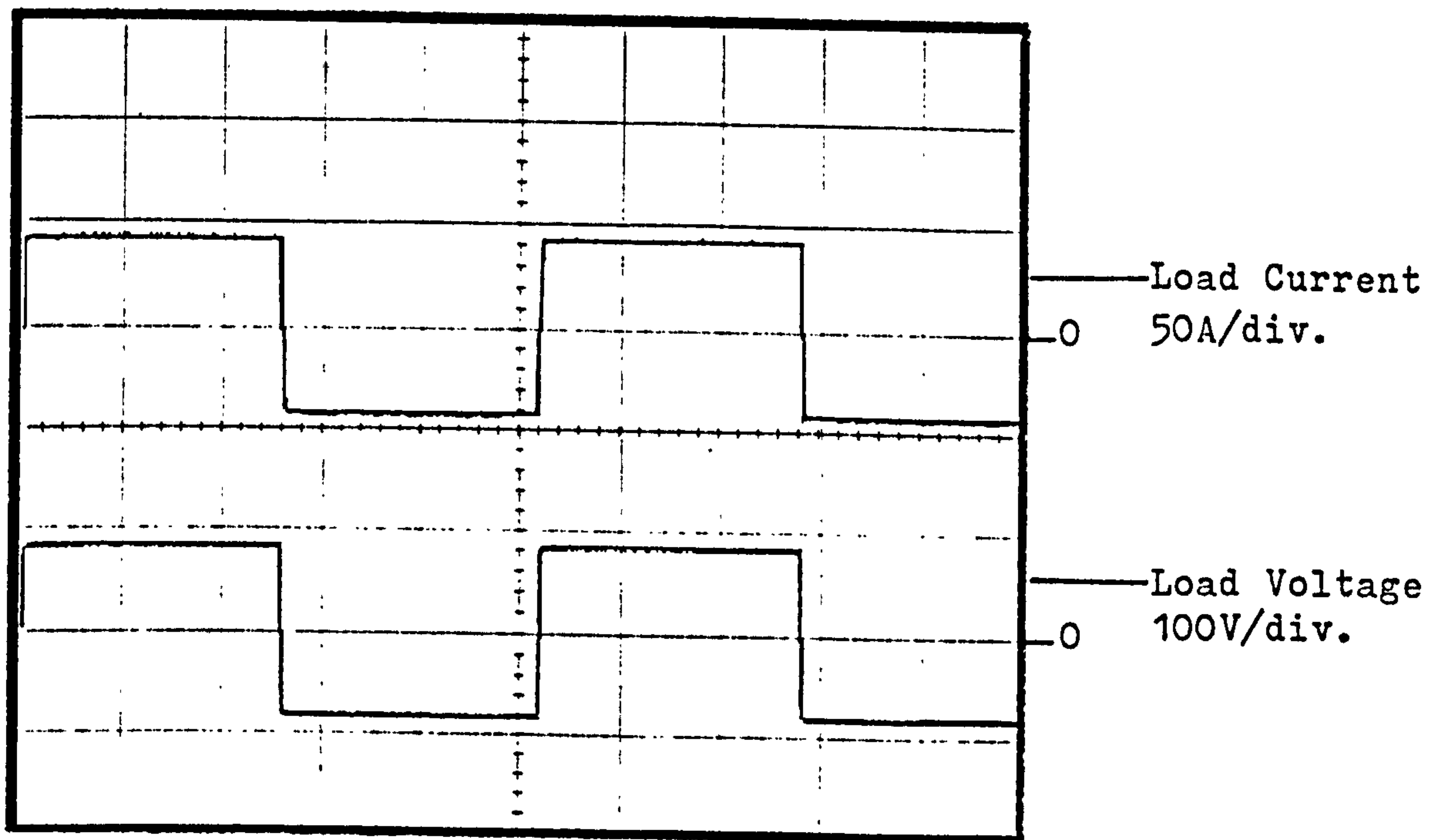


Figure 4.1 Single phase bridge inverter with lumped stray inductances shown in broken lines

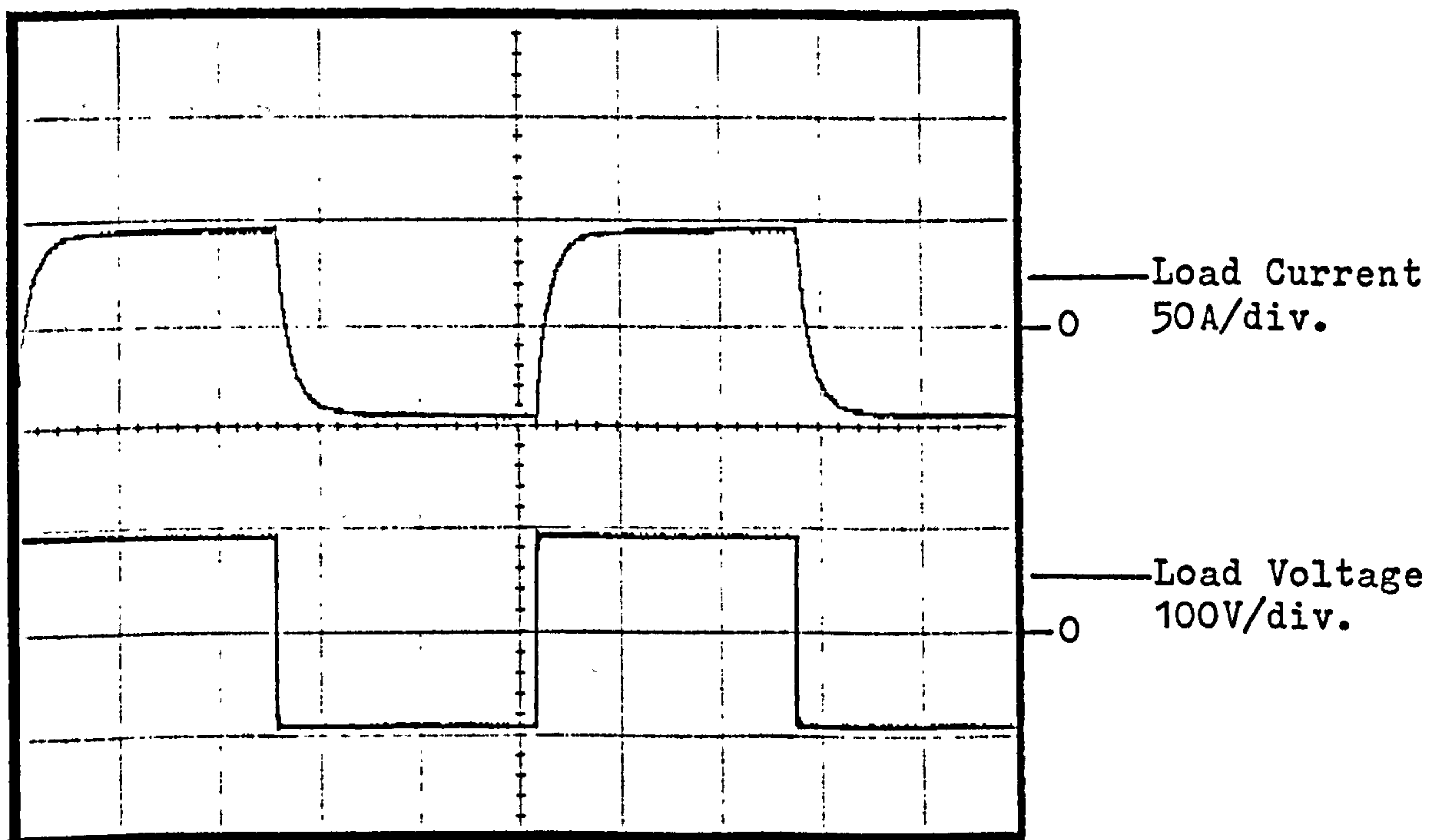
time in the second half-cycle, GTOs B1 and B2 take over conduction when required if supplied with a steady back-porch (BP) drive. The supply voltage automatically reverses when the diodes conduct and the feedback interval commences, giving no difference of voltage waveform for resistive and inductive loads.

In practice, GTO turn-on and turn-off is not instantaneous. This leads to a temporary shoot-through condition across the DC rails as two devices switch together, say B2 on and A2 off. A dead-band of about  $5\mu\text{s}$  is therefore introduced between turning off the upper row devices and turning on the complementary lower devices, and vice versa.

Additionally, control of the load voltage can be obtained by introducing zero intervals into the square wave, all such shapes being known as the quasi-square [28], (Figure 4.2(c)).



(a) Resistive Load



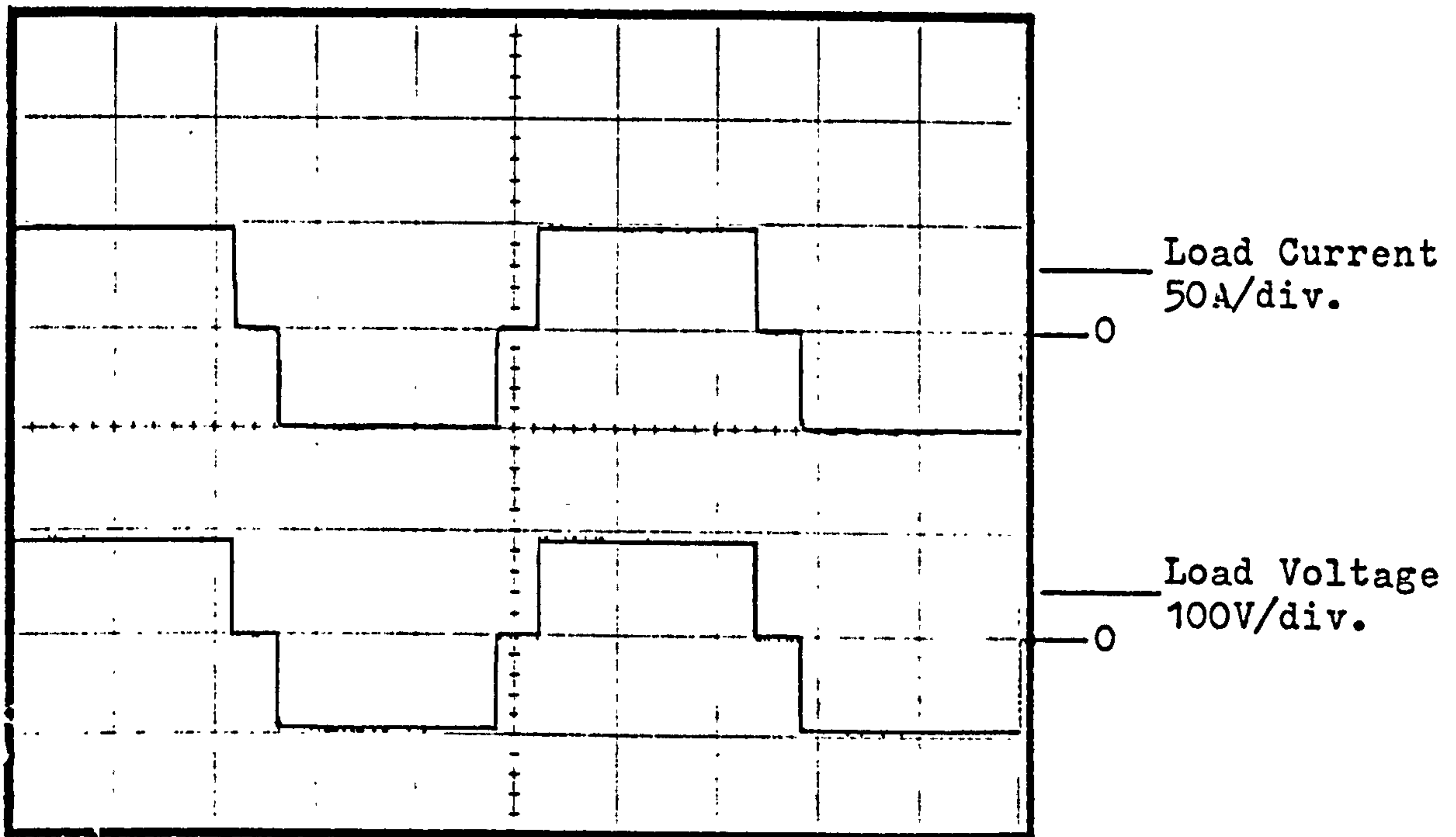
(b) Inductive Load

Time Scale: 2mSec/div.

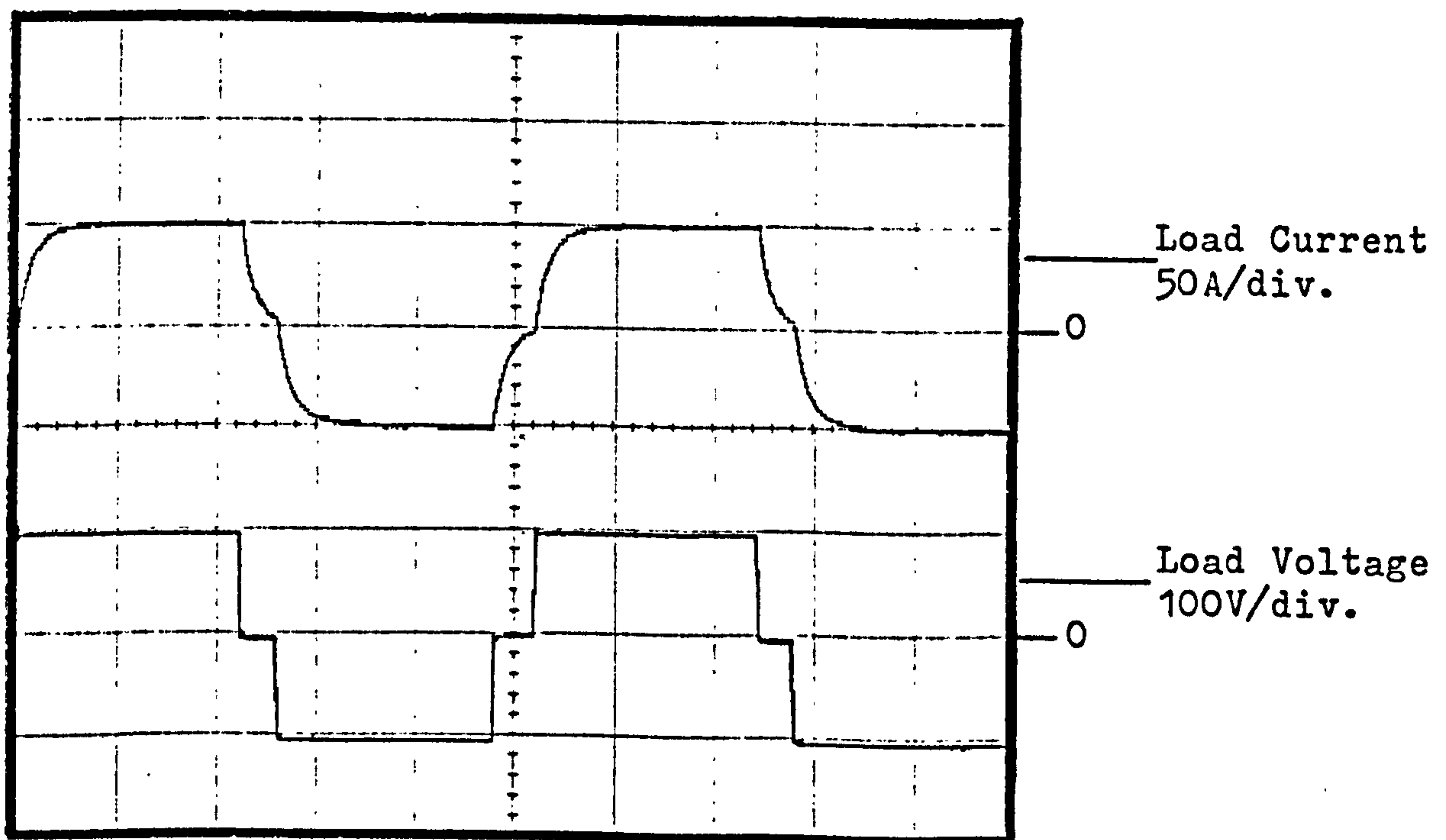
Square Output

Figure 4.2 The experimental H-bridge voltage and current outputs





(c) Resistive Load



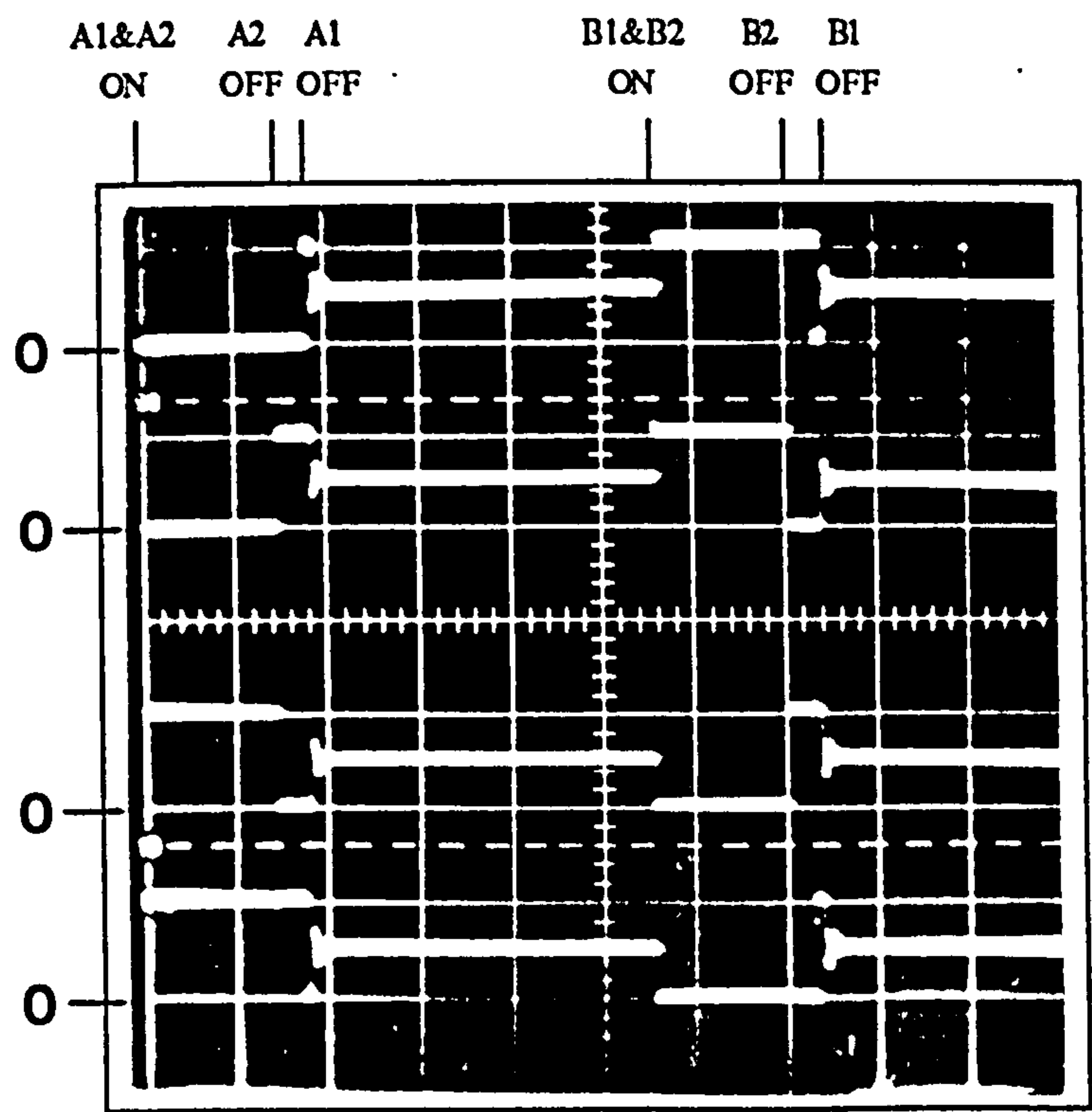
(d) Inductive Load

Time Scale: 2mSec/div

Quasi-square Output

Figure 4.2 The experimental H-bridge voltage and current outputs

The quasi-square wave can be generated by phase-advancing the turn-off of the complementary GTOs A2 and B2 while leaving the series path GTOs A1 and B1 in turn conducting, (Figure 4.3).



- (1) (A1) A-K Voltage (200V/div.)
- (2) (A2) A-K Voltage (200V/div.)
- (3) (B1) A-K Voltage (200V/div.)
- (4) (B2) A-K Voltage (200V/div.)

Time Scale: 1mS/div.

A2 and B2 turning off first for quasi-square output

Figure 4.3 GTOs A1, A2, B1 and B2 anode-cathode voltages

Let GTOs A1 and A2 be conducting. If GTO A2 is turned off, an inductive load current transfers to diode D3 but with GTO A1 still on, effectively short-circuiting the load giving zero load voltage. When later GTO A1 is turned off, the only path for the load current is via diodes D3 and D4, feeding back inductive energy and connecting the DC supply to the load in the negative sense as before with both GTOs off.

### 4.3 Bridge Switching Patterns

*Summarising the above, it is apparent that the switching pattern may provide turn-off for either one or both of a series conducting pair of GTOs. In either case with a resistive load, the output voltage and current half-cycle is then terminated and the freewheeling diodes do not conduct. With the more usual inductive load:*

- (a) For single GTO turn-off, say A2, the load current commutates from the source into a freewheeling path through GTO A1 and diode D3. Subsequent turn-off of the second GTO, A1, before the freewheeling current has fallen to zero, will commutate the load current from the freewheeling path to a feedback path through diodes D3 and D4 returning load inductive energy to the source.*
- (b) For double GTO turn-off, A1 and A2, the load current commutates directly to a feedback path through diodes D3 and D4, and therefore reverses in the source.*

### 4.4 The Experimental H-Bridge

#### 4.4.1 Power circuit

*Figure 4.1 shows the configuration of the bridge main circuit. The four GTOs used are AEG type G200 A100 rated at 200A repetitive controllable on-state current and 1kV repetitive off-state voltage. A 310V DC voltage source ( $E_d$ ) is provided from a variac-controlled rectified 220V AC 3-phase supply as used in section 2.9. A static load of  $2\Omega$  (nominal) in series with  $650\mu\text{H}$  (nominal) is used to give a peak current of 100A at an output frequency of 100Hz. The rated critical  $dv/dt$  of the GTOs is  $1\text{kV}/\mu\text{S}$ ; a nominal  $0.47\mu\text{F}$  snubber capacitor limited the  $dv/dt$  to about  $185\text{V}/\mu\text{S}$ .*

*The freewheeling and snubber diodes are of the fast recovery types rated respectively at 35A (average) and 1kV, and 20A (average) and 600V. Although a fast turn-on is desired in the case of the snubber diode, to lessen the forward recovery voltage transient contribution to the GTO thyristor voltage spike during its fall time, and to reduce switching losses in the diode itself, it is unfortunately incompatible with a fast turn-off characteristic.*

*A  $5\Omega$ , 25W snubber resistor, is large enough to control the snubber capacitor discharge into the GTO sufficiently at turn-on and low enough to restrict the IR drop following the snubber diode  $D_s$  reverse recovery, thus providing no undershoot. This ohmic value will overdamp the oscillation of  $C_s$  with the path stray inductances after  $D_s$  reverse*



recovery, since;

$$R_s^2 / 4L^2 > 1/LC_s$$

where  $L$  is the effective oscillatory path stray inductance.

The physical layout of the H-bridge is symmetrical, giving fairly balanced internal stray inductances, with the snubber stray inductances minimised.

#### 4.4.2 Control signals

The complete logic circuit for providing the isolated control signals to the bridge GTOs is shown in Figure 4.4. The 5V DC supply unit is similar in principle to that described in sub-section 2.12.4.

IC1 is connected as an astable multivibrator, the operating frequency being determined by the the potentiometer Pt0 and capacitor C0 for values ranging from 40Hz to 150Hz. The non-inverted Q1 and the inverted  $\overline{Q1}$  output pulses of IC1 are to be associated with GTO pair A1 and A2, and B1 and B2 respectively, thus switching the pairs with a phase difference of 180°, Figure 4.5. The positive going edge of the Q1 and  $\overline{Q1}$  pulses are each used to trigger one of the two monostables in IC2, producing output pulses QA1 and QB1 with time intervals (5-50µs), controlled by the external potentiometer Pt1-capacitor C1 network.

The output from the Exclusive-OR gates XR1 and XR2, the inputs of which are QA1 and Q1, and QB1 and  $\overline{Q1}$  respectively, will introduce the required dead-band periods (Figure 4.6). The leading edge of the Exclusive-OR gate output pulses are made to trigger the monostables of IC3, whose outputs QA2 and QB2 provide a common initial on pulse for each of the GTO pairs A1, A2 and B1, B2 respectively (Figure 4.7), and those of IC4 and IC5, to produce the back-porch (BP) signals, the width of each being independently variable. The trailing edge of each BP pulse is then employed to initiate the off and negative bias (NB) pulses for the associated GTO, using the monostables of IC6 to 9, Figures 4.4 and 4.8. The Q1 and  $\overline{Q1}$  outputs of IC1 are applied to the reset inputs of ICs4 and 5 respectively, thus preventing the BP period of any GTO being applied for more than 180°. Similarly, the complements of each initial on pulse are used to inhibit the negative bias signals at the associated GTO turn-on (Figure 4.6).

Each pulse period is determined by the external R-C networks connected to the IC

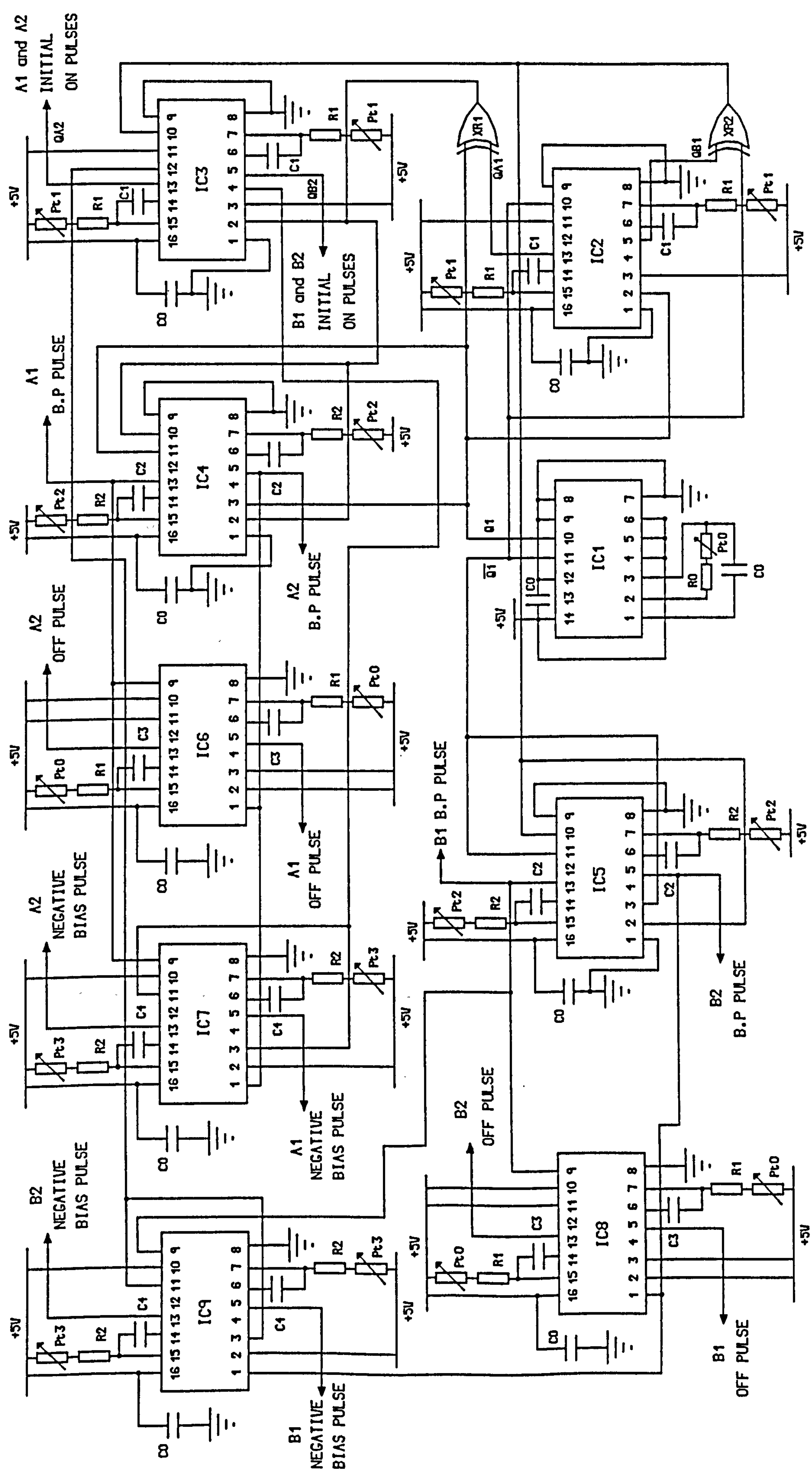
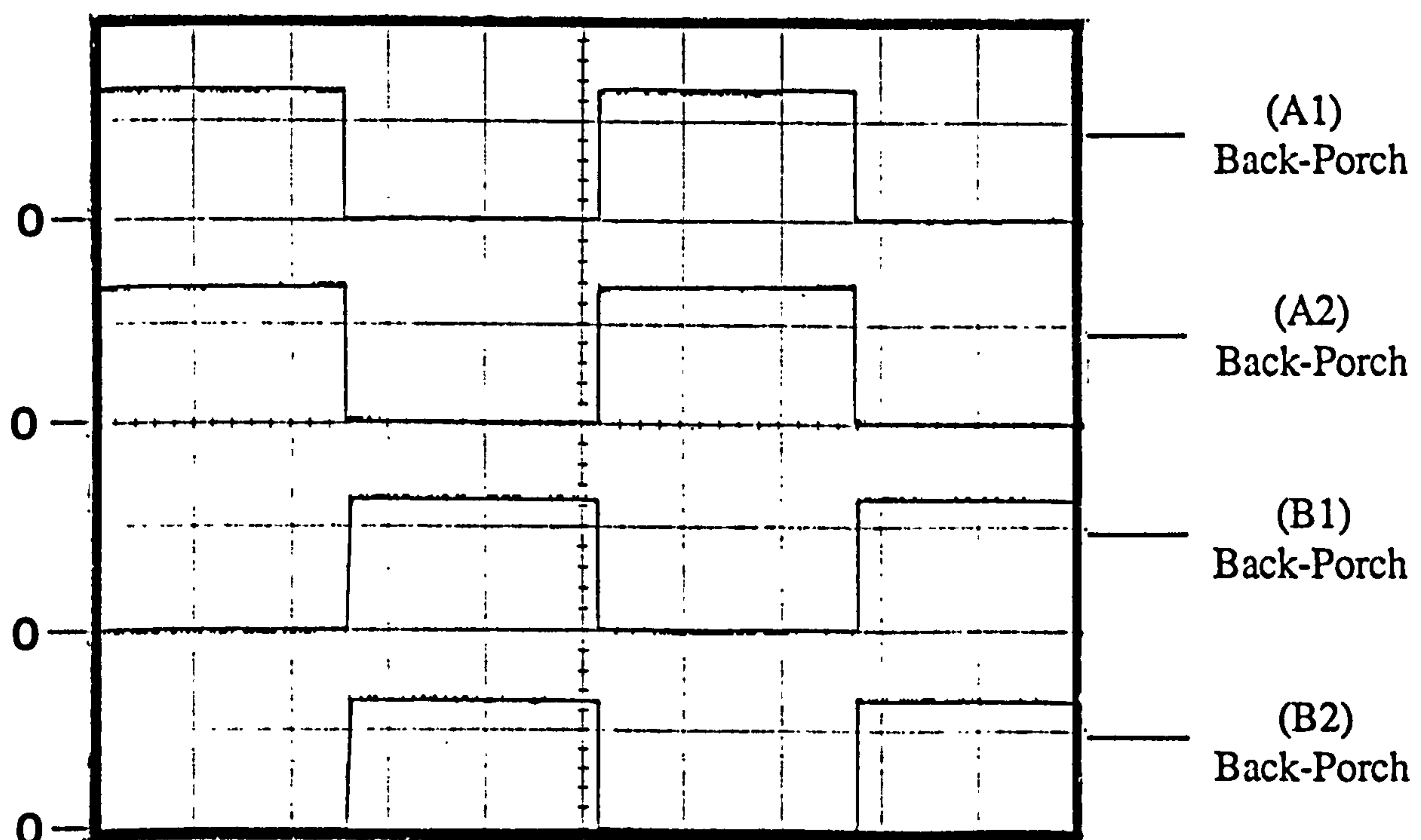


Figure 4.4 Experimental H-bridge control signals circuit



producing that pulse, Figure 4.4. The initial on pulses are fixed at  $14\mu\text{s}$ , where the BP and off pulses may be varied, to suit requirements, between 10-50% duty cycle and  $25\text{-}75\mu\text{s}$  respectively. The dead-band periods can be adjusted to  $5\text{-}10\mu\text{s}$  following the end of the off signal.

The purpose of the power supply decoupling capacitors  $C_0$ , is to bypass the power supply rail noise to ground, thus avoiding a malfunctioning of the ICs from this cause. The final control signals of about  $3.5\text{V}$  magnitude are applied to the inputs of the opto-isolators of the gate drive circuits.



Voltage Scale:  $2\text{V/div.}$

Time Scale:  $2\text{mS/div.}$

Figure 4.5 Back-porch control signals

#### 4.4.3 The gate drive circuits

The bridge GTOs gate drive circuits are similar to that described fully in sub-section



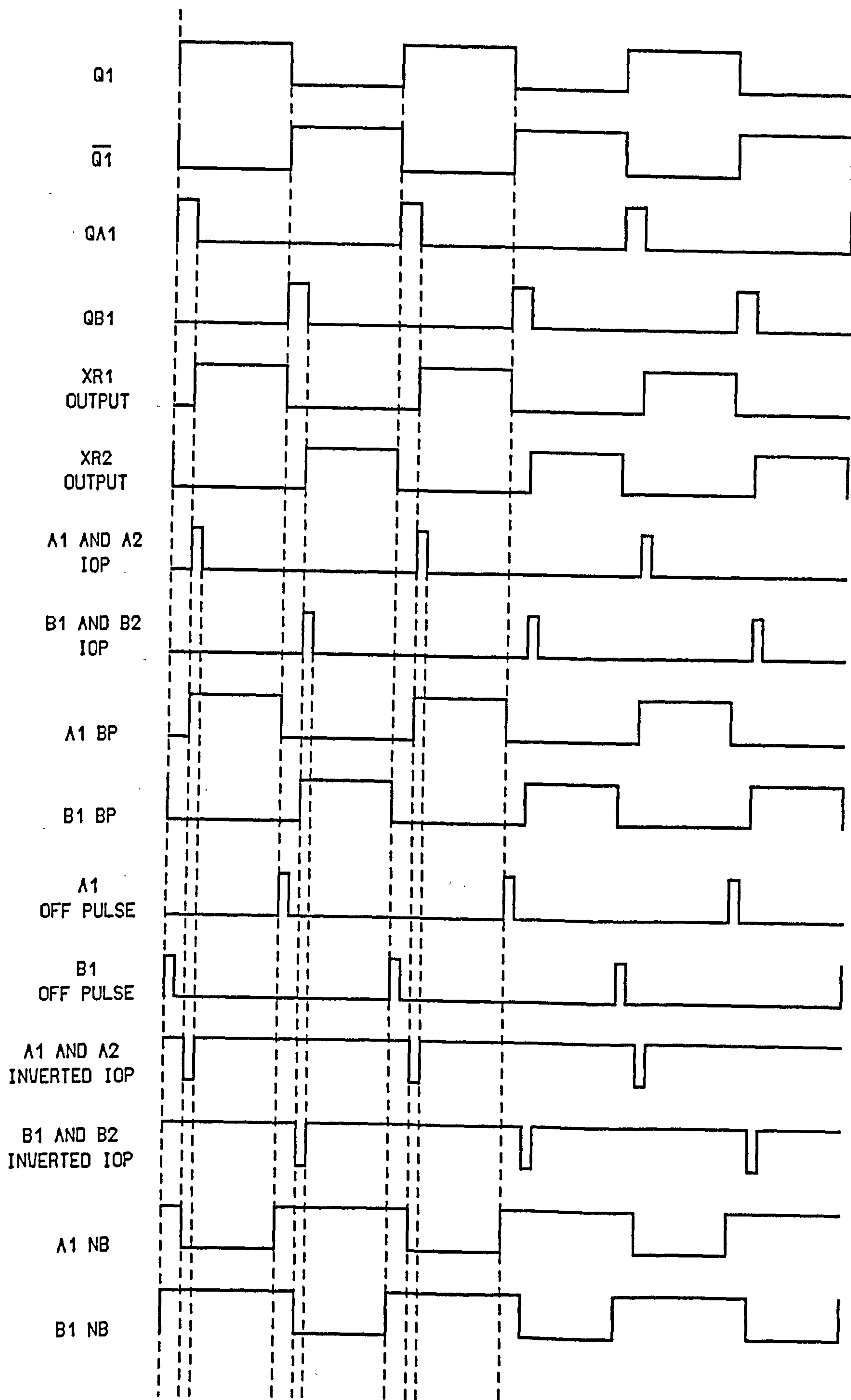


Figure 4.6 GTOs gate control logic

**2.12.3.** *The GTO turn-on is initiated by applying an initial current pulse of 9A, with an approximate rate of rise of 7A/μs, and sustained for 14μs, after which the current is dropped to the BP level, which is adjusted at 1.5A, Figure 4.9. At turn-off, the 12V negative voltage source is applied to the gate; the negative gate current increases at a rate of about 25A/μs, this implying a gate circuit path inductance of about 0.48μH. The negative gate voltage pulse is maintained for 50μs, thereafter a negative bias voltage of 4V is applied (Figure 4.9).*

#### **4.5 Transients with the GTO Thyristor Switching in the H-Bridge with Inductive Load**

*The transient effects of the GTO thyristor switching when the current path stray inductances are considered, and the effects on the other inactive devices in the H-bridge, are modelled by solving the first order differential equations using the Runge-Kutta fourth order numerical method (section 3.2). As with the chopper, small mutual coupling and current path resistances are ignored to reduce complexity. Also the simplifying assumptions made in sub-section 3.2.2 applied here.*

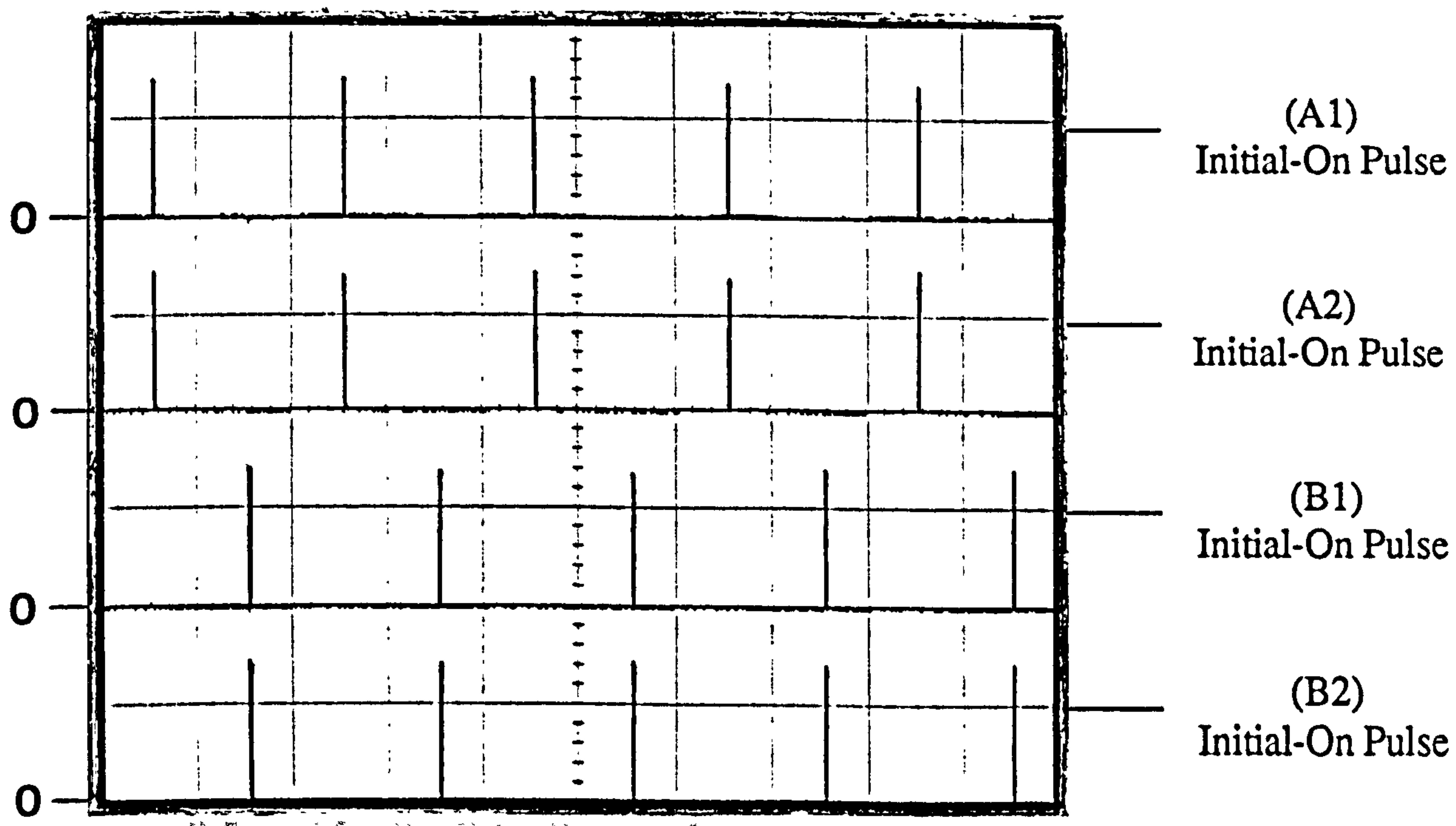
*Mathematical modelling to solve the system equations in the frequency domain, using the Laplace transform method, becomes tremendously complex since it requires very many different solutions to the complex equations with interdependent initial conditions. The mathematical modelling here is therefore by totally numerical methods using the computer.*

*With the circuit data as in section 4.4, the duty cycle (δ) of each GTO thyristor depends on the commutation pattern employed, but always:*

$$\delta \geq 5 \frac{L}{R} \geq 5 R_s C_s$$

*thus allowing the load current to reach its steady-state value during which the snubber capacitor should be fully discharged.*

*Also referring to Figure 4.1, the measured, and in the case of small loops the estimated,*

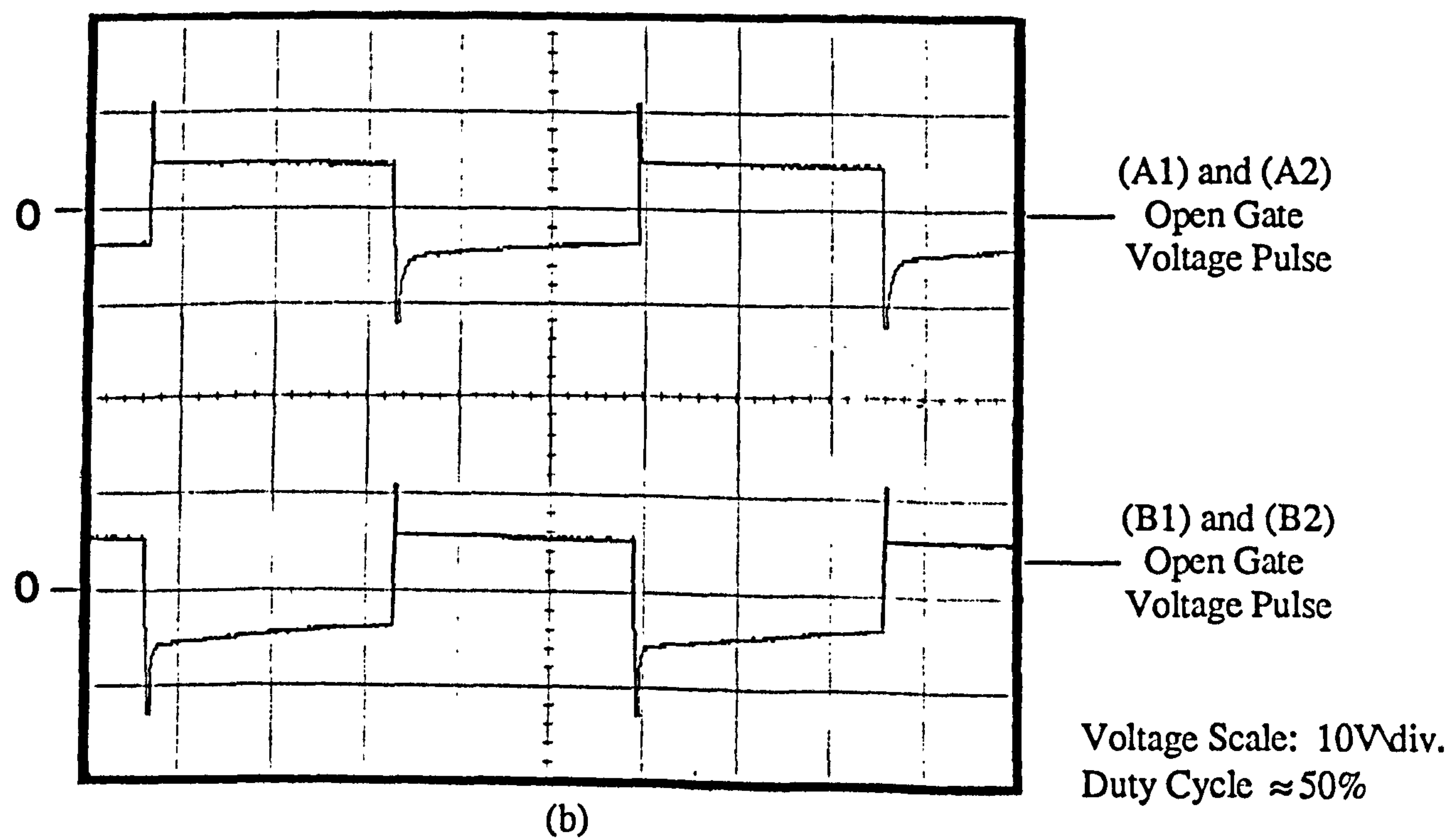
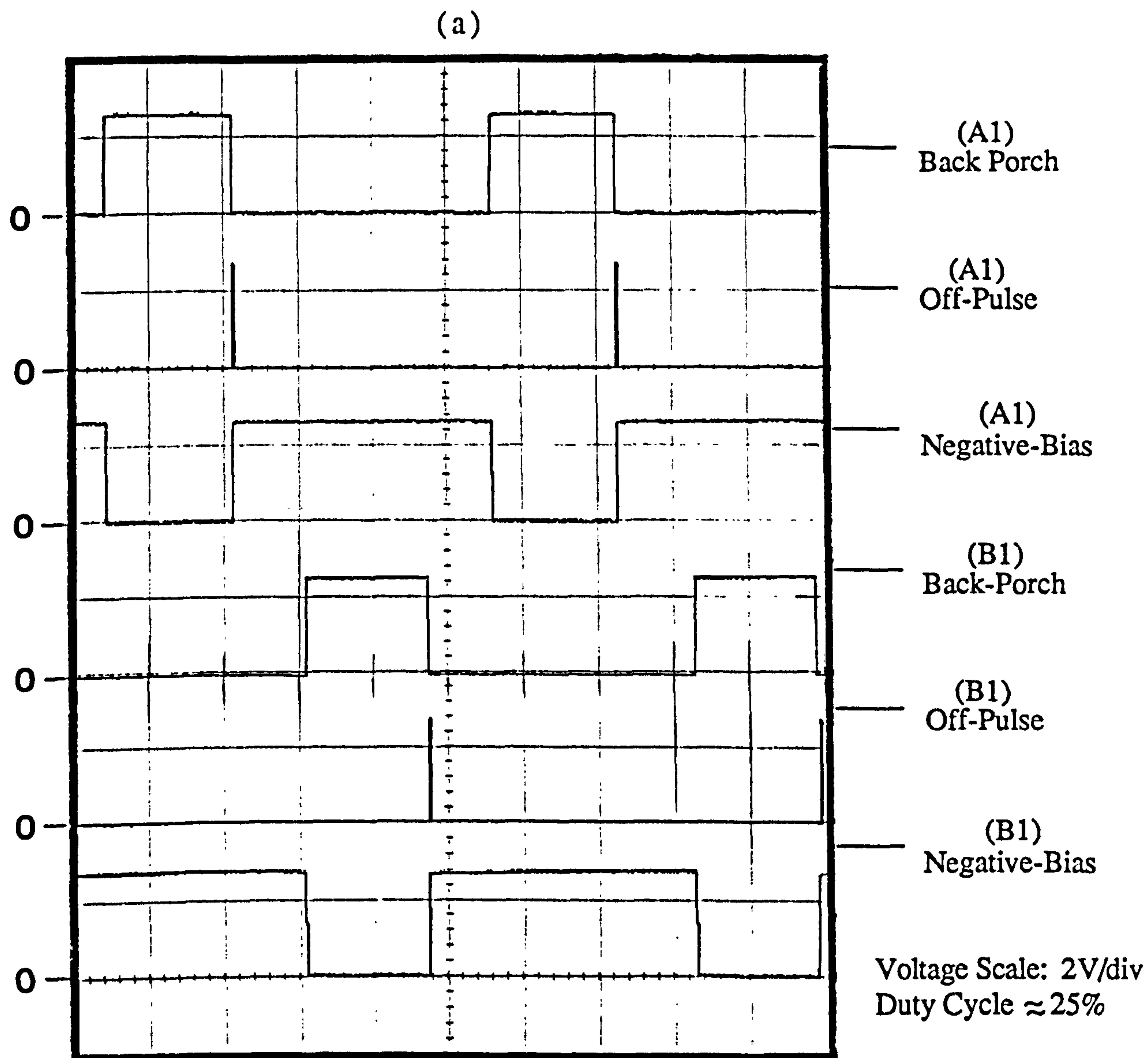


Voltage Scale: 2V/div.

Time Scale: 5mS/div.

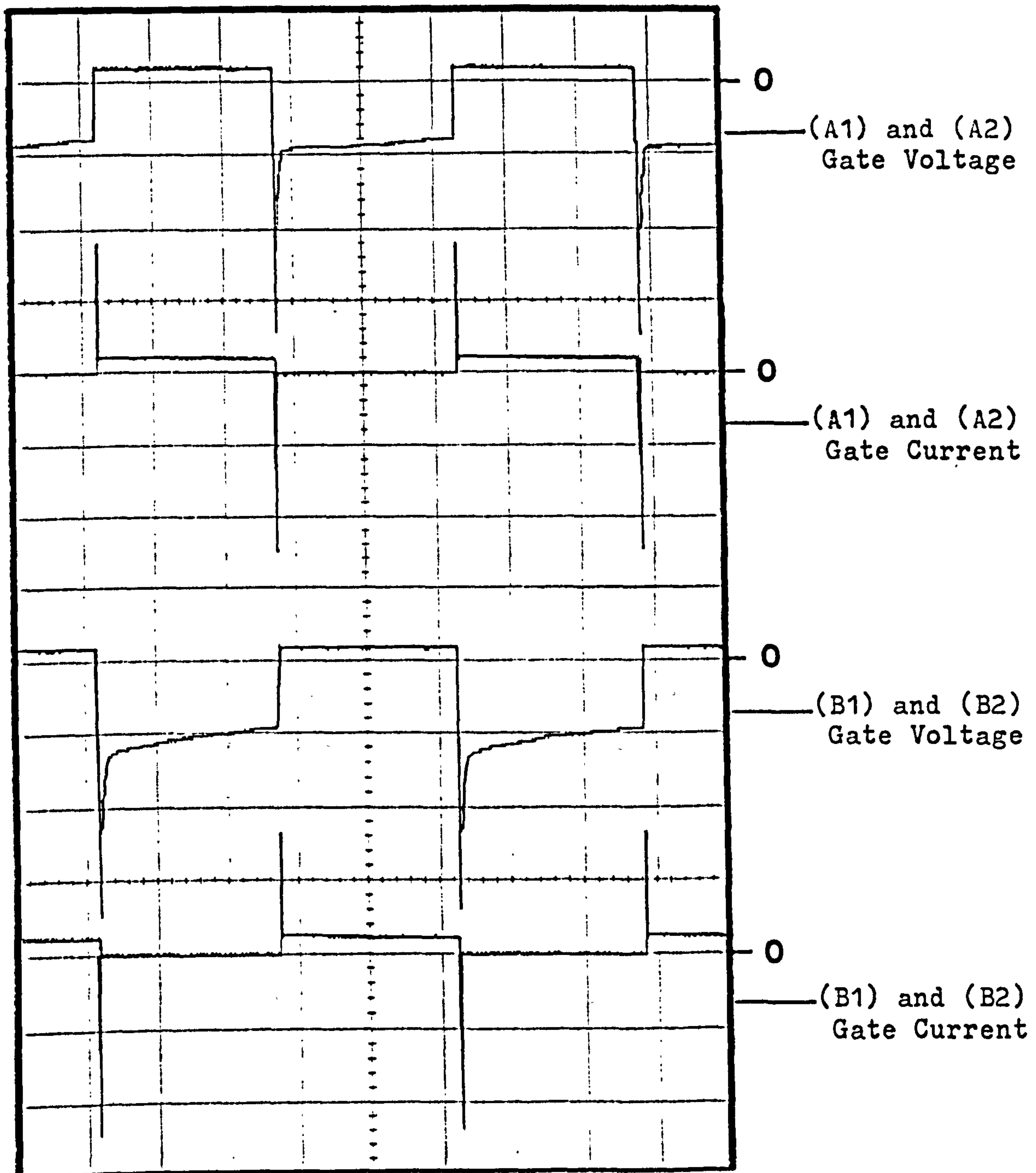
Figure 4.7 Initial-on control signals





Time Scale (a and B): 2mS/div.

Figure 4.8 Control signals



Voltage Scale: 5V/div.

Current Scale: 5A/div.

Time Scale: 2mS/div.

50% Duty Cycle

Figure 4.9 GTOs gate voltages and currents

values of the stray inductances are:

Supply inductance ( $L_d$ )	$\approx 2.7\mu H$	(measured)
$L_{a1}, L_{a2}, L_{b1}, L_{b2}$	$\approx 0.15\mu H$	(estimated)
$L_{D1}, L_{D2}, L_{D3}, L_{D4}$	$\approx 0.3\mu H$	(estimated)
$L_{d3}, L_{d4}$	$\approx 0.3\mu H$	(estimated)
$L_s$	$\approx 0.15\mu H$	(estimated)

In all results, the current directions are shown with respect to the GTO anode current directions.

#### 4.5.1 Turn-on transients

##### a) GTO thyristors gated with zero initial load current

If the load current falls to zero during freewheeling or feedback, all four GTOs are blocking prior to turn-on, each supporting half the supply voltage ( $E_d / 2$ ). The turn-on process is divided into three time intervals as follows.

**Interval  $t_1$ :** When GTOs A1 and A2 are gated on, the equivalent circuit is as that shown in Figure 4.10(a) with the state equations representing this interval, which ends at the full reverse recovery of B1 snubber diode, being shown in the system matrix of Figure 4.10(b).

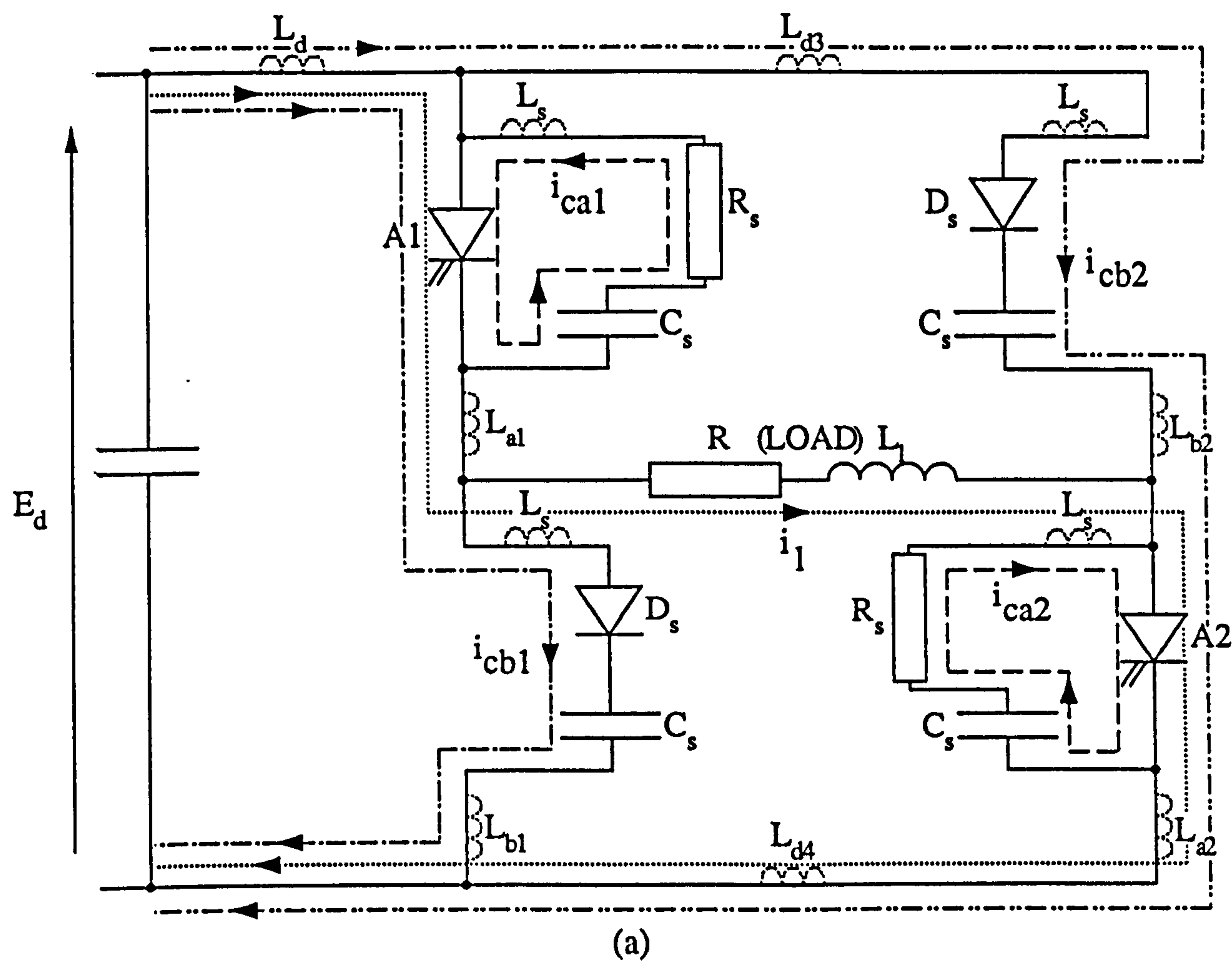
The snubber capacitors of GTOs A1 and A2 start discharging locally through them while the B1 and B2 snubber capacitor voltages rise to  $E_d$  and, owing to the path stray inductances, will overshoot by up to  $E_d / 2$  neglecting any damping (Appendix I). Hence the maximum peak voltage across the non-conducting GTOs at turn-on of the other pair is, at most,  $3E_d / 2$ .

Figure 4.11(a) and (b) shows respectively the experimental and computed results.

As the B1 and B2 snubber capacitors charge via GTOs A1 and A2 respectively, the oscillatory charging current path for that of B1 contains less stray inductance than that



Time interval t1

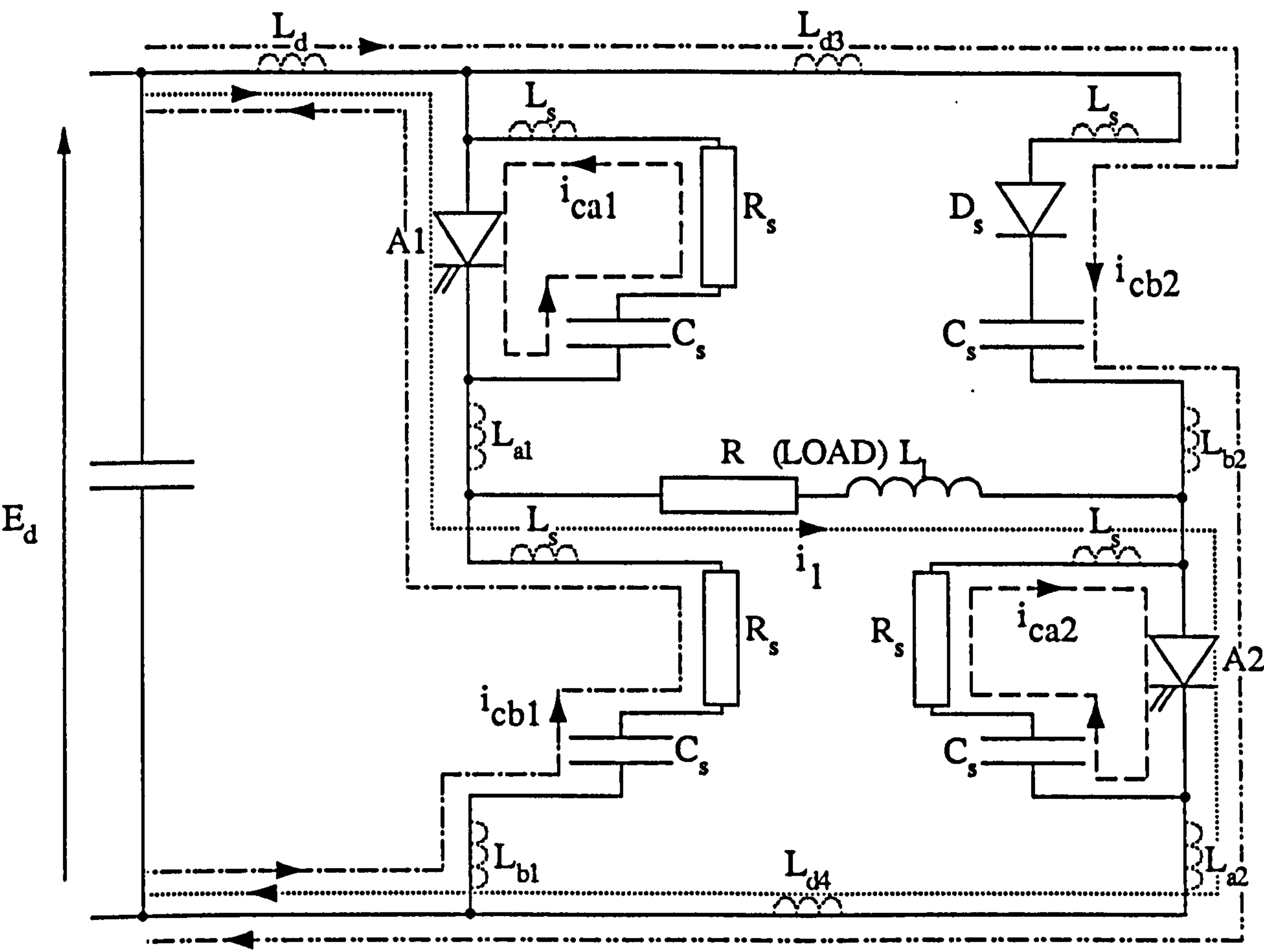


COLUMNS		(1)	(2)	(3)	(4)	(5)	(6)	(7)			
$p \ i_{ca1}$	=	$-\frac{R_s}{L_s}$	0	0	0	$\frac{1}{L_s}$	0	0	$i_{ca1}$	+ $E_d \frac{L_2}{L_1}$	
$p \ i_{cb1}$		0	0	0	$\frac{RL_3}{L_1}$	0	$-\frac{L_4}{L_1}$	$-\frac{L_5}{L_1}$	$i_{cb1}$		
$p \ i_{cb2}$		0	0	0	$\frac{RL_7}{L_1}$	0	$-\frac{L_8}{L_1}$	$-\frac{L_9}{L_1}$	$i_{cb2}$		
$p \ i_1$		0	0	0	$-\frac{RL_{12}}{L_{10}}$	0	$\frac{L_{13}}{L_{10}}$	$\frac{L_{14}}{L_{10}}$	$i_1$		$E_d \frac{L_{11}}{L_{10}}$
$p \ v_{ca1}$		$-\frac{1}{C_s}$	0	0	0	0	0	0	$v_{ca1}$		0
$p \ v_{cb1}$		0	$\frac{1}{C_s}$	0	0	0	0	0	$v_{cb1}$		0
$p \ v_{cb2}$		0	0	$\frac{1}{C_s}$	0	0	0	0	$v_{cb2}$		0

(b)

Figure 4.10 Equivalent circuits and state equations matrices for GTOs A1 and A2 turning on together (zero initial load current)

Time interval  $t_2$



(c)

COLUMNS	(1)	(2)	(3)	(4)	(5)	(6)	(7)
$p\ i_{ca1}$		0					
$p\ i_{cb1}$		$-\frac{R_s L_4}{L_1}$					
$p\ i_{cb2}$		$-\frac{R_s L_8}{L_1}$					
$p\ i_1$		$\frac{R_s L_{13}}{L_{10}}$					
$p\ v_{ca1}$		0					
$p\ v_{cb1}$		$\frac{1}{C_s}$					
$p\ v_{cb2}$		0					

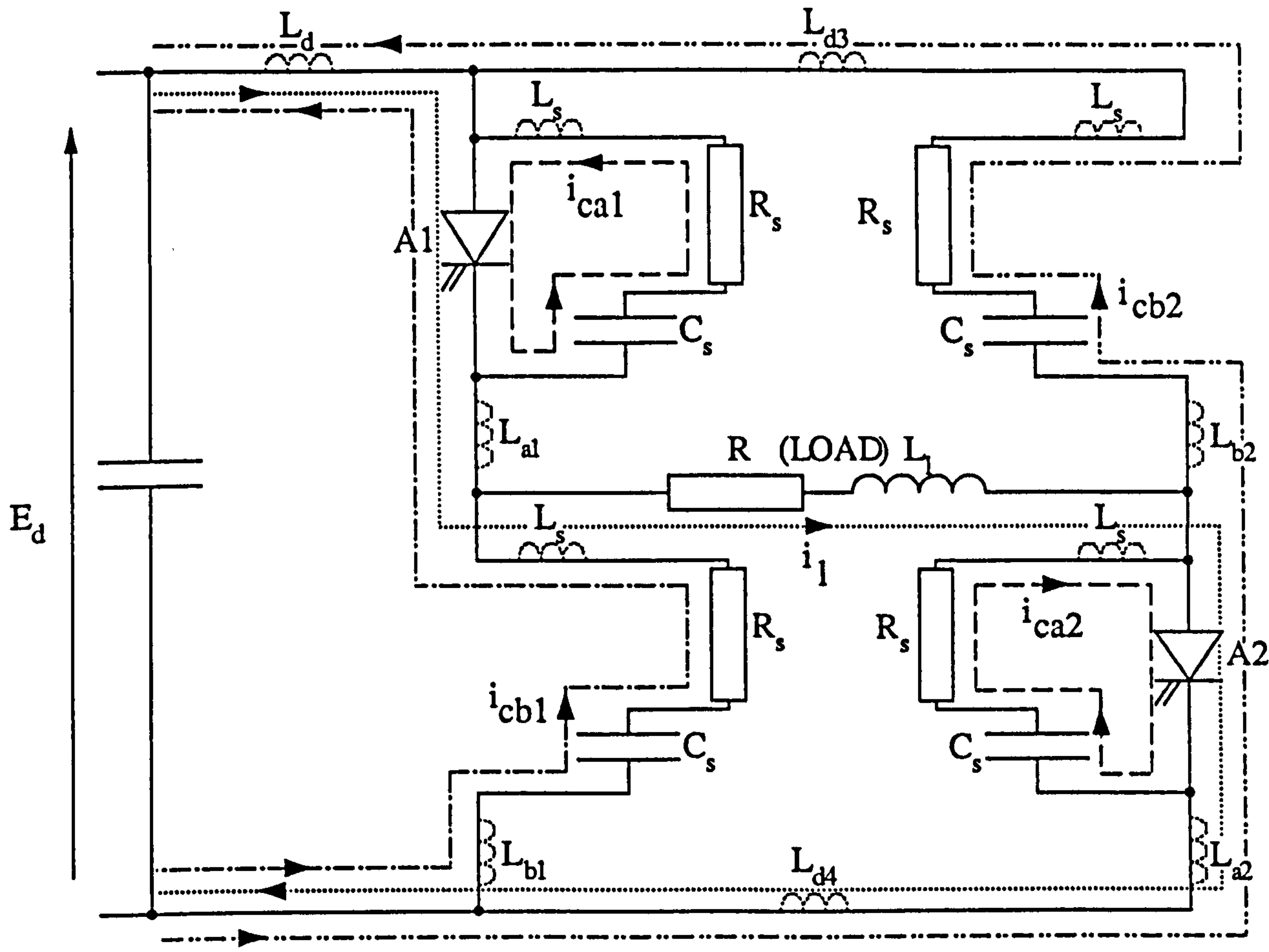
(Columns 1, and 3 to 7 as in (b))

$i_{ca1}$	0
$i_{cb1}$	$E_d \frac{L_2}{L_1}$
$i_{cb2}$	$E_d \frac{L_6}{L_1}$
$i_1$	$+ E_d \frac{L_{11}}{L_{10}}$
$v_{ca1}$	0
$v_{cb1}$	0
$v_{cb2}$	0

(d)

Figure 4.10 Equivalent circuits and state equations matrices for GTOs A1 and A2 turning on together (zero initial load current)

Time interval t3



(e)

COLUMNS	(1)	(2)	(3)	(4)	(5)	(6)	(7)
---------	-----	-----	-----	-----	-----	-----	-----

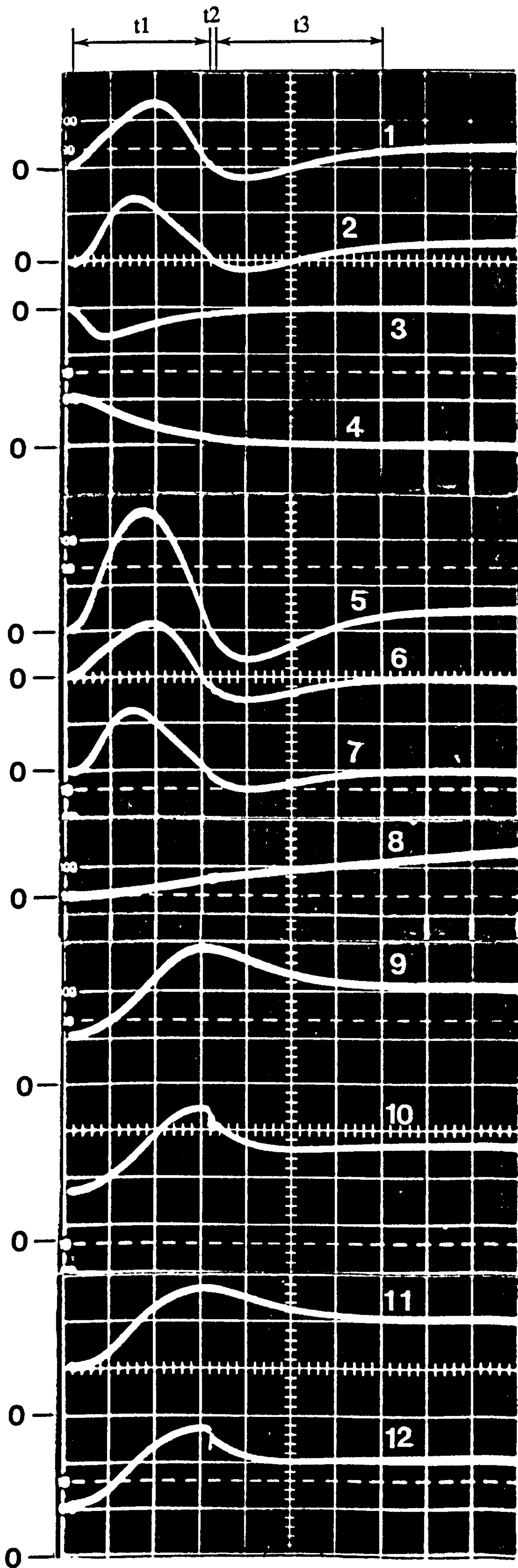
$$\begin{bmatrix} p i_{ca1} \\ p i_{cb1} \\ p i_{cb2} \\ p i_1 \\ p v_{ca1} \\ p v_{cb1} \\ p v_{cb2} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ -\frac{R_s L_4}{L_1} & -\frac{R_s L_5}{L_1} \\ -\frac{R_s L_8}{L_1} & -\frac{R_s L_9}{L_1} \\ \frac{R_s L_{13}}{L_{10}} & \frac{R_s L_{14}}{L_{10}} \\ 0 & 0 \\ \frac{1}{C_s} & 0 \\ 0 & \frac{1}{C_s} \end{bmatrix} \begin{bmatrix} i_{ca1} \\ i_{cb1} \\ i_{cb2} \\ i_1 \\ v_{ca1} \\ v_{cb1} \\ v_{cb2} \end{bmatrix} + \begin{bmatrix} 0 \\ E_d \frac{L_2}{L_1} \\ E_d \frac{L_6}{L_1} \\ E_d \frac{L_{11}}{L_{10}} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

(Columns 1, and 4 to 7 as in (b))

(f)

Figure 4.10 Equivalent circuits and state equations matrices for GTOs A1 and A2 turning on together (zero initial load current)





(1) A1 Branch Current  
(20A/div.)

(2) A2 Branch Current  
(20A/div.)

(3) A1 Snubber Capacitor  
Current (20A/div.)

(4) A1 Snubber Capacitor  
Voltage (100V/div.)

(5) Supply Current  
(20A/div.)

(6) B1 Snubber Capacitor  
Current (20A/div.)

(7) B2 Snubber Capacitor  
Current (20A/div.)

(8) Load Current  
(5A/div.)

(9) B1 Snubber Capacitor  
Voltage (100V/div.)

(10) B1 A-K Voltage  
(100V/div.)

(11) B2 Snubber Capacitor  
Voltage (100V/div.)

(12) B2 A-K Voltage  
(100V/div.)

Time Scale: 2 $\mu$ S/div.

(a) Experimental Results

Figure 4.11 Waveforms at GTOs A1 and A2 turn-on together (zero initial load current)



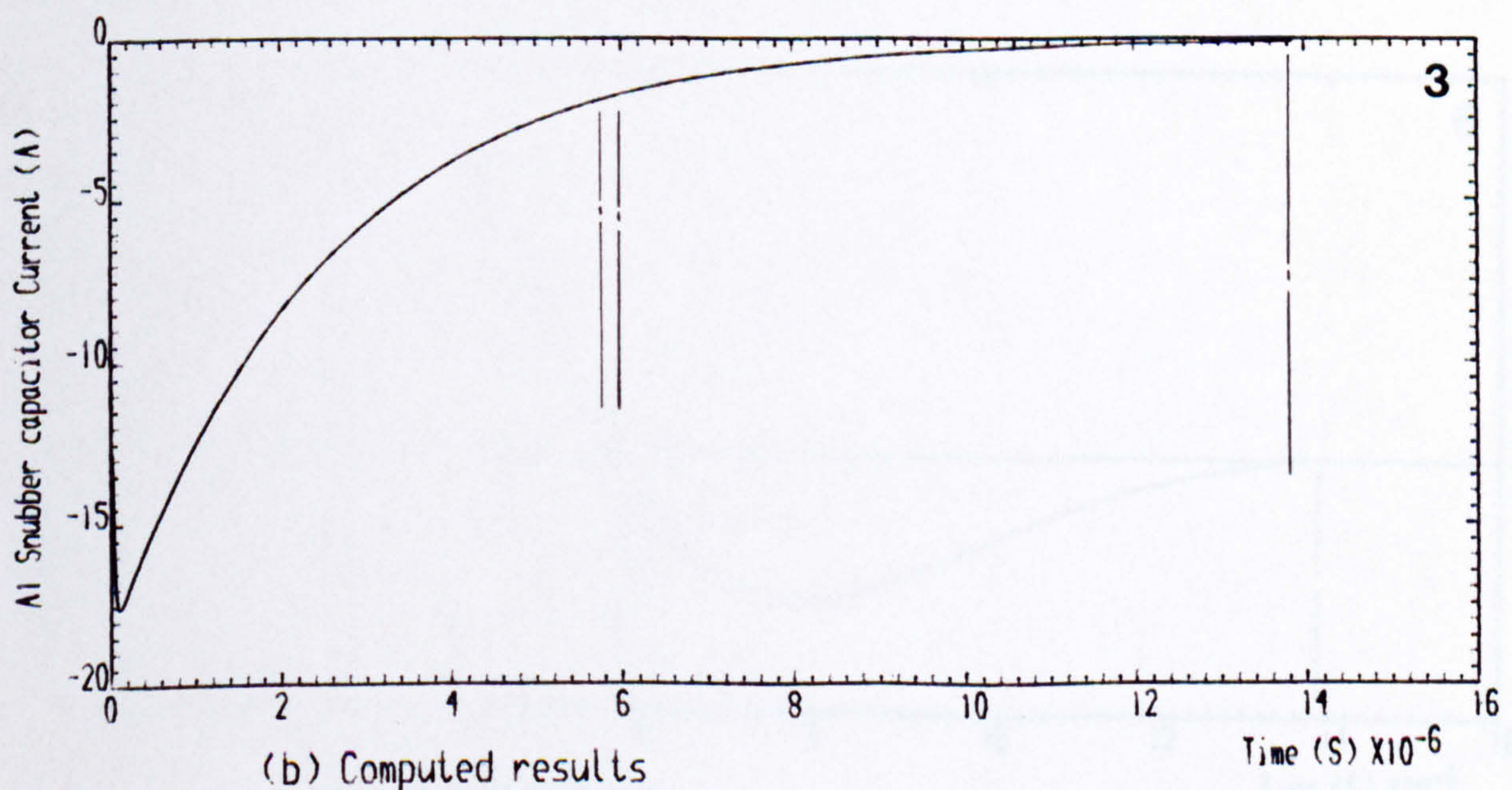
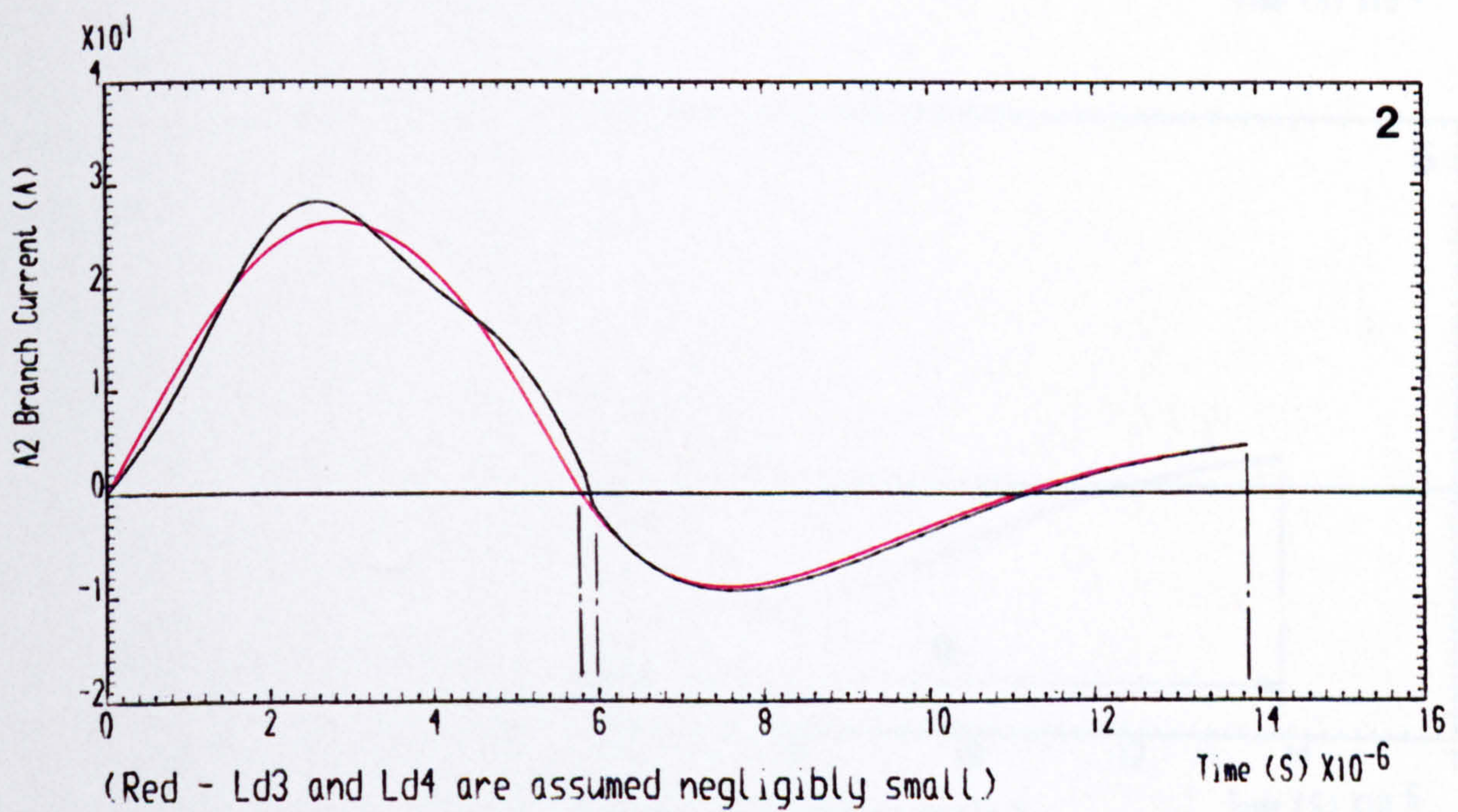
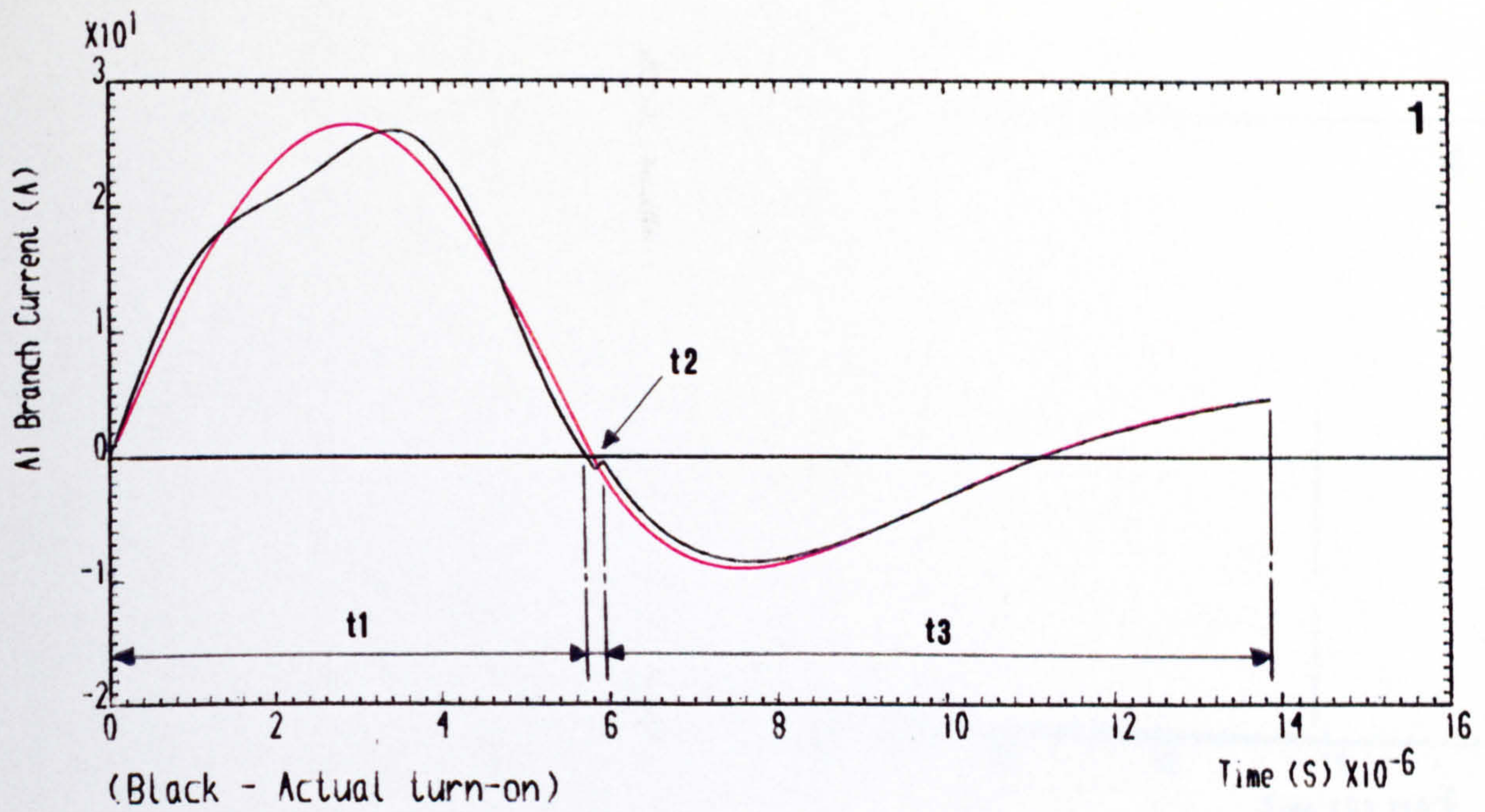


Figure 4.11 WaveForms at GTOs A1 and A2 turn-on together (zero initial load current)

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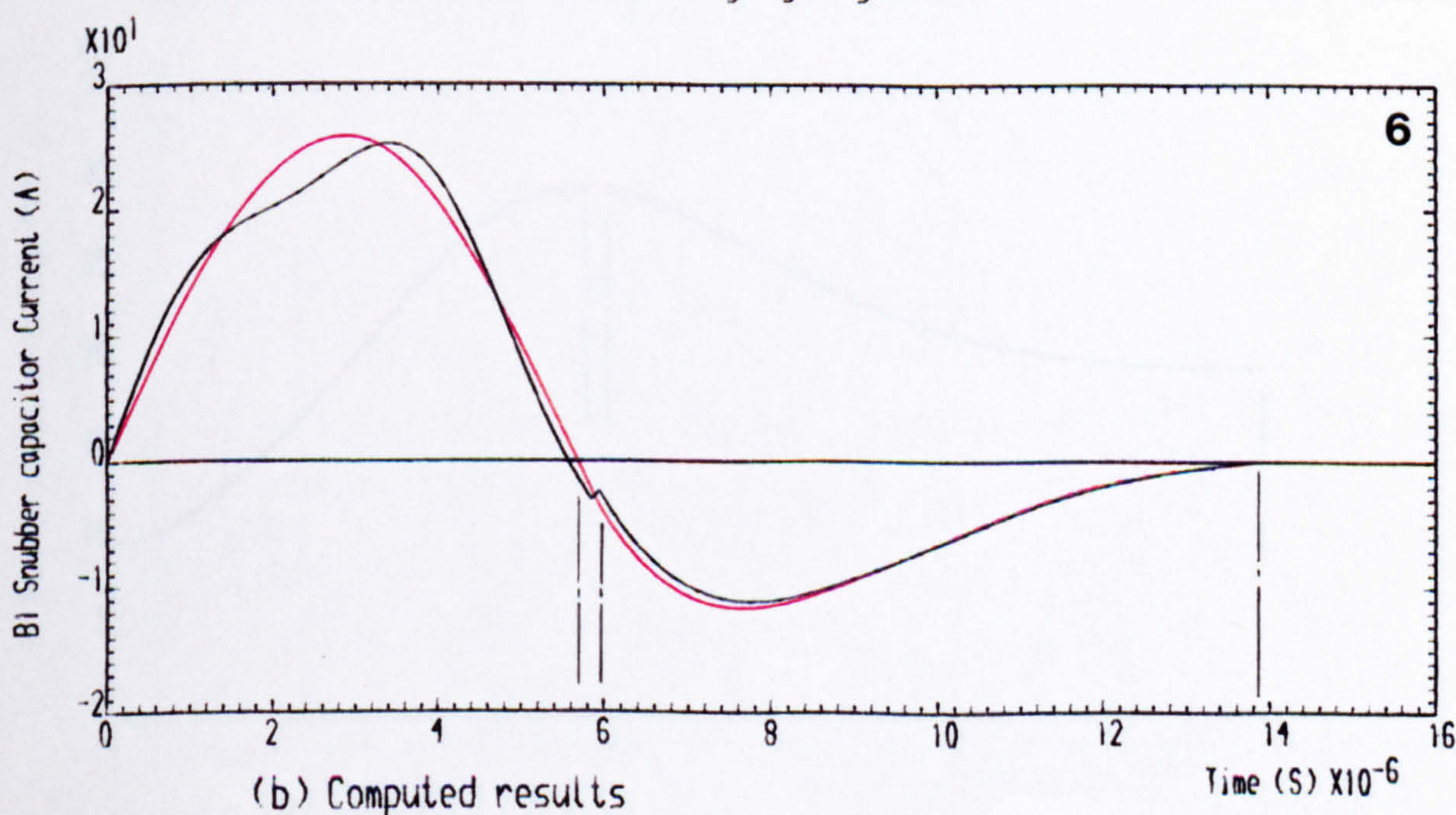
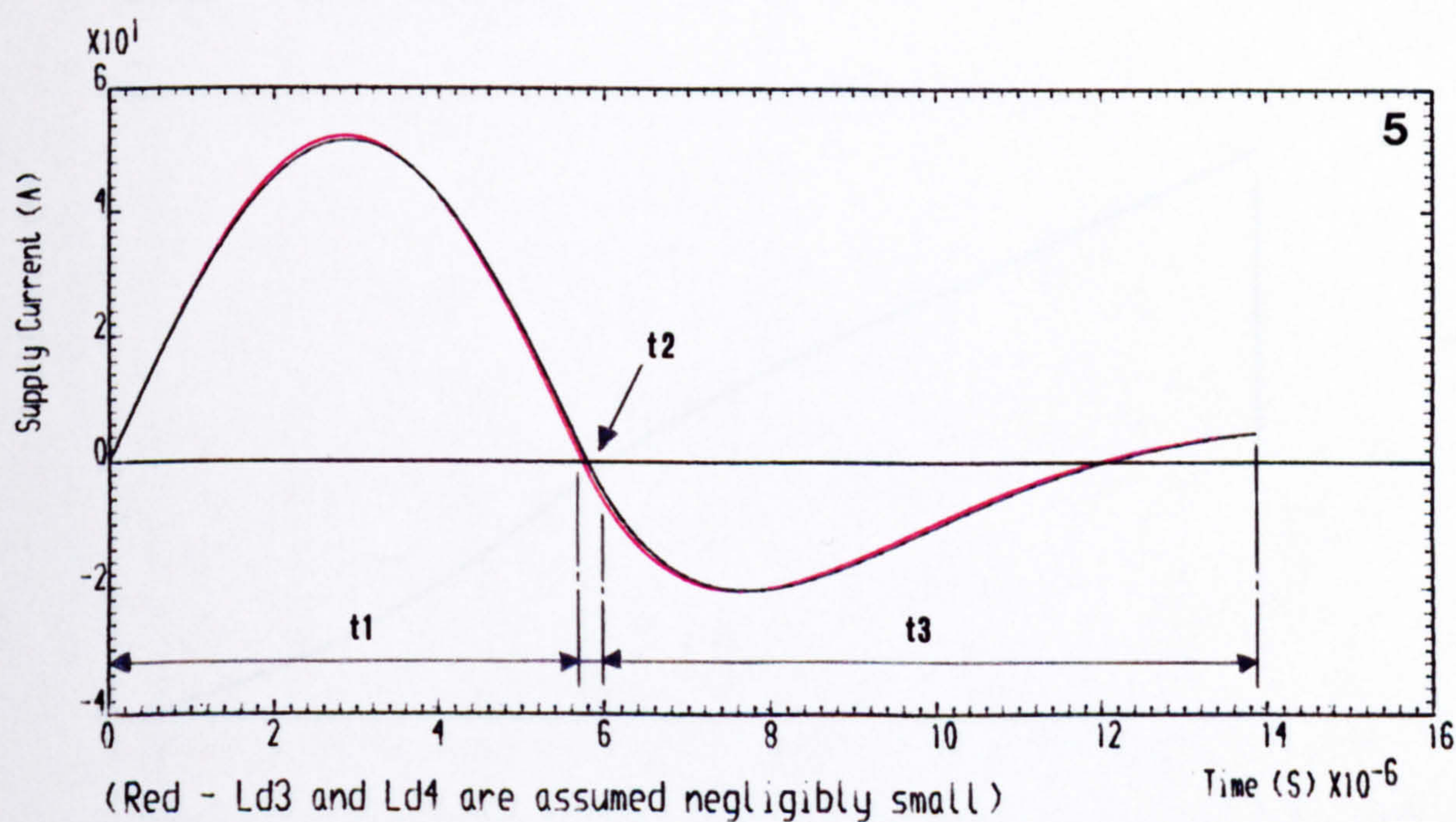
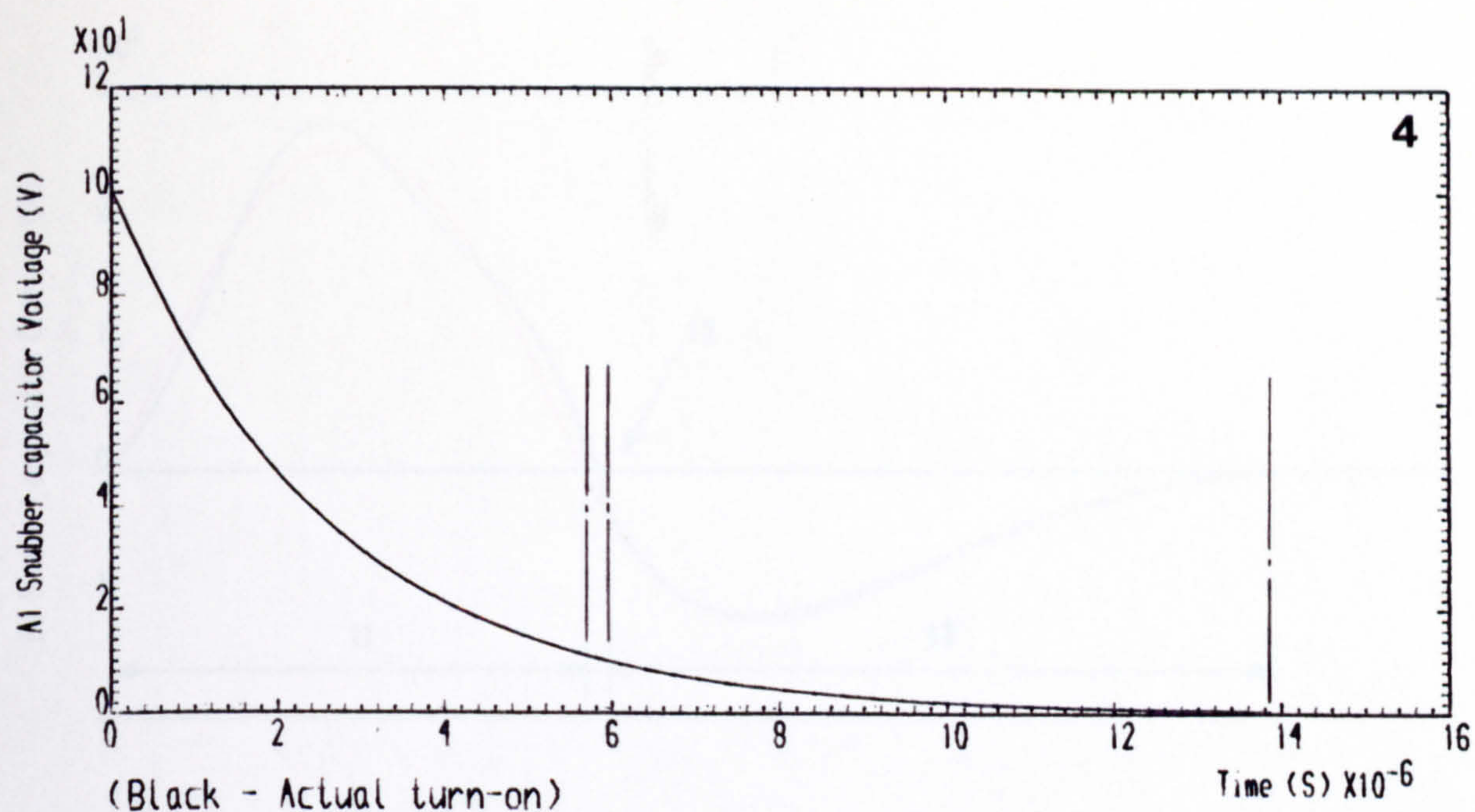


Figure 4.11 WaveForms at GTOs A1 and A2 turn-on together (zero initial load current)

CONTINUED ..



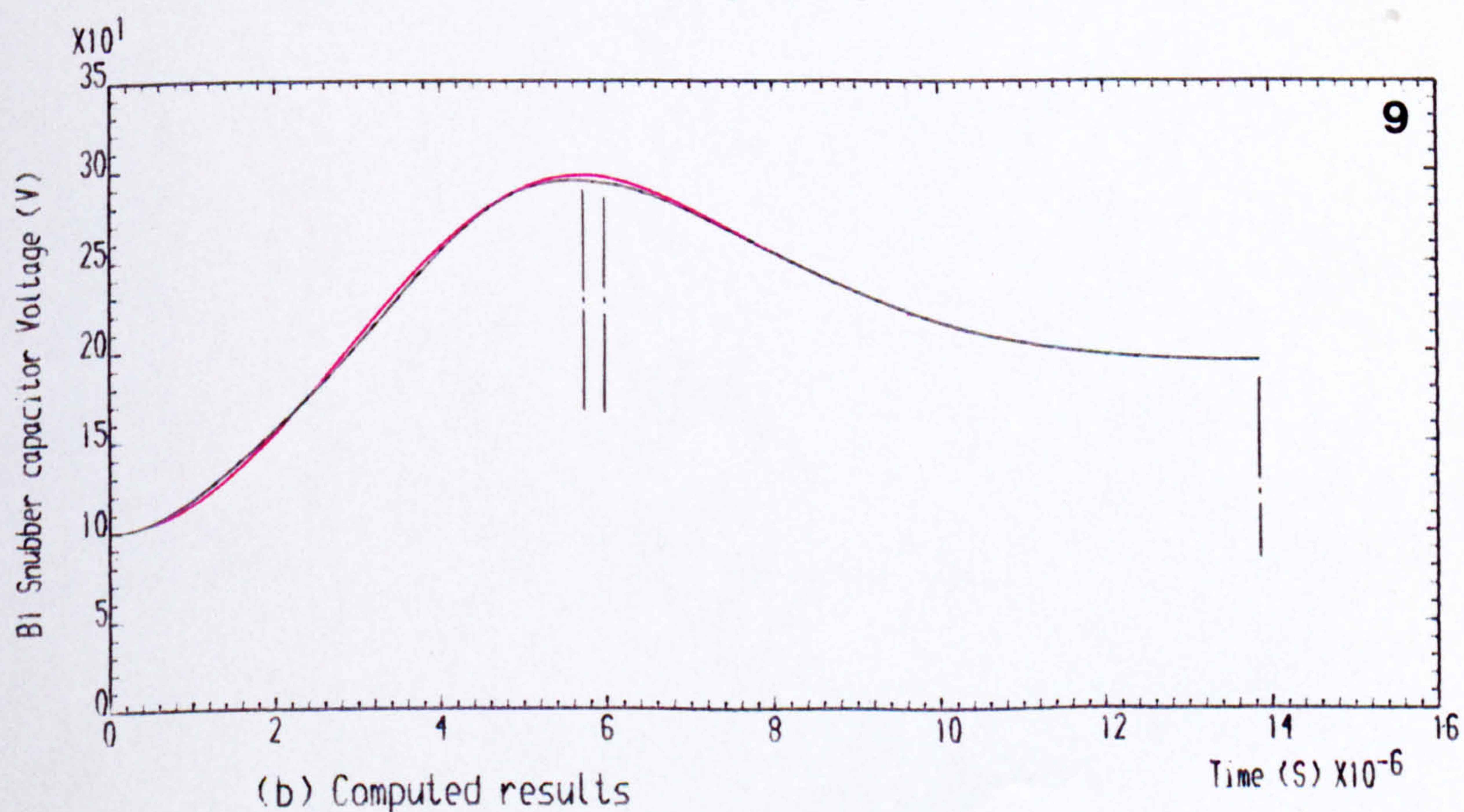
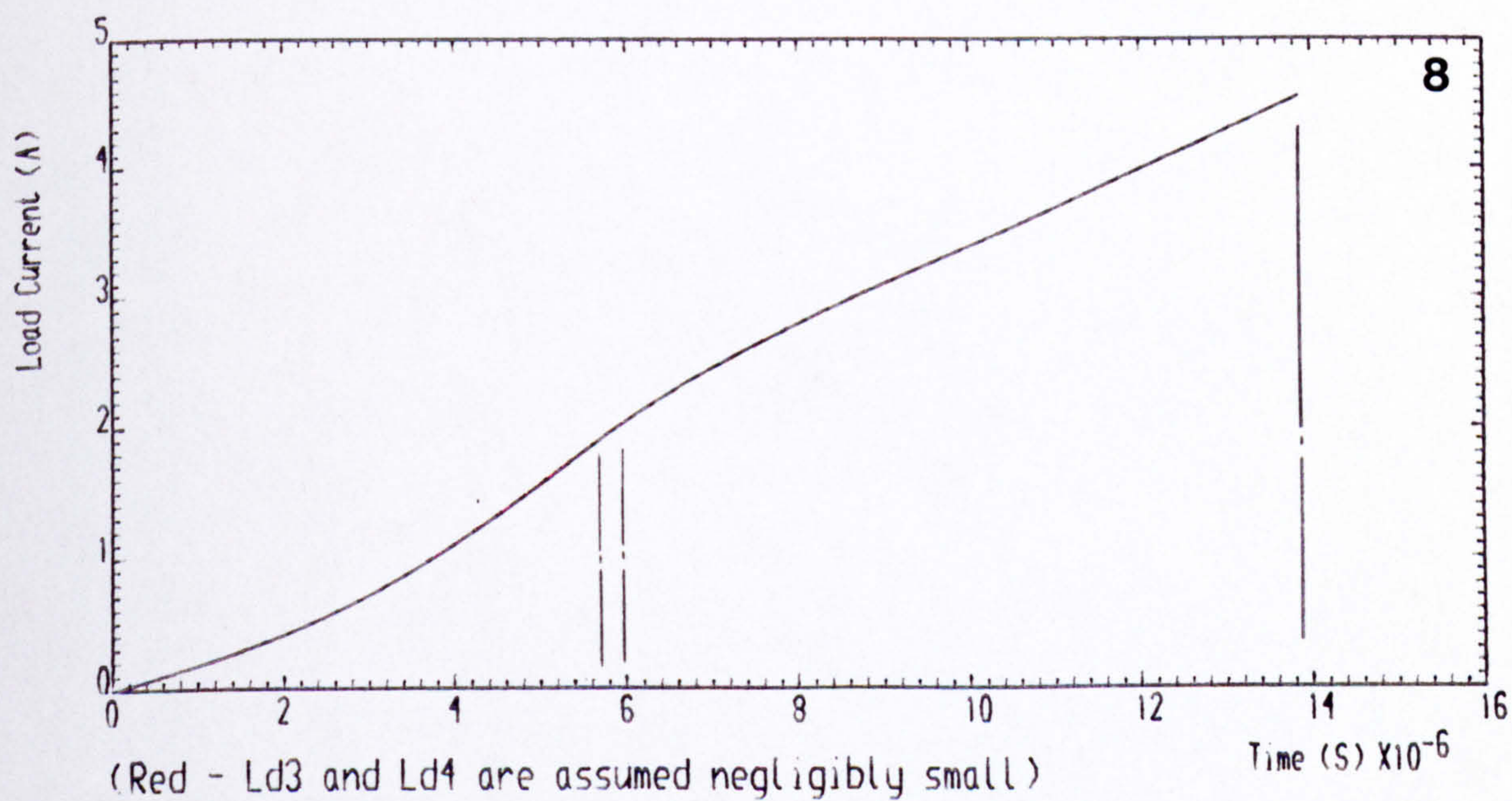
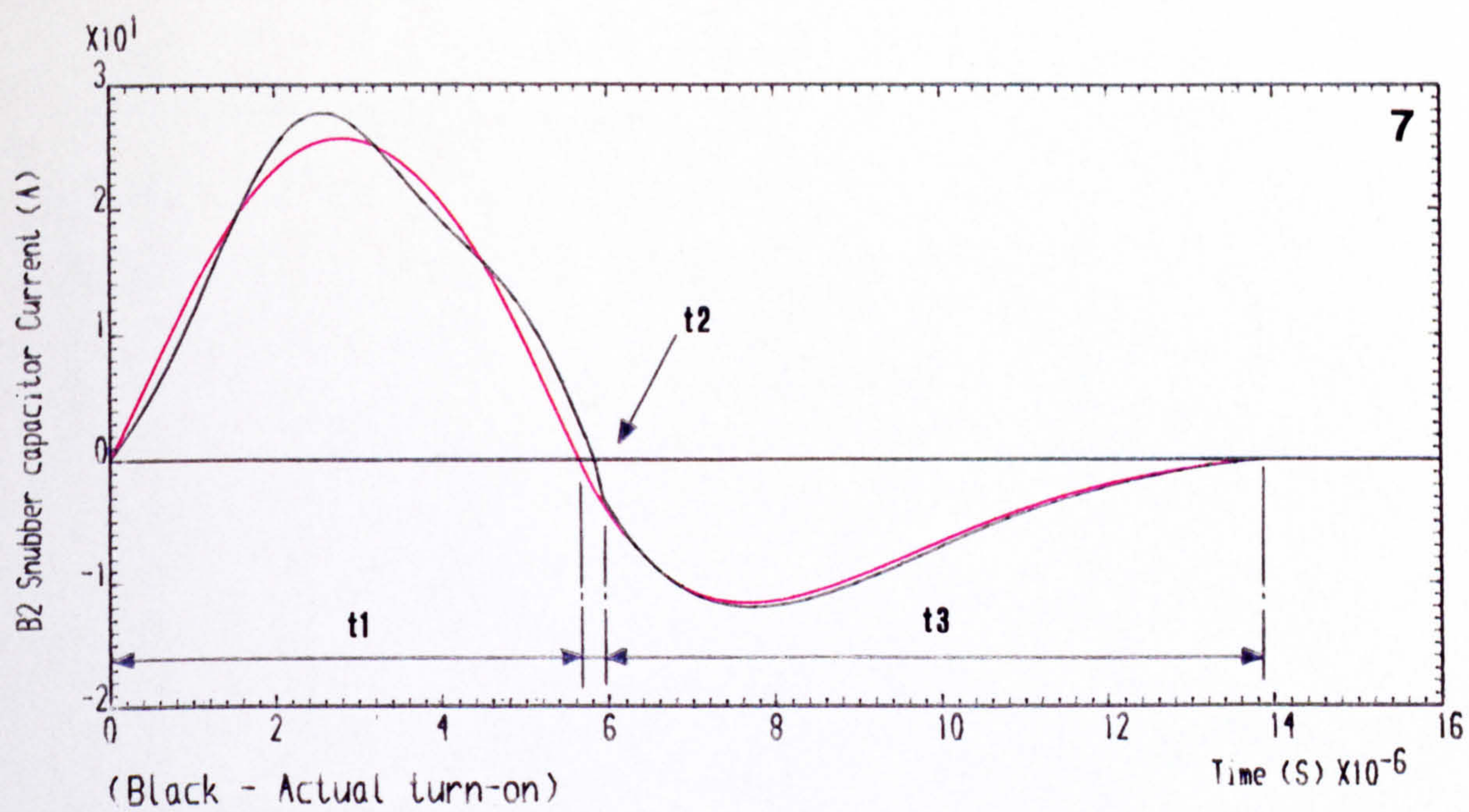


Figure 4.11 Waveforms at GTOs A1 and A2 turn-on together (zero initial load current)

CONTINUED ..



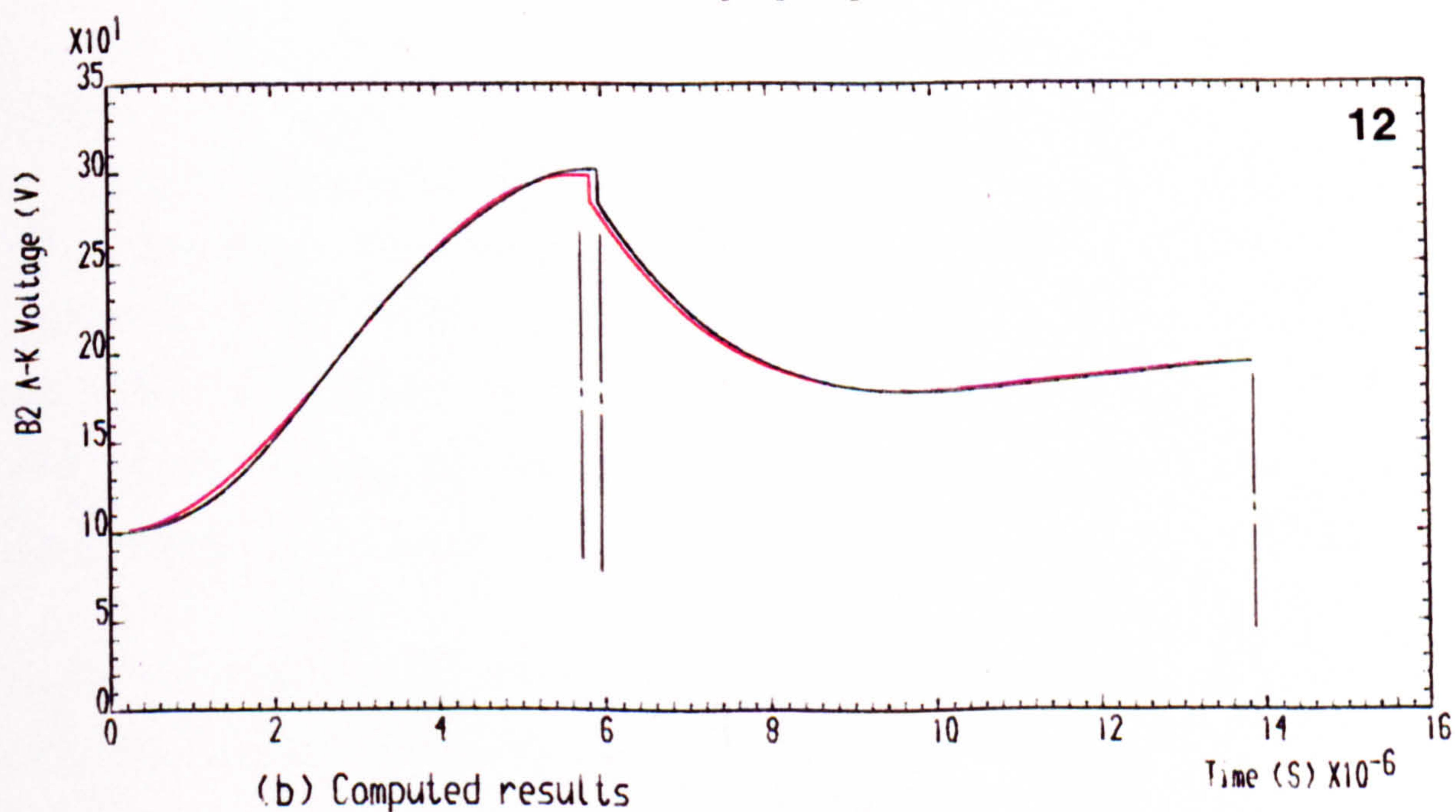
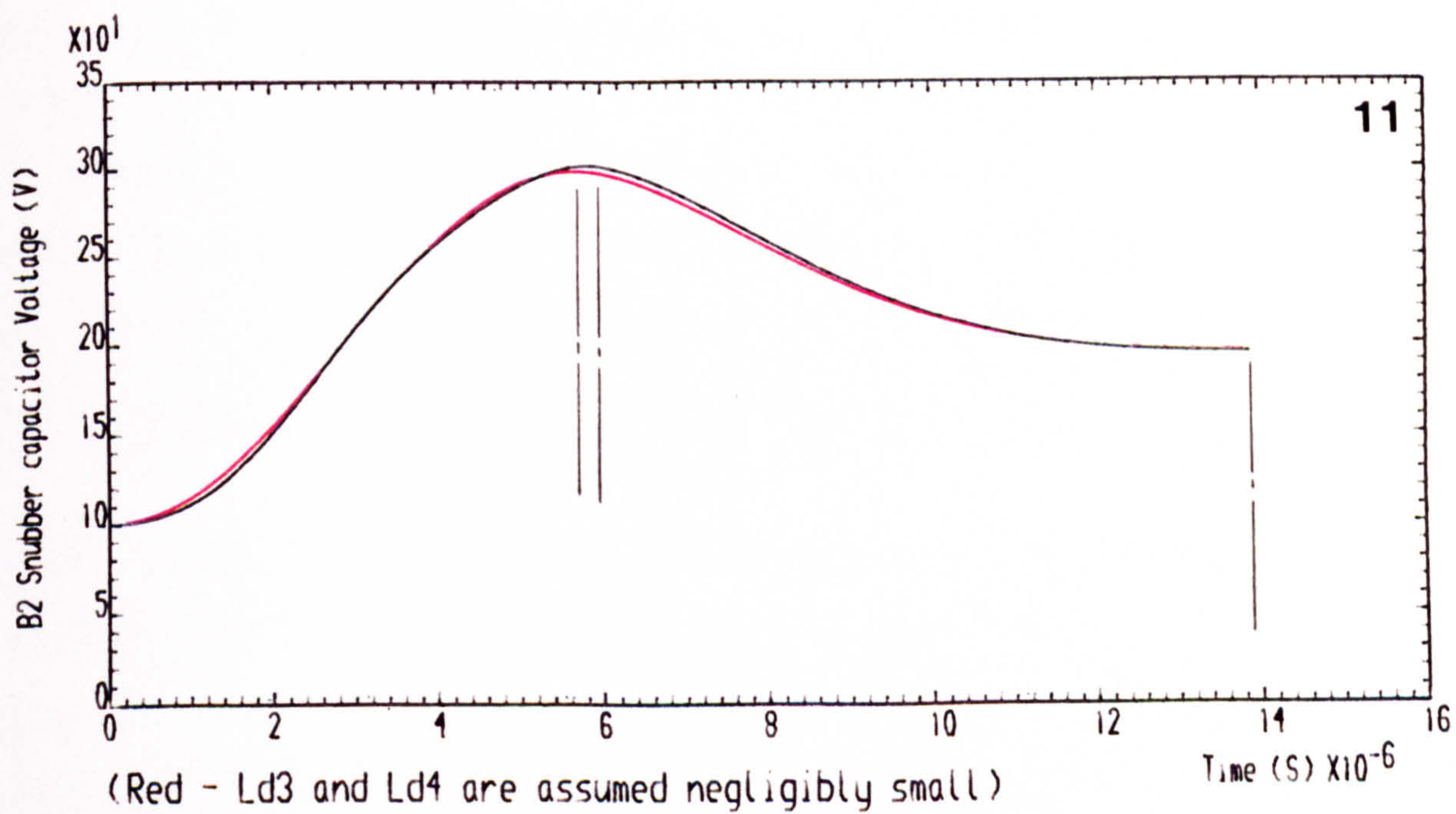
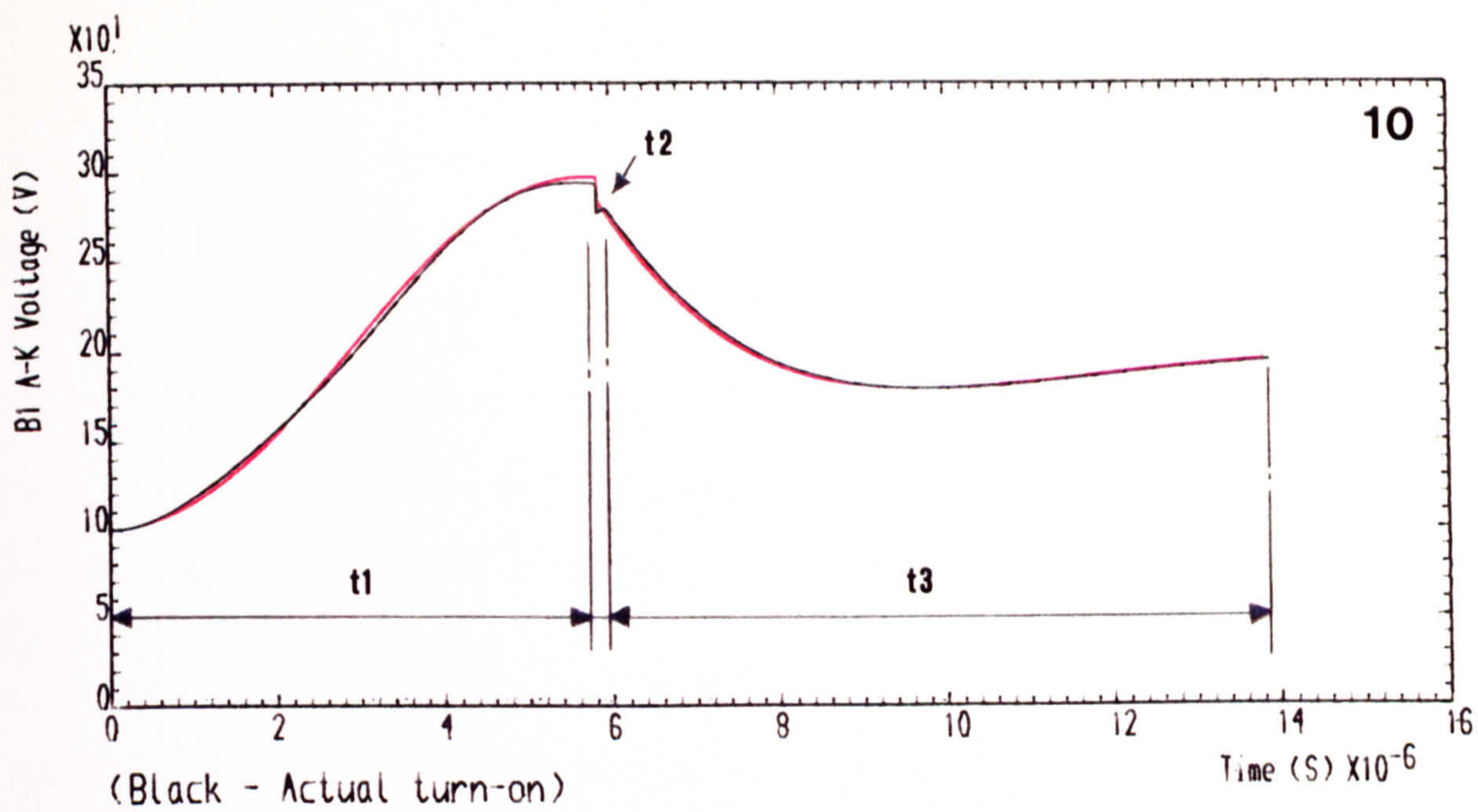


Figure 4.11 WaveForms at GTOs A1 and A2 turn-on together (zero initial load current)

END ..



of B2 by an amount ( $L_{d3} + L_{d4}$ ), giving the difference in the waveform oscillation as shown by traces (6) and (7) of Figure 4.11(a) and (b). The red traces of the latter show the predicted waveforms when the strays  $L_{d3}$  and  $L_{d4}$  are assumed negligibly small, the two capacitor currents then being identical.

The rate of rise of the load current ( $i_l$ ) is controlled mainly by the load inductance, i.e.  $E_d / L_l$  initially, which approximates to  $0.3 \text{ A}/\mu\text{s}$  but, as the voltage across GTO B1 overshoots  $E_d$ , due mainly to the induced voltage across  $L_d$  caused by the oscillatory supply current decaying in it, a slightly faster rate is experienced (Figure 4.11, trace (8)).

At B1 snubber capacitor full charge, its series snubber diode undergoes reverse recovery, with its current rising against that of the GTO A1 branch as well as maintaining the load current (via GTO A2), while GTO B2 snubber capacitor completes its charging due to its longer oscillation period with  $L_{d3}$  and  $L_{d4}$  present in the current path. The latter experiences a slightly higher voltage oscillation peak than that across B1 snubber capacitor. The voltage contribution by  $L_{d3}$  and  $L_{d4}$  to GTO B2 voltage is small, but becomes significant if the values of  $L_{d3}$  and  $L_{d4}$  become relatively large.

**Interval  $t_2$ :** This very short interval lasts from the reverse recovery of B1 snubber diode to the reverse recovery of B2 snubber diode. The latter is later due to  $L_{d3}$  and  $L_{d4}$  giving increased oscillation time. The equivalent circuit and its state equations become as shown respectively in Figure 4.10(c) and (d). The B1 snubber capacitor current, having diverted from the snubber diode to the resistor, produces a voltage drop across GTO B1, Figure 4.11 (trace 10). But as the voltage across GTO B2 is now higher than that across GTO B1, a large rapid voltage reduction across B1 is prevented. This is due to the overcharged B2 snubber capacitor voltage being coupled, via the DC rails to GTO B1, maintaining its voltage to nearly that across GTO B2. Traces (10) and (12) show the very short interval  $t_2$ . This interval, which becomes larger with increased  $L_{d3}$  and/or  $L_{d4}$ , will be referred to as the 'hold-up' period subsequently.

During B2 snubber diode reverse recovery its current, with that of the B1 snubber capacitor discharge, contributes to the slowly rising load current.



**Interval t3:** This starts as the B2 snubber diode is fully reverse recovered, and ends when the B1 and B2 snubber capacitor discharge currents reach zero (Figure 4.11, trace (6) and (7)). The equivalent circuit and the state equations are given in Figure 4.10(e) and (f) respectively. Here, after diode reverse recovery, the B2 snubber capacitor current has diverted to its snubber resistor, dropping the voltage across GTO B2 by the  $IR$  drop. The B1 snubber capacitor discharge current is now rising again in its snubber resistor. The voltages across GTOs B1 and B2, therefore, decay by overdamped oscillation to the supply value  $E_d$ , Figure 4.11, traces (10) and (12).

An important feature is that GTOs A1 and A2 can experience zero current when the rising discharge currents of B1 and B2 snubber capacitors exceed the small load current plus the A1 and A2 snubber capacitor discharge currents respectively. GTOs A1 and A2 subsequently take over the load current again as they are provided with a BP drive.

Interval t3 is followed by GTOs B1 and B2 each blocking the supply voltage ( $E_d$ ), with the load current continuing its rise to its steady state value (approximately 90A) via GTOs A1 and A2.

The effective stray inductances are principally those of the source and the bridge outer loops with the smaller values in the arms and snubber loops having a marginal effect.

#### **b) GTO thyristors gated from the freewheeling condition**

This is not valid because all GTOs must be turned off before a complementary pair can be gated so that a shoot-through condition (say GTOs A1 and B1 conducting together) is avoided [26].

#### **c) GTO thyristors gated from the feedback condition**

Here there will be no switching transients. The load voltage reversal occurs when diodes D3 and D4 (say) take the load current from GTOs A1 and A2. The current reversal instant depends on the load time constant and, providing GTOs B1 and B2 have a BP drive, they will automatically come into conduction then, with the circuit potentials already having been established [26].

#### 4.5.2 Turn-off transients

Here the simultaneous fall of GTO anode current and rise of snubber current is identical with that described in sub-section 3.2.1(a), and will be adopted as time interval  $t_1$  in all cases.

##### a) At single GTO thyristor A2 turn-off

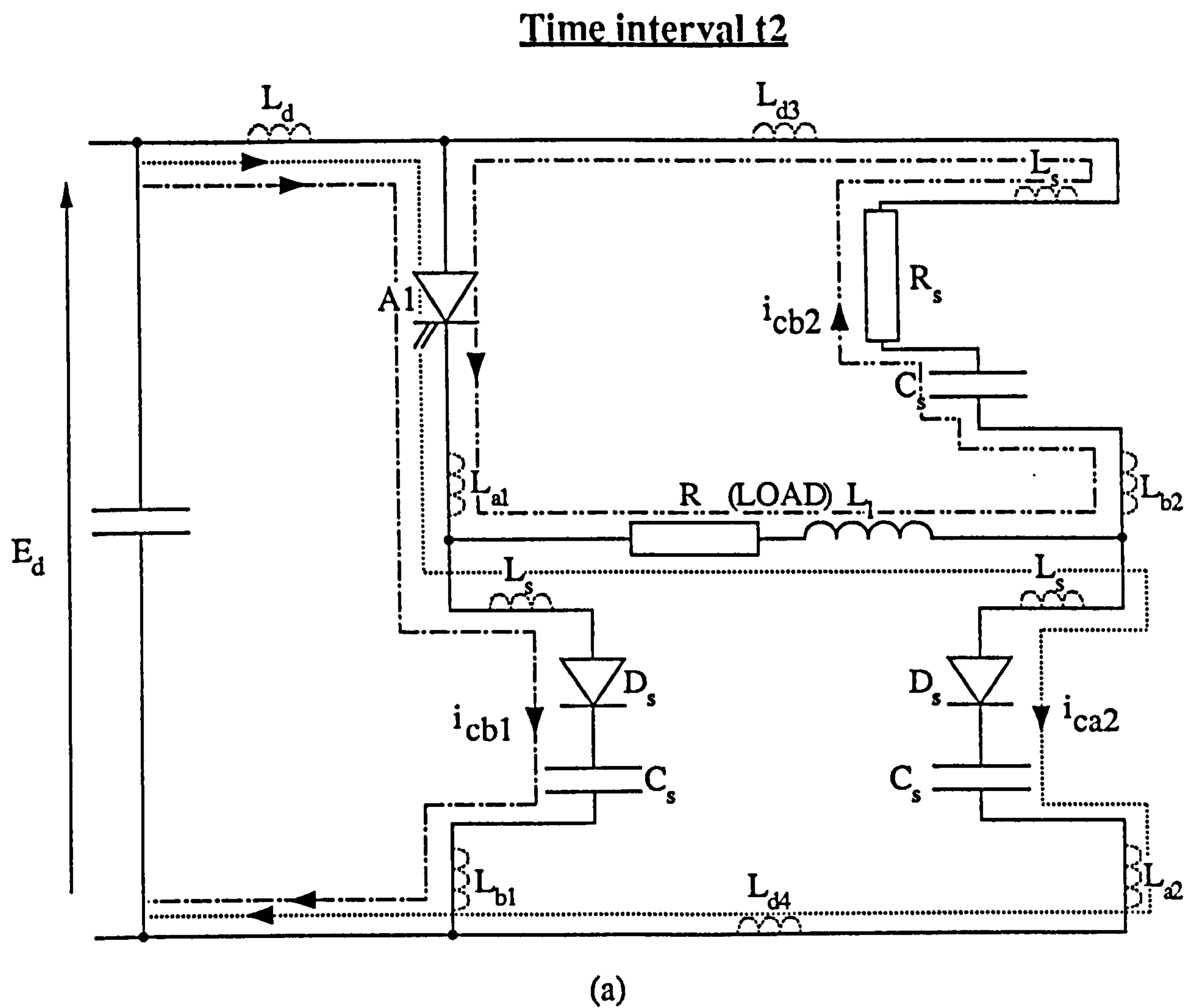
Referring to Figure 4.1, let GTOs A1 and A2 be conducting. Consider A2 interrupting the load current, with interval  $t_1$  completed.

**Interval  $t_2$ :** Figure 4.13(a) and (b) provides respectively the experimental and computed results, with Figure 4.12(a) and (b) showing the equivalent circuit and its state system matrix. This interval begins when the peak diverted A2 snubber capacitor current is reached, and ends as the voltage across GTO B2 decays to zero, Figure 4.13 traces (1) and (6).

As GTO A2 anode current is completely diverted into its snubber, apart from the small tail current, the voltage across the snubber capacitor builds up. The B2 snubber capacitor (originally charged to the supply voltage  $E_d$ ) discharges, the constant load current dividing between the A2 and B2 branches. The rising B2 branch current freewheels through GTO A1, the supply current falls and the resulting induced  $L_d di/dt$  lifts the bridge DC rail voltage above  $E_d$  giving an oscillatory overcharging of B1 snubber capacitor through GTO A1. This is demonstrated in Figure 4.13, traces (3) and (14). As this interval approaches its end, the A2 snubber capacitor exceeds  $E_d$  due to  $L_d$ ,  $L_{d3}$  and  $L_{d4}$ .

**Interval  $t_3$ :** Diode D3 now commences conduction indicating the start of this interval which ceases at the full reverse recovery of the A2 snubber diode. The equivalent circuit and state equations are shown in Figures 4.12(c) and (d). The rising B2 branch current flow is now being taken over by diode D3 from the parallel snubber capacitor, (Figure 4.13, traces (10) and (11)), the rate of its rise being controlled by  $L_{D3}$  and  $L_s$ . The A2 snubber capacitor current fall rate increases, having previously fallen from the initial value diverted from GTO A2 to  $I_o$ , Figure 4.13, trace (1). Its voltage further overshoots  $E_d$  to its peak value, trace (4). Since the diversion of load current into the freewheeling path is now more rapid, the B1 voltage overshoot



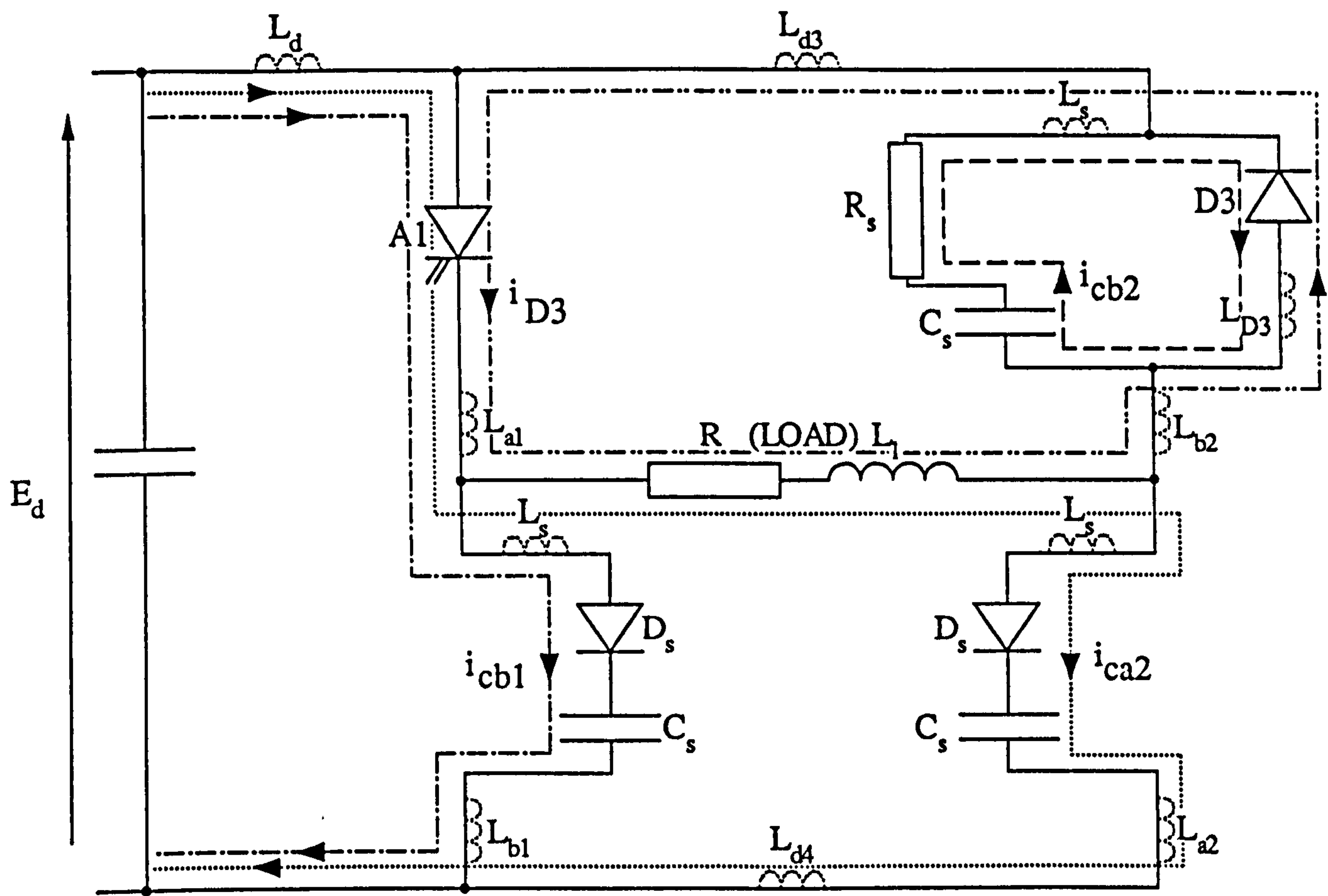


COLUMNS	(1)	(2)	(3)	(4)	(5)	(6)		
$\begin{bmatrix} p \ i_{ca2} \\ p \ i_{cb1} \\ p \ i_{cb2} \\ p \ v_{ca2} \\ p \ v_{cb1} \\ p \ v_{cb2} \end{bmatrix}$	$=$	$\begin{bmatrix} -R \frac{L_3}{L_2} & 0 & -\left(R \frac{L_3}{L_2} + R_s \frac{L_4}{L_2}\right) & -\frac{L_5}{L_2} & \frac{L_6}{L_2} & -\frac{L_4}{L_2} \\ R \frac{L_{14}}{L_{12}} & 0 & -\left(R \frac{L_{14}}{L_{12}} - R_s \frac{L_{17}}{L_{12}}\right) & \frac{L_{15}}{L_{12}} & -\frac{L_{16}}{L_{12}} & \frac{L_{17}}{L_{12}} \\ R \frac{L_8}{L_2} & 0 & -\left(R \frac{L_8}{L_2} - R_s \frac{L_{11}}{L_2}\right) & \frac{L_9}{L_2} & -\frac{L_{10}}{L_2} & \frac{L_{11}}{L_2} \\ \frac{1}{C_s} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_s} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_s} & 0 & 0 & 0 \end{bmatrix}$	$+$	$\begin{bmatrix} i_{ca2} \\ i_{cb1} \\ i_{cb2} \\ v_{ca2} \\ v_{cb1} \\ v_{cb2} \end{bmatrix}$	$=$	$\begin{bmatrix} E_d \frac{L_1}{L_2} \\ E_d \frac{L_{13}}{L_{12}} \\ E_d \frac{L_7}{L_2} \\ 0 \\ 0 \\ 0 \end{bmatrix}$		

(b)

Figure 4.12    Equivalent circuits and state equations matrices for A2 turning off first, (start of freewheeling)

Time interval t3



(c)

<u>COLUMNS</u>	(1)	(2)	(3)	(4)	(5)	(6)	(7)
----------------	-----	-----	-----	-----	-----	-----	-----

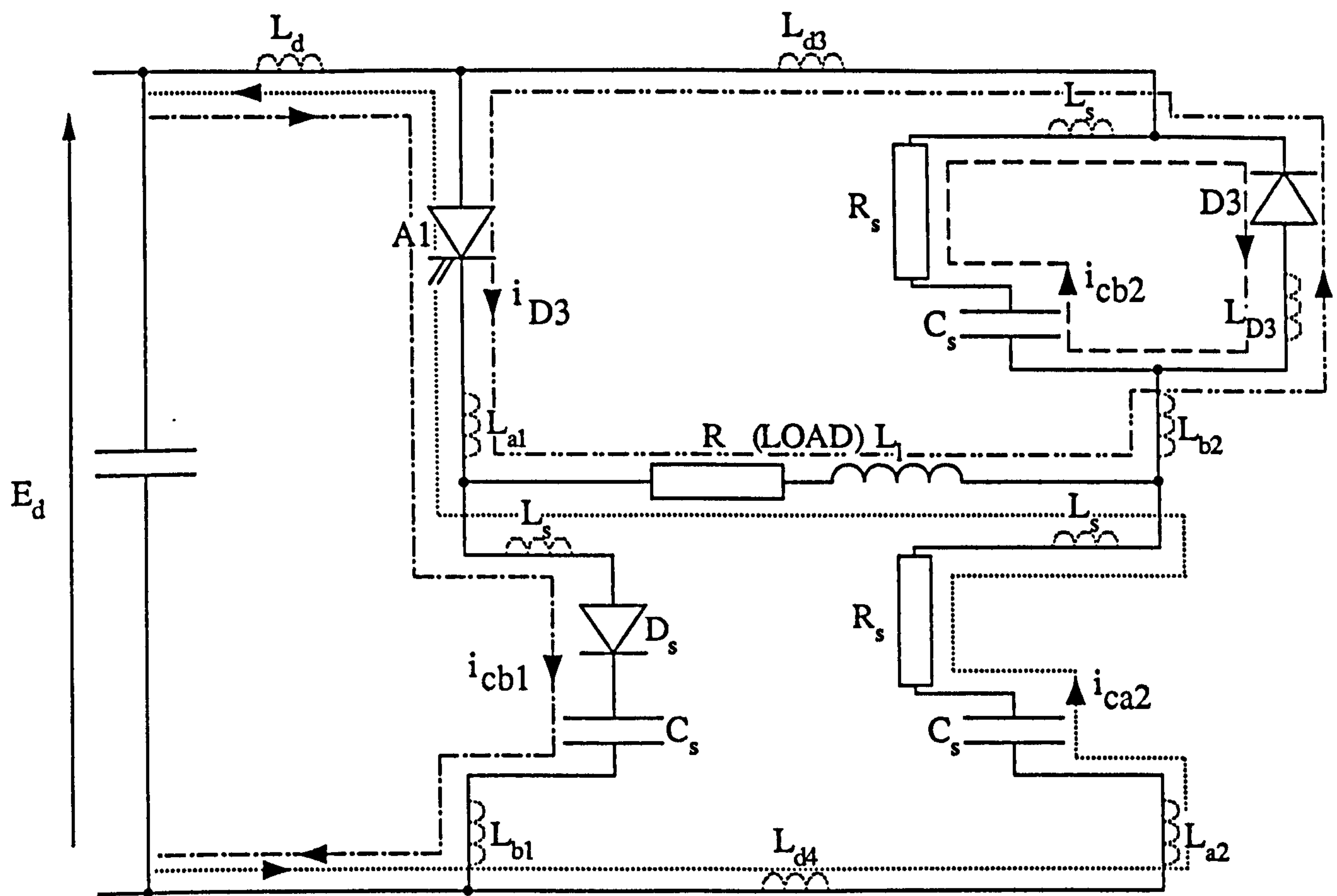
$$\begin{bmatrix} p i_{ca2} \\ p i_{D3} \\ p i_{cb1} \\ p i_{cb2} \\ p v_{ca2} \\ p v_{cb1} \\ p v_{cb2} \end{bmatrix} = \begin{bmatrix} R \frac{L_{20}}{L_{18}} - R \frac{L_{20}}{L_{18}} & 0 & - \left( R \frac{L_{20}}{L_{18}} - R_s \frac{L_{23}}{L_{18}} \right) & \frac{L_{21}}{L_{18}} - \frac{L_{22}}{L_{18}} & \frac{L_{23}}{L_{18}} \\ -R \frac{L_{30}}{L_{34}} & R \frac{L_{30}}{L_{34}} & 0 & \left( R \frac{L_{30}}{L_{34}} - R_s \frac{L_{33}}{L_{34}} \right) & -\frac{L_{31}}{L_{34}} - \frac{L_{32}}{L_{34}} & -\frac{L_{33}}{L_{34}} \\ R \frac{L_{25}}{L_{18}} - R \frac{L_{25}}{L_{18}} & 0 & - \left( R \frac{L_{25}}{L_{18}} - R_s \frac{L_{28}}{L_{18}} \right) & -\frac{L_{26}}{L_{18}} & \frac{L_{27}}{L_{18}} & \frac{L_{28}}{L_{18}} \\ R \frac{L_{37}}{L_{35}} - R \frac{L_{37}}{L_{35}} & 0 & - \left( R \frac{L_{37}}{L_{35}} - R_s \frac{L_{40}}{L_{35}} \right) & \frac{L_{38}}{L_{35}} & \frac{L_{39}}{L_{35}} & \frac{L_{40}}{L_{35}} \\ \frac{1}{C_s} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_s} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{C_s} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{ca2} \\ i_{D3} \\ i_{cb1} \\ i_{cb2} \\ v_{ca2} \\ v_{cb1} \\ v_{cb2} \end{bmatrix} + \begin{bmatrix} E_d \frac{L_{19}}{L_{18}} \\ E_d \frac{L_{29}}{L_{34}} \\ E_d \frac{L_{24}}{L_{18}} \\ -E_d \frac{L_{36}}{L_{35}} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

(d)

Figure 4.12 Equivalent circuits and state equations matrices for A2 turning off first, (start of freewheeling)



Time interval t4



(e)

COLUMNS		(1)	(2)	(3)	(4)	(5)	(6)	(7)	
$p \ i_{ca2}$	$=$	$\left( R \frac{L_{20}}{L_{18}} + R_s \frac{L_{21}}{L_{18}} \right)$							
$p \ i_{D3}$		$-\left( R \frac{L_{30}}{L_{34}} + R_s \frac{L_{31}}{L_{34}} \right)$							
$p \ i_{cb1}$		$\left( R \frac{L_{25}}{L_{18}} - R_s \frac{L_{26}}{L_{18}} \right)$							
$p \ i_{cb2}$		$\left( R \frac{L_{37}}{L_{35}} + R_s \frac{L_{38}}{L_{35}} \right)$							
$p \ v_{ca2}$		$\frac{1}{C_s}$							
$p \ v_{cb1}$		0							
$p \ v_{cb2}$	0								

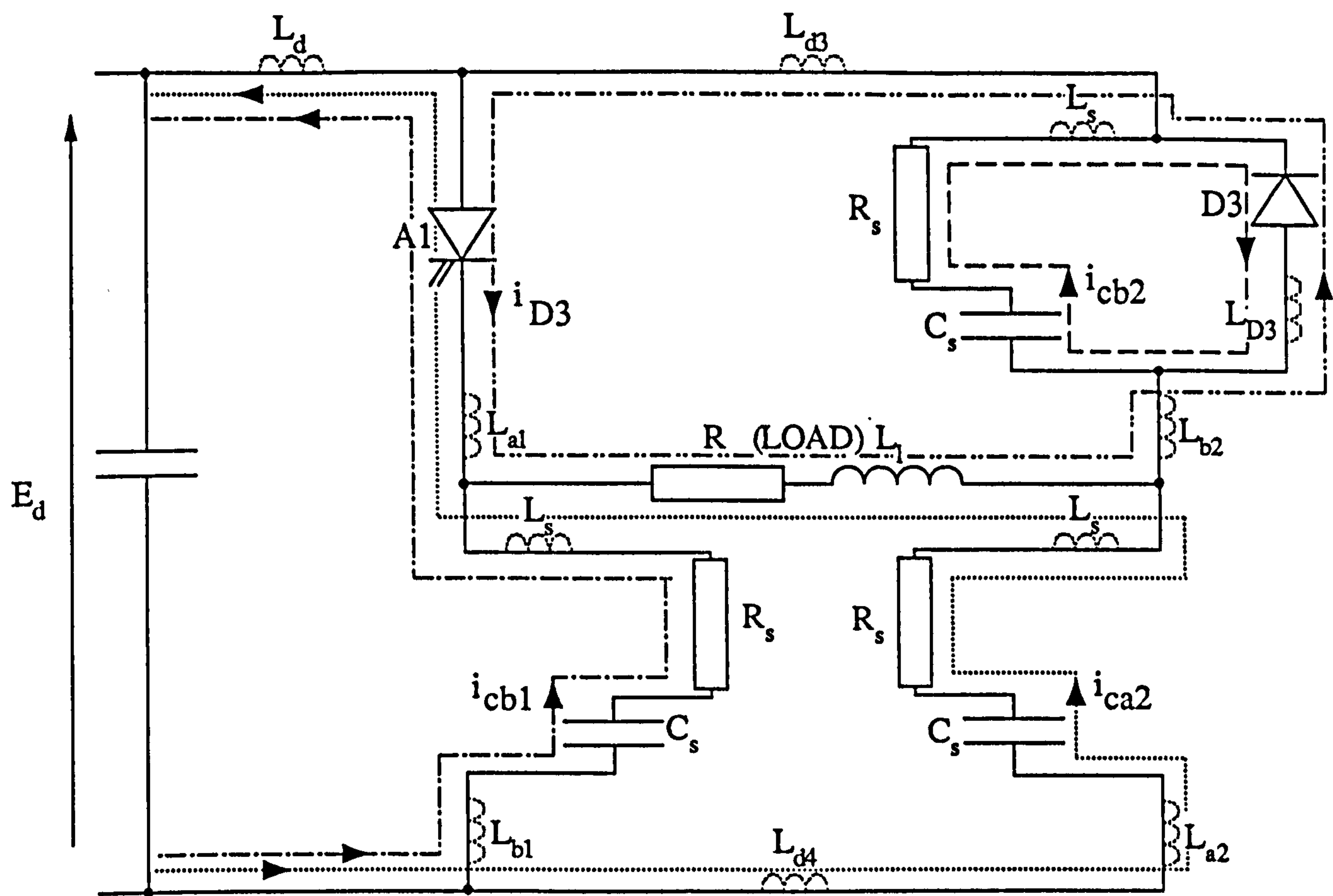
(Columns 2 to 7 as in (d))

$i_{ca2}$	$+$	$E_d \frac{L_{19}}{L_{18}}$
$i_{D3}$		$E_d \frac{L_{29}}{L_{34}}$
$i_{cb1}$		$E_d \frac{L_{24}}{L_{18}}$
$i_{cb2}$		$-E_d \frac{L_{36}}{L_{35}}$
$v_{ca2}$		0
$v_{cb1}$	0	
$v_{cb2}$	0	

(f)

Figure 4.12    Equivalent circuits and state equations matrices for A2 turning off first, (start of freewheeling)

Time interval t5



(g)

COLUMNS

	(1)	(2)	(3)	(4)	(5)	(6)	(7)
$p \ i_{ca2}$	$\left( R \frac{L_{20}}{L_{18}} + R_s \frac{L_{21}}{L_{18}} \right)$		$-R_s \frac{L_{22}}{L_{18}}$				$i_{ca2}$
$p \ i_{D3}$	$-\left( R \frac{L_{30}}{L_{34}} + R_s \frac{L_{31}}{L_{34}} \right)$		$-R_s \frac{L_{32}}{L_{34}}$				$i_{D3}$
$p \ i_{cb1}$	$\left( R \frac{L_{25}}{L_{18}} - R_s \frac{L_{26}}{L_{18}} \right)$		$R_s \frac{L_{27}}{L_{18}}$				$i_{cb1}$
$p \ i_{cb2}$	$\left( R \frac{L_{37}}{L_{35}} + R_s \frac{L_{38}}{L_{35}} \right)$		$R_s \frac{L_{39}}{L_{35}}$	(Columns 2, and 4 to 7 as in (d))			$i_{cb2}$
$p \ v_{ca2}$	$\frac{1}{C_s}$		0				$v_{ca2}$
$p \ v_{cb1}$	0		$\frac{1}{C_s}$				$v_{cb1}$
$p \ v_{cb2}$	0		0				$v_{cb2}$

(h)

Figure 4.12 Equivalent circuits and state equations matrices for A2 turning off first, (start of freewheeling)



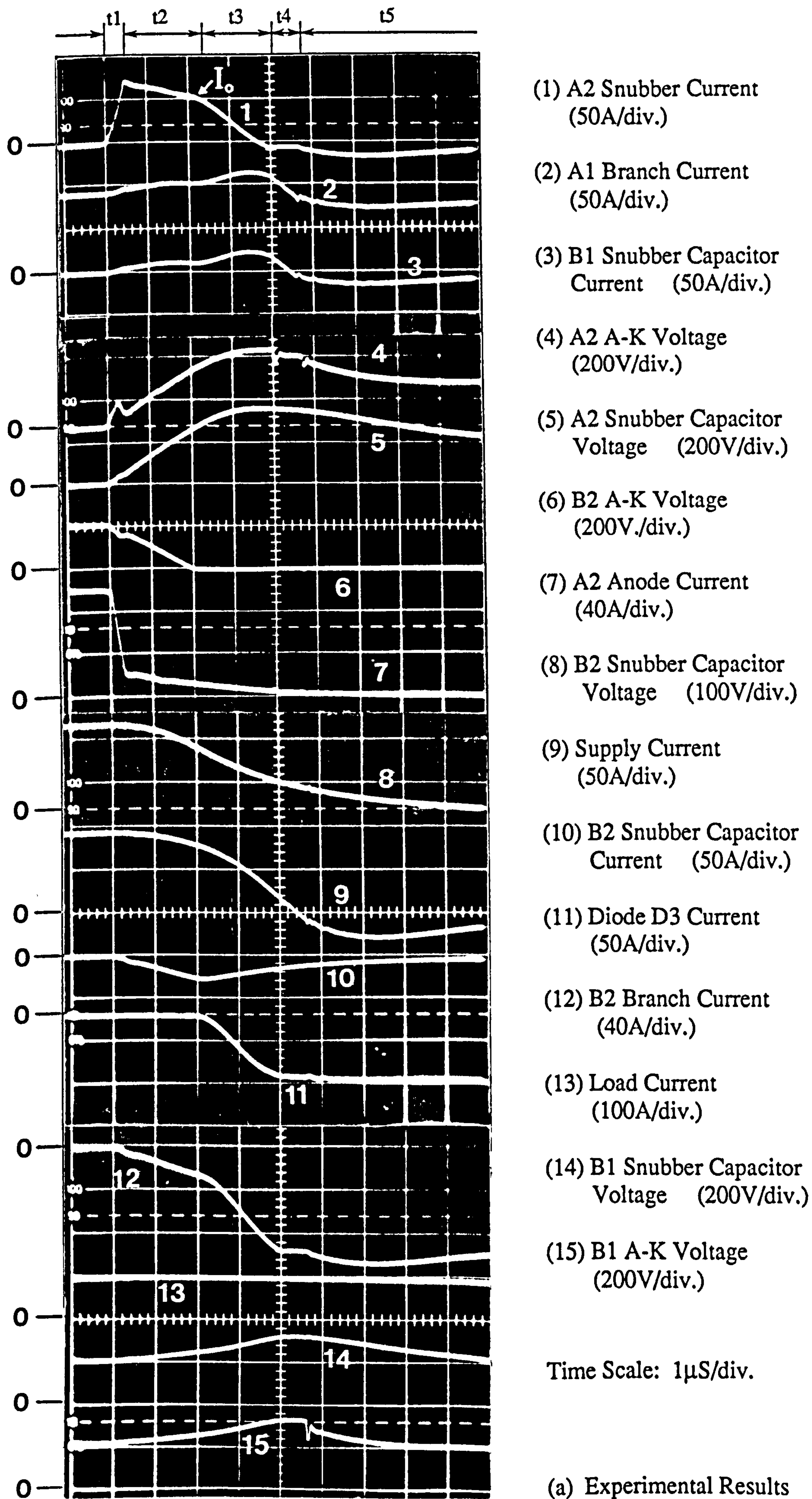
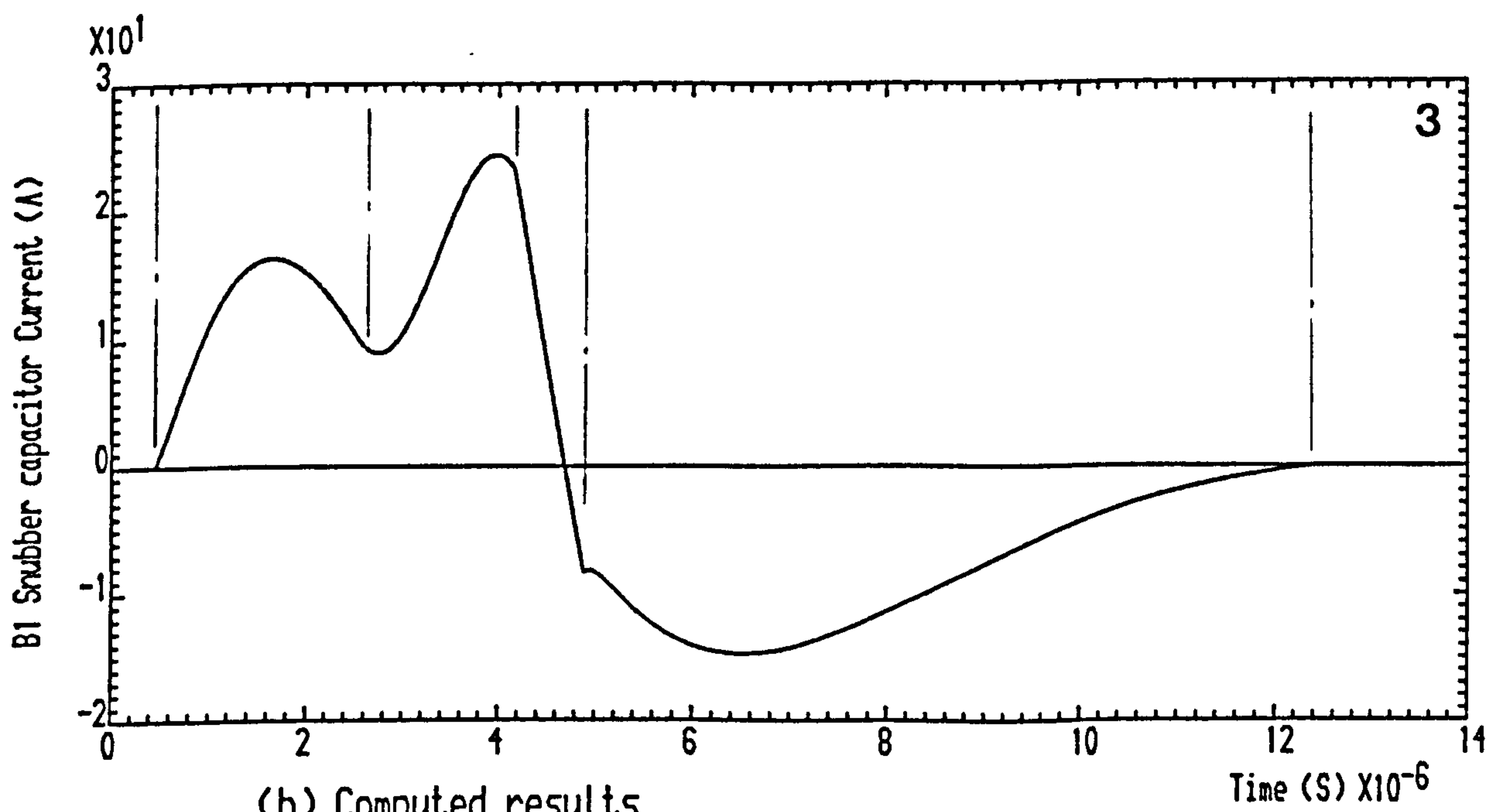
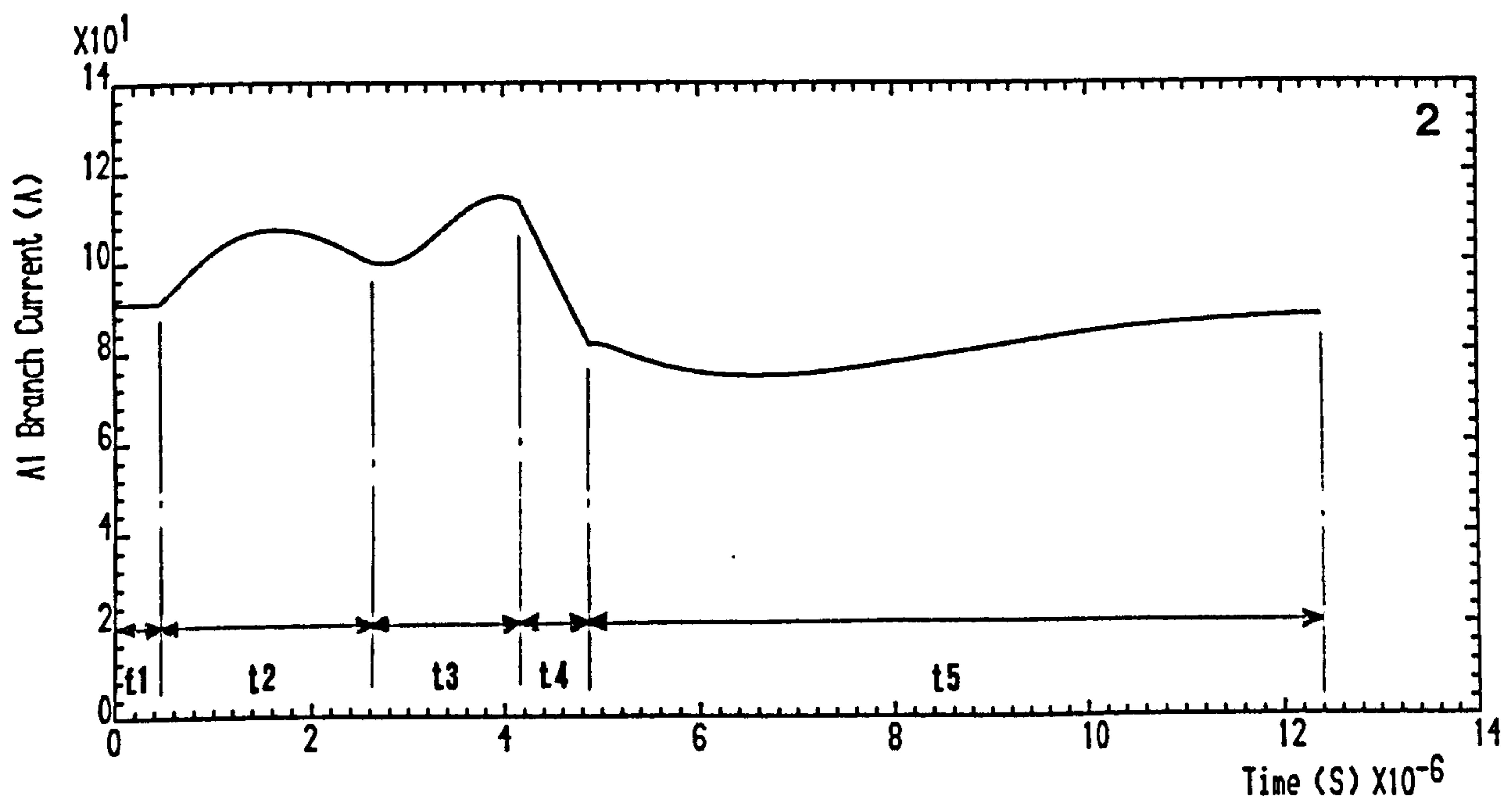
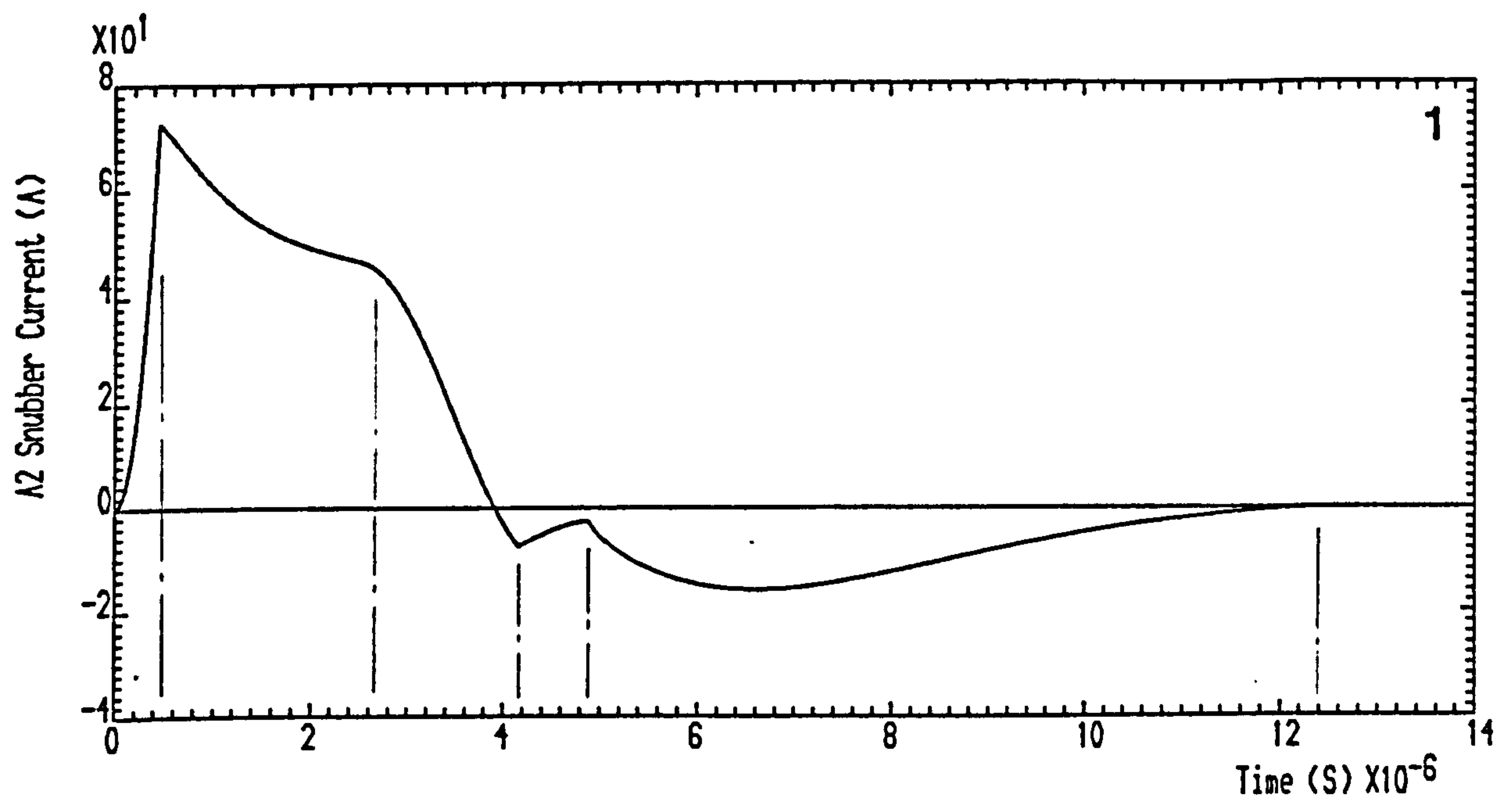


Figure 4.13 Waveforms at GTO A2 turn-off first

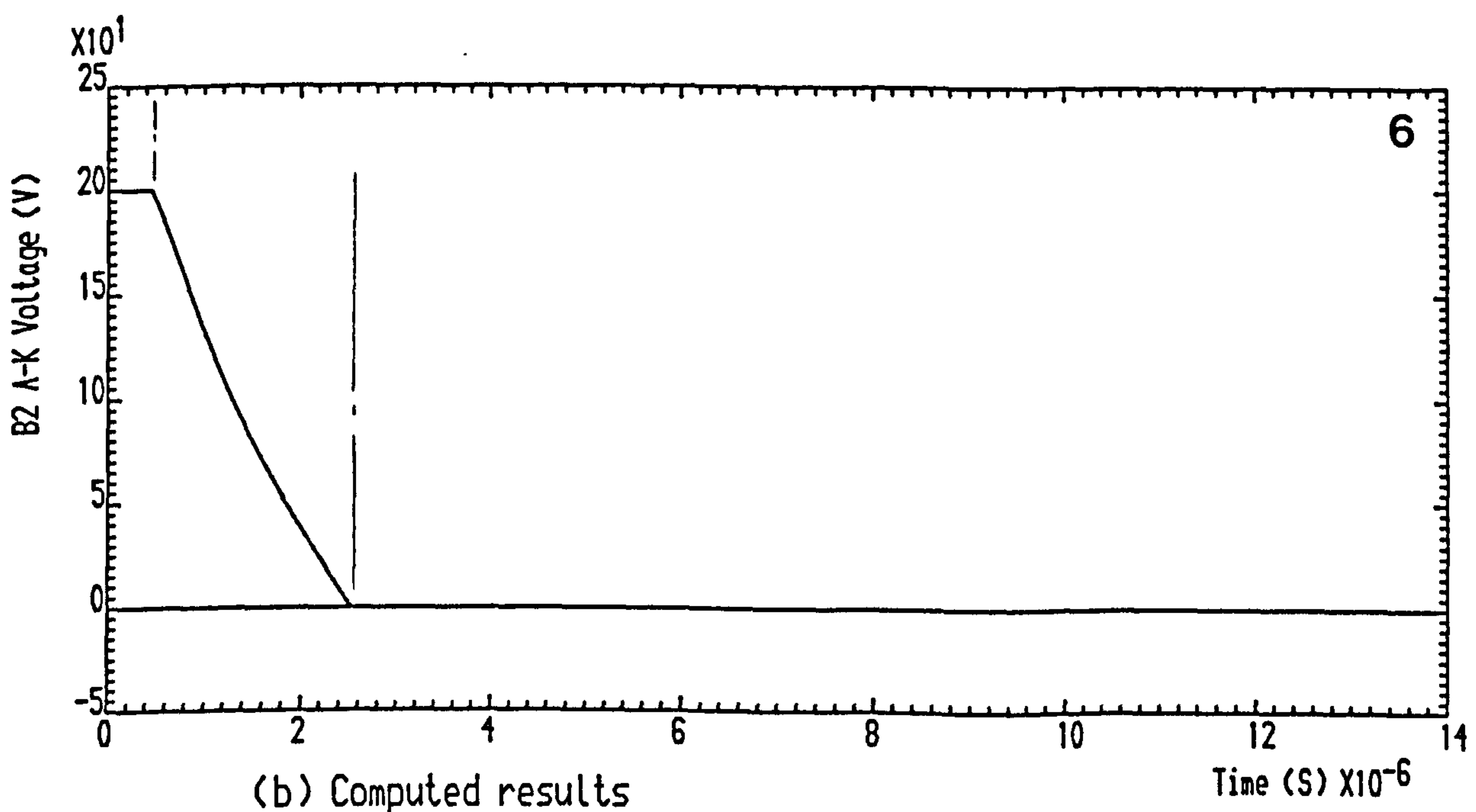
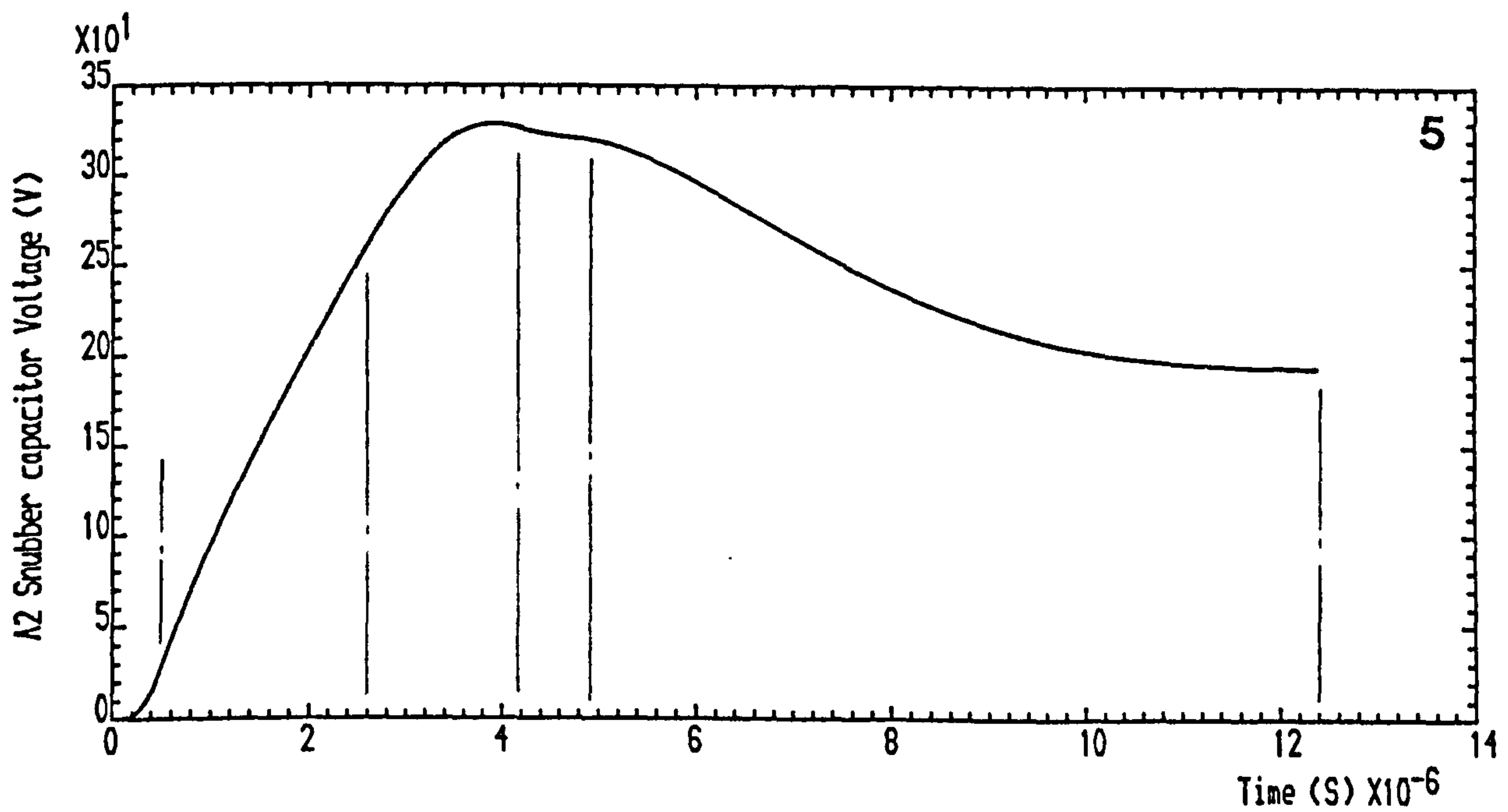
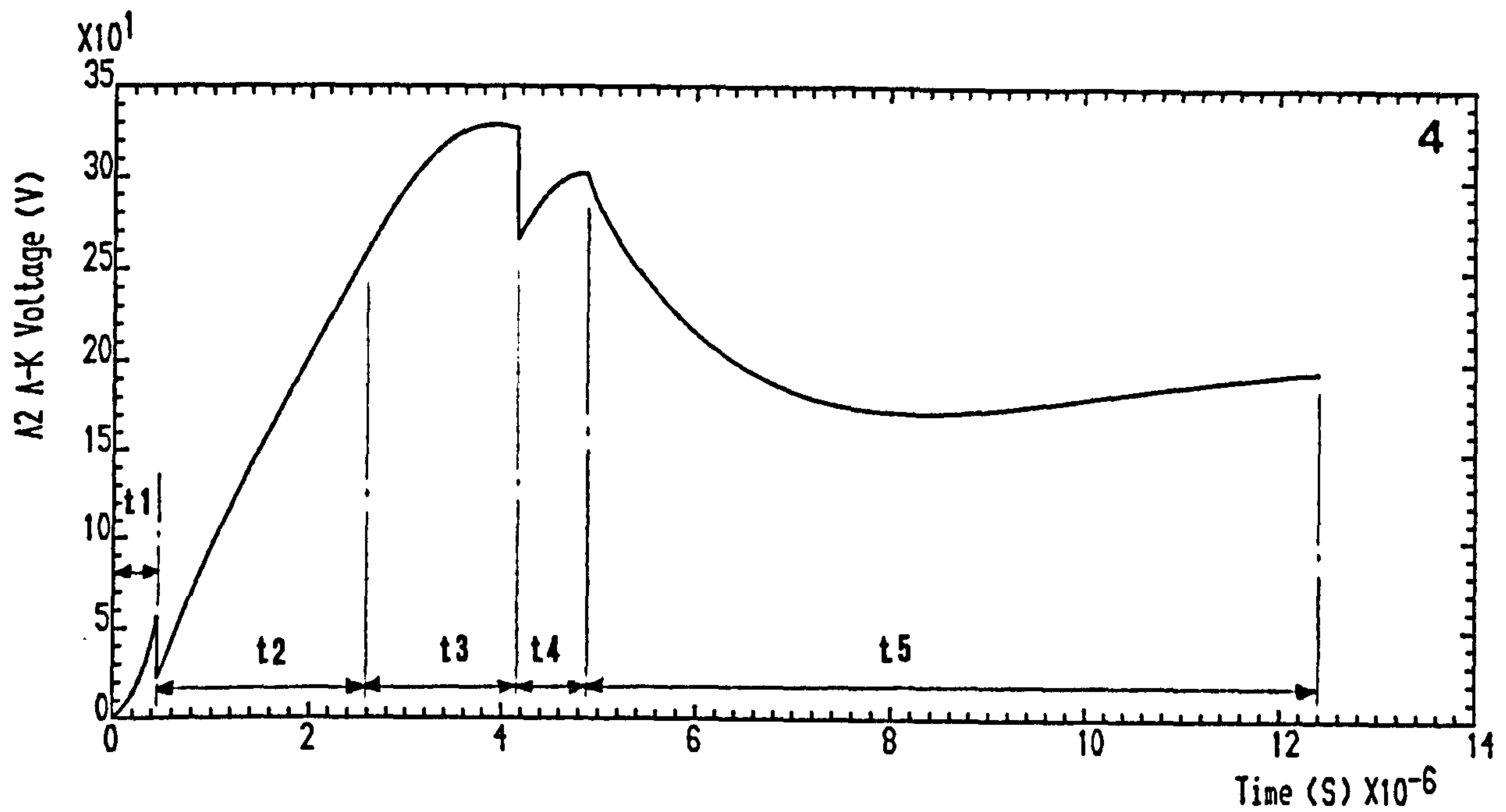


(b) Computed results

Figure 4.13 Waveforms at GTO A2 turn-off First

CONTINUED ..





(b) Computed results

Figure 4.13 Waveforms at GTO A2 turn-off First

CONTINUED ..

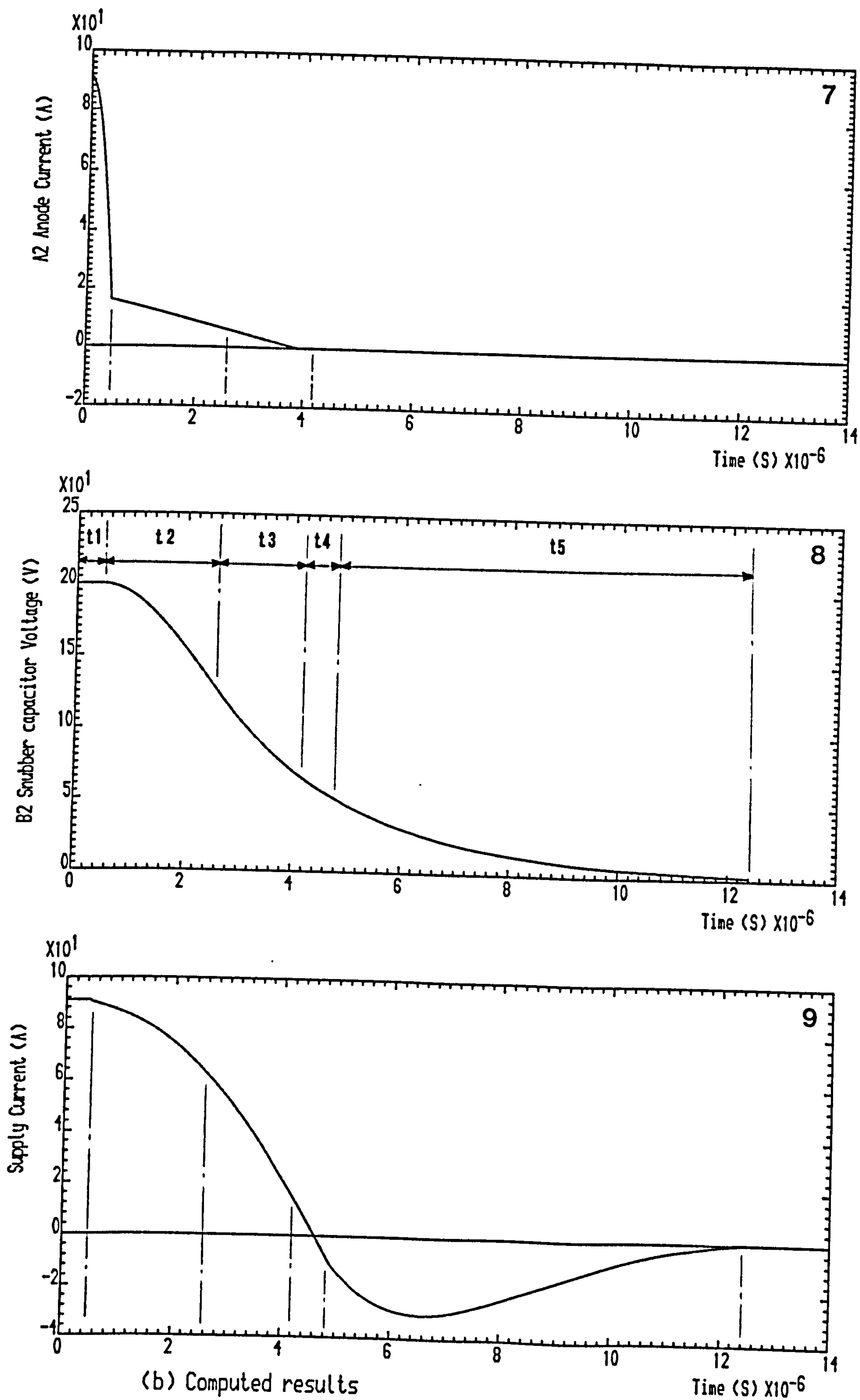
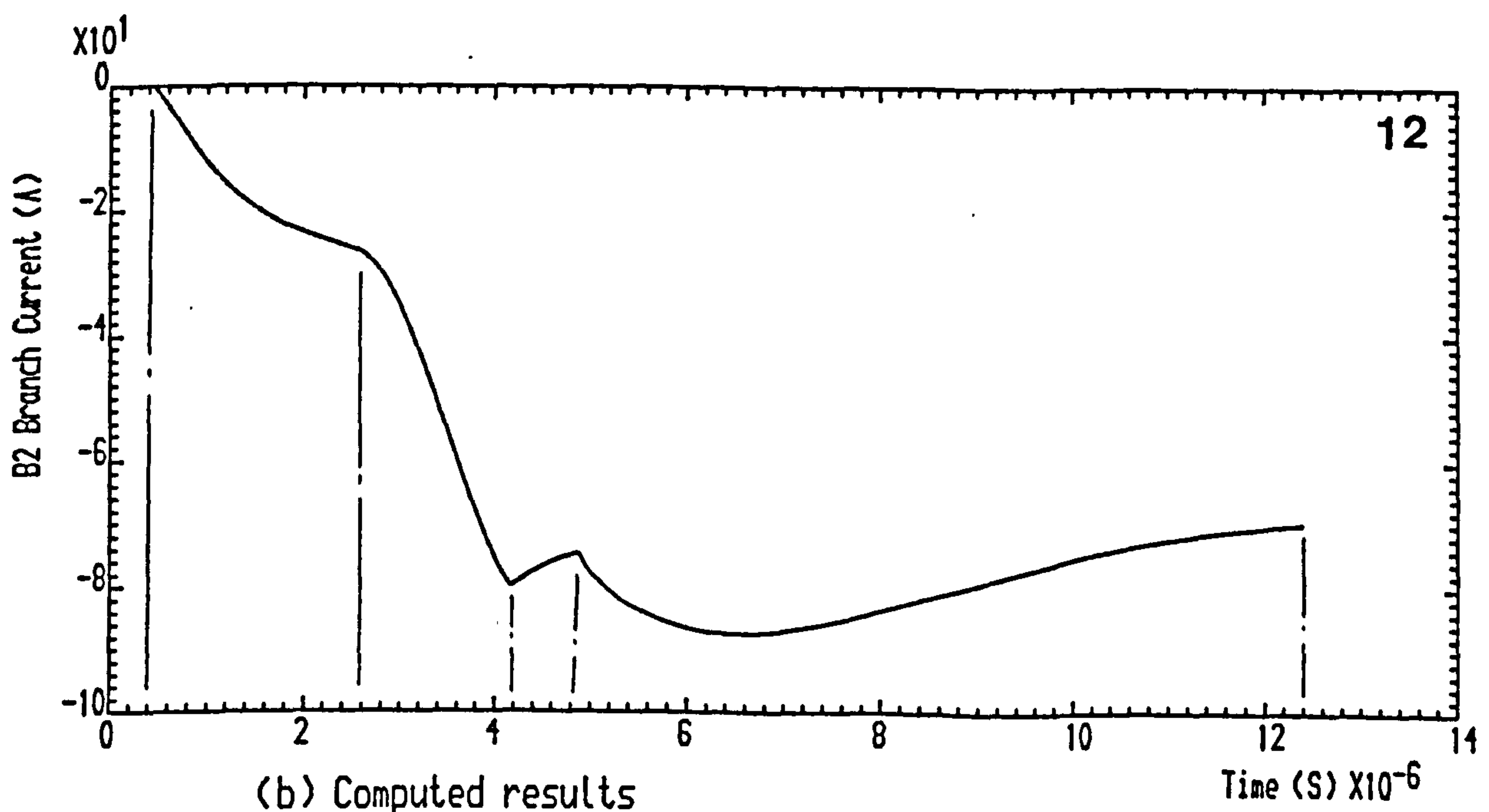
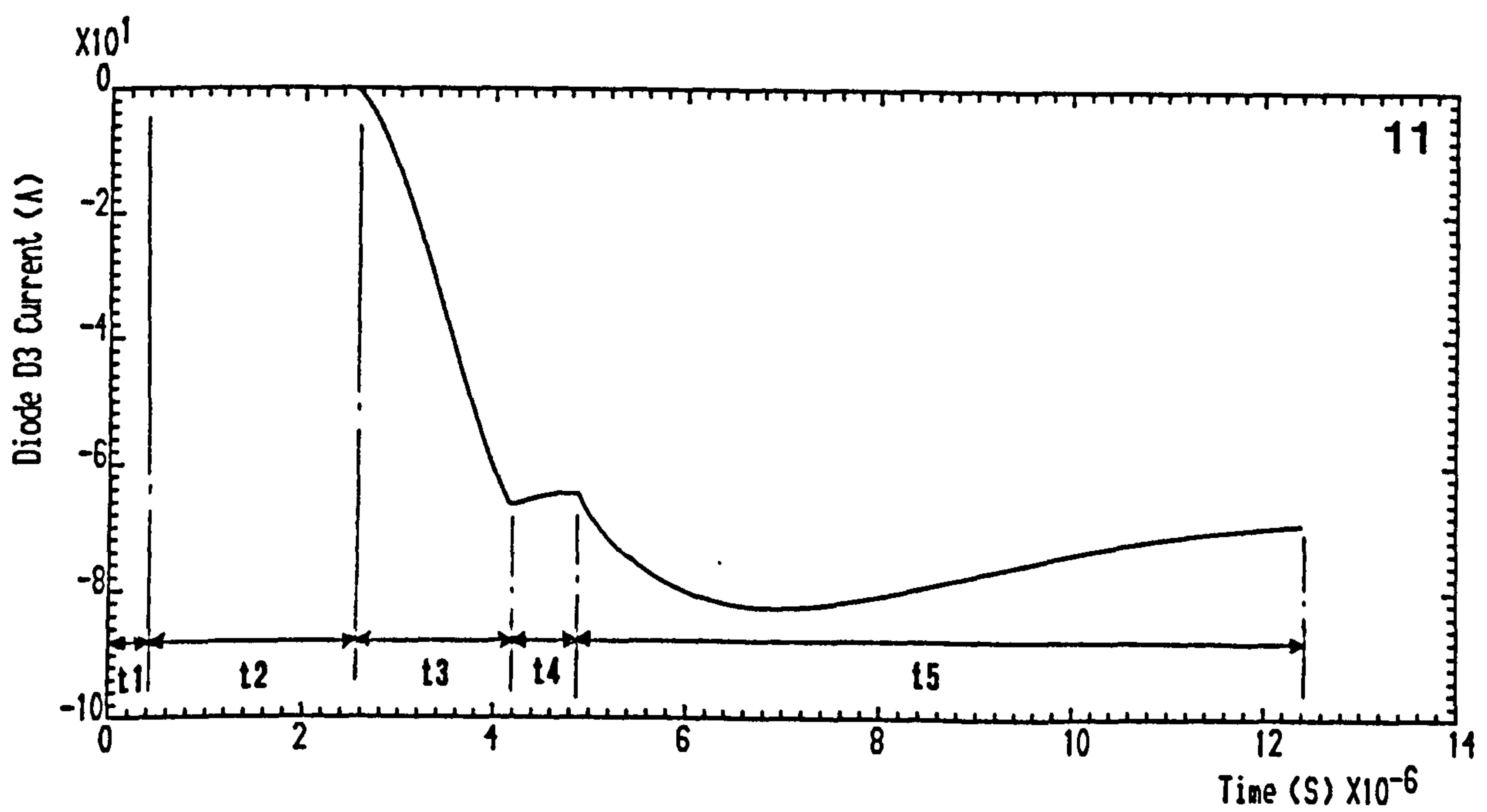
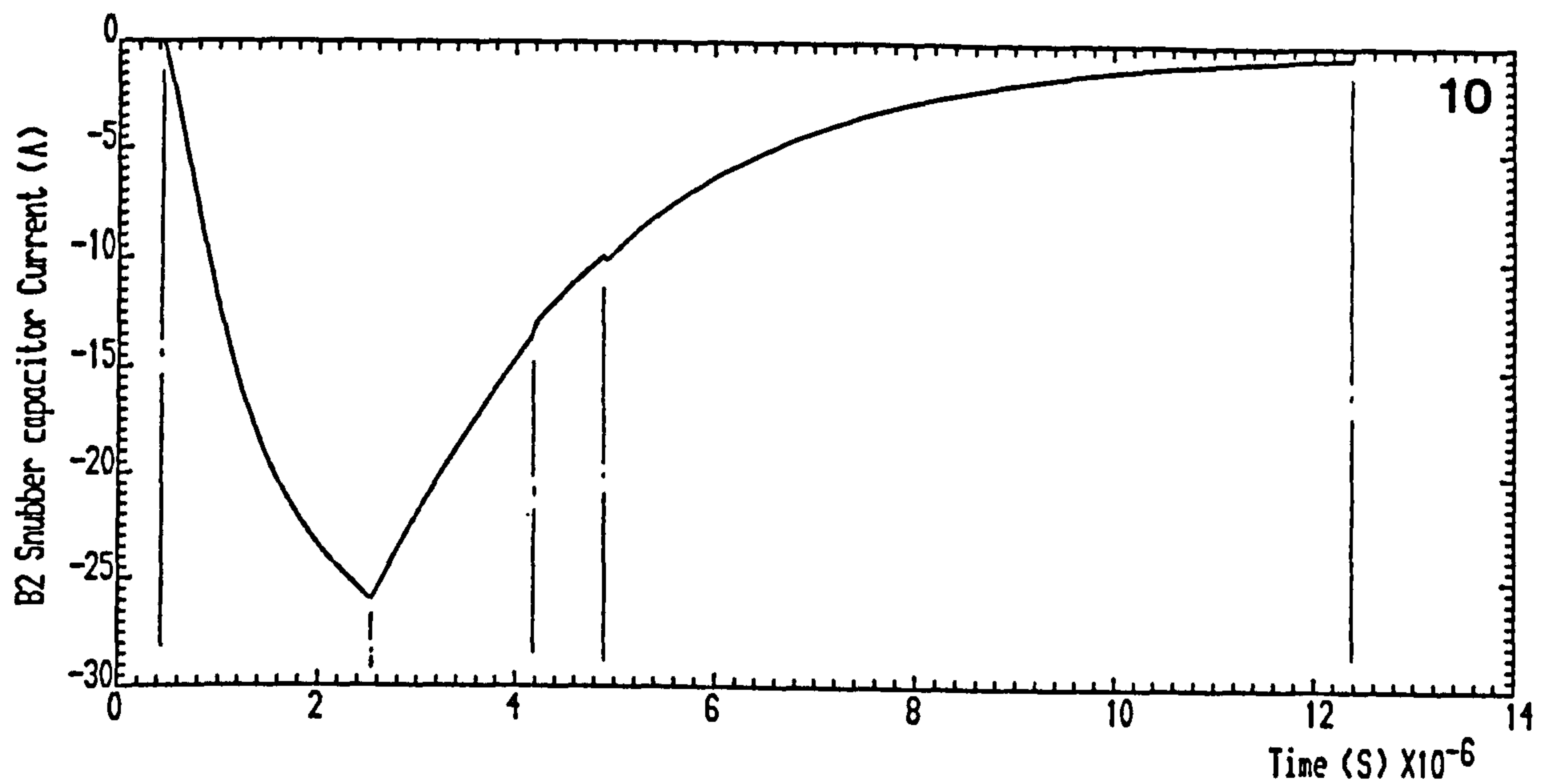


Figure 4.13 WaveForms at GTO A2 turn-off First

CONTINUED ..





(b) Computed results

Figure 4.13 Waveforms at GTO A2 turn-off First

CONTINUED ..

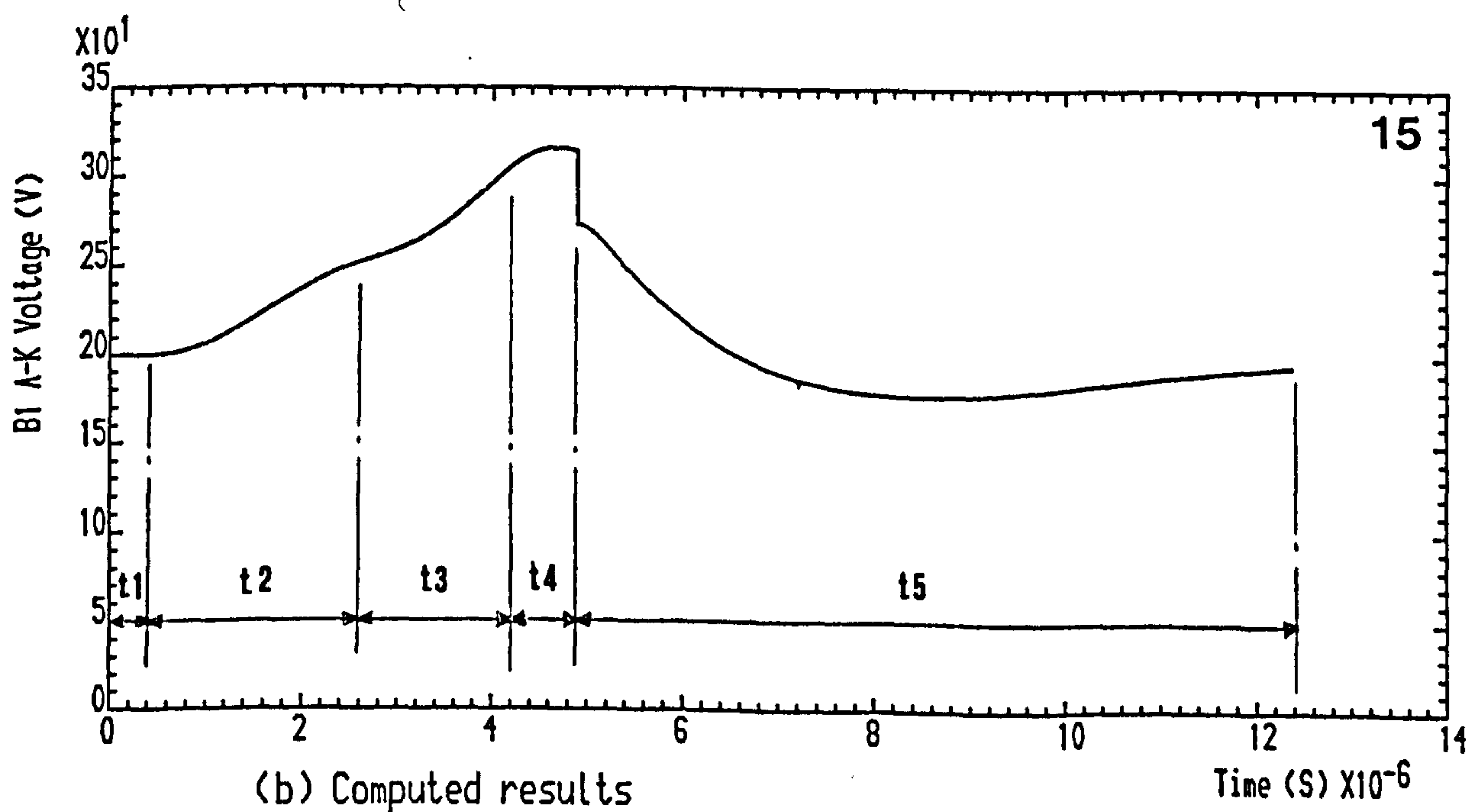
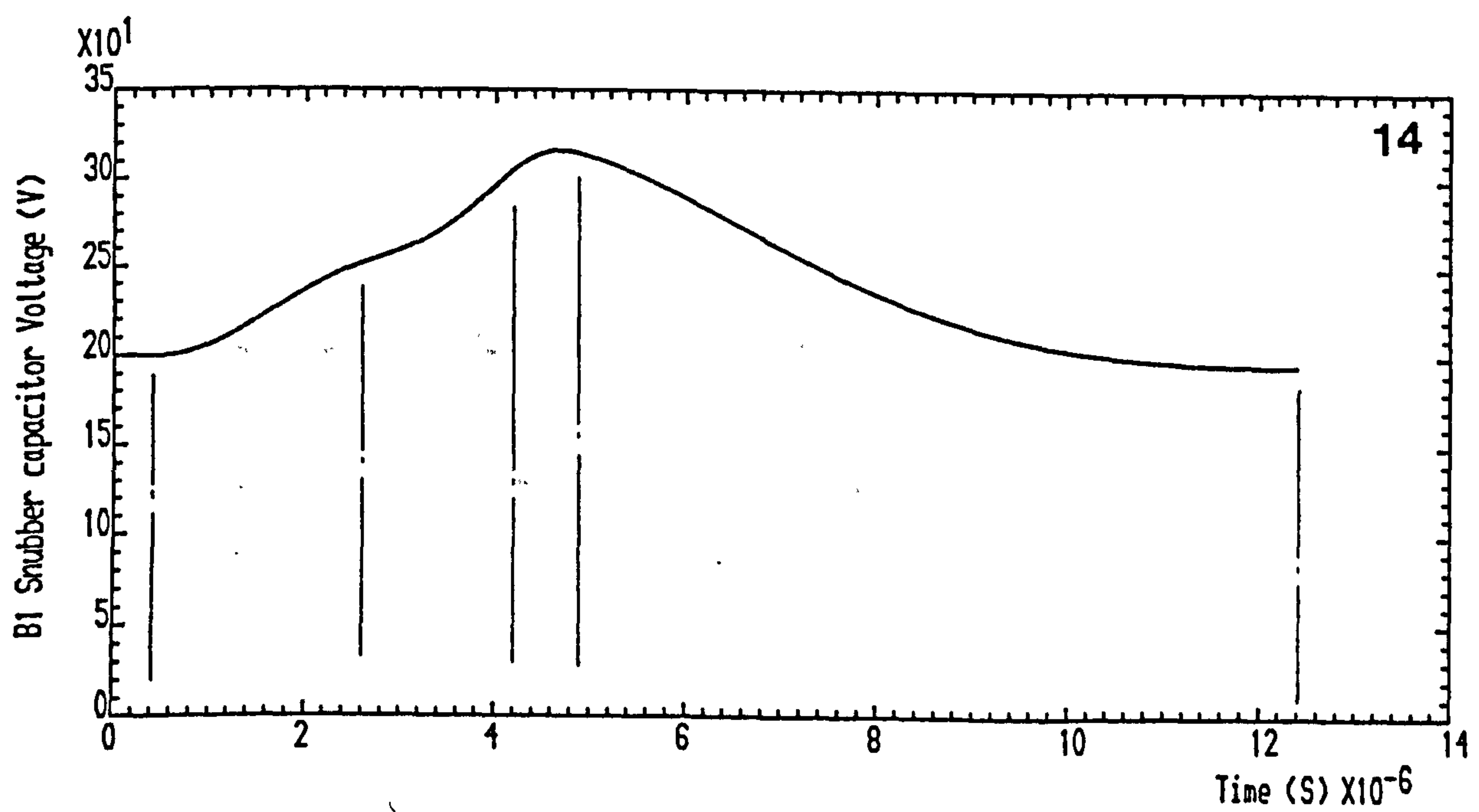
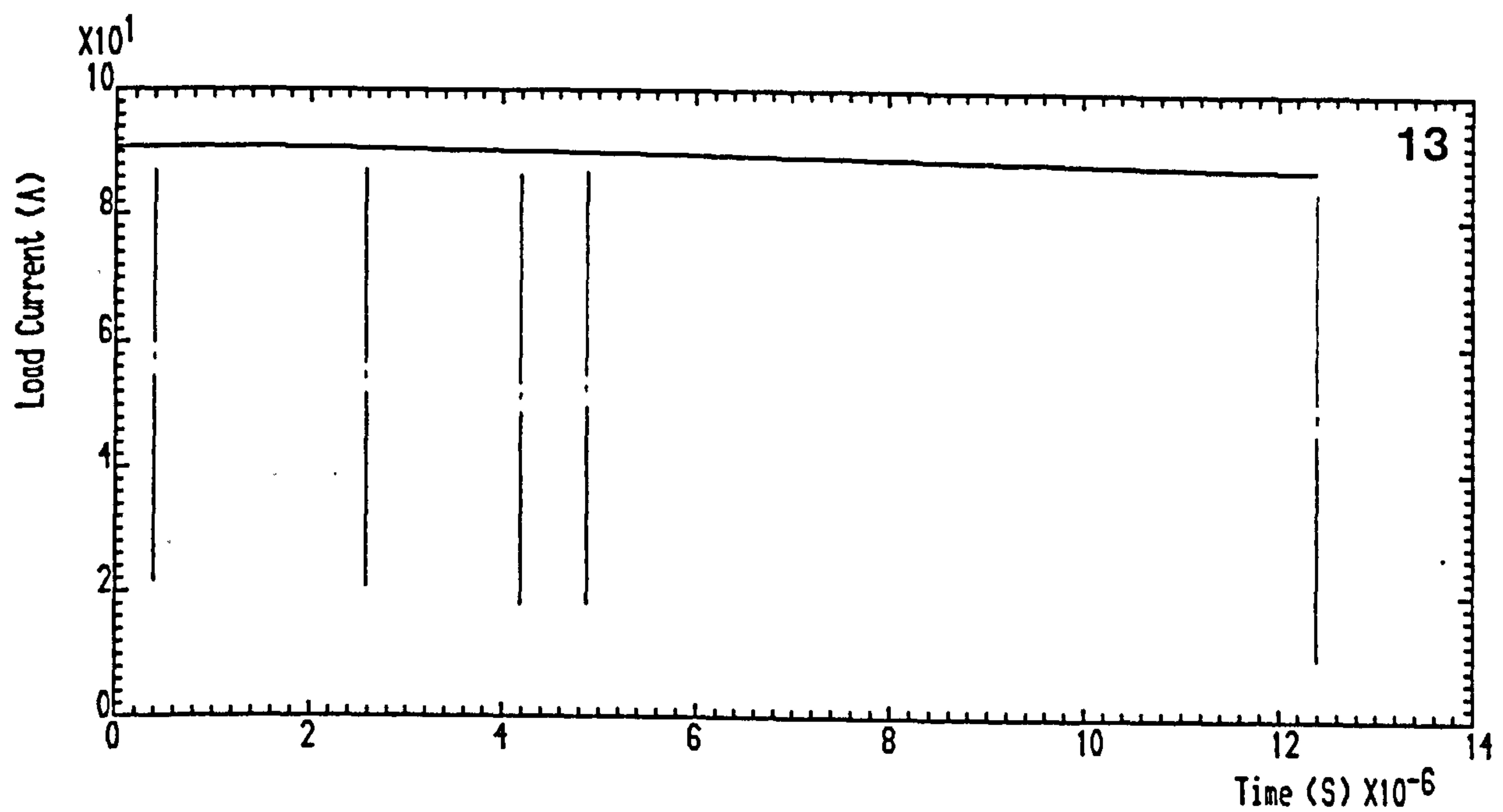


Figure 4.13 WaveForms at GTO A2 turn-off First

END ..



current is increased, trace (3). This is due to the increased  $L_d di/dt$  of the source.

**Interval  $t_4$ :** The duration is from the reverse recovery of A2 snubber diode to the reverse recovery of B1 snubber diode. The equivalent circuit and the state equations become those shown in Figure 4.12(e) and (f) respectively.

Upon recovery of the A2 snubber diode, the associated capacitor discharge current transfers to its snubber resistor, damping its oscillation. However, a substantial voltage drop across A2 is prevented by the 'hold-up' effect, caused by the overcharged B1 snubber capacitor voltage being coupled to A2 via the DC rails, GTO A1 and diode D3 (Figure 4.13, traces (4) and (15)). B1 snubber capacitor charging current falls and reverses, starting B1 snubber diode reverse recovery.

**Interval  $t_5$ :** The equivalent circuit and state equations for this interval, which lasts from B1 snubber diode reverse recovery to the A2 and B1 snubber capacitor discharge currents reaching zero, are shown respectively in Figure 4.12(g) and (h). B1 and A2 snubber capacitors are now discharging through their snubber resistors back to the supply, with the voltages across the associated GTOs decaying to the supply value  $E_d$ . Interval  $t_5$  is succeeded by GTO A1 and diode D3 conducting the total freewheeling load current.

The most influential stray inductances are those of the source, the bridge rails and the freewheeling loops.

**b) At second GTO thyristor A1 turn-off following A2**

GTO A1 is now turning off with load current freewheeling through A1 and D3 initially. The current first diverts into the A1 snubber circuit. The load current, having decayed during freewheeling, is less than for GTO A2 turn-off and produces a much lower voltage spike across A1 during  $t_1$ , Figure 4.15, trace (4).

**Interval  $t_2$ :** This starts from the A1 snubber capacitor current peak, and ends as the A2 snubber capacitor half-cycle of overcharging is completed. The equivalent circuit and the associated state equations appear in Figure 4.14(a) and (b) respectively. Initially the constant load current divides between charging and discharging the A1 and B1 snubber capacitors respectively. Since current commences to return back to the supply, a slight  $L_d di/dt$  is induced which lifts the voltage across

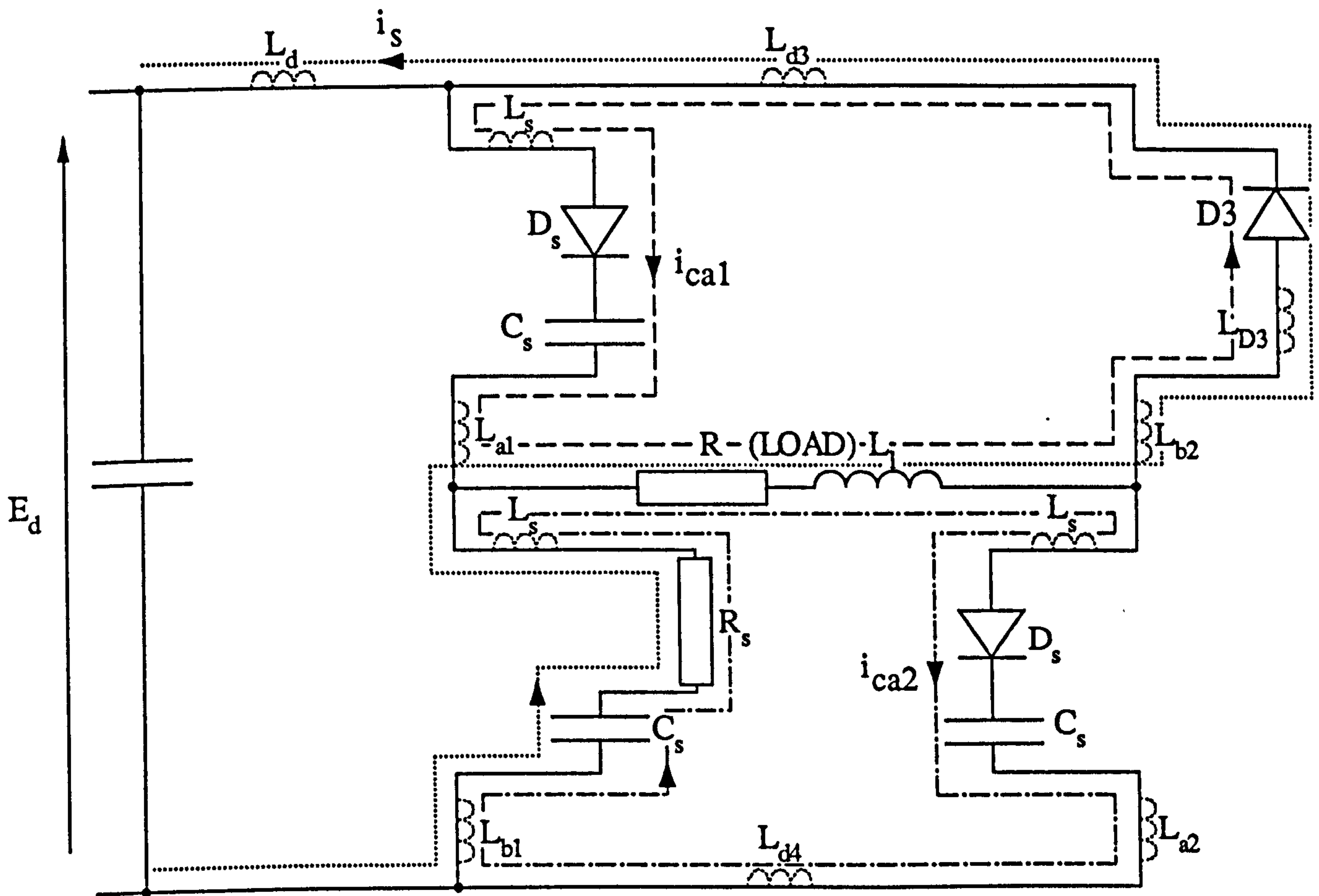
the DC rails causing the A2 snubber capacitor voltage to rise above  $E_d$ , as in Figure 4.15, traces (14) and (15). The A1 snubber capacitor charging current is falling, and the B1 snubber capacitor discharging current is rising as their voltages rise to and fall from  $E_d$  respectively.

**Interval t3:** The start of the A2 snubber capacitor discharge indicates the start of interval t3, the equivalent circuit and state equations of which, are shown in Figure 4.14(c) and (d), and the fall of GTO B1 voltage to zero indicates the end of it, Figure 4.15, trace (5). With A2 snubber diode reverse recovery being rapid due to the low forward current, the A2 snubber capacitor current reverses almost immediately into its snubber resistor, the voltage across the associated GTO decaying to  $E_d$ , Figure 4.15, trace (16). As this damped current rises (trace (14)), a slightly slower rate of rise is experienced by the negative supply current (trace (13)), this having a small effect on the A1 and B1 snubber capacitor currents (traces (2) and (7)), as the load current is virtually constant during this interval (trace(6)).

**Interval t4:** This interval, the equivalent circuit and system matrix of which are shown in Figure 4.14(e) and (f), commences when D4 starts conduction and ends when A2 snubber capacitor discharge current falls to zero. Upon forward biasing of D4, it takes over the rising discharge of B1 snubber capacitor, this then discharging locally. The load current being constant, the A1 snubber capacitor current fall rate increases as its voltage further overshoots  $E_d$ , Figure 4.15, traces (2) and (3).

Since the rise of the feedback current in the supply is now more rapid, the induced voltage across  $L_d$  again lifts the voltage across GTO A2, causing a rapid fall of its snubber capacitor discharge current (trace (14)). Alternatively, it may be considered that the oscillatory overshoot voltage across GTO A1 is coupled to GTO A2 via the DC rails and diodes D3 and D4, exerting a hold-up effect.

**Interval t5:** This interval begins as the A2 snubber capacitor starts overcharging again and ends when A1 snubber diode is fully reverse recovered. The equivalent circuit and its state equations are shown in Figure 4.14(g) and (h). With A2 snubber diode now forward biased, the associated capacitor charges above  $E_d$ , again Figure 4.15, traces (14) and (15). The A1 snubber capacitor charging current continues to fall, its voltage approaching its oscillatory peak.

Time interval t2

(a)

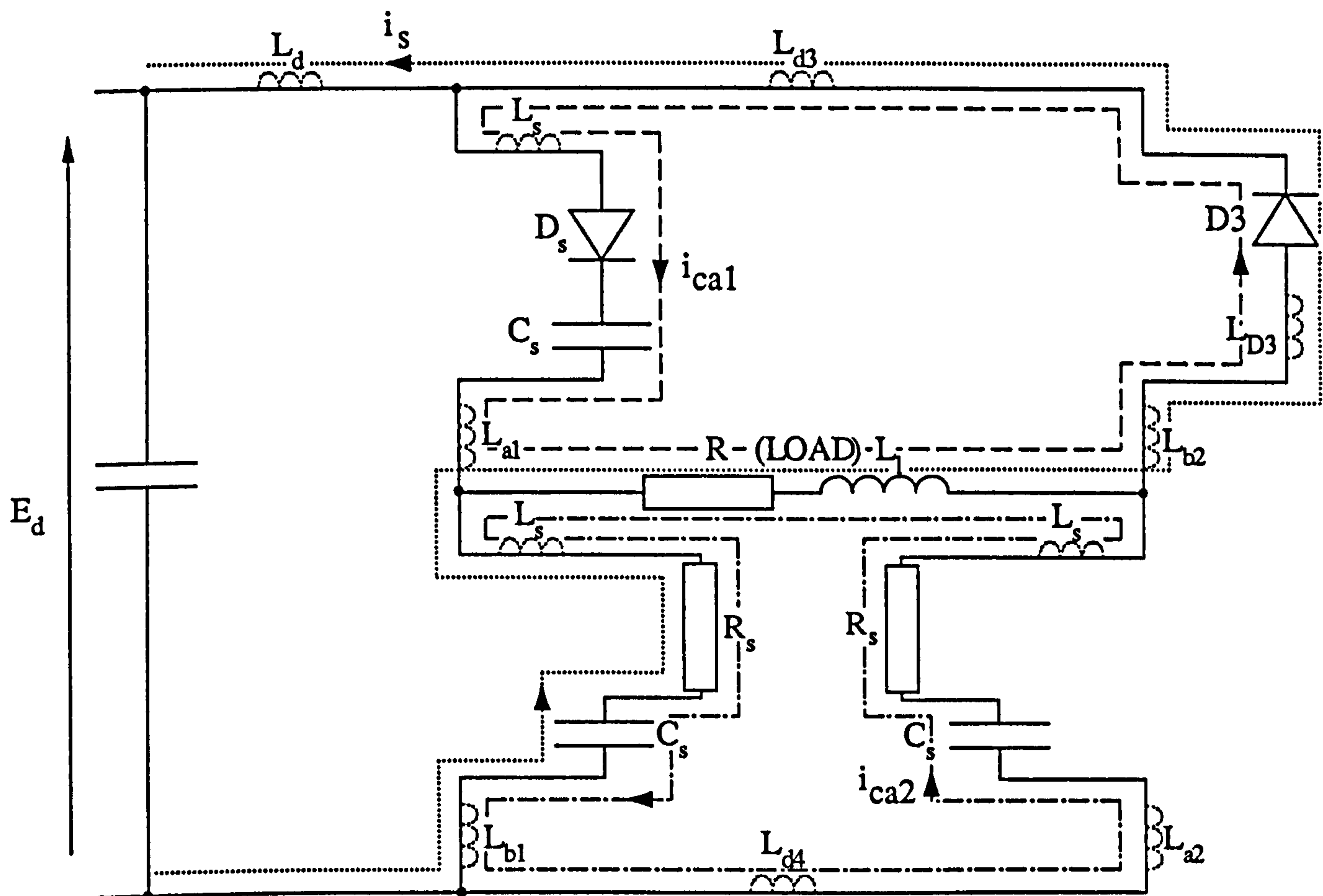
COLUMNS	(1)	(2)	(3)	(4)	(5)	(6)
$p i_{ca1}$	$-R \frac{L_8}{L_1}$	$-(R \frac{L_8}{L_1} + R_s \frac{L_{11}}{L_1})$	$(R \frac{L_8}{L_1} + R_s \frac{L_{11}}{L_1})$	$-\frac{L_9}{L_1}$	$-\frac{L_{10}}{L_1}$	$\frac{L_{11}}{L_1}$
$p i_{ca2}$	$-R \frac{L_3}{L_1}$	$-(R \frac{L_3}{L_1} + R_s \frac{L_6}{L_1})$	$(R \frac{L_3}{L_1} + R_s \frac{L_6}{L_1})$	$-\frac{L_4}{L_1}$	$-\frac{L_5}{L_1}$	$\frac{L_6}{L_1}$
$p i_s$	$-R \frac{L_{14}}{L_{12}}$	$-(R \frac{L_{14}}{L_{12}} + R_s \frac{L_{17}}{L_{12}})$	$(R \frac{L_{14}}{L_{12}} + R_s \frac{L_{17}}{L_{12}})$	$-\frac{L_{15}}{L_{12}}$	$-\frac{L_{16}}{L_{12}}$	$\frac{L_{17}}{L_{12}}$
$p v_{ca1}$	$\frac{1}{C_s}$	0	0	0	0	0
$p v_{ca2}$	0	$\frac{1}{C_s}$	0	0	0	0
$p v_{cb1}$	0	$-\frac{1}{C_s}$	$\frac{1}{C_s}$	0	0	0

$$= \begin{bmatrix} i_{ca1} \\ i_{ca2} \\ i_s \\ v_{ca1} \\ v_{ca2} \\ v_{cb1} \end{bmatrix} + \begin{bmatrix} E_d \frac{L_7}{L_1} \\ E_d \frac{L_2}{L_1} \\ E_d \frac{L_{13}}{L_{12}} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

(b)

Figure 4.14 Equivalent circuits and state equations matrices for GTO A1 turning off after A2 (start of feedback).



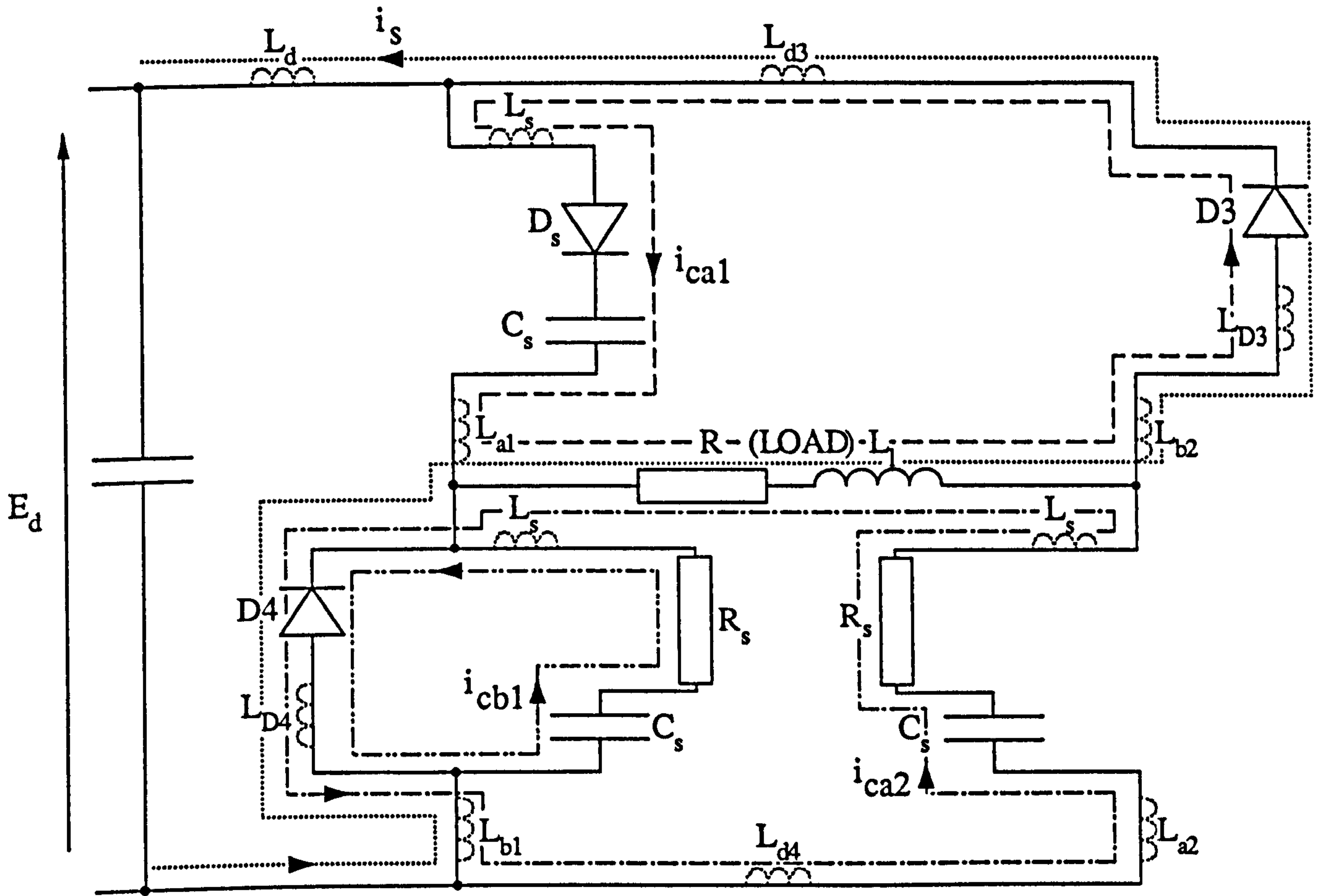
Time interval t3

(c)

<u>COLUMNS</u>	(1)	(2)	(3)	(4)	(5)	(6)		
$\begin{bmatrix} p i_{ca1} \\ p i_{ca2} \\ p i_s \\ p v_{ca1} \\ p v_{ca2} \\ p v_{cb1} \end{bmatrix}$	$=$	$\begin{bmatrix} - \left[ R \frac{L_8}{L_1} + R_s \left( \frac{L_{10} + L_{11}}{L_1} \right) \right] \\ - \left[ R \frac{L_3}{L_1} + R_s \left( \frac{L_5 + L_6}{L_1} \right) \right] \\ - \left[ R \frac{L_{14}}{L_{12}} + R_s \left( \frac{L_{16} + L_{17}}{L_{12}} \right) \right] \\ 0 \\ \frac{1}{C_s} \\ -\frac{1}{C_s} \end{bmatrix}$	(Columns 1, and 3 to 7 as in (b))			$\begin{bmatrix} i_{ca1} \\ i_{ca2} \\ i_s \\ v_{ca1} \\ v_{ca2} \\ v_{cb1} \end{bmatrix}$	$+$	$\begin{bmatrix} E_d \frac{L_7}{L_1} \\ E_d \frac{L_2}{L_1} \\ E_d \frac{L_{13}}{L_{12}} \\ 0 \\ 0 \\ 0 \end{bmatrix}$

(d)

Figure 4.14 Equivalent circuits and state equations matrices for GTO A1 turning off after A2 (start of feedback).

Time interval t4

(e)

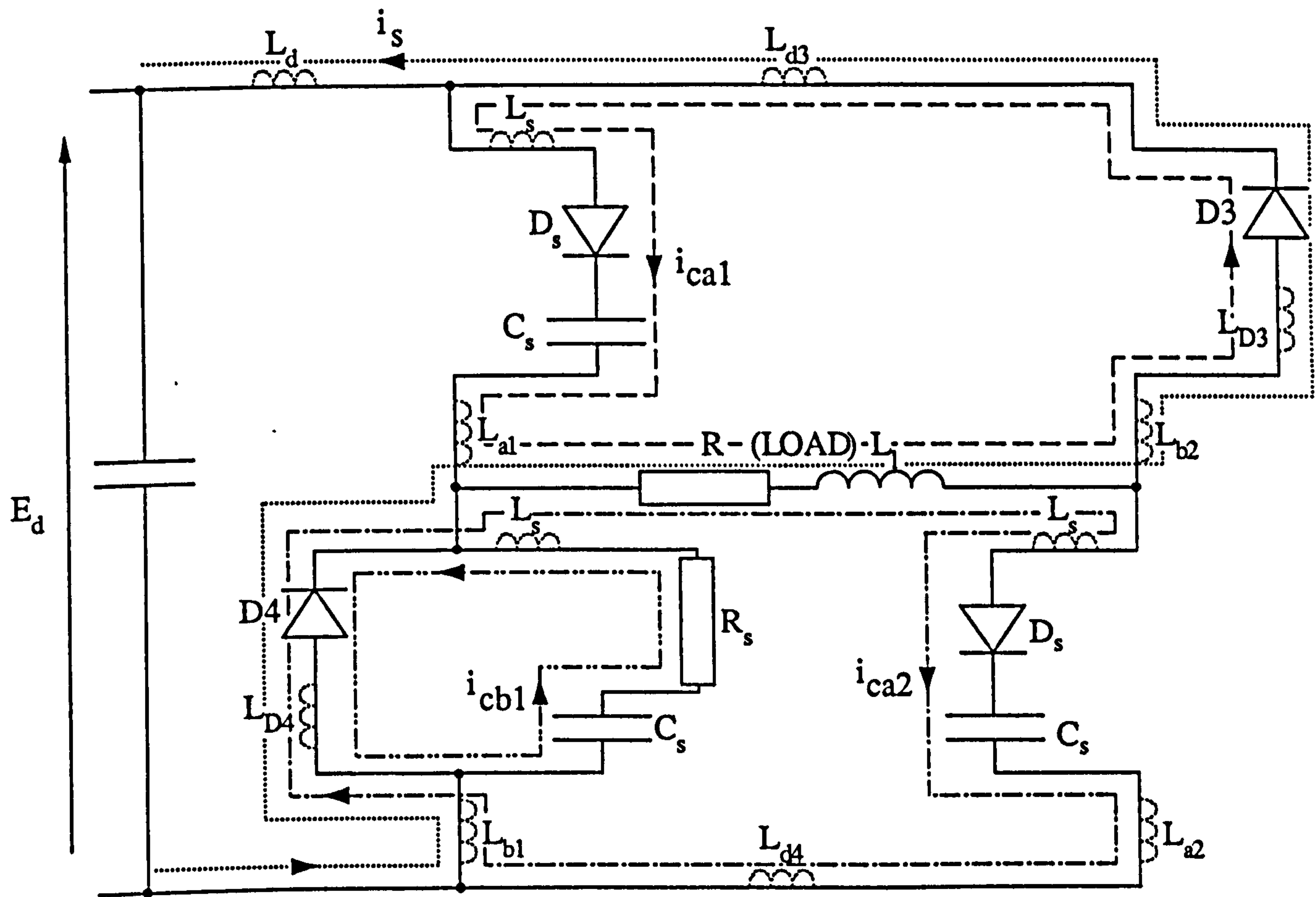
COLUMNS    (1)                    (2)                    (3)                    (4)                    (5)                    (6)                    (7)

$$\begin{bmatrix} p i_{ca1} \\ p i_{ca2} \\ p i_{cb1} \\ p i_s \\ p v_{ca1} \\ p v_{ca2} \\ p v_{cb1} \end{bmatrix} = \begin{bmatrix} -R \frac{L_{37}}{L_{35}} & -\left(R \frac{L_{37}}{L_{35}} - R_s \frac{L_{39}}{L_{35}}\right) & R_s \frac{L_{40}}{L_{35}} & R \frac{L_{37}}{L_{35}} & \frac{L_{38}}{L_{35}} & \frac{L_{39}}{L_{35}} & \frac{L_{40}}{L_{35}} \\ -R \frac{L_{20}}{L_{18}} & -\left(R \frac{L_{20}}{L_{18}} + R_s \frac{L_{22}}{L_{18}}\right) & R_s \frac{L_{23}}{L_{18}} & R \frac{L_{20}}{L_{18}} & \frac{L_{21}}{L_{18}} & -\frac{L_{22}}{L_{18}} & \frac{L_{23}}{L_{18}} \\ -R \frac{L_{31}}{L_{29}} & -\left(R \frac{L_{31}}{L_{29}} - R_s \frac{L_{33}}{L_{29}}\right) & R_s \frac{L_{34}}{L_{29}} & R \frac{L_{31}}{L_{29}} & \frac{L_{32}}{L_{29}} & \frac{L_{33}}{L_{29}} & \frac{L_{34}}{L_{29}} \\ -R \frac{L_{25}}{L_{18}} & -\left(R \frac{L_{25}}{L_{18}} + R_s \frac{L_{27}}{L_{18}}\right) & R_s \frac{L_{28}}{L_{18}} & R \frac{L_{25}}{L_{18}} & \frac{L_{26}}{L_{18}} & -\frac{L_{27}}{L_{18}} & \frac{L_{28}}{L_{18}} \\ \frac{1}{C_s} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_s} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_s} & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{ca1} \\ i_{ca2} \\ i_{cb1} \\ i_s \\ v_{ca1} \\ v_{ca2} \\ v_{cb1} \end{bmatrix} + \begin{bmatrix} E_d \frac{L_{36}}{L_{35}} \\ E_d \frac{L_{19}}{L_{18}} \\ E_d \frac{L_{30}}{L_{29}} \\ E_d \frac{L_{24}}{L_{18}} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

(f)

Figure 4.14 Equivalent circuits and state equations matrices for GTO A1 turning off after A2 (start of feedback).

Time interval t5



(g)

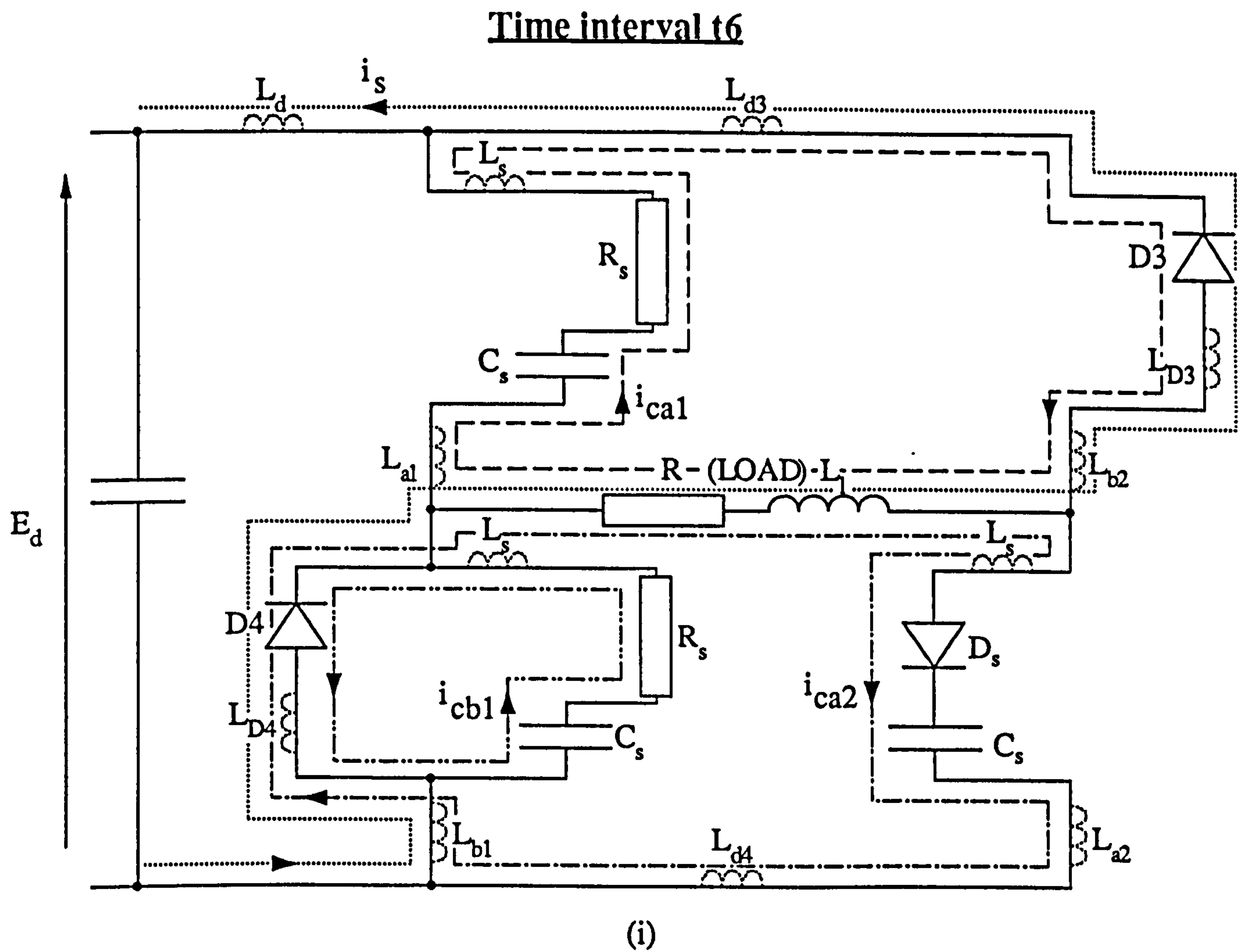
COLUMNS      (1)      (2)      (3)      (4)      (5)      (6)      (7)

$\begin{bmatrix} p i_{ca1} \\ p i_{ca2} \\ p i_{cb1} \\ p i_s \\ p v_{ca1} \\ p v_{ca2} \\ p v_{cb1} \end{bmatrix}$	$=$	$\begin{bmatrix} -R \frac{L_{37}}{L_{35}} \\ -R \frac{L_{20}}{L_{18}} \\ -R \frac{L_{31}}{L_{29}} \\ -R \frac{L_{25}}{L_{18}} \\ 0 \\ \frac{1}{C_s} \\ 0 \end{bmatrix}$	<p>(Columns 1, and 3 to 7 as in (f))</p>	$\begin{bmatrix} i_{ca1} \\ i_{ca2} \\ i_{cb1} \\ i_s \\ v_{ca1} \\ v_{ca2} \\ v_{cb1} \end{bmatrix}$	$+$	$\begin{bmatrix} E_d \frac{L_{36}}{L_{35}} \\ E_d \frac{L_{19}}{L_{18}} \\ E_d \frac{L_{30}}{L_{29}} \\ E_d \frac{L_{24}}{L_{18}} \\ 0 \\ 0 \\ 0 \end{bmatrix}$
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(h)

Figure 4.14    Equivalent circuits and state equations matrices for GTO A1 turning off after A2 (start of feedback).





**COLUMNS**

(1)      (2)      (3)      (4)      (5)      (6)      (7)

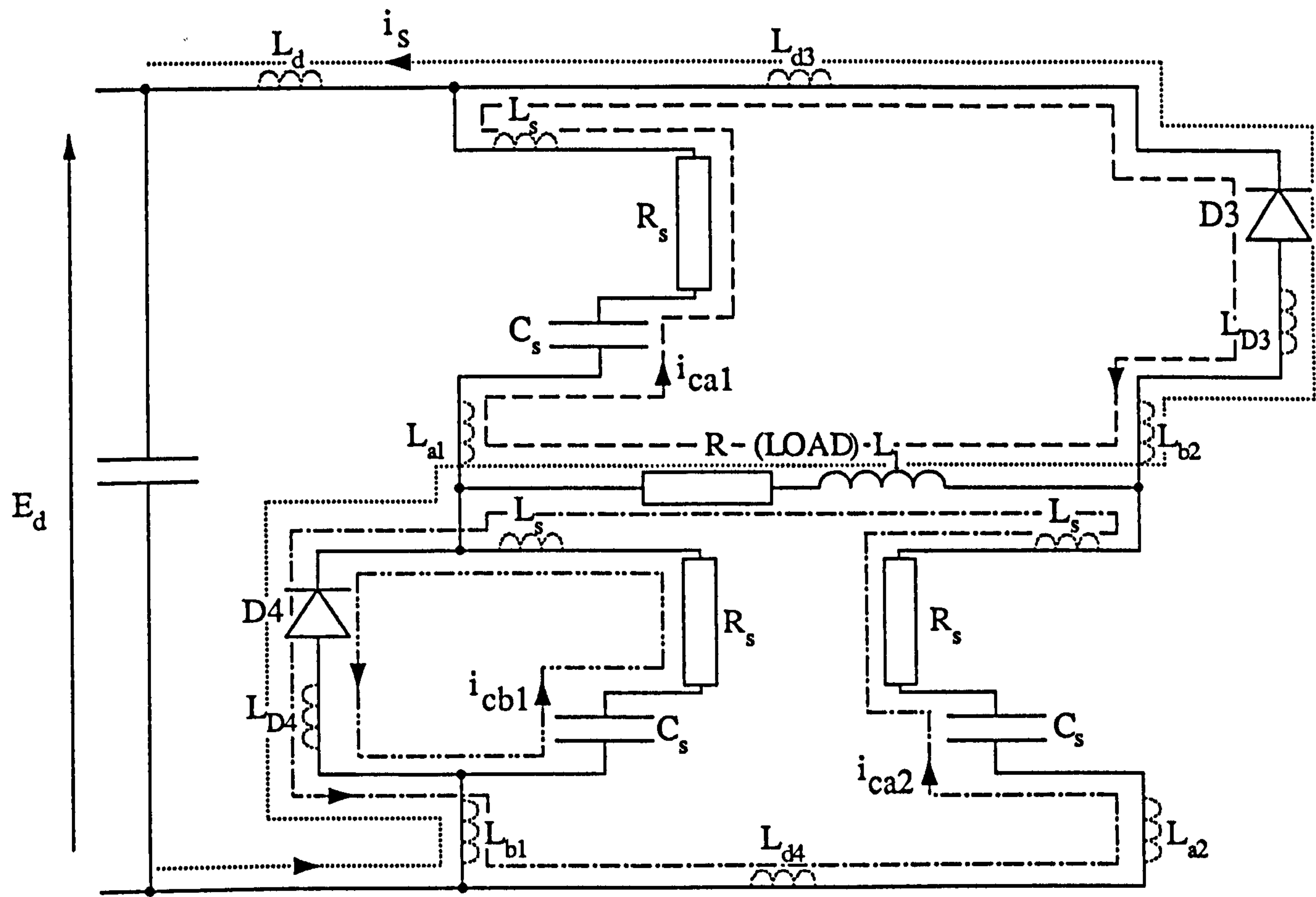
$$\begin{bmatrix} p i_{ca1} \\ p i_{ca2} \\ p i_{cb1} \\ p i_s \\ p v_{ca1} \\ p v_{ca2} \\ p v_{cb1} \end{bmatrix} = \begin{bmatrix} -\left(R \frac{L_{37}}{L_{35}} - R_s \frac{L_{38}}{L_{35}}\right) & -R \frac{L_{37}}{L_{35}} \\ -\left(R \frac{L_{20}}{L_{18}} - R_s \frac{L_{21}}{L_{18}}\right) & -R \frac{L_{20}}{L_{18}} \\ -\left(R \frac{L_{31}}{L_{29}} - R_s \frac{L_{32}}{L_{29}}\right) & -R \frac{L_{31}}{L_{29}} \\ -\left(R \frac{L_{25}}{L_{18}} - R_s \frac{L_{26}}{L_{18}}\right) & -R \frac{L_{25}}{L_{18}} \\ \frac{1}{C_s} & 0 \\ 0 & \frac{1}{C_s} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} i_{ca1} \\ i_{ca2} \\ i_{cb1} \\ i_s \\ v_{ca1} \\ v_{ca2} \\ v_{cb1} \end{bmatrix} + \begin{bmatrix} E_d \frac{L_{36}}{L_{35}} \\ E_d \frac{L_{19}}{L_{18}} \\ E_d \frac{L_{30}}{L_{29}} \\ E_d \frac{L_{24}}{L_{18}} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

(Columns 3 to 7 as in (f))

(j)

Figure 4.14 Equivalent circuits and state equations matrices for GTO A1 turning off after A2 (start of feedback).

Time interval t7



(k)

COLUMNS

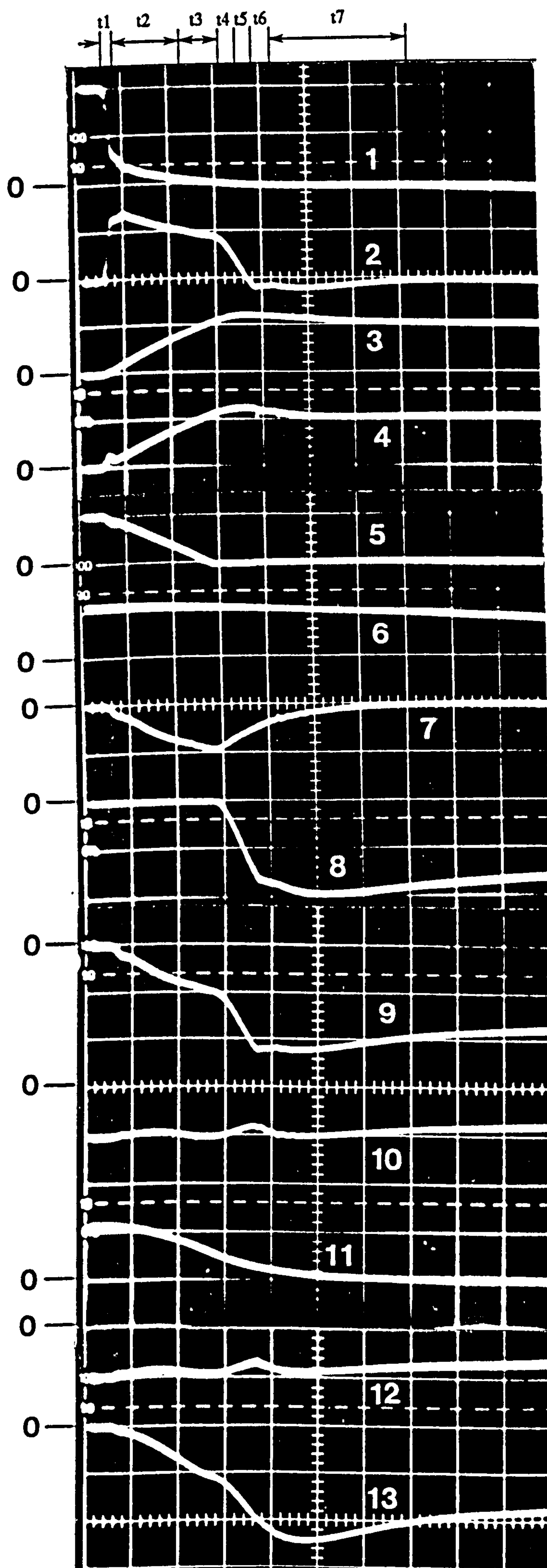
(1)                      (2)                      (3) (4) (5) (6) (7)

$\begin{bmatrix} p i_{ca1} \\ p i_{ca2} \\ p i_{cb1} \\ p i_s \\ p v_{ca1} \\ p v_{ca2} \\ p v_{cb1} \end{bmatrix}$	$=$	$\begin{bmatrix} -\left(R\frac{L_{37}}{L_{35}} - R_s\frac{L_{38}}{L_{35}}\right) - \left(R\frac{L_{37}}{L_{35}} - R_s\frac{L_{39}}{L_{35}}\right) \\ -\left(R\frac{L_{20}}{L_{18}} - R_s\frac{L_{21}}{L_{18}}\right) - \left(R\frac{L_{20}}{L_{18}} + R_s\frac{L_{22}}{L_{18}}\right) \\ -\left(R\frac{L_{31}}{L_{29}} - R_s\frac{L_{32}}{L_{29}}\right) - \left(R\frac{L_{31}}{L_{29}} - R_s\frac{L_{33}}{L_{29}}\right) \\ -\left(R\frac{L_{25}}{L_{18}} - R_s\frac{L_{26}}{L_{18}}\right) - \left(R\frac{L_{25}}{L_{18}} + R_s\frac{L_{27}}{L_{18}}\right) \\ \frac{1}{C_s} & 0 \\ 0 & \frac{1}{C_s} \\ 0 & 0 \end{bmatrix}$	$\begin{bmatrix} i_{ca1} \\ i_{ca2} \\ i_{cb1} \\ i_s \\ v_{ca1} \\ v_{ca2} \\ v_{cb1} \end{bmatrix}$	$+$	$\begin{bmatrix} E_d\frac{L_{36}}{L_{35}} \\ E_d\frac{L_{19}}{L_{18}} \\ E_d\frac{L_{30}}{L_{29}} \\ E_d\frac{L_{24}}{L_{18}} \\ 0 \\ 0 \\ 0 \end{bmatrix}$
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(Columns 3 to 7  
as in (f))

(l)

Figure 4.14    Equivalent circuits and state equations matrices for GTO A1 turning off after A2 (start of feedback).



- (1) A1 Anode Current (20A/div)
- (2) A1 Snubber Capacitor Current (20A/div.)
- (3) A1 Snubber Capacitor Voltage (200V/div.)
- (4) A1 A-K Voltage (200V/div.)
- (5) B1 A-K Voltage (200V/div.)
- (6) Load Current (40A/div.)
- (7) B1 Snubber Capacitor Current (20A/div.)
- (8) Diode D4 Current (20A/div.)
- (9) B1 Branch Current (20A/div.)
- (10) B2 Branch Current (40A/div.)
- (11) B1 Snubber Capacitor Voltage (200V/div.)
- (12) Diode D3 Current (40A/div.)
- (13) Supply Current (20A/div.)

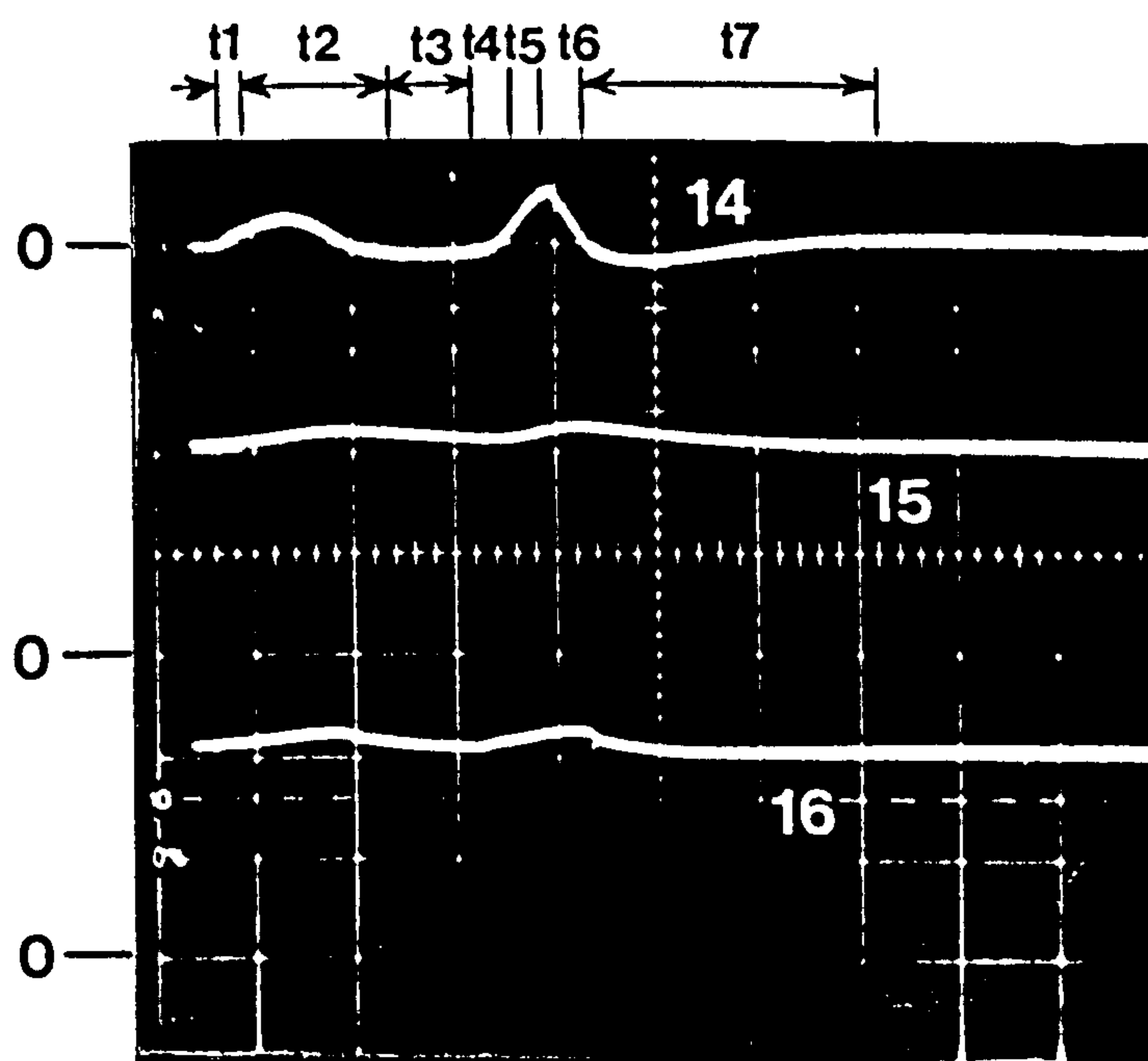
Time Scale: 2 $\mu$ S/div.

(a) Experimental Results

Figure 4.15 Waveforms at GTO A1 turn-off after A2

CONTINUED





(14) A2 Snubber Capacitor Current  
(10A/div.)

(15) A2 Snubber Capacitor Voltage  
(100V/div.)

(16) A2 A-K Voltage  
(100V/div.)

Time Scale: 2 $\mu$ S/div.

(a) Experimental Results

Figure 4.15 Waveforms at GTO A1 turn-off after A2

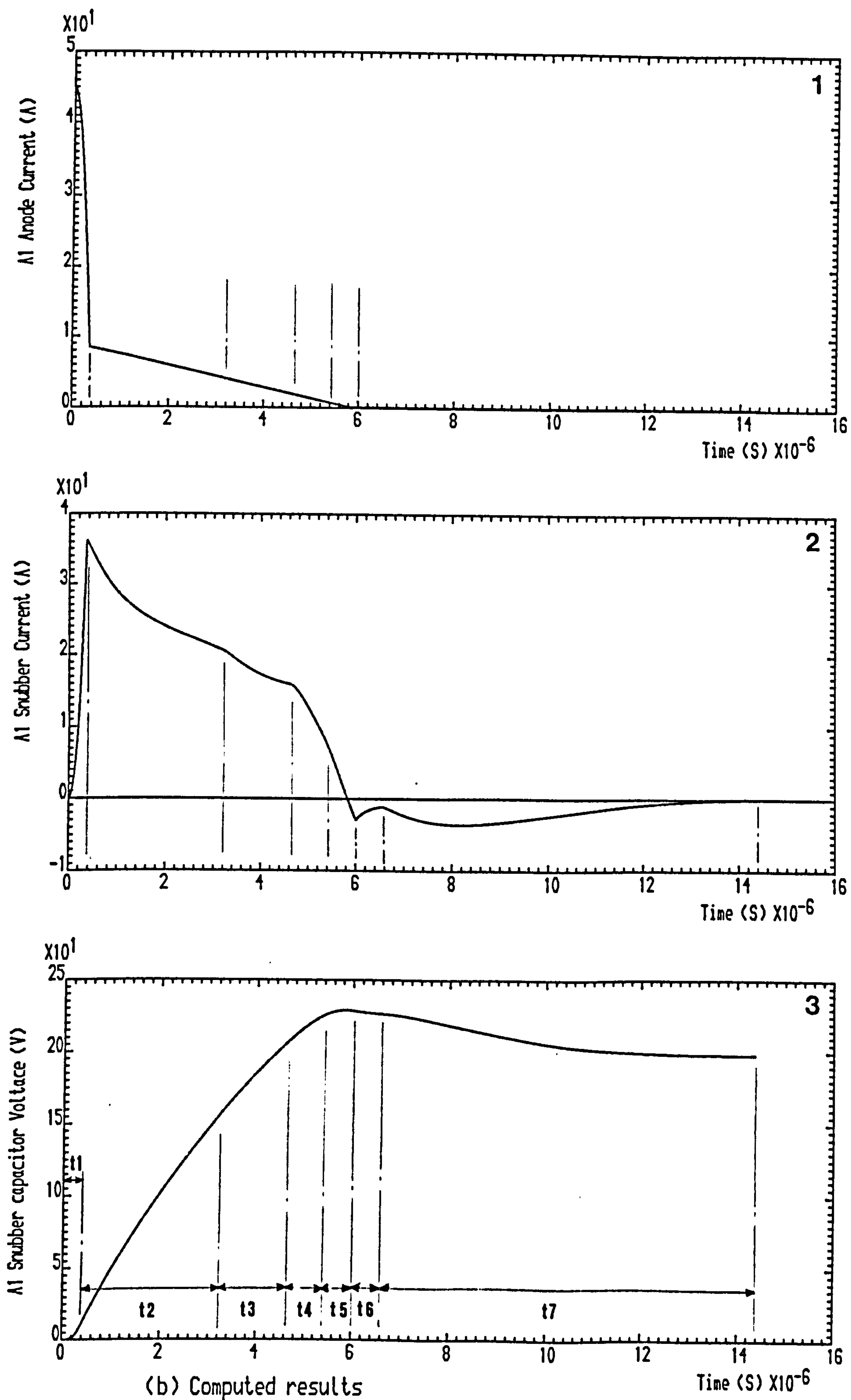
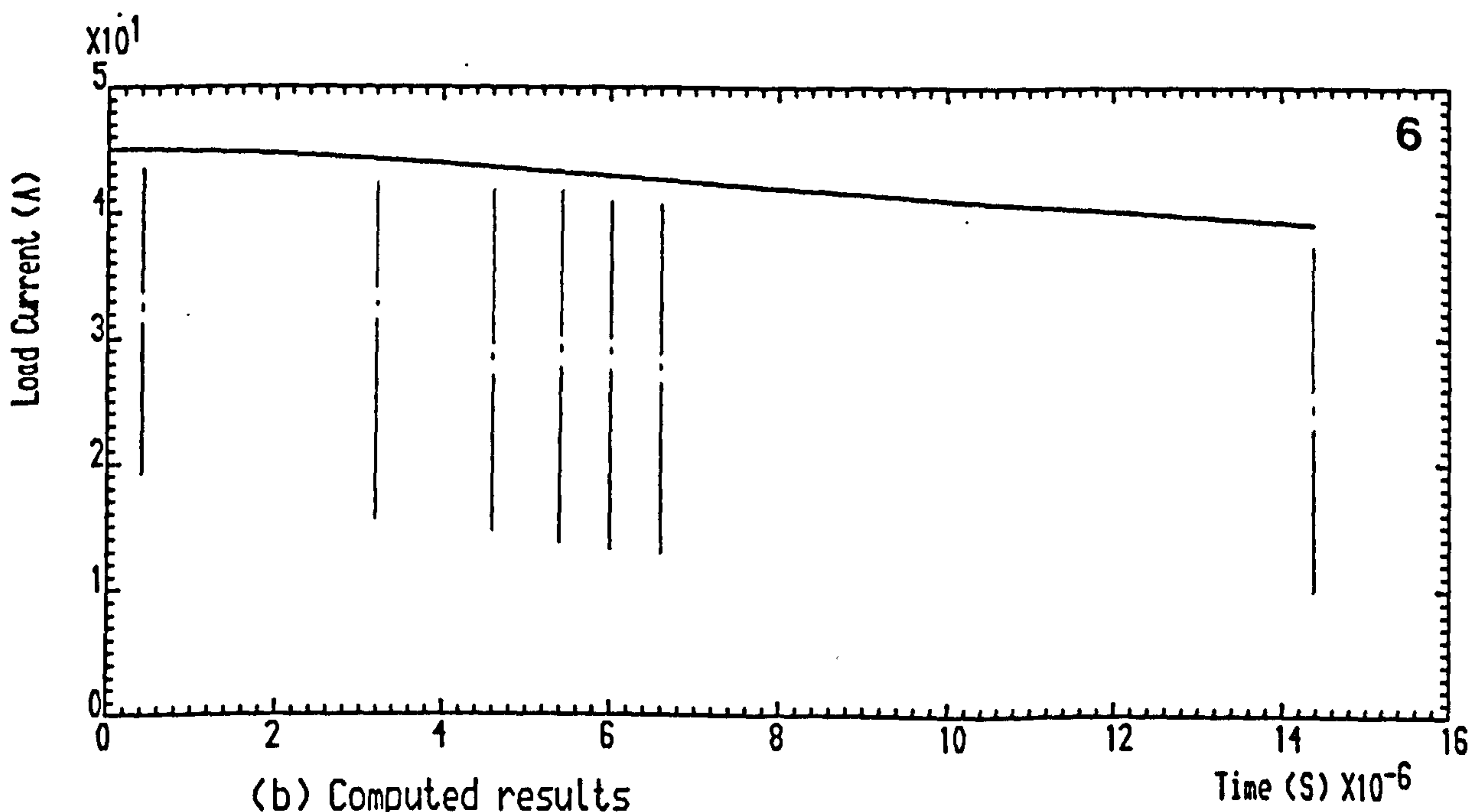
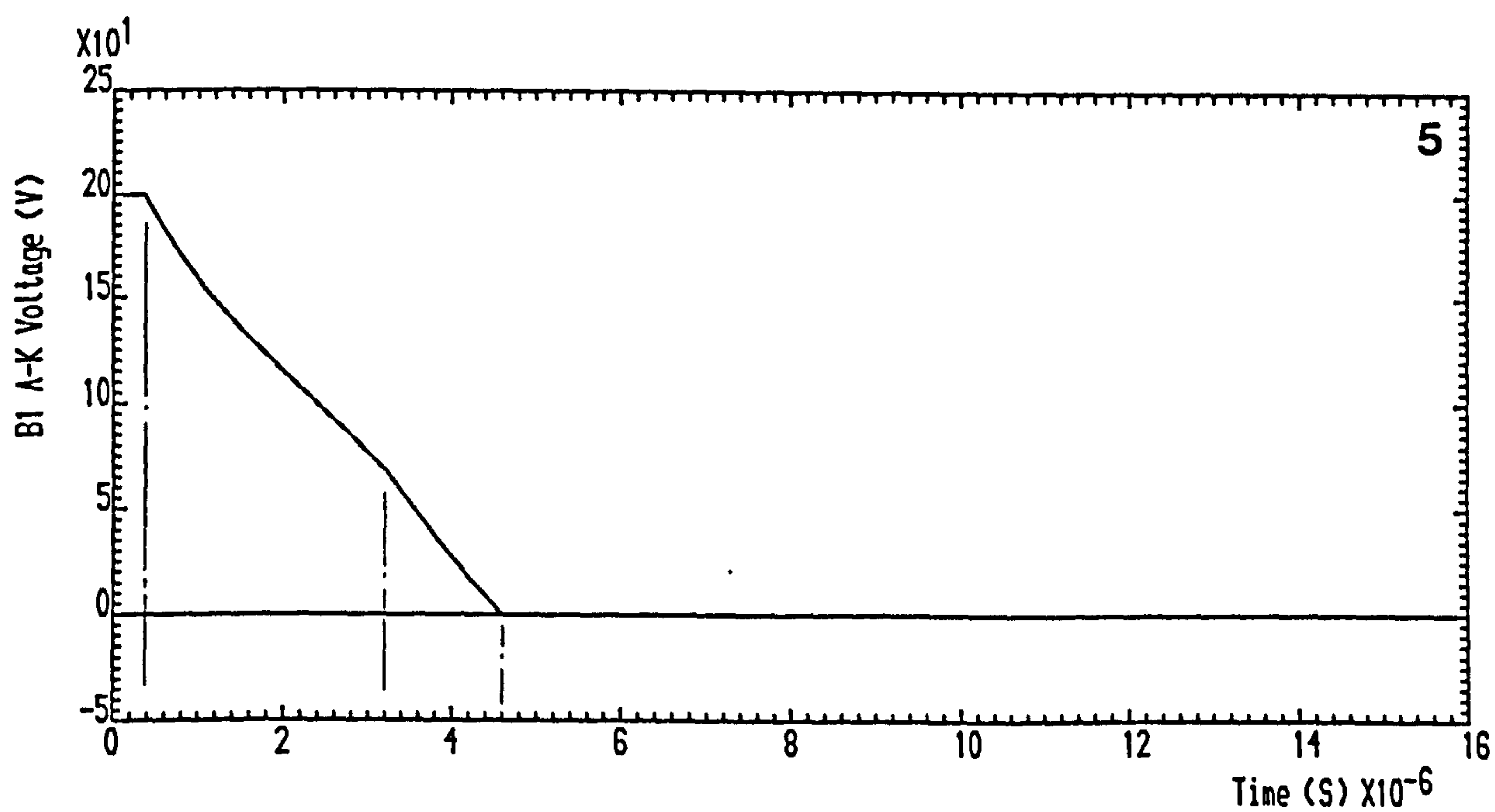
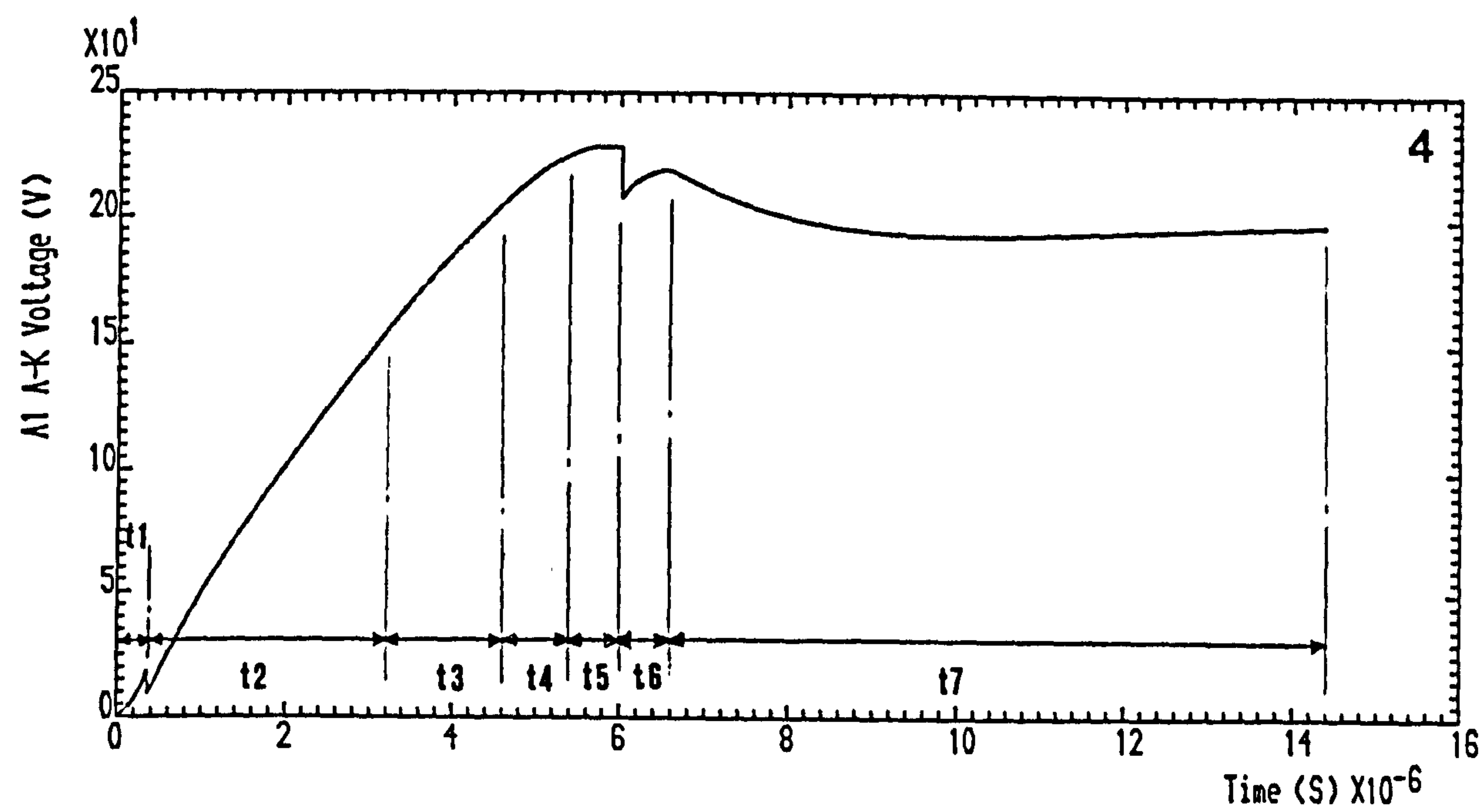


Figure 4.15 Waveforms at GTO A1 turn-off after A2

CONTINUED ..

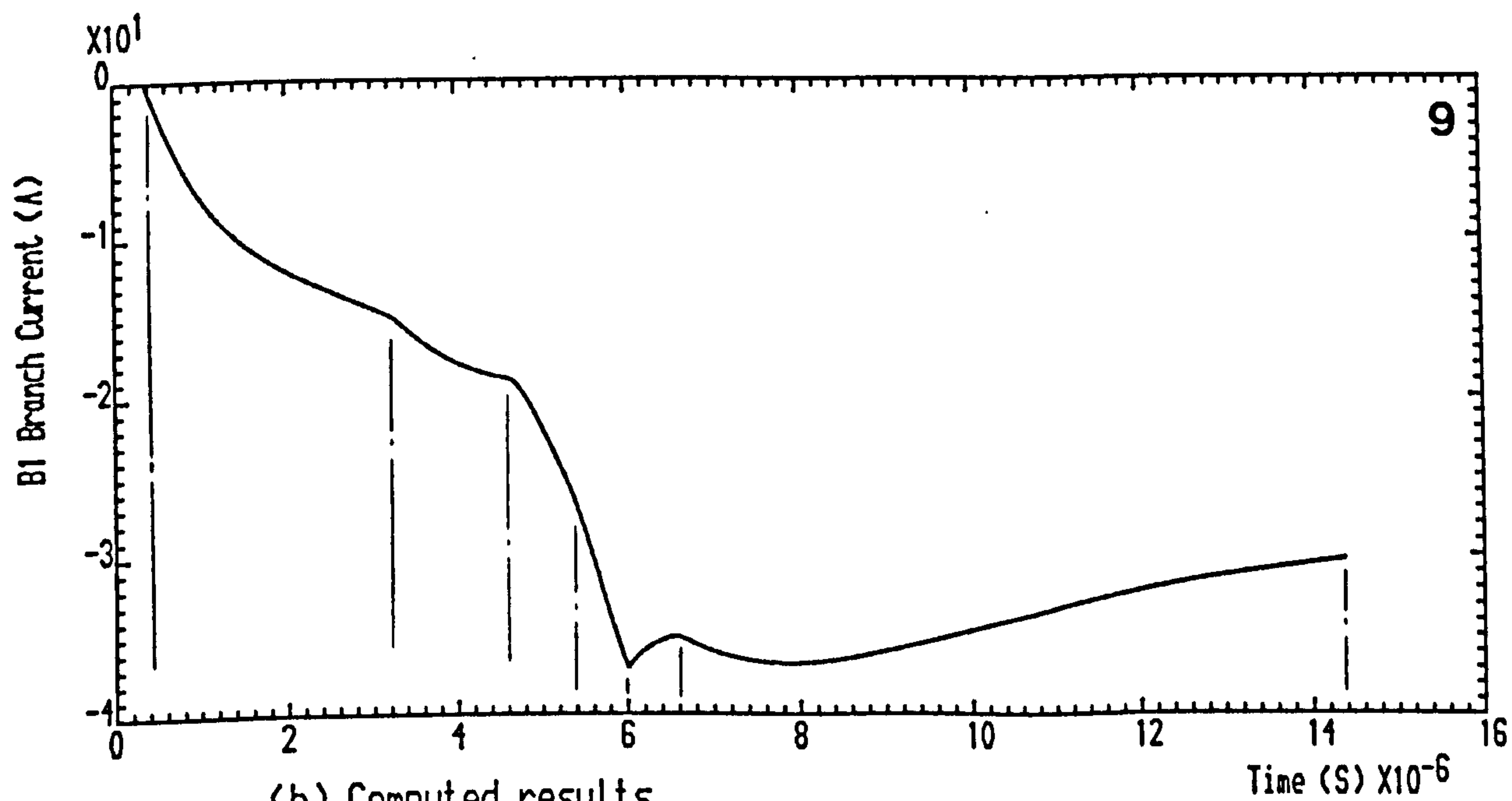
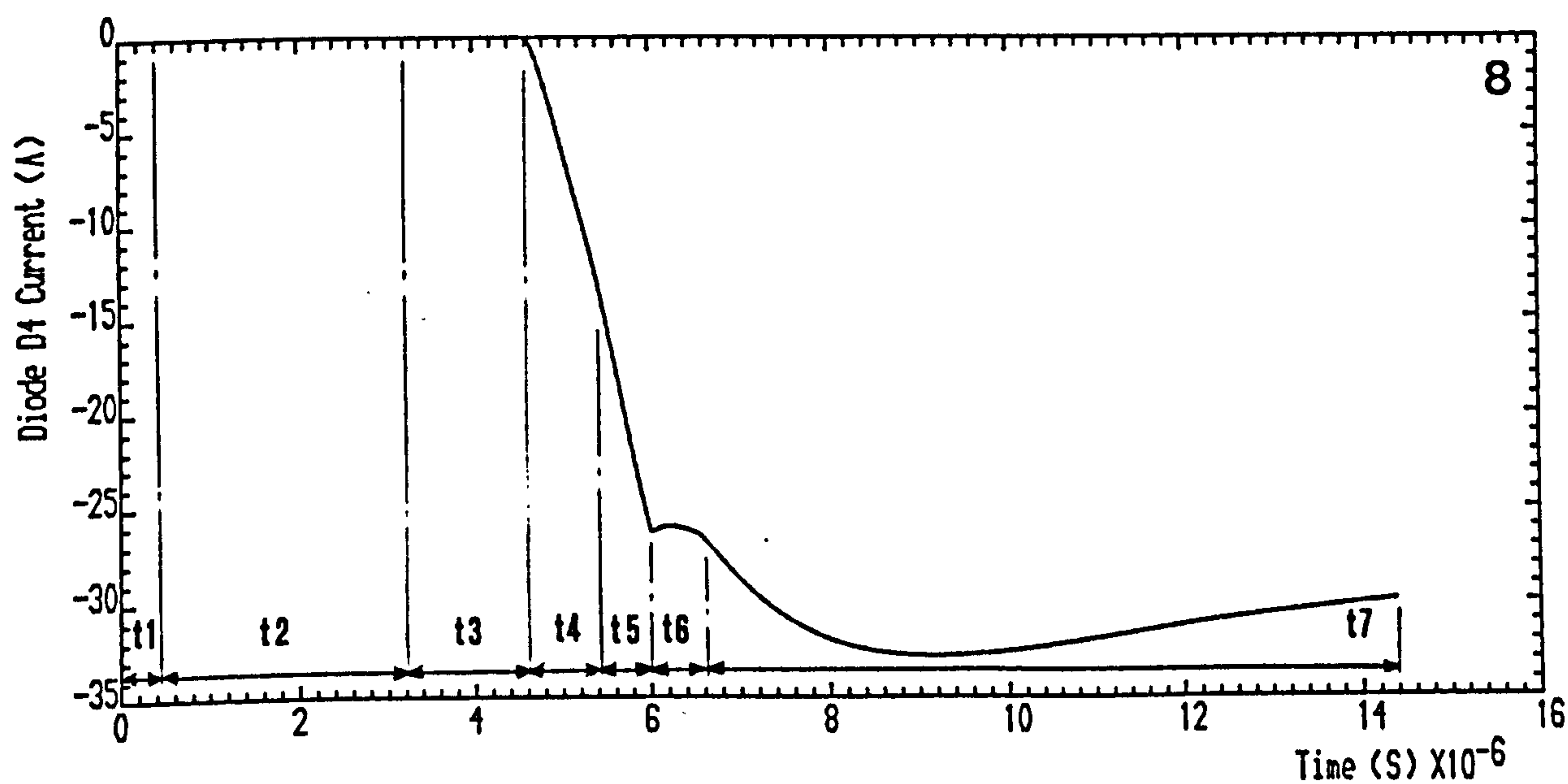
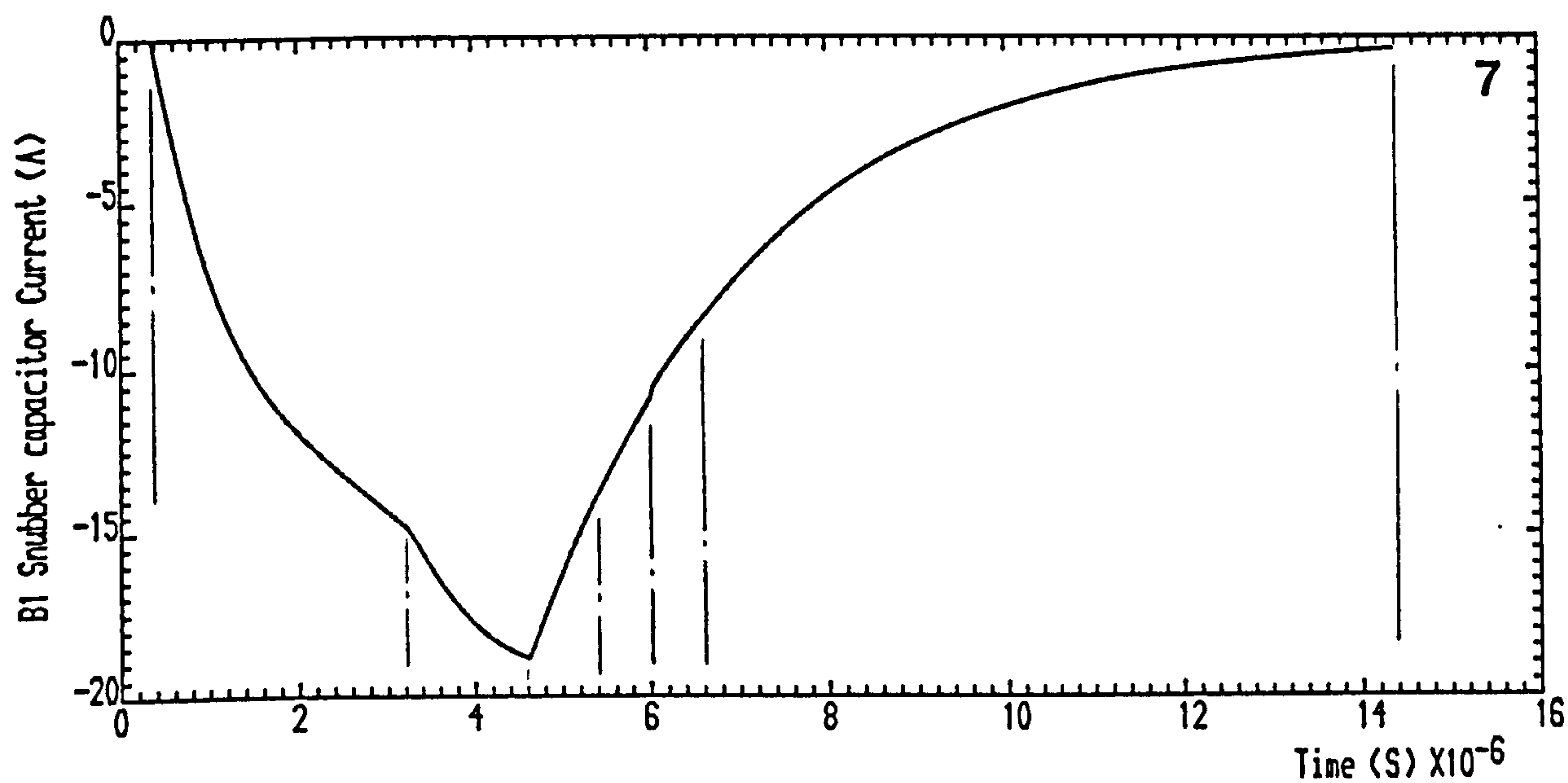


(b) Computed results

Figure 4.15 Waveforms at GTO A1 turn-off after A2

CONTINUED ..

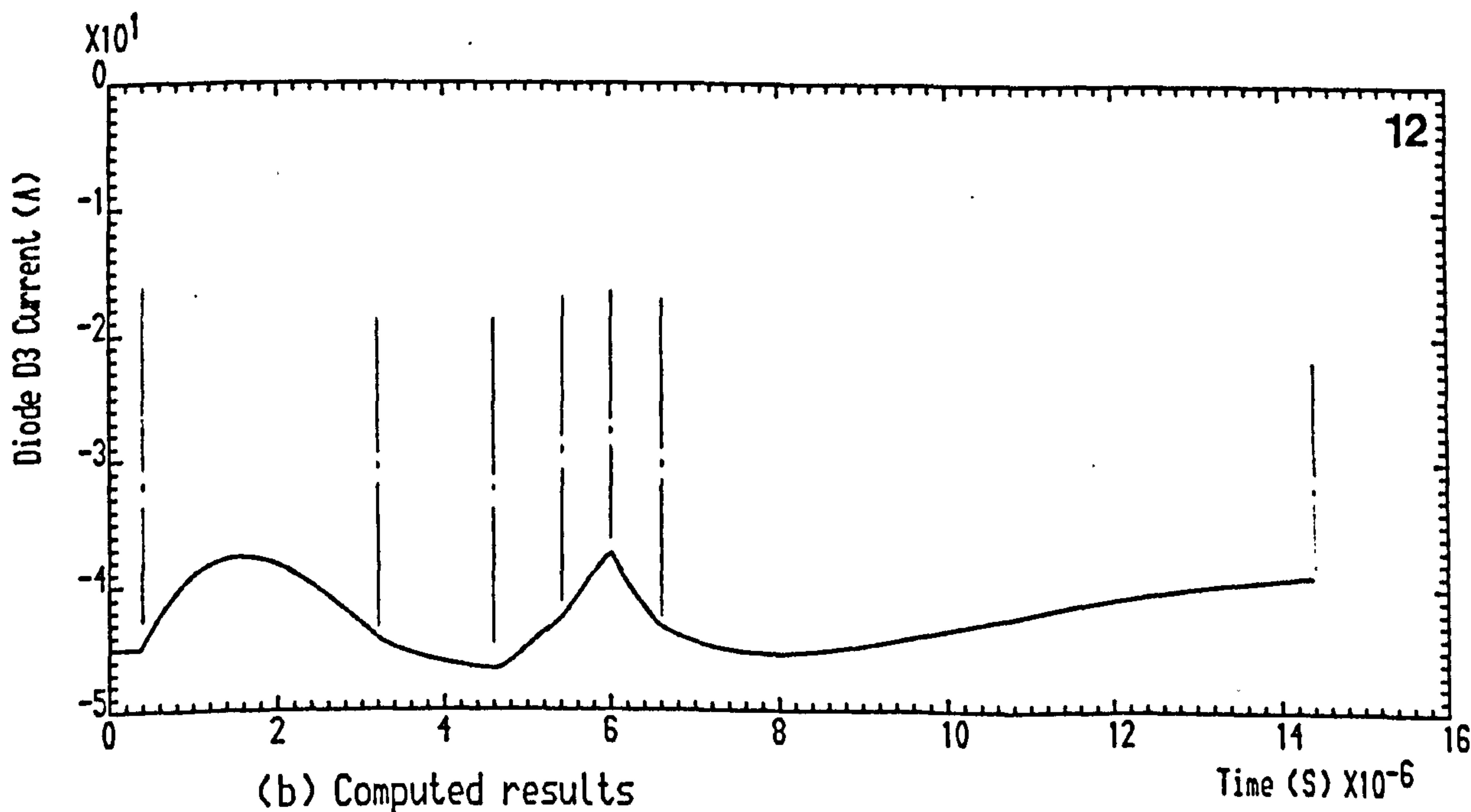
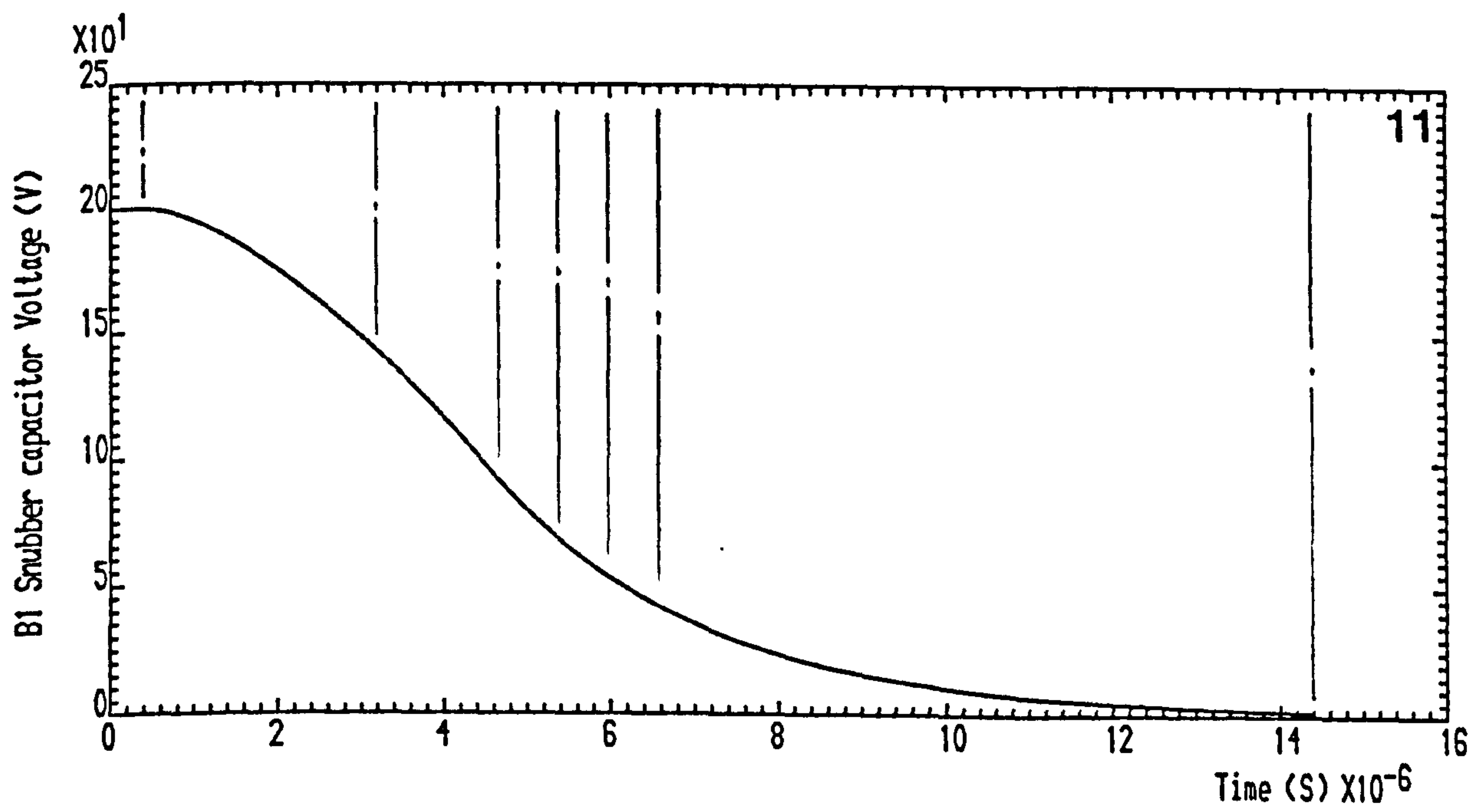
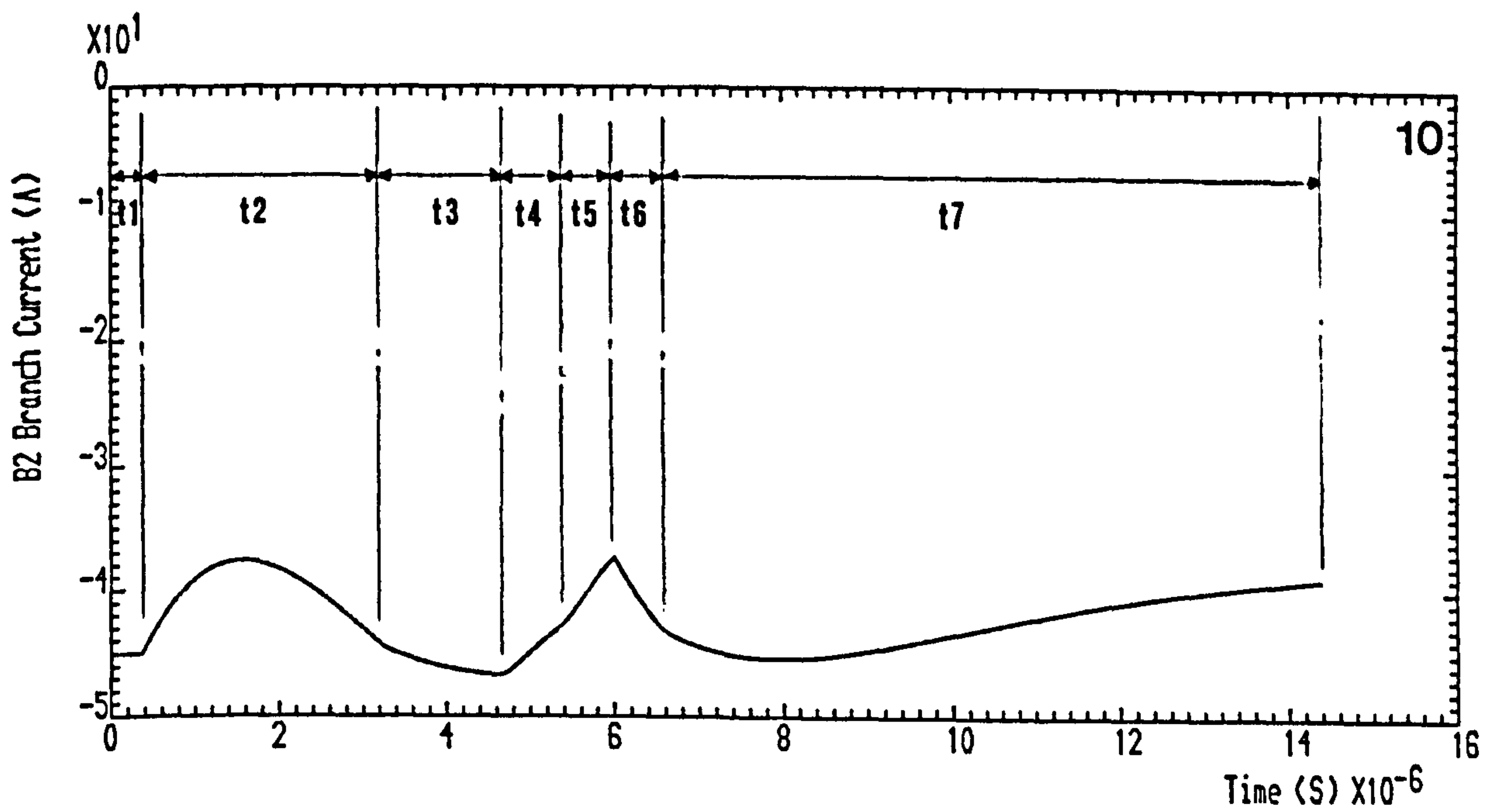




(b) Computed results

Figure 4.15 WaveForms at GTO A1 turn-off after A2

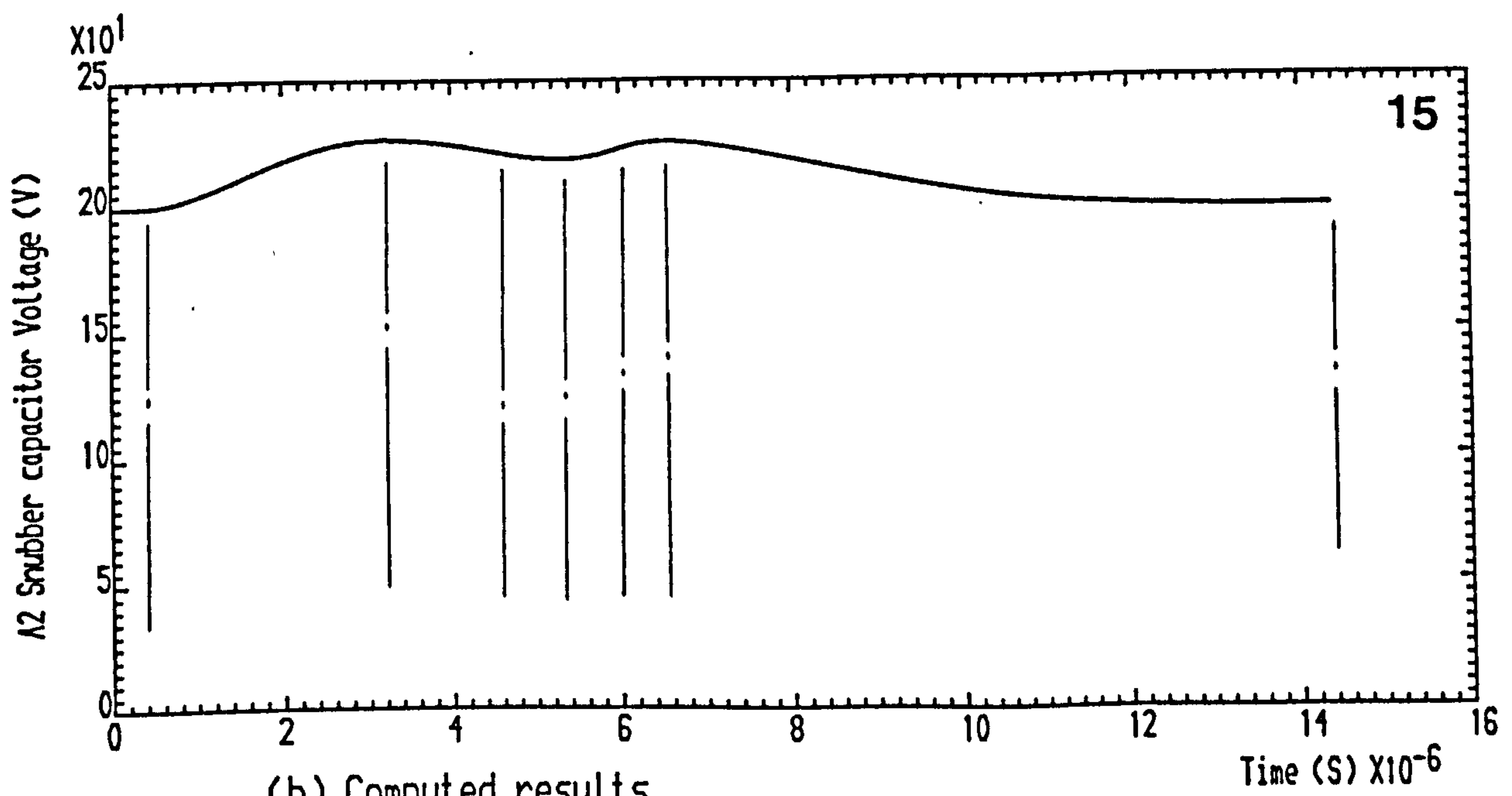
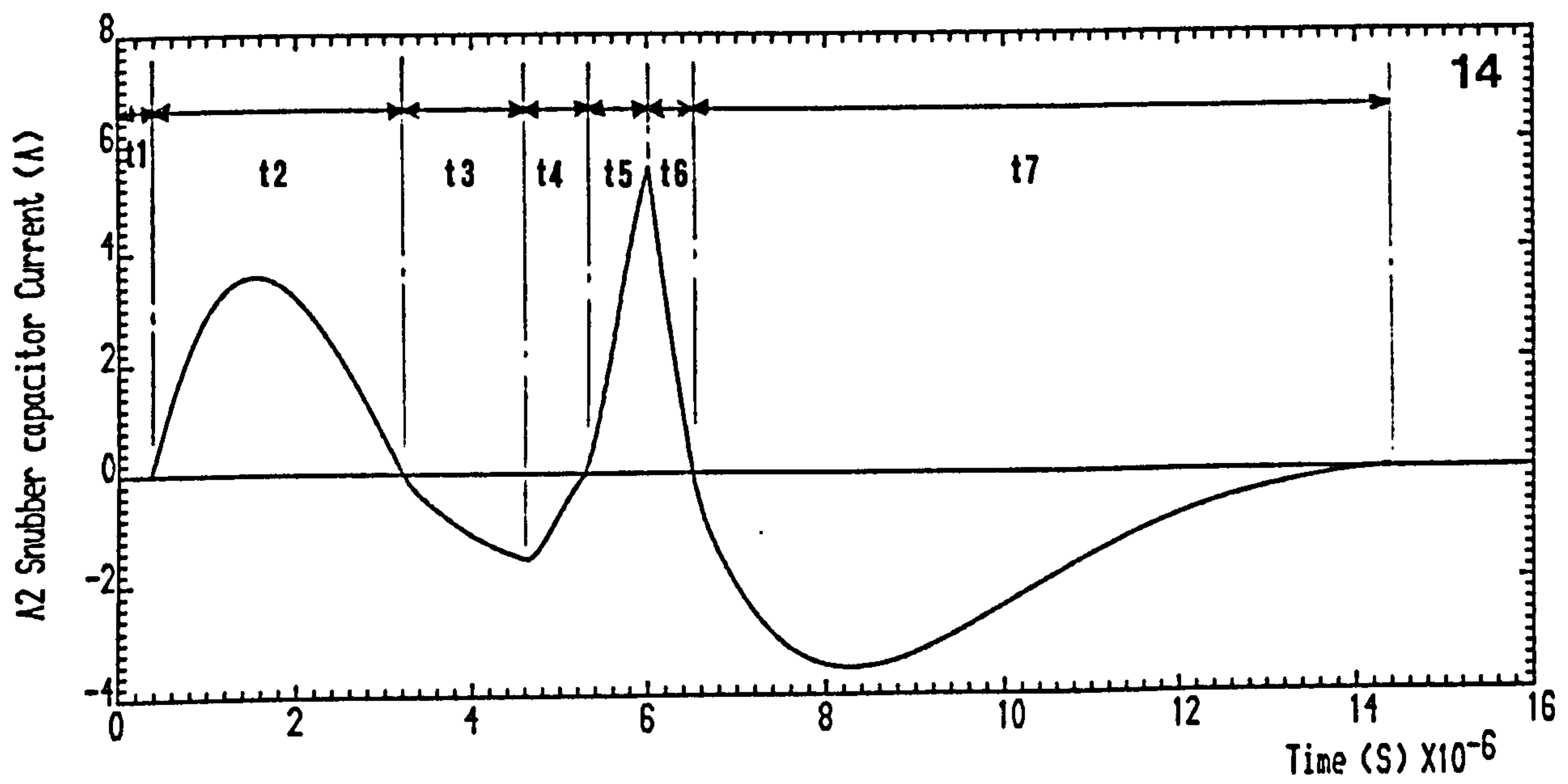
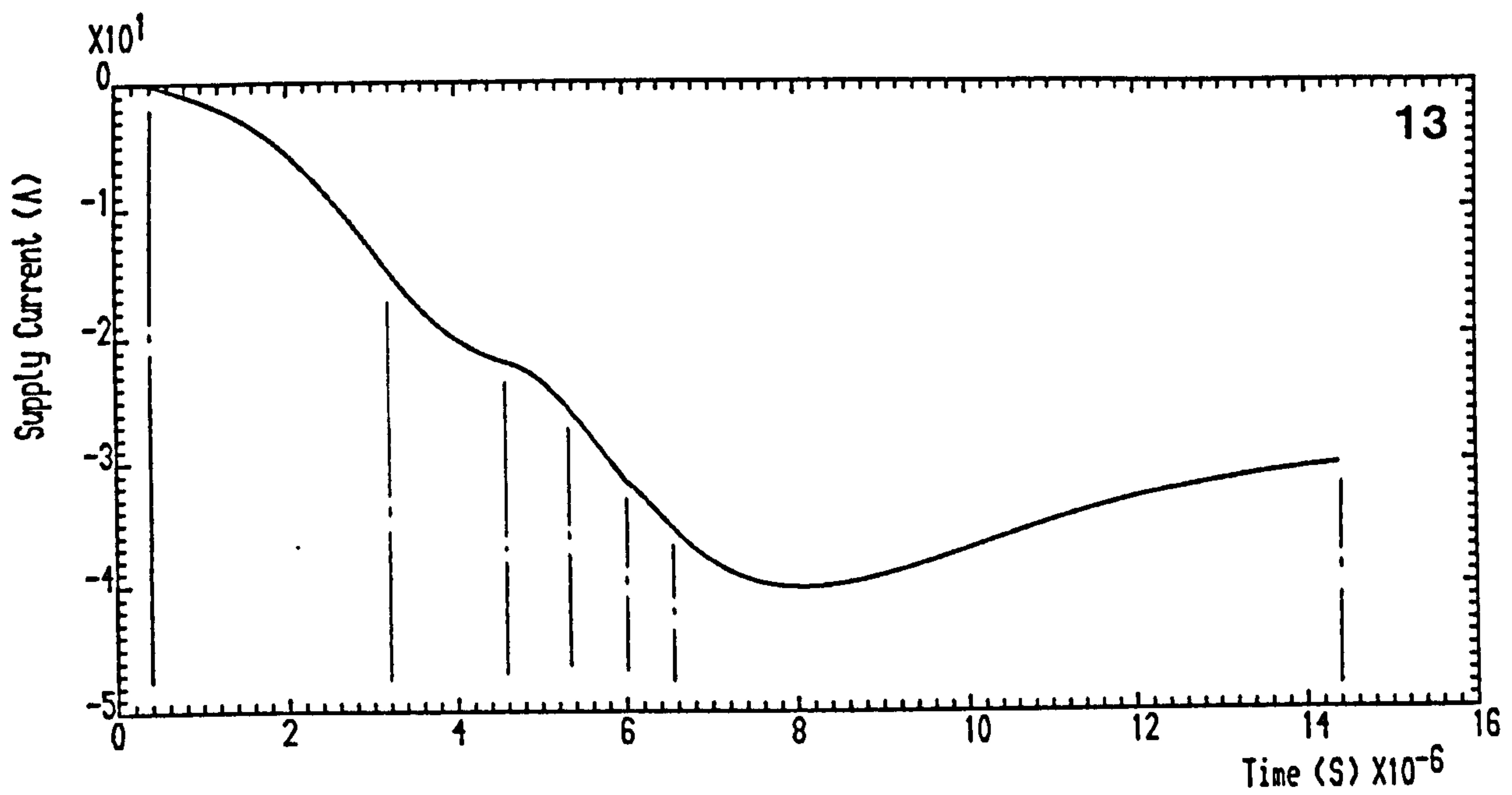
CONTINUED ..



(b) Computed results

Figure 4.15 Waveforms at GTO A1 turn-off after A2

CONTINUED ..



(b) Computed results

Figure 4.15 Waveforms at GTO A1 turn-off after A2

CONTINUED ..



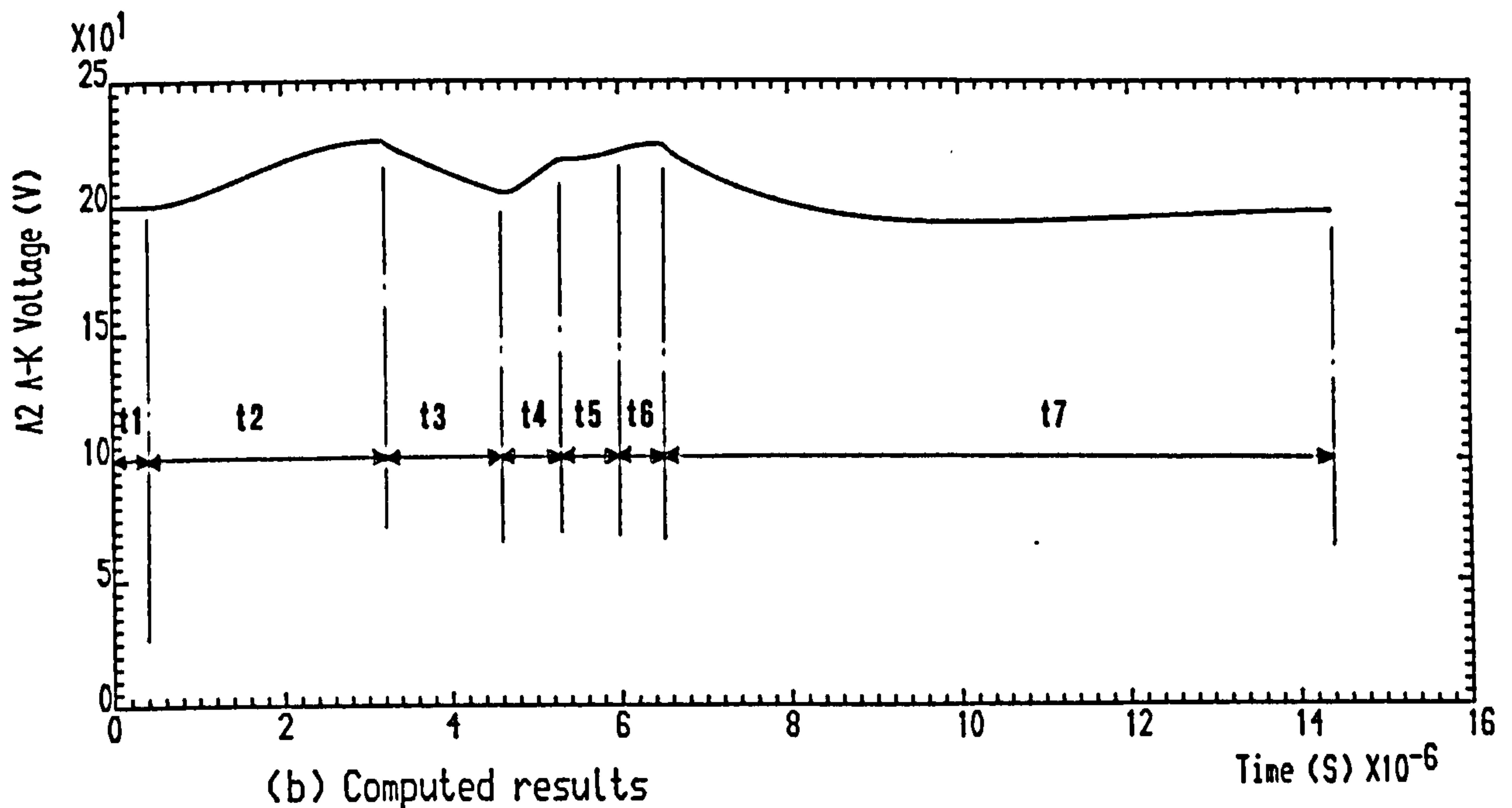


Figure 4.15 Waveforms at GTO A1 turn-off after A2

END ..

**Interval t6:** This interval, which is represented by the equivalent circuit and state equations of Figure 4.14(i) and (j) respectively, lasts from the reverse recovery of A1 snubber diode to the full charge of A2 snubber capacitor. As A1 snubber capacitor starts discharging through its snubber resistor, a 'hold-up' effect is experienced by GTO A1 due to the over-voltage across GTO A2, Figure 4.15, traces (4) and (16).

**Interval t7:** This interval commences when A2 snubber capacitor starts discharging and ends when the A1 and A2 snubber capacitor discharge currents fall to zero. The equivalent circuit and its state equations are shown in Figure 4.14(k) and (l). The A1 and A2 snubber capacitors discharge through their snubber resistors to blocking voltage  $E_d$ , Figure 4.14, traces (2), (3), (14) and (15).

Interval t7 is followed by diodes D3 and D4 conducting the decaying load inductive energy back to the source, with GTOs A1 and A2 blocking the supply voltage.

The effective stray inductances are principally those of the source, antiparallel diodes and the bridge DC rails.

**c) At turn-off of both conducting GTOs A1 and A2 together**

By turning off the conducting GTO pair A1 and A2, the load current transfers to diodes D3 and D4 symmetrically if  $L_{d3}$  and  $L_{d4}$  are negligibly small, the usual GTO voltage spikes and oscillatory overshoots occurring. The load current divides between the upper and lower branches at the nodes at both sides of the H-bridge instead of just one. There is no independent blocking GTO thyristor to experience a diagonally coupled over-voltage, as before.

A feature likely to occur in practice is a difference of turn-off instant between the two GTOs being switched (switching time mismatch). This can be attributed to GTO turn-off time differences [27] and/or timing inaccuracies of the gate drive applied. On the experimental rig, a gate drive turn-off pulse timing discrepancy is observed and a difference of GTO turn-off waveforms giving approximately  $1.2\mu\text{s}$  lag of GTO A1 turn-off relative to A2, as demonstrated in Figure 4.16. The result is that the conditions of single GTO turn-off occur for this short interval giving some small asymmetry in the waveforms. This is detailed as follows, with the actual computed waveforms shown in black and the predicted balanced switching waveforms in red in Figure 4.18(b).

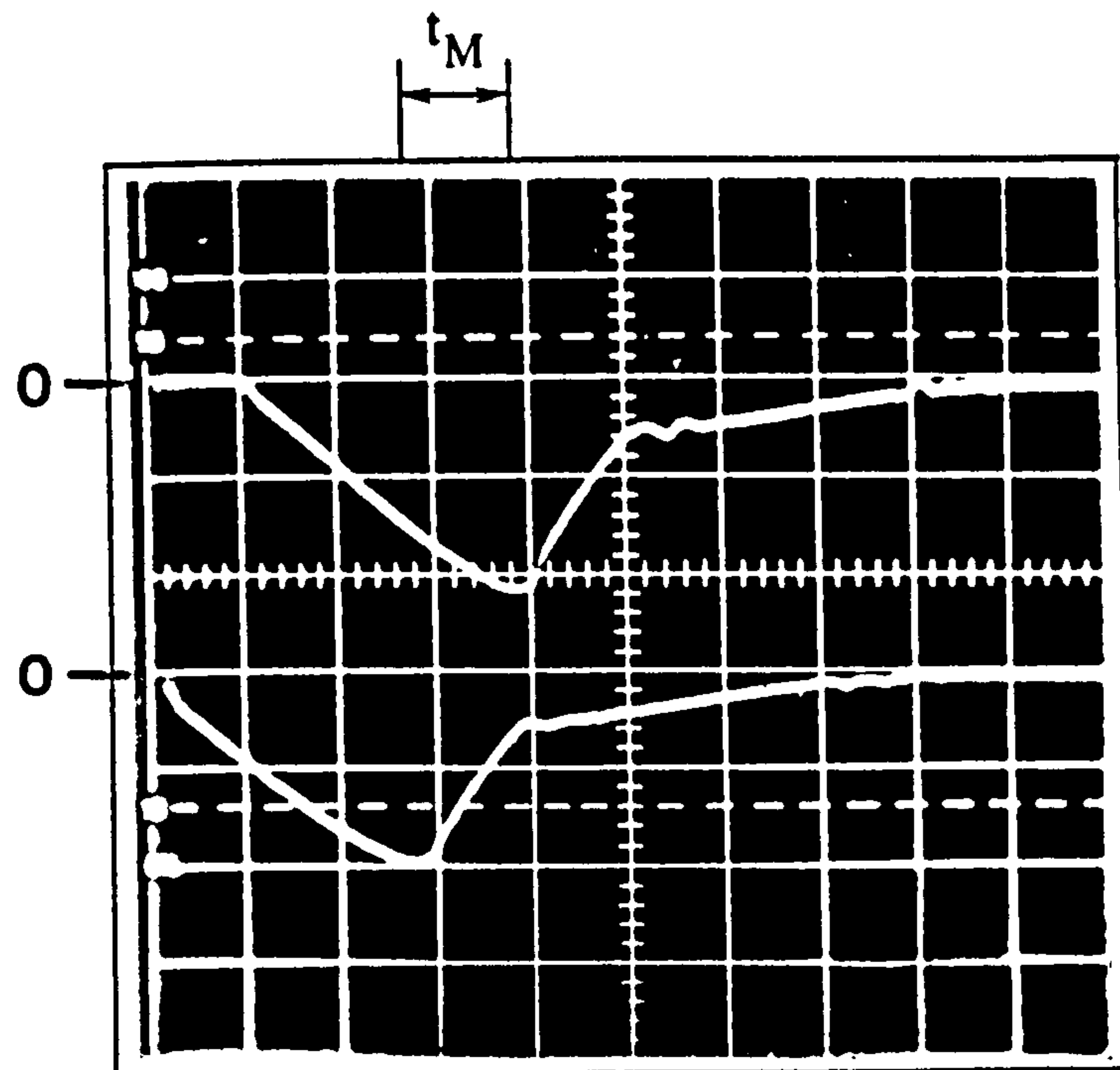
Upon completion of interval t1 for GTO A2, the equivalent circuit and state equations for interval t2 become as shown earlier in Figure 4.13(a) and (b).

**Interval t2:** As before, when A2 turns off first, the B1 snubber capacitor overcharging commences through GTO A1 due to the rise in DC rail potential caused by  $L_d di/dt$ , which results in A1 having to turn-off increased current (Figure 4.18, traces (1), (2) and (8)). This could be dangerous if it is operating near its turn-off current limit.

**Interval t3:** The equivalent circuit and matrix state equations of this interval are given in Figure 4.17(a) and (b). The duration is the GTO A1 current fall time, Figure 4.18, trace (1).

GTO A1 turns off with the constant load current supporting a slight increase in A2 snubber capacitor current as that of B2 snubber capacitor, now in part being returned to the supply, falls at a reduced rate, Figure 4.18, traces (6), (7) and (16). It can be





- (1) A1 Negative Gate Current (20A/div.)  
 (2) A2 Negative Gate Current (20A/div.)

Time Scale: 1  $\mu$ S/div.

Figure 4.16 Switching time mismatch ( $t_M$ ) at GTOs A1 and A2 turning off together

seen from the experimental results (figure 4.18(a), traces (2) and (18)) that during this interval, the B1 snubber capacitor current starts to decay, whereas, with the computed waveforms, Figure 4.18(b), trace (2), it does not. This is due to the somewhat approximated GTO characteristics, i.e. linear anode current fall instead of the cosine function (chapter 3, sub-section 3.3.1 (b)).

**Interval t4:** This is a short period, where the B1 snubber capacitor oscillatory overcharging current completes its decay to zero, Figure 4.18, traces (2) and (18). The equivalent circuit and its system matrix are shown in Figure 4.17(c) and (d).

**Interval t5:** This commences when the B1 snubber capacitor starts its discharge and ends when the voltage across B2 reaches zero. The equivalent circuit and state equations are as those of Figure 4.17(e) and (f).



The charging currents of A1 and A2 snubber capacitors are now falling, whereas the B1 and B2 snubber capacitor discharge currents are rising accordingly through their snubber resistors and the source, Figure 4.18, traces (3), (6), (13) and (18). It can be seen from trace (19), that a sudden voltage drop occurs across GTO B1 as its snubber capacitor current reverses into the associated snubber resistor. The voltages across A1 and A2 snubber capacitors overshoot  $E_d$ , traces (4) and (9).

**Interval t6:** This interval starts as diode D3 commences to conduct and ceases when the A2 snubber diode is fully reverse recovered. The equivalent circuit and state equations are shown respectively in Figure 4.17(g) and (h).

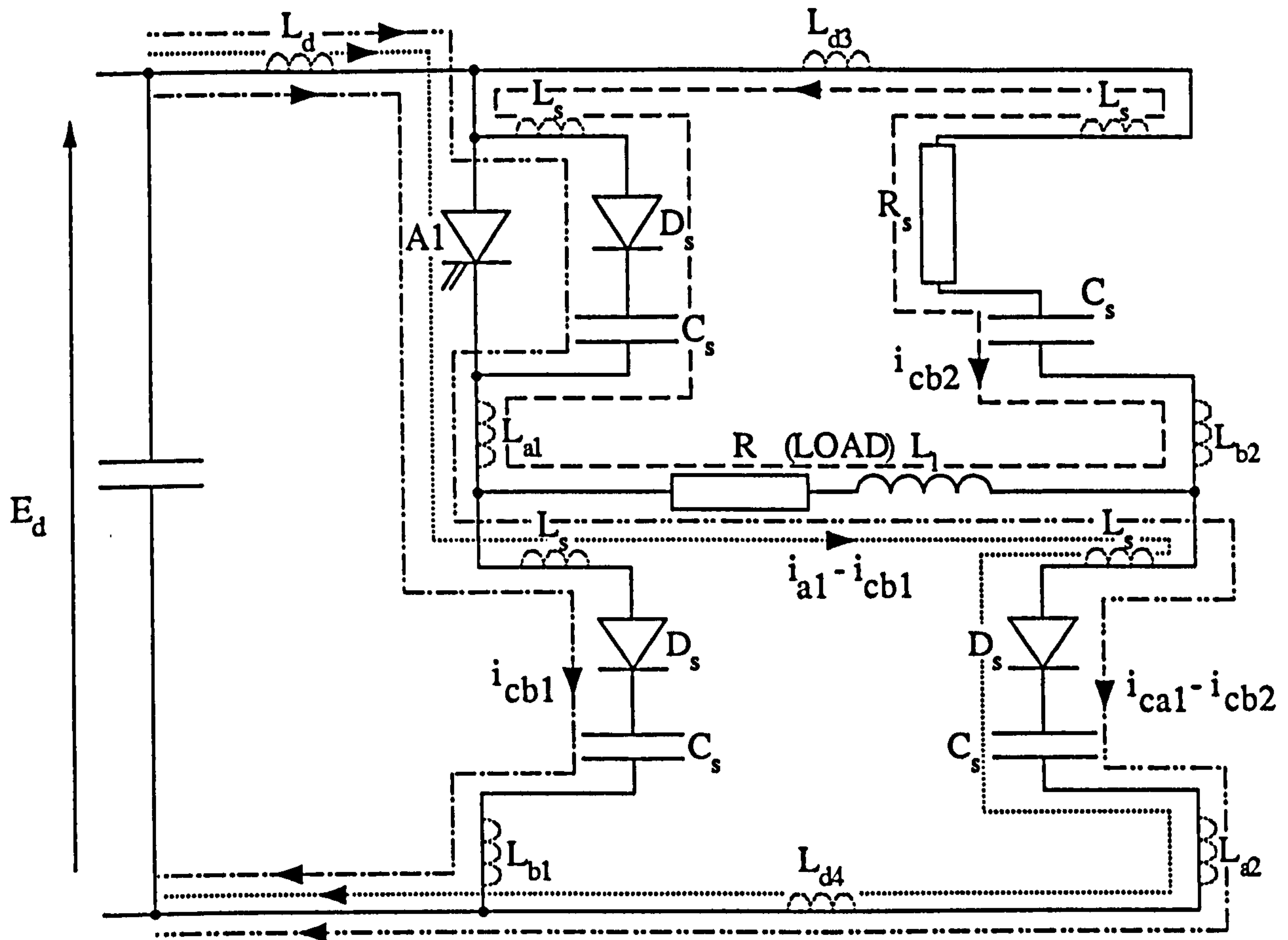
The forward biasing of diode D3, results in the increased rate of A2 snubber capacitor current decay, Figure 4.18, trace (6), with the voltage across it further overshooting the supply value and approaching its oscillatory peak, trace (9). The feedback current into the supply is now more rapid, giving a higher induced  $L_d di/dt$  which is felt across A1. Thus the A1 snubber capacitor charging current is being prevented from falling very much, Figure 4.18, trace (3). The now local discharge of B2 snubber capacitor current decays through its series resistor and diode D3.

**Interval t7:** Figure 4.17(i) and (j) give the equivalent circuit and matrix state equations of this very short interval which lasts from the reverse recovery of A2 snubber diode to the fall of B1 voltage to zero. The A2 snubber capacitor discharge current having transferred to the associated snubber resistor, drops the voltage across GTO A2 with a 'hold-up' effect exerted by the A1-B1 phase leg, Figure 4.18, trace (10).

**Interval t8:** This interval, the equivalent circuit and state equations of which are shown in Figure 4.17(k) and (l), is from the conduction commencement of diode D4 to the complete reverse recovery of A1 snubber diode. Diode D4 current rises, having taken over the rising B1 branch current from B1 snubber capacitor which is now discharging locally. The A1 snubber capacitor current perceptibly falls at a faster rate as its voltage approaches its oscillatory peak and exerts a 'hold-up' effect across GTO A2 via the DC rails and diodes D3 and D4, Figure 4.18, traces (5) and (10).

**Interval t9:** The start and fall to zero of A1 snubber capacitor discharge current indicates respectively the start and end of interval t9, the equivalent circuit and state

# Time interval t3



(a)

COLUMNS	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)		
$p i_{ca1}$	0	0	0	0	0	0	0	0	$i_{ca1}$	$-N$
$p i_{ca2}$	0	0	0	0	0	0	0	0	$i_{ca2}$	$N$
$p i_{cb1}$	$-\frac{RL_d}{L_{23}}$	$-\frac{RL_d}{L_{23}}$	$\frac{RL_d}{L_{23}}$	$\frac{R_s L_d}{L_{23}}$	$-\frac{L_d}{L_{23}}$	0	$-\frac{L_{21}}{L_{23}}$	$\frac{L_d}{L_{23}}$	$i_{cb1}$	$\frac{E_d L_{21} - NL_{18}}{L_{23}}$
$p i_{cb2}$	$\frac{RL_{20}}{L_{23}}$	$\frac{RL_{20}}{L_{23}}$	$-\frac{RL_{20}}{L_{23}}$	$-\frac{R_s L_{20}}{L_{23}}$	$\frac{L_{20}}{L_{23}}$	0	$\frac{L_1}{L_{23}}$	$-\frac{L_{20}}{L_{23}}$	$i_{cb2}$	$\frac{-E_d L_1 + NL_{22}}{L_{23}}$
$p v_{ca1}$	0	$\frac{1}{C_s}$	0	0	0	0	0	0	$v_{ca1}$	0
$p v_{ca2}$	$\frac{1}{C_s}$	$\frac{1}{C_s}$	$-\frac{1}{C_s}$	$\frac{1}{C_s}$	0	0	0	0	$v_{ca2}$	0
$p v_{cb1}$	0	0	$\frac{1}{C_s}$	0	0	0	0	0	$v_{cb1}$	0
$p v_{cb2}$	0	0	0	$\frac{1}{C_s}$	0	0	0	0	$v_{cb2}$	0

$$N = \frac{[2(t-t_0) I_{A1}]}{t_f^2}$$

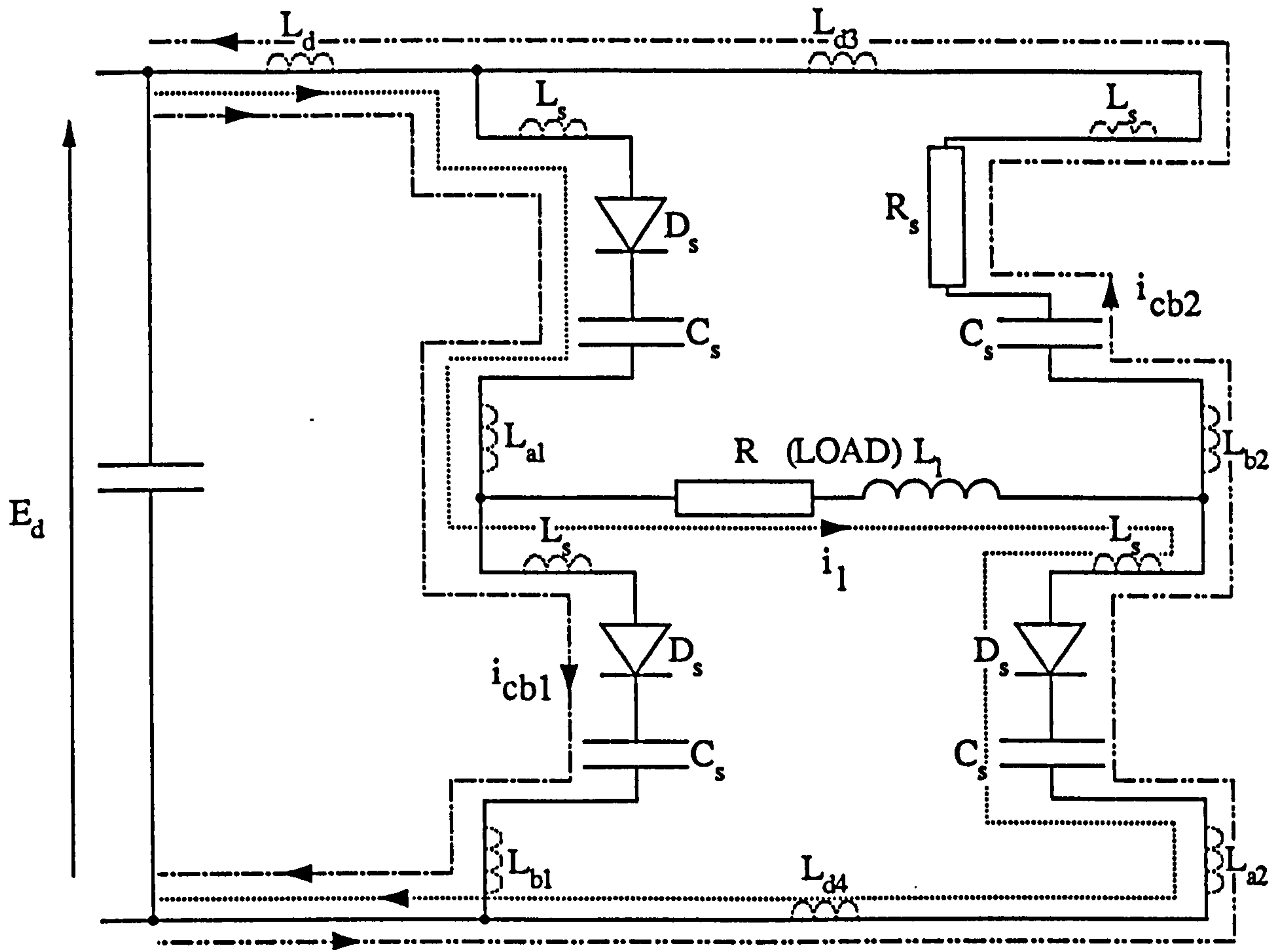
where  $t_0$  is the instant when  $I_{A1}$  commences falling

(b)

Figure 4.17 Equivalent circuits and state equations matrices at GTOs A1 and A2 turn-off together (Unbalanced turn-off).



Time interval t4



(c)

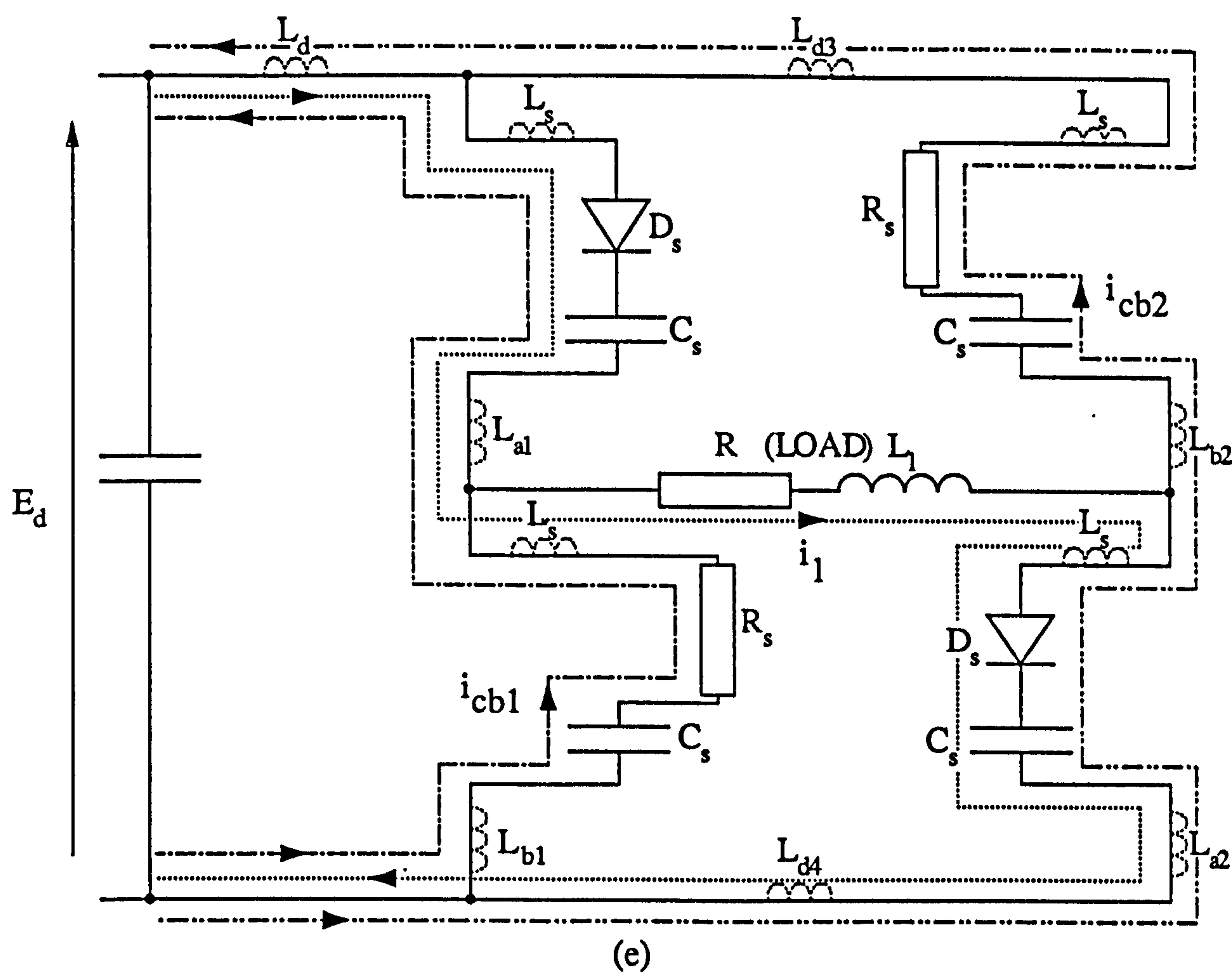
COLUMNS	(1)	(2)	(3)	(4)	(5)	(6)	(7)			
$p i_{cb1}$	0	$-\frac{R_s L_{36}}{L_{24}}$	$\frac{RL_{32}}{L_{24}}$	$\frac{L_{33}}{L_{24}}$	$\frac{L_{34}}{L_{24}}$	$-\frac{L_{35}}{L_{24}}$	$-\frac{L_{36}}{L_{24}}$	$i_{cb1}$	$\frac{E_d L_{31}}{L_{24}}$	
$p i_{cb2}$	0	$-\frac{R_s L_{30}}{L_{24}}$	$\frac{RL_{26}}{L_{24}}$	$\frac{L_{27}}{L_{24}}$	$\frac{L_{28}}{L_{24}}$	$-\frac{L_{29}}{L_{24}}$	$-\frac{L_{30}}{L_{24}}$	$i_{cb2}$	$\frac{E_d L_{25}}{L_{24}}$	
$p i_1$	0	$\frac{R_s L_{43}}{L_{37}}$	$-\frac{RL_{39}}{L_{37}}$	$-\frac{L_{40}}{L_{37}}$	$-\frac{L_{41}}{L_{37}}$	$\frac{L_{42}}{L_{37}}$	$\frac{L_{43}}{L_{37}}$	$i_1$	$\frac{E_d L_{38}}{L_{37}}$	
$p v_{ca1}$	$\frac{1}{C_s}$	0	$\frac{1}{C_s}$	0	0	0	0	$v_{ca1}$	+	0
$p v_{ca2}$	0	$\frac{1}{C_s}$	$\frac{1}{C_s}$	0	0	0	0	$v_{ca2}$		0
$p v_{cb1}$	$\frac{1}{C_s}$	0	0	0	0	0	0	$v_{cb1}$		0
$p v_{cb2}$	0	$\frac{1}{C_s}$	0	0	0	0	0	$v_{cb2}$		0

(d)

Figure 4.17 Equivalent circuits and state equations matrices at GTOs A1 and A2 turn-off together (Unbalanced turn-off).



Time interval  $t_5$



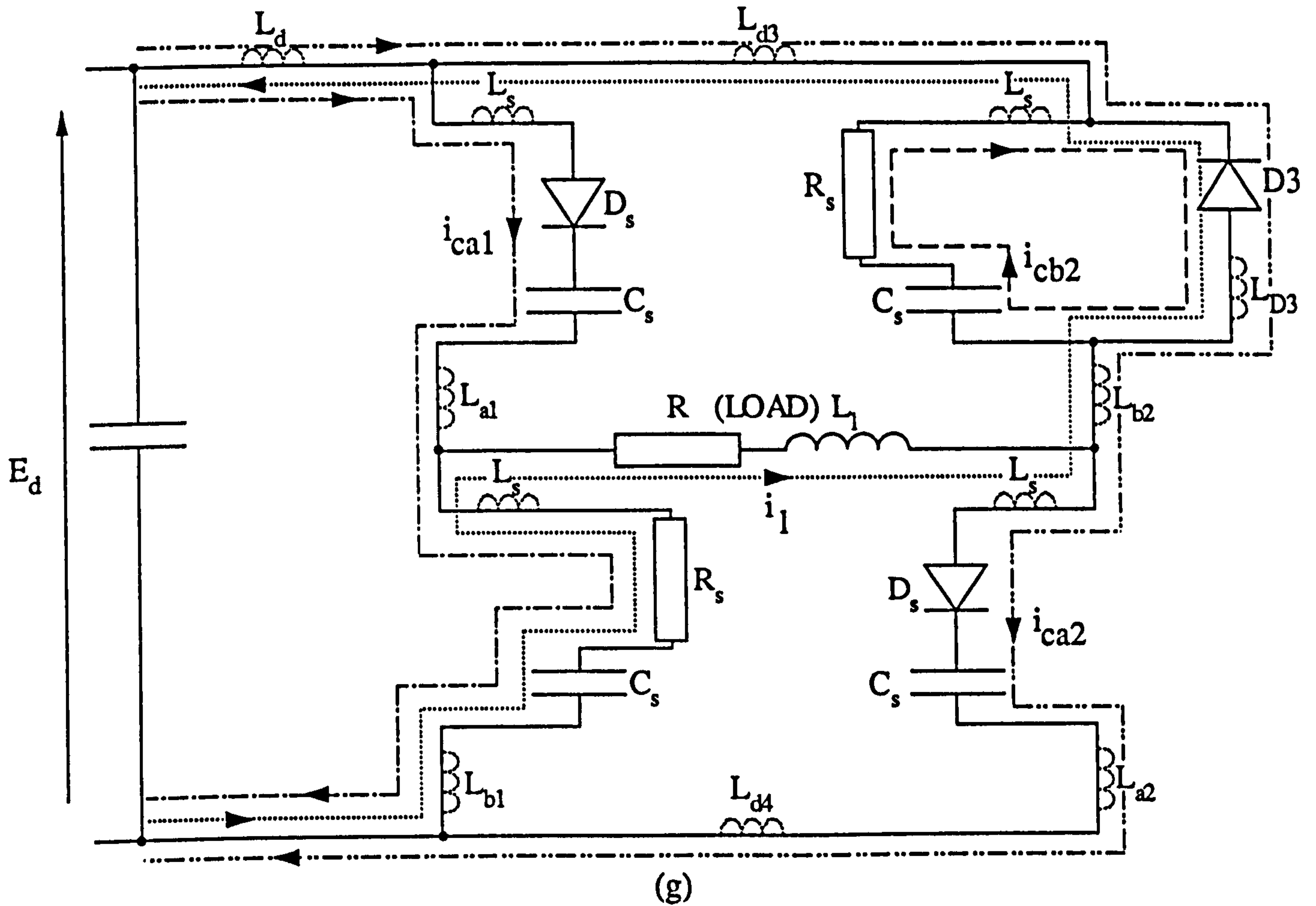
COLUMNS	(1)	(2)	(3)	(4)	(5)	(6)	(7)
$p \ i_{cb1}$	$-\frac{R_s L_{35}}{L_{24}}$						$i_{cb1}$
$p \ i_{cb2}$	$-\frac{R_s L_{29}}{L_{24}}$						$i_{cb2}$
$p \ i_1$	$\frac{R_s L_{42}}{L_{37}}$						$i_1$
$p \ v_{ca1}$	$\frac{1}{C_s}$						$v_{ca1}$
$p \ v_{ca2}$	0						$v_{ca2}$
$p \ v_{cb1}$	$\frac{1}{C_s}$						$v_{cb1}$
$p \ v_{cb2}$	0						$v_{cb2}$

(Columns 2 to 7 as in (d))

							$+$	$\frac{E_d L_{31}}{L_{24}}$
								$\frac{E_d L_{25}}{L_{24}}$
								$\frac{E_d L_{38}}{L_{37}}$
								0
								0
								0
								0

(f)

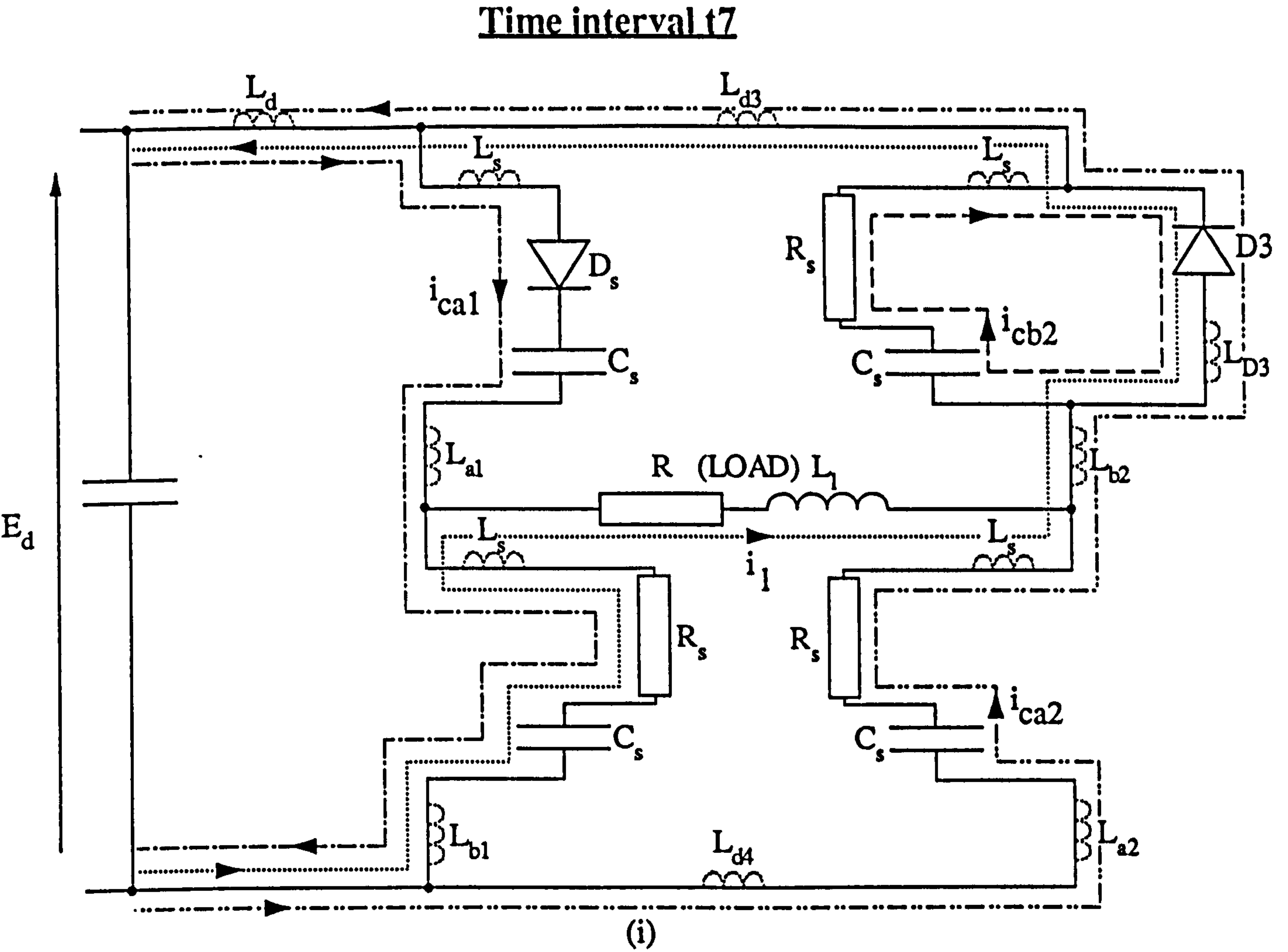
Figure 4.17 Equivalent circuits and state equations matrices at GTOs A1 and A2 turn-off together (Unbalanced turn-off).

Time interval  $t_6$ 

COLUMNS	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)		
$p i_{ca1}$	$\frac{R_s(L_{46}-L_{47})}{L_{44}}$	0	$\frac{R_s L_{50}}{L_{44}}$	$-\frac{[R_s(L_{46}-L_{47})+RL_{46}]}{L_{44}}$	$-\frac{L_{47}}{L_{44}}$	$-\frac{L_{48}}{L_{44}}$	$\frac{L_{49}}{L_{44}}$	$\frac{L_{50}}{L_{44}}$	$i_{ca1}$	$\frac{E_d L_{45}}{L_{44}}$
$p i_{ca2}$	$\frac{R_s(L_{52}-L_{53})}{L_{44}}$	0	$\frac{R_s L_{56}}{L_{44}}$	$-\frac{[R_s(L_{52}-L_{53})+RL_{52}]}{L_{44}}$	$-\frac{L_{53}}{L_{44}}$	$-\frac{L_{54}}{L_{44}}$	$\frac{L_{55}}{L_{44}}$	$\frac{L_{56}}{L_{44}}$	$i_{ca2}$	$\frac{E_d L_{51}}{L_{44}}$
$p i_{cb2}$	$\frac{R_s(L_{72}+L_{68})}{L_{65}}$	0	$\frac{R_s L_{71}}{L_{65}}$	$\frac{[R_s(L_{73}+L_{67})+RL_{67}]}{L_{65}}$	$\frac{L_{68}}{L_{65}}$	$\frac{L_{69}}{L_{65}}$	$\frac{L_{70}}{L_{65}}$	$\frac{L_{71}}{L_{65}}$	$i_{cb2}$	$\frac{E_d L_{66}}{L_{65}}$
$p i_1$	$\frac{R_s(L_{64}-L_{60})}{L_{57}}$	0	$\frac{R_s L_{63}}{L_{57}}$	$-\frac{[R_s(L_{59}-L_{60})+RL_{59}]}{L_{57}}$	$-\frac{L_{60}}{L_{57}}$	$\frac{L_{61}}{L_{57}}$	$\frac{L_{62}}{L_{57}}$	$\frac{L_{63}}{L_{57}}$	$i_1$	$\frac{E_d L_{58}}{L_{57}}$
$p v_{ca1}$	$\frac{1}{C_s}$	0	0	0	0	0	0	0	$v_{ca1}$	0
$p v_{ca2}$	0	$\frac{1}{C_s}$	0	0	0	0	0	0	$v_{ca2}$	0
$p v_{cb1}$	$\frac{1}{C_s}$	0	0	$-\frac{1}{C_s}$	0	0	0	0	$v_{cb1}$	0
$p v_{cb2}$	0	0	$\frac{1}{C_s}$	0	0	0	0	0	$v_{cb2}$	0

(h)

Figure 4.17 Equivalent circuits and state equations matrices at GTOs A1 and A2 turn-off together (Unbalanced turn-off).



COLUMNS	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	
$p\ i_{ca1}$		$-\frac{R_s L_{48}}{L_{44}}$						$i_{ca1}$	$\frac{E_d L_{45}}{L_{44}}$
$p\ i_{ca2}$		$-\frac{R_s L_{54}}{L_{44}}$						$i_{ca2}$	$\frac{E_d L_{51}}{L_{44}}$
$p\ i_{cb2}$		$\frac{R_s L_{69}}{L_{65}}$						$i_{cb2}$	$\frac{E_d L_{66}}{L_{65}}$
$p\ i_1$		$-\frac{R_s L_{61}}{L_{57}}$						$i_1$	$\frac{E_d L_{58}}{L_{57}}$
$p\ v_{ca1}$		0						$v_{ca1}$	0
$p\ v_{ca2}$		$\frac{1}{C_s}$						$v_{ca2}$	0
$p\ v_{cb1}$		0						$v_{cb1}$	0
$p\ v_{cb2}$		0						$v_{cb2}$	0

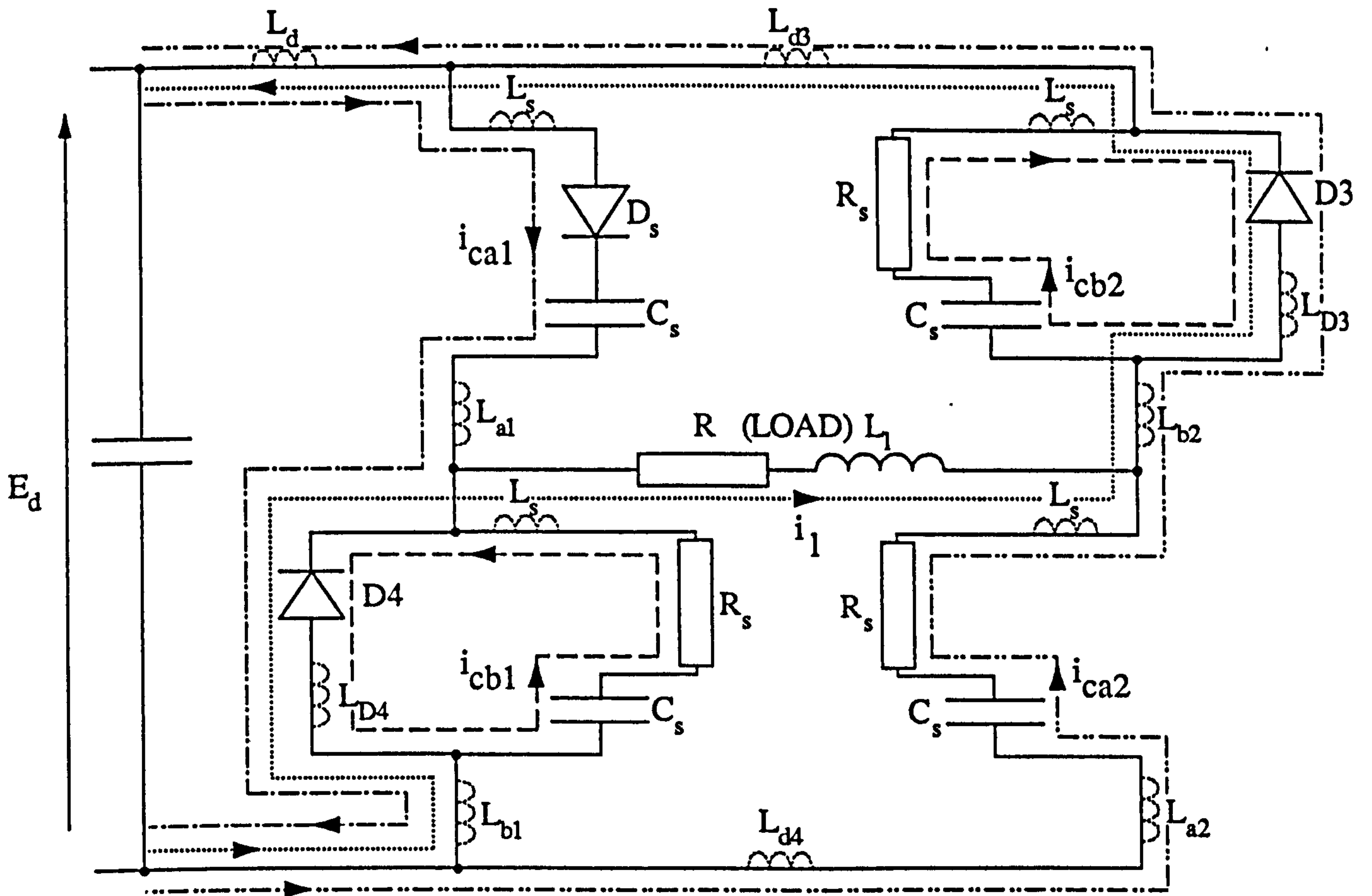
(Columns 1, and 3 to 8 as in (h))

(j)

Figure 4.17 Equivalent circuits and state equations matrices at GTOs A1 and A2 turn-off together (Unbalanced turn-off).



Time interval t8



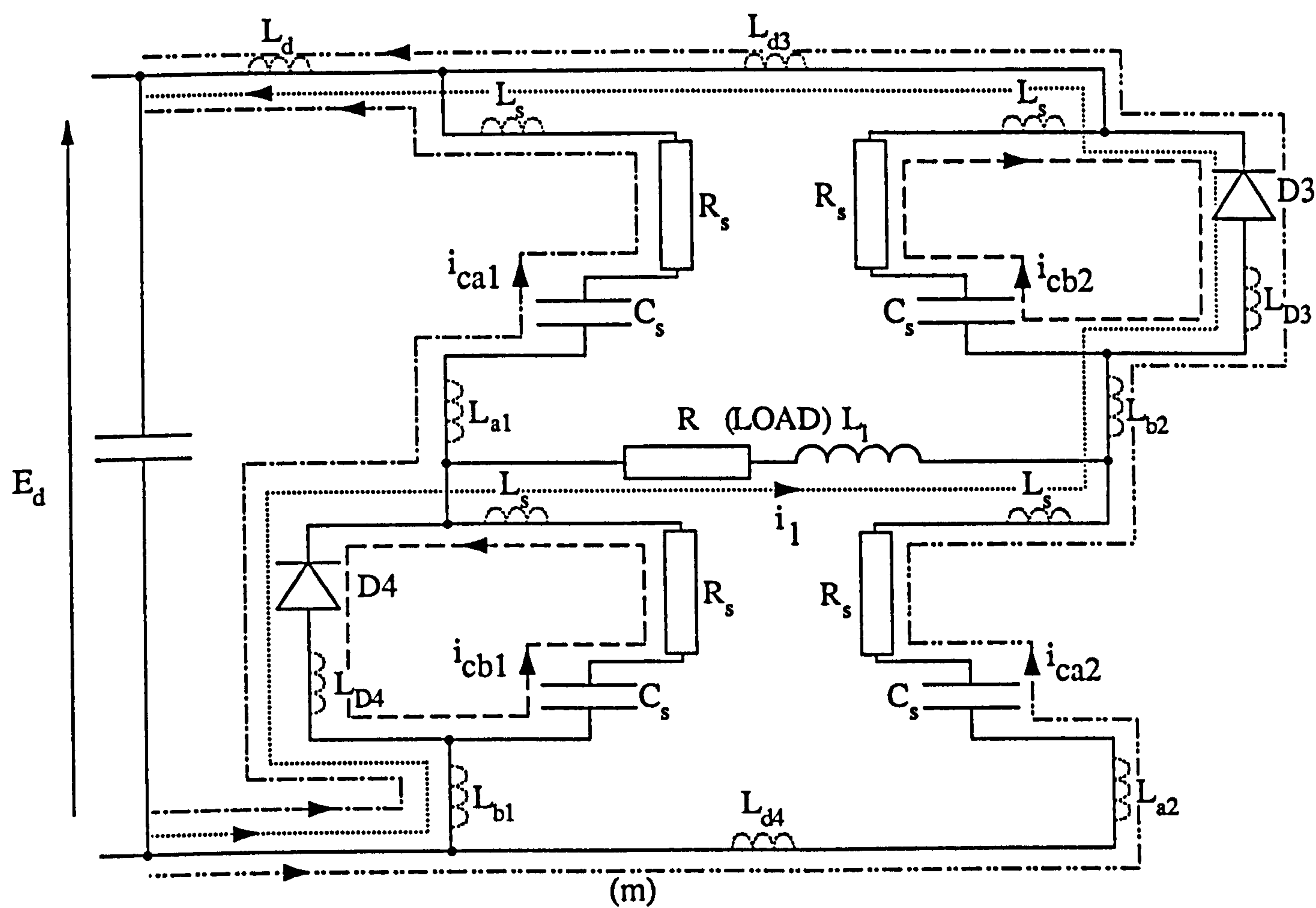
(k)

COLUMNS		(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)		
$p i_{ca1}$		0	$-\frac{R_s L_{78}}{L_{74}}$	$\frac{R_s L_{79}}{L_{74}}$	$\frac{R_s L_{80}}{L_{74}}$	$-\frac{R L_{76}}{L_{74}}$	$-\frac{L_{77}}{L_{74}}$	$-\frac{L_{78}}{L_{74}}$	$\frac{L_{79}}{L_{74}}$	$\frac{L_{80}}{L_{74}}$	$i_{ca1}$	$\frac{E_d L_{75}}{L_{74}}$
$p i_{ca2}$		0	$-\frac{R_s L_{84}}{L_{74}}$	$\frac{R_s L_{85}}{L_{74}}$	$\frac{R_s L_{86}}{L_{74}}$	$-\frac{R L_{82}}{L_{74}}$	$-\frac{L_{83}}{L_{74}}$	$-\frac{L_{84}}{L_{74}}$	$\frac{L_{85}}{L_{74}}$	$\frac{L_{86}}{L_{74}}$	$i_{ca2}$	$\frac{E_d L_{81}}{L_{74}}$
$p i_{cb1}$		0	$\frac{R_s L_{104}}{L_{94}}$	$\frac{R_s L_{105}}{L_{94}}$	$\frac{R_s L_{106}}{L_{94}}$	$\frac{R L_{102}}{L_{94}}$	$\frac{L_{103}}{L_{94}}$	$\frac{L_{104}}{L_{94}}$	$\frac{L_{105}}{L_{94}}$	$\frac{L_{106}}{L_{94}}$	$i_{cb1}$	$\frac{E_d L_{101}}{L_{94}}$
$p i_{cb2}$		0	$\frac{R_s L_{98}}{L_{94}}$	$\frac{R_s L_{99}}{L_{94}}$	$\frac{R_s L_{100}}{L_{94}}$	$\frac{R L_{96}}{L_{94}}$	$\frac{L_{97}}{L_{94}}$	$\frac{L_{98}}{L_{94}}$	$\frac{L_{99}}{L_{94}}$	$\frac{L_{100}}{L_{94}}$	$i_{cb2}$	$\frac{E_d L_{95}}{L_{94}}$
$p i_1$	=	0	$-\frac{R_s L_{91}}{L_{87}}$	$\frac{R_s L_{92}}{L_{87}}$	$\frac{R_s L_{93}}{L_{87}}$	$-\frac{R L_{89}}{L_{87}}$	$-\frac{L_{90}}{L_{87}}$	$-\frac{L_{91}}{L_{87}}$	$\frac{L_{92}}{L_{87}}$	$\frac{L_{93}}{L_{87}}$	$i_1$	$\frac{E_d L_{88}}{L_{87}}$
$p v_{ca1}$		$\frac{1}{C_s}$	0	0	0	0	0	0	0	0	$v_{ca1}$	0
$p v_{ca2}$		0	$\frac{1}{C_s}$	0	0	0	0	0	0	0	$v_{ca2}$	0
$p v_{cb1}$		0	0	$\frac{1}{C_s}$	0	0	0	0	0	0	$v_{cb1}$	0
$p v_{cb2}$		0	0	0	$\frac{1}{C_s}$	0	0	0	0	0	$v_{cb2}$	0

(l)

Figure 4.17 Equivalent circuits and state equations matrices at GTOs A1 and A2 turn-off together (Unbalanced turn-off).

Time interval t9



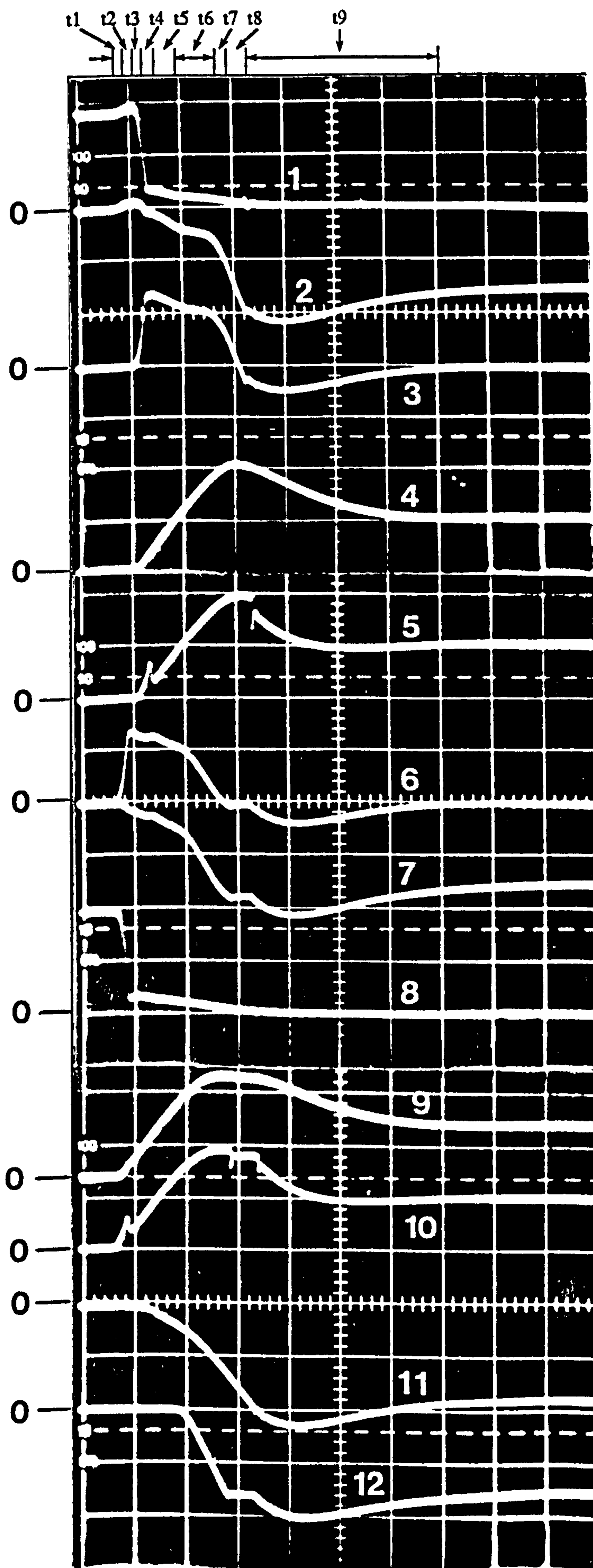
COLUMNS

$p i_{ca1}$	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	$i_{ca1}$	$\frac{E_d L_{75}}{L_{74}}$
$p i_{ca2}$	$-\frac{R_s L_{83}}{L_{74}}$									$i_{ca2}$	$\frac{E_d L_{81}}{L_{74}}$
$p i_{cb1}$	$\frac{R_s L_{103}}{L_{94}}$									$i_{cb1}$	$\frac{E_d L_{101}}{L_{94}}$
$p i_{cb2}$	$\frac{R_s L_{97}}{L_{94}}$									$i_{cb2}$	$\frac{E_d L_{95}}{L_{94}}$
$p i_1$	$-\frac{R_s L_{90}}{L_{87}}$									$i_1$	$+\frac{E_d L_{88}}{L_{87}}$
$p v_{ca1}$	$\frac{1}{C_s}$									$v_{ca1}$	0
$p v_{ca2}$	0									$v_{ca2}$	0
$p v_{cb1}$	0									$v_{cb1}$	0
$p v_{cb2}$	0									$v_{cb2}$	0

(Columns 2 to 9 as in (l))

(n)

Figure 4.17 Equivalent circuits and state equations matrices at GTOs A1 and A2 turn-off together (Unbalanced turn-off).



- (1) A1 Anode Current (50A/div.)
- (2) B1 Branch Current (50A/div.)
- (3) A1 Snubber Current (50A/div.)
- (4) A1 Snubber Capacitor Voltage (200V/div.)
- (5) A1 A-K Voltage (200V/div.)
- (6) A2 Snubber Current (50A/div.)
- (7) B2 Branch Current (50A/div.)
- (8) A2 Anode Current (50A/div.)
- (9) A2 Snubber Capacitor Voltage (200V/div.)
- (10) A2 A-K Voltage (200V/div.)
- (11) Supply Current (100A/div.)
- (12) Diode D3 Current (50A/div.)

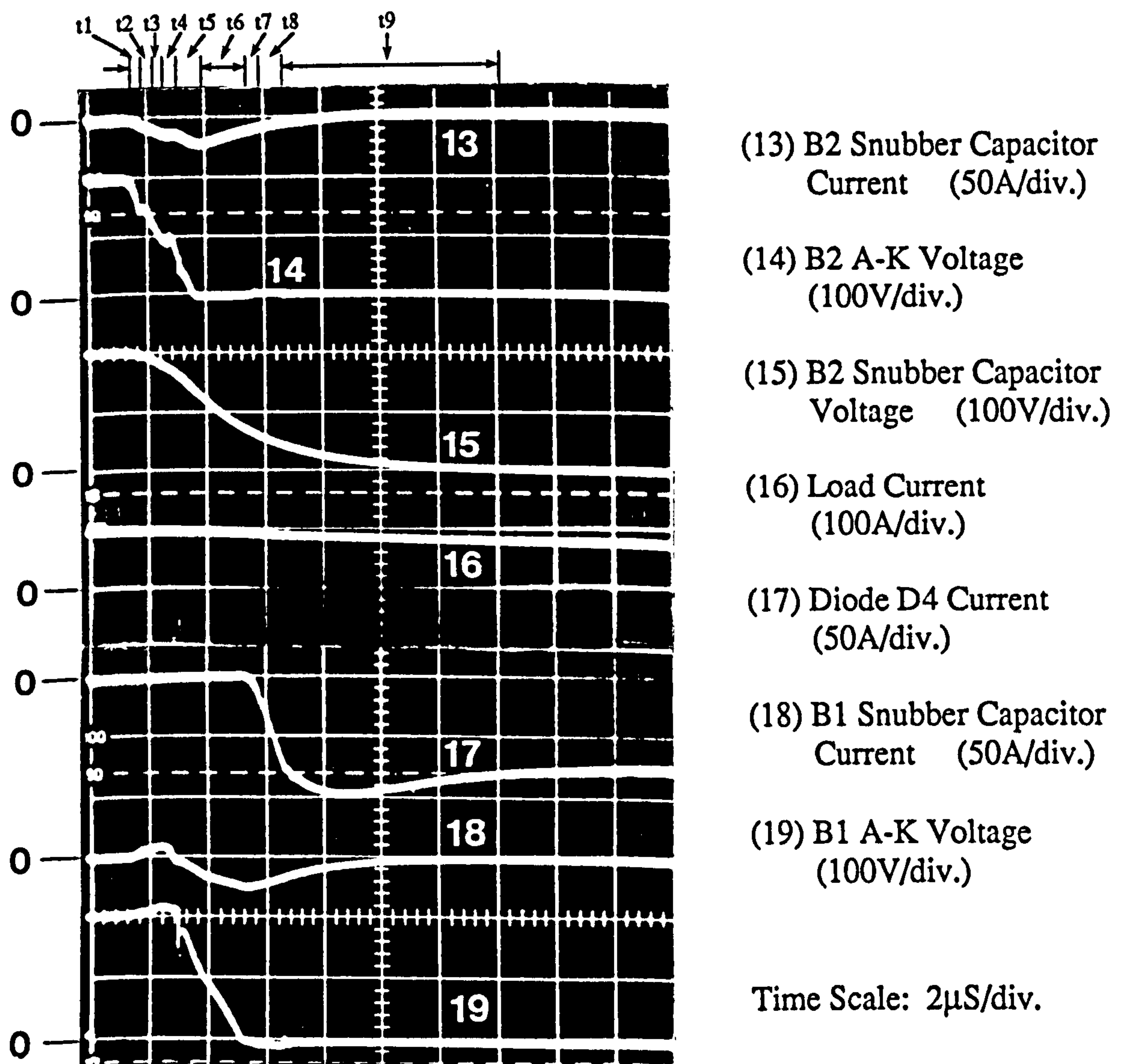
Time Scale: 2 $\mu$ S/div.

(a) Experimental Results

Figure 4.18 Waveforms at GTOs A1 and A2 turn-off together (unbalanced)

CONTINUED





(a) Experimental Results

Figure 4.18 Waveforms at GTOs A1 and A2 turn-off together (unbalanced)



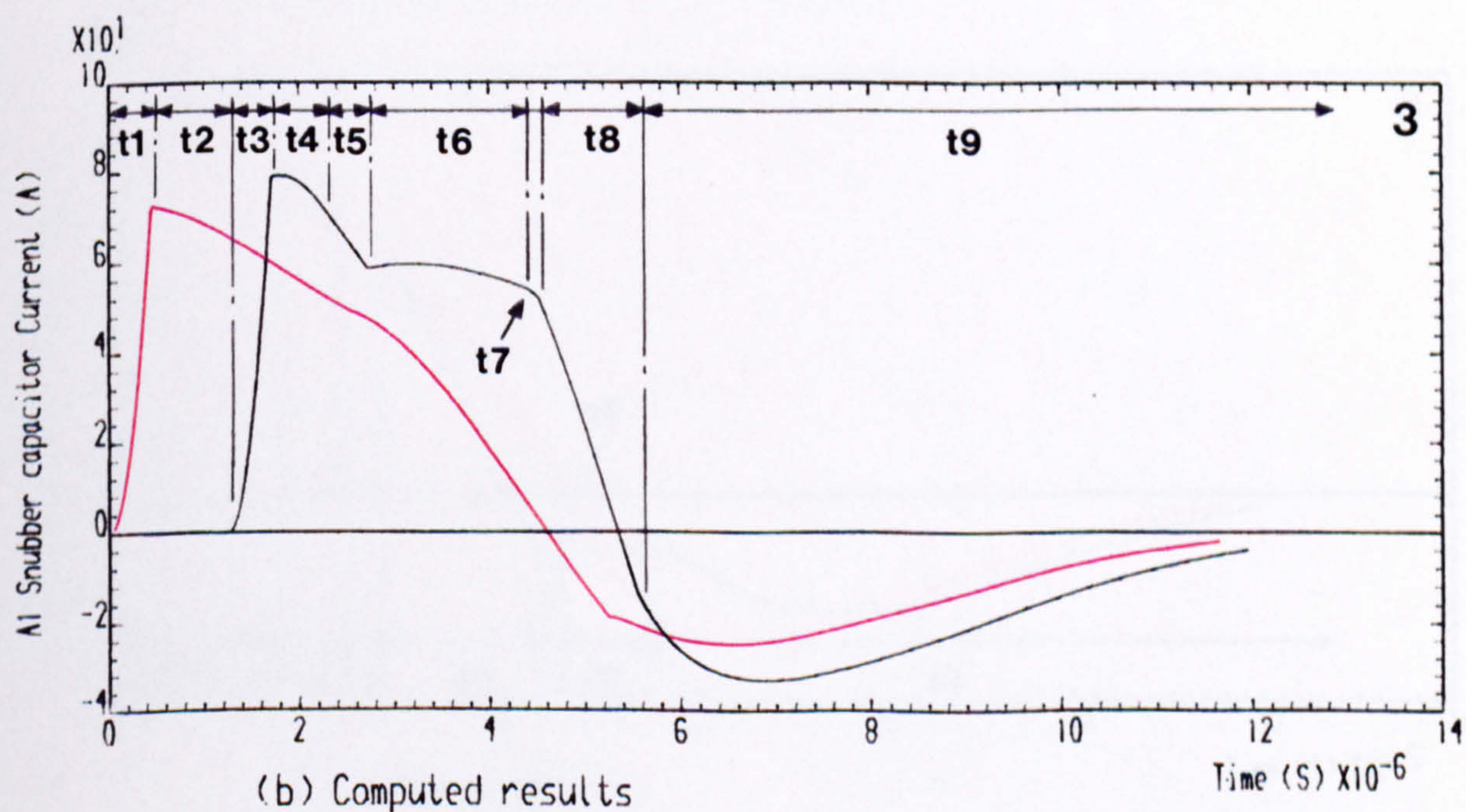
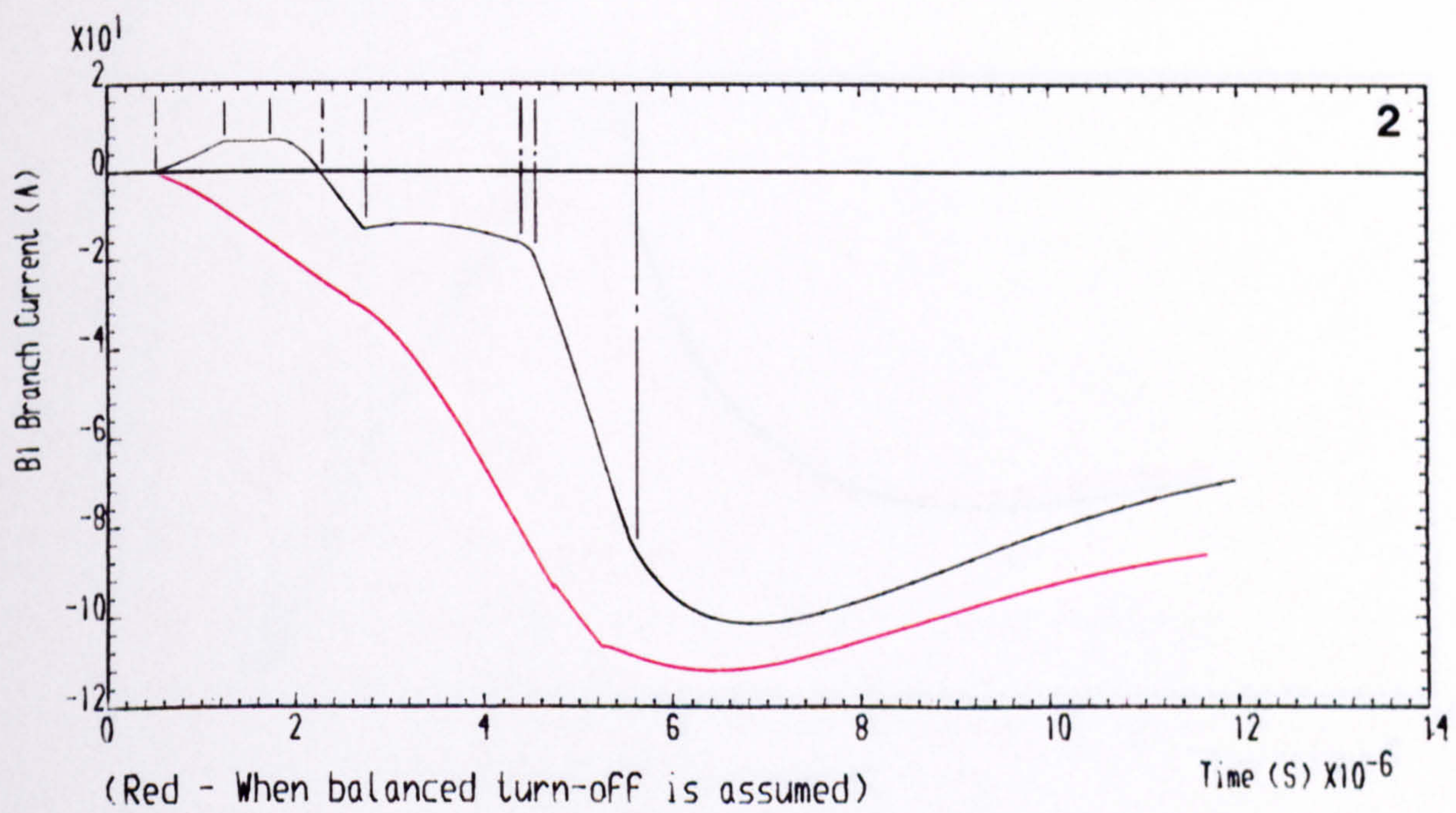
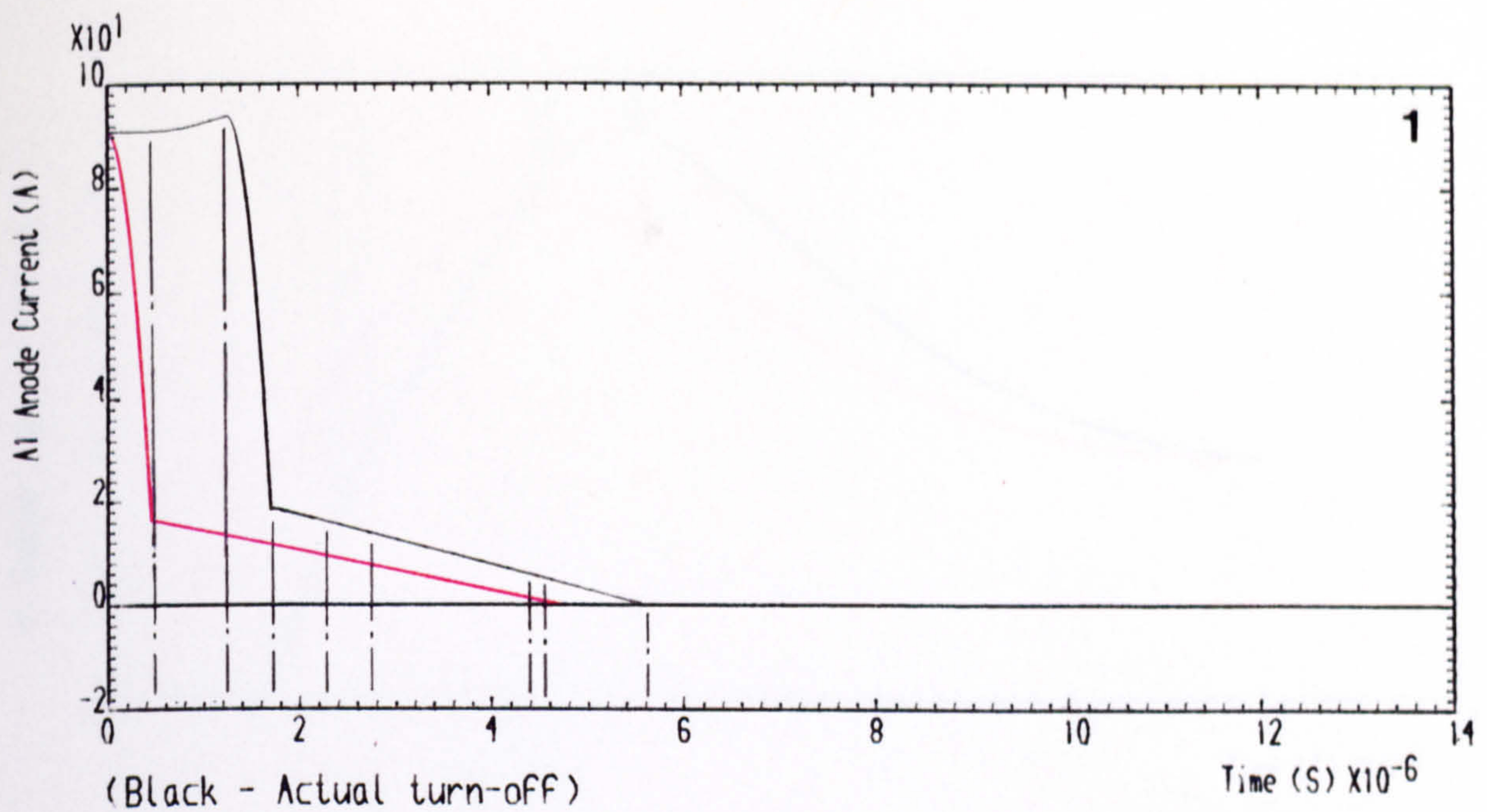


Figure 4.18 Waveforms at GTOs A1 and A2 turn-off together (unbalanced)

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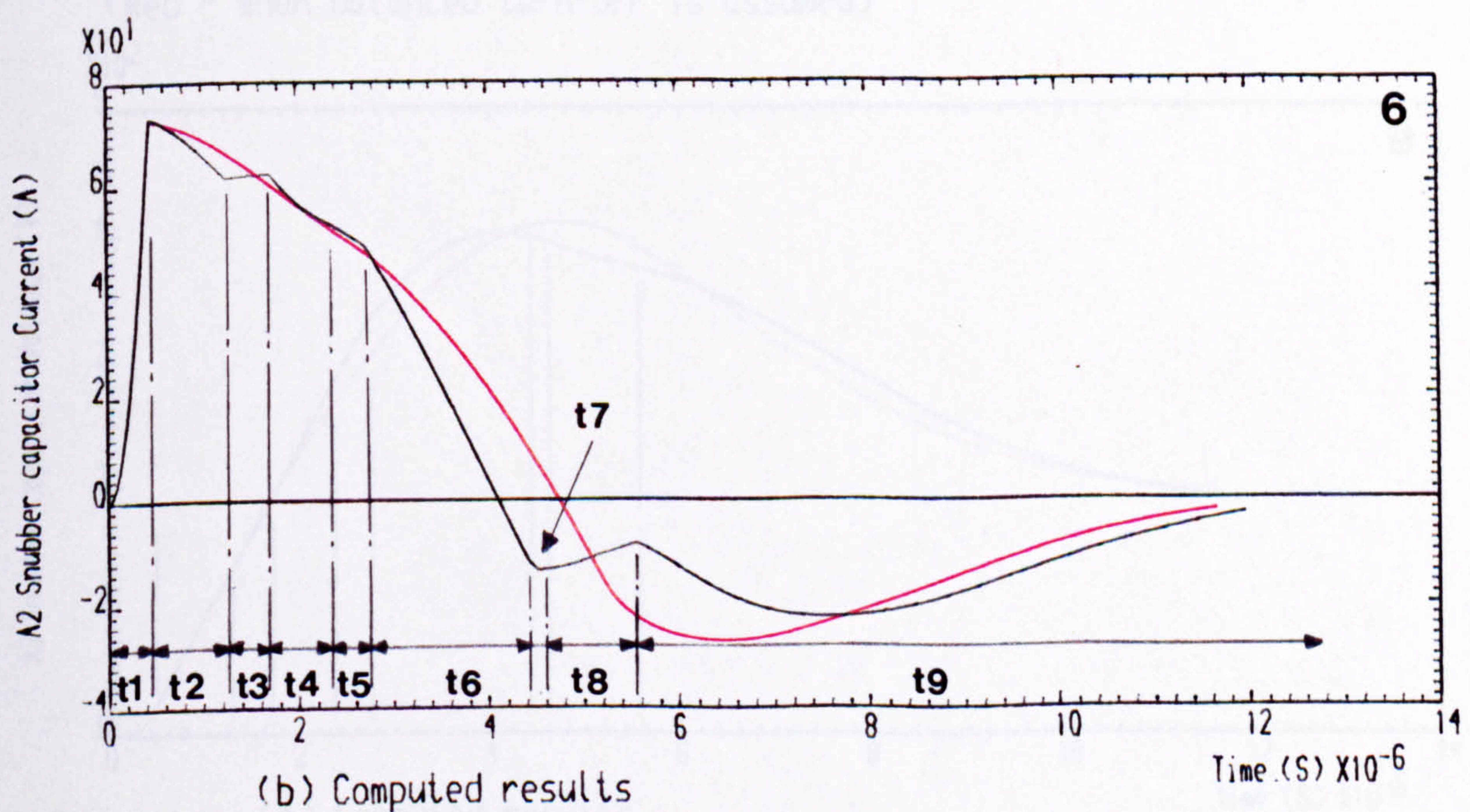
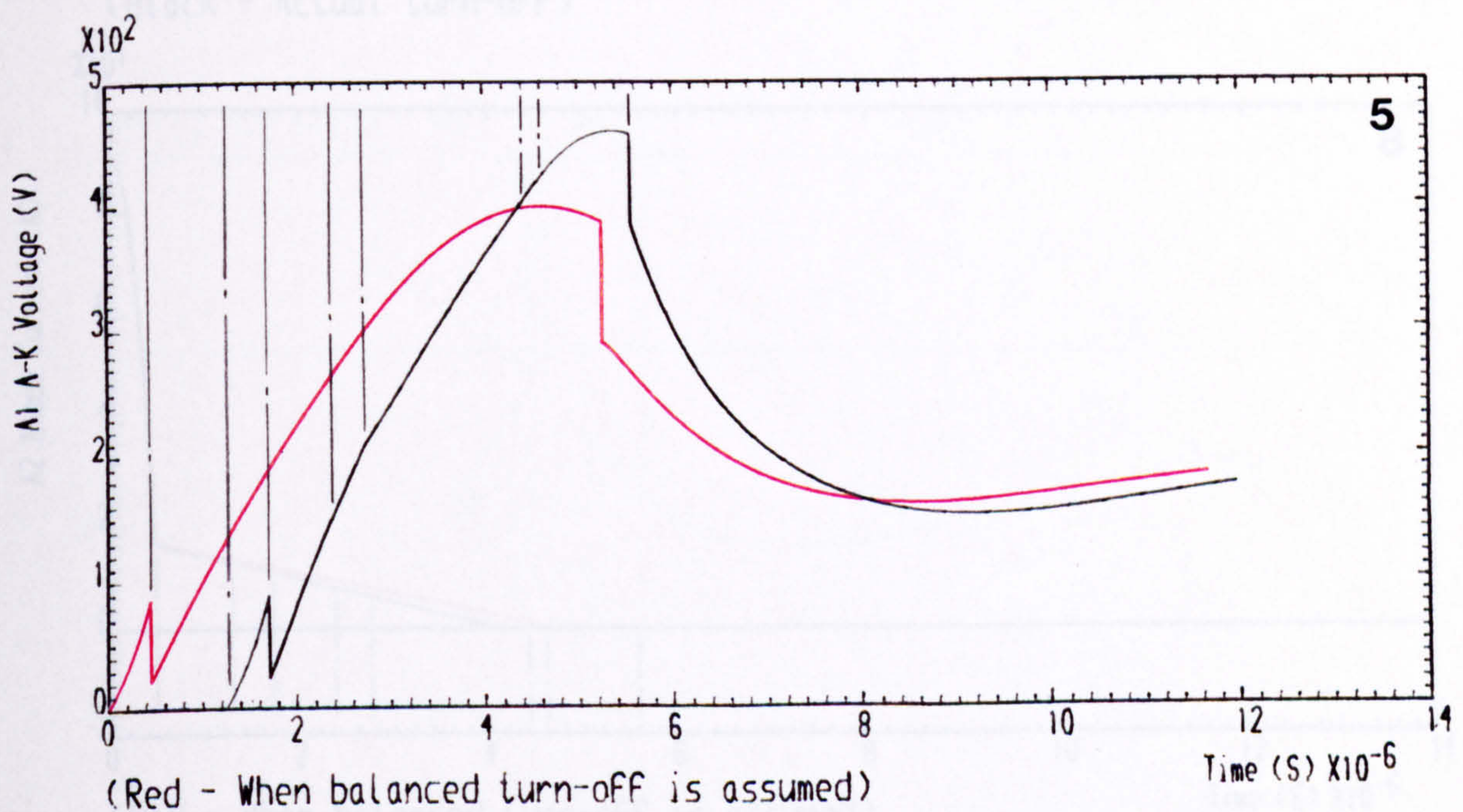
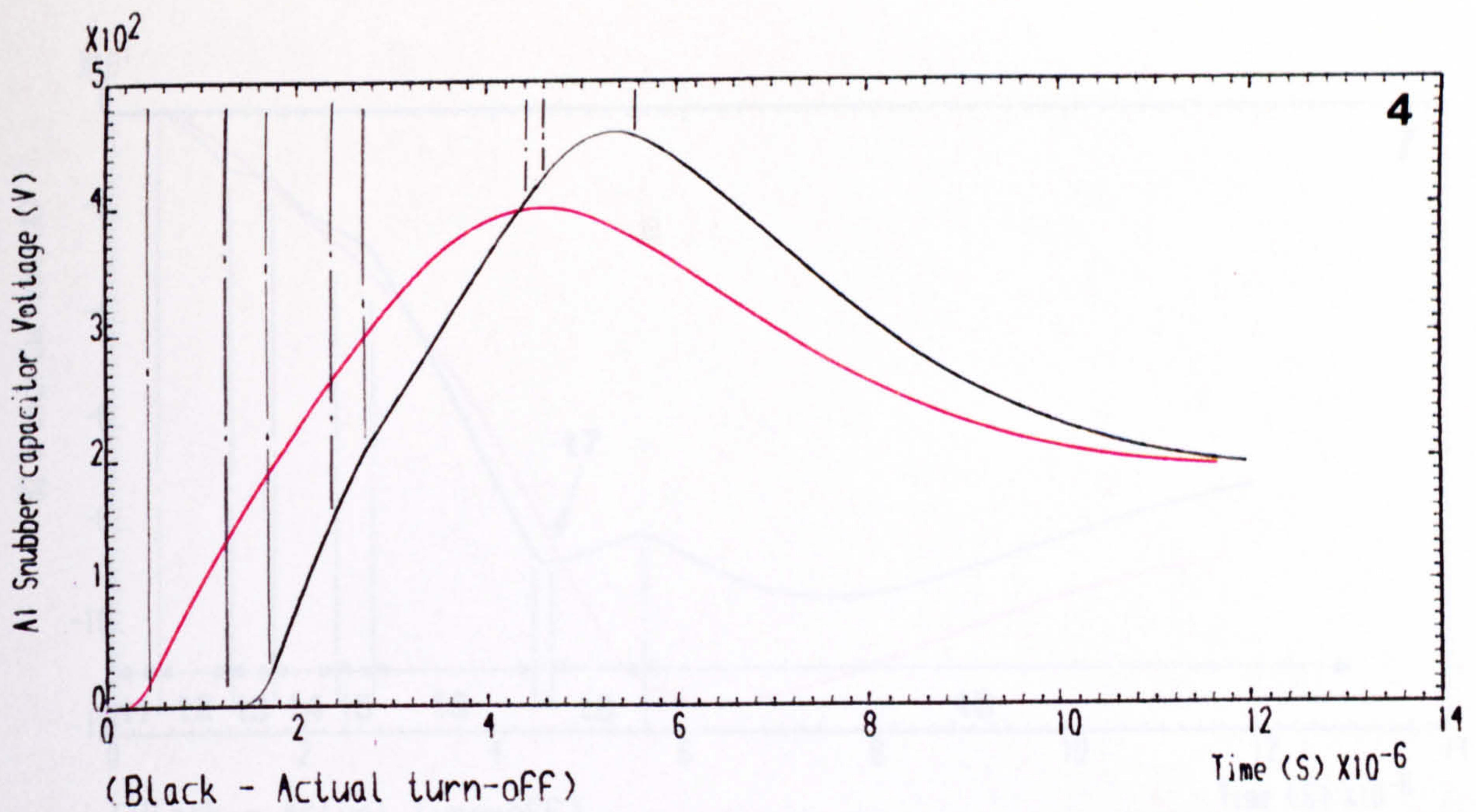


Figure 4.18 Waveforms at GTOs A1 and A2 turn-off together (unbalanced)

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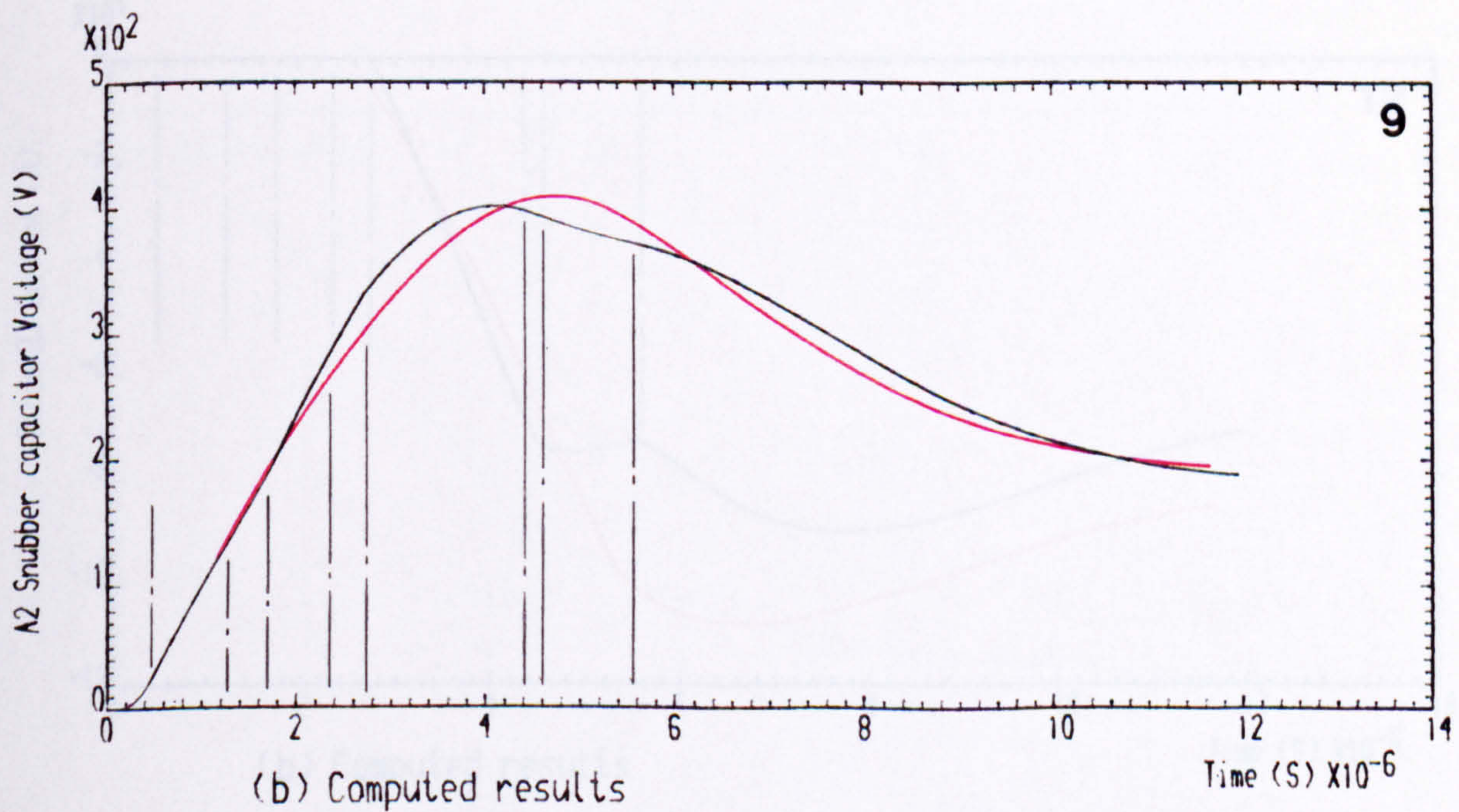
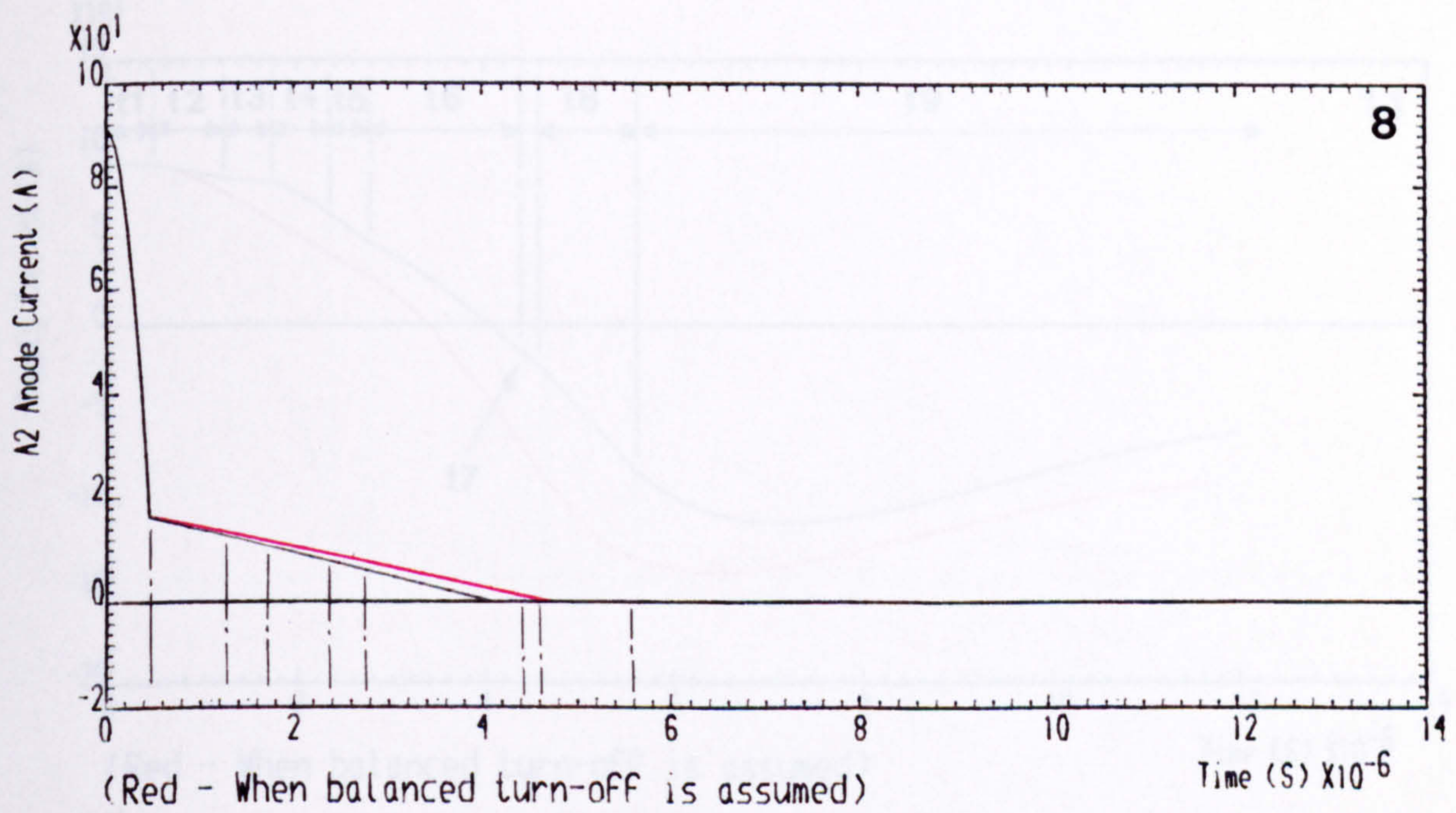
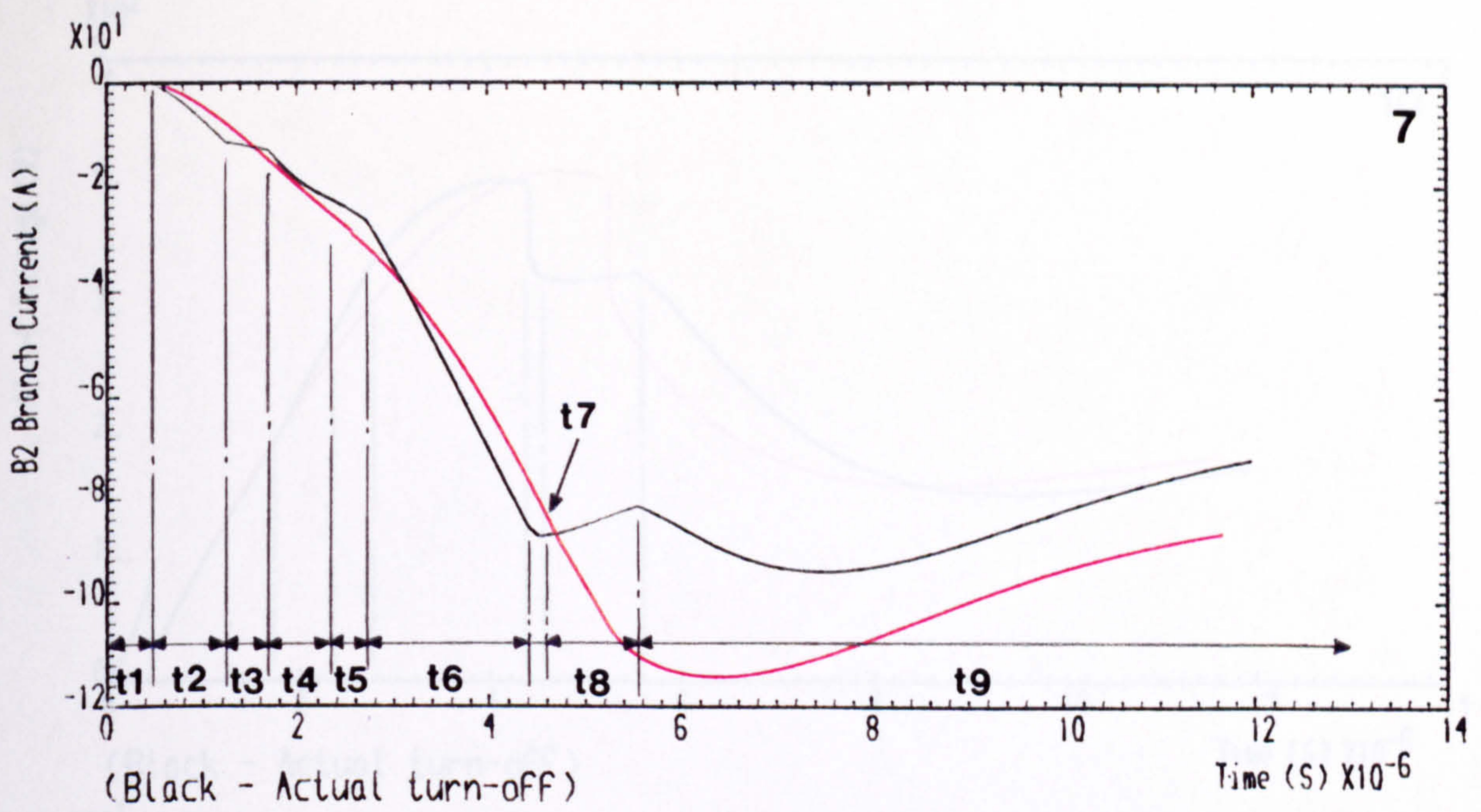


Figure 4.18 Waveforms at GTOs A1 and A2 turn-off together (unbalanced)

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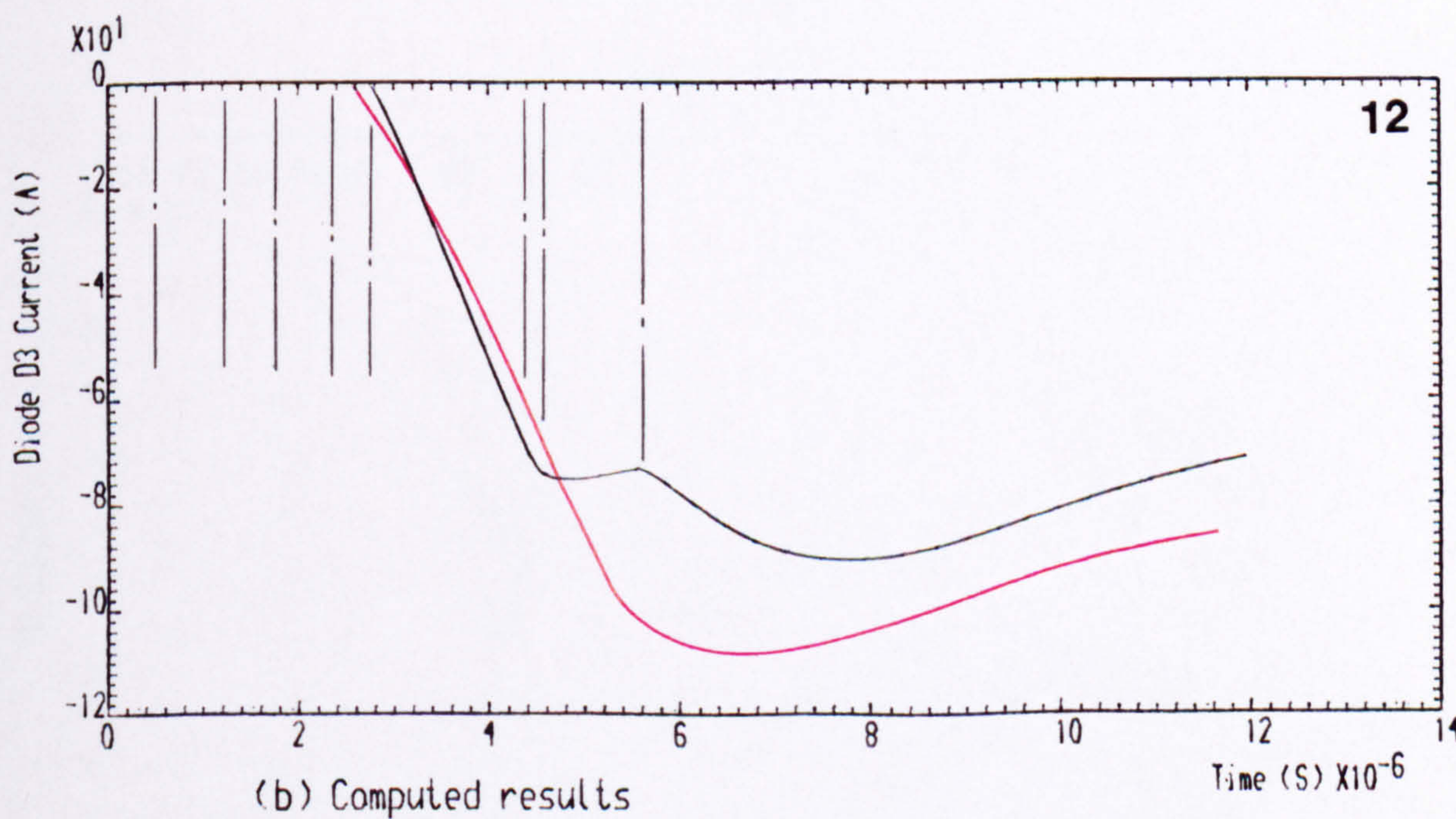
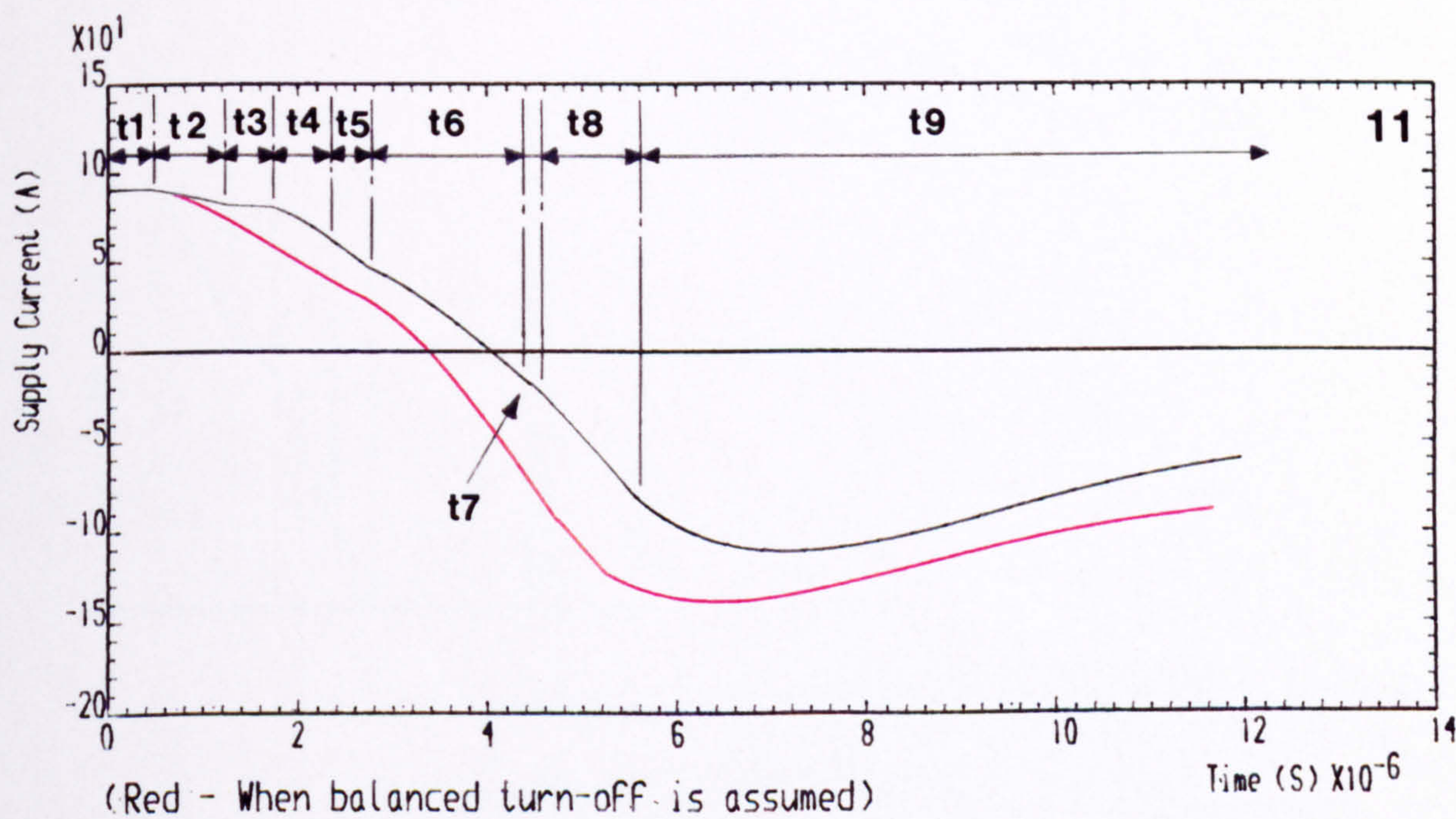
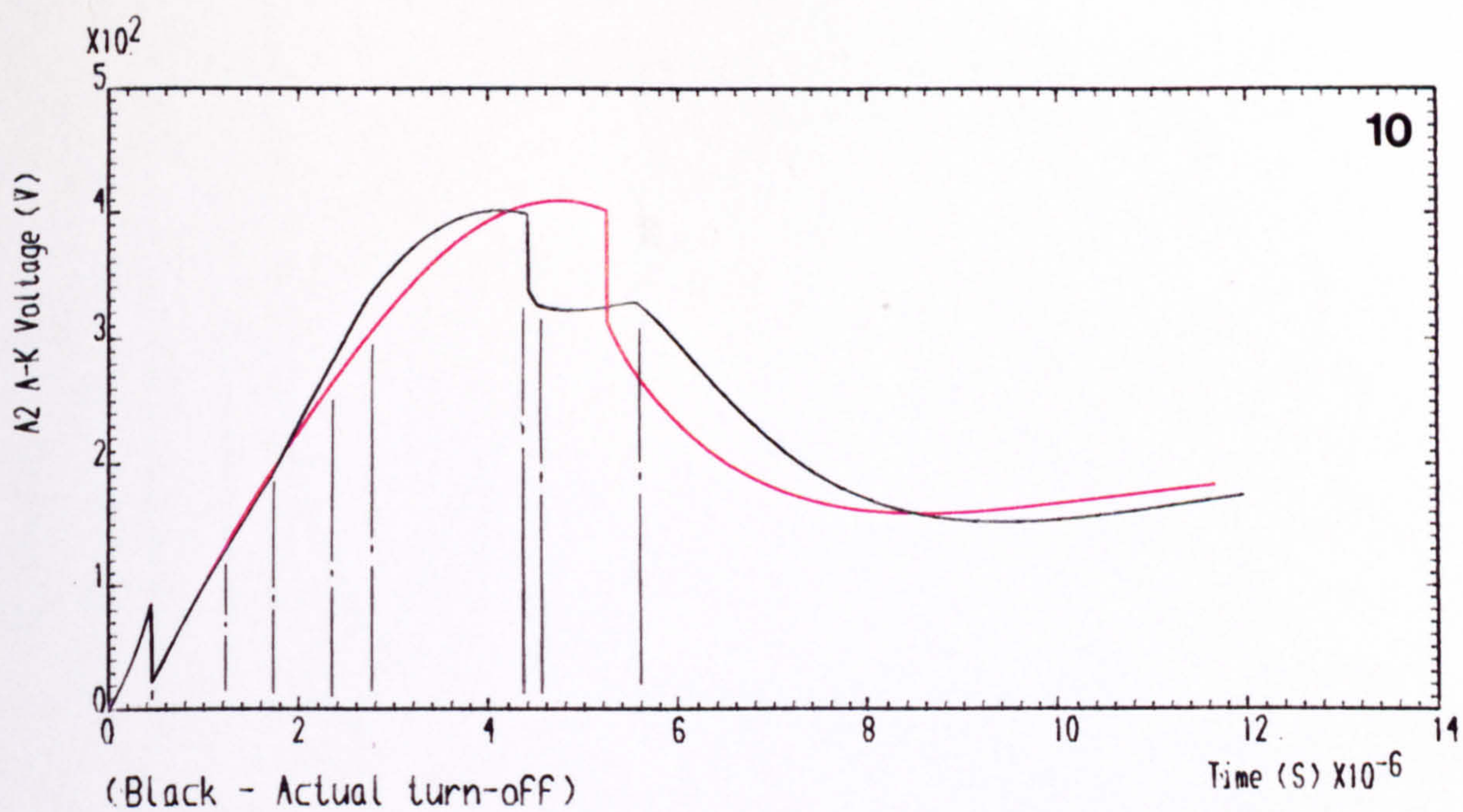


Figure 4.18 Waveforms at GTOs A1 and A2 turn-off together (unbalanced)

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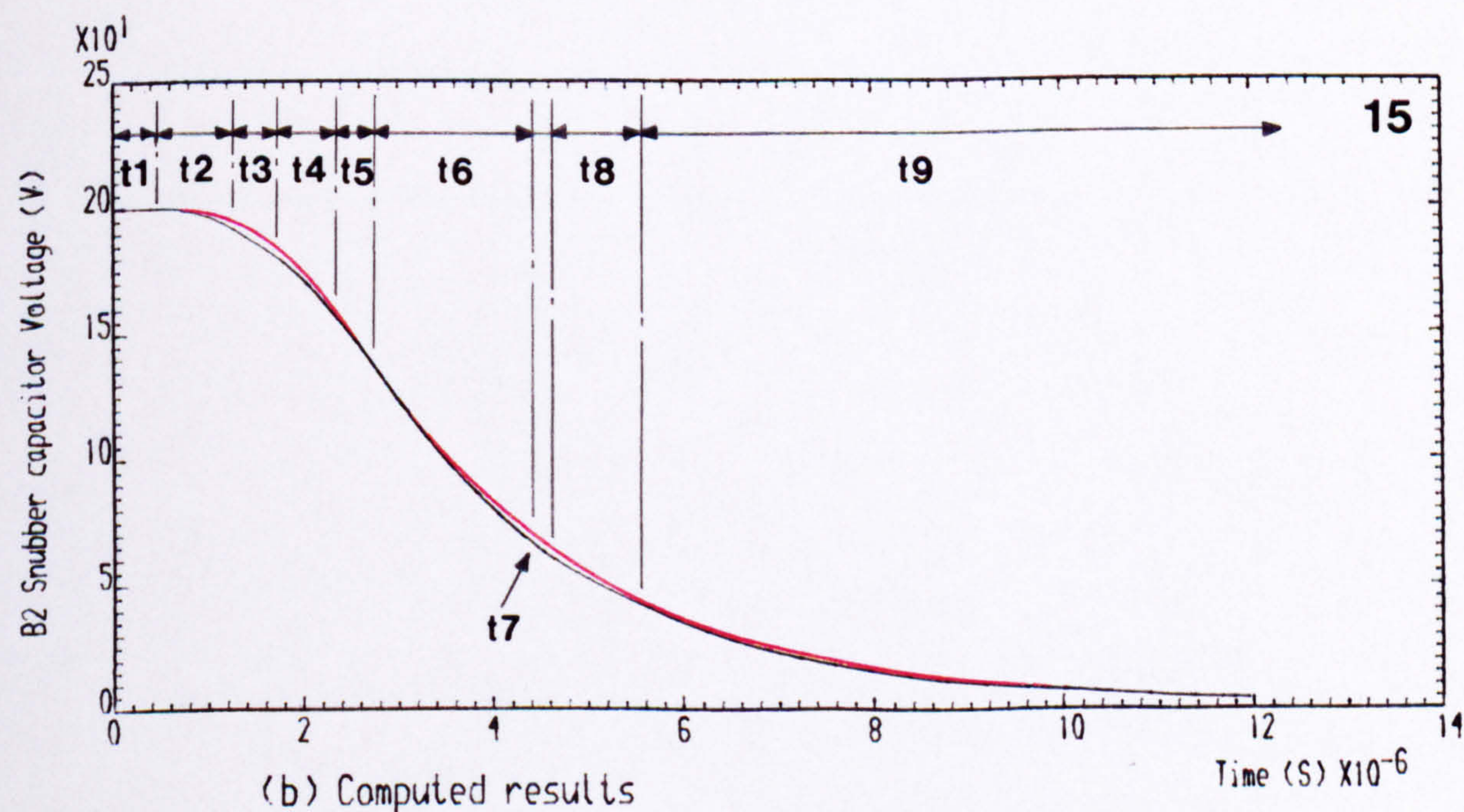
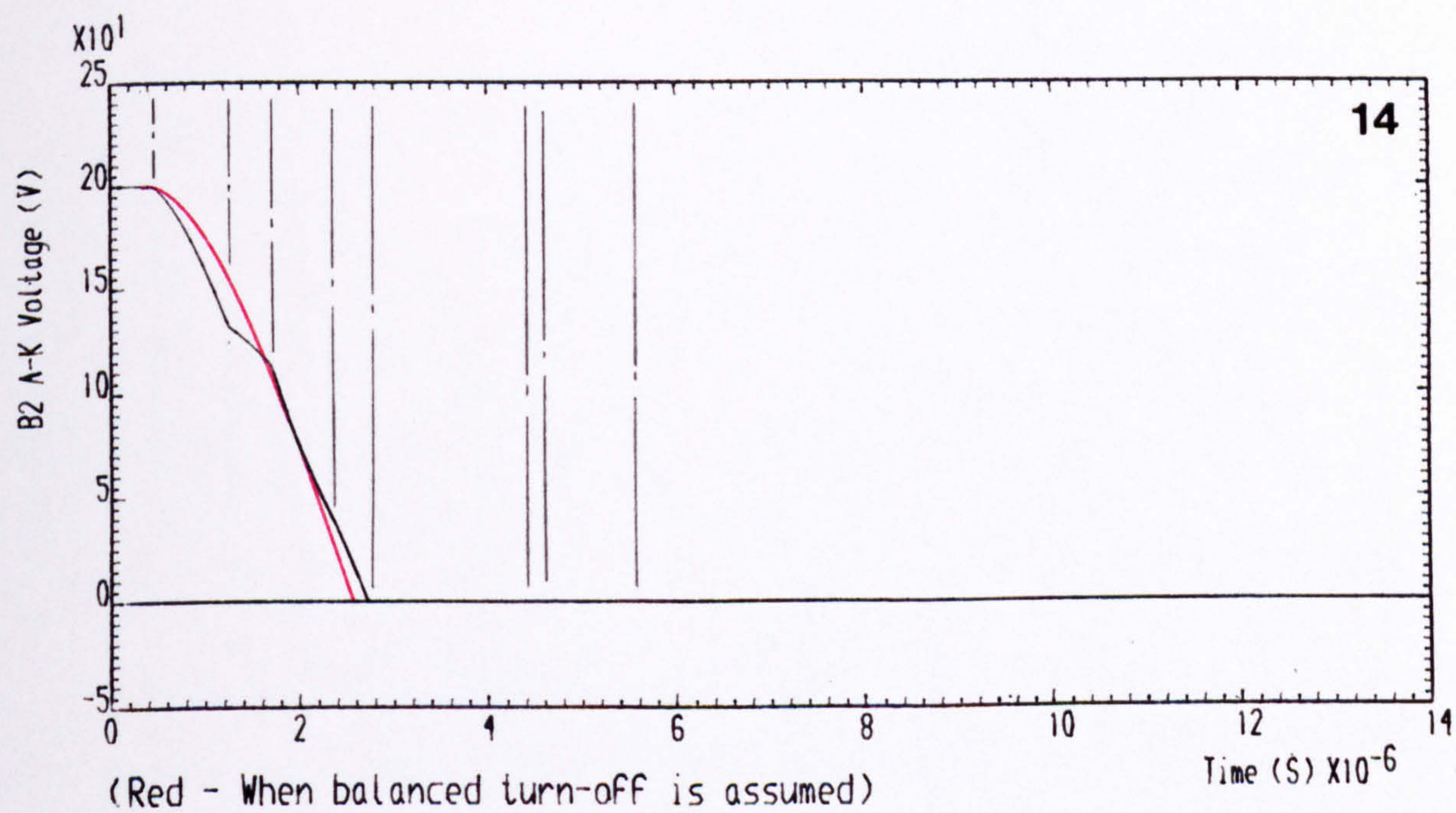
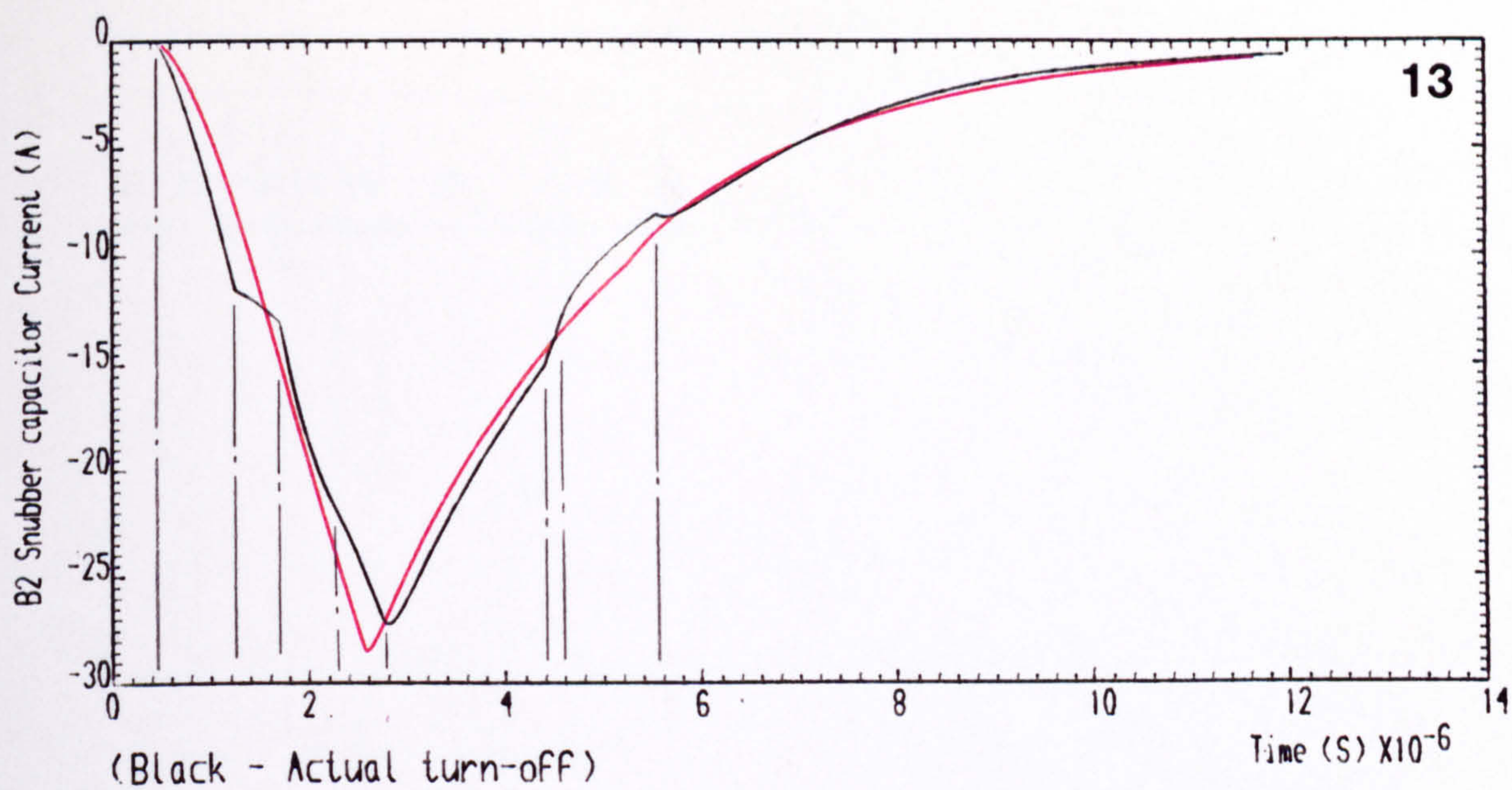


Figure 4.18 Waveforms at GTOs A1 and A2 turn-off together (unbalanced)

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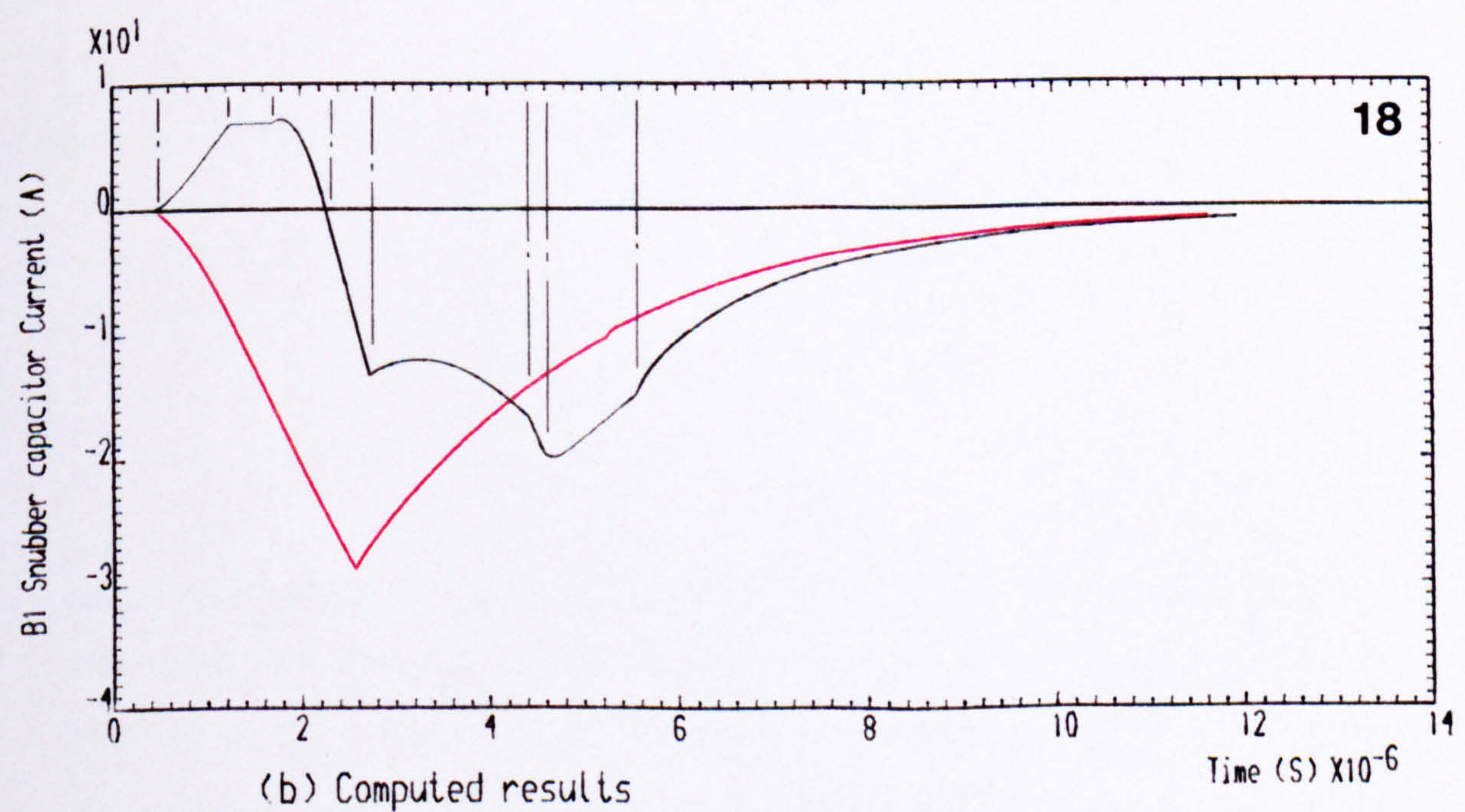
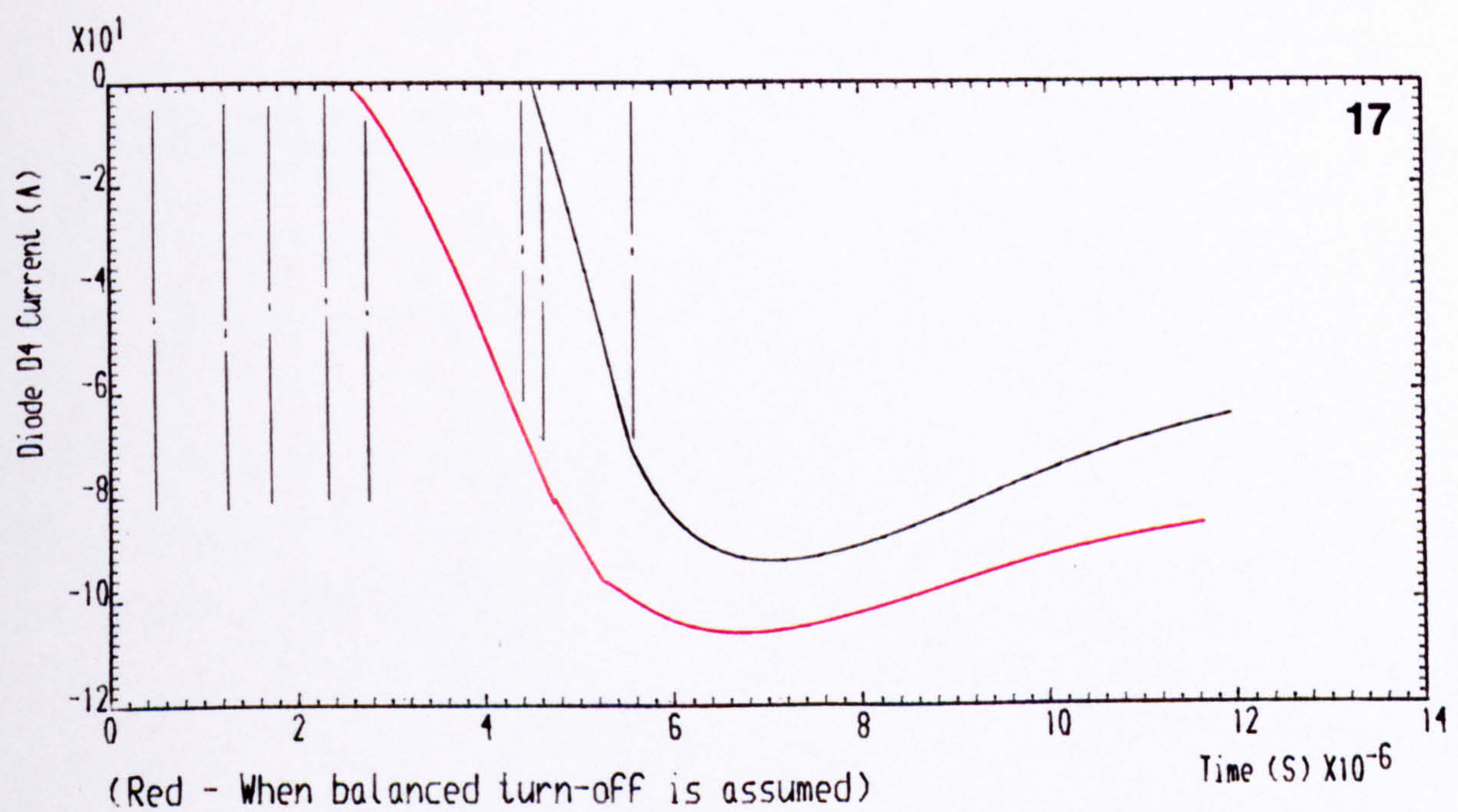
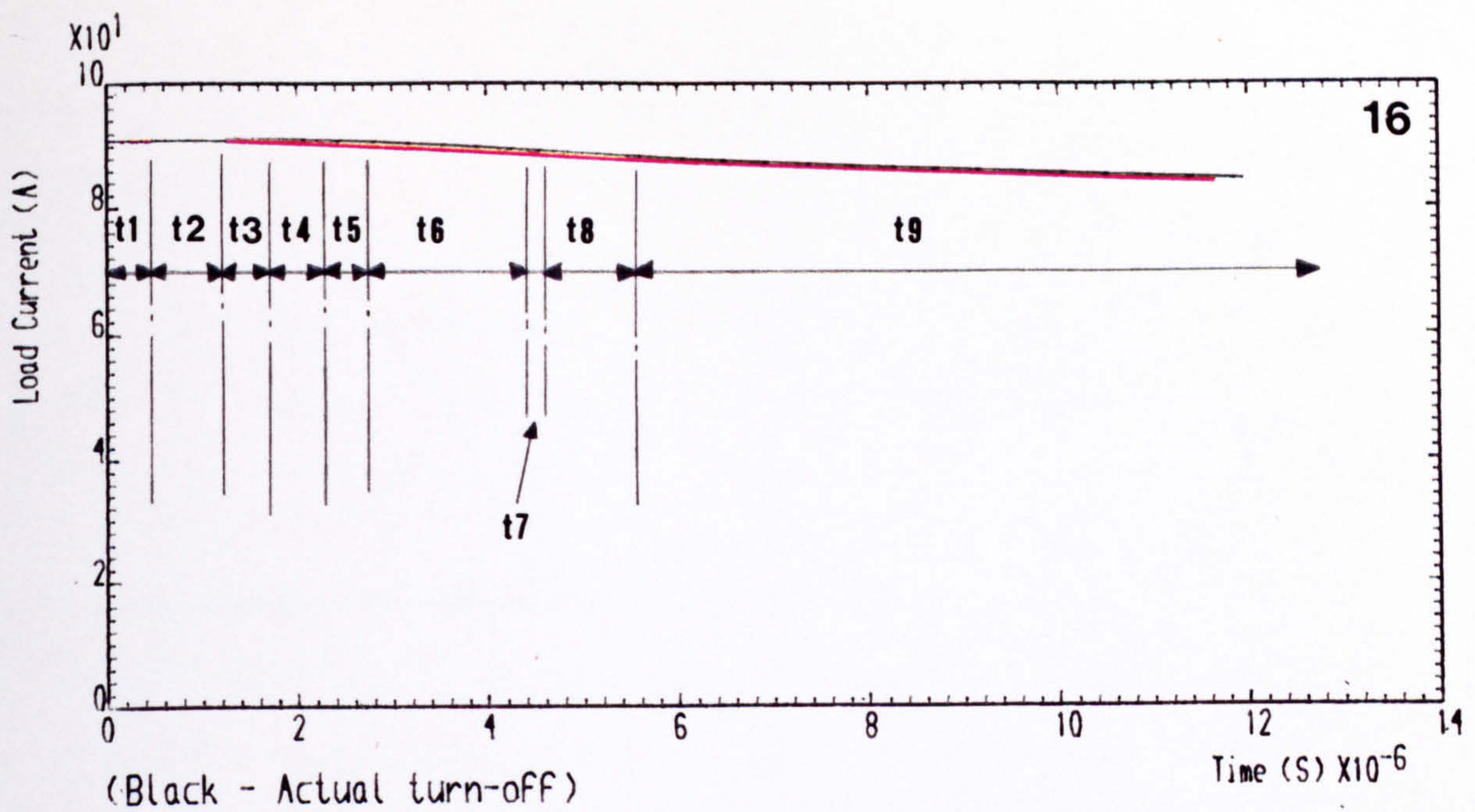


Figure 4.18 Waveforms at GTOs A1 and A2 turn-off together (unbalanced)

CONTINUED ..



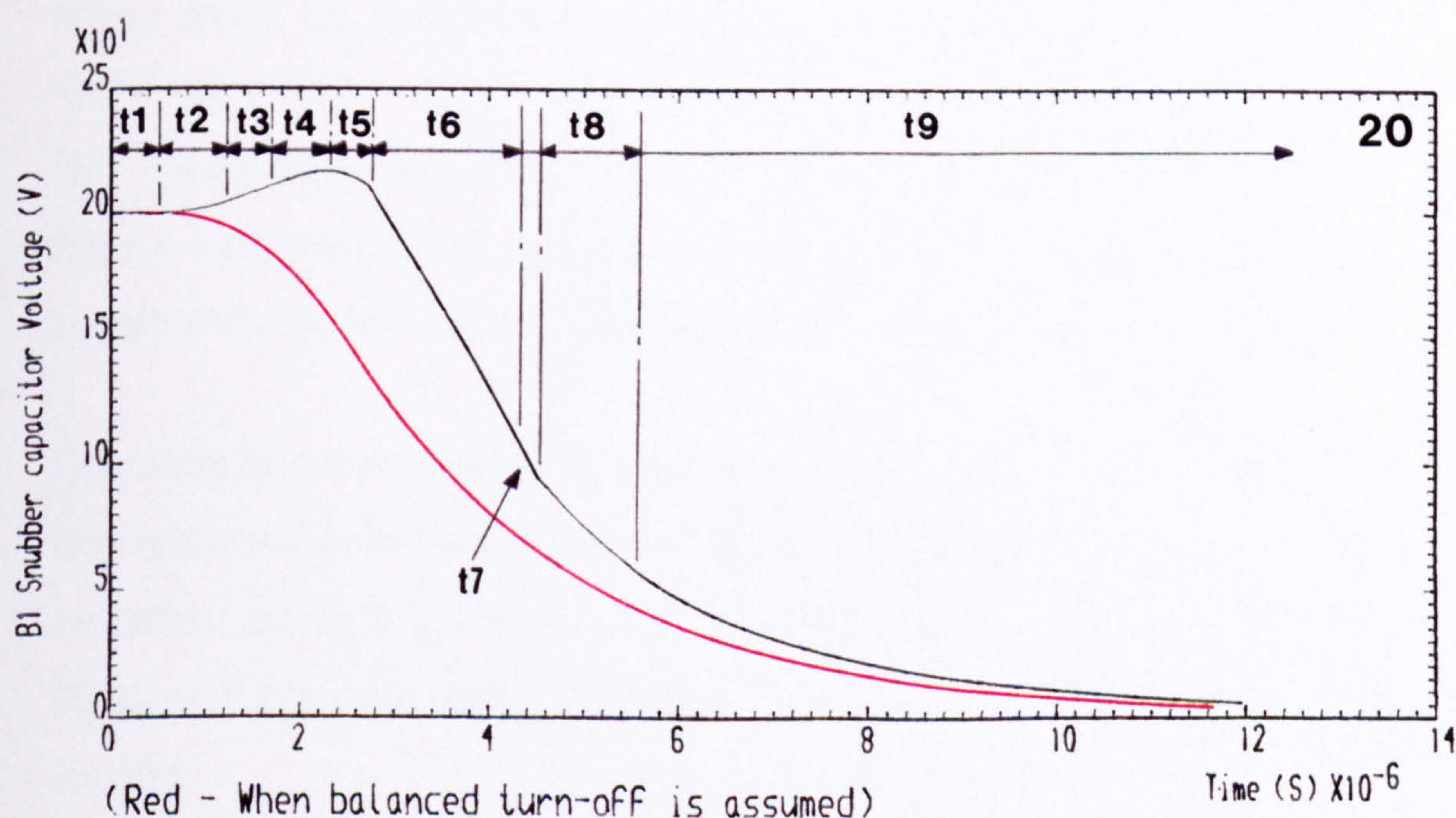
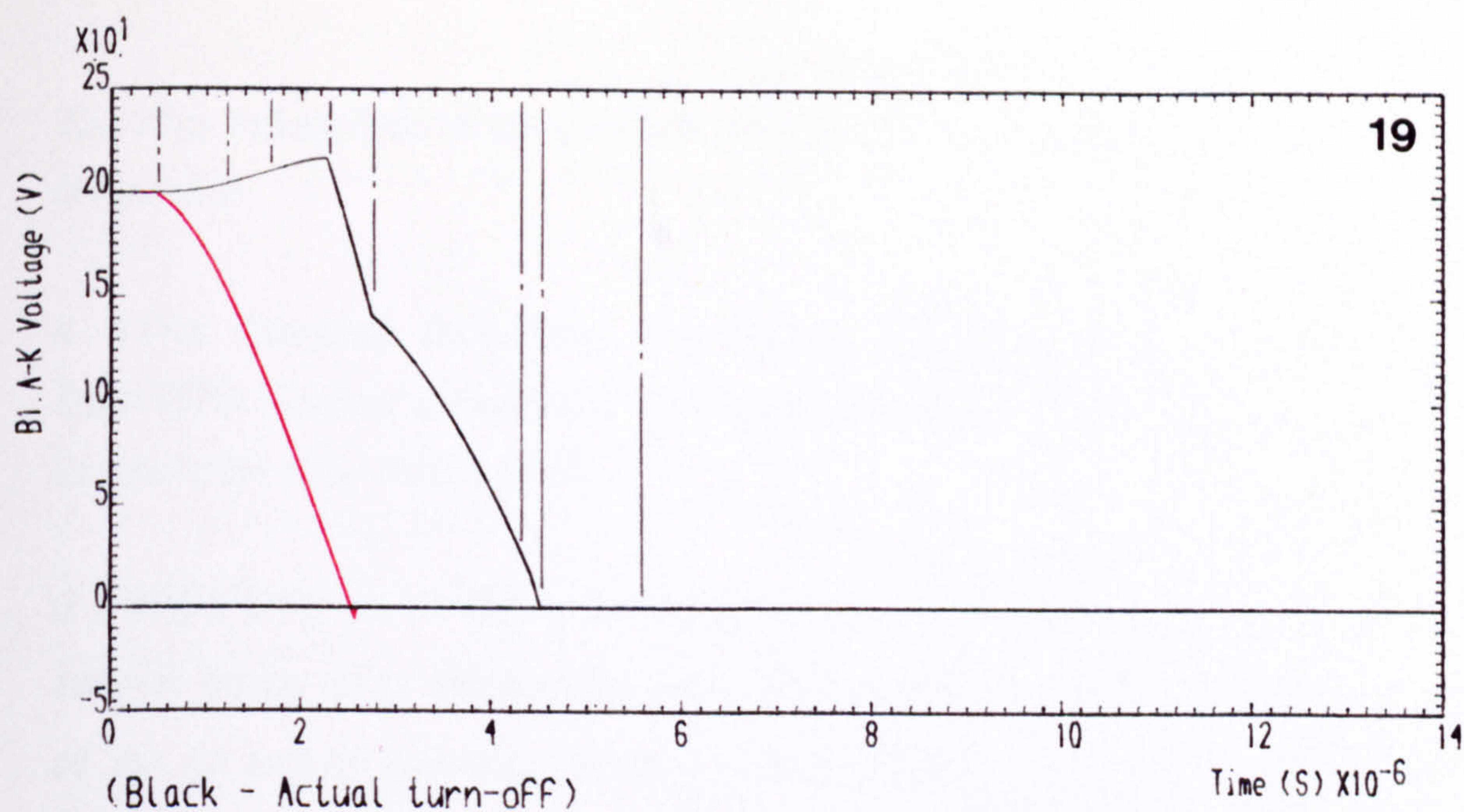


Figure 4.18 Waveforms at GTOs A1 and A2 turn-off together (unbalanced)

END ..

equations of which are given in Figure 4.17(m) and (n). A1 and A2 snubber capacitors now discharge into the source through their snubber resistors with their voltages decaying to  $E_d$ . Interval  $t_9$  is followed by the feedback current falling through diodes D3 and D4, with GTOs A1 and A2 each supporting the supply voltage.



*The stray inductances of the source and those of the antiparallel diode arms are the most influential.*

#### **4.6 The Coupled Switching Transients within the H-Bridge - Summary**

*Each GTO thyristor experiences an oscillatory voltage overshoot at turn-off due to the lumped path stray inductances.*

*If a single GTO A2 (or B2) is turned off with A1 (B1) remaining in conduction, with the internal bridge stray inductances being low relative to that of the supply  $L_d$ , virtually all the A2 turn-off overshoot voltage is conductively coupled round the outside of the bridge and is felt across the blocking GTO B1. Expressed alternatively, most of the A2 overshoot voltage is generated by the supply inductance, and the voltage across B1 rises from the supply voltage level ( $E_d$ ) to the overshoot value experienced by GTO A2, as in Figure 4.12, traces (14) and (15). If  $L_{d3}$  or/and  $L_{d4}$  are increased the overshoot across A2 is higher, but a smaller portion of it, is felt across B1.*

*At a subsequent A1 turn-off, its overshoot voltage is much less than that for A2 due to the reducing freewheeling current being interrupted. Higher  $L_d$  increases the overshoot across A1, virtually all of which is coupled across A2. However, for A2 or B2 turn-off, the inductances  $L_{d3}$  and  $L_{d4}$  increase the overshoot also. These are also coupled.*

*When the switching pattern has simultaneous turn-off of the two conducting GTOs A1 and A2, and since B1 and B2 snubber capacitors discharge from  $E_d$ , then there are no coupled overshoots across the bridge, Figure 4.18(b) (red curves). This is not true if a switching time mismatch occurs.*

*It is worth mentioning that at GTOs A1 and A2 (or B1 and B2) turn-on from zero initial load current, the stray inductances, mainly those of  $L_d$ ,  $L_{d3}$  and  $L_{d4}$ , cause the blocking B1 and B2 voltages to overshoot the supply voltage, Figure 4.11, traces (10) and (12), but are limited to  $3E_d/2$ .*

*Also due principally to  $L_d$ , the sudden voltage drop from the peak value normally*

experienced by the GTO at turn-off, as the capacitor overshoot discharge current transfers from the snubber diode to the resistor, is largely negated by the coupled overshoot across the other switching or the blocking device, this being the 'hold-up' period.

#### **4.7 Ways of Minimising Parasitic Transient Effects in the H-Bridge**

The general points made in section 3.6 relating to the chopper, regarding minimisation of stray circuit inductances are applicable here. Additional features which relate to the H-bridge operating to give a quasi-square output voltage with either freewheeling or feedback interval are [25]:

##### **a) Choice of components:**

- i) The final switching devices for the gate drive circuits, should be very fast - FETs are usual - and drives as well synchronised as possible; to minimise switching time mismatch.*
- ii) Relating to the H-bridge circuit; all diodes should be of the fast recovery types.*

##### **b) Circuit configuration:**

- i) The bridge loop areas should be as small as possible.*
- ii) The semiconductors in each switching branch - GTO, freewheeling diode and snubber diode - should be mounted on the same cooling fin as closely as possible.*
- iii) The upper and lower switching arms of the H-bridge should be very close together.*

#### **4.8 Significance of the Supply Inductance**

*a) Whenever the source current falls during commencement of load current freewheeling or feedback, the induced  $L_d di/dt$  lifts the bridge DC rail potential, giving transient over-voltages across blocking devices.*

*b) The bridge DC rail inductance slightly reduces the above effect across those devices remote from the input.*

*c) Hence the source inductance is especially important and should be minimised by positioning the input capacitor(s) as close to the circuit as possible. Even so, it is*



*likely to be much more significant than the stray inductances within the bridge, as it is easier to reduce these.*

#### **4.9 Conclusions**

*The GTO thyristor switching has been investigated for the H-bridge with resistive-inductive load and freewheeling and feedback paths in the quasi-square output voltage mode. Practical results and computed values of the amplitudes and durations of the transient overshoot voltages appearing across the GTO thyristors at turn-on and off, and their interaction within the bridge, are provided and compared. They show good correlation and confirm the analysis. Differences are mainly due to difficulties in determining precisely the stray inductances data, and the initial assumptions (sub-section 3.2.2).*

*Points which have emerged are:*

- a ) The GTO oscillatory overshoot voltage depends on the effective path stray inductances defined by the particular device(s) being switched, and the current interrupted.*
- b ) The source stray inductance  $L_d$  is the most influential and is usually the largest in the circuit.*
- c ) Overshoot transients for one GTO thyristor in a bridge are coupled conductively to the others.*
- d ) The peak voltage oscillation across each of the two blocking GTOs during turn-on of the complementary pair, the initial load current being zero, will approach 150% supply voltage. Under this condition, the transient charge/discharge currents of the snubber capacitors can interrupt the initial low load current flow through the conducting GTOs, hence the back-porch drive is essential.*
- e ) Switching time mismatch at turn-off of a conducting pair of GTO thyristors results in asymmetry of the transients. Since the later switching GTO undergoes turn-off during the switching transient from the first, it is likely to be required to interrupt a higher current than expected. This can be dangerous if the GTO is operating near its turn-off current limit.*
- f ) Turn-on time mismatch has negligible effect for quasi-square voltage control.*

## CHAPTER 5

### Stray Inductances Effects in the H-Bridge with Pulse Width Modulation (PWM) of Output Voltage

#### 5.1 Introduction

*Electronic switching power inverters are firmly established as the power sources for AC motor drive systems in variable speed applications, and for other uses where a near sinusoidal output of a desired fundamental component is required. Pulse width modulation (PWM) has become an attractive technique for controlling switching inverters in such applications and, in particular for reducing the low order harmonic components in the output voltage waveform.*

*Switching devices with a self-extinguishing function, such as the GTO thyristor or the power transistor, have facilitated the development of light-weight, low cost and more efficient inverters with the employment of pulse width modulation techniques.*

*As the range of application of GTO thyristors in PWM inverters is extending to higher power levels, the problem of efficient snubbing becomes more and more important to ensure safe device switching conditions.*

*The aim now is to extend the previous reasoning to ascertain any additional effects caused by the stray path inductances with PWM control.*

#### 5.2 Background to PWM

*The most important aspects of any pulse-width modulation control technique is the way in which the PWM pattern is obtained. The three distinct approaches in formulating the switching strategies currently in common use are the natural sampled, the regular sampled and the optimized PWM. The principles behind these techniques will be outlined in the following sub-sections, where consideration is given only to the widely used sinusoidal modulation. Other types, such as square, triangular and trapezoidal modulations are possible with only minor modifications to the principles of the above strategies.*

##### 5.2.1 Natural sampled strategy

*PWM inverter control schemes based on natural sampling technique are most widely used.*



*This is because of its inherent simplicity and ease of implementation by analogue techniques.*

*The method of natural sampling is by the direct comparison of a triangular (sampling signal) waveform with a sinusoidal (reference signal) waveform, termed respectively, the carrier and modulating signals, to provide the required PWM pulse widths, as illustrated in Figure 5.1.*

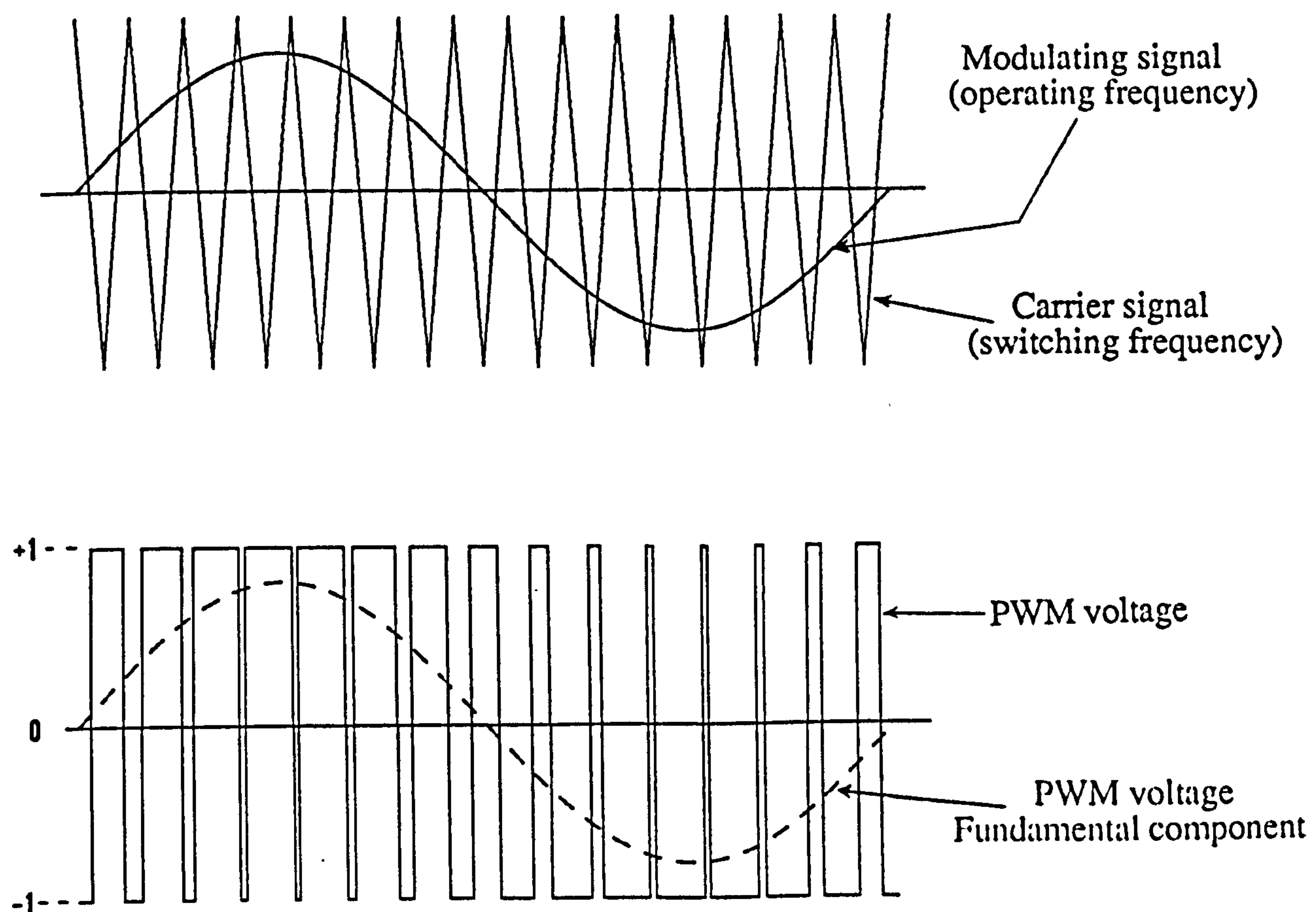


Figure 5.1 2-level natural sampled PWM

*The instantaneous intersection of the two waveforms determines the PWM pulse widths which, are therefore proportional to the amplitude of the modulating signal at that switching instant. Overmodulation occurs at high modulating signal amplitude when the latter fails to intersect all the 'teeth' of the carrier signal resulting in a large pulse width in the middle region of the half-cycle of the modulating signal, Figure 5.2.*

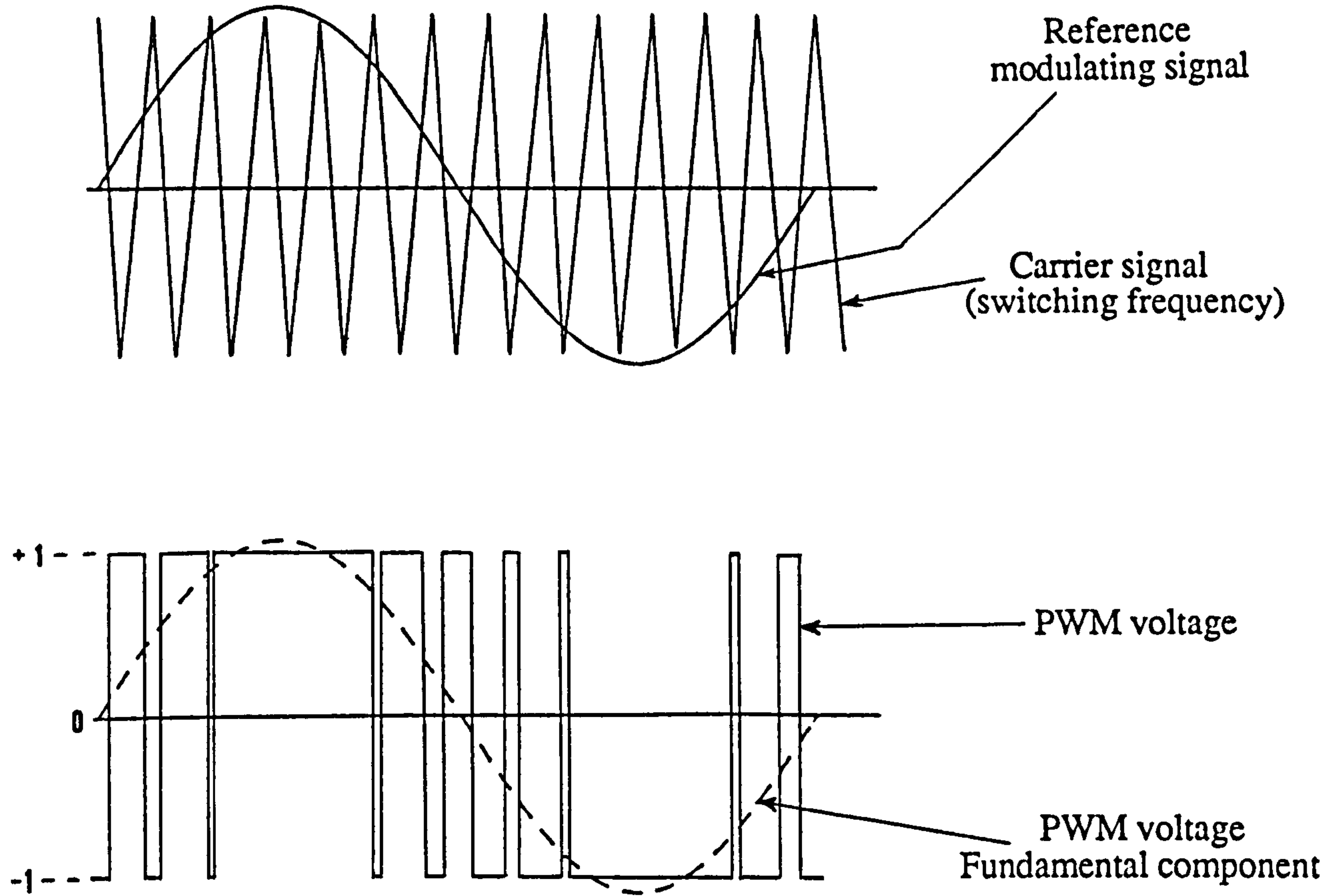


Figure 5.2 2-level natural sampled PWM with over modulation

*The natural sampling method has the following important features [1]:*

- a) The centres of the PWM pulses are not equidistant or uniformly spaced.*
- b) The widths of the PWM pulses cannot readily be defined by analytical expressions.*

*However, the widths of the pulses can be defined using a transcendental equation of the form [29]:*

$$t_p = \frac{T}{2} \left[ 1 + \frac{M}{2} (\sin \omega_m t_1 + \sin \omega_m t_2) \right] \quad (5.1)$$

*where  $t_p$  is the width of the modulated pulse*



$M$  is the modulation index, defined to be the ratio of the carrier to the modulating signal amplitudes

$\omega_m$  is the angular frequency of the modulating signal

$t_1$  is the instant at which the pulse rises

$t_2$  is the instant at which the pulse falls

$T$  is the carrier signal period.

The technique shown in Figure 5.1 is referred to as 2-level PWM [30], as the PWM voltage switches between levels (+1) and (-1), whereas a 3-level PWM can be produced by switching the PWM voltage between levels (+1), 0 and (-1), as shown in Figure 5.3. The latter can be achieved by changing the polarity of the modulating signal every half-cycle. Although the natural switching strategy inherently calls for an analogue technique, a digital implementation is possible.

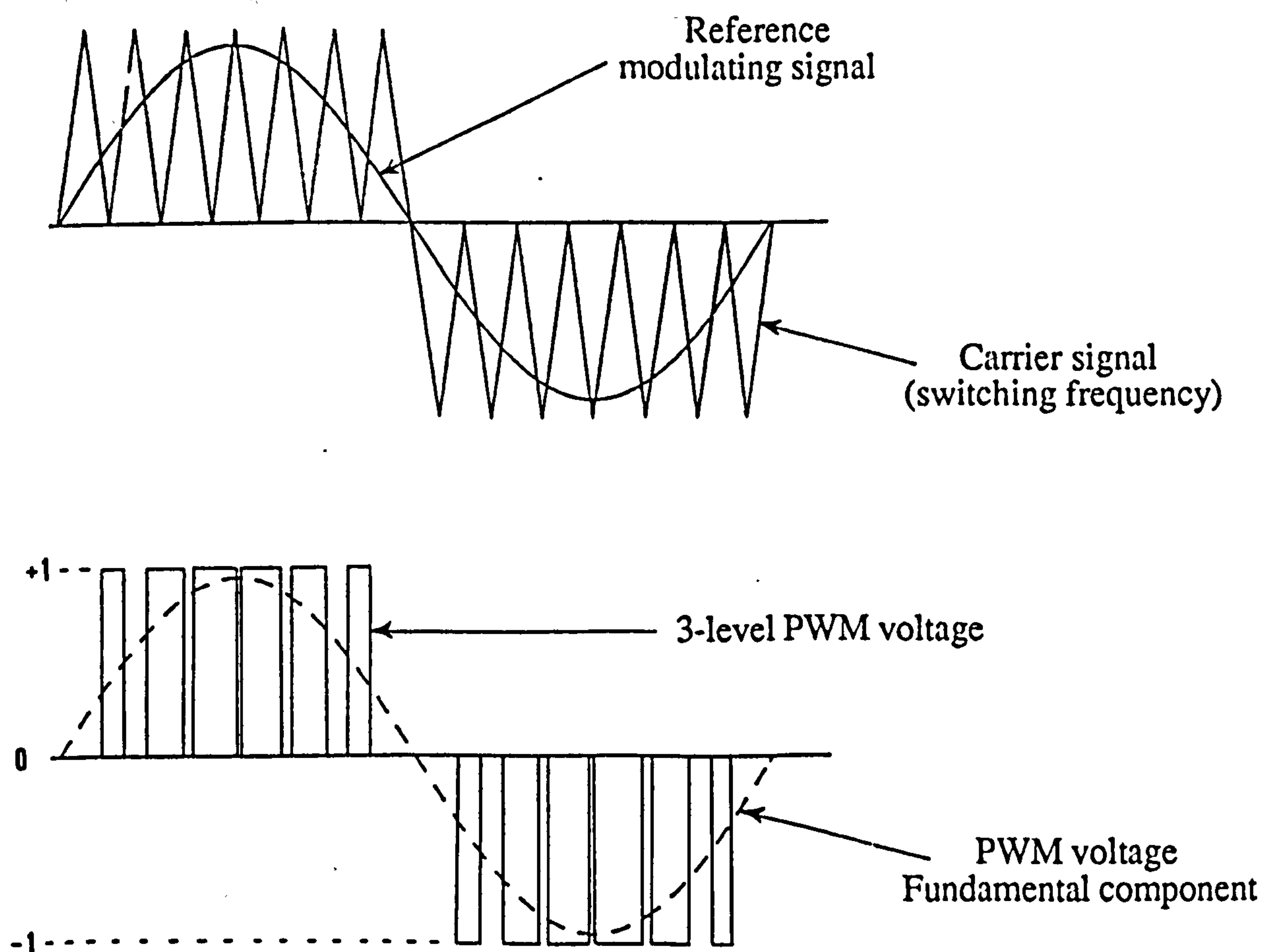


Figure 5.3 3-level natural sampled PWM

### 5.2.2 Regular sampled PWM

The regular sampled PWM control, Figure 5.4, is better suited for digital or microprocessor implementation. The pattern is given by the comparison of the carrier signal with a stepped signal obtained by regularly sampling the sinusoidal wave and holding its value at the same level (intersample period [29]), until the next sampling instant giving a constant modulating wave amplitude while each sample is being taken. The switching instants  $T_1$  and  $T_2$  (Figure 5.4) of the width modulated pulses are determined by the intersection points of the two signals, the widths of which are proportional to the constant amplitude of the modulating wave with their centres uniformly spaced in time, making it possible to predict the widths and positions of the pulses. Consequently, a simple trigonometric function for calculating the pulse widths is [29]:

$$t_p = \frac{T}{2} (1 + M \sin \omega_m t_1) \quad (5.2)$$

where  $t_1$  is a sampled instant.

Regular sampled PWM can be generated either as a 2 or 3-level control; also as illustrated in Figure 5.5, it may be 'symmetric' or 'asymmetric' modulation. The former is achieved as explained above; the sample and hold of the modulating wave being operated at the carrier frequency and the leading and trailing edges of each width modulated pulse are determined using the same intersample period, Figure 5.5(a). For the 'asymmetrically' modulated PWM, Figure 5.5(b), the switching instants of the width modulated pulses are determined using two consecutive intersample periods, hence each pulse edge is modulated by a different amount, i.e. the sample and hold being operated at twice the carrier wave frequency. Thus for the 'asymmetrical' modulation [29]:

$$t_p = \frac{T}{2} \left[ 1 + \frac{M}{2} (\sin \omega_m t_1 + \sin \omega_m t_3) \right] \quad (5.3)$$

where  $t_1$  and  $t_3$  are sampling instants.

Although the 'asymmetric' modulation contains more information about the modulating signal and produces a better harmonic spectrum than that of the 'symmetrically' modulated, it requires double the number of calculations.



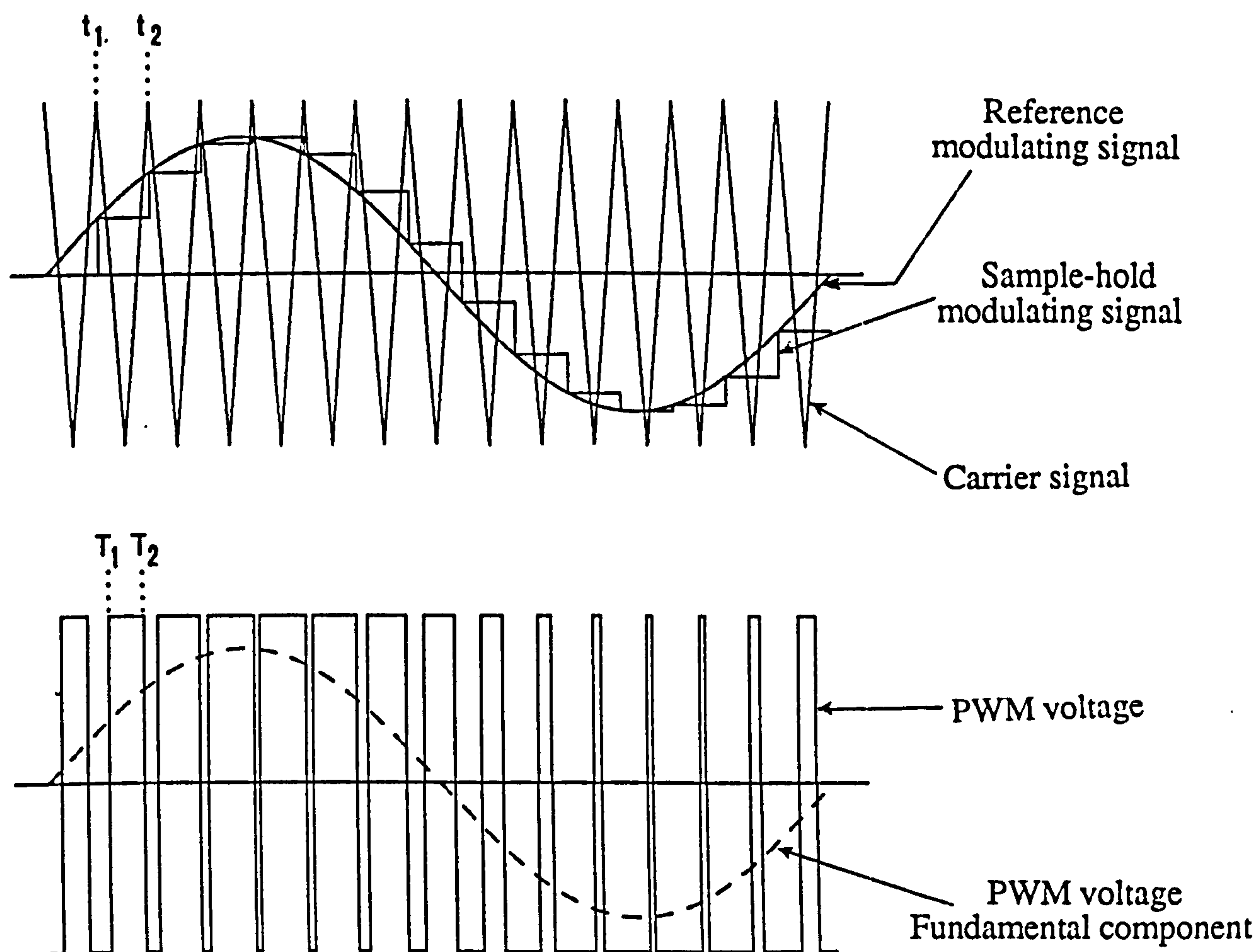


Figure 5.4 Regular sampled PWM

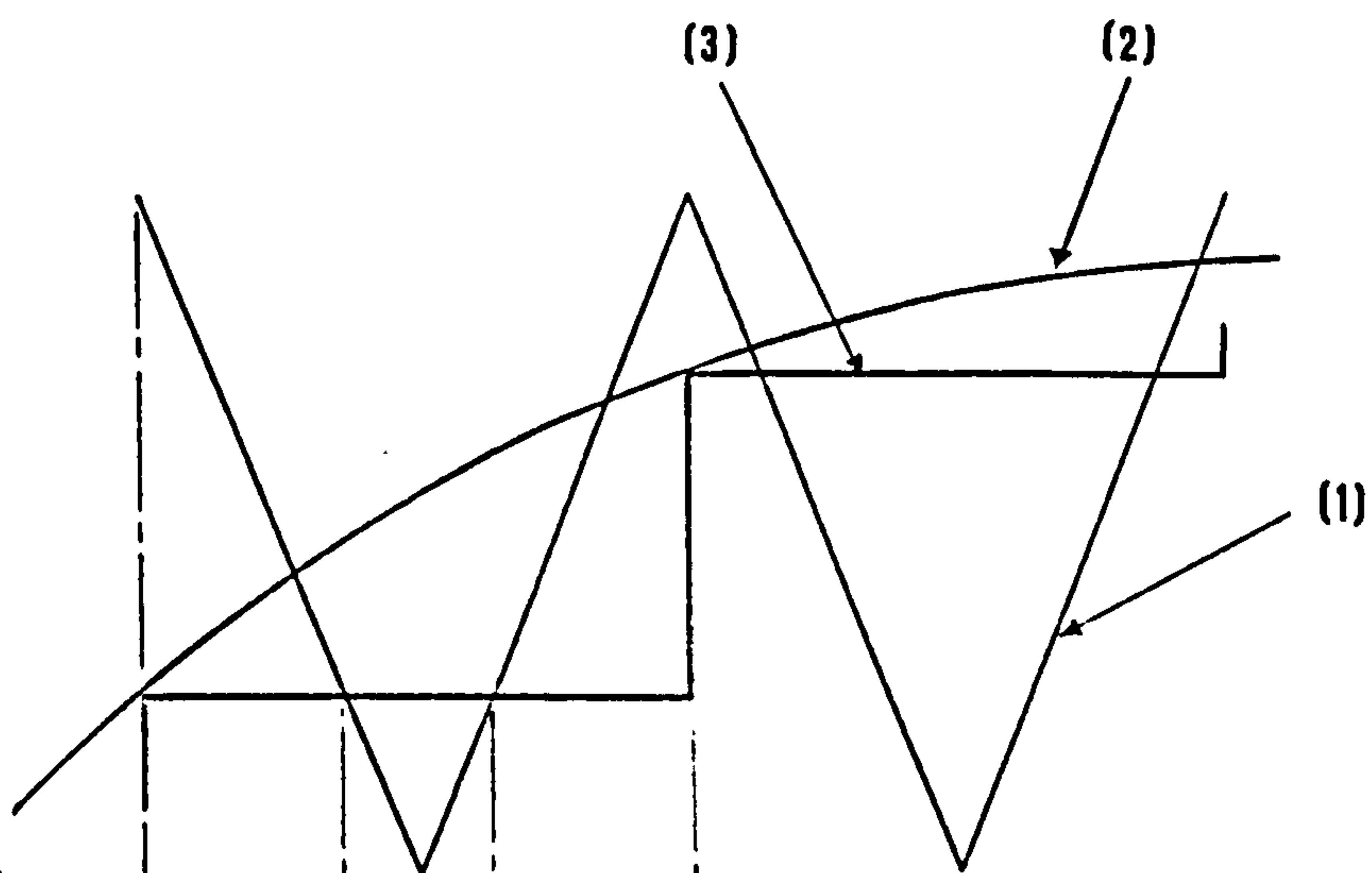
### 5.2.3 Optimised PWM

*The optimum PWM strategy is based on defining a PWM waveform in terms of a set of switching angles with respect to a particular performance criteria such as elimination or minimisation of particular voltage harmonics or the minimisation of total harmonic distortion.*

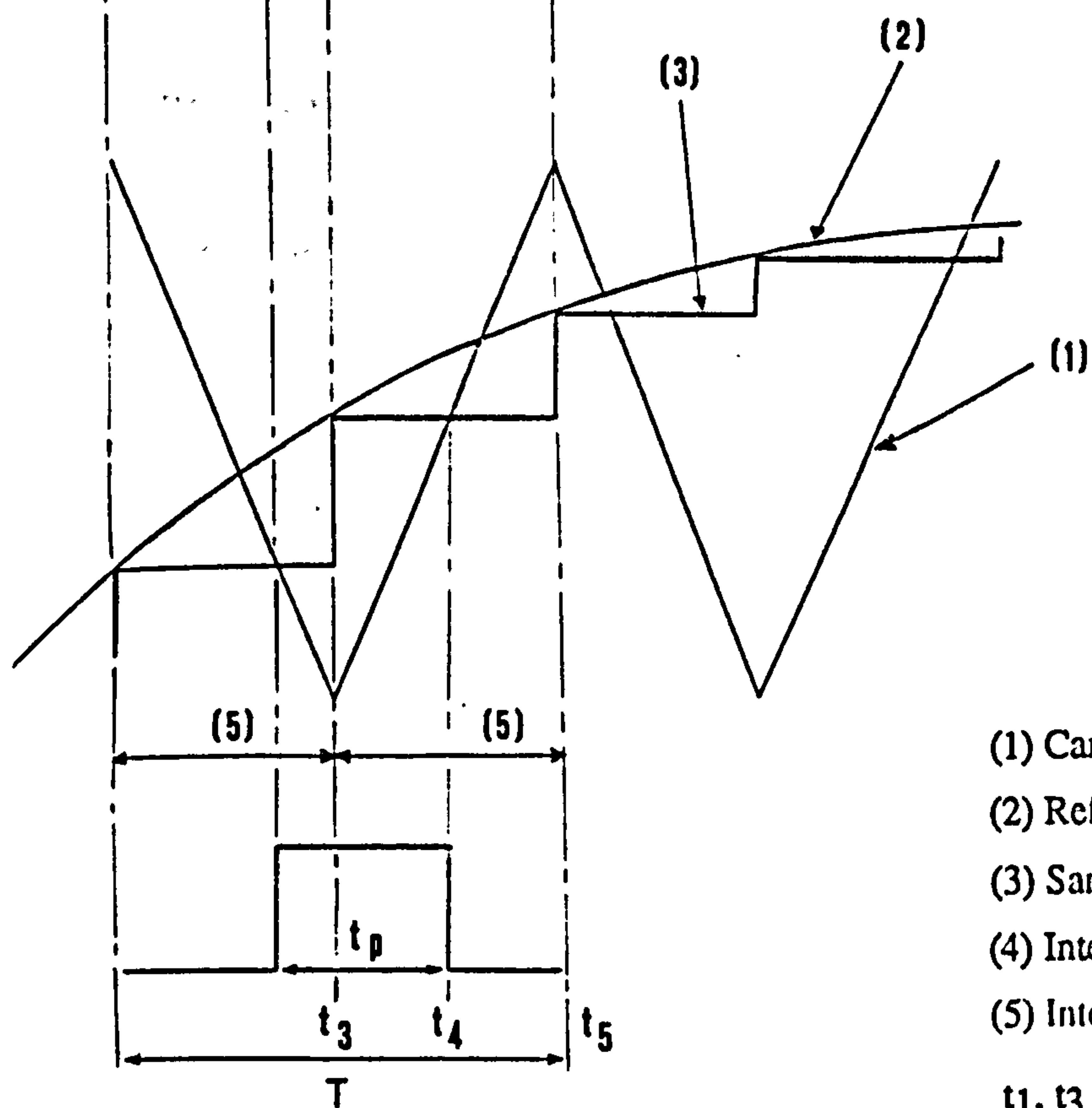
*Once the optimised switching angles are determined from solution of algorithms on a main frame computer, they are subsequently programmed into a microprocessor memory in order to generate the PWM switching strategy in 'real time'.*

### 5.3 The H-Bridge Modes of Operation with PWM

*The H-bridge, Figure 4.1, may be operated in either of the following modes:*



(a) Symmetric regular sampled PWM



- (1) Carrier signal
- (2) Reference modulating signal
- (3) Sample-hold modulating signal
- (4) Intersample period (symmetric PWM)
- (5) Intersample period (asymmetric PWM)

$t_1$ ,  $t_3$  and  $t_5$  are sampling instants  
 $t_2$  and  $t_4$  are switching instants

(b) Asymmetric regular sampled PWM

Figure 5.5 Symmetric and asymmetric regular sampled PWM



**Mode (1)** - For the positive half-cycle of the operating frequency, GTO A1 is switching at the carrier wave frequency, whereas GTO A2 is turned on for the full half-cycle (Figure 5.6, traces (3) and (4)). From Chapter 4, it will be apparent that the inductive load current at GTO A1 turn-off freewheels through diode D4 and GTO A2. It returns to GTOs A1 and A2 when A1 turns on again. GTOs B1 and B2 and diode D2 are engaged in a similar manner for the negative half-cycle. This gives a three-level PWM pattern.

**Mode (2)** - Each diagonal pair of GTO thyristors (A1 and A2, and B1 and B2), is switching at the carrier frequency for each half-cycle of the operating frequency (Figure 5.7, traces (3), (4), (5) and (6)), this giving two-level PWM output.

Now within each half-cycle, when both GTOs of a conducting pair are off, the inductive load current is fed back to the DC supply. The current commutates back to the same GTO pair at their following turn-on.

#### **5.4 Modelling of Parasitic Transient Behaviour at GTO Thyristor Switching In the H-Bridge within a Half-Cycle**

The procedure for obtaining and solving the system equations is similar to that used previously, with all previous simplifying assumptions applying here. The H-bridge is operated and modelled with the following conditions:

Carrier frequency = 720Hz

Modulating frequency = 40Hz

Supply voltage = 200V

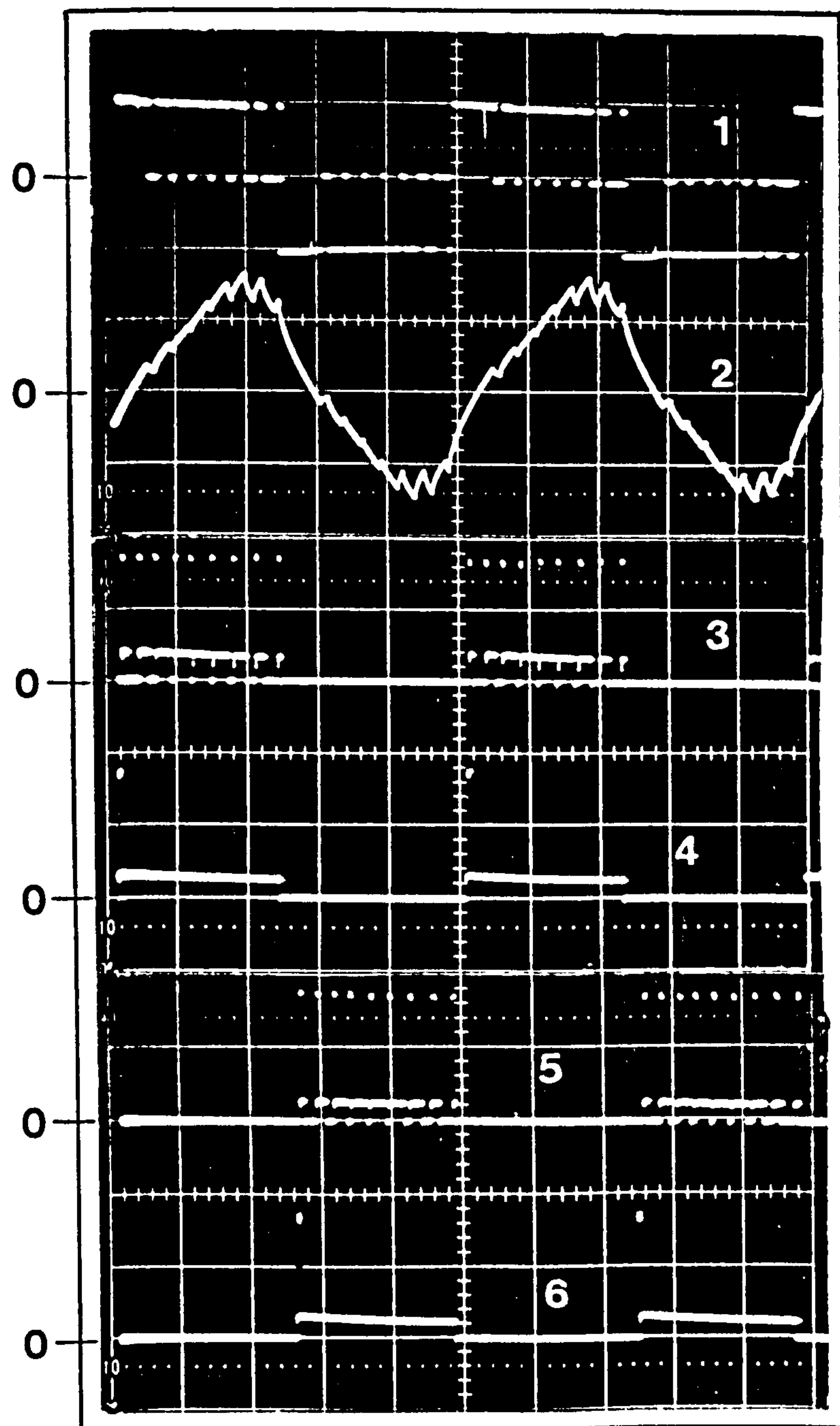
Load resistance =  $2.2\Omega$

Load inductance =  $650\mu H$

Snubber component values and stray path inductances are as given in Chapter 4.

##### **5.4.1 Turn-off transients**

The transients when turning off either one or both conducting GTOs are identical with those of Chapter 4. The new feature here lies in the GTO turn-on transients since, within the PWM half-cycle, a previously conducting GTO is turned on again. With the previous

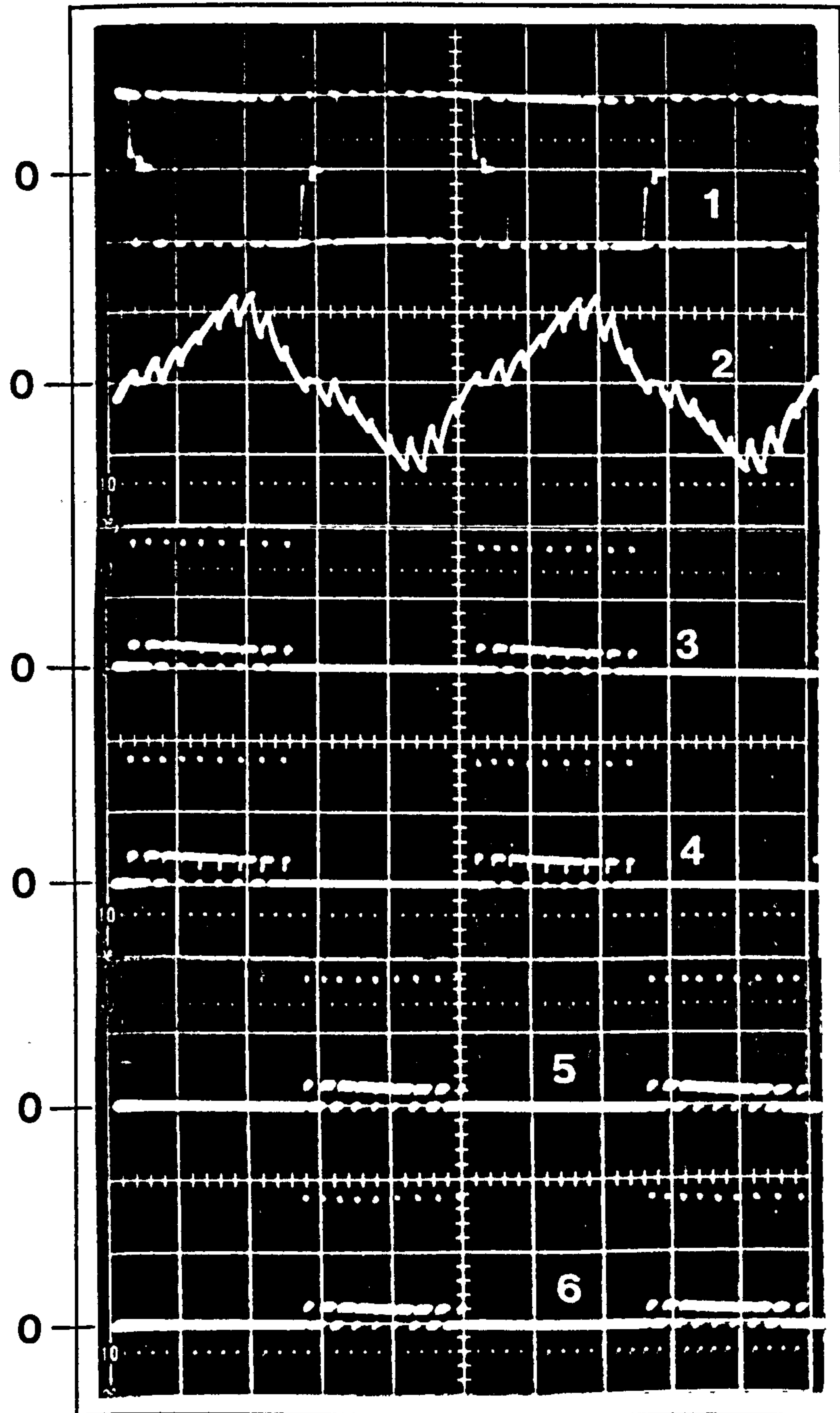


- |                               |             |
|-------------------------------|-------------|
| (1) Load Voltage (3-Level)    | (200V/div.) |
| (2) Load Current              | (50A/div.)  |
| (3) GTO A1 Gate Current Pulse | (5A/div.)   |
| (4) GTO A2 Gate Current Pulse | (5A/div.)   |
| (5) GTO B1 Gate Current Pulse | (5A/div.)   |
| (6) GTO B2 Gate Current Pulse | (5A/div.)   |

Time Scale: 5mS/div.

Figure 5.6 Bridge operation with GTOs A1 and B1 switching at carrier signal frequency (3-level PWM)





- |                               |             |
|-------------------------------|-------------|
| (1) Load Voltage (2-Level)    | (200V/div.) |
| (2) Load Current              | (50A/div.)  |
| (3) GTO A1 Gate Current Pulse | (5A/div.)   |
| (4) GTO A2 Gate Current Pulse | (5A/div.)   |
| (5) GTO B1 Gate Current Pulse | (5A/div.)   |
| (6) GTO B2 Gate Current Pulse | (5A/div.)   |

Time Scale: 5mS/div.

Figure 5.7 Bridge operation with GTOs A1 and A2 and B1 and B2 switching at carrier signal frequency (2-level PWM)

quasi-square output, the incoming GTOs were always the alternate pair to start a new half-cycle.

#### **5.4.2 Turn-on transients**

*It follows from the end of the previous section that the turn-on at the start of each half-cycle with both two-level and three-level PWM produces transients identical with a quasi-square output, described in sub-section 4.5.1(a). GTO turn-on within a half-cycle is now considered in detail.*

##### **a) Single GTO thyristor turn-on from freewheeling (Mode (1))**

*With GTO A1 off (A2 permanently on), the load current freewheels through A2 and D4, giving zero load voltage. When A1 is turned on again, the situation reverts to a DC source supplied load. This can be appropriate for the bridge operating as a DC chopper as well as an inverter.*

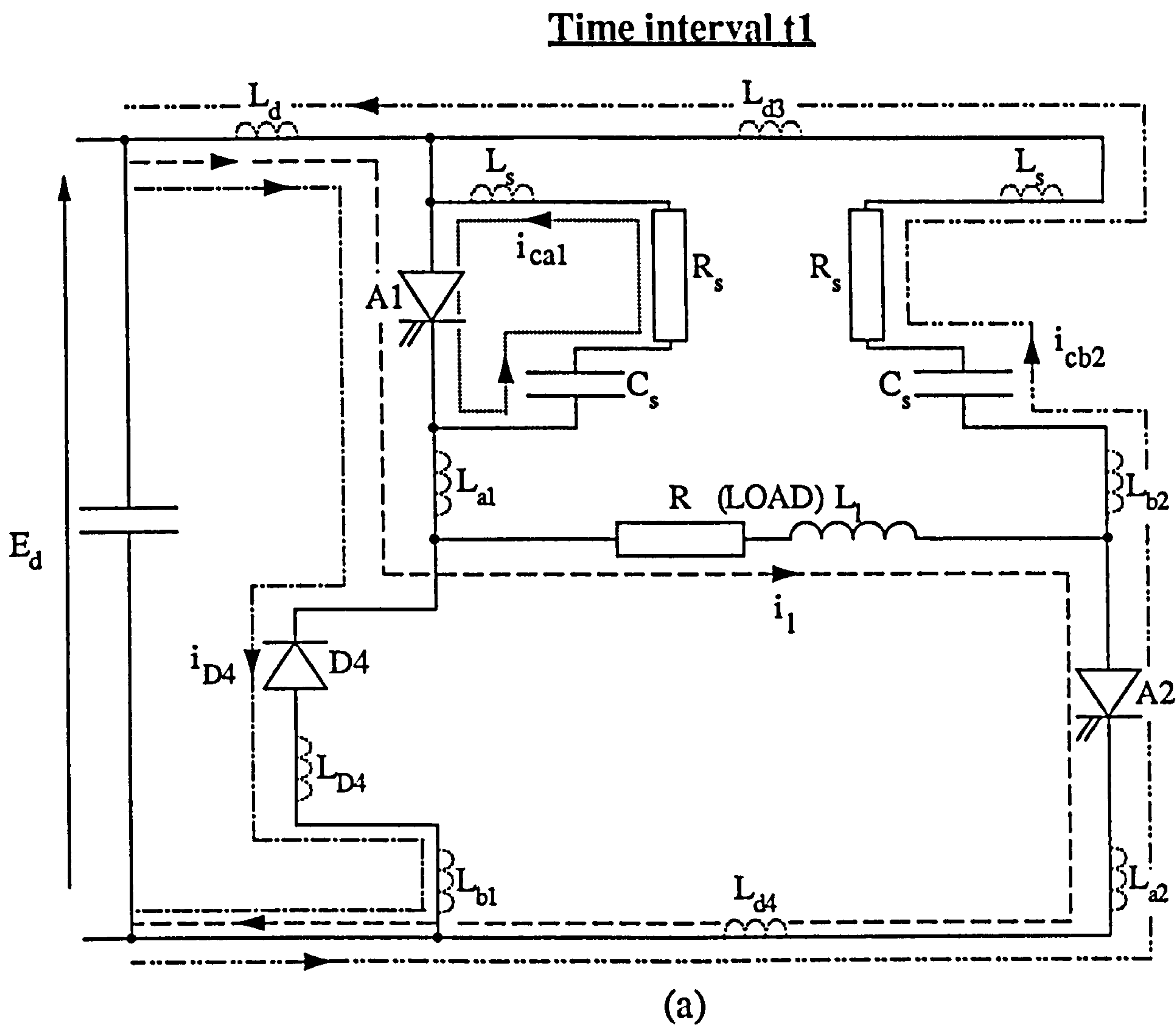
*The GTO A1 turn-on process is divided into five time intervals:*

**Interval  $t_1$ :** *The equivalent circuit and state equations of this interval, which commences as the supply current starts rising and ends when diode D4 has fully reverse recovered, are shown respectively in Figure 5.8(a) and (b). As A1 picks up the load current from diode D4, its snubber capacitor, previously charged to  $E_d$ , discharges locally through the associated resistor and GTO A1. The observed and computed waveforms are shown in Figure 5.9(a) and (b) respectively.*

*As the supply current rises through  $L_d$  and A1, it initially depresses the bridge DC rail potential, and produces a coupled transient across the blocking GTO B2 with an oscillatory discharge of its snubber capacitor through its snubber resistor, Figure 5.9, traces (6), (10) and (11). The load current is maintained constant by the high load inductance (trace (5)).*

*An important feature is that during diode D4 reverse recovery, a temporary shoot-through condition occurs across the DC rails (via GTO A1). Inductances  $L_d$ ,  $L_{a1}$ ,  $L_{D4}$  and  $L_{b1}$  exert a limiting influence on the current rise, and frequently the  $L_a$  and  $L_b$  inductances are enhanced by added inductors, usually with their own freewheeling diodes to avoid greatly increasing the voltage overshoot at GTO turn-off.*



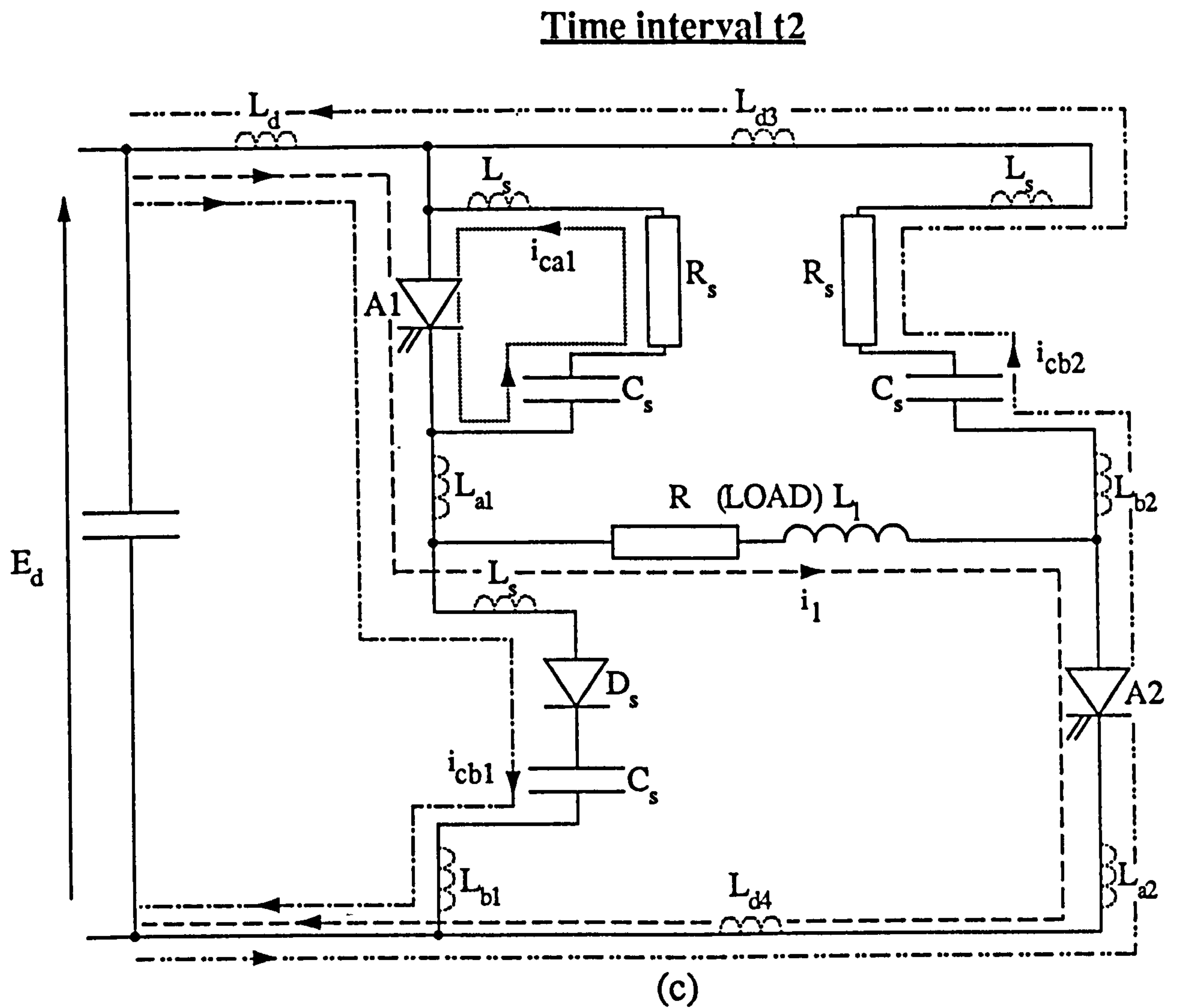


COLUMNS

	(1)	(2)	(3)	(4)	(5)	(6)		
$p i_{ca1}$	$-\frac{R_s}{L_s}$	0	0	0	$\frac{1}{L_s}$	0	$i_{ca1}$	0
$p i_{cb2}$	0	$-\frac{R_s L_7}{L_1}$	0	$\frac{R L_6}{L_1}$	0	$-\frac{L_7}{L_1}$	$i_{cb2}$	$E_d \frac{L_5}{L_1}$
$p i_{D4}$	0	$-\frac{R_s L_4}{L_1}$	0	$\frac{R L_3}{L_1}$	0	$-\frac{L_4}{L_1}$	$i_{D4}$	$E_d \frac{L_2}{L_1}$
$p i_1$	0	$\frac{R_s L_{11}}{L_8}$	0	$-\frac{R L_{10}}{L_8}$	0	$\frac{L_{11}}{L_8}$	$i_1$	$E_d \frac{L_9}{L_8}$
$p v_{ca1}$	$-\frac{1}{C_s}$	0	0	0	0	0	$v_{ca1}$	0
$p v_{cb2}$	0	$\frac{1}{C_s}$	0	0	0	0	$v_{cb2}$	0

(b)

Figure 5.8    Equivalent circuit and state equations matrices for GTO A1 picking up load current from the freewheeling path.



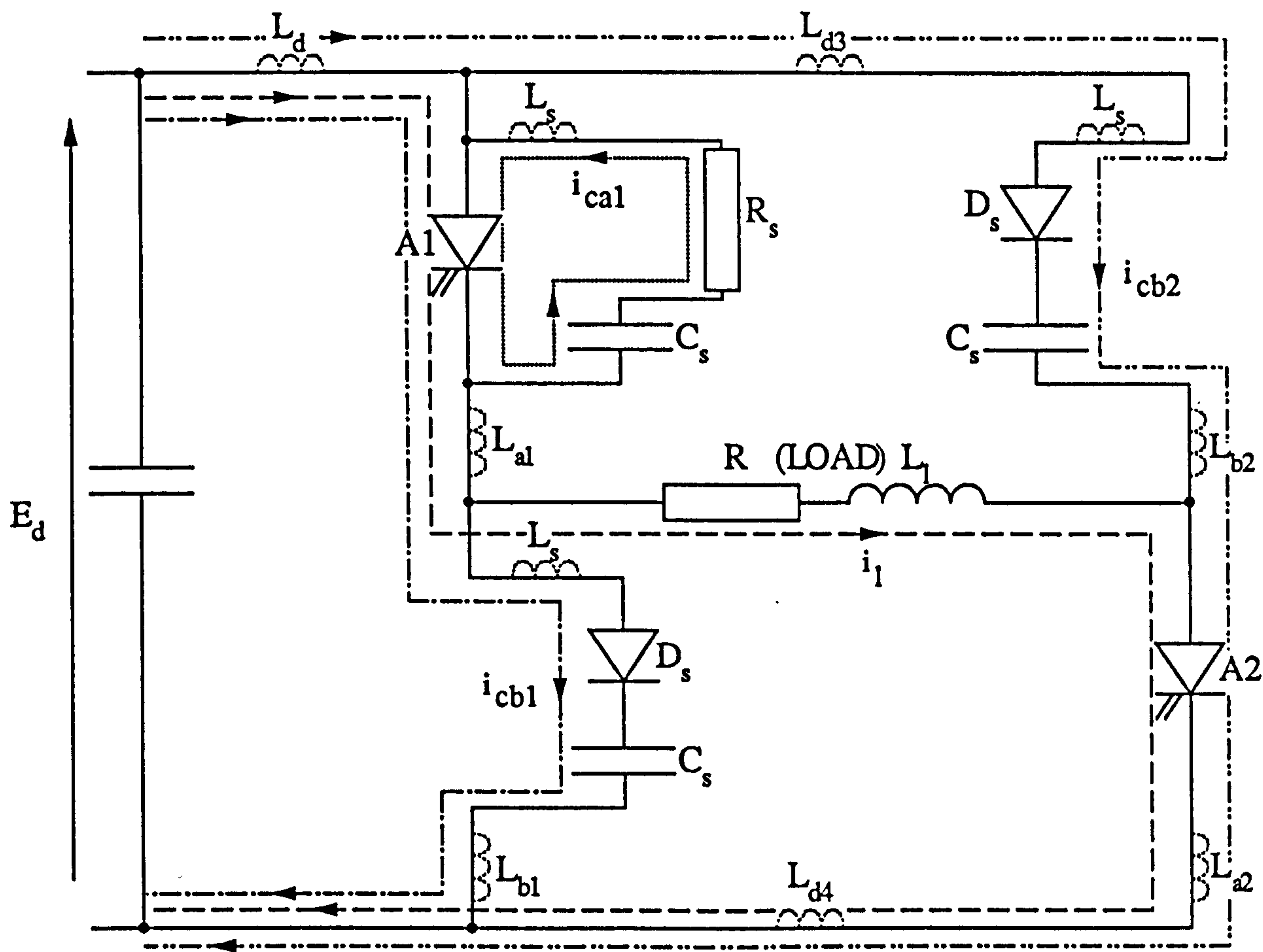
COLUMNS	(1)	(2)	(3)	(4)	(5)	(6)	(7)		
$p i_{ca1}$	$-\frac{R_s}{L_s}$	0	0	0	$\frac{1}{L_s}$	0	0	$i_{ca1}$	0
$p i_{cb1}$	0	0	$-\frac{R_s L_4}{L_{12}}$	$\frac{R L_3}{L_{12}}$	0	$-\frac{L_{13}}{L_{12}}$	$-\frac{L_4}{L_{12}}$	$i_{cb1}$	$E_d \frac{L_2}{L_{12}}$
$p i_{cb2}$	0	0	$-\frac{R_s L_{16}}{L_{12}}$	$\frac{R L_{15}}{L_{12}}$	0	$-\frac{L_4}{L_{12}}$	$-\frac{L_{16}}{L_{12}}$	$i_{cb2}$	$E_d \frac{L_{14}}{L_{12}}$
$p i_1$	0	0	$\frac{R_s L_{21}}{L_{17}}$	$-\frac{R L_{19}}{L_{17}}$	0	$\frac{L_{20}}{L_{17}}$	$\frac{L_{21}}{L_{17}}$	$i_1$	$E_d \frac{L_{18}}{L_{17}}$
$p v_{ca1}$	$-\frac{1}{C_s}$	0	0	0	0	0	0	$v_{ca1}$	0
$p v_{cb1}$	0	$\frac{1}{C_s}$	0	0	0	0	0	$v_{cb1}$	0
$p v_{cb2}$	0	0	$\frac{1}{C_s}$	0	0	0	0	$v_{cb2}$	0

(d)

Figure 5.8    Equivalent circuits and state equations matrices for GTO A1 picking up load current from the freewheeling path.



Time interval t3



(e)

COLUMNS	(1)	(2)	(3)	(4)	(5)	(6)	(7)
$p \ i_{ca1}$			0				$i_{ca1}$
$p \ i_{cb1}$			0				$i_{cb1}$
$p \ i_{cb2}$			0				$i_{cb2}$
$p \ i_1$			0				$i_1$
$p \ v_{ca1}$			0				$v_{ca1}$
$p \ v_{cb1}$			0				$v_{cb1}$
$p \ v_{cb2}$			$\frac{1}{C_s}$				$v_{cb2}$

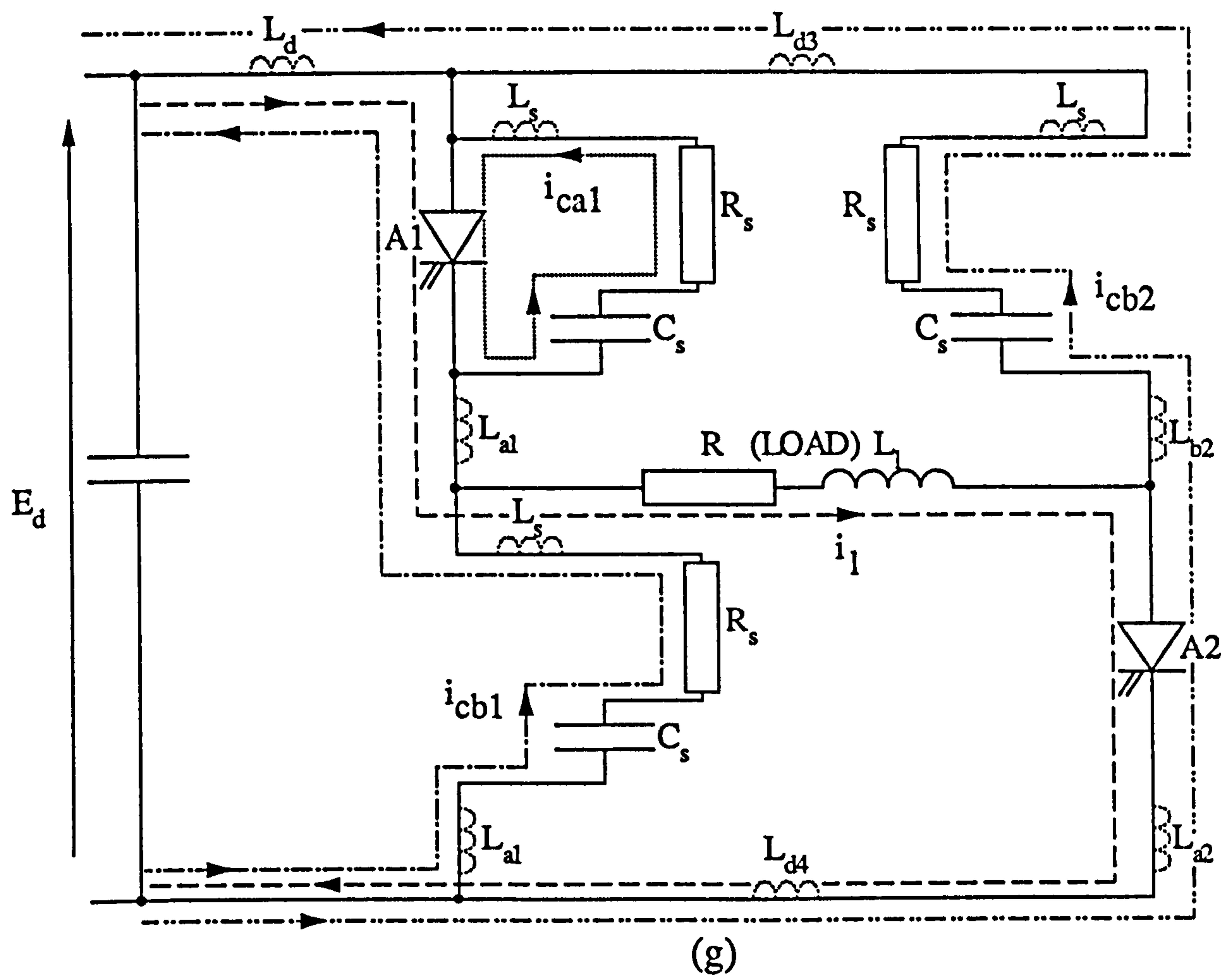
(Columns 1 and 2, and 4 to 7 as in (d))

$i_{ca1}$	0
$i_{cb1}$	$E_d \frac{L_2}{L_{12}}$
$i_{cb2}$	$E_d \frac{L_{14}}{L_{12}}$
$i_1$	$E_d \frac{L_{18}}{L_{17}}$
$v_{ca1}$	0
$v_{cb1}$	0
$v_{cb2}$	0

(f)

Figure 5.8 Equivalent circuits and state equations matrices for GTO A1 picking up load current from the freewheeling path.

Time interval t5



(g)

COLUMNS	(1)	(2)	(3)	(4)	(5)	(6)	(7)
$p \ i_{ca1}$		0					$i_{ca1}$
$p \ i_{cb1}$		$-\frac{R_s L_{13}}{L_{12}}$					$i_{cb1}$
$p \ i_{cb2}$		$-\frac{R_s L_4}{L_{12}}$					$i_{cb2}$
$p \ i_1$	=	$\frac{R_s L_{20}}{L_{17}}$		(Columns 1, and 3 to 7 as in (d))			$i_1$
$p \ v_{ca1}$		0					$v_{ca1}$
$p \ v_{cb1}$		$\frac{1}{C_s}$					$v_{cb1}$
$p \ v_{cb2}$		0					$v_{cb2}$

(h)

Figure 5.8    Equivalent circuits and state equations matrices for GTO A1 picking up load current from the freewheeling path.



A voltage spike similar to that felt by the GTO during its anode current fall time at turn-off is experienced here by GTO B1, Figure 5.9, trace (9). This is due to the reverse recovery 'snap-off' of this transient shoot-through current in the stray inductance  $L_{D4}$ . However, here, the voltage spike peak is fairly small as a fast reverse recovery diode is used and  $L_{D4}$  is very small.

**Interval  $t_2$ :** This interval, the equivalent circuit and state equations of which become as shown respectively in Figure 5.8(c) and (d), lasts from the reverse recovery of diode D4 until the discharge current of B2 snubber capacitor has reached zero. B1 snubber capacitor starts charging oscillatorily through GTO A1 with its voltage rising from zero, although in practice the capacitor charges slightly during diode D4 reverse recovery. The discharge current of B2 snubber capacitor is now decaying to zero.

**Interval  $t_3$ :** This is the time taken for the B2 snubber capacitor to recharge with an opposite oscillatory half-cycle, giving voltage overshoot across it. The interval ends as the B2 snubber diode reverse recovers, Figure 5.9, traces (4) and (10). The equivalent circuit and state equations are given in Figure 5.8(e) and (f) respectively.

The voltage overshoot across the B2 snubber capacitor is due to the supply current oscillation decay in  $L_d$  (ignoring the small voltage drops across  $L_{d3}$  and  $L_{d4}$ ). The  $L_d$  induced voltage also causes the B1 snubber capacitor to further overshoot  $E_d$  as demonstrated in Figure 5.9, traces (3) and (8).

**Interval  $t_4$ :** This interval lasts from the reverse recovery of B2 snubber diode to the reverse recovery of B1 snubber diode. The circuit topology for this time interval is similar to that of time interval  $t_2$ .

The B2 snubber diode reverse recovery current is now commutated to the associated resistor, dropping the voltage across GTO B2. GTO B1 then exerts a hold-up effect on B2 voltage until B1 snubber diode reverse recovery is completed, Figure 5.9, traces (9) and (11).

**Interval  $t_5$ :** This interval starts as the B1 snubber diode is fully reverse recovered, and ends when the discharge currents of B1 and B2 reach zero (traces (3) and (4)). The equivalent circuit and state equations are shown respectively in Figure 5.8(g) and (h). The B1 snubber diode reverse recovery is completed with the capacitor current now

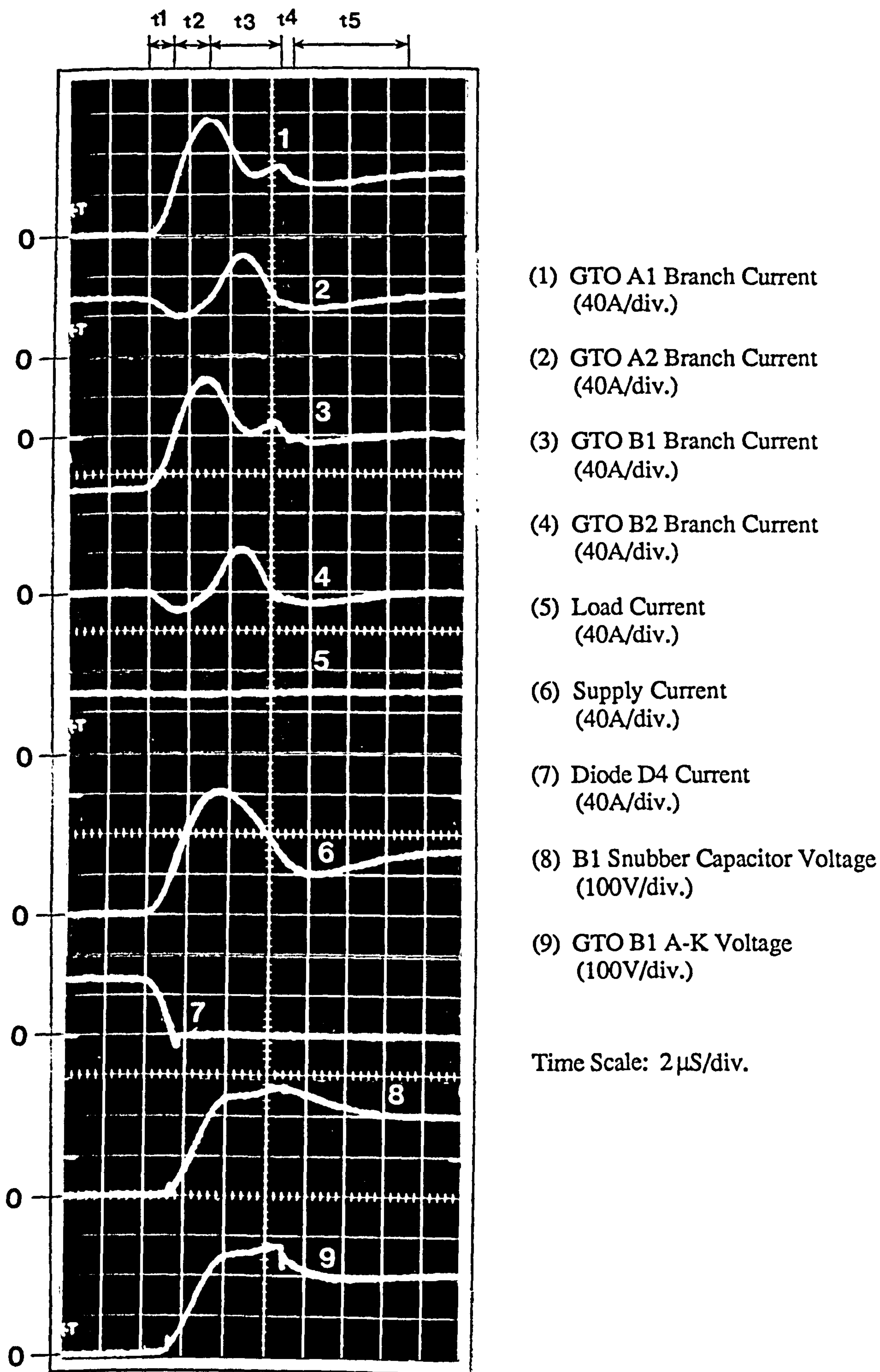
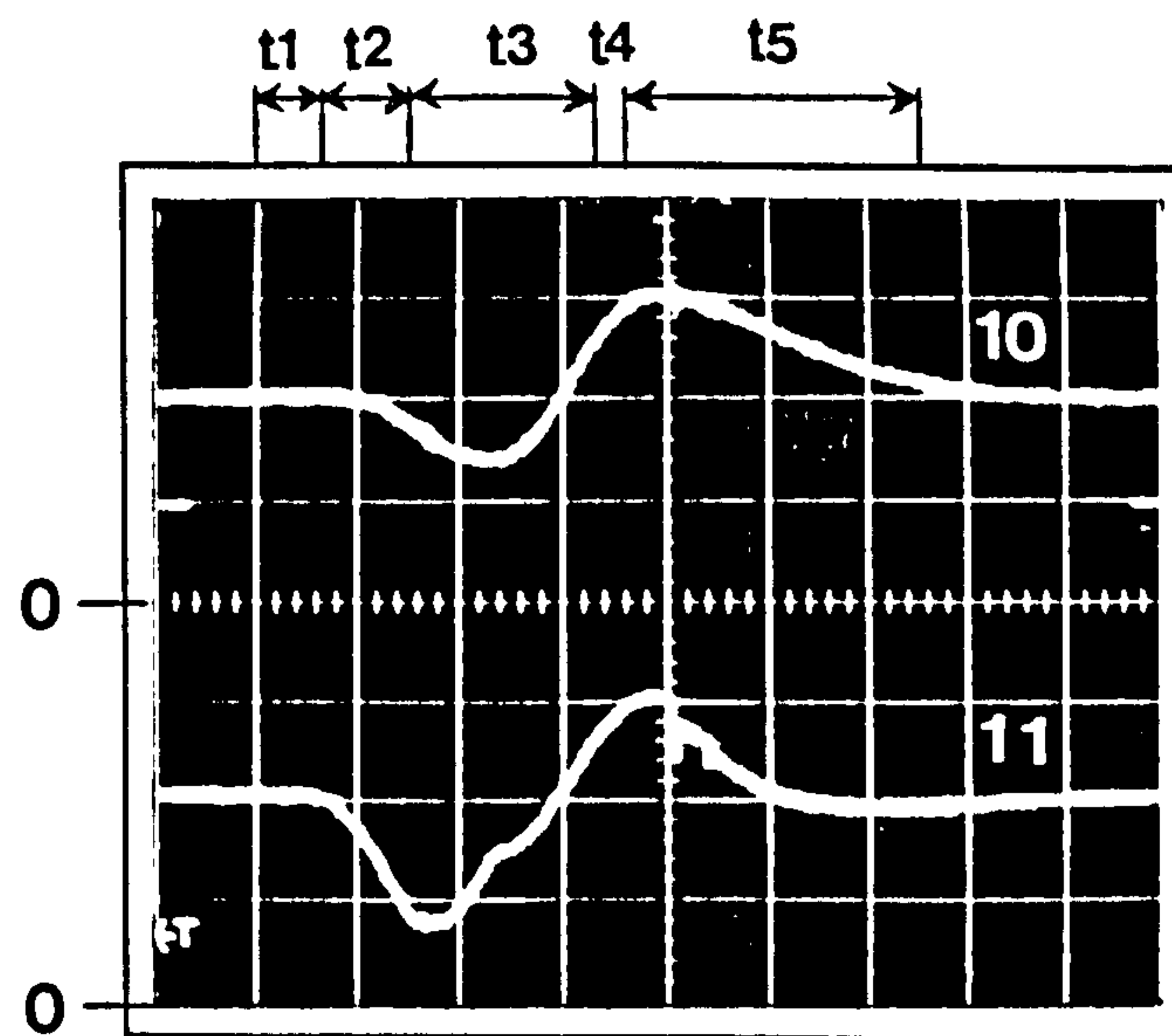


Figure 5.9 Waveforms at GTO A1 picking up load current from the freewheeling path



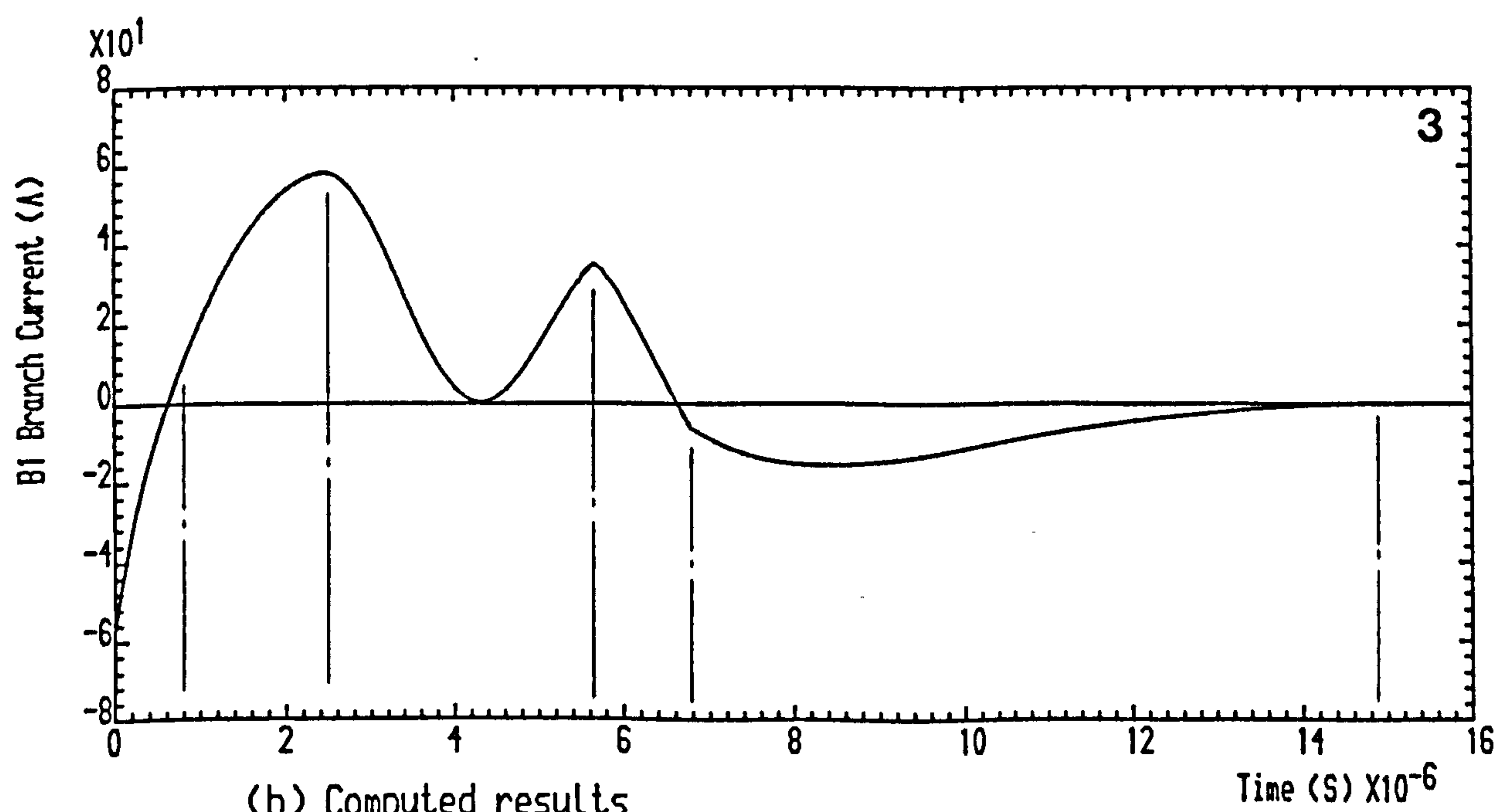
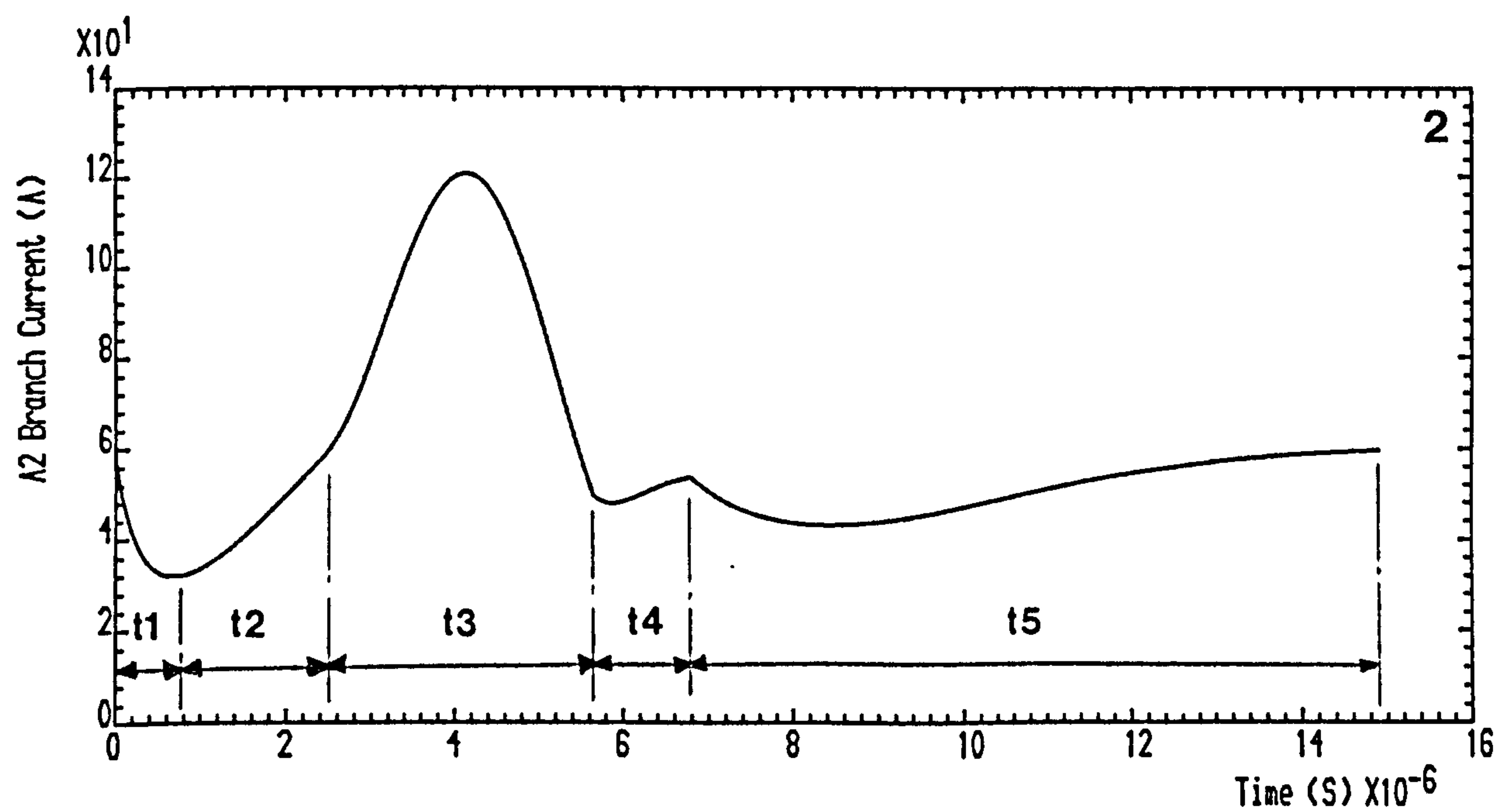
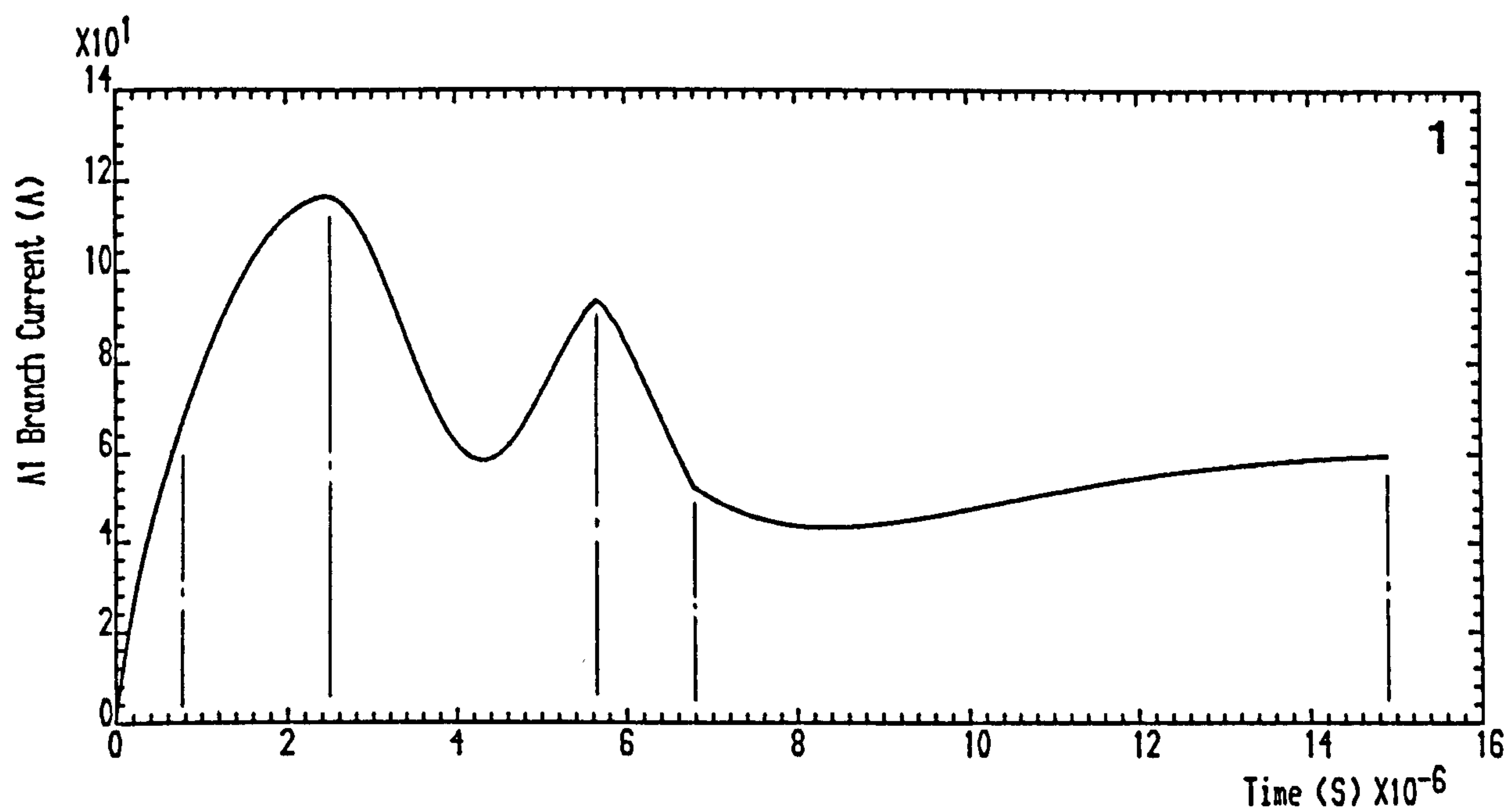


(10) B2 Snubber Capacitor Voltage (100V/div.)  
 (11) GTO B2 A-K Voltage (100V/div.)

Time Scale: 2  $\mu$ S/div

(a) Experimental Results

Figure 5.9 Waveforms at GTO A1 picking up load current from the freewheeling path

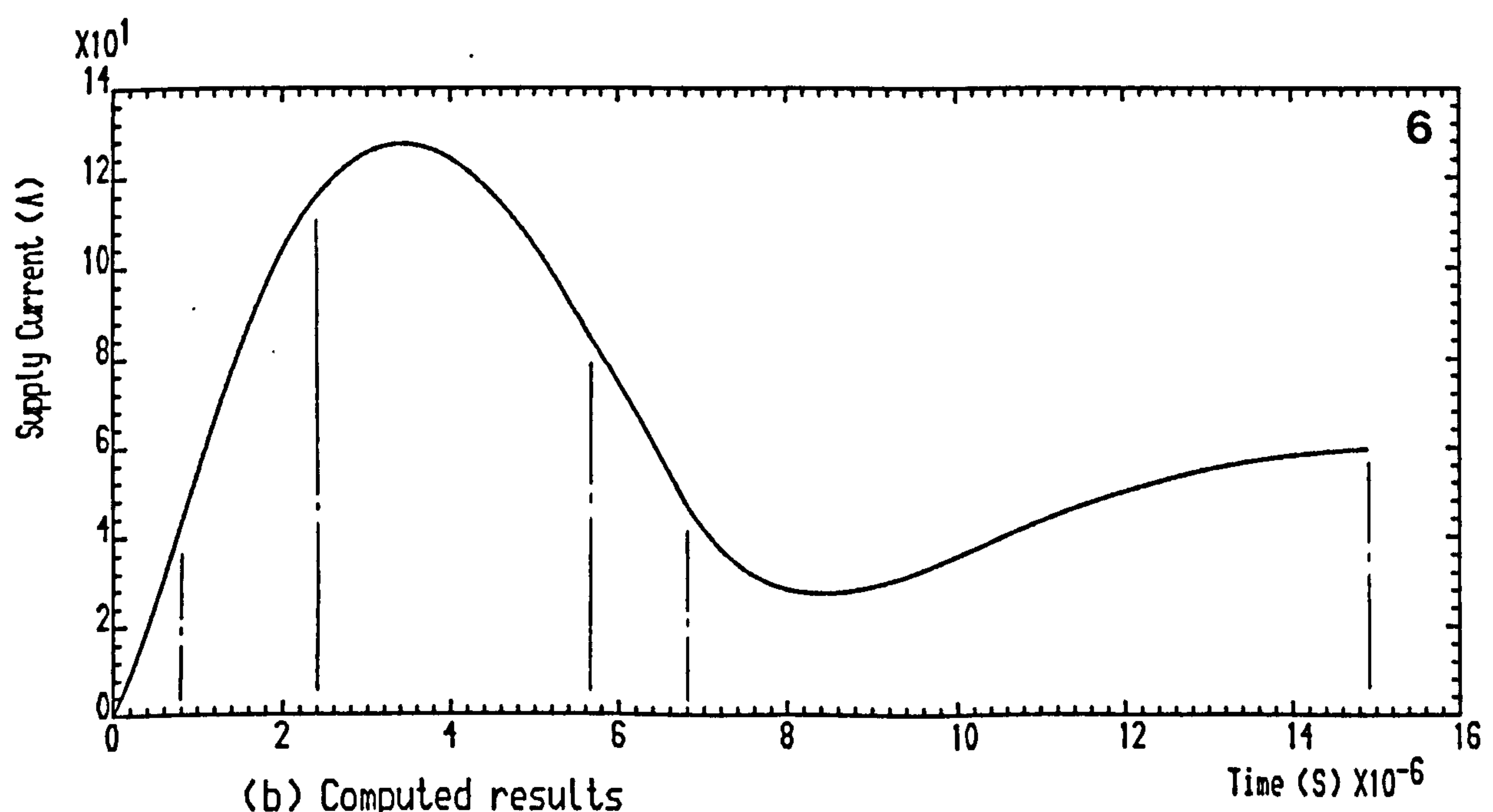
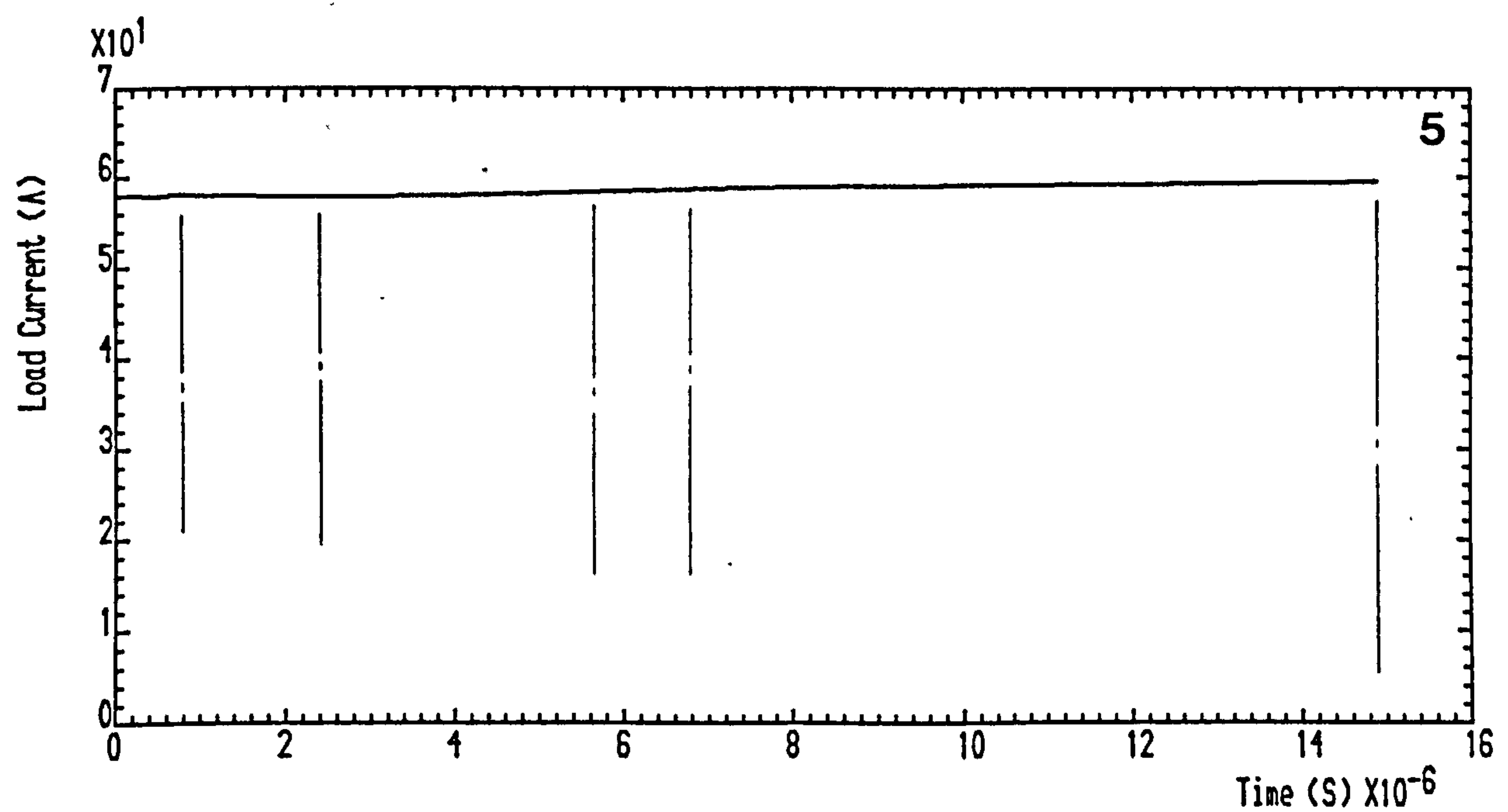
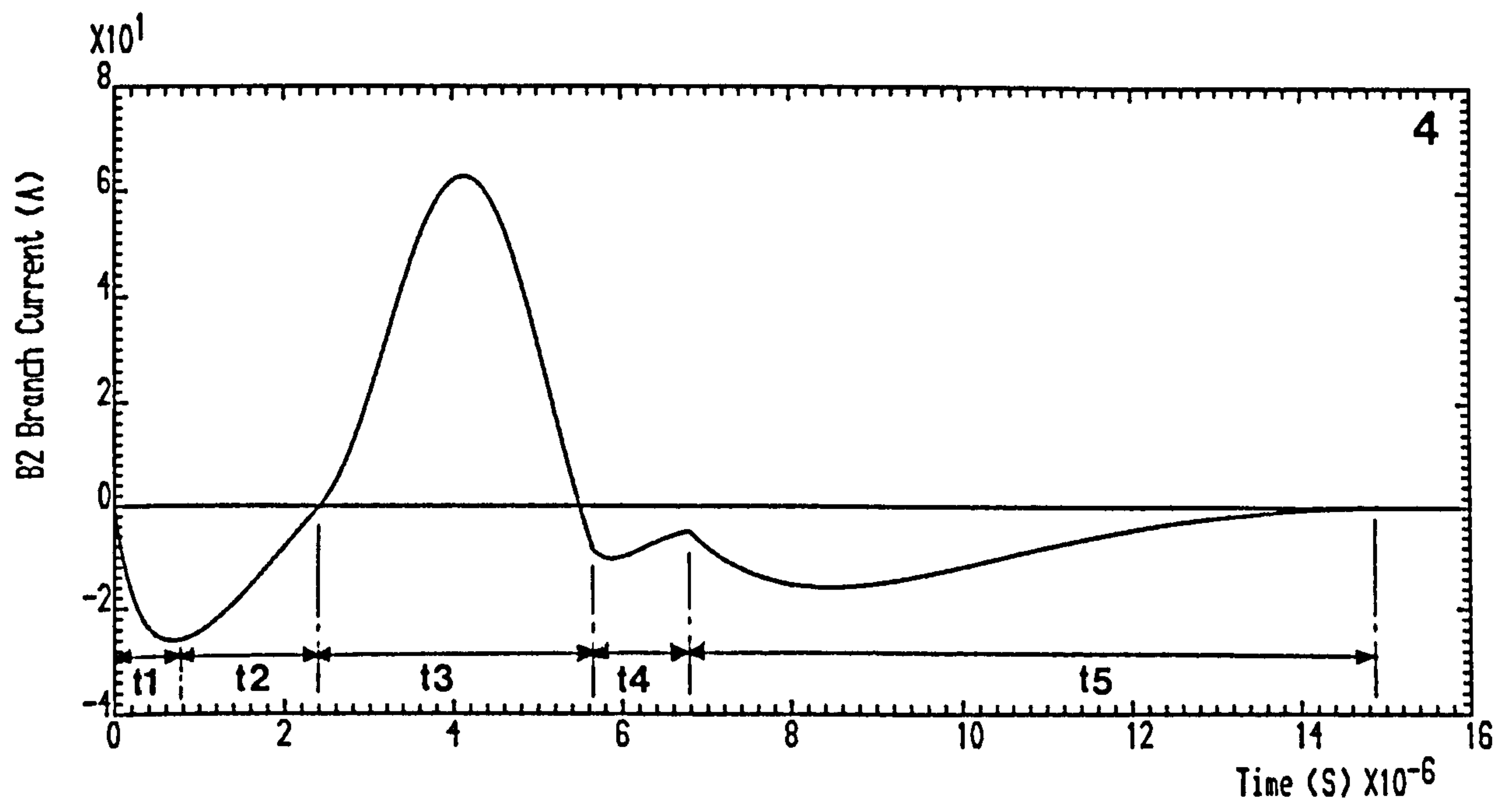


(b) Computed results

Figure 5.9 WaveForms at GTO A1 picking up load current From the Freewheeling path

CONTINUED ..

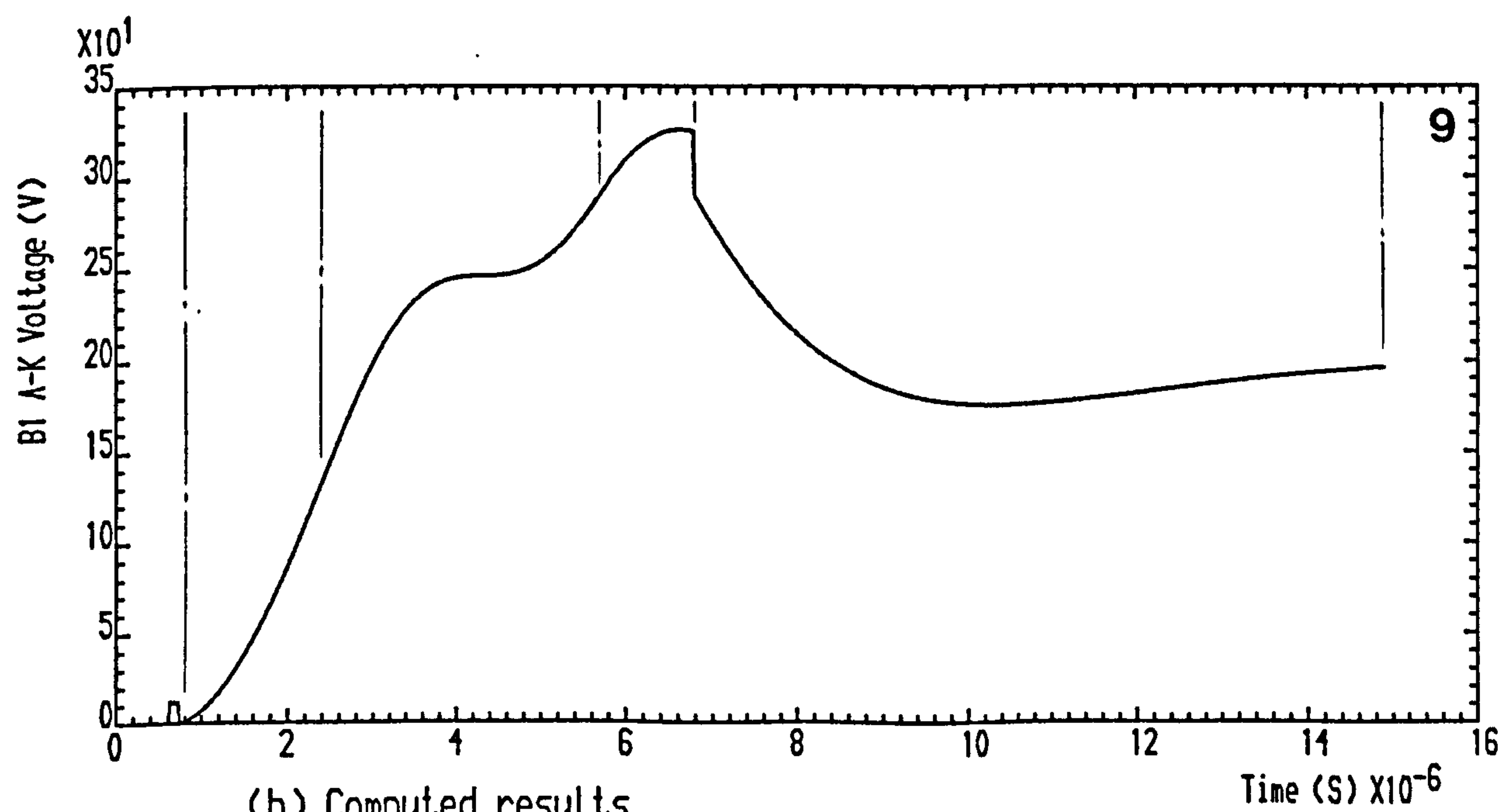
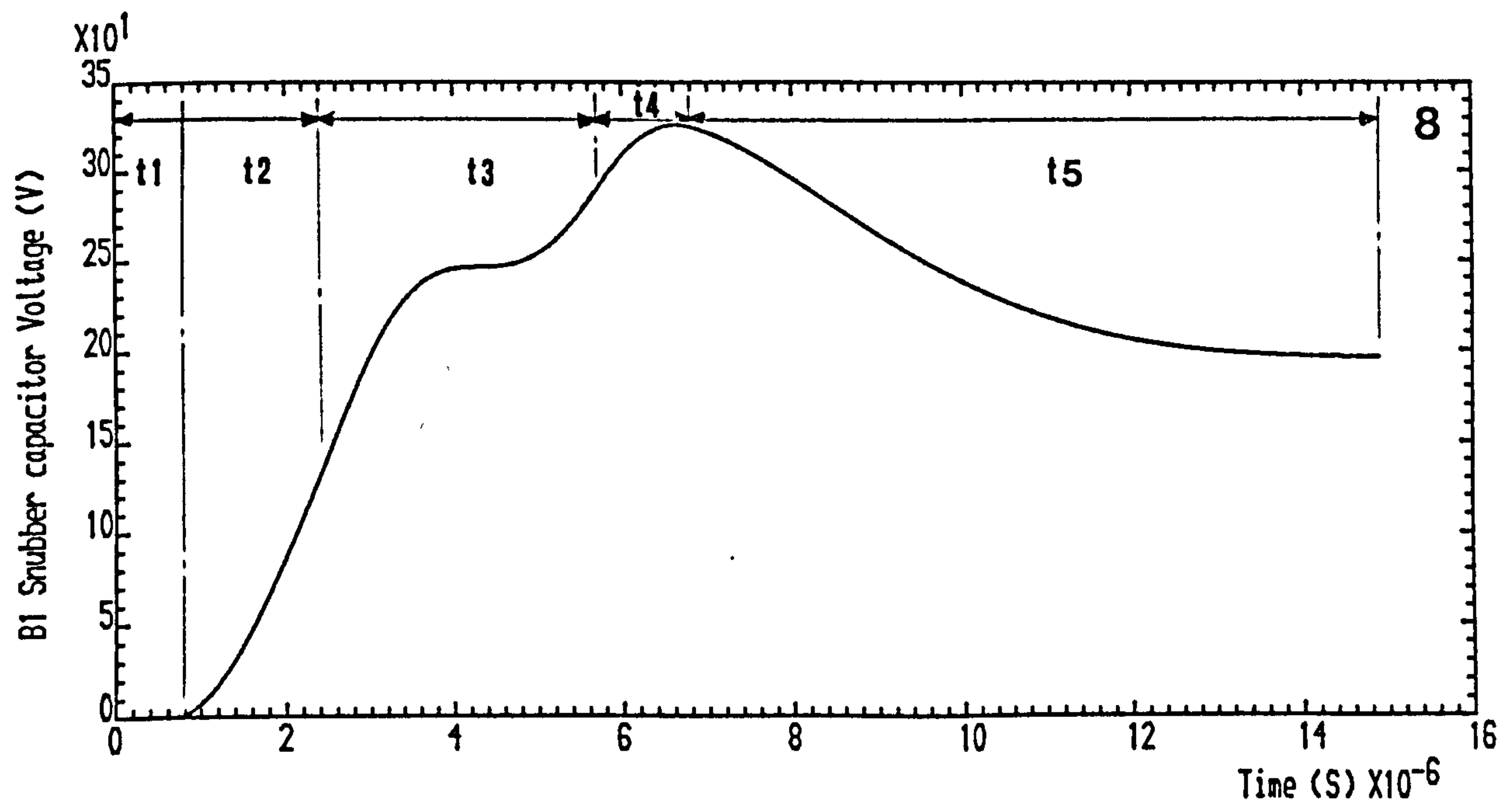
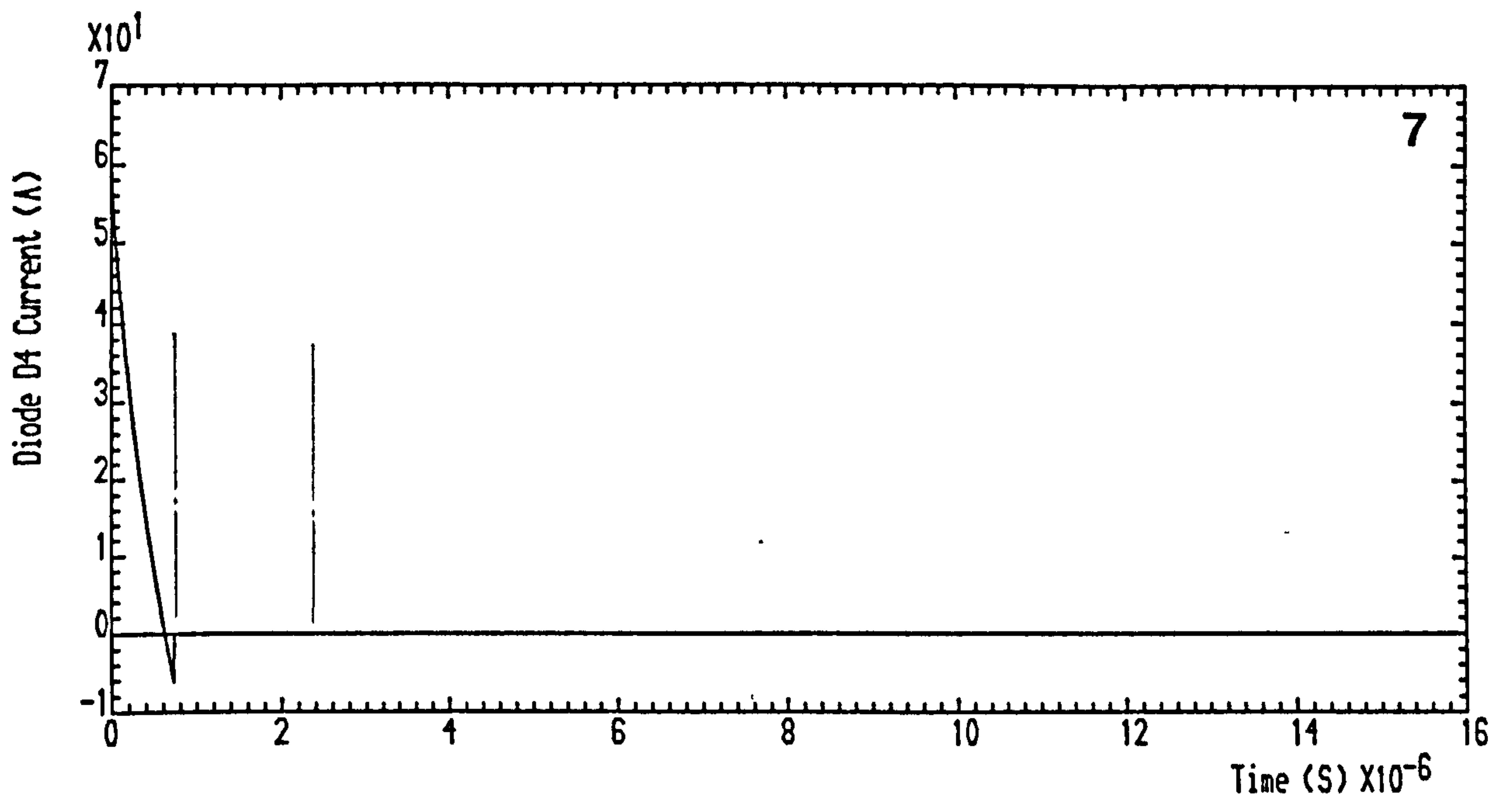




(b) Computed results

Figure 5.9 Waveforms at GTO A1 picking up load current from the Freewheeling path

CONTINUED ..



(b) Computed results

Figure 5.9 WaveForms at GTO A1 picking up load current from the Freewheeling path

CONTINUED ..



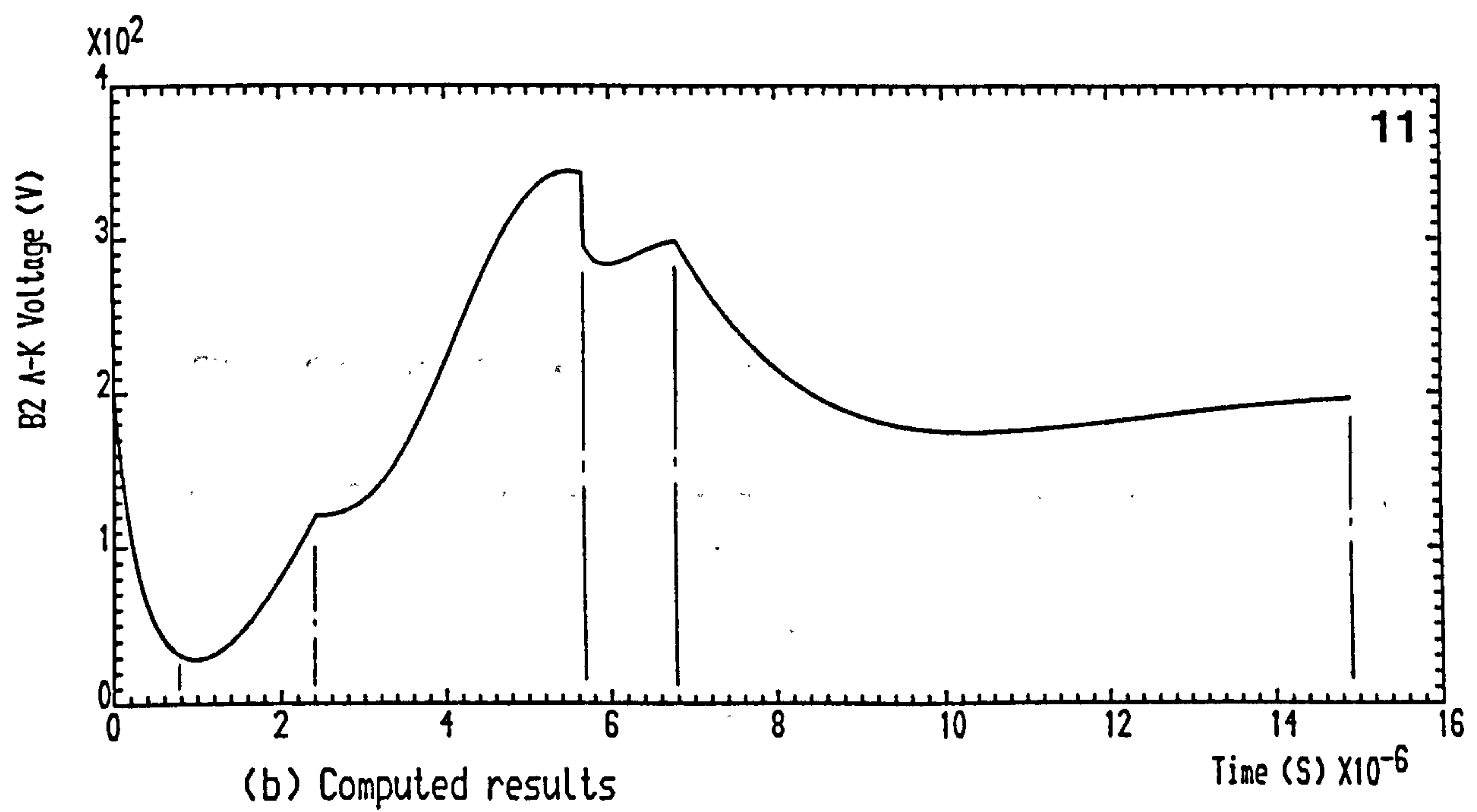
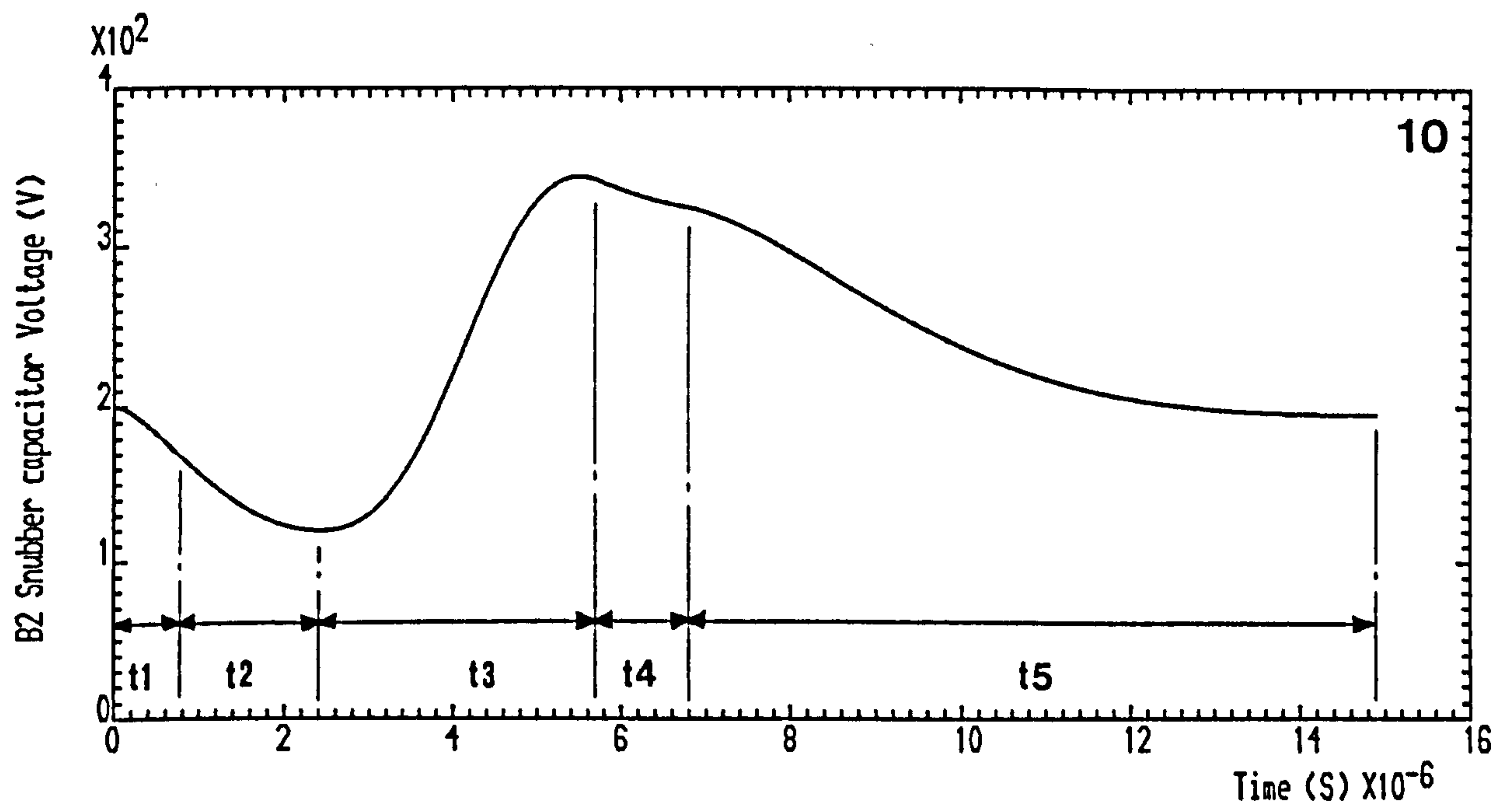


Figure 5.9 WaveForms at GTO A1 picking up load current from the Freewheeling path

END ..

transferred to the snubber resistor. Both B1 and B2 potentials subside to  $E_d$ , with the load current now rising, Figure 5.9, traces (9), (11) and (5). At the end of interval  $t_5$ , GTOs A1 and A2 are conducting the rising DC source supplied load current, with GTOs B1 and B2 each blocking  $E_d$ .

The DC source stray inductance  $L_d$  is found to be the main effective one, the others having lesser effects.

**b) Double GTO thyristor turn-on from feedback (Mode (2))**

Here the switching on, of the previously conducting pair A1 and A2 will revert the load voltage to its original polarity from the reversed polarity during feedback. This can also apply for the bridge operating as a DC chopper.

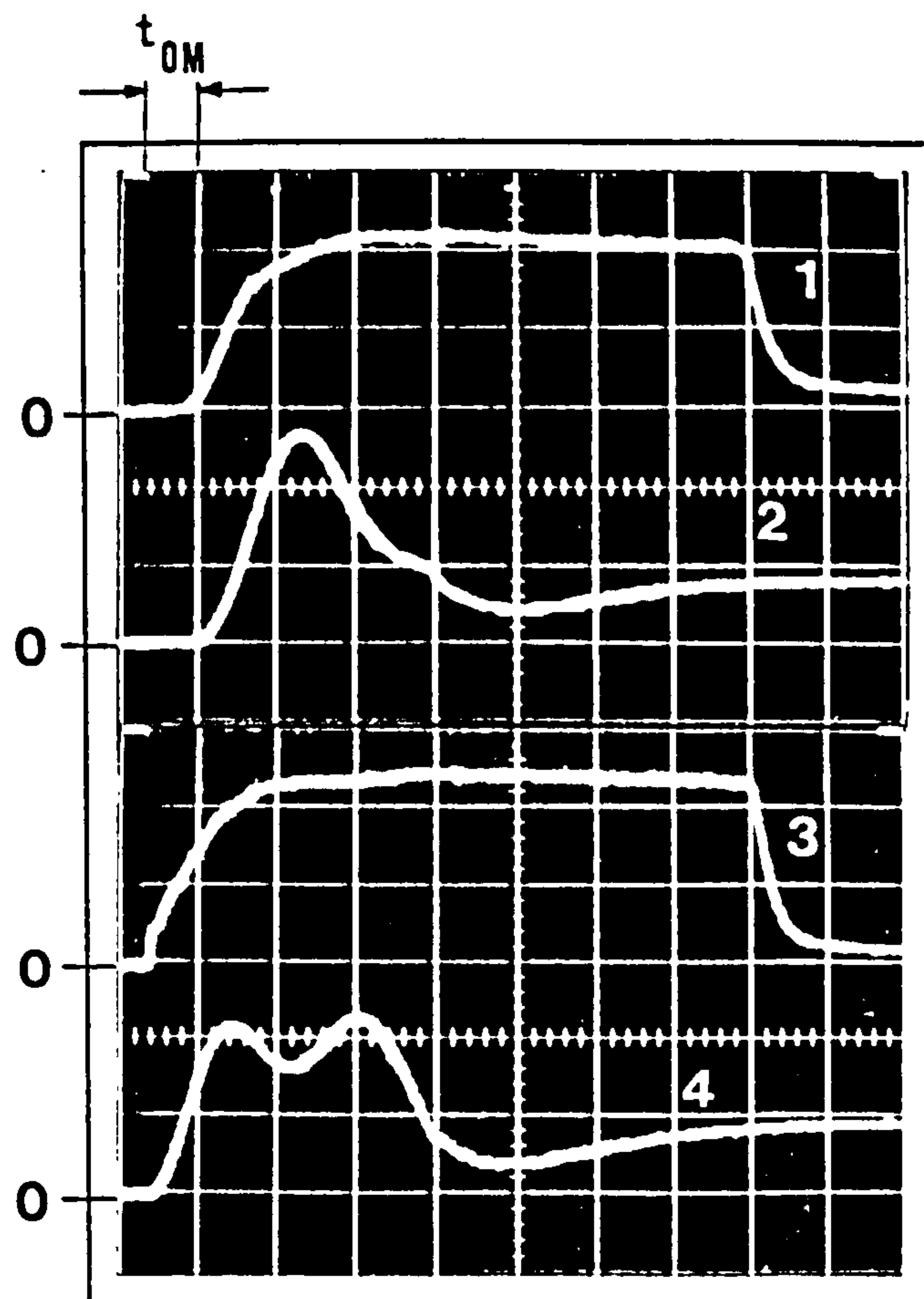
Unbalanced turn-on may be present. Here this occurred experimentally and is attributed to the difference in gate turn-on drive timing for GTOs A1 and A2, with the former being switched on approximately  $1\mu s$  after the latter. This effect, of which full details are given in the following description, is demonstrated in Figure 5.10.

**Interval  $t_1$ :** This interval commences as the A2 branch current starts rising, and ceases as GTO A1 turns-on. The equivalent circuit and matrix state equations are given in Figure 5.11(a) and (b) respectively. Figure 5.12 gives the experimental and the corresponding computed (black trace) waveforms.

Due to the turn-on time mismatch, GTO A2 switches on first, picking up the load current from diode D3, while its snubber capacitor discharges round the local loop formed through the snubber resistor. The feedback current through the supply now decays oscillatorily in  $L_d$ , the induced voltage across which depresses the DC rail voltage causing a slight oscillatory discharge of the A1 snubber capacitor through diode D4 and the source, Figure 5.12, traces (6) and (8). If balanced turn-on is assumed, diode D3 current will take longer to decay than that of diode D4 as illustrated in Figure 5.12(b), red traces (7) and (8), due to the presence of  $L_{d3}$  and  $L_{d4}$  in the bridge circuit. If these are negligibly small, a symmetrical bridge operation would result as shown in the predicted waveform of Figure 5.12(b) (green traces).

It is pure coincidence that diode D3 completes reverse recovery at the instant of A1





- |  |            |
|--|------------|
| (1) GTO A1 Initial-On Gate Current Pulse   | (5A/div.)  |
| (2) GTO A1 Anode Current + Snubber Current | (40A/div.) |
| (3) GTO A2 Initial-On Gate Current Pulse   | (5A/div.)  |
| (4) GTO A2 Anode Current + Snubber Current | (40A/div.) |

Time Scale: 2  $\mu$ S/div.

Figure 5.10 Turn-on gate drive time mismatch ( $t_{OM}$ ) during GTOs A1 and A2 turn-on together

turn-on (Figure 5.12, traces (1) and (7)). However, the voltage spike due to  $L_{D3}$  at this instant is also felt by GTO B2 (trace (12)).

Again consideration must be given to the potential danger of the transient shoot-through current caused by the overlapping GTO turn-on and diode reverse recovery in series across the DC rails.

Generally, the turn-on time mismatch results in the feedback diode of the same leg as the later turn-on GTO to conduct excess current. Dynamic overloading and possibly a

permanent damage of the diode may occur if it is operating near its peak rated current. Also due to this transient over-current, the diode experiences a higher reverse recovery current peak and longer reverse recovery time [31].

**Interval  $t_2$ :** This interval, the equivalent circuit and matrix state equations of which are shown respectively in Figure 5.11(c) and (d), lasts from the reverse recovery of diode D3 to the reverse recovery of diode D4. GTO A1 now being switched on, picks up the load current from diode D4, with its snubber capacitor commencing its local discharge. B2 snubber capacitor now charges through A2 and the DC source, Figure 5.12, traces (1), (4) and (11).

The load current is maintained constant during this interval (trace (5)).

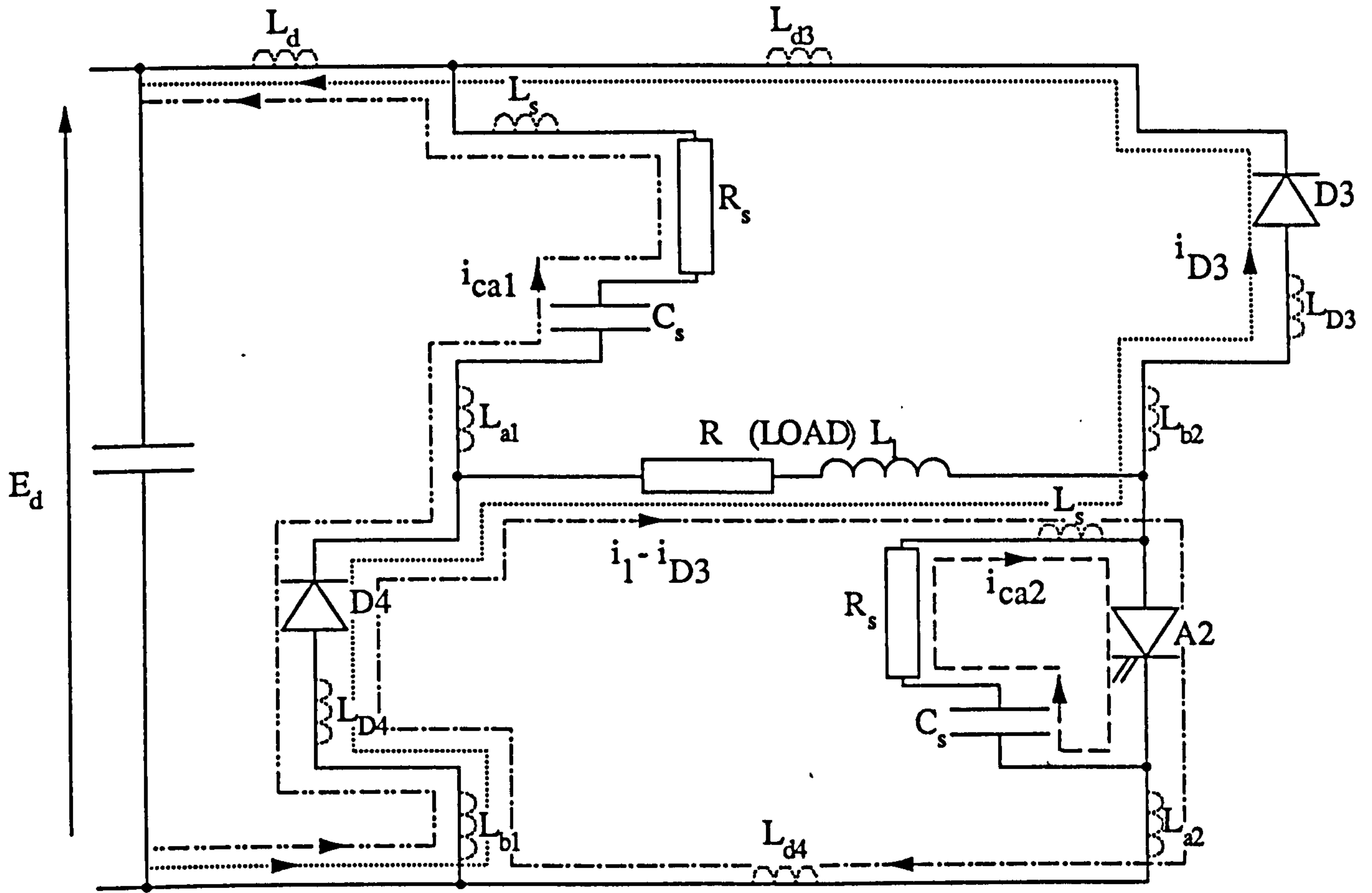
**Interval  $t_3$ :** Diode D4 having reverse recovered, indicates the start of  $t_3$ , the equivalent circuit and matrix state equations of which are given respectively in Figure 5.11(e) and (f). This ends at the B2 snubber diode reverse recovery. B1 snubber capacitor charges and its voltage reaches  $E_d$  prior to that of B2 snubber capacitor, after which, both overshoot  $E_d$ , Figure 5.12, traces (9) and (11).

The oscillatory charging of B1 and B2 snubber capacitors is principally controlled by  $L_d$  (ignoring the  $L_{d3}$  and  $L_{d4}$  small effects) (traces (3) and (4)). The B2 snubber capacitor acquires its full charge first (traces (11) and (9)), thereafter experiencing a slight discharge as the snubber diode reverse recovers. The load current is then rising slightly (trace (5)).

**Interval  $t_4$ :** The equivalent circuit and matrix state equations of interval  $t_4$ , which lasts from the reverse recovery of B2 snubber diode to the reverse recovery of B1 snubber diode, become those of Figure 5.11(g) and (h) respectively. As before, the over-voltage across GTO B1 causes the hold-up effect on GTO B2, Figure 5.12, traces (10) and (12).

**Interval  $t_5$ :** The beginning of this interval is indicated by the transfer of B1 snubber diode reverse recovery current to the associated resistor; it ends when this current has decayed to zero. The equivalent circuit and state equations are shown in Figure 5.11(i) and (j) respectively. Both GTO B1 and B2 potentials decay to  $E_d$  as the discharge current of their snubber capacitors falls to zero, Figure 5.12, traces (10), (12), (3) and (4).



Time interval t1

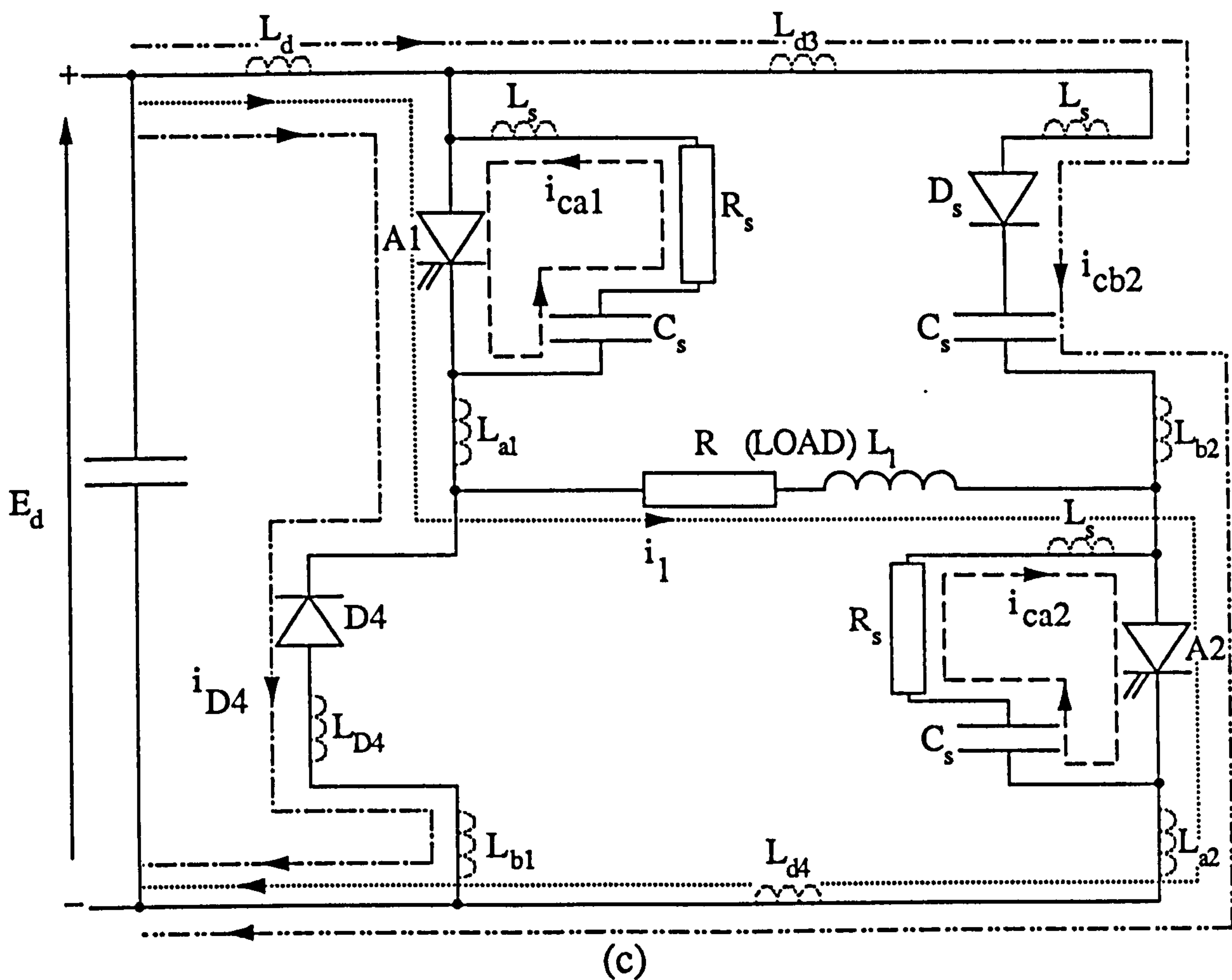
(a)

COLUMNS	(1)	(2)	(3)	(4)	(5)	(6)		
$p i_{ca1}$	$-\frac{R_s L_7}{L_1}$	0	0	$\frac{R L_6}{L_1}$	$\frac{L_7}{L_1}$	0	$i_{ca1}$	$E_d \frac{L_5}{L_1}$
$p i_{ca2}$	0	$-\frac{R_s}{L_s}$	0	0	0	$\frac{1}{L_s}$	$i_{ca2}$	0
$p i_{D3}$	$-\frac{R_s L_{11}}{L_8}$	0	0	$\frac{R L_{10}}{L_8}$	$\frac{L_{11}}{L_8}$	0	$i_{D3}$	$E_d \frac{L_9}{L_8}$
$p i_1$	$\frac{R_s L_4}{L_1}$	0	0	$-\frac{R L_3}{L_1}$	$-\frac{L_4}{L_1}$	0	$i_1$	$-E_d \frac{L_2}{L_1}$
$p v_{ca1}$	$-\frac{1}{C_s}$	0	0	0	0	0	$v_{ca1}$	0
$p v_{ca2}$	0	$-\frac{1}{C_s}$	0	0	0	0	$v_{ca2}$	0

(b)

Figure 5.11 Equivalent circuits and state equations matrices for GTOs A1 and A2 picking up load current from the feedback path (Unbalanced turn-on)

Time interval t2



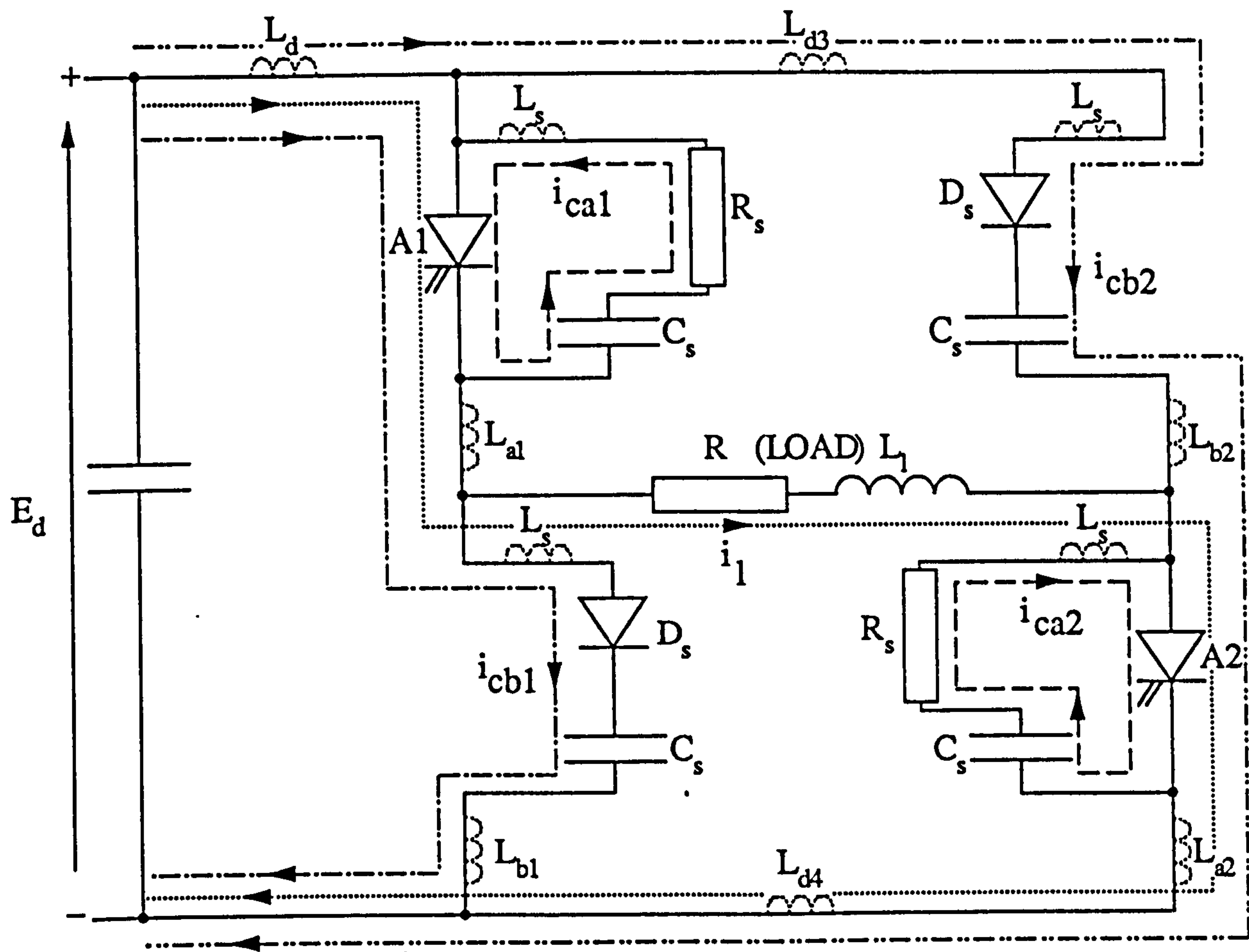
COLUMNS	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)		
$p i_{ca1}$	$-\frac{R_s}{L_s}$	$0$	$0$	$0$	$0$	$\frac{1}{L_s}$	$0$	$0$	$i_{ca1}$	$0$
$p i_{ca2}$	$0$	$-\frac{R_s}{L_s}$	$0$	$0$	$0$	$0$	$\frac{1}{L_s}$	$0$	$i_{ca2}$	$0$
$p i_{cb2}$	$0$	$0$	$0$	$0$	$\frac{RL_{14}}{L_{12}}$	$0$	$0$	$-\frac{L_{15}}{L_{12}}$	$i_{cb2}$	$E_d \frac{L_{13}}{L_{12}}$
$p i_{D4}$	$0$	$0$	$0$	$0$	$\frac{RL_{17}}{L_{12}}$	$0$	$0$	$-\frac{L_{25}}{L_{12}}$	$i_{D4}$	$E_d \frac{L_{16}}{L_{12}}$
$p i_1$	$0$	$0$	$0$	$0$	$-\frac{RL_{20}}{L_{18}}$	$0$	$0$	$\frac{L_{21}}{L_{18}}$	$i_1$	$E_d \frac{L_{19}}{L_{18}}$
$p v_{ca1}$	$-\frac{1}{C_s}$	$0$	$0$	$0$	$0$	$0$	$0$	$0$	$v_{ca1}$	$0$
$p v_{ca2}$	$0$	$-\frac{1}{C_s}$	$0$	$0$	$0$	$0$	$0$	$0$	$v_{ca2}$	$0$
$p v_{cb2}$	$0$	$0$	$\frac{1}{C_s}$	$0$	$0$	$0$	$0$	$0$	$v_{cb2}$	$0$

(d)

Figure 5.11 Equivalent circuits and state equations matrices for GTOs A1 and A2 picking up load current from the feedback path (Unbalanced turn-on)



Time interval t3

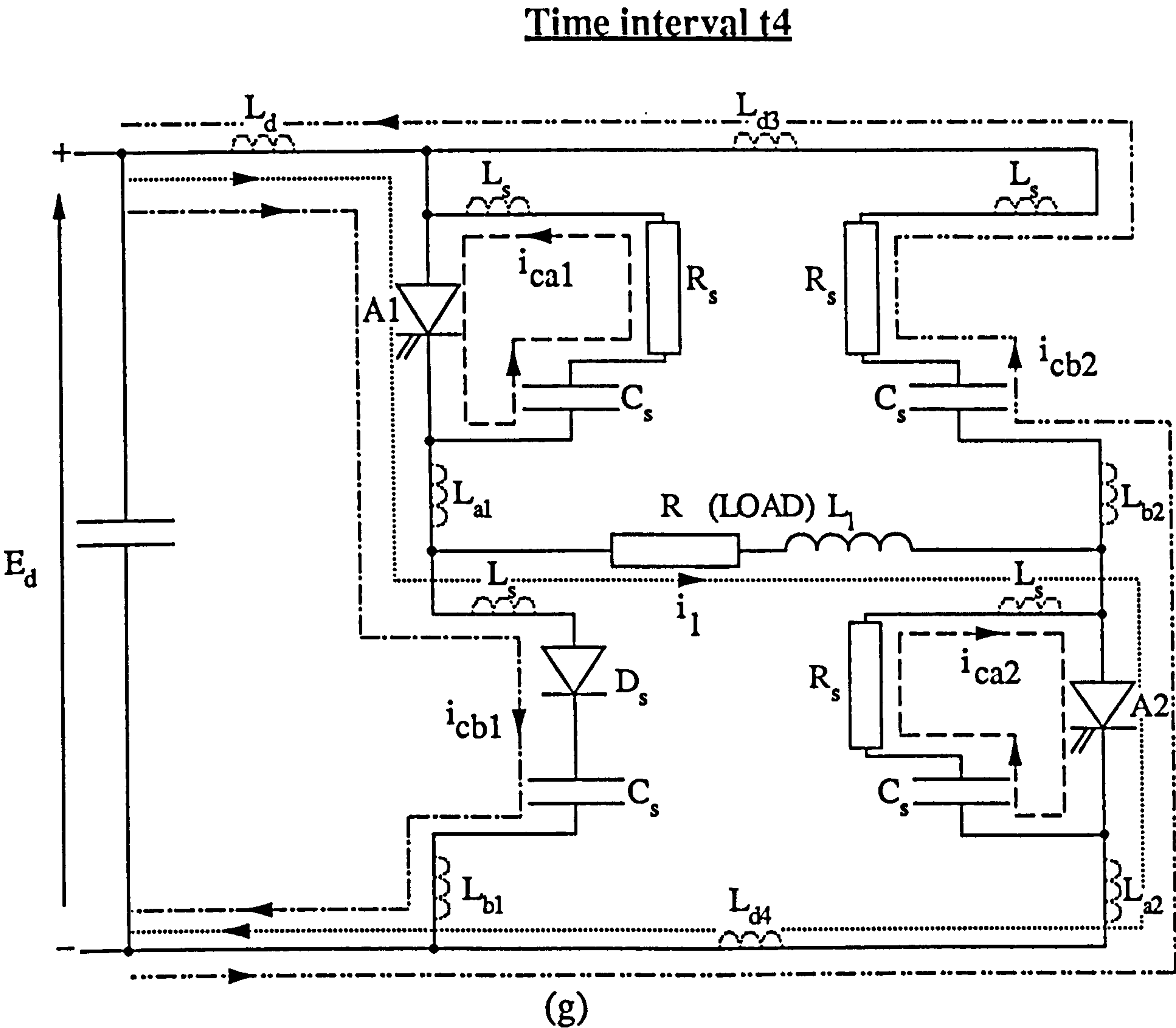


(e)

COLUMNS	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)		
$p i_{ca1}$	$-\frac{R_s}{L_s}$	0	0	0	0	$\frac{1}{L_s}$	0	0	0	$i_{ca1}$	0
$p i_{ca2}$	0	$-\frac{R_s}{L_s}$	0	0	0	0	$\frac{1}{L_s}$	0	0	$i_{ca2}$	0
$p i_{cb1}$	0	0	0	0	$\frac{RL_{28}}{L_{22}}$	0	0	$-\frac{L_{29}}{L_{22}}$	$-\frac{L_{25}}{L_{22}}$	$i_{cb1}$	$E_d \frac{L_{27}}{L_{22}}$
$p i_{cb2}$	0	0	0	0	$\frac{RL_{24}}{L_{22}}$	0	0	$-\frac{L_{25}}{L_{22}}$	$-\frac{L_{26}}{L_{22}}$	$i_{cb2}$	$E_d \frac{L_{23}}{L_{22}}$
$p i_1$	0	0	0	0	$-\frac{RL_{32}}{L_{30}}$	0	0	$\frac{L_{33}}{L_{30}}$	$\frac{L_{34}}{L_{30}}$	$i_1$	$E_d \frac{L_{31}}{L_{30}}$
$p v_{ca1}$	$-\frac{1}{C_s}$	0	0	0	0	0	0	0	0	$v_{ca1}$	0
$p v_{ca2}$	0	$-\frac{1}{C_s}$	0	0	0	0	0	0	0	$v_{ca2}$	0
$p v_{cb1}$	0	0	$\frac{1}{C_s}$	0	0	0	0	0	0	$v_{cb1}$	0
$p v_{cb2}$	0	0	0	$\frac{1}{C_s}$	0	0	0	0	0	$v_{cb2}$	0

(f)

Figure 5.11    Equivalent circuits and state equations matrices for GTOs A1 and A2 picking up load current from the feedback path (Unbalanced turn-on).



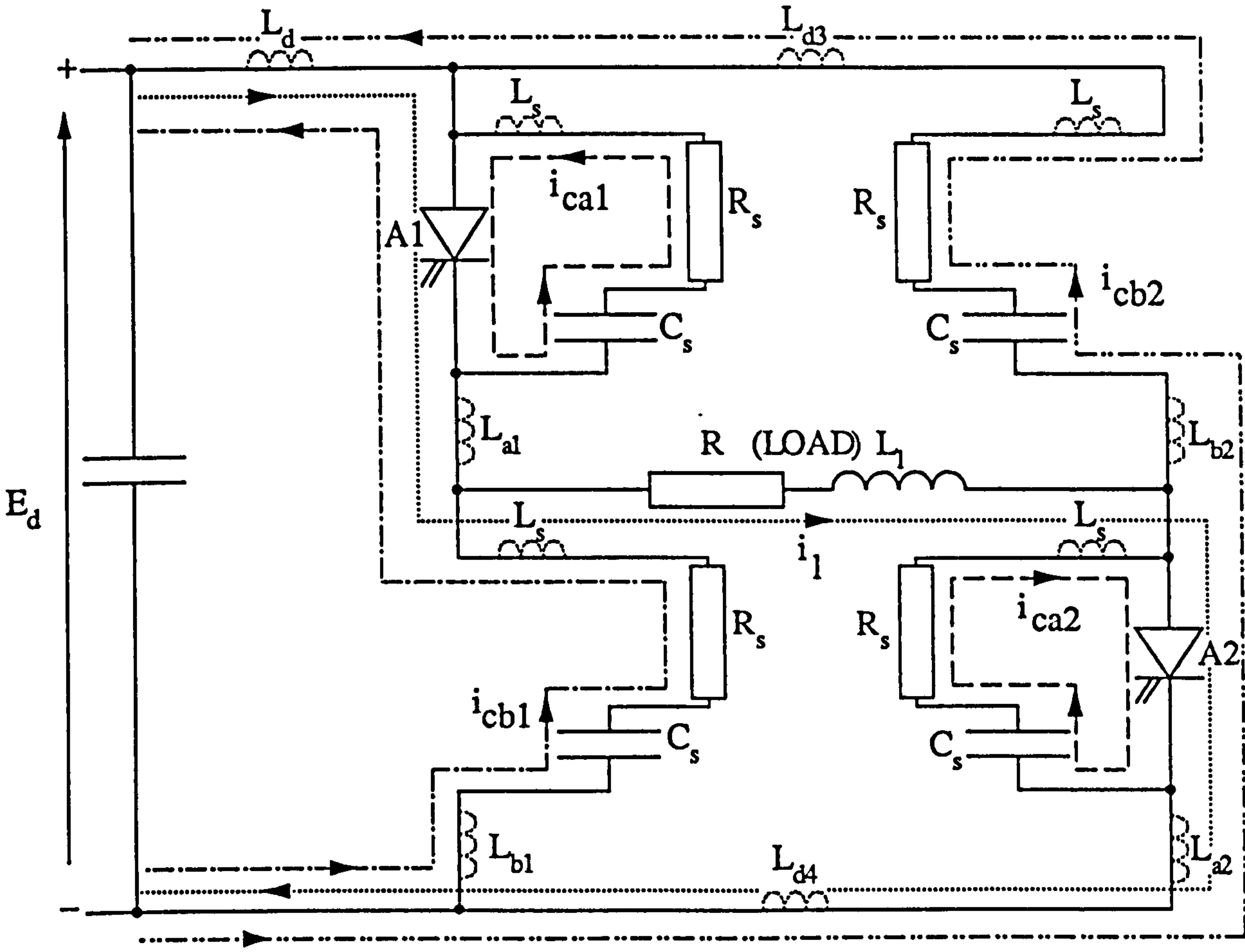
COLUMNS	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)
$\begin{bmatrix} p i_{ca1} \\ p i_{ca2} \\ p i_{cb1} \\ p i_{cb2} \\ p i_l \\ p v_{ca1} \\ p v_{ca2} \\ p v_{cb1} \\ p v_{cb2} \end{bmatrix}$	$= \begin{bmatrix} 0 \\ 0 \\ -\frac{R_s L_{25}}{L_{22}} \\ -\frac{R_s L_{26}}{L_{22}} \\ \frac{R_s L_{34}}{L_{30}} \\ 0 \\ 0 \\ 0 \\ \frac{1}{C_s} \end{bmatrix}$								
					<p>(Columns 1 to 3 and 5 to 9 as in (f))</p>				
					$+ \begin{bmatrix} i_{ca1} \\ i_{ca2} \\ i_{cb1} \\ i_{cb2} \\ i_l \\ v_{ca1} \\ v_{ca2} \\ v_{cb1} \\ v_{cb2} \end{bmatrix}$				

(h)

Figure 5.11    Equivalent circuits and state equations matrices for GTOs A1 and A2 picking up load current from the feedback path (Unbalanced turn-on).



Time interval  $t_5$



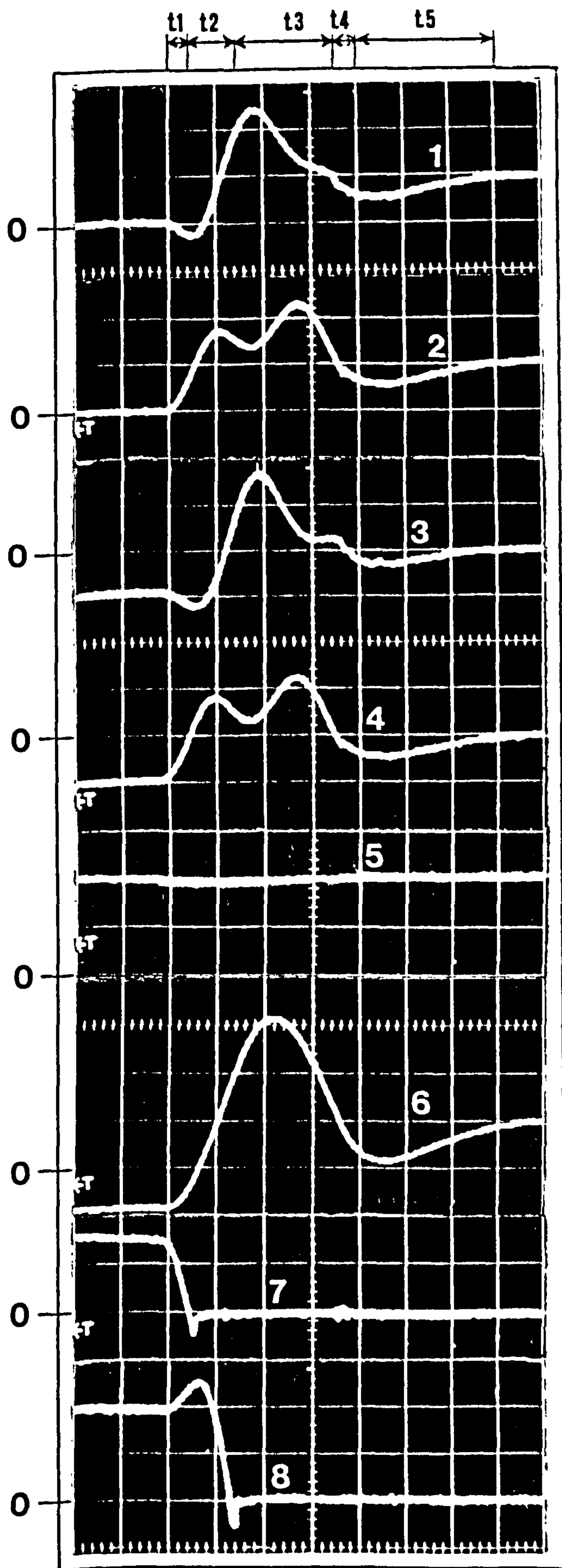
(i)

COLUMNS	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)
$\begin{bmatrix} p i_{ca1} \\ p i_{ca2} \\ p i_{cb1} \\ p i_{cb2} \\ p i_1 \\ p v_{ca1} \\ p v_{ca2} \\ p v_{cb1} \\ p v_{cb2} \end{bmatrix}$	$= \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ -\frac{R_s L_{29}}{L_{22}} & -\frac{R_s L_{25}}{L_{22}} \\ -\frac{R_s L_{25}}{L_{22}} & -\frac{R_s L_{26}}{L_{22}} \\ \frac{R_s L_{33}}{L_{22}} & \frac{R_s L_{34}}{L_{30}} \\ 0 & 0 \\ 0 & 0 \\ \frac{1}{C_s} & 0 \\ 0 & \frac{1}{C_s} \end{bmatrix}$					$\begin{bmatrix} i_{ca1} \\ i_{ca2} \\ i_{cb1} \\ i_{cb2} \\ i_1 \\ v_{ca1} \\ v_{ca2} \\ v_{cb1} \\ v_{cb2} \end{bmatrix}$	$+ \begin{bmatrix} 0 \\ 0 \\ E_d \frac{L_{27}}{L_{22}} \\ E_d \frac{L_{23}}{L_{22}} \\ E_d \frac{L_{31}}{L_{30}} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$		

(Columns 1, and 5 to 9 as in (f))

(j)

Figure 5.11    Equivalent circuits and state equations matrices for GTOs A1 and A2 picking up load current from the feedback path (Unbalanced turn-on).



(1) GTO A1 Branch Current  
(40A/div.)

(2) GTO A2 Branch Current  
(40A/div.)

(3) GTO B1 Branch Current  
(40A/div.)

(4) GTO B2 Branch Current  
(40A/div.)

(5) Load Current  
(40A/div.)

(6) Supply Current  
(40A/div.)

(7) Diode D3 Current  
(25A/div.)

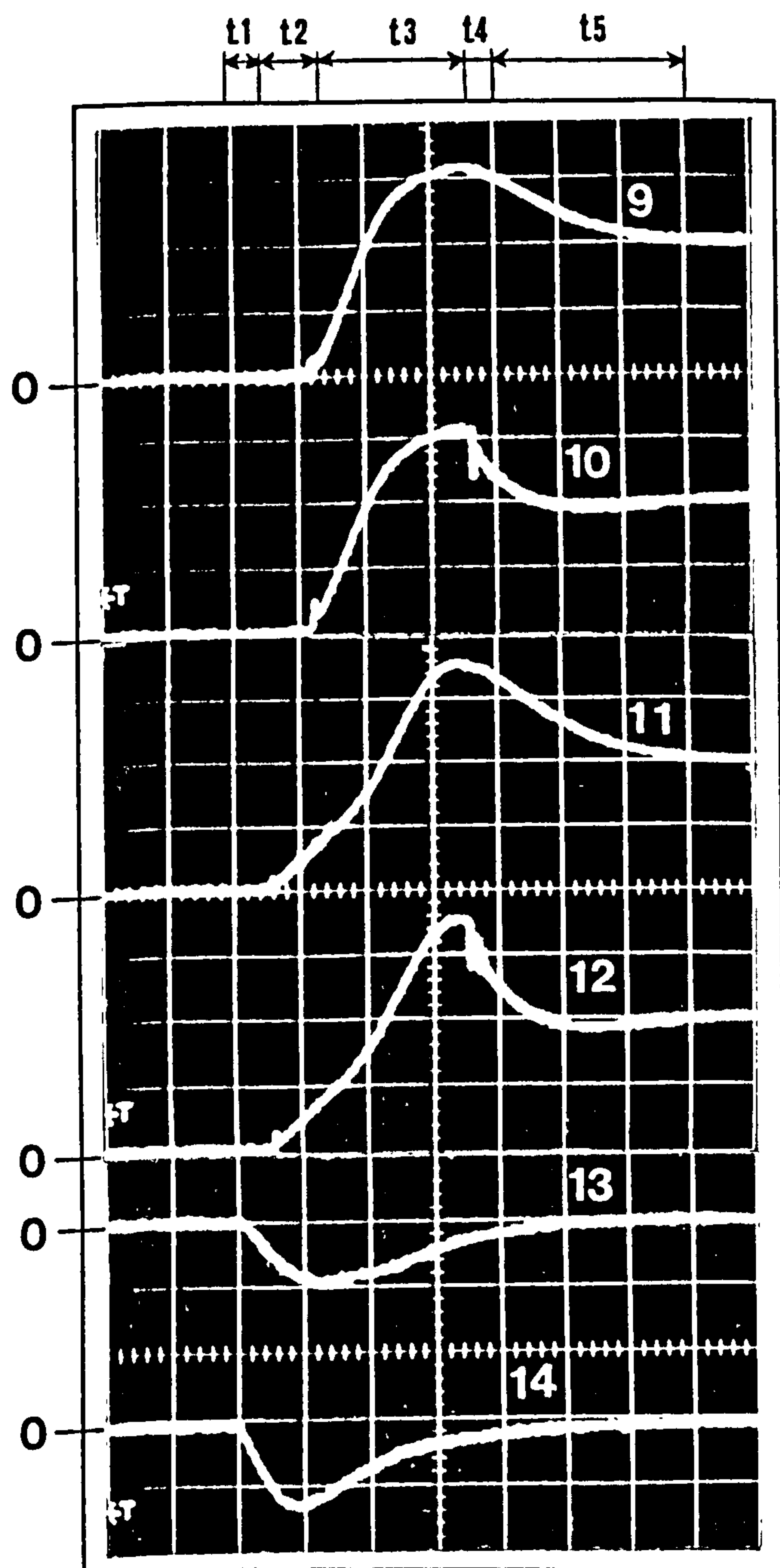
(8) Diode D4 Current  
(20A/div.)

Time Scale: 2μS/div.

(a) Experimental Results

Figure 5.12 Waveforms at GTOs A1 and A2 picking up load current from the feedback path





- (9) B1 Snubber Capacitor Voltage  
(100V/div.)
- (10) GTO B1 A-K Voltage  
(100V/div.)
- (11) B2 Snubber Capacitor Voltage  
(100V/div.)
- (12) GTO B2 A-K Voltage  
(100V/div.)
- (13) A1 Snubber Capacitor Current  
(20A/div.)
- (14) A2 Snubber Capacitor Current  
(20A/div.)

Time Scale: 2  $\mu$ S/div.

(a) Experimental Results

Figure 5.12 Waveforms at GTOs A1 and A2 picking up load current from the feedback path



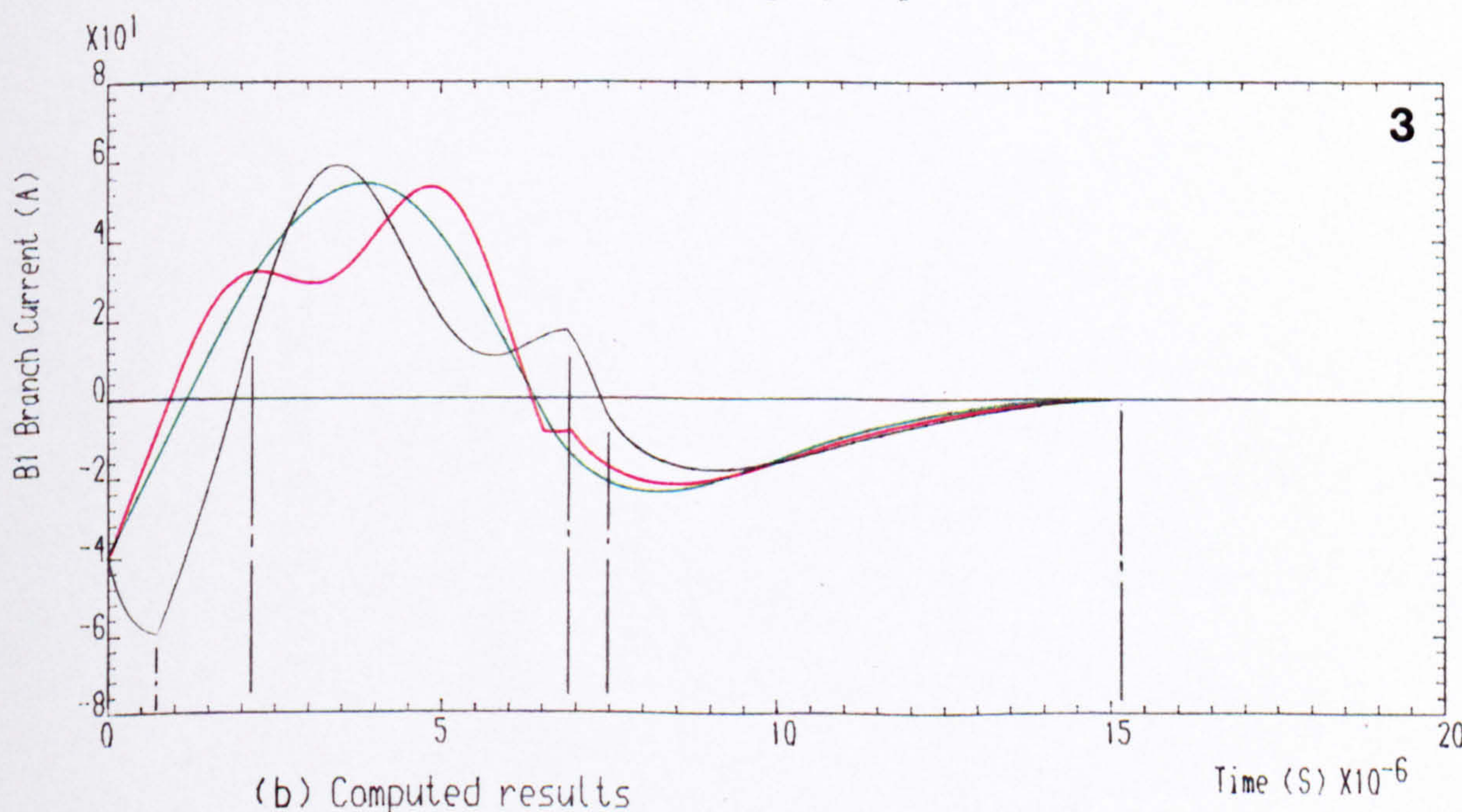
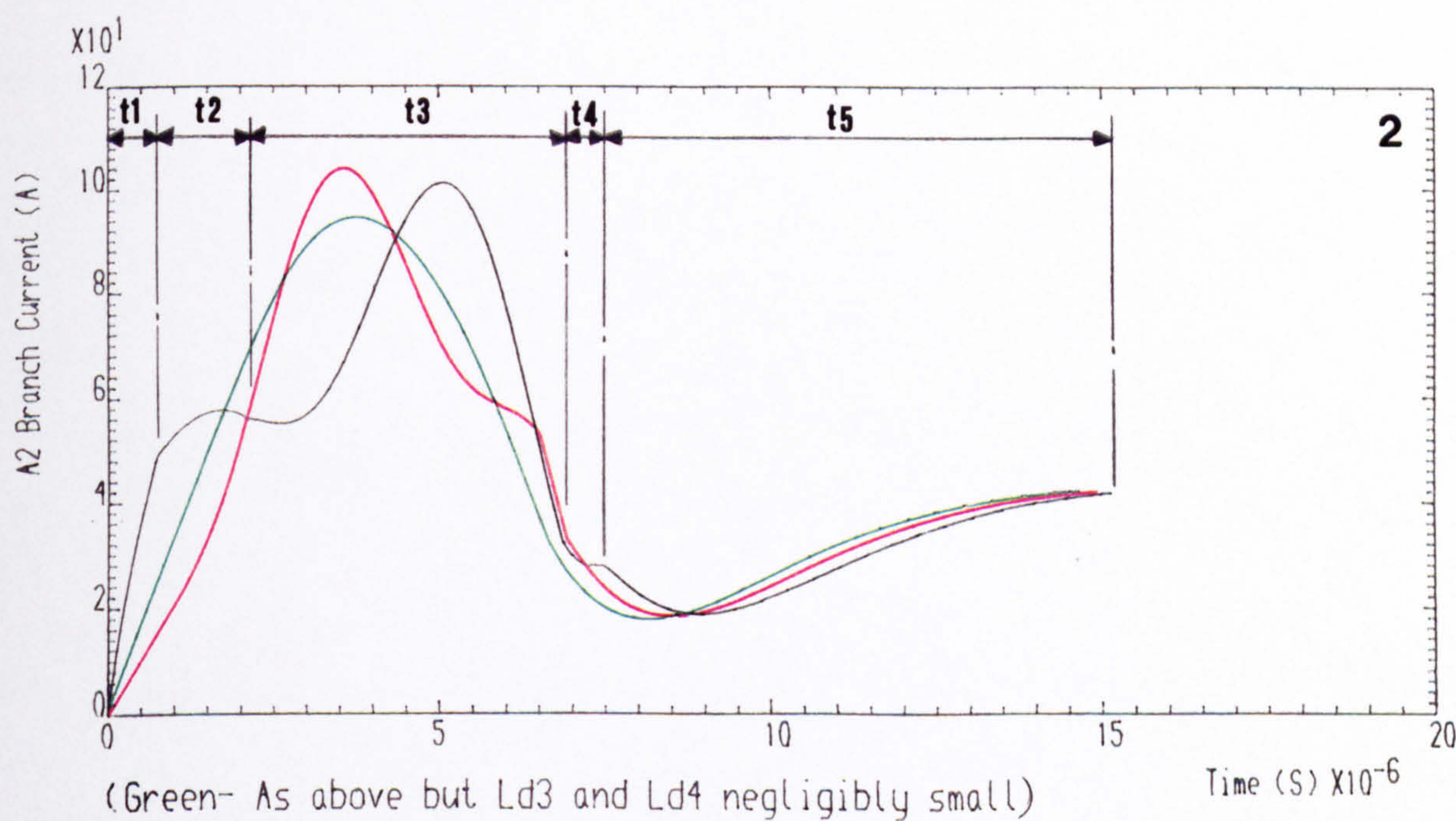
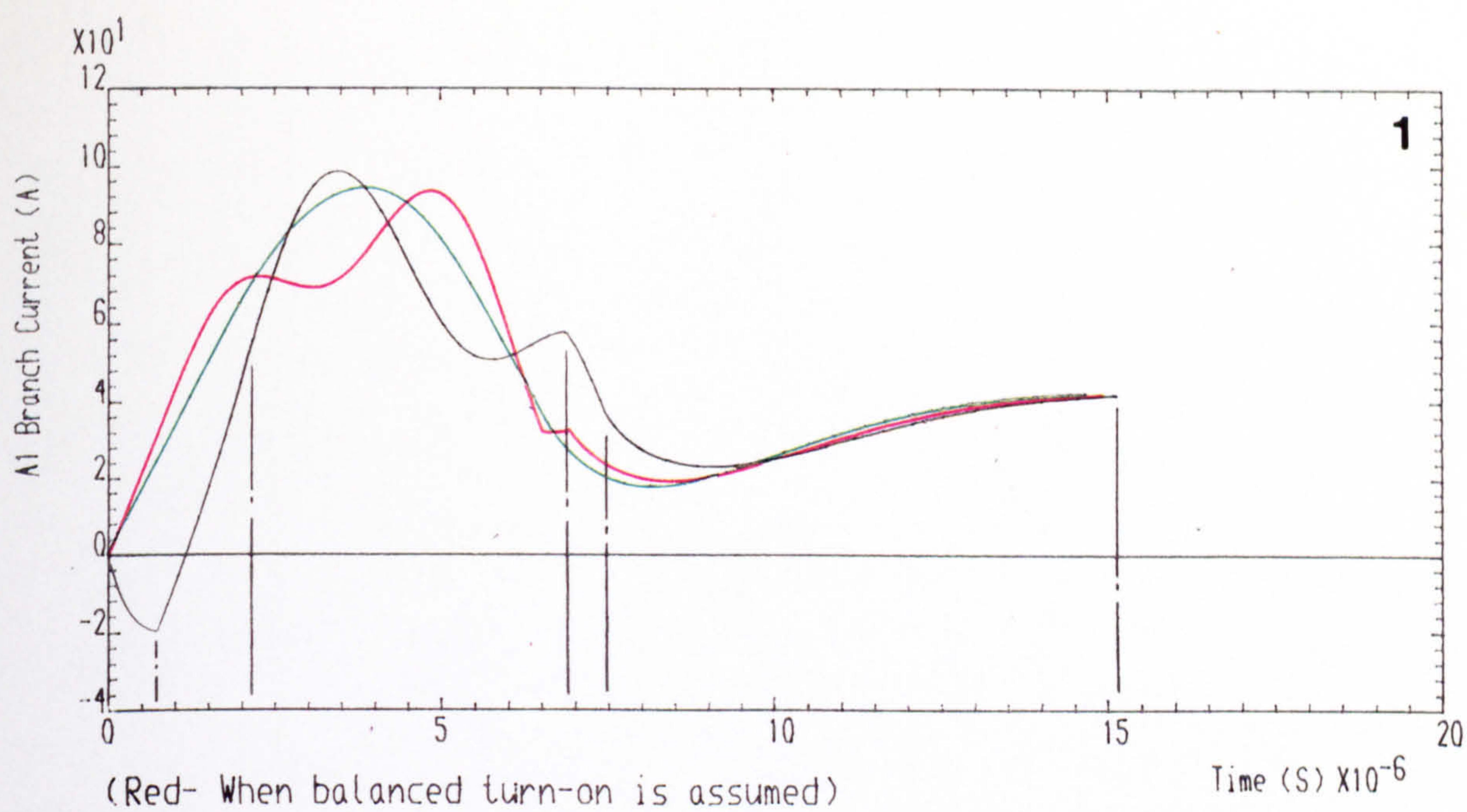


Figure 5.12 Waveforms at GTOs A1 and A2 picking up load current from the feedback path with unbalanced turn-on (Black) CONTINUED ..



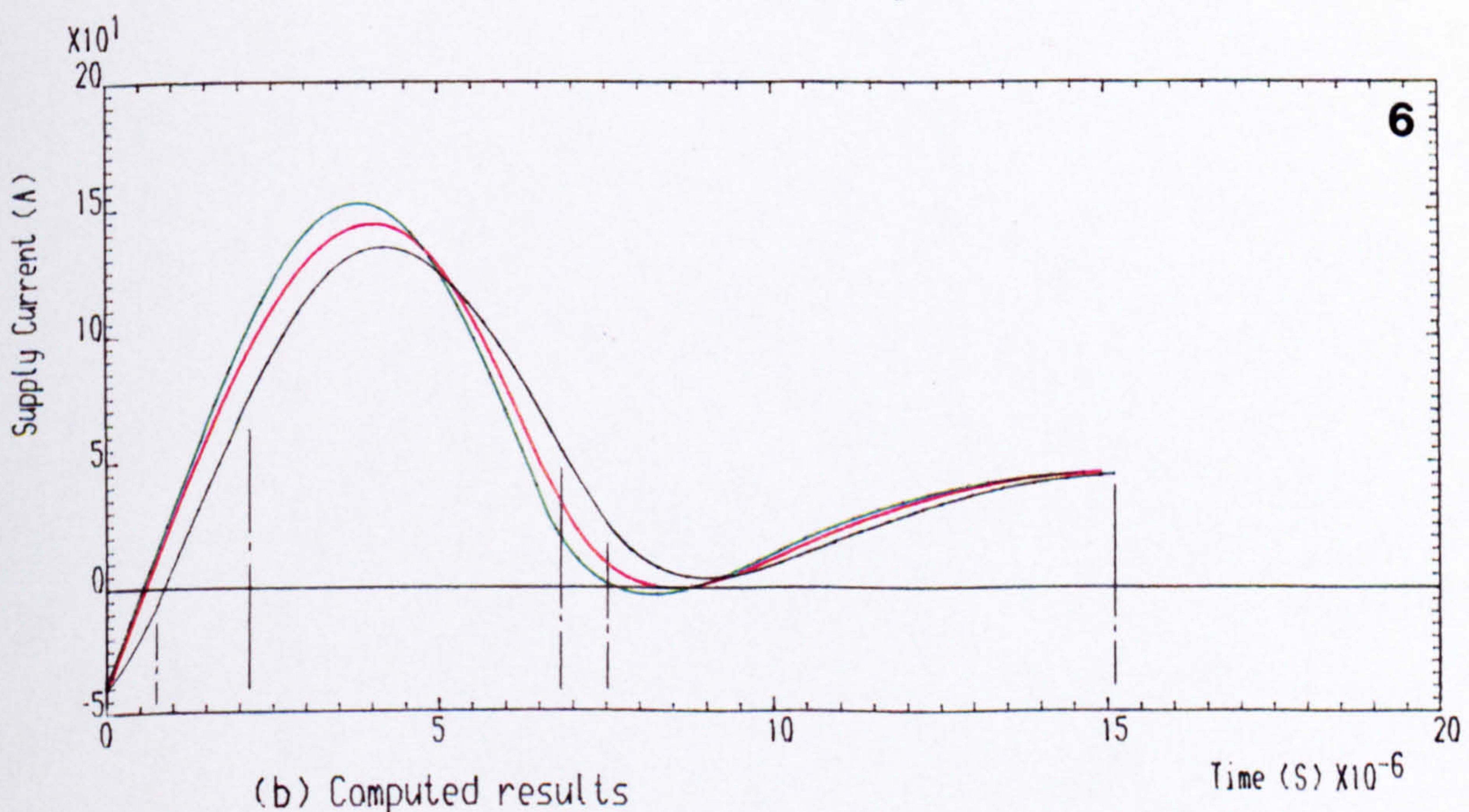
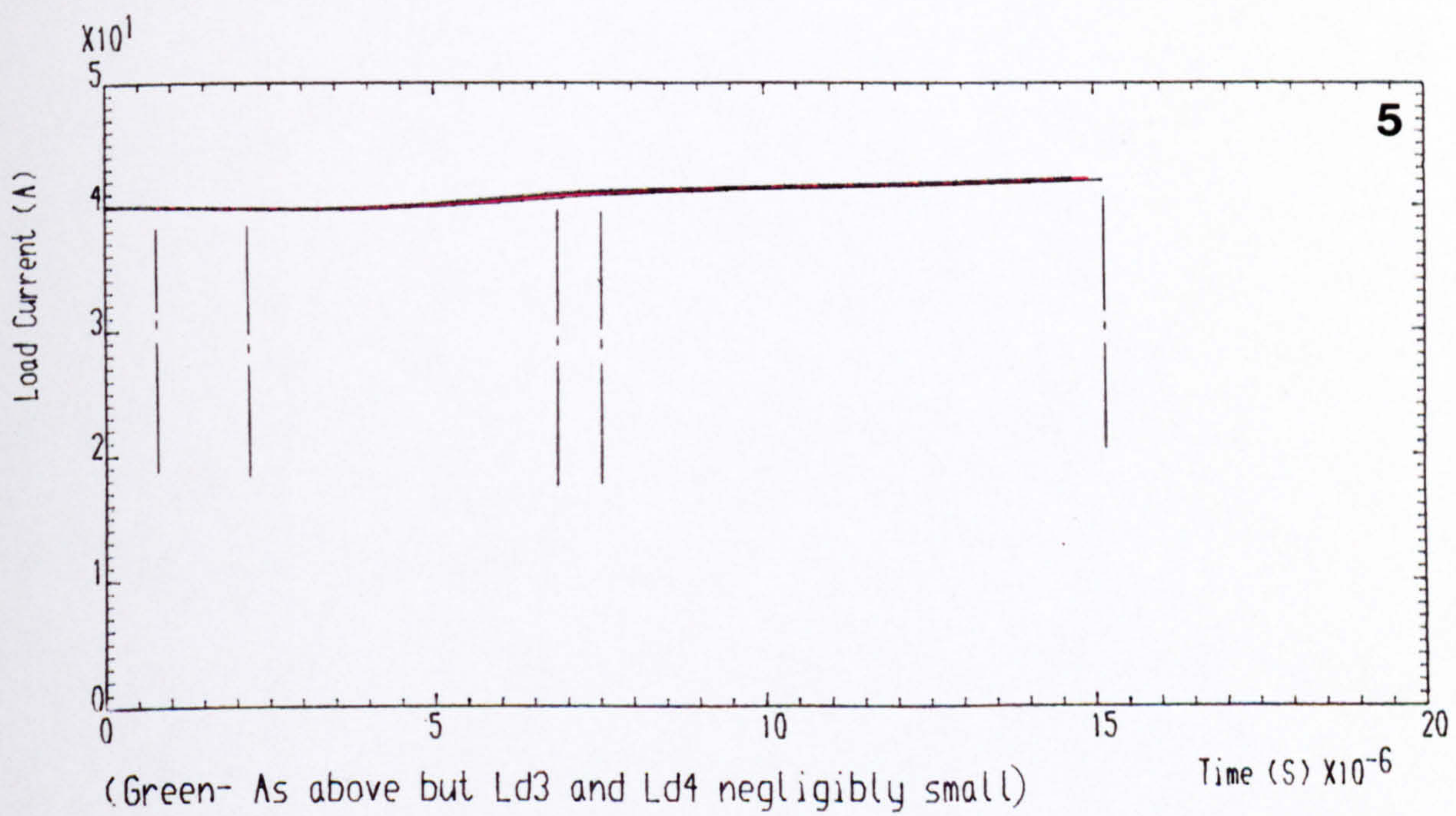
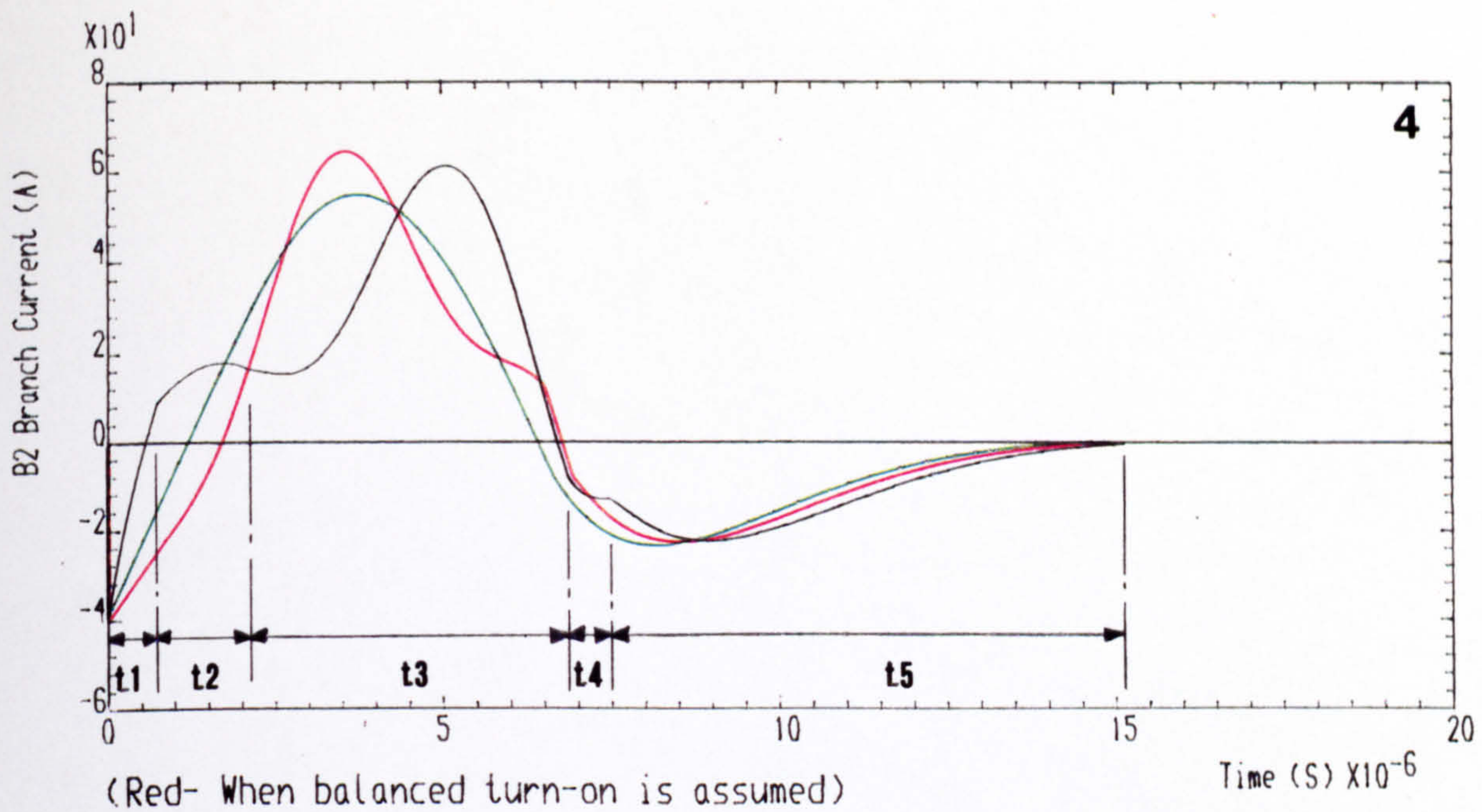


Figure 5.12 Waveforms at GTOs A1 and A2 picking up load current from the feedback path with unbalanced turn-on (Black) CONTINUED ..



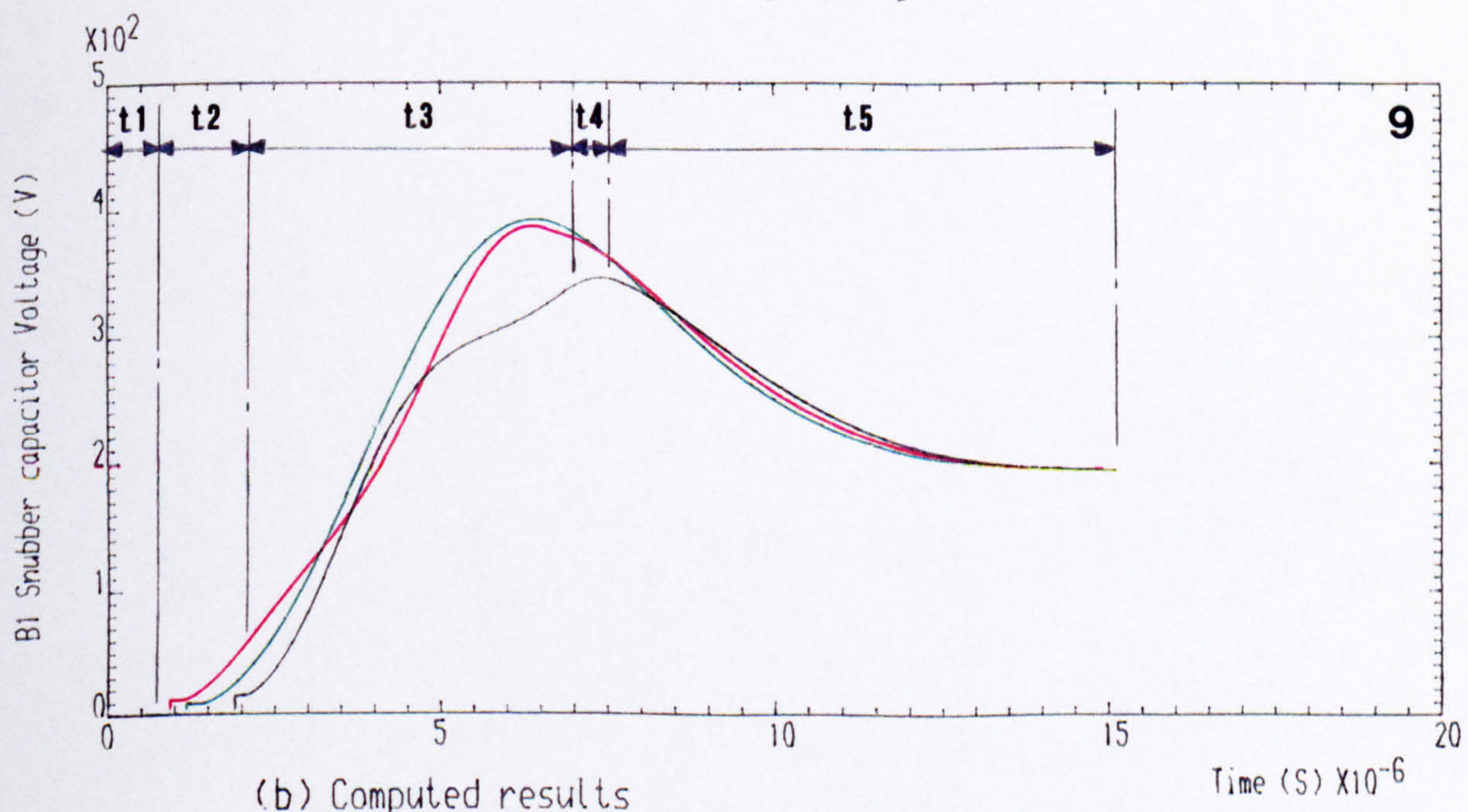
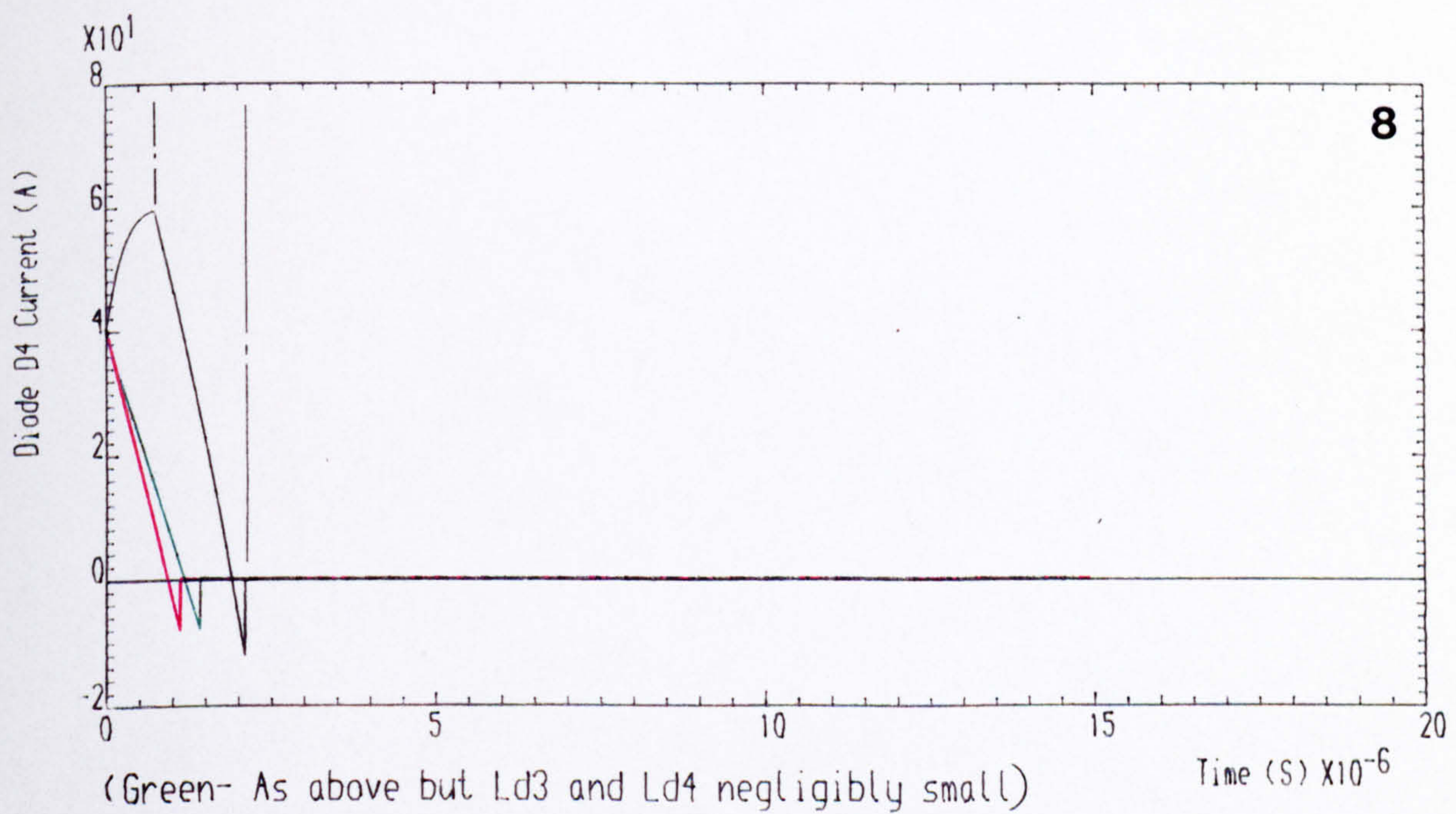
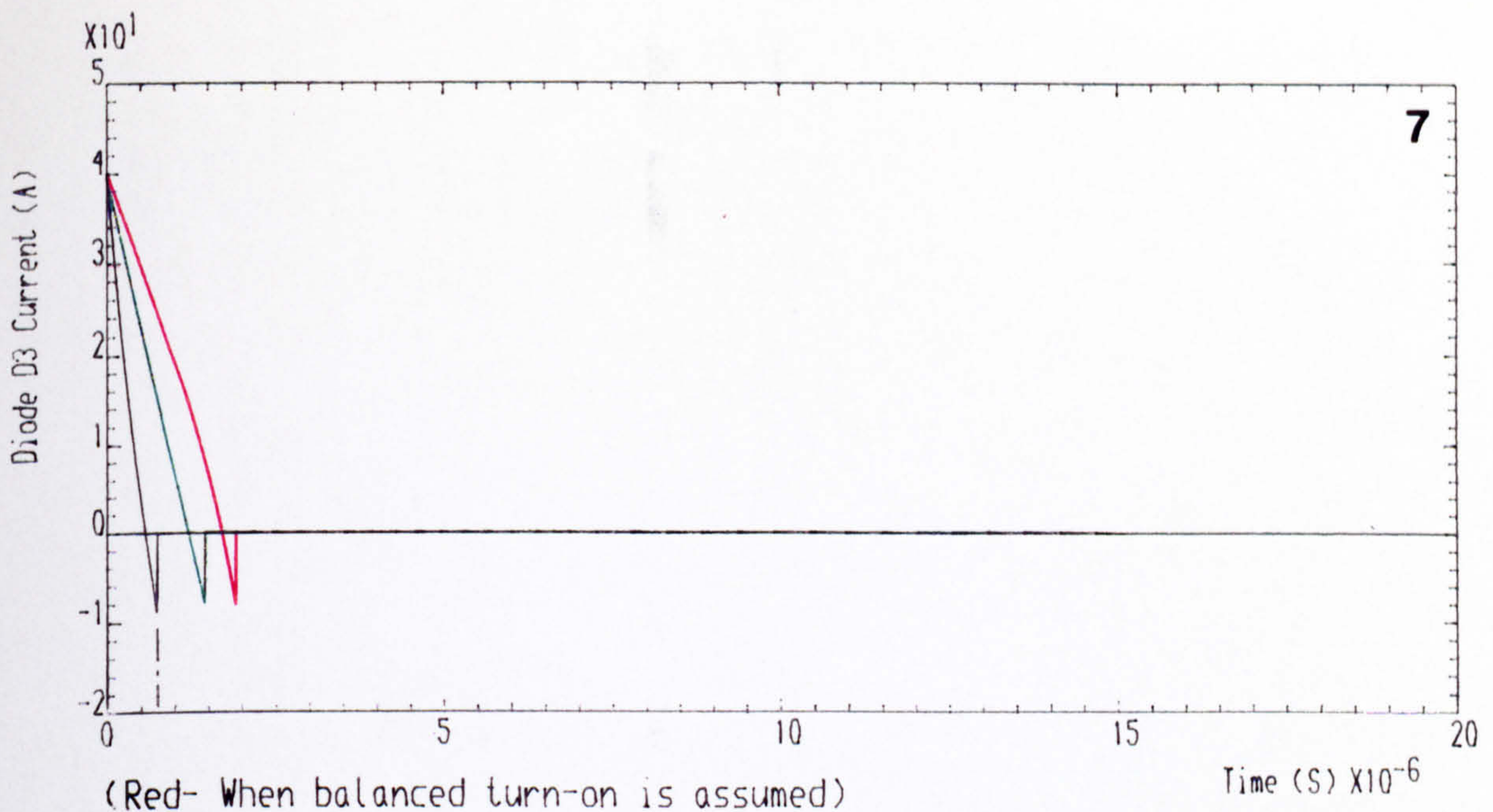


Figure 5.12 Waveforms at GTOs A1 and A2 picking up load current from the feedback path with unbalanced turn-on (Black) CONTINUED ..



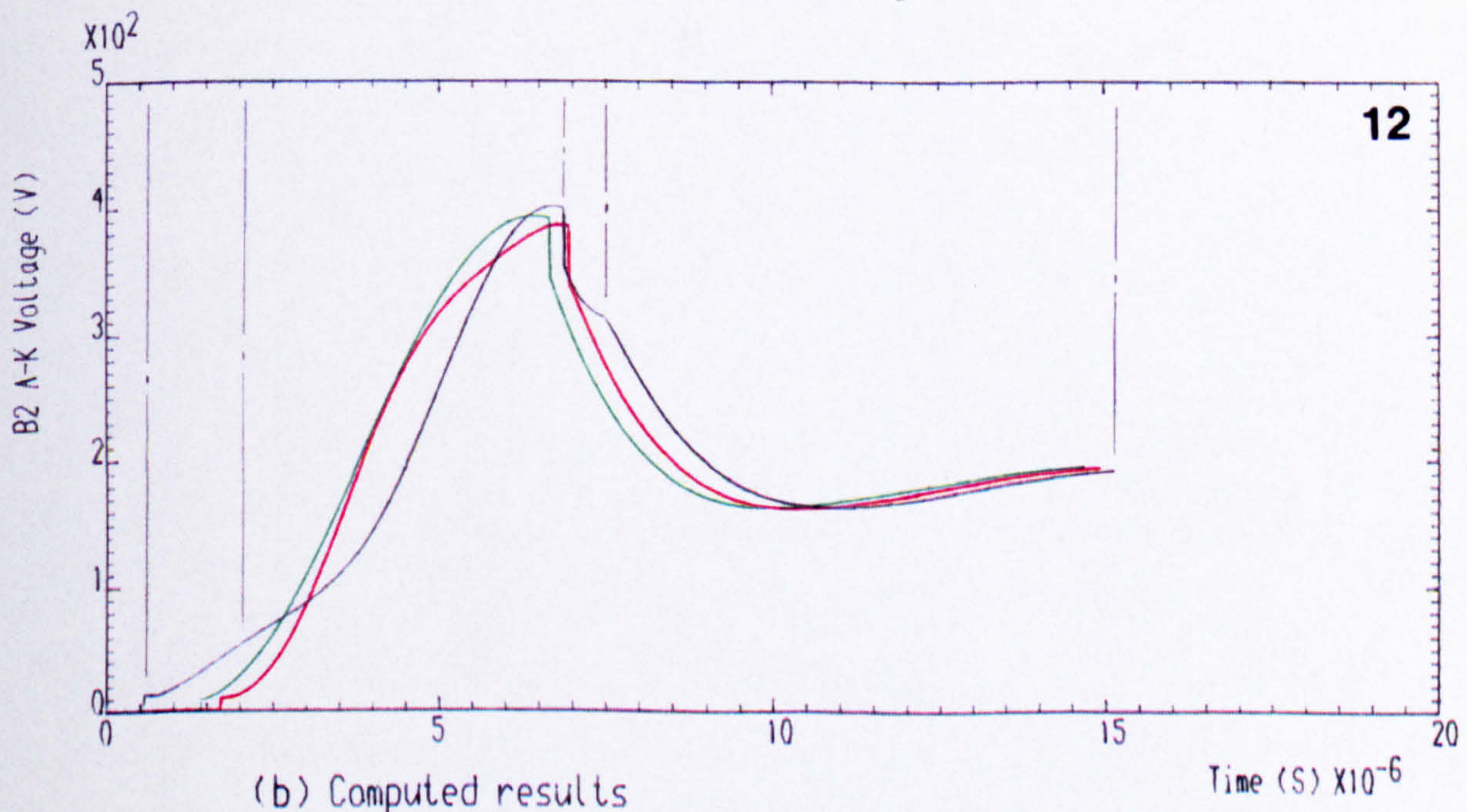
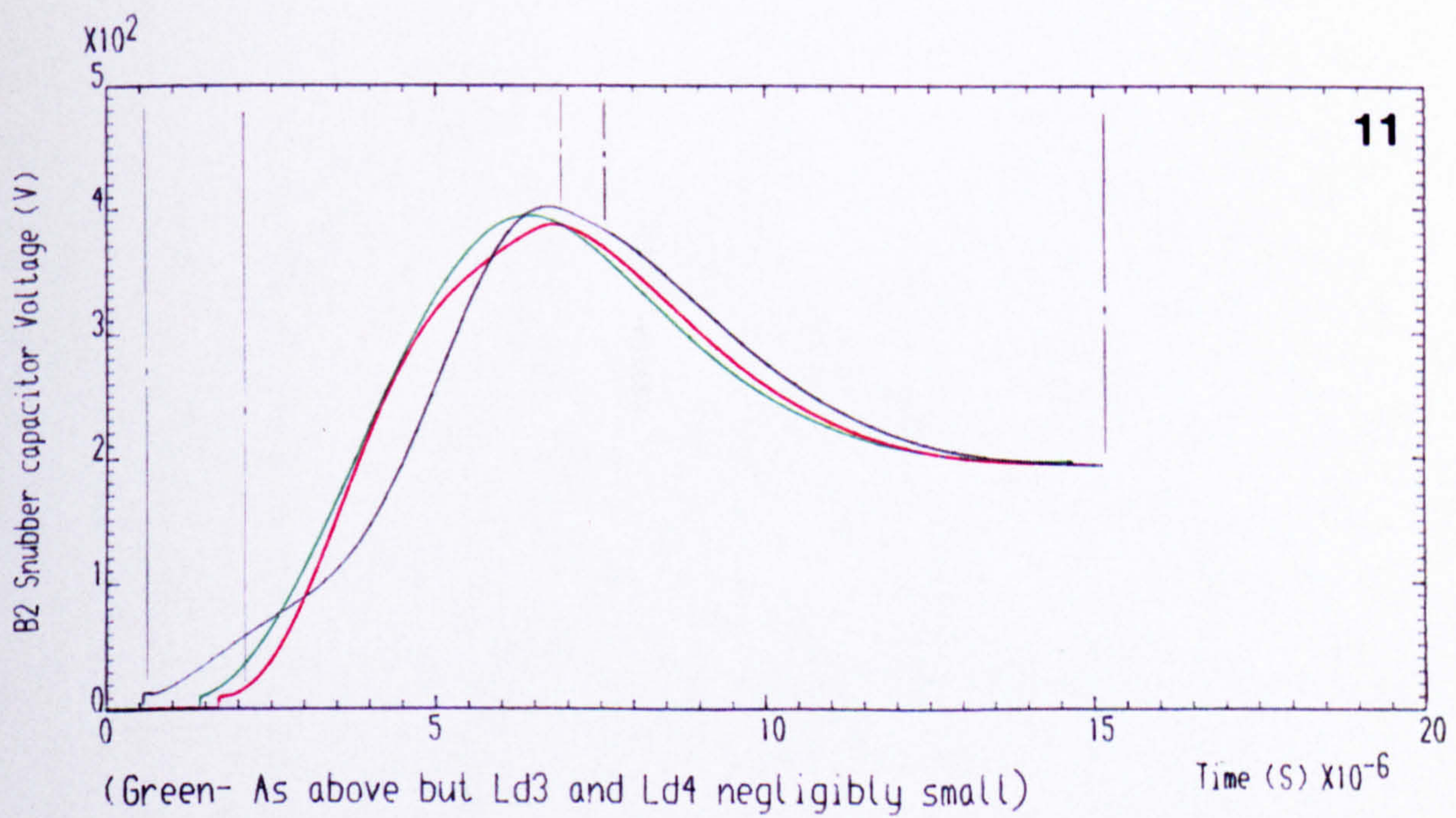
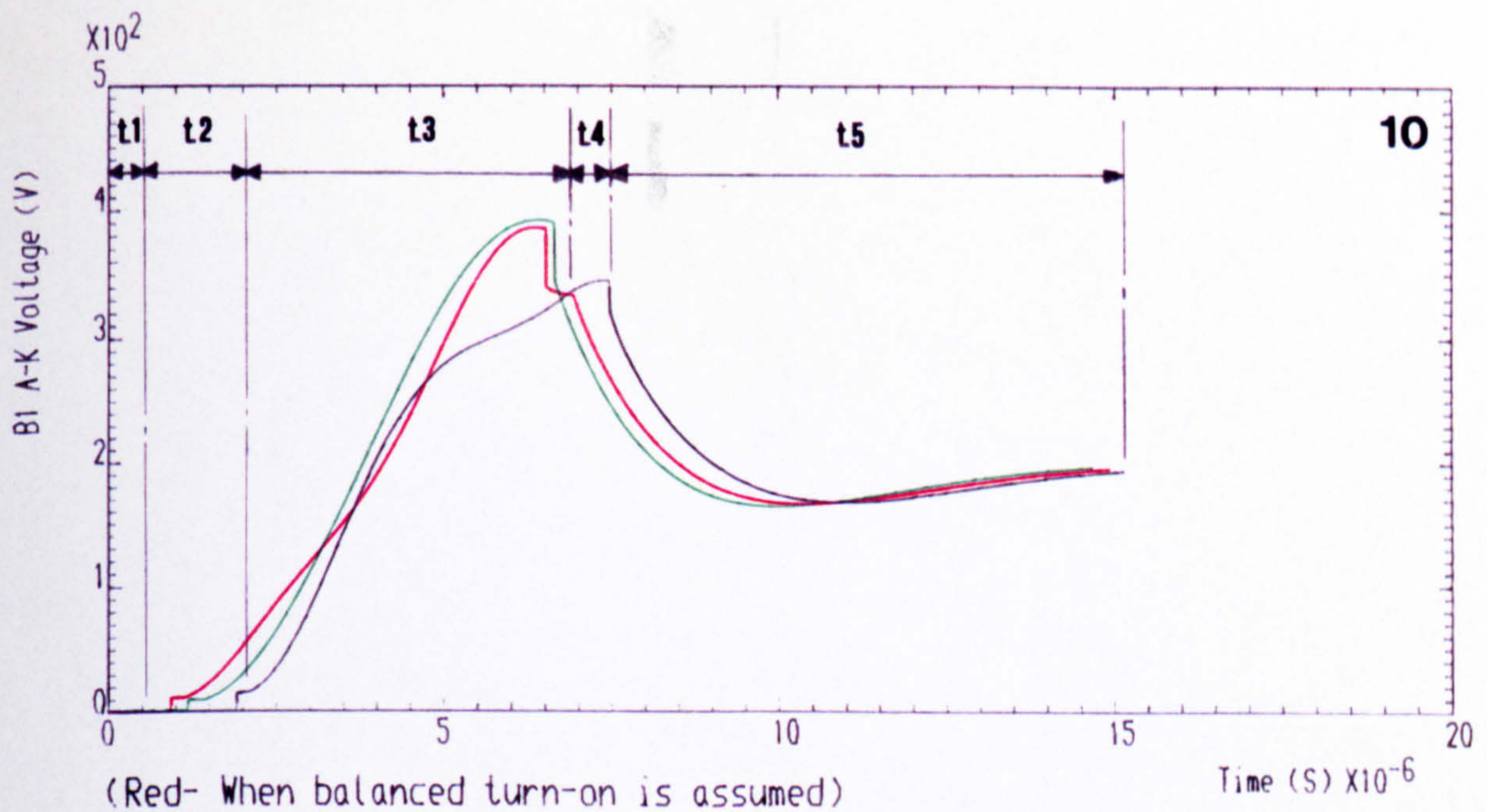


Figure 5.12 Waveforms at GTOs A1 and A2 picking up load current from the feedback path with unbalanced turn-on (Black) CONTINUED ..



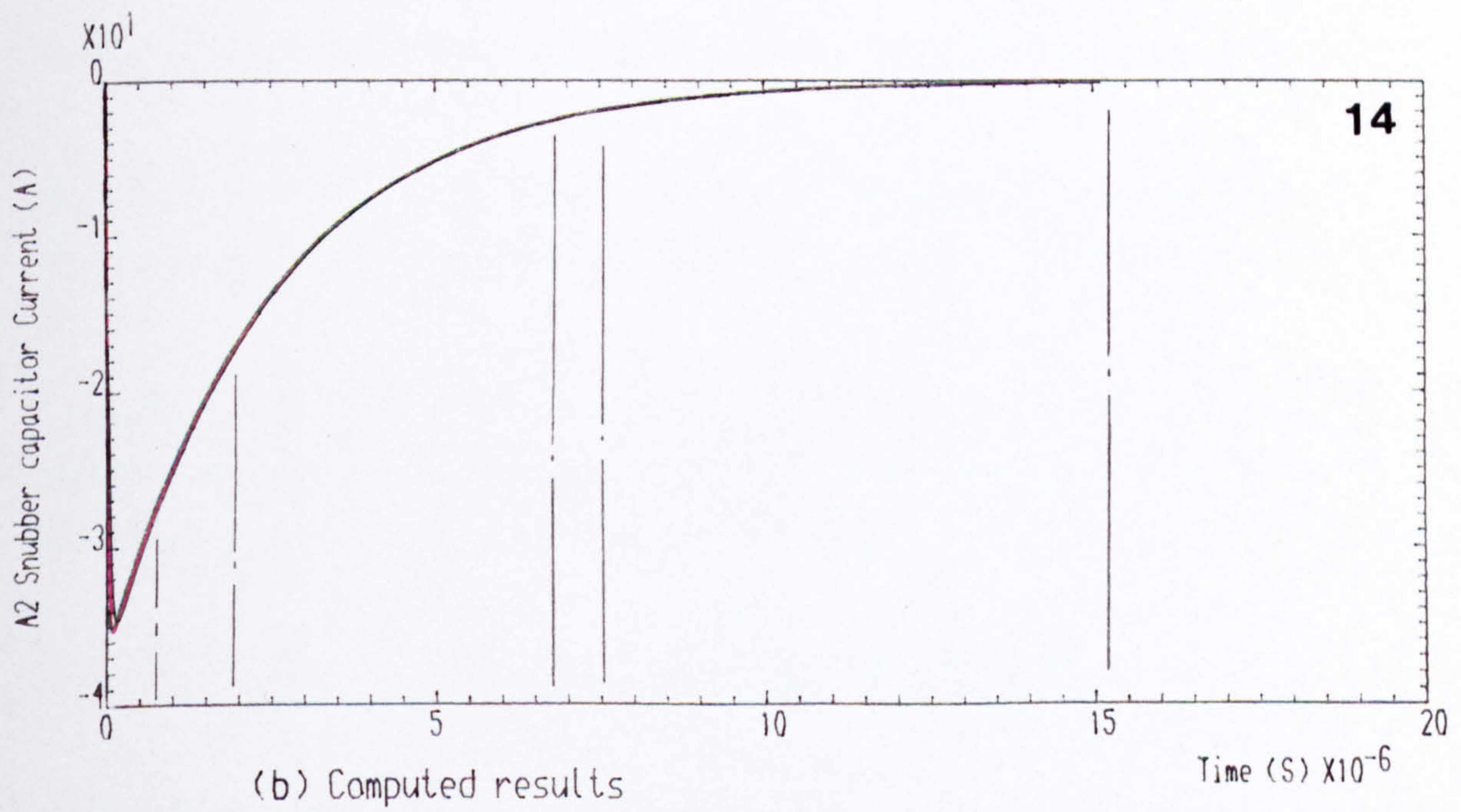
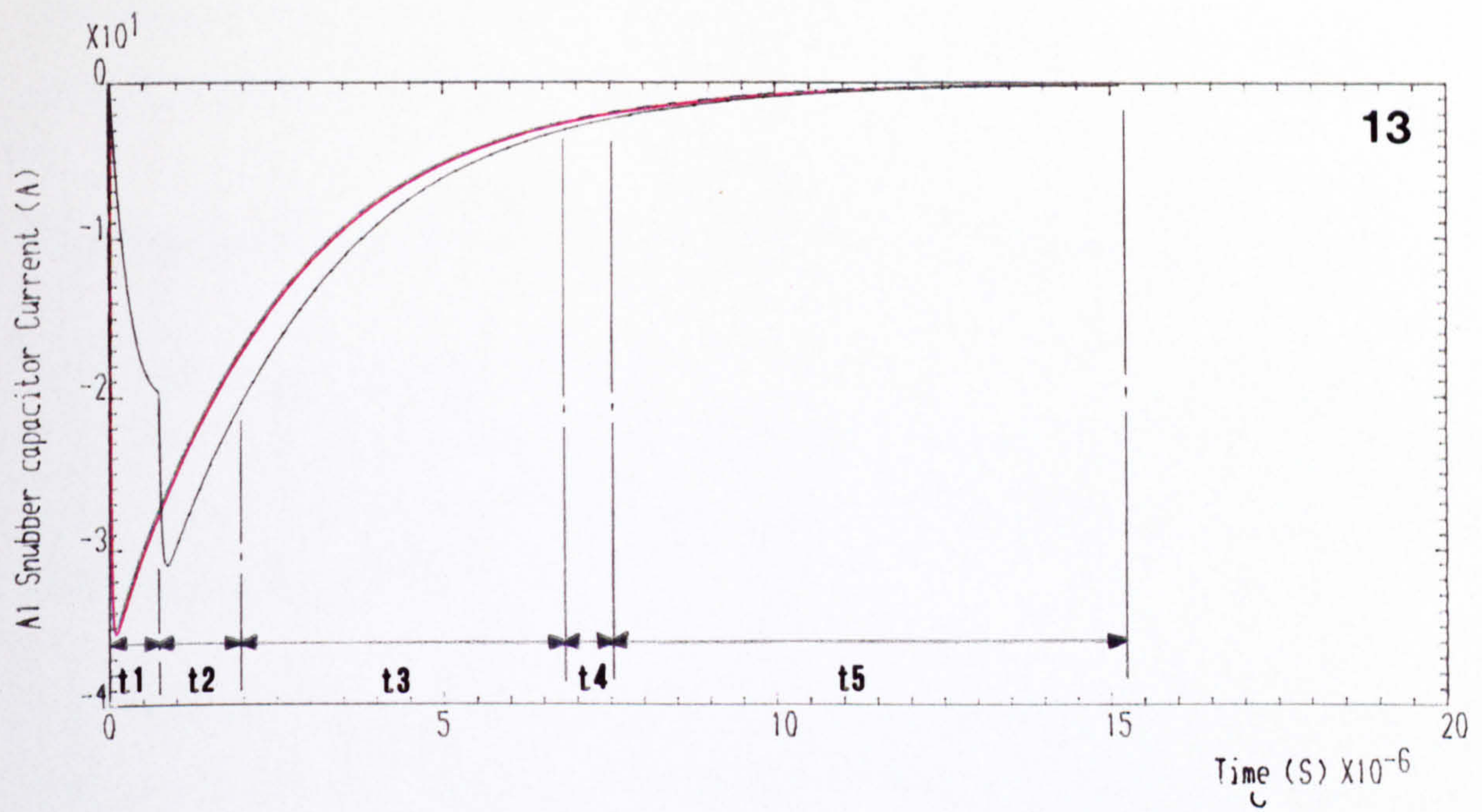


Figure 5.12 Waveforms at GTOs A1 and A2 picking up load current from the feedback path with unbalanced turn-on (Black)

END ..



*On expiry of interval  $t_5$ , the load energy is fully supplied by the DC source, with GTOs B1 and B2 supporting the supply voltage  $E_d$ .*

*The most influential stray inductance here is that of the supply.*

### **5.5 Summary of Main Points**

*i) The turn-off procedure is the same for quasi-square and PWM operations, but turn-on within a half-cycle is different because, with PWM, the current returns to the previously conducting GTO.*

*ii) When the source picks up load current supply from freewheeling or feedback at GTO turn-on, it produces initially a depression of the DC rail voltage due to the source inductance  $L_d$ , leading to some discharge of the blocking GTO snubber capacitor.*

*iii) Any turn-on time mismatch when turning on the GTOs together, produces increased current in the feedback diode of the same leg as the later turn-on GTO.*

*iv) An unavoidable transient shoot-through condition occurs at GTO turn-on as the antiparallel diode of the same leg undergoes reverse recovery. An additional GTO anode inductor accompanied by a freewheeling diode may be used to limit this.*

*v) The effects (iii) and (iv) are potentially damaging.*

### **5.6 Conclusions**

*The points made in Chapter 4 regarding methods of minimising switching transient effects, choice of circuit components and circuit layout are applicable here.*

*The concluding comments with points a, b, c, d and e in Chapter 4 are also applicable here. Additionally with PWM; turn-on time has been defined and possibly dangerous conditions revealed. Again, the computed and experimental results compare very well.*

## Chapter 6

### OVER-CURRENT PROTECTION FOR THE GTO THYRISTOR

#### 6.1 Introduction

*The satisfactory operation of GTO thyristor circuits depends heavily on the ability of the system to survive severe over-current conditions. Establishing a suitable over-current protection method can prove difficult.*

*The standard method for diodes and conventional thyristors, namely fusing, is not always adequate for GTOs, as the speed of fault current interruption may not be fast enough. Alternatives must be considered also.*

*The possible methods for GTO over-current protection are:*

*a) Mechanical circuit breaker on the supply, with all devices turned on to spread the fault current.*

*b) Fusing, this may be:*

*i) Individual GTO fusing;*

*ii) Input line fusing with all devices turned on to spread the fault current (which can be looked upon as a crowbarring action, see below);*

*c) Active electronic method;*

*i) Crowbar thyristor protection;*

*ii) Controlled self turn-off protection;*

*Each of these will be described, but the emphasis in this chapter is placed on (c) (i) and (ii), for which protection systems have been designed, constructed and tested.*

#### 6.2 Over-Current Protection Requirements of the GTO Thyristor

*Generally, the peak junction temperature produced by an over-current resulting from transient overloading, output short circuit, control circuit failure, supply fluctuation, etc., may prove destructive to semiconductor devices [39]. Since their thermal capacity is low, over-current protection must be fast to avoid excessive heating and damage, a typical maximum peak operating junction being 125°C.*



*Power semiconductors, in general, have two ratings which relate to their over-current protection:*

- a) Non-repetitive peak surge current rating  $I_{TSM}$ .*
- b) The  $I^2t$  rating.*

*Additionally, the GTO thyristor is prone to destruction if an attempt is made to turn off too high a current, this being defined by its maximum non-repetitive controllable on-state current  $I_{TCSM}$ . This rating is somewhat higher than its maximum repetitive controllable current  $I_{TCM}$ .*

*Whichever over-current protection method is considered, apart from that by self gate turn-off, the current through the GTO must be interrupted before the rated value of the non-repetitive peak surge current is reached. Similarly, the protection system must not allow through to the GTO a greater  $\int i^2 dt$  than the GTO  $I^2t$  rating during the interruption process. These factors are common to power diode, conventional thyristors and GTO thyristors. Unfortunately, these ratings are lower for the GTO than the conventional thyristor (and diode), making the protection problem more difficult.*

*Table 6.1 gives some data which illustrates this for devices with approximately the same RMS current and voltage ratings[32,33,34].*

*The reason for the lower ratings for the GTO are twofold. The internal carrier regeneration process is less than with the thyristor, meaning that the device is not so deeply in saturation (in bipolar transistor terms). This gives an increased conduction voltage drop and internal heat generation. The highly interdigitated gate-cathode structure leaves less cathode area for current conduction, producing a higher thermal resistance and localised overheating. This feature also defines the controllable current ratings.*

*The maximum current criterion is different when self gate turn-off protection is employed. The fault current must be detected at a value above the semiconductor device working load current, with allowance for normal surges. The protection action must be completed between the rising fault current detection and below the peak non-repetitive controllable current rating  $I_{TCSM}$ .*

DEVICE	Rated RMS on-state current (A)	Repetitive peak off-state voltage (V)	Peak non-repetitive surge current $I_{TSM}$ (A)	Peak non-repetitive controllable on- state current $I_{TCSM}$ (A)	Peak repetitive controllable on- state current $I_{TCM}$ (A)	$I^2_t$ (A <sup>2</sup> s)
Thyristor	40	1000	350	—	—	615
	80	1200	1200	—	—	7200
	125	1000	1520	—	—	11550
	550	1600	7650	—	—	290000
GTO	40	1000	270	180	90	365
	70	1200	330	280	200	540
	125	1000	1500	490	350	11000
	550	1600	4500	1680	1200	101000

Table 6.1 Device data

### 6.3 Circuit Breaker Protection for the GTO Thyristor.

*Mechanical circuit breakers are normally too slow for semiconductors, the interrupting time being some tens of milliseconds. Depending on the circuit, under load short circuit conditions, it may be possible to detect the over current and turn on all the devices to spread the fault current during circuit breaker opening, and thereby limit the individual device current to within its surge current rating. The current spreading depends on stray inductances and is almost impossible to predict accurately. Virtually always, the semiconductor devices must be overrated for this method, which is therefore uneconomical and is only used where other methods are unsatisfactory.*

### 6.4 Fuse Protection for the GTO

*The most destructive fault current to be protected against with semiconductors is that where the device is in short circuit path across the supply [35]. With a low source impedance, the prospective fault current will be of such a magnitude that the current must be interrupted very early in the rise to protect the GTO thyristor.*

*Relating the to Figure 6.1, the apex of the triangle of current must have a value (the*



cut-off current) which is below the non-repetitive peak surge current of the GTO  $I_{TSM}$ . Additionally the  $\int i^2 dt$  of the <sup>shaded</sup> triangular area must be less than the GTO  $I^2 t$  rating.

The disadvantage of fuses is that they shut down the circuit until they are replaced, and as stated earlier, the method may not be feasible for GTOs owing to the unavailability of fuses with cut-off current and  $I^2 t$  values which are low enough to provide protection. Hence active methods using electronic switching must be considered.

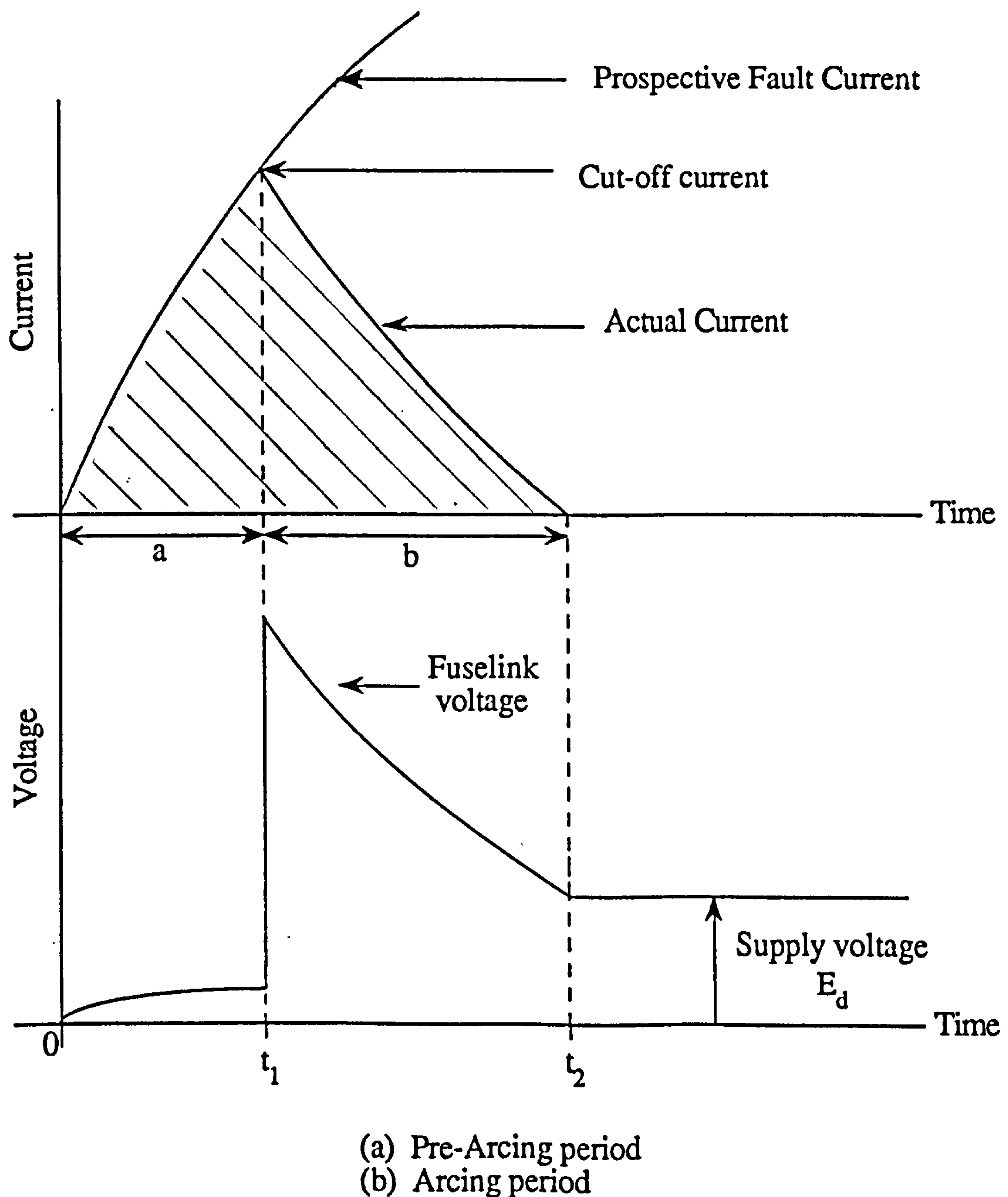


Figure 6.1 Stages in fusing

## 6.5 Active Electronic Methods

*Active methods for over-current protection must have the following features:*

- a) A fast fault current level detection system.*
- b) A means of interrupting the fault current before it has risen to a value that will overstress the GTO.*

*The detection system (a) is common to any active method of protection. This will*

*generate a signal which will then activate (b). The two methods of implementing (b) are considered in detail later.*

## 6.6 The Current Level Sensor

*A block diagram of the experimental current level detector is shown in Figure 6.2. This comprises a current level monitoring device, such as a Hall effect sensor, the output of which is processed through fast linear amplifiers to produce a final logic signal  $V_s$  that corresponds to an over-current. It is desirable for practical purposes that the Hall voltage is required to be linear with the current to be sensed. To increase the flexibility of the current sensor, a means of adjusting the trip current setting is necessary.*

*The protection capability of the sensor circuit is limited by the maximum value of flux density to which the Hall effect device can remain linear. In the experimental arrangement, the maximum GTO controllable on-state current  $I_{TCM}$  corresponding to this is about 95A. The sensor circuit is therefore designed for GTOs having  $I_{TCM}$  values ranging from 10A to 95A. The current detection setting is approximately 5% higher than the operating peak device current (irrespective of fault current  $di/dt$ ). This is adjustable.*

*Time delays superimposed into the output of the Hall effect device must be compensated for in order to enhance the sensor circuit effective time. A detailed description of the causes, behaviour and compensation of these delays is given later in sub-section 6.6.4.*

*Upon commencement of over-current, the corresponding output signal  $V_s$  of the current sensor circuit is processed suitably via the GTO gate control logic for the two active methods of protection considered.*



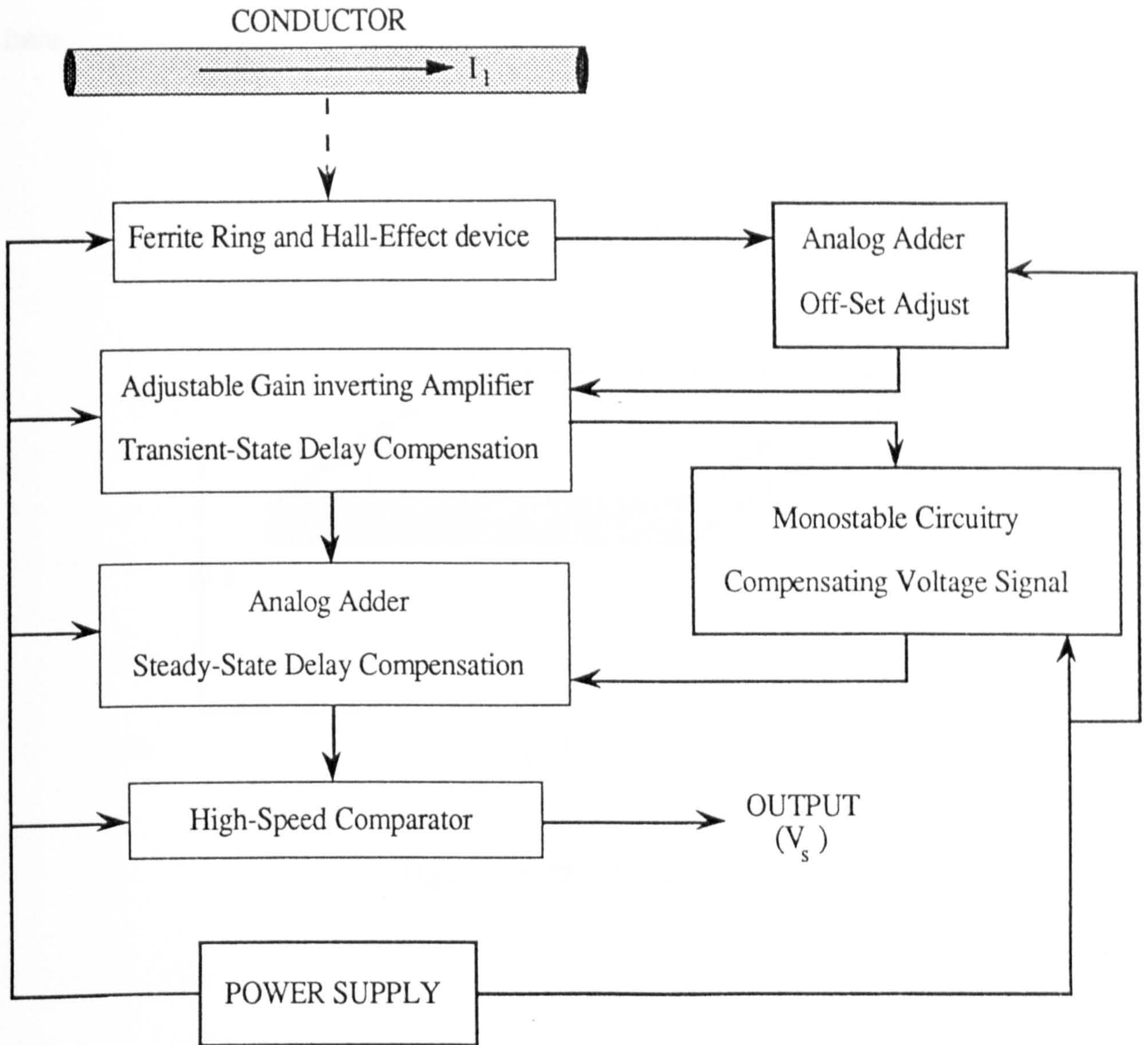


Figure 6.2 Block diagram of current sensor with delay time compensation

### 6.6.1 The Hall Effect Device and Offset Adjustment

*In principle, the application of a magnetic field to a slab of semiconductor material, having electrons and holes drifting in opposite directions, produces an electric field across the slab and a potential difference  $V_H$  is established. This is the Hall effect and  $V_H$  is the Hall voltage.*

*The Hall effect is caused, as demonstrated in Figure 6.3, by electron deflection within the material concentrating the negative charges to one side or the other depending on the polarity of the applied magnetic field. The principle stated above is applied in Hall effect integrated circuits to produce magnetically activated sensors, such as the one employed*



here.

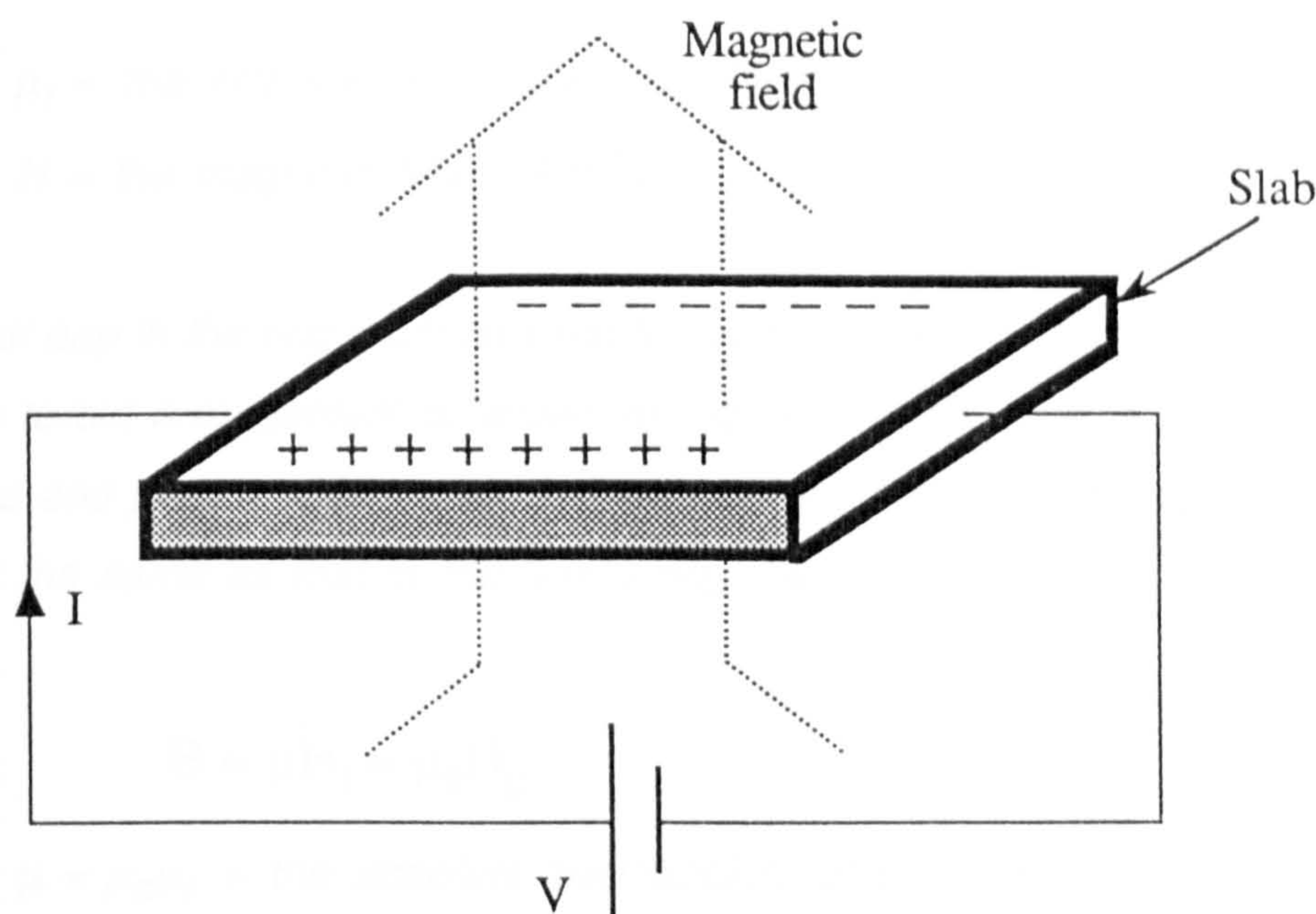


Figure 6.3 The Hall effect

The Hall effect sensor is activated by the magnetic field from the current to be monitored. In general, the flux density  $B$  at a distance  $R$  from a linear conductor carrying current  $I$  in free space is given by [36]:

$$B = \frac{\mu_0 I}{2\pi R} \tag{6.1}$$

where  $\mu_0$  = permeability of free space, ( $\text{Hm}^{-1}$ )

Calculation shows that a magnetic flux density of about 2mT at 1cm from the centre of a circular conductor would correspond to a 100 A flowing in that conductor. Therefore, some means to increase  $B$  is essential.

6.6.2 The Magnetic Field Sensor (Transducer)

To increase the magnetic flux density  $B$ , a ferrite toroid is placed round the conductor. This has the effect of increasing the available flux density  $B$  according to the



relationship:

$$B = \mu_0 \mu_r H \quad (6.2)$$

where  $\mu_r$  = the relative permeability of ferrite, (dimensionless)

$H$  = the magnetic field, ( $\text{Am}^{-1}$ )

However, an air gap in the ring must exist to accommodate the Hall effect device in the flux path. The toroid arrangement is shown in Figure 6.4. The flux is assumed to leave the pole pieces and pass across the air gap without any lateral spreading, so that the gap flux density is the same as that in the ferrite ring, i.e.

$$B = \mu H_f = \mu_0 H_g \quad (6.3)$$

where  $\mu = \mu_0 \mu_r$  = the absolute permeability of the ferrite, ( $\text{Hm}^{-1}$ )

$H_f$  and  $H_g$  are respectively the ferrite and air gap magnetic field strengths.

The mean lengths of the flux path in the ferrite and the air gap are  $l_f$  and  $l_g$  respectively, and assuming a uniform  $\mu_r$  and  $\mu_0$ , and linear relationship between  $B$  and  $H_f$  at low flux densities, then by applying Ampere's law, the following is obtained

$$\int H \, dl = \int_0^{l_f} H_f \, dl + \int_{l_f}^{l_g} H_g \, dl = I \quad (6.4)$$

Thus

$$I = H_f l_f + H_g l_g \quad (6.5)$$

Substituting equation 6.3 into 6.5 gives

$$B = \frac{I}{\left(\frac{l_f}{\mu}\right) + \left(\frac{l_g}{\mu_0}\right)} \quad (6.6)$$



Inspecting equation 6.6, it can be seen that the dominating factor in the magnitude of  $B$  produced for a given current  $I$  is the length of the air gap  $l_g$ , because the ratio  $\mu$  to  $\mu_0$  is about 1500:1 [36]. With  $l_g$  equal to approximately 3mm (the thickness of the Hall effect device employed), equation 6.6 approximates to:

$$B \approx 0.42 I \text{ (mT)} \quad (6.7)$$

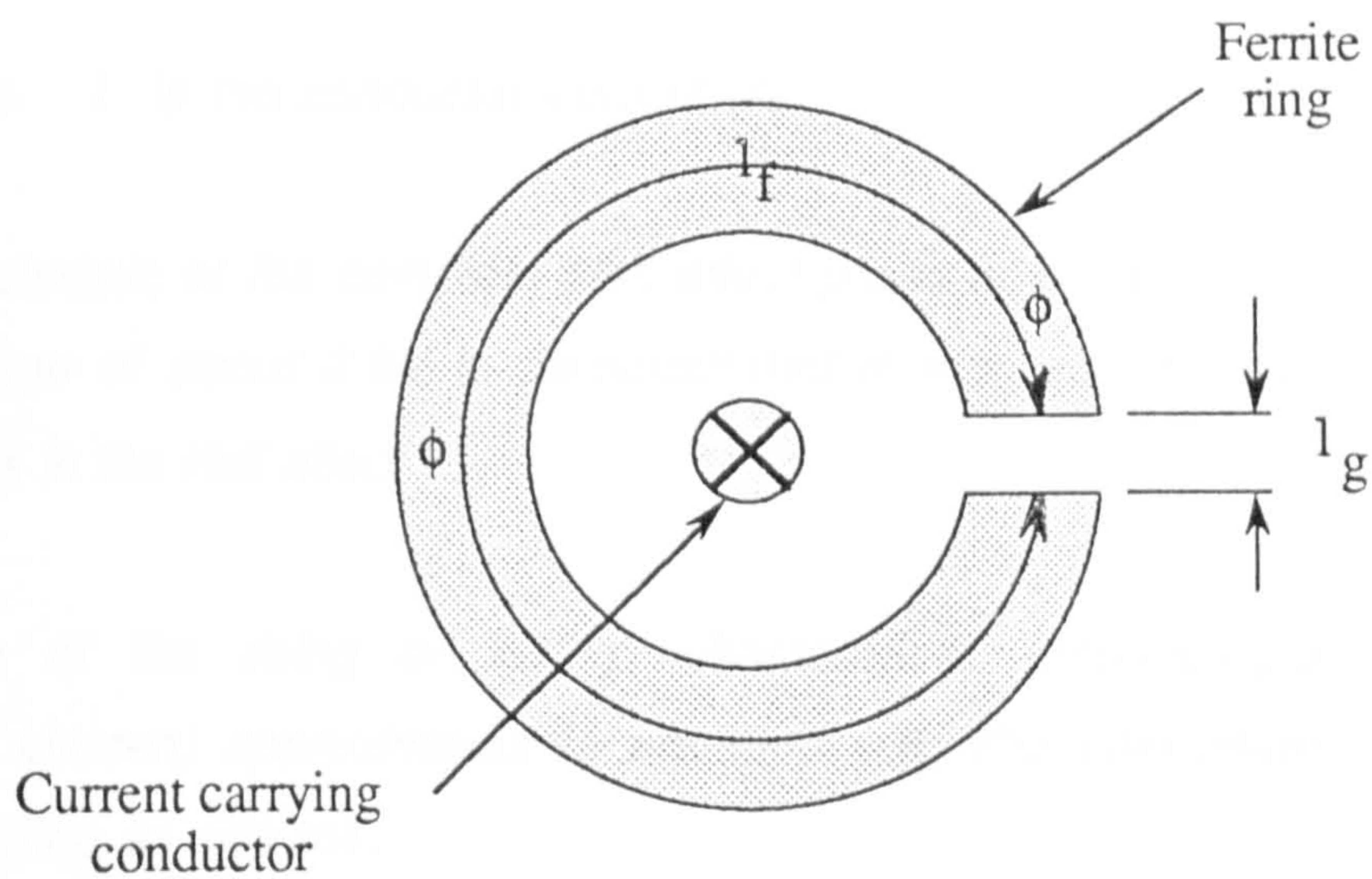


Figure 6.4 Introduction of the ferrite ring into the flux path

In practice, not all the flux is retained within the ferrite, as a small amount of leakage occurs. Also fringing in the air gap spreads the flux over an area greater than the cross section of the ferrite core, causing the mean flux density in the air gap to be less than that in the ferrite ring. For the purpose of current sensing, neglecting leakage and fringing leads to a very small error since  $l_g \ll l_f$ .

The Hall effect transducer sensitivity  $\Delta V_H$  is  $V_H/B$  (mV/mT). For the one employed,  $B$  is calculated from equation 6.6 and  $V_H$  is obtained experimentally. This is measured to be about 33mV/mT.



Using equation 6.7, the relation between the Hall voltage and the current being mentioned is:

$$\Delta V_H \approx (33 \text{ mV/mT})(0.421 \text{ mT})$$

thus

$$\Delta V_H \approx 14 \text{ mV/A}$$

giving

$$V_H \approx 141 \text{ mV} \quad (6.8)$$

where  $I$  is the conductor current (A)

The characteristic of the complete Hall effect probe is shown in Figure 6.5. A zero flux offset voltage of about 2.8V is demonstrated due to voltage drops of the integrated components in the Hall effect IC.

The slope of the rising or falling characteristic (depending on which of the two outputs is chosen) approximates to equation 6.8. The characteristic is linear for flux densities rising to  $\pm 40 \text{ mT}$ .

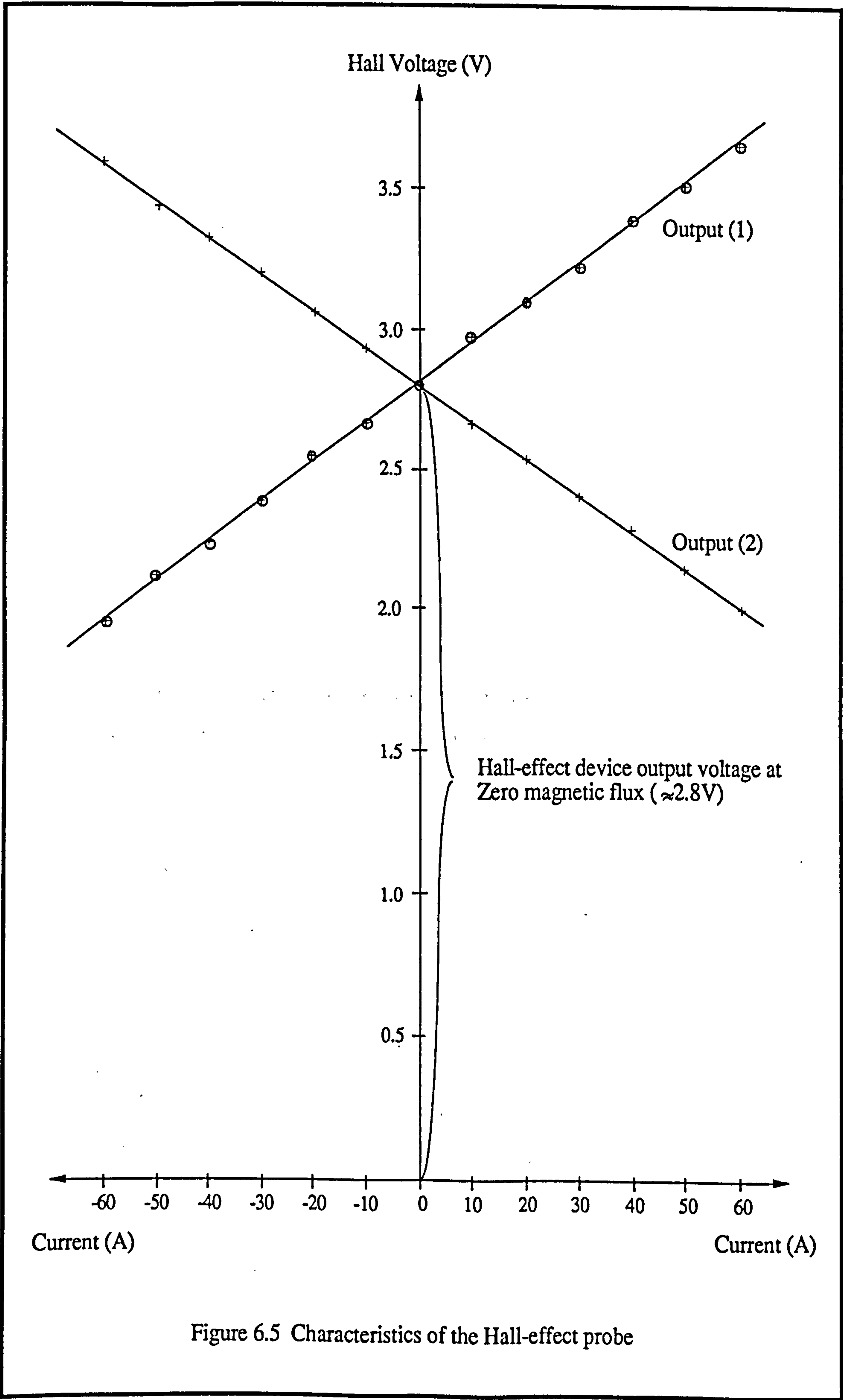
The direct voltage component at zero magnetic flux is blocked by a capacitor in the output circuit. However, the AC output voltage from the capacitor is then adjusted by means of an analogue adder or summing amplifier (Figure 6.2). A fast slew rate ( $50 \text{ V}/\mu\text{S}$ ) operational amplifier forms the basis for this stage (Figure 6.6). The summing amplifier has unity gain giving an output voltage equal to the algebraic sum of each input voltage. This may be expressed as:

$$V_{\text{out}} = \frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 \quad (6.9)$$

where  $R_f$  = the feedback resistor

$R_1$  and  $R_2$  = the input resistors

and as a voltage follower, the gain  $R_f/R_1 = R_f/R_2 = 1$ .





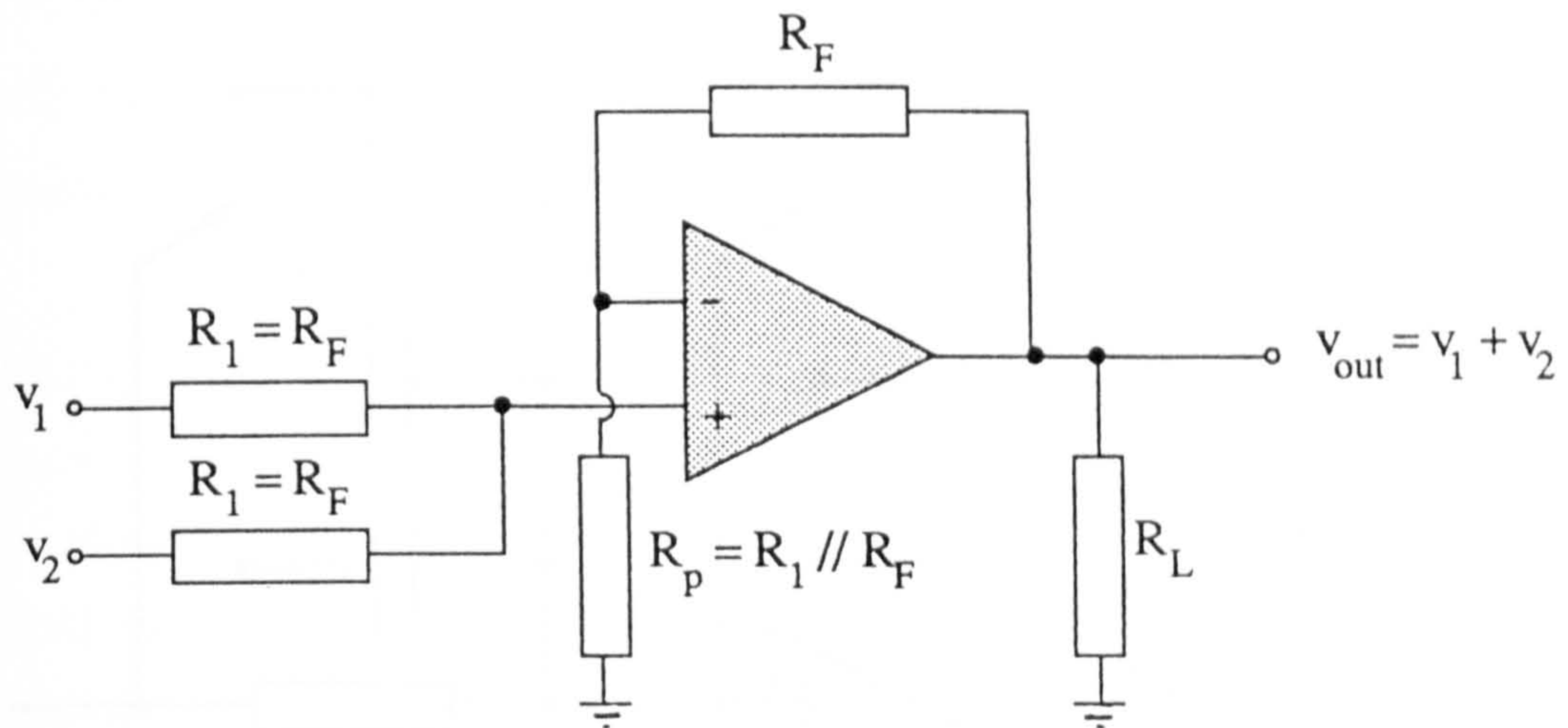


Figure 6.6 Analog adder circuit

In this case ( $v_1$ ) is the negative Hall effect transducer output voltage and ( $v_2$ ) is an adjustable DC voltage ranging from 0 to -3V to trim out the offset.

### 6.6.3 The Adjustable Gain Inverting Amplifier

A fast operational amplifier (Figure 6.2) is also used here. For an inverting amplifier (Figure 6.7), the output voltage  $v_{out}$  is controlled as a function of the negative of the input voltage  $v_{in}$ .

$$v_{out} = -\frac{R_f}{R_{in}} v_{in} \quad (6.10)$$

where  $R_f$  = the feedback resistor

$R_{in}$  = the input resistor to the inverting input.

and the transfer ratio  $v_{out}/v_{in}$  being the overall gain  $A_v$  of the amplifier.

With the stipulation given earlier in section 6.6 concerning the range of the current levels for the sensor circuit to act upon, the output voltage of the amplifier voltage  $v_{out}$  is set to give 5V for each current setting. Thus the required gain of this amplifier falls into the range (using equation 6.10);

$$3.8 \leq A_v \leq 35.7$$



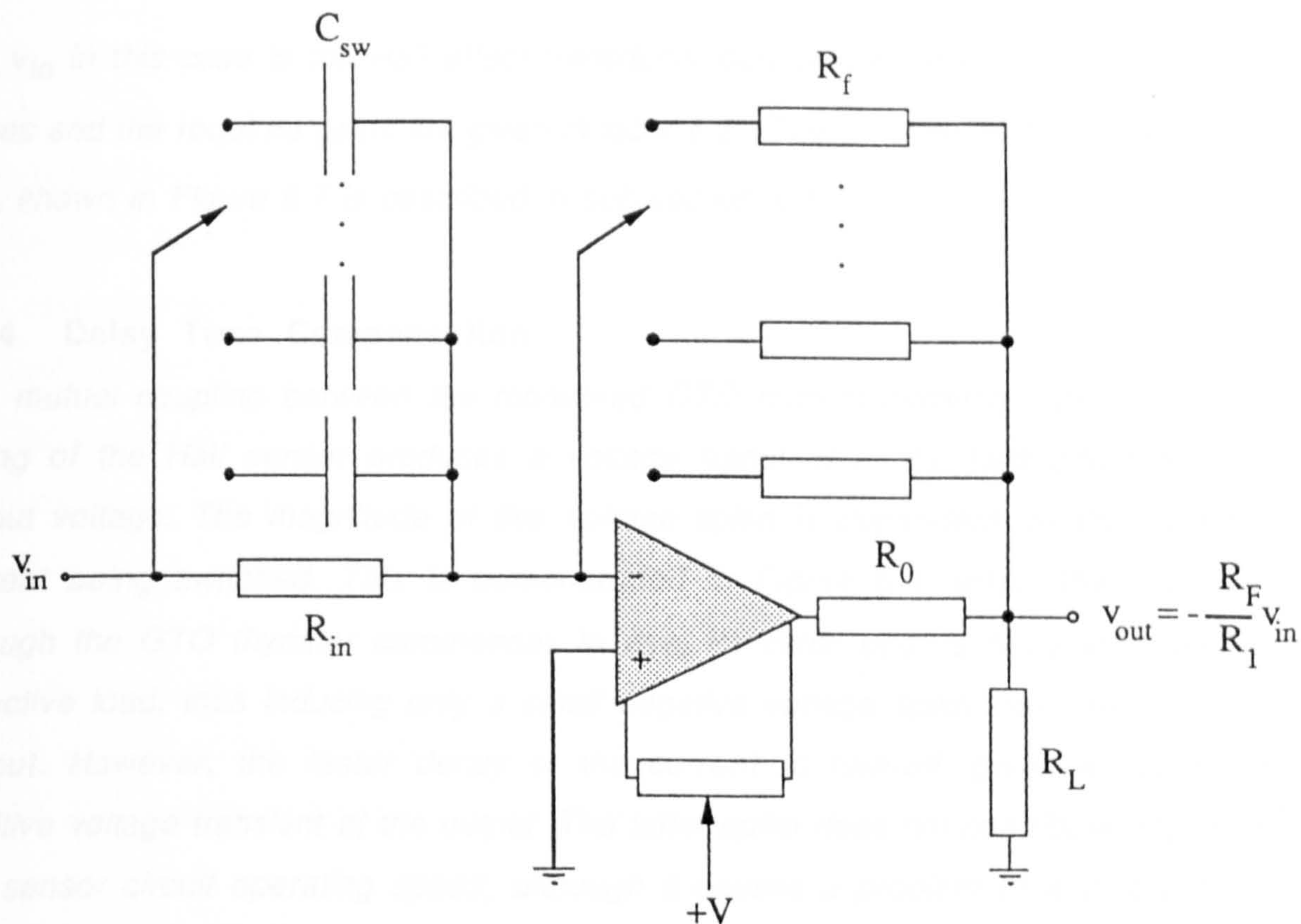


Figure 6.7 Variable gain inverting amplifier

Peak load current to be monitored for normal operation (A)	$V_H$ from equation 6.8 (mV)	Feedback resistor $R_F$ (k $\Omega$ )	Gain $A_v$ from equation 6.10 ( $R_{in} = 10\text{k}\Omega$ )
10	140	357	35.7
15	210	238	23.8
20	280	179	17.9
25	350	143	14.3
30	420	119	11.9
35	490	102	10.2
40	560	89	8.9
45	630	79	7.9
50	700	71	7.1
60	840	60	6.0
70	980	51	5.1
80	1120	45	4.5
90	1260	40	4.0
95	1330	38	3.8

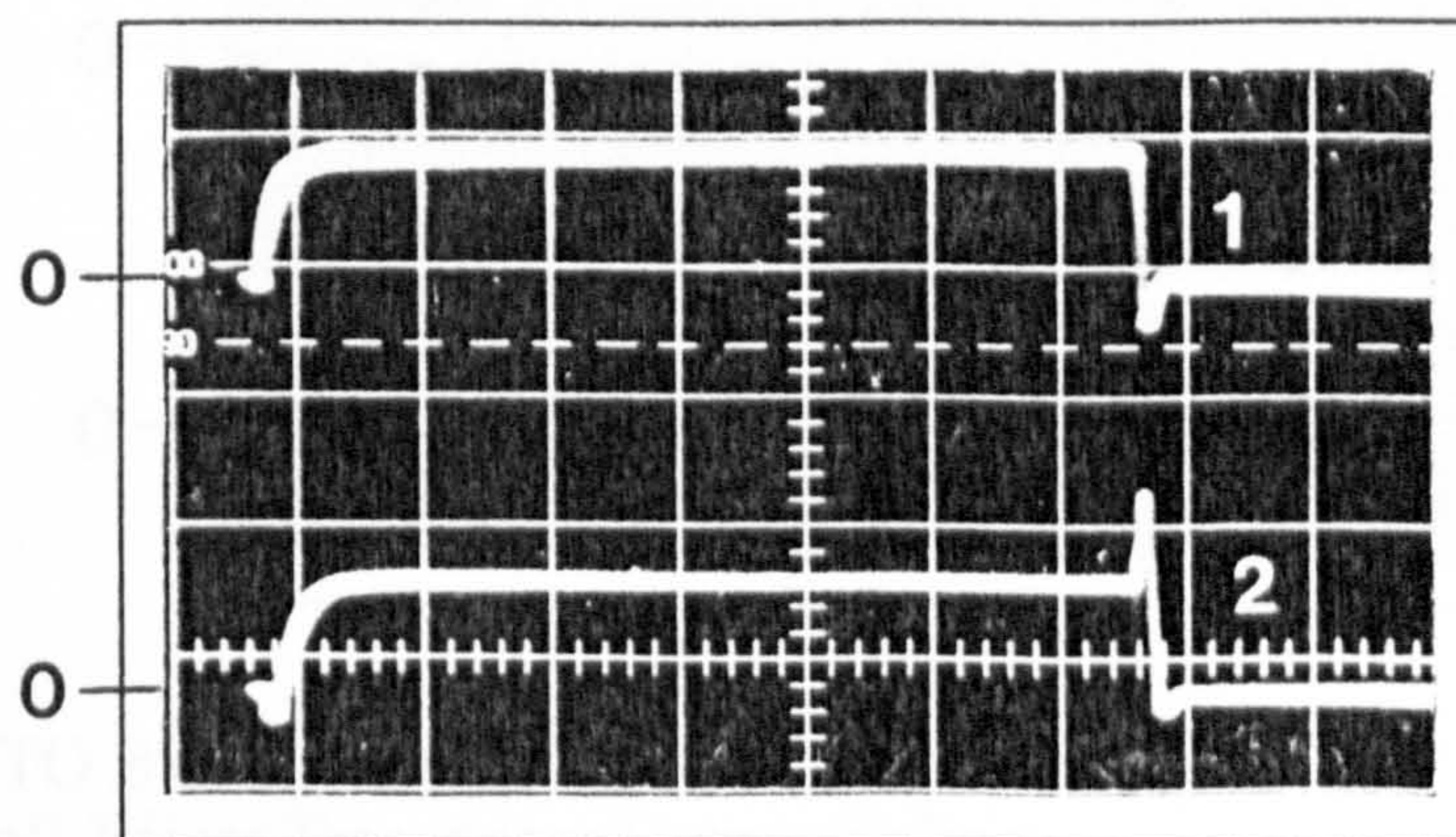
Table 6.2 Variable gain range of the amplifier stage to provide various current settings



The  $v_{in}$  in this case is the Hall effect transducer output voltage  $v_H$ . These set current values and the required gains are given in table 6.2. The function of the capacitor switch  $C_{sw}$  shown in Figure 6.7 is described in sub-section 6.6.4.

#### 6.6.4 Delay Time Compensation

The mutual coupling between the monitored GTO current carrying conductor and the wiring of the Hall sensor produces a voltage transient in the Hall effect transducer output voltage. The magnitude of this voltage spike is dependent on the  $di/dt$  of the current being switched. This is demonstrated in Figure 6.8; when the load current through the GTO thyristor commences to rise, its initial  $di/dt$  is fairly low due to the inductive load, thus inducing only a small negative voltage spike into the transducer output. However, the faster decay of the current at turn-off, gives a much higher positive voltage transient at the output. The latter spike does not contribute any delay to the sensor circuit operating speed, although it causes a problem of a different nature which will be dealt with in the next sub-section. However, although small, the negative voltage spike at the start of the load current rise does contribute time delay to the sensor circuit response and compensation for this is essential.



- |                              |            |
|------------------------------|------------|
| (1) GTO Branch Current       | (20A/div.) |
| (2) Amplifier Output Voltage | (5V/div.)  |

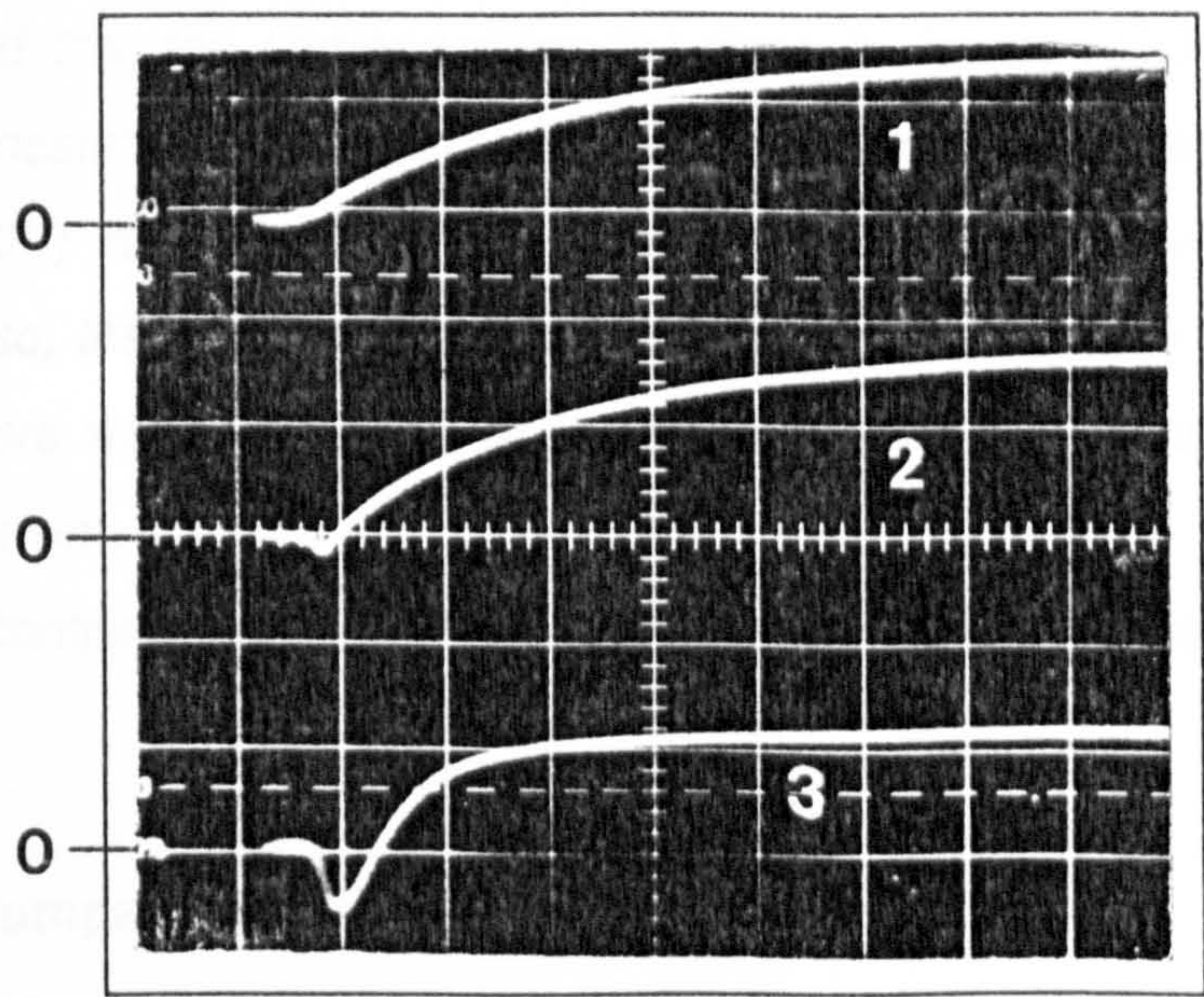
Time Scale: 0.1mS/div.

Figure 6.8 The Voltage Transients



A high fault current results either when the GTO turns on into a fault condition, or when the fault arises with the device already carrying full load current. The delay compensation considered for each of these is as follows:

- a) For the GTO switching on into a short circuit (case 1): The delay in the sensor response due to the negative voltage spike can be compensated for by increasing the rate of rise of the transducer output voltage. This is achieved by including the speed up capacitors  $C_{sw}$  and  $C_c$  (rise-time response by charge- control [37]) shown in the full circuit of Figure 6.13. The benefit is shown by the oscillogram of Figure 6.9, trace 3. The reduction of the transducer time constant is about  $9\mu S$ .
- b) For a short circuit superimposed on full load current (case 2): Figure 6.10 shows the behaviour of the negative voltage spikes as the fault current rises suddenly during the load current steady-state (trace 1). It can be seen from trace 4, that a delay of about  $3.5\mu S$  is contributed.



- (1) GTO Branch Current (20A/div.)
- (2) Hall-Effect Transducer Output Voltage (0.2V/div.)
- (3) Inverting Amplifier Compensated Output Voltage (5V/div.)

Time Scale:  $5\mu S/\text{div.}$

Figure 6.9 Compensation for the GTO turn-on into a short-circuit

The approach adopted is to employ the leading edge of the spike to trigger a fast



monostable. Its output voltage pulse, of fixed duration, is then amplified to a little in excess of the worst case spike voltage, here about 14V (5V+9V, Figure 6.10), as the level of the amplifier output voltage will not at any time prior to a fault exceed 5V as mentioned previously, and the amplifier saturates at about  $\pm 9V$ , Figure 6.10, trace 4. The compensating voltage pulse is then added to the original voltage spike to eliminate it, as illustrated in Figure 6.10, traces 3,4 and 5. At the start of the spike, the compensated voltage level must always be greater than the spike voltage to activate the voltage level detector (next sub-section). Trace 5 (the addition of traces 3 and 4) shows that the spike is not completely eliminated, but compensation for  $3.1\mu S$  of the  $3.5\mu S$  duration is achieved. The remaining  $0.4\mu S$  is due to the propagation delay of the monostable integrated circuitry.

The other two pulses of Figure 6.10, trace 3 are due to the other falling edges of the voltage waveform, shown in trace 4, and are unavoidable. Their effect on the sensor circuit performance is negligible.

It must be noted that the compensation for case 2 is not valid for case 1. This is because the monostable that generates the compensating pulse cannot be triggered by the negative (w.r.t 0V) voltage spike. The speed-up capacitors proved to be adequate, as shown later. Also, the compensation for case 1 is not possible for case 2 as the induced voltage spike here will cause a fall of the transducer output voltage that corresponds to the full load current.

The time delay compensation for both cases must be always on stand-by while the GTO(s) in conduction.

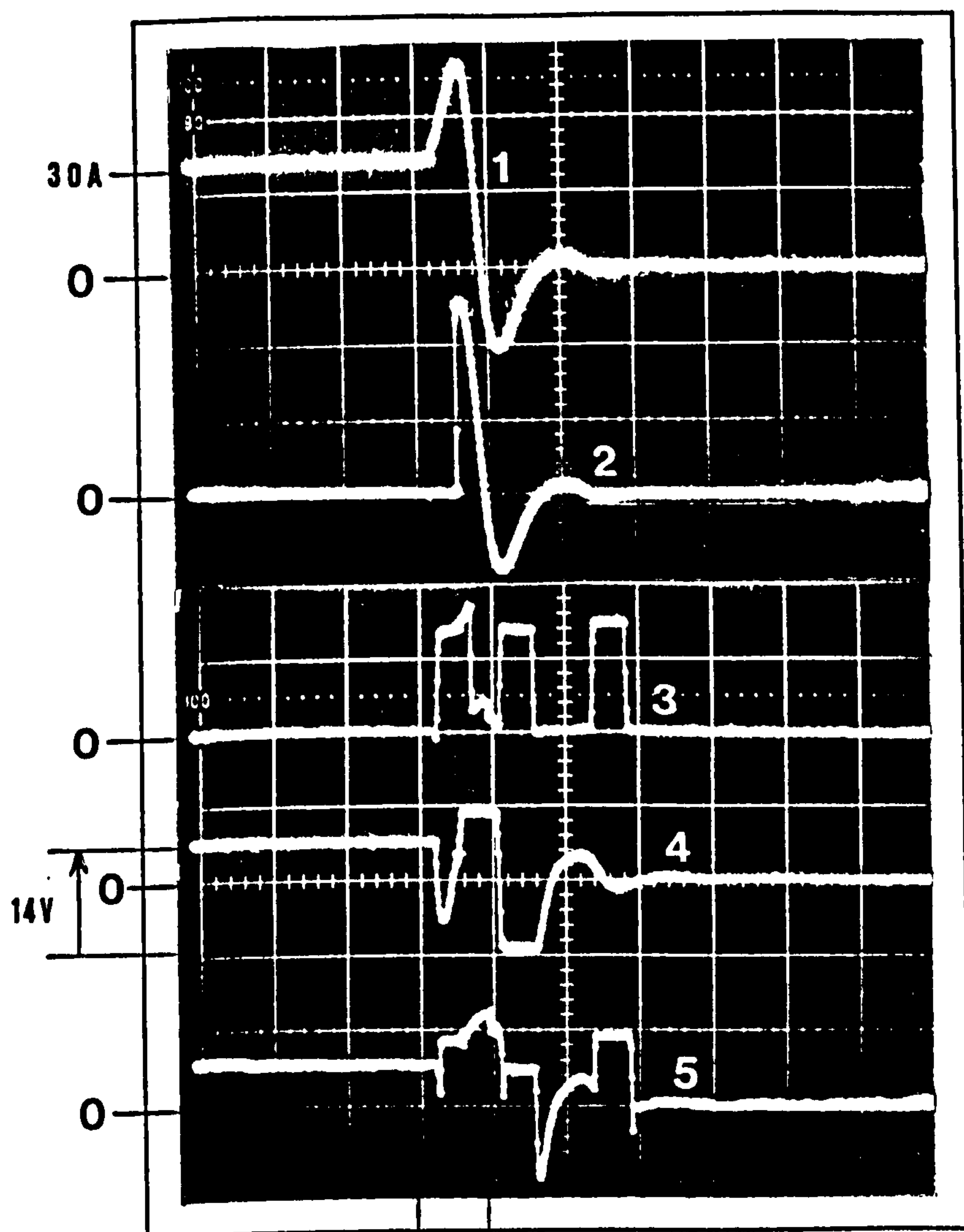
#### 6.6.5 The Comparator with Hysteresis.

Again, a fast slew rate operational amplifier is employed. The comparator or voltage level detector determines if an input voltage  $v_{in}$  is above or below a reference voltage  $V_R$  to activate fault tripping. In response, the output voltage will assume either a low or a high state.

The common operational amplifier comparator connection can be modified to provide hysteresis, thus achieving noise immunity without altering the reference voltage level.

Referring to Figure 6.11, the hysteresis voltages above and below  $V_R$  are respectively [41]:





(1) GTO Branch Current  
(20A/div.)

(2) GTO Snubber Current  
(20A/div.)

(3) Compensating Voltage  
Pulse (10V/div.)

(4) Inverting Amplifier Output  
Voltage (10V/div.)

(5) Analog Adder Output  
(Compensated) Voltage  
(10V/div.)

Time Scale: 10 $\mu$ /div.

WINDOW  
(1 $\mu$ S/div.)

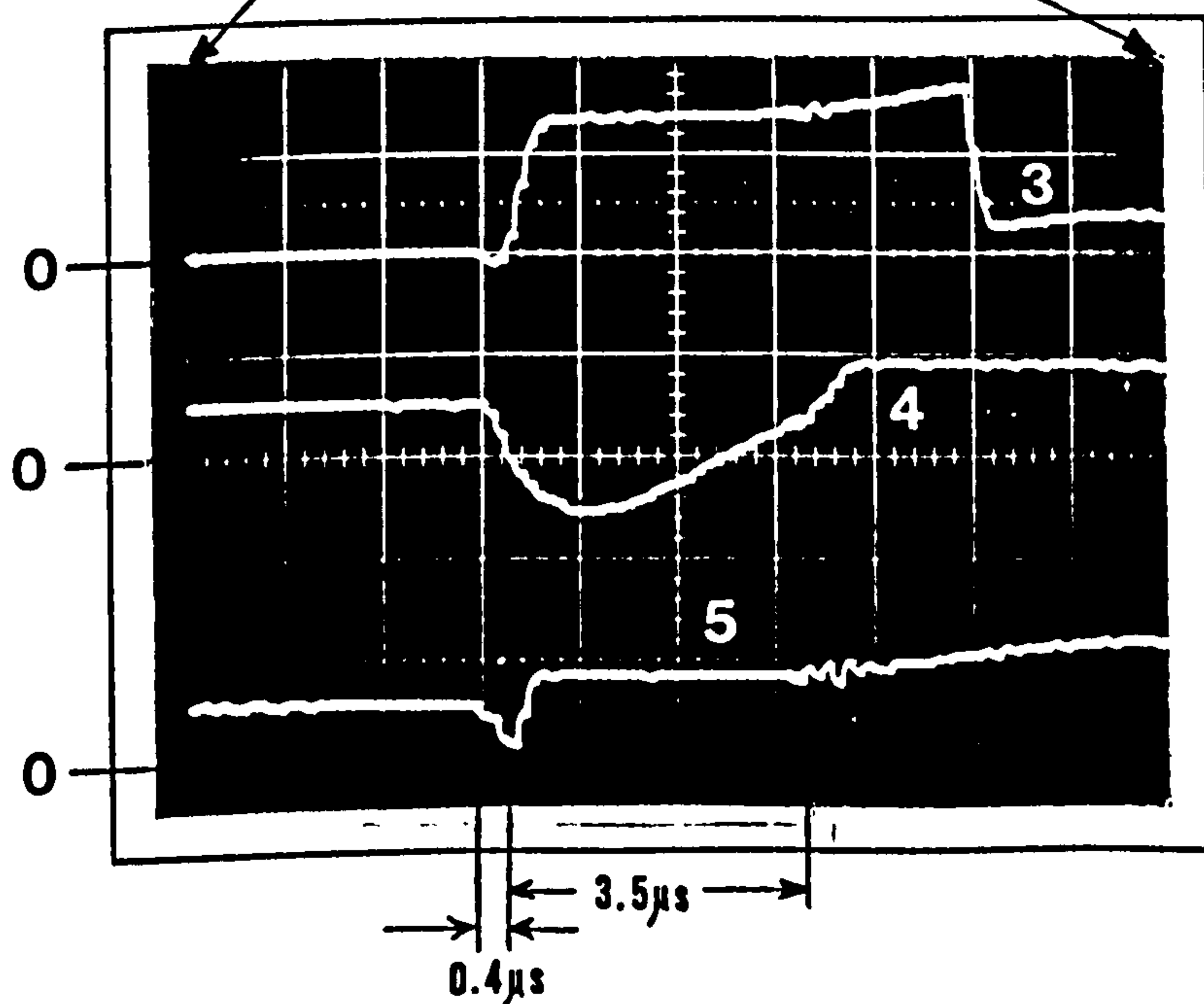


Figure 6.10 Delay time compensation for a fault occurrence when GTO conducting full load current



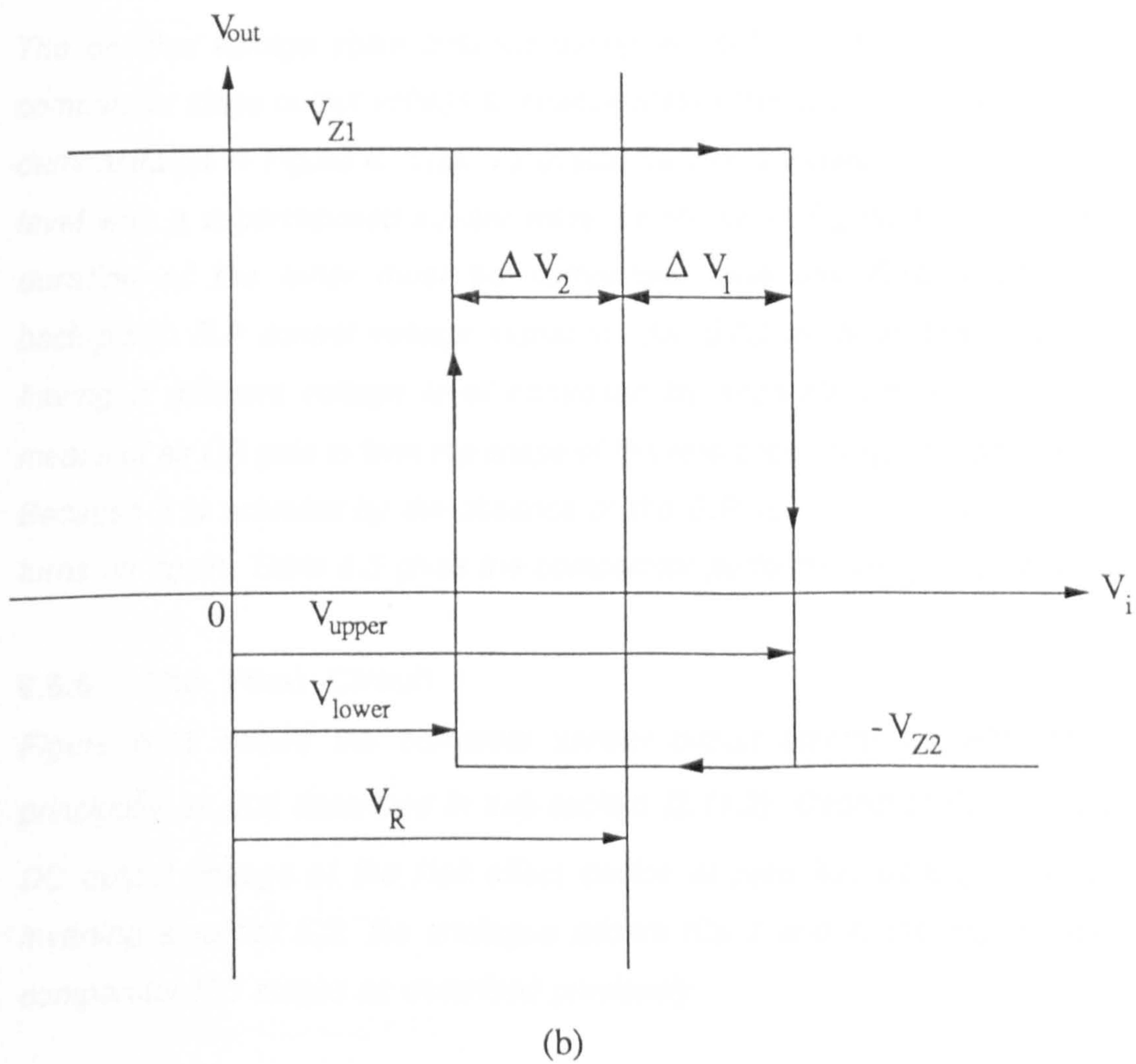
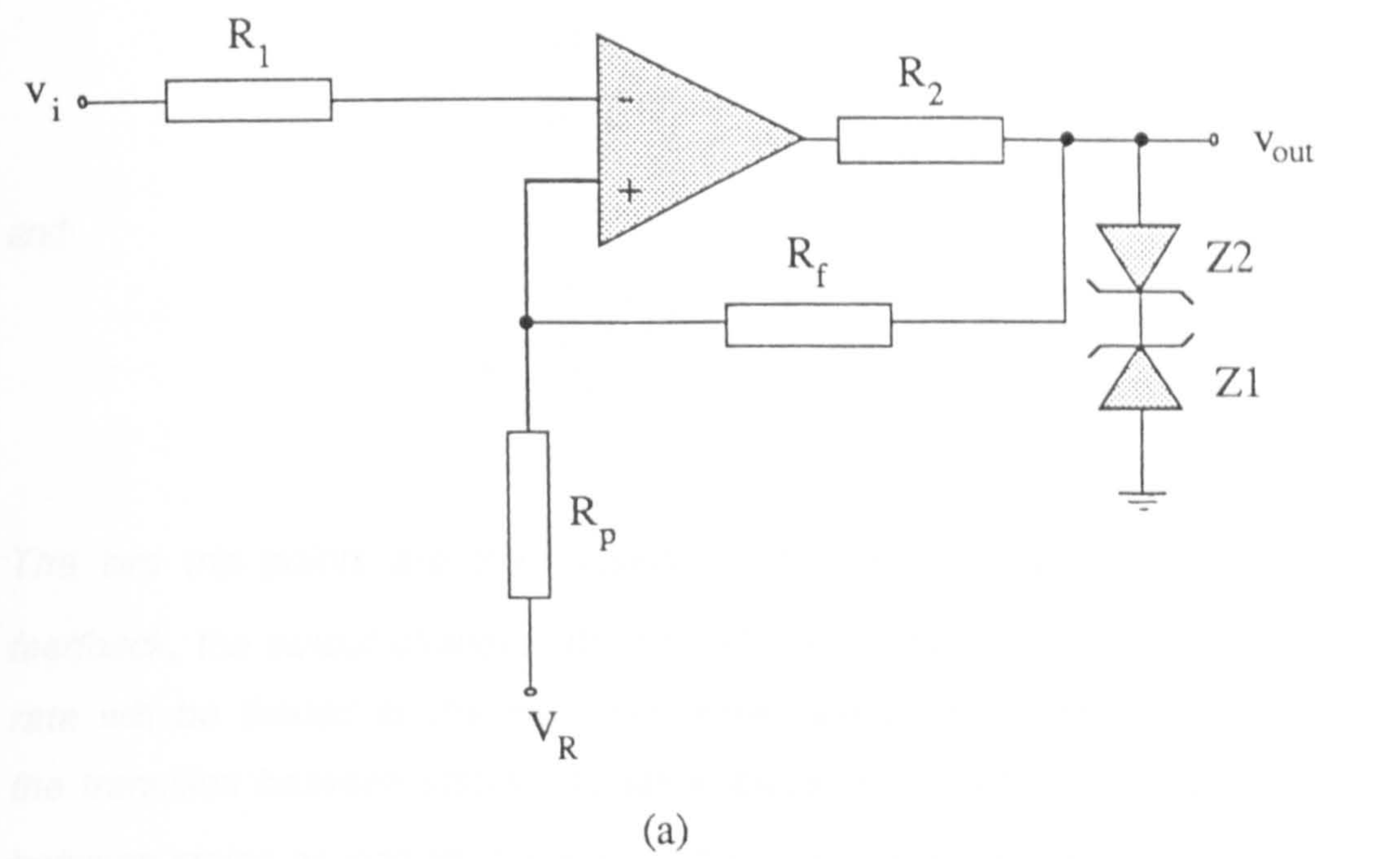


Figure 6.11 (a) Inverting level detector with hysteresis  
(b) Transfer function for (a)

$$\Delta V_1 = \frac{R_p V_{Z1}}{R_p + R_f} \quad (6.11)$$

and

$$\Delta V_2 = \frac{R_p V_{Z2}}{R_p + R_f} \quad (6.12)$$

The two trip points are then  $V_R + \Delta V_1$  and  $V_R - \Delta V_2$ . Since the circuit has positive feedback, the output changes abruptly whenever the trip points are exceeded. The slew rate will be limited to the maximum slew rate of the operational amplifier [41]. Once the transition between states has taken place, noise will not cause the output to chatter between states as long as the noise in the input voltage  $v_{in}$  is less than  $\Delta V_1 + \Delta V_2$ .

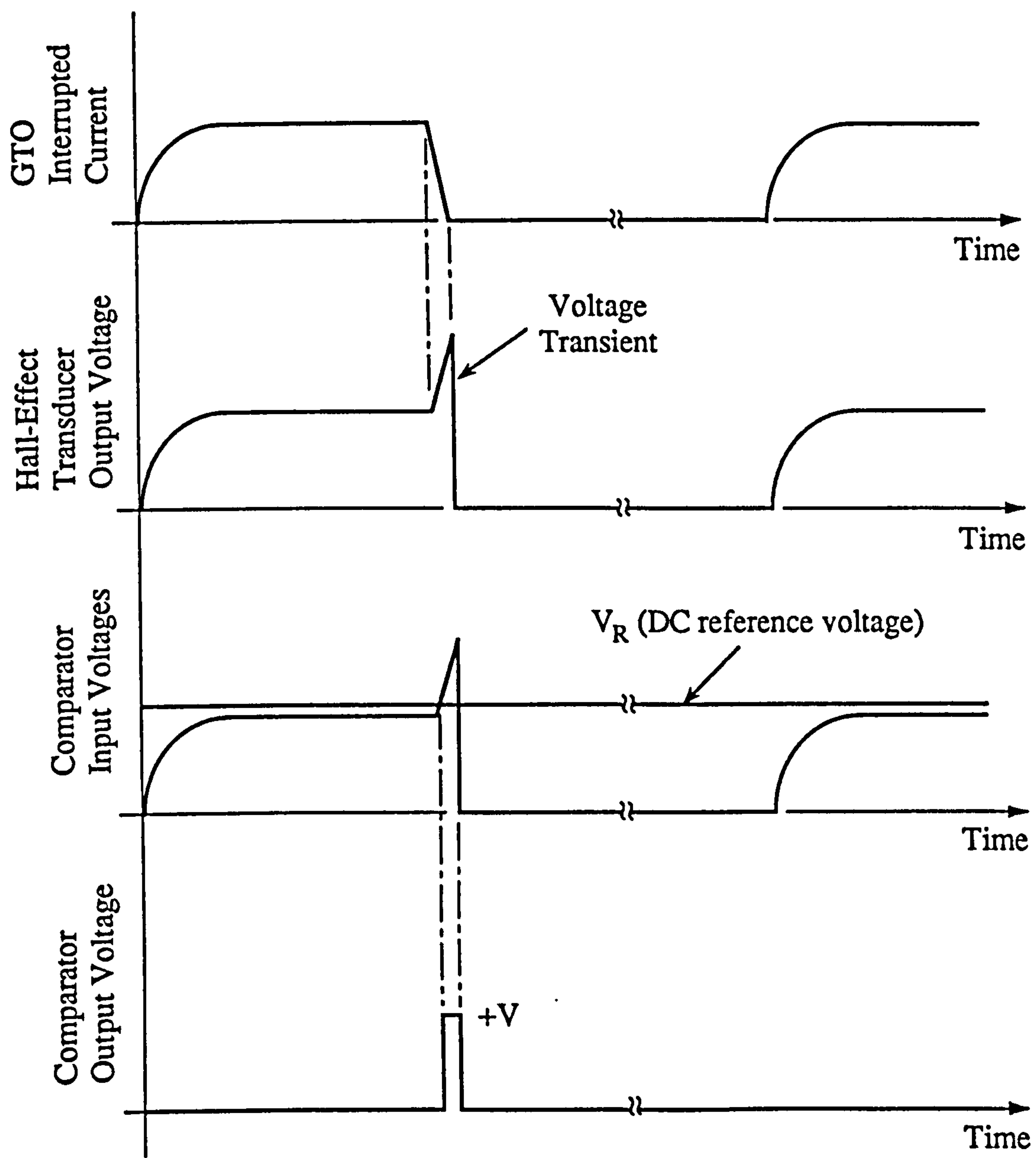
The positive voltage spike induced during the GTO thyristor turn-off would cause the comparator stage output voltage to change state when a DC reference voltage is used, as demonstrated in Figure 6.12(a). To overcome this, a reference voltage comprising a DC level with a superimposed square wave as shown in Figure 6.12(b) is used. Since the duration of the latter must be compatible with any GTO mark/space ratio, the back-porch B.P control voltage signal for the GTO thyristor and its complement, each having a different voltage level controlled by separate amplifiers, are combined by means of an OR gate to form the shape of this reference voltage enhancement square wave. Because it is actuated by the absence of the B.P voltage, it remains high until the GTO turns on again. Table 6.3 gives the comparator performance figures obtained.

#### 6.6.6 The Final Circuit

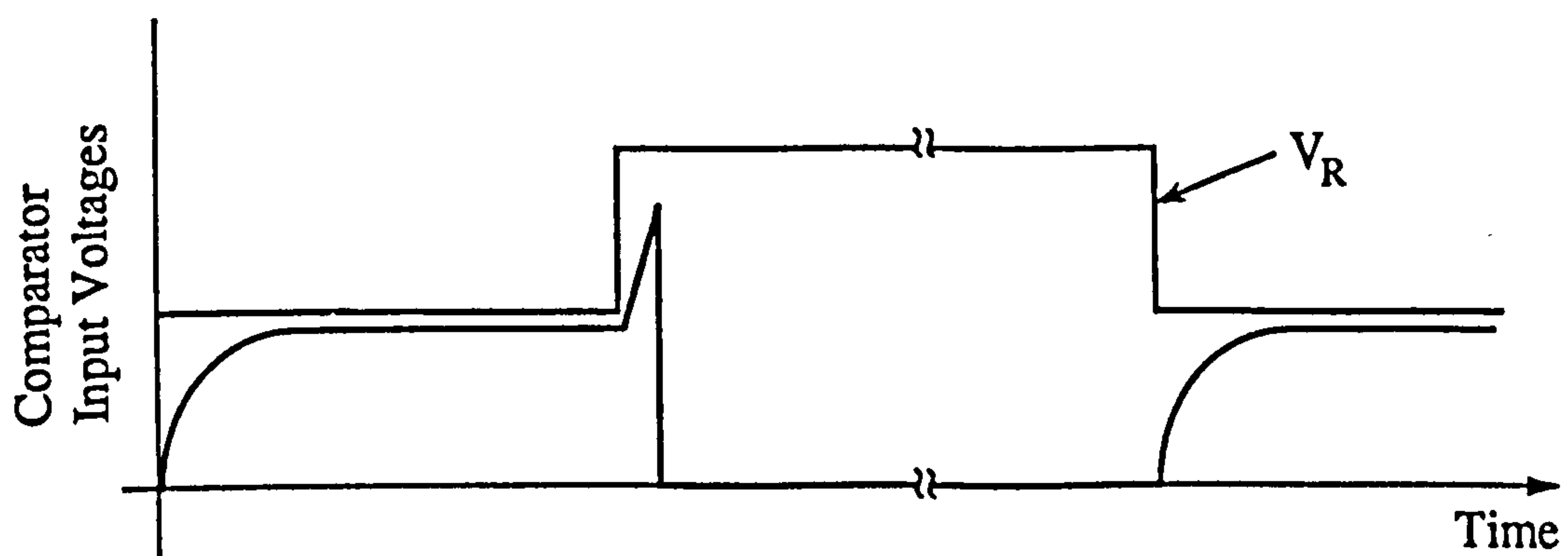
Figure 6.13 shows the complete sensor circuit electronics with its power supply principally as that described in sub-section (2.11.2). Capacitor  $C_b$  is used to block the DC output voltage of the Hall effect device at zero flux density. The adjustable gain inverting amplifier IC2, the analogue adders ICs 1 and 4, the monostable IC3 and the comparator IC5 stages as described previously.

Small capacitor  $C_0$  is used for power supply decoupling in each stage to avoid spurious operation from noise. Also the capacitors  $C_{f1}$ ,  $C_{f2}$ ,  $C_{f3}$  and  $C_{f4}$  are used to compensate the effects of the stray capacitance of the wiring, and that of the operational amplifier input [40]. Stray output capacitance can also cause stability problems [40], hence by adding a





(a) DC reference voltage



(b) Enhanced square wave reference voltage

Figure 6.12 The voltage transient of the Hall-effect transducer output voltage

Peak load current to be protected (A)	Trip current (105%) of GTO peak anode current (A)	Compensated inverting amplifier output voltage (V)	$V_R = 5.3V$ (minimum) (equation 6.8 * $A_v$ ) $15V$ (maximum) $R_1 = 470k\Omega$ and $R_p = 10k\Omega$	
			$\Delta V_1$ (equation 6.11) $V_{Z1} = 5.6V$ (V)	$\Delta V_2$ (equation 6.11) $V_{Z2} = 5.6V$ (V)
10	10.50	<div>↑</div> <div>5.0</div> <div>↓</div>	<div>↑</div> <div>0.1</div> <div>↓</div>	<div>↑</div> <div>0.1</div> <div>↓</div>
15	15.75			
20	21.00			
25	26.25			
30	31.50			
35	36.75			
40	42.00			
45	47.25			
50	52.50			
60	63.00			
70	73.50			
80	84.00			
90	94.50			
95	99.75			

Table 6.3 Comparator performance data

small output resistor  $R_{01}$ ,  $R_{02}$ ,  $R_{03}$  and  $R_{04}$  in series with the output, this is isolated.  $R_{04}$  is also a limiter to ZD4 and ZD5 branch current.

Transistors  $T_1$ ,  $T_2$ ,  $T_3$  and  $T_6$  together with zener diodes ZD1, ZD2, ZD3 and ZD6 respectively, are employed to drop the main DC rail potential to the values required by some circuit components. The fast switching transistors  $T_4$ ,  $T_5$ ,  $T_7$  and  $T_8$  are used for voltage signal amplification purposes. Diodes D1 and D2 act as OR gate, and D3 is to clip the negative part of the comparator output voltage.

The sensor final output voltage  $V_s$  of about 5V (high-to-low) is then employed to provide the over-current protection requirements of the GTO and/or the crowbar thyristor gate controls.



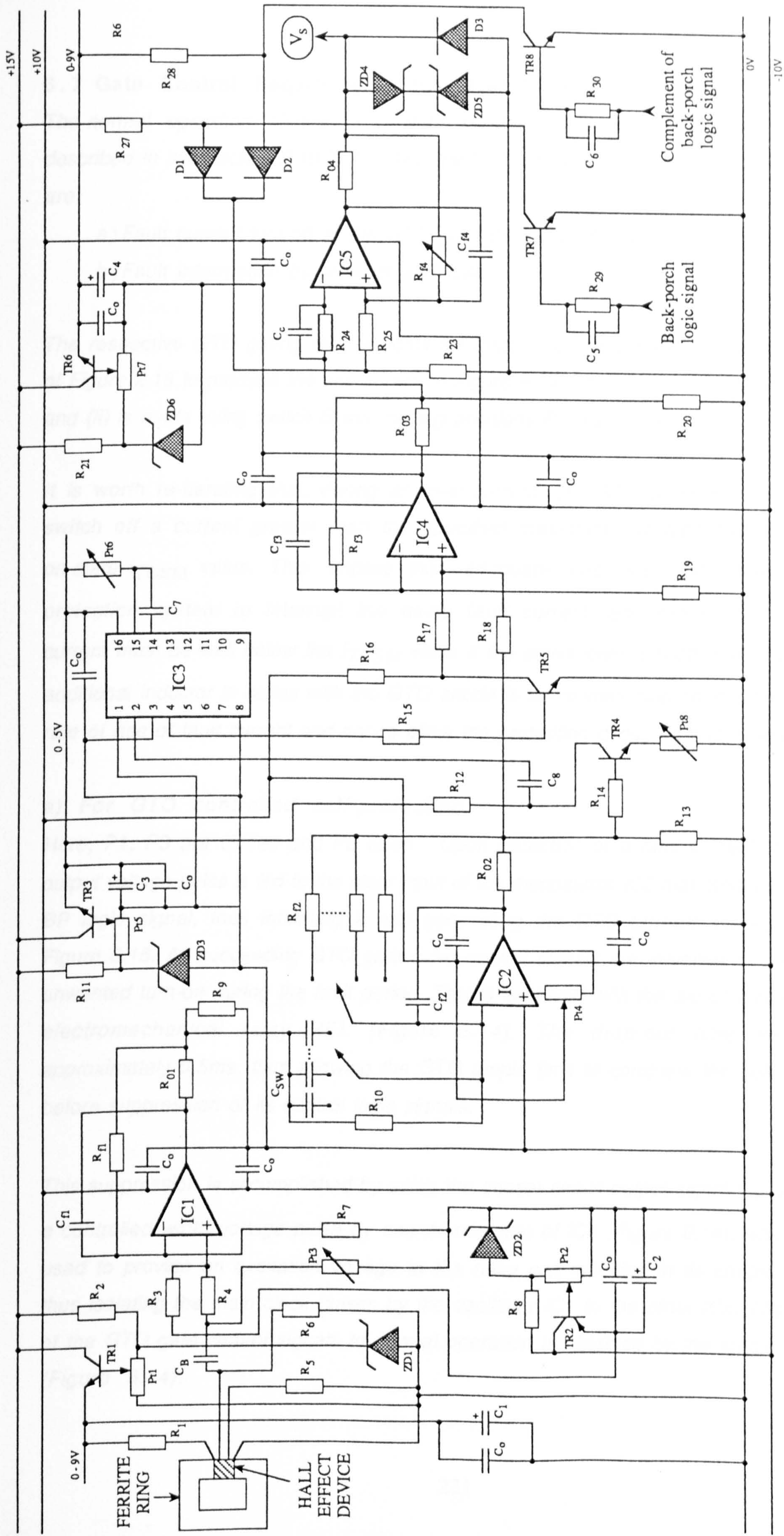


Figure 6.13 Current sensor circuit



## **6.7 Gate Control Requirements for Over-Current Protection**

*The normal operation of the GTO gate control circuit shown in Figure 2.18 is as described in sub-section 2.10.2. The two methods of over-current protection considered are:*

- a) Fault current turn-off at the GTO gate by self-protection.*
- b) Fault interruption by crowbar and fuse.*

*The respective GTO gating requirements for these are incorporated within the circuitry of Figure 2.18 to produce the one shown in Figure 6.14. The choice between methods (i) and (ii) is made using switch S with setting positions P1, P2 and P3.*

*It is worth re-iterating that, during an over-current, the GTO must not be forced to switch off a current greater than the specified maximum non-repetitive controllable on-state  $I_{TCSM}$  value. This implies that adequate time must be allowed for the protection system to interrupt the rising fault current, and the normal operating current must be well below the  $I_{TCSM}$  value if the active gate turn-off is considered. An additional inductor in series with the GTO anode is sometimes needed to slow down the rate of rise of fault current and hence allow the protection circuit time to operate.*

### **a) For GTO controlled self-protection.**

*Here, P1, P3 are closed and P2 open. Upon detection of a fault current, the sensor output voltage pulse is fed to the clear input of the monostable IC2 that produces the GTO BP logic signal, thus inhibiting it and generating the GTO turn-off signal, shown in Figure 6.15. All succeeding GTO gate drive control signals are inhibited to prevent any unwanted turn-on during the fault period. This is achieved with the aid of a change over electromechanical relay REL (Figure 6.14). The drop-out time for this is approximately 0.5ms, thus allowing the GTO ample time to complete the self-protection before suppression of its control logic signals.*

*This suppression is accomplished by using the sensor circuit output signal  $V_s$  to generate a controlled width voltage pulse by one monostable of IC4 (Figure 6.14), which is then used to provide an excitation voltage to the relay coil resulting in its contact opening, thus isolating the main clock pulses by the oscillator IC1 to the other ICs. The resetting of the GTO gate control signals to normal operation is obtained by the toggle switch SI (Figure 6.14).*



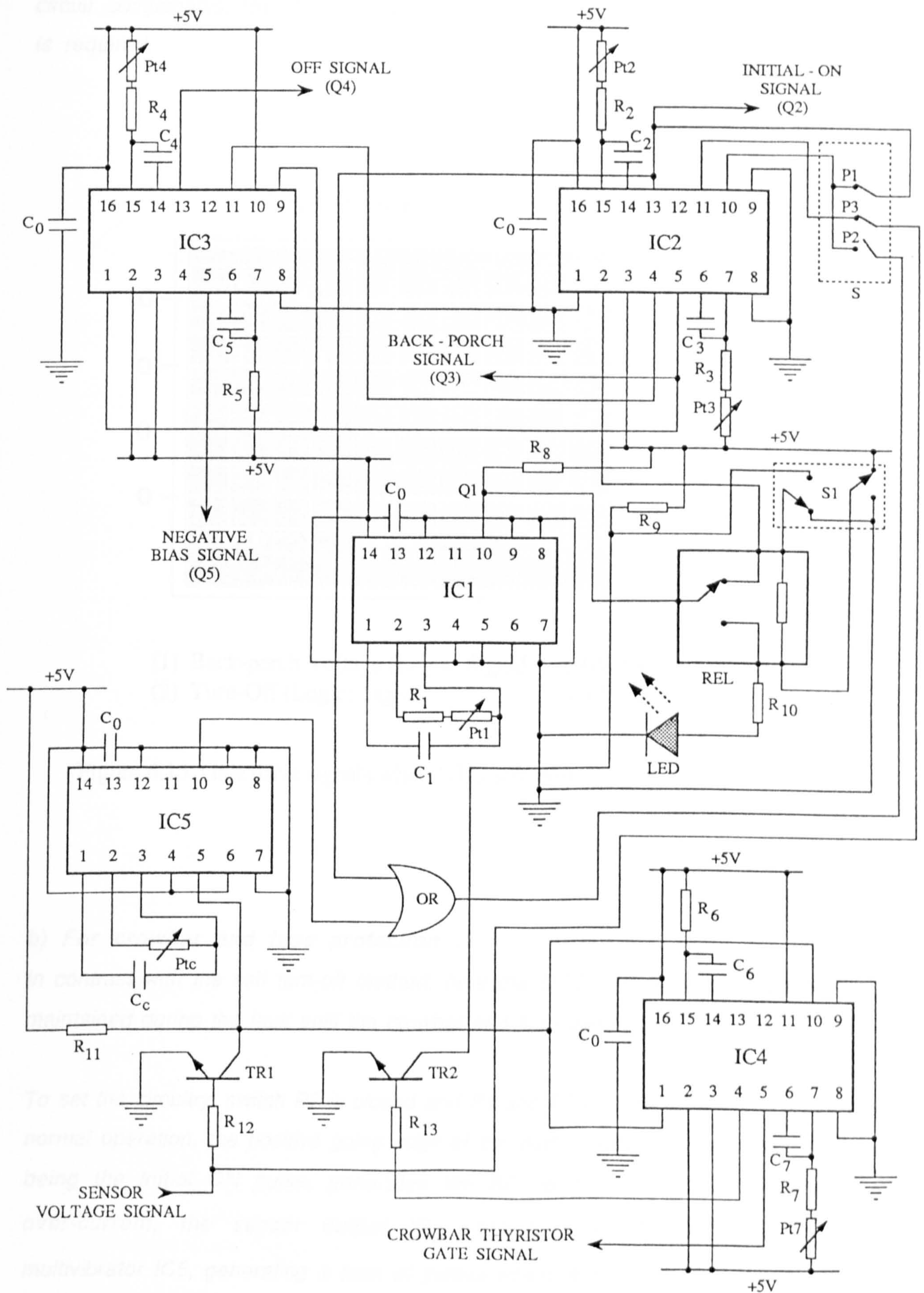
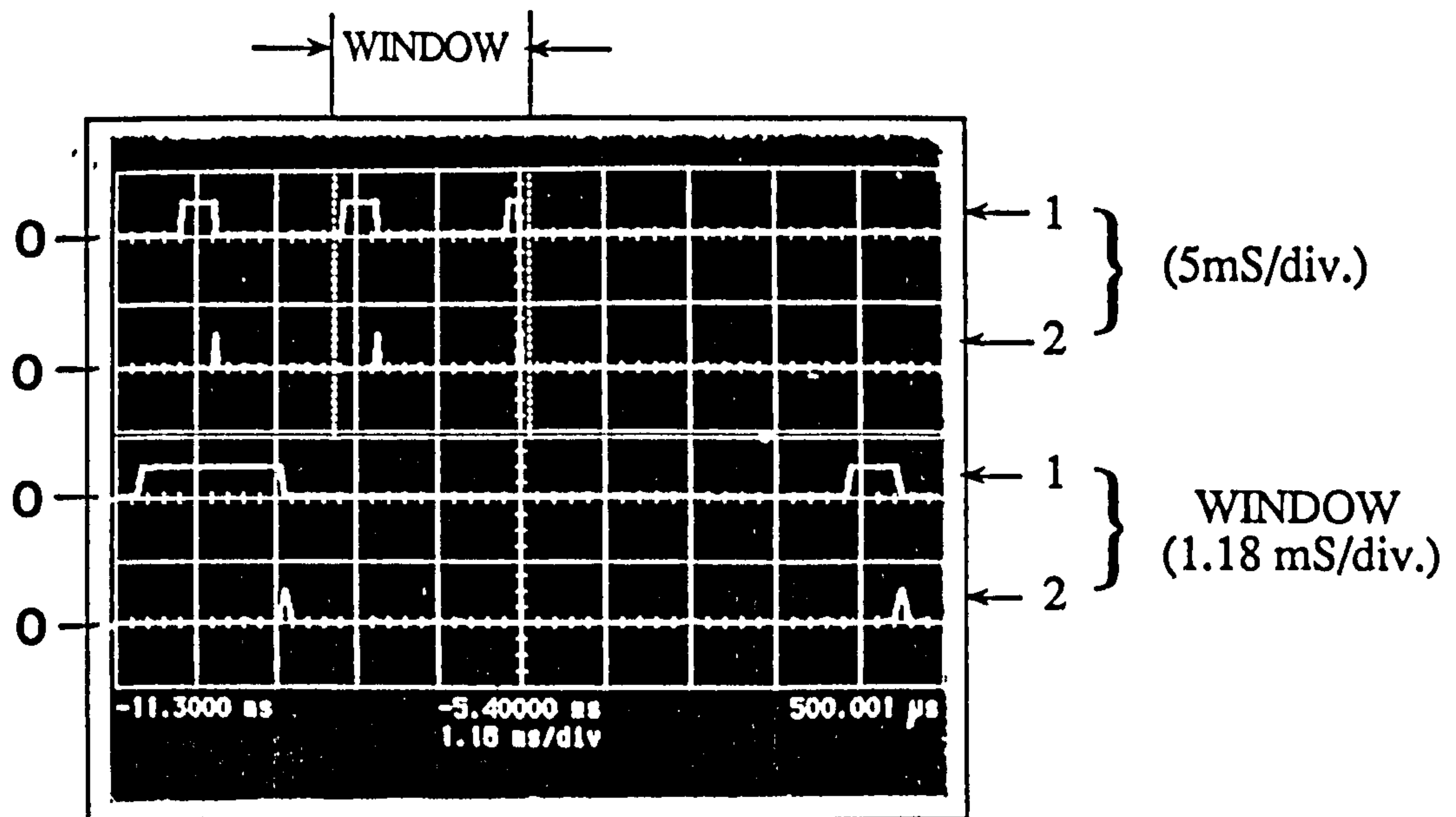


Figure 6.14 The control logic circuitry



An electronic latch may be used in place of the EM relay above, but at the cost of extra circuit components. The latch is better suited when high frequency GTO operation is required.



- (1) Back-porch Voltage (Logic) Signal (10V/div.)  
 (2) Turn-Off (Logic) Signal (10V/div.)

Figure 6.15 Gate drive signals when GTO self-protection method

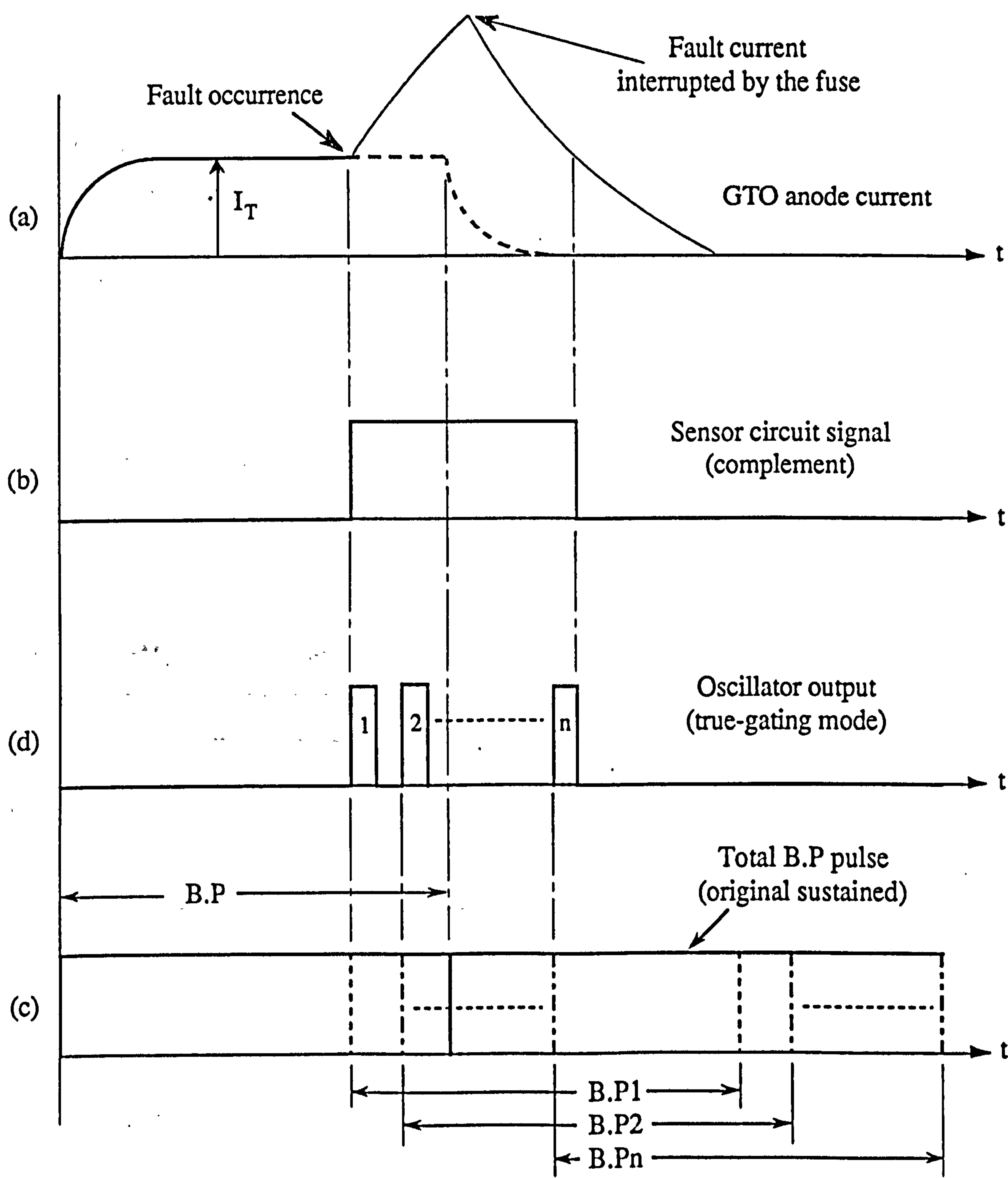
**b) For crowbar and fuse protection .**

In contrast with the self turn-off method, here the GTO back-porch gate drive must be maintained during the fault until the crowbar and fuse operation is complete.

To set the circuitry, switch  $P2$  is closed and  $P1$  and  $P3$  are opened (Figure 6.14). Under normal operation, the positive going edge of the output voltage signal of the OR gate, being the initial ON pulse, generates the BP pulse in IC2. On detection of the over-current, the sensor output ( $V_s$ ) complement ( $\overline{V_s}$ ) is fed to an astable multivibrator IC5, generating a train of pulses which lasts for the duration of the fault. This is illustrated in Figure 6.16 (c). These pulses are then fed to the OR gate whose output triggers the same monostable again with each pulse generating an extra BP signal in conjunction with, and having the same duration as, that of the original BP pulse



(Figure 6.16 (d)). Therefore the BP of the GTO thyristor being protected is sustained until well beyond the clearance of the fault.



B.P = Original Back-Porch Signal  
 B.P1 = Back-Porch Signal Generated by Pulse (1)  
 B.P2 = Back-porch Signal Generated by Pulse (2)  
 B.Pn = Back-Porch Signal Generated by Pulse (n)

Figure 6.16 Gate drive requirements for over-current protection by the crowbar and fuse method

6.8 Crowbar Thyristor Gate Drive

The crowbar thyristor drive control signal, the width of which can be varied between 10μS and 200μS, is produced by the circuit shown in Figure 6.17. A high speed opto-isolated IC1 is employed for isolation from the logic circuitry of Figure 6.14. The output voltage pulse of the opto-isolator IC1(+3.5V) is then amplified and conditioned by the switching transistors TR2 and TR3 (Figure 6.17), before being applied to the gate of the power MOSFET TR4 driving it hard-on for the pulse duration. The crowbar thyristor current pulse has a value set by R7 and Pt3 to about 15A, the di/dt of which is approximately 4A/μS.

6.9 Experimental Results

6.9.1 Test Circuit Details

Results are obtained from tests on the chopper circuits of Figure 6.18. The GTO thyristor employed is Mullard type BTV59 1000R, rated at 15A average, 1KV repetitive peak off-state voltage, and capable of interrupting currents up to 50A. The device  $I_{TCSM}$ ,  $I_{TSM}$  and  $I^2t$  ratings are respectively 80A, 125A and 50 A<sup>2</sup>s. Table 6.4 below provides some of the measured GTO performance data at normal load (R=3Ω and L<sub>F</sub>=100μH), with Figure 6.19 showing some characteristics.

Repetitive on-state current $I_T$ (A)	25	50
Peak negative gate current (A)	9.25	12.5
Approximate negative gate current $di_G/dt$ (A/μS)	25	25
Peak snubber current (A)	23	46
Supply voltage ( $E_d$ ) (V)	78	153
Supply RMS current (A)	9.7	19.4
Storage time ( $t_s$ ) (μS)	0.63	0.86
Fall time ( $t_f$ ) (μS)	0.12	0.25
Overshoot time ( $t_{os}$ ) (μS)	4.5	4.5

Table 6.4 GTO thyristor test data



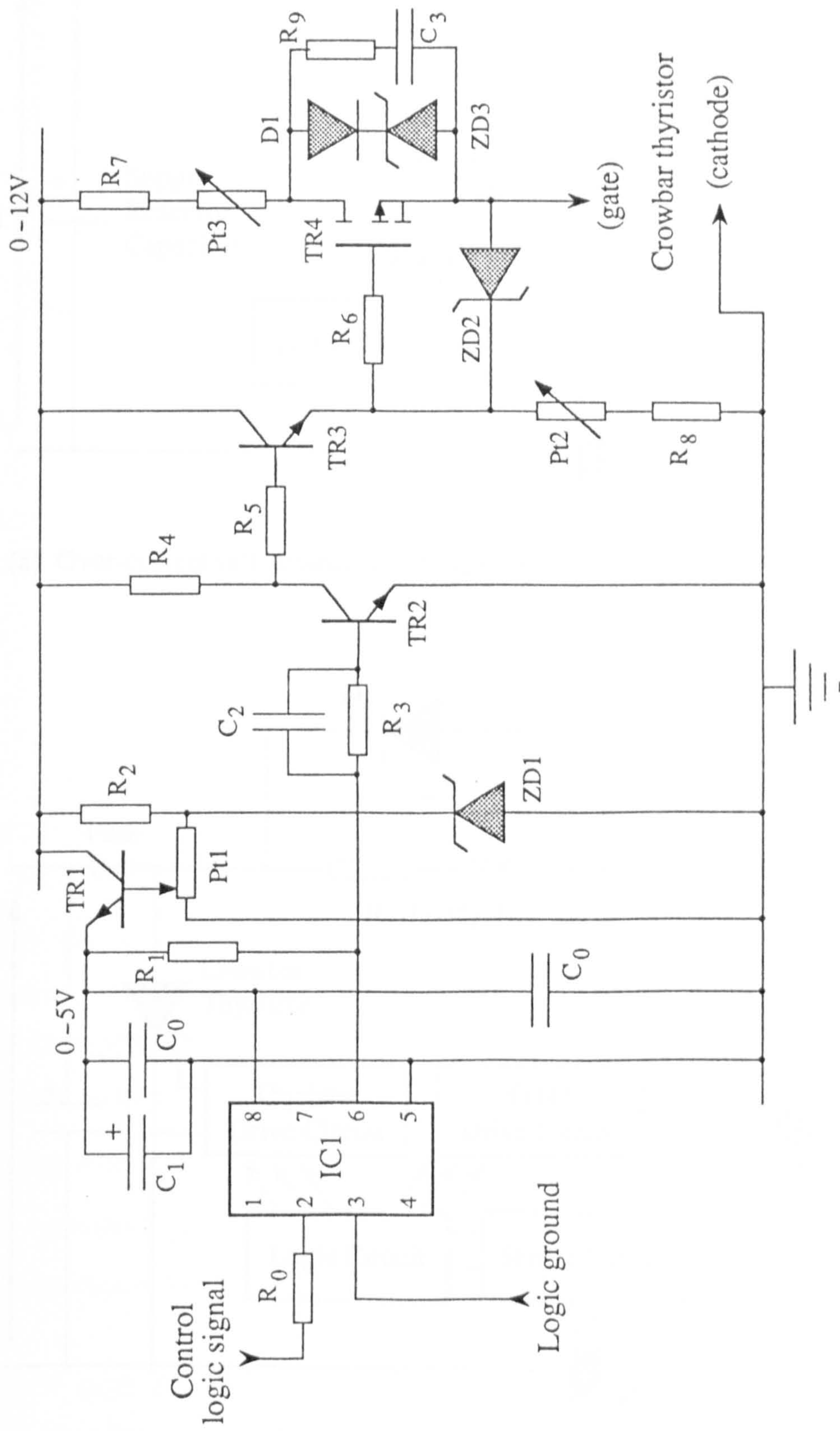
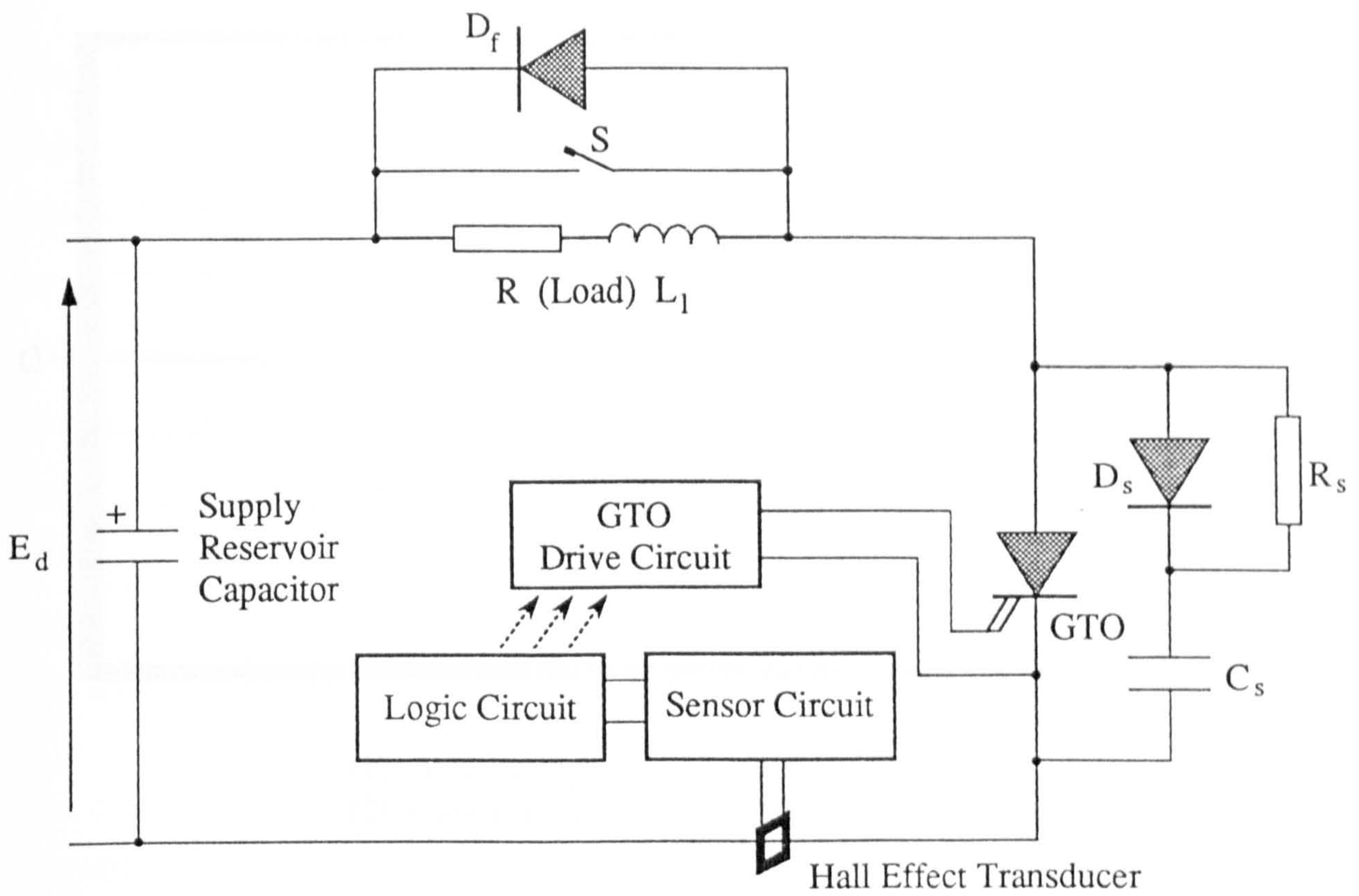
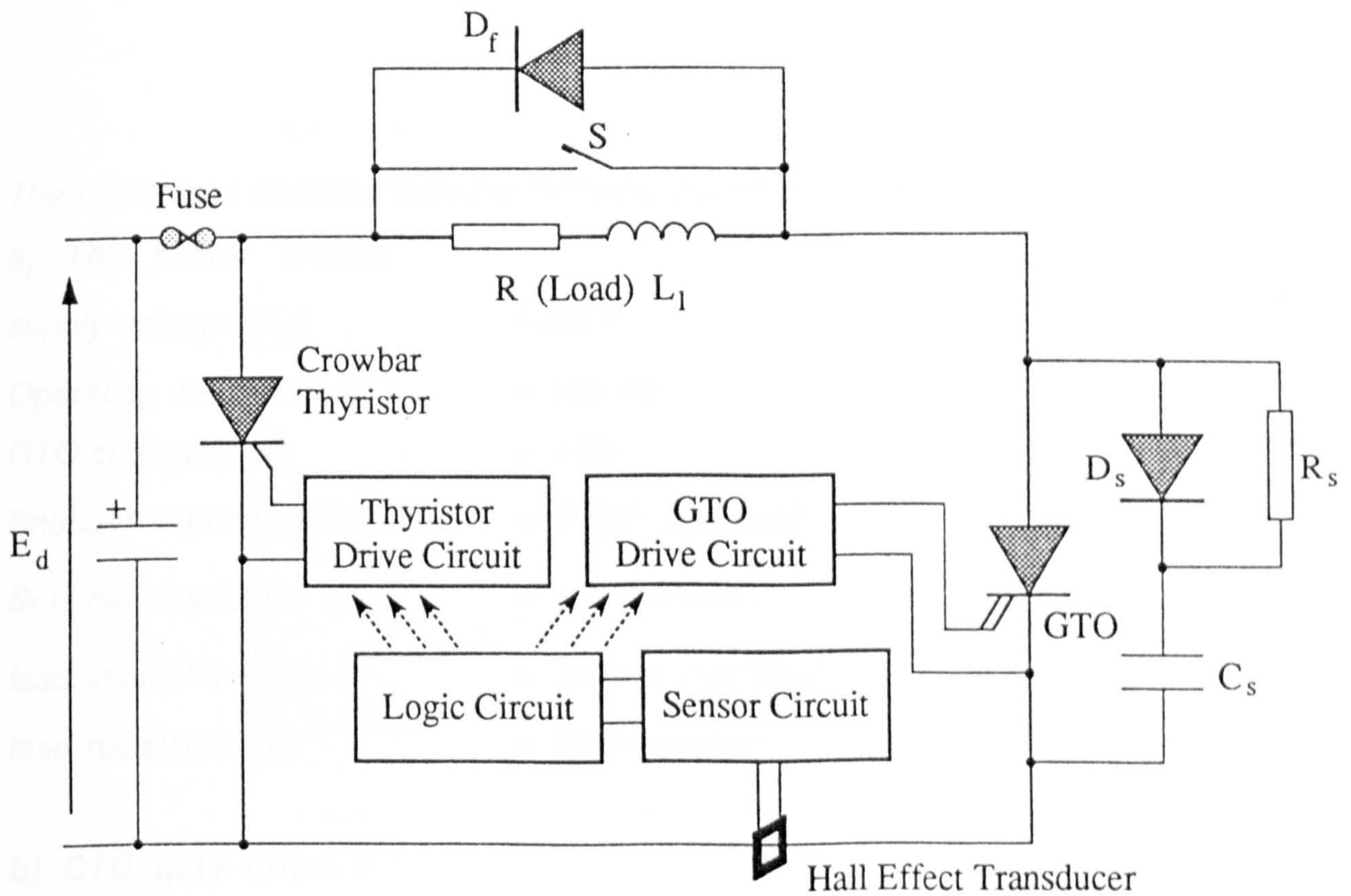


Figure 6.17 Crowbar thyristor gating circuit



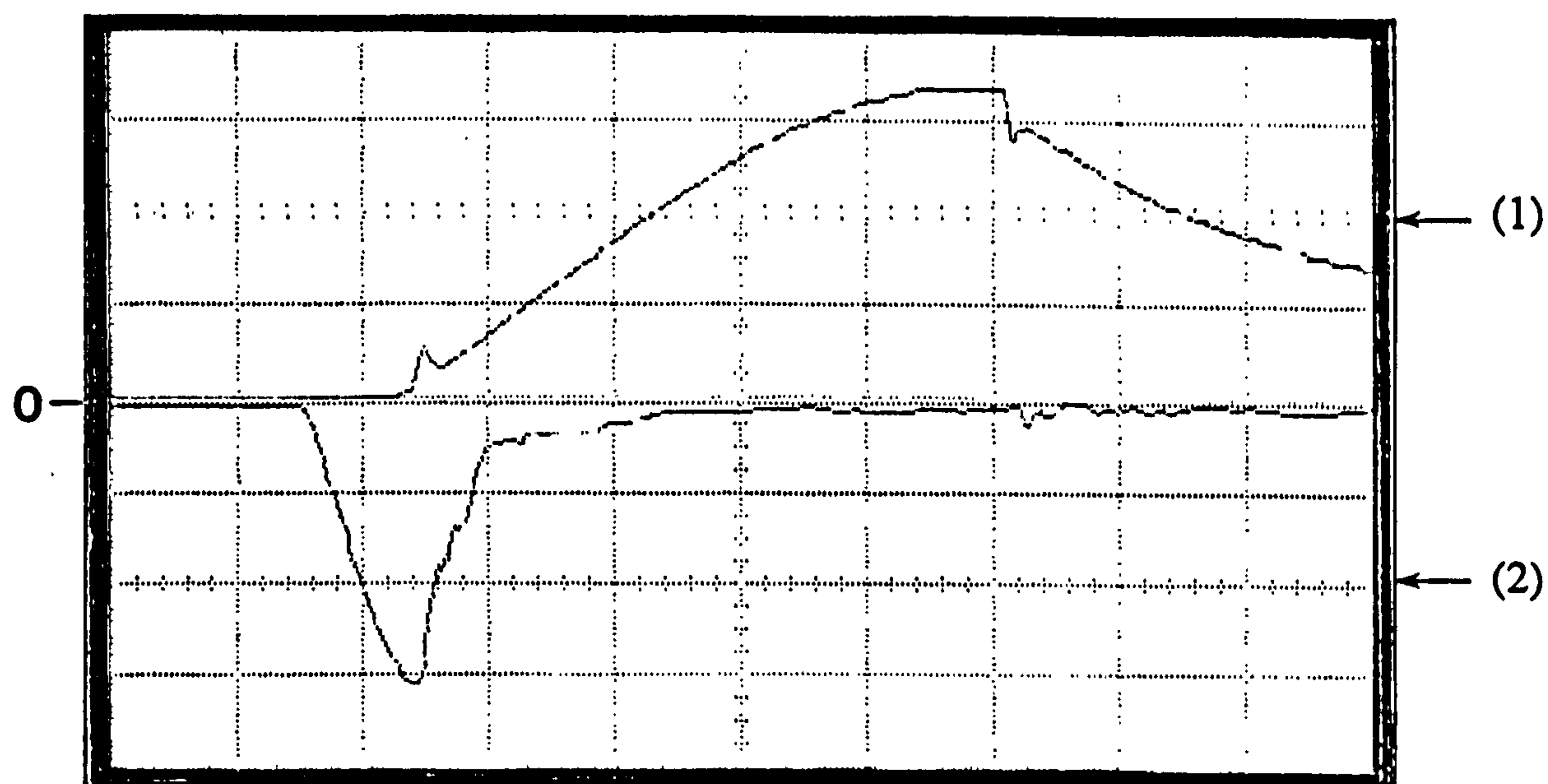
(a) Over-current self-protection for the GTO thyristor



(b) Over-current protection for the GTO thyristor by fuse and crowbar thyristor

Figure 6.18 Test circuits arrangement





(1) A-K Voltage (100V/div.)  
 (2) Gate Current (4A/div.)

Time Scale: 1  $\mu$ S/div.

Figure 6.19 Characteristics of the BTV59 1000R type GTO

*The circuit was operated with the following conditions; unless stated otherwise;*

**a) The power circuit**

supply voltage ( $E_d$ )	= 100V
Operating frequency ( $f$ )	= 100 Hz
GTO duty cycle ( $\delta$ )	= 15%
Snubber capacitor ( $C_s$ )	= 0.5 $\mu$ F (nominal)
Snubber resistance ( $R_s$ )	= 5 $\Omega$ (nominal)
load inductance ( $L_l$ )	= 100 $\mu$ H (nominal)
load resistance ( $R$ )	= 3 $\Omega$ (nominal)

**b) GTO gate drive**

Initial on current pulse (IOP)	= 1.5A rising at 2.5A/ $\mu$ S with 13 $\mu$ S duration
Back-porch current (BP)	= 0.6A
Negative turn-off voltage pulse	= 11V (13V under self protect condition)
Negative gate current di/dt	= 25A/ $\mu$ S (30A/ $\mu$ S under self protect condition)
Negative bias voltage (NB)	= 4V

The total propagation delays of the electronic circuitries are as follow:

Logic (control signals) circuit delay ( $t_l$ )  $\approx 0.4\mu S$  (measured).

Sensor circuit uncompensated delay  $\approx 5.5\mu S$  (estimated).

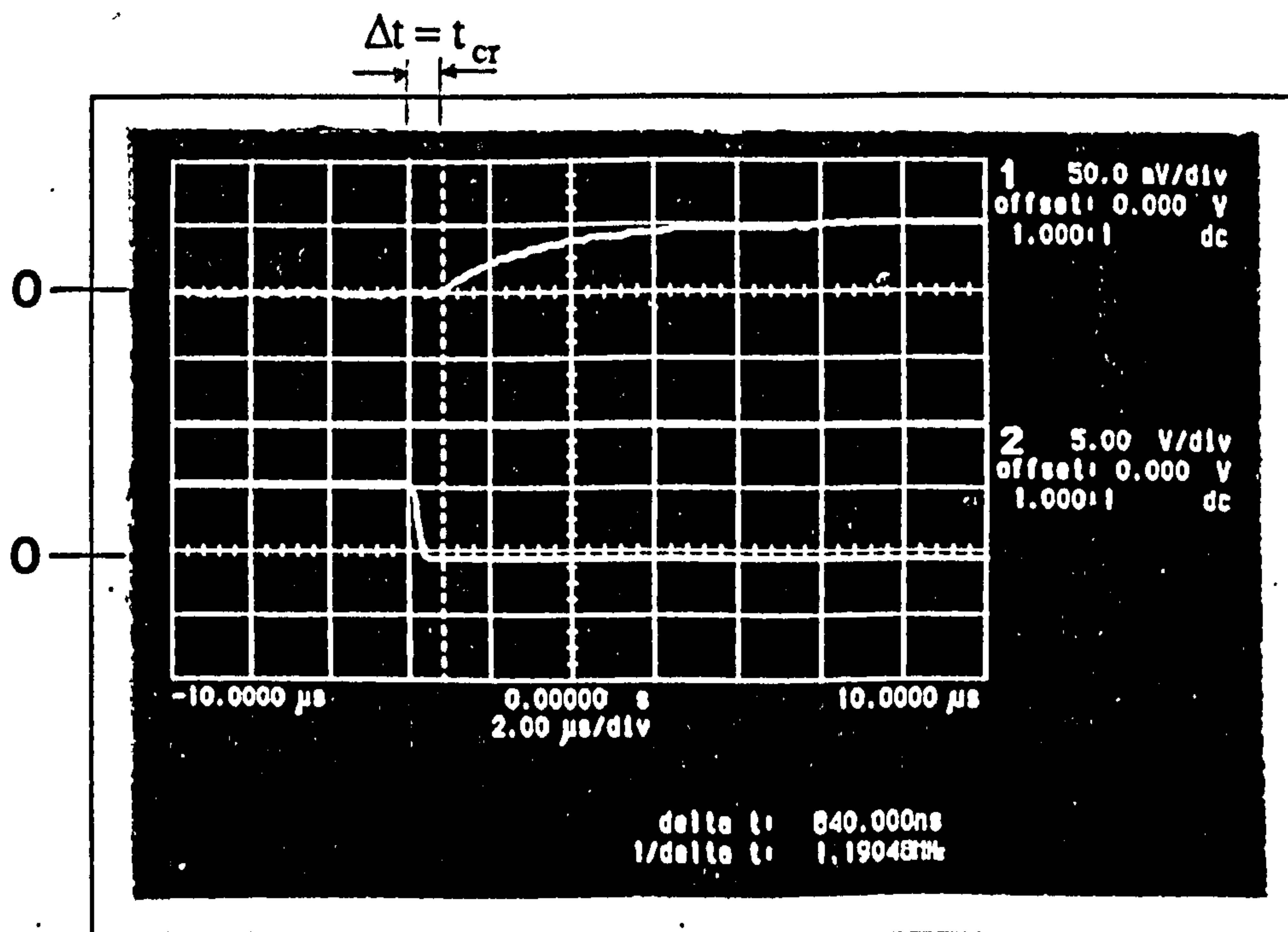
Sensor circuit effective compensated delay ( $t_{se}$ )  $= 0.8\mu S$  (measured, Figure 6.20 (c)).

Crowbar thyristor gate drive circuit delay ( $t_{cr}$ )  $= 0.84\mu S$  (measured, Figure 6.20 (a)).

GTO gate drive circuit delay ( $t_d$ )  $= 1.0\mu S$  (measured, Figure 6.20 (b)).

The snubber current rise denotes the GTO turn-off in Figures 6.20(b) and 6.10.

The experimental measurements are performed with the protection set for peak load current of 30A (Table 6.3). The fault is introduced by shorting the load by the mechanical switch S shown in Figure 6.18.



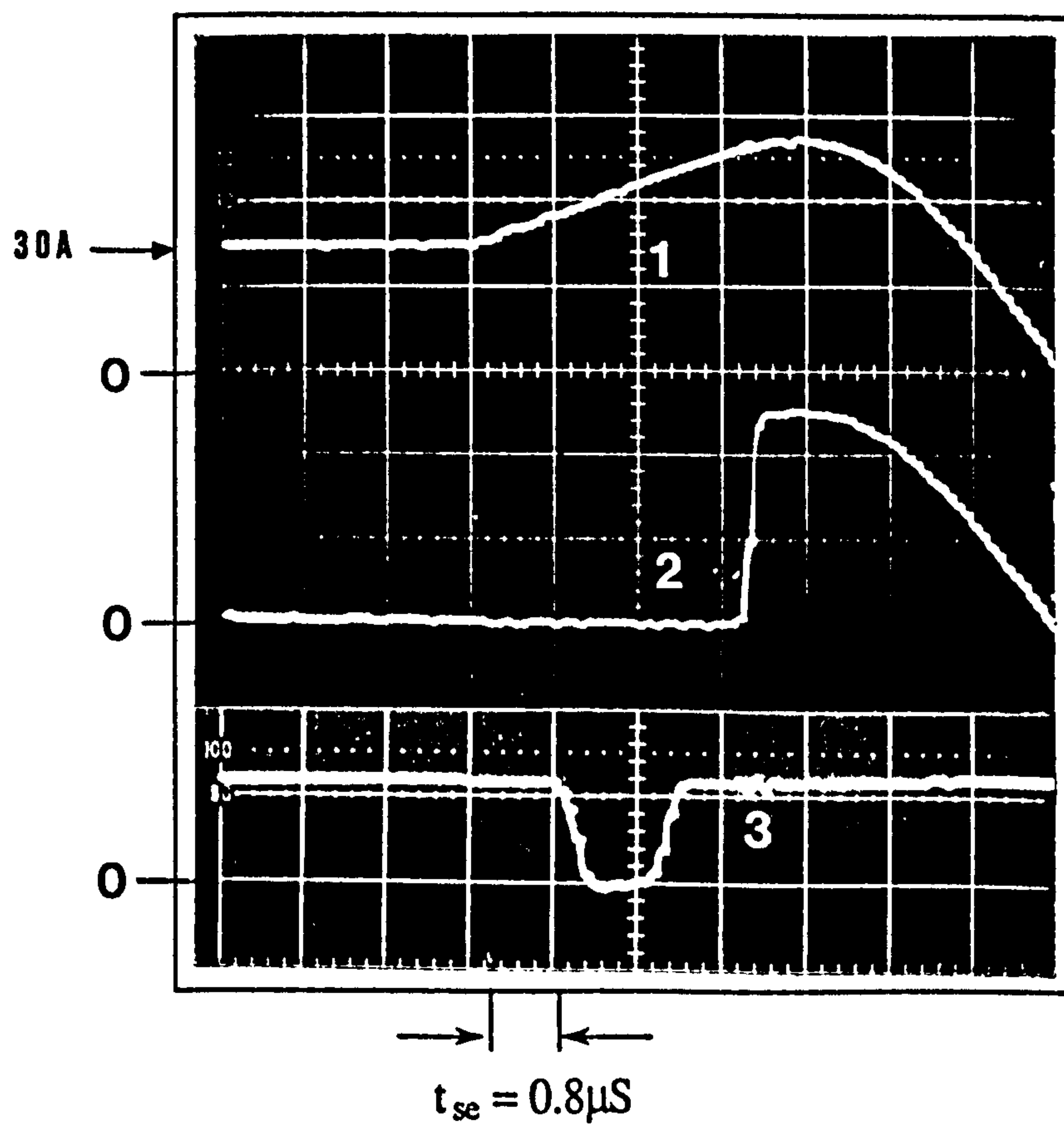
- (1) Crowbar thyristor Gate Current Pulse (10A/div.)  
(2) Sensor Circuit Output Voltage (5V/div.)

Time Scale: 2 μS/div.

(a) Crowbar thyristor gate drive circuit propagation delay

Figure 6.20 Electronic circuit propagation delay



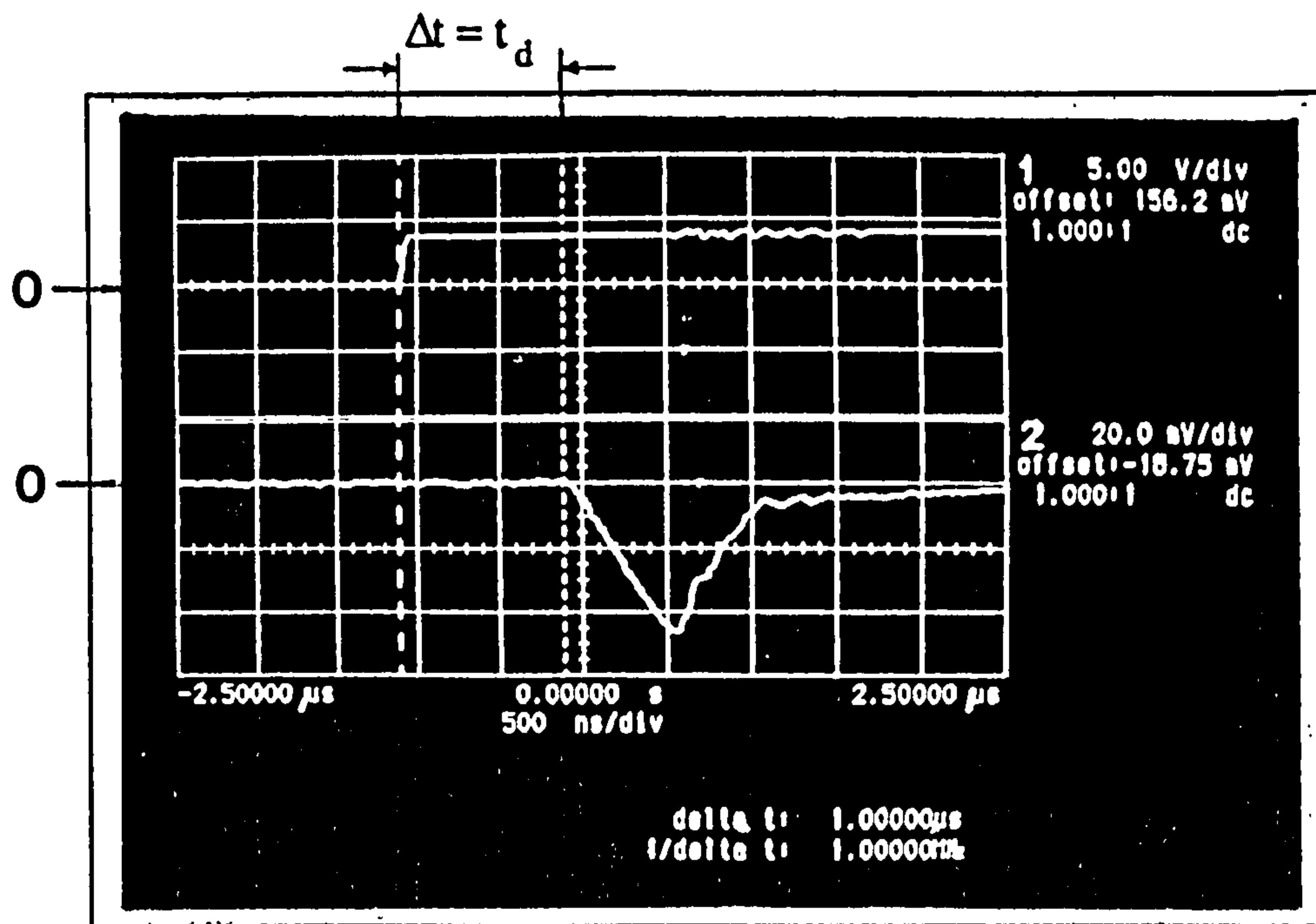


- (1) GTO Branch Current (20A/div.)
- (2) GTO Snubber Current (20A/div.)
- (3) Sensor Circuit Voltage Signal (5V/div.)

Time Scale: 1  $\mu S$ /div.

(b) Sensor circuit propagation delay (effective)

Figure 6.20 Electronic circuit propagation delay



- (1) Turn-Off Logic Signal (5V/div.)  
 (2) GTO Negative Gate Current (5A/div.)

Time Scale: 0.5 μs/div.

(c) GTO thyristor gate drive circuit propagation delay

Figure 6.20 Electronic circuit propagation delay

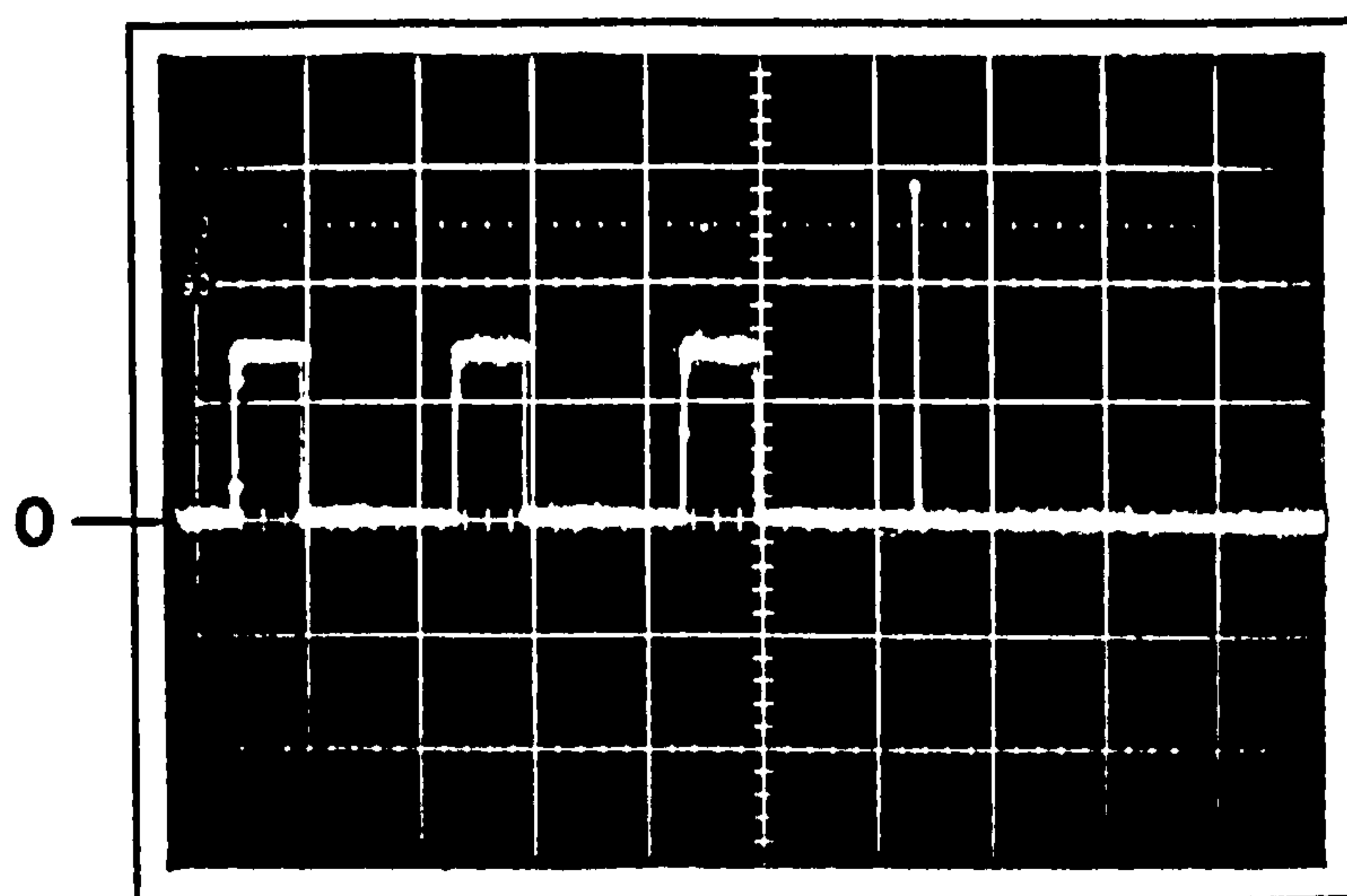
### 6.9.2 GTO Self-Protection Performance

Figure 6.21 shows the observed waveforms when the GTO is switched into a short-circuit (case 1) and when one is applied across the load during load current flow (case 2). In both cases, the fault current initially rises at about 7.6 A/μs (Figure 6.21(b) and (d), trace 1) from a 95 V supply. The stray circuit inductance of 13 μH adequately limiting the di/dt.

The fault current is detected at 31.5 A for either case and the GTO, after a total delay of approximately 3.8 μs and 3.1 μs respectively (Figure 6.21 (b) and (d), trace 1), turns off and clears peak fault currents of about 58 A and 52 A respectively.

The tripping delay components are those in the current sensor circuit ( $t_{sc}$ ), the logic circuit ( $t_l$ ), the gate drive circuit ( $t_d$ ) and the GTO turn-off time ( $t_s + t_f$ ). These add to 3.5 μs and 3.3 μs respectively for cases 1 and 2, with the GTO turn-off times being

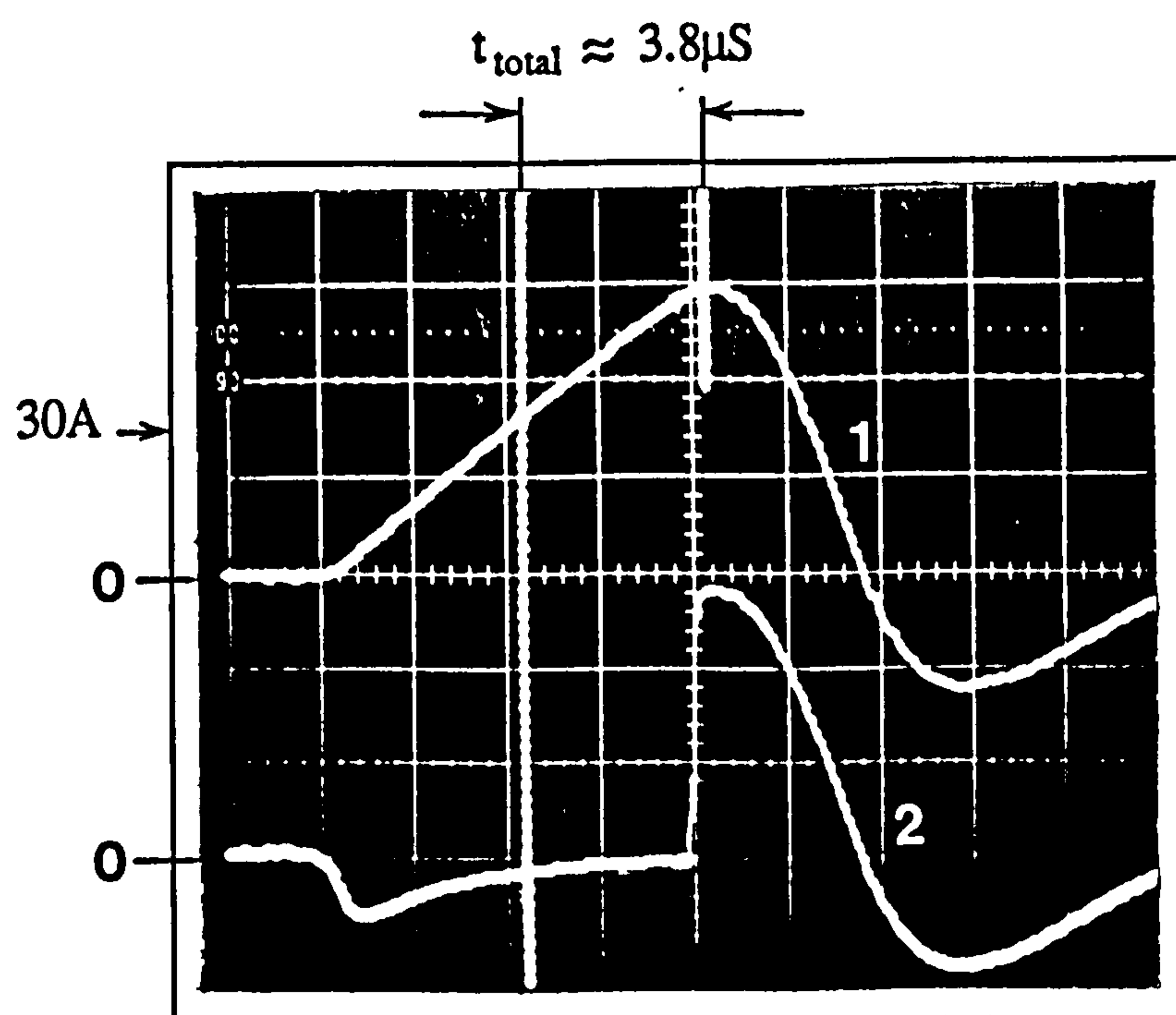




(a) GTO turn-on into a short-circuit

Load Current (20A/div.)

Time Scale: 5mS/div.



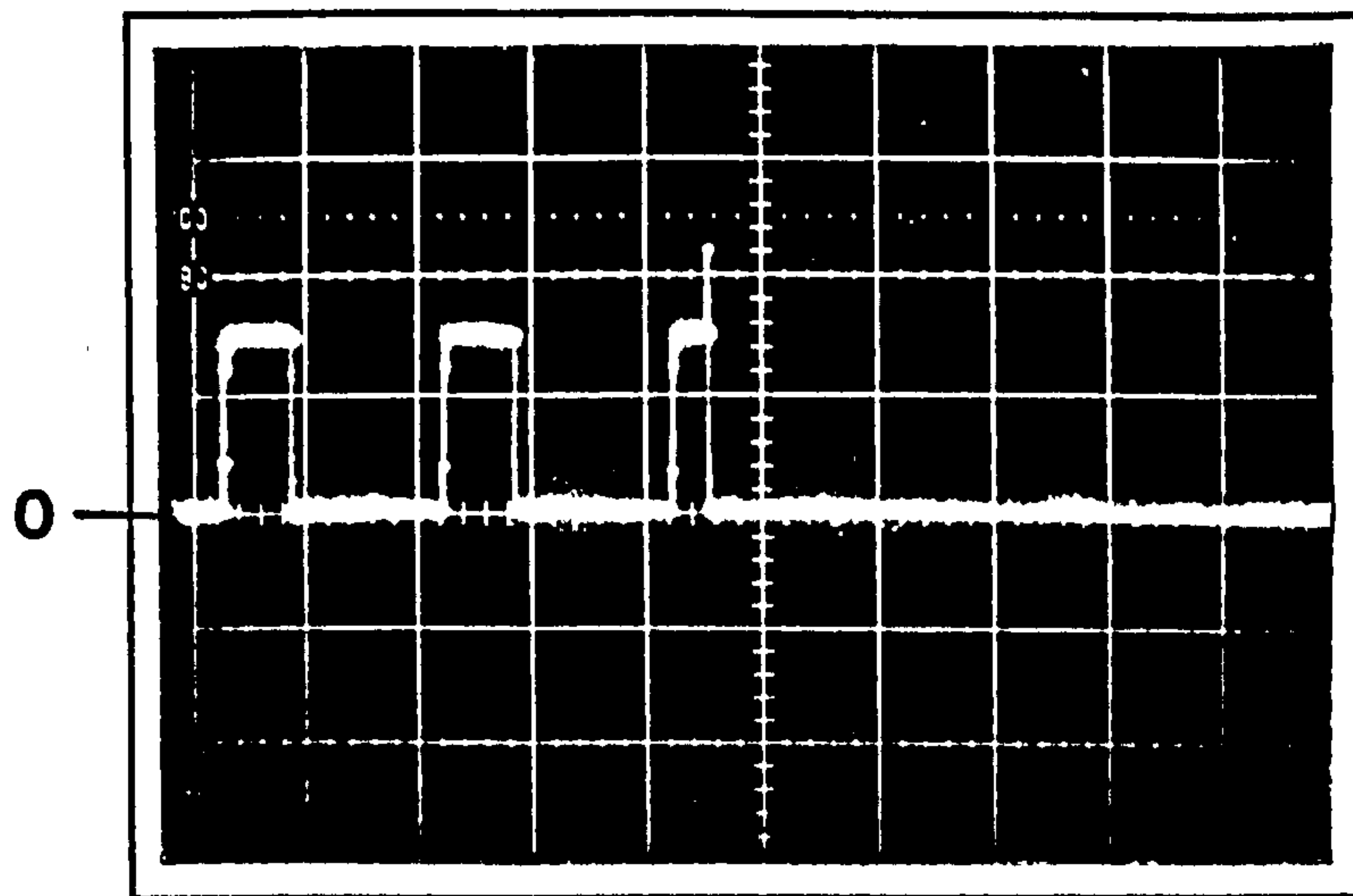
(b) GTO turn-on into a short-circuit

(1) GTO Branch Current (20A/div.)

(2) Snubber Current (20A/div.)

Time Scale: 2 $\mu$ S/div.

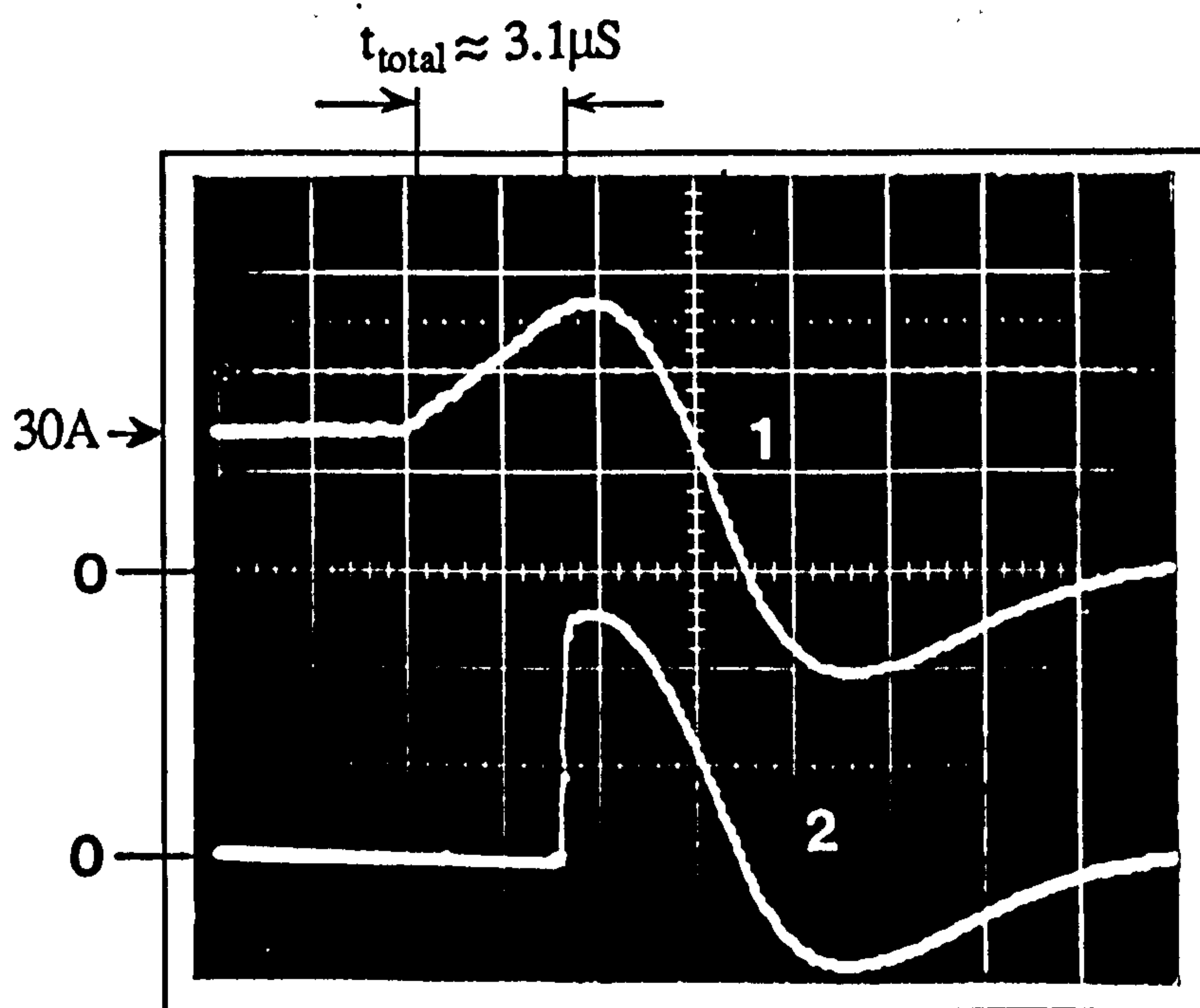
Figure 6.21 Over-current self-protection for the GTO thyristor



(c) Short circuit applied with the GTO conducting full load current

Load Current (20A/div.)

Time Scale: 5mS/div.



(d) Short circuit applied with the GTO conducting full load current

(1) GTO Branch Current (20A/div.)

(2) Snubber Current (20A/div.)

Time Scale: 2 μS/div.

Figure 6.21 Over-current self-protection for the GTO thyristor



1.3 $\mu$ S (estimated) and about 1.1 $\mu$ S (Table 6.4). Thus, their measured total values compare satisfactorily with the summed component values.

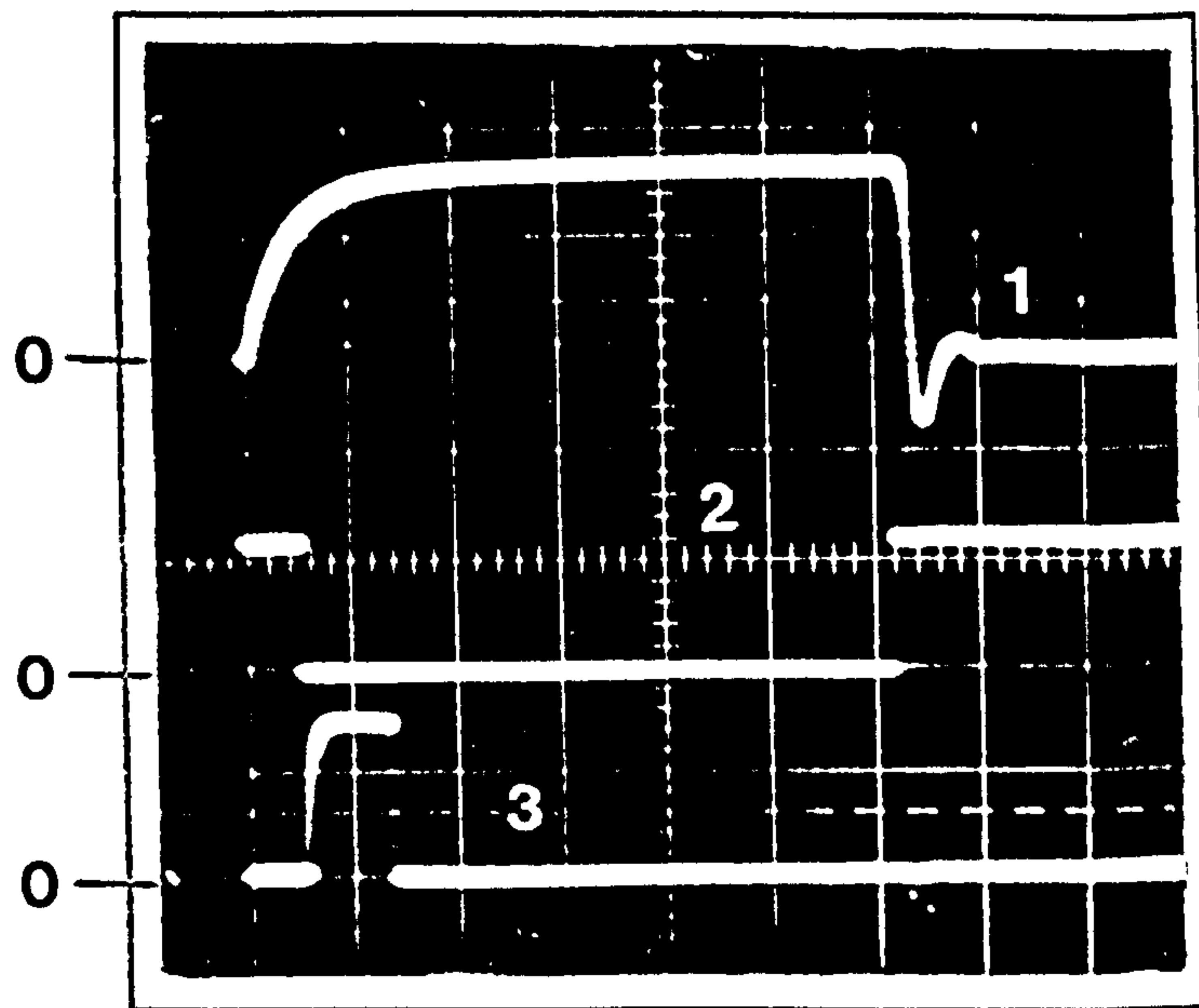
A further important feature is that of attempting to turn-off a GTO before its turn-on is complete. The device develops localised heating due to the high current densities in the cathode islands when turning off very soon after turn-on. Hence, with self-protection, consideration must be given to the above. The problem is helped by applying a very high initial turn-on gate current pulse with a fast  $di/dt$ , thus ensuring rapid turn-on of the cathode regions. Also, if the GTO turns off before the snubber capacitor is fully discharged by the turn-on process, a possible dangerous condition occurs due to excessive  $dv/dt$  following turn-off (see sub-section 2.6.2 (iv)).

### 6.9.3 Crowbar and Fuse Protection Performance

The crowbar thyristor employed is rated at 40A average and 600V, with peak non-repetitive on-state surge current of 600A and a  $I^2t$  rating of 1750A<sup>2</sup>s. Figure 6.22, trace 3, shows the current pulse produced with a shorted gate drive circuit output. It has a 15A magnitude for 40 $\mu$ S duration. When driving the crowbar thyristor, the gate current is limited by the gate impedance to about 0.5A.

The RMS current of the supply when the GTO is conducting a peak load current of 30A for 1ms at 100Hz is about 9.1A. A 10A RMS, 1KV and 65A<sup>2</sup>s semiconductor fuse is employed (Figure 6.18(b)), which has the fastest interruption time that can be considered. The fault current path stray inductance is of a value as indicated in the previous sub-section.

With the protection set for 30A peak load current, a short circuit is applied across the load. Figure 6.23 (a) and (b), shows respectively the behaviour of the GTO for cases (1) and (2). The fault current, having a  $di/dt$  of 7.6A/ $\mu$ S, is again detected at 31.5A for each case, and after a total delay of about 28 $\mu$ S and 25 $\mu$ S for respectively cases (1) and (2), the GTO fault current is interrupted by the fuse with peak values of about 70A and 60A (traces 2 and 3). The latter is lower due to the fuse element carrying full load current prior to the over-current and is therefore quite hot initially. However, Figure 6.23 (a) and (b), trace 2, also shows that the electronic circuit delay time ( $t_l$ ), which comprises the components  $t_{se}$ ,  $t_l$  and  $t_{cr}$ , and the crowbar thyristor turn-on time ( $t_{to}$ ), approximate to a total of 2.3 $\mu$ S for both cases. Addition of the separate components gives 2.6 $\mu$ S which correlates favourably with the observed value.



- |  |            |
|--|------------|
| (1) GTO Branch Current                   | (20A/div.) |
| (2) Comparator (Sensor) Output Voltage   | (5V/div.)  |
| (3) Crowbar Thyristor Gate Current Pulse | (10A/div.) |

Time Scale: 50  $\mu$ S/div.

Figure 6.22 Crowbar thyristor gate drive waveform

*The crowbar current path comprises a stray impedance of  $0.05\Omega$  and  $5.5\mu$ H giving, with a 95V supply, a  $di/dt$  of about  $17A/\mu$ S, and the crowbar current reaches 410A and 360A for cases (1) and (2) respectively, Figure 6.23 (a) and (b), trace 3.*

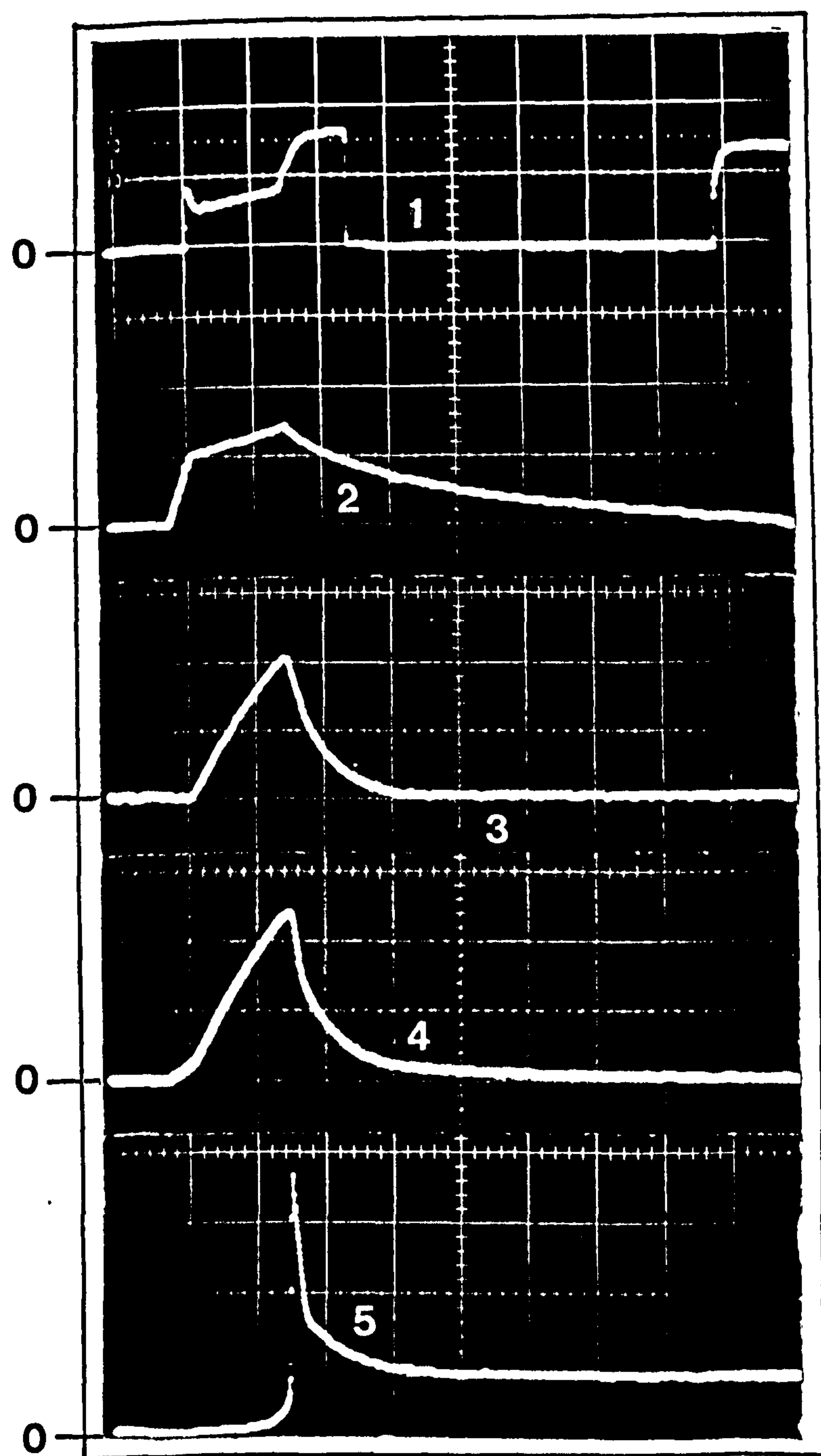
## 6.10 Conclusions

*Detection circuit design and methods of over-current protection have been described, and test results provided. Circuit requirements for active fast controlled GTO self-protection are recorded and indicate that in most applications, the small power circuit inductance is enough to permit over-current protection by gate turn-off.*

*The GTO self-protection method allows reset following a fault interruption, and is particularly appropriate to very short transients because of its much faster response.*

*Fuse protection alone is not usually possible, although with a fast turn-on crowbar thyristor it provides adequate over-current protection, but is slow both in operation and 'reset', i.e. fuse changing.*





(1) Crowbar Thyristor Gate Current Pulse (0.5A/div.)

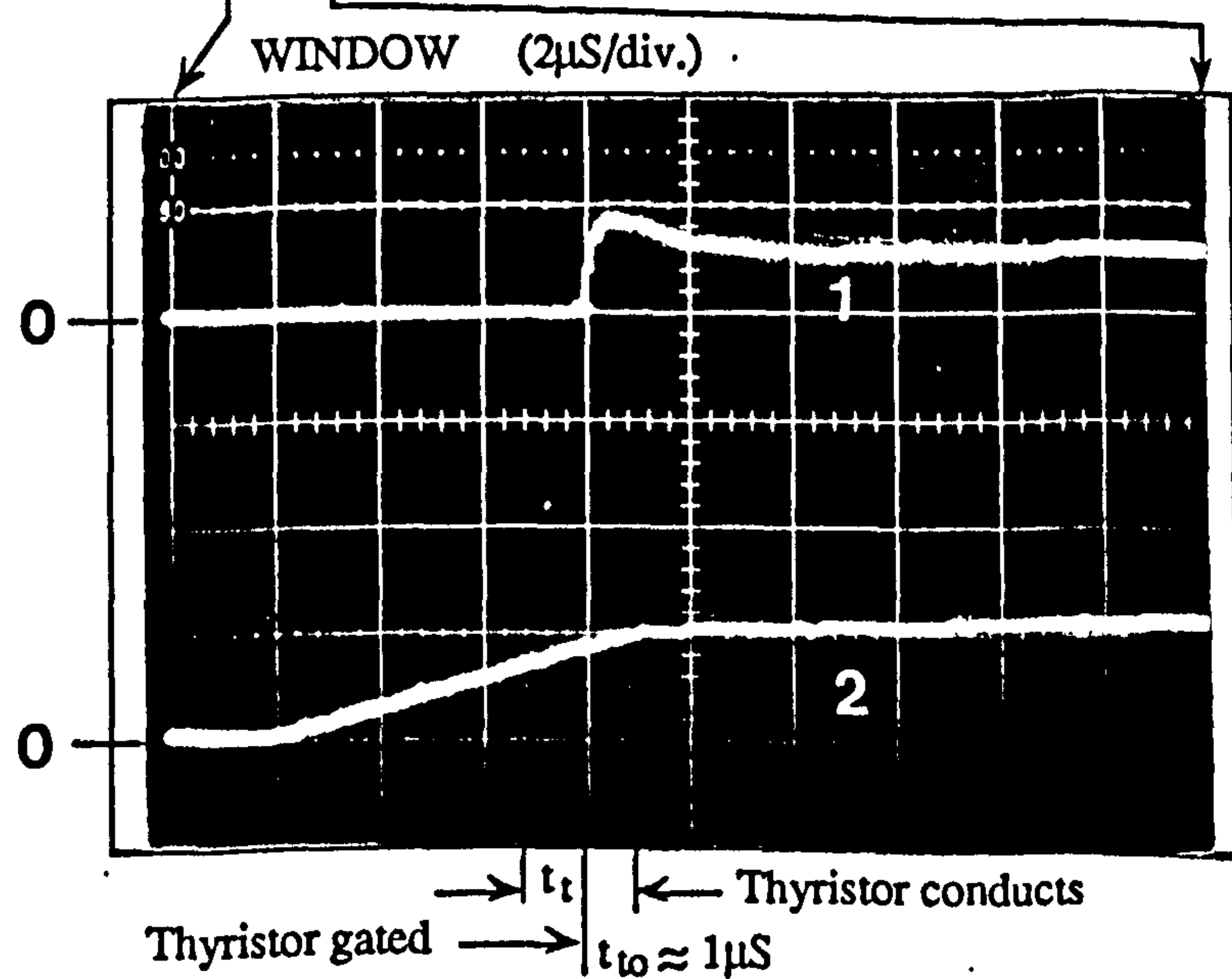
(2) GTO Anode Current (50A/div.)

(3) Crowbar Thyristor Current (200A/div.)

(4) Fuse (Supply) Current (200A/div.)

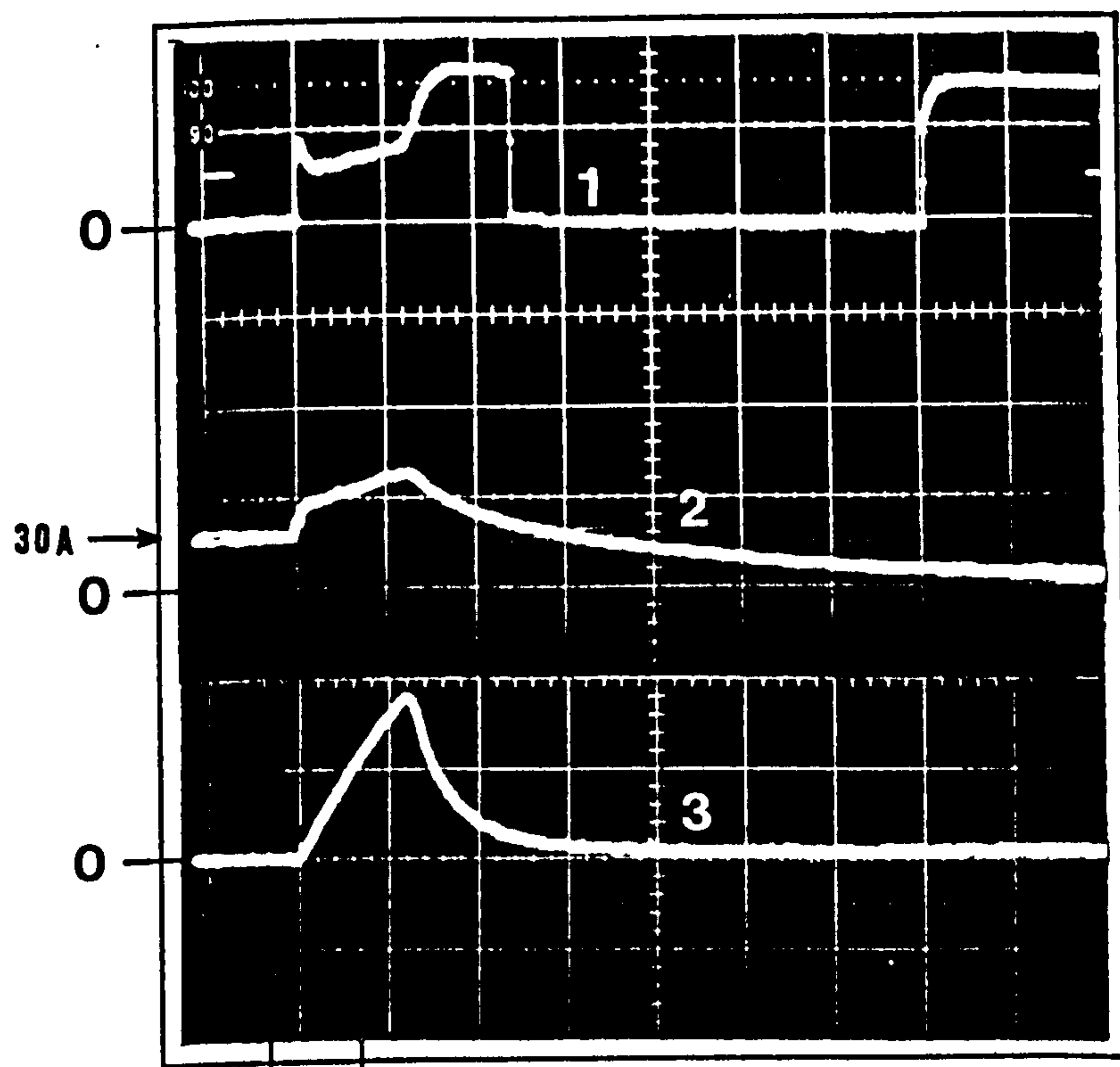
(5) Fuse Voltage (100V/div.)

Time Scale: 20μS/div.



(a) GTO turn-on into a short circuit

Figure 6.23 Over-current protection for the GTO thyristor by the crowbar and fuse

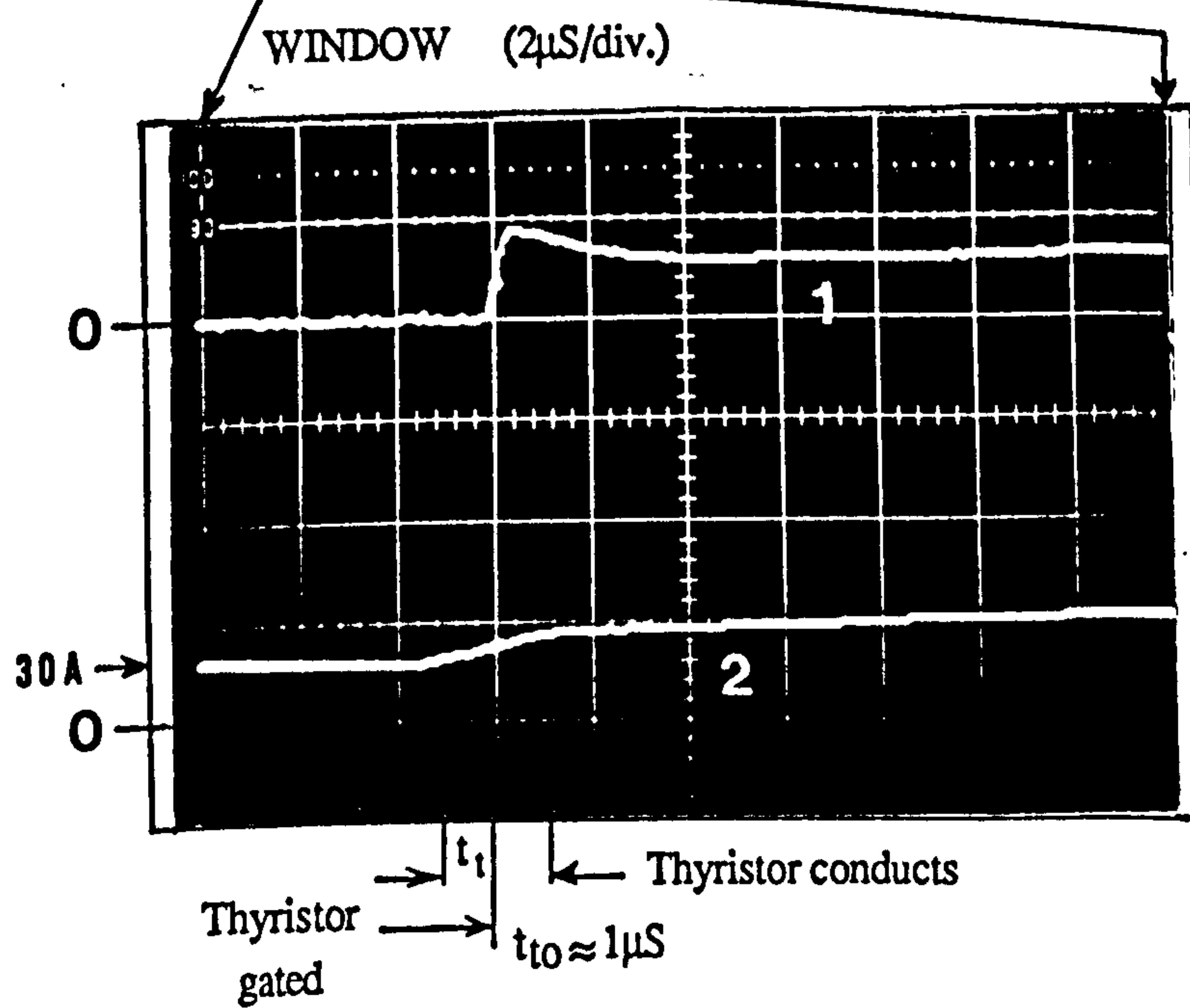


(1) Crowbar Thyristor Gate Current Pulse (0.5A/div.)

(2) GTO Anode Current (50A/div.)

(3) Crowbar Thyristor Current (200A/div.)

Time Scale: 20  $\mu$ S/div.



(b) Short circuit applied with the GTO conducting full load current

Figure 6.23 Over-current protection for the GTO thuristor by the crowbar and fuse .



## CHAPTER 7

### CONCLUSIONS

#### 7.1 Summary of Work Covered

*The work covered by this thesis is:*

- a ) An appraisal of the GTO thyristor as a power switching device compared with others;*
- b ) A description of the physical operation and working characteristics of the GTO thyristor, supported by experimental results;*
- c ) Consideration of the GTO gate drive requirements leading to the design and construction of a suitable gate drive circuitry;*
- d ) Consideration of over-voltage protection and snubbing, and the influence of circuit stray inductances in generating over-voltages across the GTO in DC chopper circuits;*
- e ) The work in (d) is extended to the H-bridge inverter with consideration being given to the various possible GTO switching patterns, with transients at GTO turn-on and off being defined;*
- f ) All circuit switching behaviour has been analysed by numerical techniques and the simple DC chopper also by the Laplace transform technique. The relevant waveforms have been computed and compared with experimental results obtained from specially designed and constructed laboratory circuits;*
- g ) Methods for GTO over-current protection have been considered and two methods of active protection developed to working systems, and results from them quoted.*

#### 7.2 Concluding Comments

*The investigation has shown that the GTO thyristor can be used as a reliable switching device at high powers as a better alternative to the conventional thyristor or power transistor providing it is operated within its defined limits. During experimentation,*

*some devices were lost from causes which can be explained, such as attempting to turn off excessive current, turn-off failure due to excessive  $dv/dt$  and control circuit interference from another laboratory user.*

*Despite such problems, the laboratory designs and experimentation were successful and so were the circuit analysis techniques. The Laplace method was found to be satisfactory for the simpler circuit configuration of the DC chopper, but became far too complex for use with the inverter. The Runge-Kutta numerical method proved most satisfactory for all circuits. However, prior knowledge of the GTO and diode terminal characteristics is necessary, especially at turn-off, and realistic values for the stray inductances are needed. Overall, the experimental results correlate very well with the computed ones.*

*The practical effects of switching time mismatch and diode reverse recovery were included, and valuable conclusions drawn regarding the resulting increased currents which some devices are then called upon to switch. This may lead to dangerous operating conditions if they are not anticipated.*

*The over-current protection requirements of the GTO and its gate drive are considered. Possible methods for the device protection are described, and active electronic approaches are satisfactorily utilised. The design and performance of a fast over-current detection circuit for use with these active methods is successful.*

*The important features regarding the effect of stray inductances and over-current protection are:*

- a ) All stray inductances contribute to the voltage overshoots across those GTOs which are switching and on this basis should be minimised. In practice, the value of the stray source inductance will normally be considerably greater than those within the power circuit. The importance of the strays has direct relevance to the circuit layout, although this cannot be considered in isolation. Other constraints apply; for example, available space and its shape, cooling measures, mechanical considerations of strength, shock and vibration withstand.*
- b ) The stray inductances within the branches of the bridge can usefully limit the shoot-through current  $di/dt$  at GTO turn-on when picking up current from the feedback/freewheeling diode, during its reverse recovery, above or below it as appropriate. These inductances can be enhanced by suitable device layout. If*



*inadequate for this, they are supplemented by an added wound inductor per branch having its own parallel freewheeling diode to avoid significantly worsening the overshoot problem.*

- c ) Switching a single GTO on or off results in a rise or fall in DC supply current and an induced EMF across the source inductance which depresses or lifts the bridge DC rail potential. This effectively results in cross-coupled switching transients from one device to others in the bridge which are in a quiescent blocking state within the bridge*
- d ) The effects of (c) can be serious with turn-on and turn-off mismatch between a diagonal pair of switching GTOs. With the former, the shoot-through and feedback diode reverse recovery conditions for the late turn-on device become more severe; with the latter, the late turn-off GTO must interrupt increased current. Allowances must be made in the device ratings.*
- e ) The importance of minimising especially the DC source inductance by using an input capacitor with low self-inductance is apparent. The techniques of positioning the capacitor close to the bridge, the use of short rectangular cross-section connectors, and paralleling capacitors to reduce the overall internal inductance should be used.*
- f ) Minimisation of the stray inductances counteracts their beneficial effects in limiting a rising current  $di/dt$ , under the short-circuit fault condition. As with (b), the addition of series inductor with a freewheeling diode may be needed.*
- g ) Conventional thyristors can be protected by fuse. GTOs can be turned off by gate turn-off signals generated after very fast detection of a rising fault current. A combination of crowbar and fuse is also adequate, although slower, and fuse replacement is necessary. The GTO self-protection method is much favoured due to its fast response and effectiveness.*

### **7.3 Suggestions for Further Work**

*During the course of the present research, several areas of interest have arisen for further work. These are:*

- a ) Incorporating a GTO thyristor model into the computer programmes:  
The computer modelling of the GTO by active and passive components may be assessed.*

*The two-transistor model of the device may prove to be a useful approach. This is then utilised in the programmes for the numerical analysis of the systems.*

***b ) A further stage in the development of the work:***

*To extend the investigation on the effects of the stray inductances during GTO switching to the 3-phase bridge inverter with relation to both quasi-square and PWM control. The principles, however, are covered in this thesis.*

***c ) Losses or regenerative snubber circuits:***

*The losses of the polarised RCD snubber network during GTO switching may be greatly reduced by employing non-dissipative snubber circuits. Here the trapped stored snubber energy is either returned to the DC supply or fed into the load. The disadvantage of such techniques is the increased component count, some of which may be active, increased complexity and reduced reliability.*



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## APPENDIX I

### Analysis of Chopper GTO Turn-Off with Resistive Load

*a) During overshoot time ( $t_{os}$ )*

*Using the Laplace operational circuit of Figure 3.4(b), shown in Figure I.1, where  $L$  (effective inductance) =  $(L_d + L_1 + L_s)$*

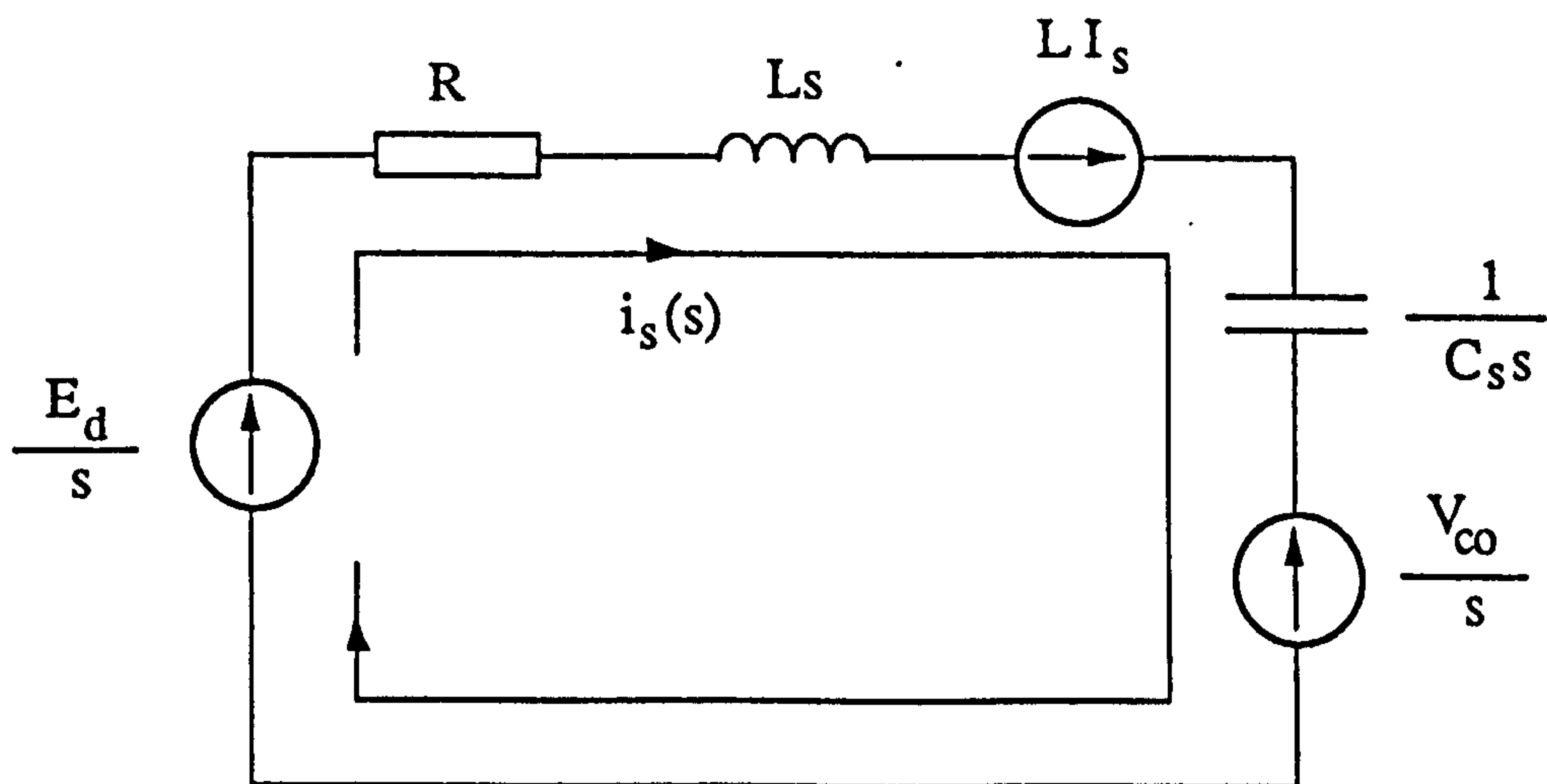


Figure I.1 Laplace operational circuit during the overshoot time  $t_{os}$

$$i_s(s) \left( sL + R + \frac{1}{C_s s} \right) = \frac{E_d - V_{co}}{s} + LI_s \quad (I.1)$$

*The inverse Laplace transform gives*

$$i_s = \frac{E_d - V_{co}}{\omega L} e^{-bt} \sin \omega t + I_s e^{-bt} \cos \omega t - I_o \frac{b}{\omega} e^{-bt} \sin \omega t \quad (I.2)$$

where  $i_s = i_s(t)$  (similar adaptation is used in all analysis)

$$b = \frac{R}{2L}, \quad \omega^2 = \frac{1}{LC} - b^2$$

This gives

$$i_s = e^{-bt} \left\{ I_s \cos \omega t + \left[ \frac{E_d - V_{co}}{\omega L} - I_s \frac{b}{\omega} \right] \sin \omega t \right\} \quad (1.3)$$

$$= \sqrt{I_s^2 + \left[ \frac{E_d - V_{co}}{\omega L} - I_s \frac{b}{\omega} \right]^2} e^{-bt} \cos (\omega t - \alpha) \quad (1.4)$$

Therefore

$$i_s = I_s \sqrt{1 + \tan^2 \alpha} e^{-bt} \cos (\omega t - \alpha) \quad (1.5)$$

where

$$\tan \alpha = \frac{E_d - V_{co}}{I_s \omega L} - \frac{b}{\omega}$$

The capacitor voltage is given by:

$$v_c = \frac{1}{C_s} \int i_s dt + K \text{ (constant of integration)}$$

Constant  $K$  is obtained by using the conditions  $v_c = V_{co}$  when  $t = 0$ , giving finally

$$v_c = I_s \sqrt{\frac{L(1 + \tan^2 \alpha)}{C_s}} [e^{-bt} \sin (\omega t - \alpha - \beta) + \sin (\alpha + \beta)] + V_{co} \quad (1.6)$$

where



$$\tan \beta = \frac{b}{\omega}$$

The peak capacitor voltage on overshoot is given when  $t = t_{os}$ . Therefore

$$V_{pk} = I_s \sqrt{\frac{L(1 + \tan^2 \alpha)}{C_s}} [e^{-bt_{os}} \sin(\omega t_{os} - \alpha - \beta) + \sin(\alpha + \beta)] + V_{co} \quad (1.7)$$

$V_{pk}$  occurs when  $i_s = 0$ , then

$$\cos(\omega t_{os} - \alpha) = 0, \text{ or } \omega t_{os} = \frac{\pi}{2} + \alpha$$

Alternatively, using energy consideration:

final stored energy = initial stored energy + energy supplied - energy lost

$$\frac{1}{2} C_s V_{pk}^2 = \left( \frac{1}{2} L I_s^2 + \frac{1}{2} C_s V_{co}^2 \right) + \frac{2}{\pi} E_d I_s t_{os} - \frac{1}{2} I_s^2 R t_{os} \quad (1.8)$$

using the assumption that  $\omega t_{os} = \pi/2$  or very nearly.

**b) During undershoot time ( $t_{us}$ )**

If it is assumed that the capacitor discharge through the source is overdamped due to  $R_s$ , and that  $\Delta V_1$  (Figure 3.3) is very small,  $I_{rp}$  and the stray inductance can be ignored.

From Figure 1.1 with added snubber resistance  $R_s$ ,  $V_{co}$  replaced by  $V_{pk}$  and the loop current reversed for capacitor discharge,

$$i_s(s) \left( R_T + \frac{1}{C_s s} \right) = \frac{V_{pk} - E_d}{s} \quad (1.9)$$

where  $R_T = R + R_s$ , and the inverse Laplace transform gives

$$i_s = \frac{(V_{pk} - E_d)}{R_T} e^{-\frac{t}{\tau}} \quad (1.10)$$

where  $\tau$  is the discharge time constant  $= R_T C_s$ .

The decaying capacitor voltage is

$$v_c = \frac{1}{C_s} \int i_s dt + K \text{ (constant of integration)}$$

giving, when  $v_c = V_{pk}$  at  $t = 0$ ,

$$v_c = (V_{pk} - E_d) e^{-\frac{t}{\tau}} + E_d \quad (1.11)$$

The GTO thyristor voltage is

$$v_{GTO} = v_c - i_s R_s \quad (1.12)$$

Then

$$v_{GTO} = \frac{R (V_{pk} - E_d)}{R_T} e^{-\frac{t}{\tau}} + E_d. \quad (1.13)$$

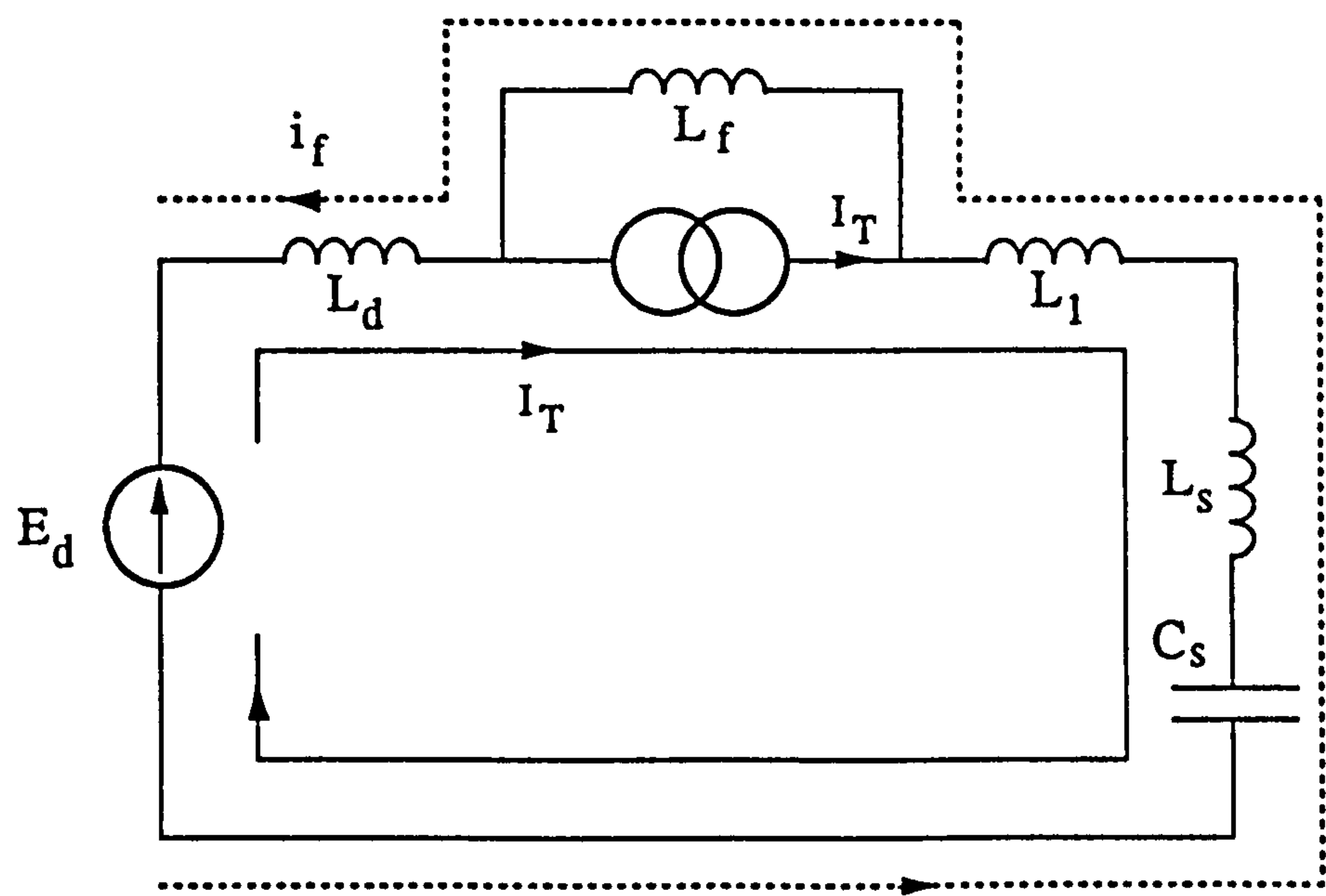


APPENDIX II

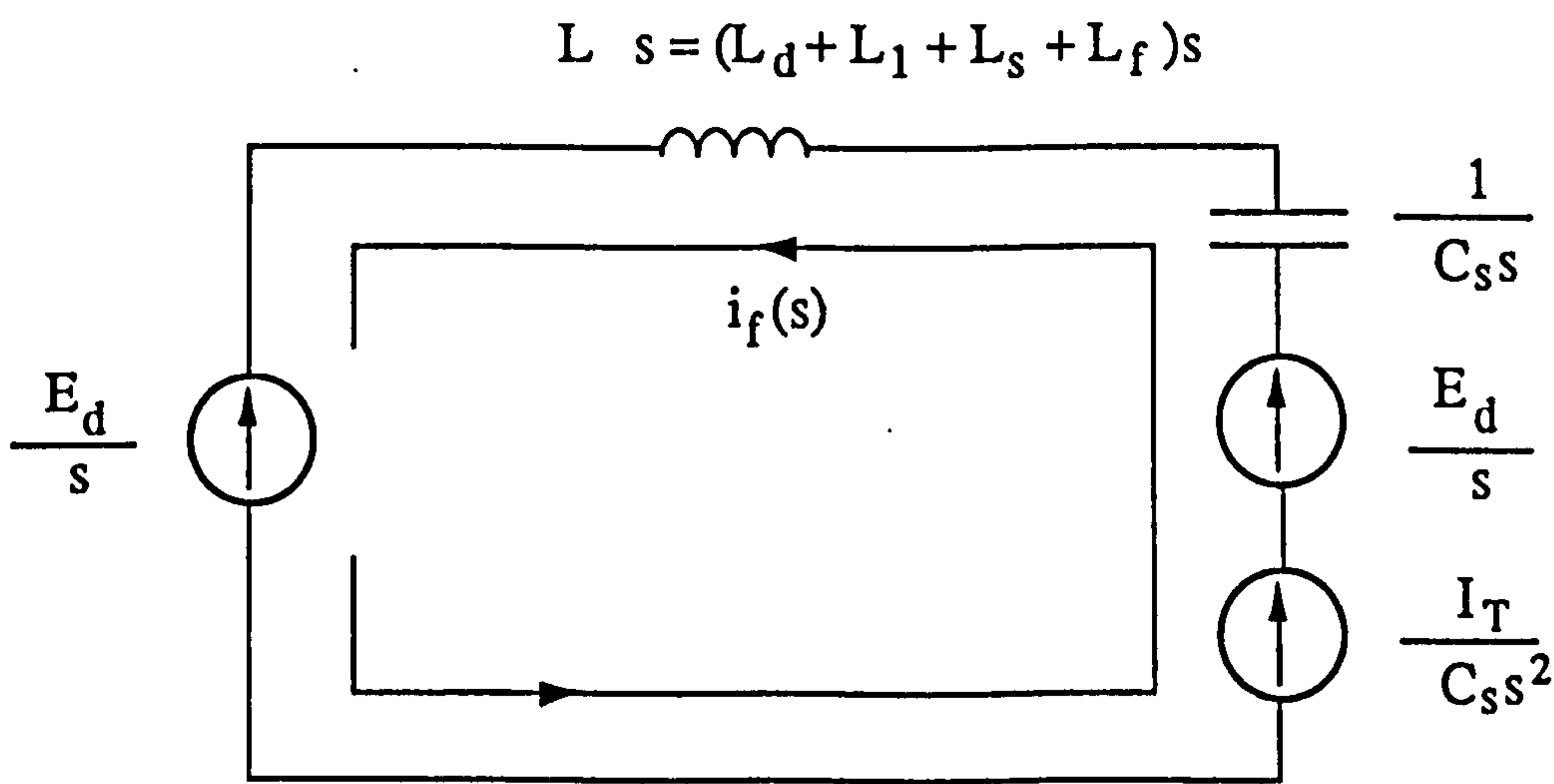
Analysis of Chopper GTO Turn-Off with Inductive Load

a) During the overshoot time ( $t_{os}$ )

The equivalent circuit of Figure 3.8(b) can be drawn alternatively, as in Figure II.1(a), and its Laplace operational circuit is given in Figure II.1(b).



(a)



(b)

Figure II.1 Equivalent circuits during the overshoot period at GTO turn-off in chopper with inductive load

Consider the circuits in Figure 11.1, and neglect any GTO decaying tail current. The load current (and initial snubber current) is  $I_T$  and the high load inductance maintains this constant during  $t_{os}$  as load current is diverted into the freewheeling diode, thereby acting as a current generator. The Laplace operational circuit represents this by the transform of a capacitor voltage rising linearly with time. Since  $I_T$  is constant, there is no  $(L_d + L_1 + L_s)$  term containing  $I_T$ . The adopted loop current  $i_f$  rises and cancels  $I_T$  in the GTO snubber, thereby diverting this current into the freewheeling path.

$$i_f(s) (Ls + \frac{1}{C_s s}) = \frac{E_d}{s} - \frac{E_d}{s} + \frac{I_T}{C_s s^2} \quad (11.1)$$

where the effective inductance  $L = L_d + L_1 + L_s + L_f$

$$i_f(s) = \frac{I_T}{LC_s} * \frac{1}{s(s^2 + \omega^2)} \quad (11.2)$$

and

$$\omega^2 = \frac{1}{LC_s}$$

Using partial fractions gives

$$i_f(s) = \frac{I_T}{\omega^2 LC_s} \left( \frac{1}{s} - \frac{s}{s^2 + \omega^2} \right) \quad (11.3)$$

The inverse Laplace transform gives

$$i_f = I_T(1 - \cos \omega t) \quad (11.4)$$



The forward charging current through  $C_s$  is

$$i_s = I_T - i_f \quad (11.5)$$

$$= I_T \cos \omega t \quad (11.6)$$

The overshoot time concludes when  $i_s = 0$  and the capacitor voltage reaches its peak.

Then

$$\omega t_{os} = \frac{\pi}{2}$$

and

$$t_{os} = \frac{\pi}{2\omega} \sqrt{LC_s}$$

The peak capacitor voltage is

$$\begin{aligned} V_{pk} &= \frac{1}{C_s} \int_0^{\frac{\pi}{2\omega}} i_s dt + E_d \\ &= I_T \sqrt{\frac{L}{C_s}} + E_d \end{aligned} \quad (11.7)$$

Alternatively, using energy consideration:

*final stored energy = initial stored energy + energy supplied - energy lost*

The total energy lost in the load during current transfer from  $(L_d + L_l + L_s)$  to  $L_f$  is best obtained using the voltage induced across  $L_f$  which is the same as that across the load  $(R + L_l)$ . The load current  $I_T$  is constant.

$$\text{Energy lost} = \int e i \, dt = I_T \int_0^{t_{os}} e \, dt = I_T \int_0^{I_T} L_f \, di = I_T^2 L_f \quad (11.8)$$

$$\text{Energy supplied} = \int_0^{t_{os}} E_d i \, dt = \frac{2}{\pi} E_d I_T t_{os} \quad (11.9)$$

*Therefore*

$$\frac{1}{2} C_s V_{pk}^2 + \frac{1}{2} L_f I_T^2 + \frac{1}{2} L I_T^2 = \left( \frac{1}{2} L_T I_T^2 + \frac{1}{2} C_s E_d^2 \right) + \frac{2}{\pi} E_d I_T t_{os} - I_T^2 L_f + \frac{1}{2} L I_T^2 \quad (11.10)$$

*where*  $L_T = L_d + L_f + L_3,$

*therefore*

$$\frac{1}{2} C_s V_{pk}^2 = \frac{1}{2} (L_T - 3L_f) I_T^2 + \frac{1}{2} C_s E_d^2 + \frac{2}{\pi} E_d I_T t_{os} \quad (11.11)$$



## APPENDIX III

### Analysis of H-Bridge GTOs Turn-On from Zero Initial Load Current

*As GTOs A1 and A2 switch on, the high load inductance causes the load current to rise slowly, reaching only a low value by the time B1 and B2 snubber capacitors are fully charged. Hence it is neglected for simplicity.*

*From Figure 4.1, let  $L_1 = L_s + L_{a1} + L_{b1}$  and*

$$L_2 = L_{d3} + L_s + L_{b2} + L_{a2} + L_{d4} .$$

*Using Laplace transform analysis, with the equivalent circuit shown in Figure III.1, (losses neglected).*

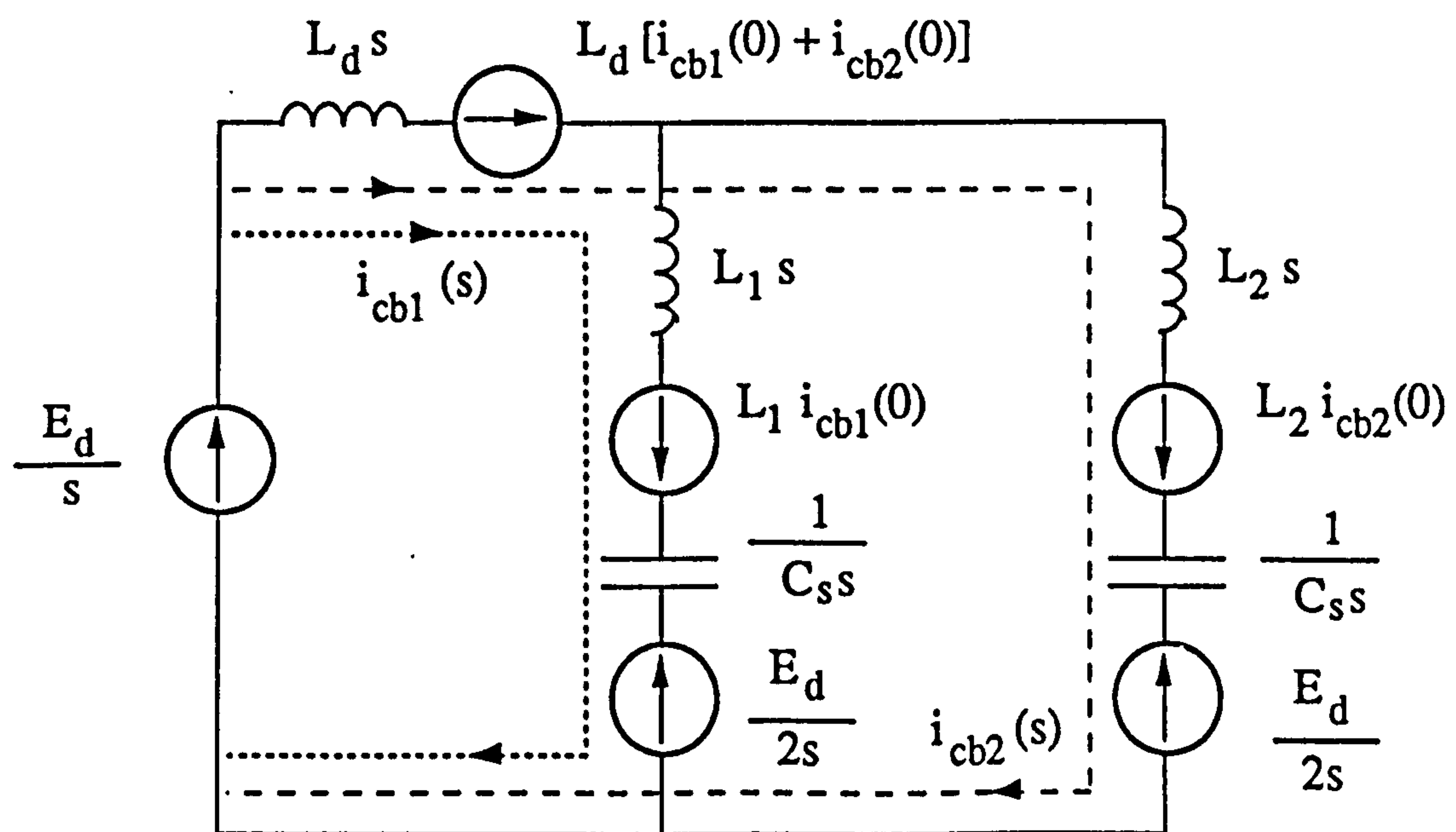


Figure III.1 Laplace equivalent circuit

*The loop currents  $i_{cb1}$  and  $i_{cb2}$  are rising. By Kirchhoff's voltage law; and  $i_{cb1}(0) = i_{cb2}(0) = 0$ .*

For  $i_{cb1}$  loop and using  $i_{cb1}$  and  $i_{cb2}$  instead of  $i_{cb1}(s)$  and  $i_{cb2}(s)$  respectively:

$$\frac{E_d}{s} = L_d s (\bar{i}_{cb1} + \bar{i}_{cb2}) + L_1 s \bar{i}_{cb1} + \frac{\bar{i}_{cb1}}{C_s s} \quad (III.1)$$

For  $i_{cb2}$  loop and using  $i_{cb1}$  and  $i_{cb2}$  instead of  $i_{cb1}(s)$  and  $i_{cb2}(s)$  respectively:

$$\frac{E_d}{s} = L_d s (\bar{i}_{cb1} + \bar{i}_{cb2}) + L_2 s \bar{i}_{cb2} + \frac{\bar{i}_{cb2}}{C_s s} \quad (III.2)$$

Subtract (III.1) from (III.2) therefore,

$$\bar{i}_{cb1} = \frac{(L_2 C_s s^2 + 1)}{(L_1 C_s s^2 + 1)} \bar{i}_{cb2} \quad (III.3)$$

Substitute (III.3) in (III.2) gives,

$$\frac{E_d}{2} = \frac{L_3^2 C_s \bar{i}_{cb2}}{(L_1 C_s s^2 + 1)} \left[ s^4 + \frac{L_4}{L_3^2 C_s} s^2 + \frac{1}{L_3^2 C_s^2} \right] \quad (III.4)$$

where

$$L_3^2 = L_1 L_d + L_2 L_d + L_1 L_2$$

and

$$L_4 = 2L_d + L_1 + L_2$$

Hence

$$\frac{E_d}{2} = \frac{L_3^2 C_s \bar{i}_{cb2}}{(L_1 C_s s^2 + 1)} [(s^2 + \omega_1^2)(s^2 + \omega_2^2)] \quad (III.5)$$



where

$$\omega_1^2 = \frac{L_4 - \sqrt{L_4^2 - 4L_3^2}}{2L_3^2 C_s}$$

and

$$\omega_2^2 = \frac{L_4 + \sqrt{L_4^2 - 4L_3^2}}{2L_3^2 C_s}$$

are the angular frequencies in rad/sec.

Rearrange (III.5) and by Partial Fractions:

$$\bar{i}_{cb2} = \frac{E_d}{2L_3^2 C_s} \left[ \frac{As + B}{(s^2 + \omega_1^2)} + \frac{Ds + E}{(s^2 + \omega_2^2)} \right] \quad (III.6)$$

where

$$A = -D = 0, B = \frac{L_1 C_s \omega_1^2 + 1}{(\omega_2^2 - \omega_1^2)} \text{ and } E = \frac{L_1 C_s \omega_2^2 - 1}{(\omega_2^2 - \omega_1^2)}$$

Thus

$$\bar{i}_{cb1} = \frac{E_d}{2\sqrt{L_4^2 - 4L_3^2}} \left[ \frac{(1 - \omega_1^2 L_1 C_s)}{\omega_1} * \frac{\omega_1}{(s^2 + \omega_1^2)} - \frac{(1 - \omega_2^2 L_1 C_s)}{\omega_2} * \frac{\omega_2}{(s^2 + \omega_2^2)} \right] \quad (III.7)$$

where

$$(\omega_2^2 - \omega_1^2) = \frac{\sqrt{L_4^2 - 4L_3^2}}{L_3^2 C_s}$$

The inverse transform gives

$$i_{cb2} = \frac{E_d}{2\sqrt{L_4^2 - 4L_3^2}} \left[ \frac{(1 - \omega_1^2 L_1 C_s)}{\omega_1} \sin \omega_1 t - \frac{(1 - \omega_2^2 L_1 C_s)}{\omega_2} \sin \omega_2 t \right] \quad (III.8)$$

similarly

$$i_{cb1} = \frac{E_d}{2\sqrt{L_4^2 - 4L_3^2}} \left[ \frac{(1 - \omega_1^2 L_2 C_s)}{\omega_1} \sin \omega_1 t - \frac{(1 - \omega_2^2 L_2 C_s)}{\omega_2} \sin \omega_2 t \right] \quad (III.9)$$

The voltage across B1 snubber capacitor is given by

$$v_{cb1} = \frac{1}{C_s} \int i_{cb1} dt + K (\text{constant})$$

$$v_{cb1} = \frac{E_d}{2C_s \sqrt{L_4^2 - 4L_3^2}} \left[ \frac{(\omega_1^2 L_2 C_s - 1)}{\omega_1^2} \cos \omega_1 t - \frac{(\omega_2^2 L_2 C_s - 1)}{\omega_2^2} \cos \omega_2 t \right] + K \quad (III.10)$$

When  $t = 0$ ,

$$v_{cb1} = \frac{E_d}{2}$$

giving

$$K = E_d$$

and

$$v_{cb1} = \frac{E_d}{2C_s \sqrt{L_4^2 - 4L_3^2}} \left[ \frac{(\omega_1^2 L_2 C_s - 1)}{\omega_1^2} \cos \omega_1 t - \frac{(\omega_2^2 L_2 C_s - 1)}{\omega_2^2} \cos \omega_2 t \right] + E_d \quad (III.11)$$

Similarly



$$v_{cb2} = \frac{E_d}{2C_s \sqrt{L_4^2 - 4L_3^2}} \left[ \frac{(\omega_1^2 L_1 C_s - 1)}{\omega_1^2} \cos \omega_1 t - \frac{(\omega_2^2 L_1 C_s - 1)}{\omega_2^2} \cos \omega_2 t \right] + E_d \quad (III.12)$$

$v_{cb1}$  (or  $v_{cb2}$ ) will approach its peak value as  $i_{cb1}$  (or  $i_{cb2}$ ) falls to zero, therefore from equations (III.8) and (III.9),

$$\frac{(1 - \omega_1^2 L_1 C_s)}{\omega_1} \sin \omega_1 t_{os1} - \frac{(1 - \omega_2^2 L_1 C_s)}{\omega_2} \sin \omega_2 t_{os1} = 0 \quad (III.13)$$

and

$$\frac{(1 - \omega_1^2 L_2 C_s)}{\omega_1} \sin \omega_1 t_{os2} - \frac{(1 - \omega_2^2 L_2 C_s)}{\omega_2} \sin \omega_2 t_{os2} = 0 \quad (III.14)$$

where  $t_{os1}$  = The overshoot (total oscillation) time for  $v_{cb1}$ .  
 $t_{os2}$  = The overshoot (total oscillation) time for  $v_{cb2}$ .

Equations (III.13) and (III.14) are solved for the overshoot times by Newton's iteration method, and by substituting these values in equations (III.11) and (III.12), for any values of  $L_1$ ,  $L_2$ ,  $C_s$ ,  $\omega_1$  and  $\omega_2$ , the peak  $V_{cb1}$  or  $V_{cb2}$  value will be limited to  $3/2E_d$ .

## APPENDIX IV

### Analysis of GTO Turn-Off Gain

*Referring to Figure 2.1, the GTO thyristor will turn-off when*

$$\alpha_{\text{pnp}} I_A + I_G < (1 - \alpha_{\text{nnp}}) I_G \quad (\text{IV.1})$$

*where*

$$I_G = I_K - I_A \quad (\text{IV.2})$$

*Substitute IV.2 in IV.1 and rearrange, results*

$$\alpha_{\text{pnp}} I_A - I_A < -\alpha_{\text{nnp}} I_K \quad (\text{IV.3})$$

*Adding  $(\alpha_{\text{nnp}} I_A)$  to both sides, therefore*

$$-I_G > \frac{I_A (\alpha_{\text{nnp}} + \alpha_{\text{pnp}} - 1)}{(\alpha_{\text{nnp}})} \quad (\text{IV.4})$$

*Equation IV.4 provides the condition for the minimum negative gate current required to turn-off the GTO thyristor, hence the turn-off gain;*

$$\frac{I_T}{I_G} = \frac{\alpha_{\text{nnp}}}{(\alpha_{\text{nnp}} + \alpha_{\text{pnp}} - 1)} \quad (\text{IV.5})$$



## APPENDIX V

### Current and Voltage Ratings of the Snubber Diode (Ds)

#### a) RMS current rating

Referring to Figure 2.10, the decaying snubber current  $I_s$  may be considered to have the rough shape of first quarter of a cosine wave. Hence

$$I_{DRMS} = \sqrt{\frac{1}{T} \int_0^{\pi/2\omega} I_s^2 \cos^2 \omega t \, dt} \quad (V.1)$$

where  $I_{DRMS}^D =$  snubber diode RMS current

$I_s =$  peak snubber current (approximately  $0.9 I_T$ )

$T =$  period of operation

$\omega =$  frequency of oscillation  $= (1/LC_s)^{1/2}$

$C_s =$  snubber capacitance

$L =$  path stray inductance

Since  $\cos^2 \omega t = 1/2 (1 + \cos 2\omega t)$ ; therefore

$$I_{DRMS} = \frac{I_s}{2} \sqrt{\frac{\pi}{\omega T}} \quad (V.2)$$

#### b) Voltage rating

Referring to Figure 2.15, with Figure V.1 shows the Laplace operational circuit during the snubber reverse recovery time  $t_{rr}$  (neglecting losses), where  $L$  is the effective path stray inductance and  $C_s$  is the snubber capacitance

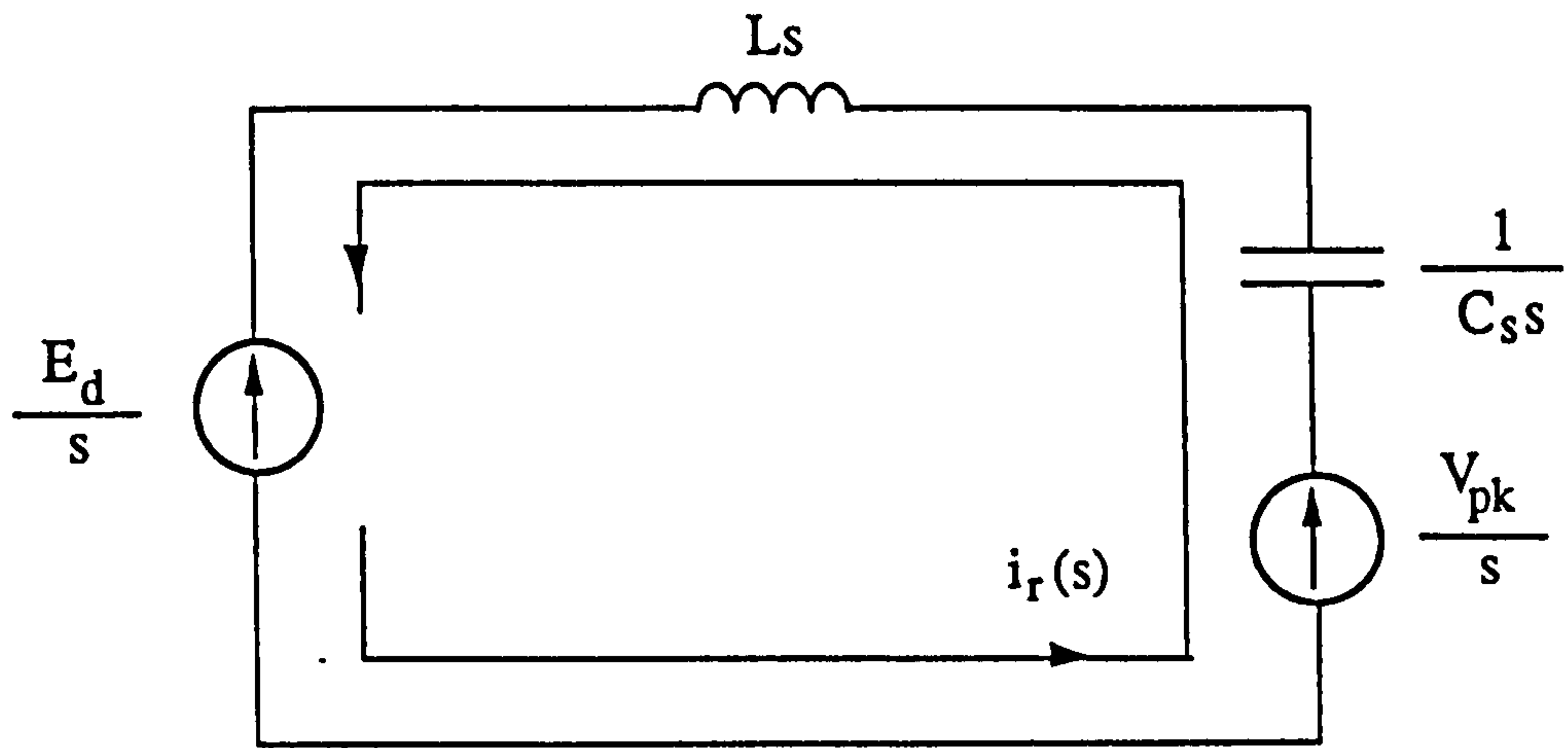


Figure V.1 Laplace operational circuit during snubber diode reverse recovery time  $t_{rr}$

$$i_r(s) * \left( Ls + \frac{1}{C_s s} \right) = (V_{pk} - E_d) \quad (V.3)$$

*The inverse Laplace transform gives*

$$i_r = (V_{pk} - E_d) * \sqrt{\frac{C_s}{L}} \sin \omega t \quad (V.4)$$

*The peak reverse recovery current  $I_{rp}$  is when  $t = t_{rr}$ ; therefore*

$$i_{rp} = (V_{pk} - E_d) * \sqrt{\frac{C_s}{L}} \sin \omega t_{rr} \quad (V.5)$$

*The capacitor voltage fall  $\Delta V_1$  (Figure 2.14) during  $t_{rr}$  is given by*

$$\Delta V_1 = \frac{1}{C_s} \int_0^{t_{rr}} i_r dt \quad (V.6)$$



*giving*

$$\Delta V_1 = (V_{pk} - E_d) (1 - \cos \omega t_{rr}) \quad (V.7)$$

## APPENDIX VI

### List of Components

#### *a ) For Figure 2.18*

*IC1 = 4047B*

*IC2, IC3 = 74LS123*

*R1 = 3.3K*

*R2 = 1K*

*R3 = 10K*

*R4 = 1.5K*

*R5 = 100K*

*Pt1, Pt3 = 47K*

*Pt2 = 5K*

*Pt4 = 10K*

*C0 = 0.1 $\mu$ F*

*C1 = 0.22 $\mu$ F*

*C2 = 0.01 $\mu$ F*

*C3 = 0.47 $\mu$ F*

*C4 = 0.047 $\mu$ F*

*C5 = 0.68 $\mu$ F*

#### *b ) For Figure 2.20*

*IC1, IC2 = 6N136*

*TR1, TR2, TR3, TR14 = ZTX451*

*TR4, TR5, TR6, TR7, TR15, TR16, TR17, TR18 = ZTX314*

*TR8, TR9, TR19, TR20 = ZTX551*

*TR10 = IRF530*

*TR11, TR12, TR13 = IRF141*

*D1, D2, D3, D4, D5, D6, D7, D8 = IN914*

*D9 = BYV28-50*

*D10 = BYW30-50*

*ZD1, ZD2 = 5.6V*

*ZD3, ZD7 = 7.5V*

*ZD4 = 12V*

*ZD5, ZD6 = 10V*

*R<sub>1</sub>, R<sub>23</sub> = 1.5K*

*R<sub>2</sub>, R<sub>3</sub>, R<sub>24</sub>, R<sub>25</sub> = 330 $\Omega$*

*R<sub>4</sub>, R<sub>5</sub>, R<sub>26</sub>, R<sub>27</sub> = 220 $\Omega$*

*R<sub>6</sub>, R<sub>9</sub>, R<sub>10</sub>, R<sub>18</sub>, R<sub>19</sub>, R<sub>28</sub>, R<sub>33</sub>, R<sub>34</sub>, R<sub>38</sub>, R<sub>39</sub> = 1K*

*R<sub>7</sub>, R<sub>15</sub>, R<sub>29</sub>, R<sub>30</sub> = 4.7K*



$R_8, R_{12}, R_{16}, R_{20}, R_{31}, R_{35}, R_{36}, R_{40} = 1.2K$

$R_{13}, R_{14}, R_{21}, R_{41} = 100\Omega$

$R_{11}, R_{17}, R_{32}, R_{37} = 10K$

$R_G = 0.5\Omega$

$Pt1, Pt2, Pt3, Pt4 = 4.7K$

$C_0, C_5 = 0.1\mu F$

$C_1, C_2, C_3, C_4 = 100\mu F$

**c) For Figure 4.4**

$IC1 = 4047B$

$IC2, IC3, IC4, IC5, IC6, IC7, IC8, IC9 = 74LS123$

$XR1, XR2 = 4070B$

$R0 = 3.3K$

$R1 = 1K$

$R2 = 5.6K$

$Pt0 = 10k$

$Pt1 = 5k$

$Pt2 = 47k$

$Pt3 = 100k$

$C0 = 0.1\mu F$

$C1 = 0.01\mu F$

$C2 = 0.47\mu F$

$C3 = 0.047\mu F$

**d) For Figure 6.13**

$IC1, IC2, IC4, IC5 = LF354$

$IC3 = 74LS123$

$TR1, TR3, TR6 = ZTX451$

$TR2 = ZTX551$

$TR4, TR5, TR7, TR8 = ZTX314$

$D1, D2, D3 = IN914$

$ZD1, ZD6 = 10V$

$ZD2 = 3.6V$

$ZD3, ZD4, ZD5 = 5.6V$

$R_1 = 1.5K$

$R_2, R_{21} = 680\Omega$

$R_3, R_4, R_7, R_{10}, R_{14}, R_{15}, R_{17}, R_{19}, R_{23}, R_{24}, R_{25}, R_{29}, R_{30} = 10K$

$R_5, R_6, R_9, R_{13}, R_{20} = 2.2K$

$$R_8 = 4.7K$$

$$R_{11}, R_{12}, R_{16}, R_{27}, R_{28} = 1K$$

$$R_{f1}, R_{f3} = 10K$$

$$R_{f4} = 470K$$

$$R_{01}, R_{02}, R_{03} = 100\Omega$$

$$R_{04} = 1K$$

$$Pt1, Pt2, Pt5, Pt7, Pt8 = 4.7K$$

$$Pt3 = 47K$$

$$Pt4 = 100K$$

$$Pt6 = 1K$$

$$C_B = 13.6\mu F$$

$$C_0, C_8 = 0.1\mu F$$

$$C_1, C_2, C_3, C_4 = 100\mu F$$

$$C_5, C_6 = 1nF$$

$$C_7 = 0.01\mu F$$

$$C_{f1}, C_{f2}, C_{f3}, C_{f4} = 10pF$$

**e) For Figure 6.14**

$$IC1, IC5 = 4047B$$

$$IC2, IC3, IC4 = 74LS123$$

$$TR1, TR2 = ZTX314$$

$$LED = T/L220$$

$$OR = SN7432N$$

$$REL = RSL6$$

$$R_1, R_{13} = 3.3K$$

$$R_2, R_7, R_8, R_9 = 1K$$

$$R_3 = 10K$$

$$R_4 = 1.5K$$

$$R_5, R_6 = 100K$$

$$R_{10} = 560\Omega$$

$$R_{11} = 150\Omega$$

$$R_{12} = 4.7K$$

$$Pt1, Pt3 = 47K$$

$$Pt2 = 5K$$

$$Pt4, Pt7, Ptc = 10K$$

$$C_0, C_c = 0.1\mu F$$

$$C_1 = 0.22\mu F$$

$$C_2, C_6, C_7 = 0.01\mu F$$



$C_3 = 0.47\mu F$   
 $C_4 = 0.047\mu F$   
 $C_5 = 0.68\mu F$

**f ) For Figure 6.17**

$IC1 = 6N137$

$TR1 = ZTX451$   
 $TR2, TR3 = ZTX314$   
 $TR4 = IRF520$

$D1 = IN4005$

$ZD1 = 6.2V$   
 $ZD2 = 10V$   
 $ZD3 = 20V$

$R_0 = 150\Omega$   
 $R_1, R_2 = 430\Omega$   
 $R_4 = 4.7K$   
 $R_5 = 10K$   
 $R_6, R_8, R_9 = 100\Omega$   
 $R_7 = 0.5\Omega$

$Pt1 = 1K$   
 $Pt2 = 10K$   
 $Pt3 = 100\Omega$

$C_0, C_3 = 0.1\mu F$   
 $C_1 = 100\mu F$   
 $C_2 = 100pF$

## APPENDIX VII

### Definition of Stray Inductances

*a) For Figure 4.10 (b), (d) and (f)*

$$\begin{aligned}
 L_1 &= -L_T(L_T L_d^2 - L_T L_{T3} L_{T4} - 2 L_d L_{T1} L_{T2} + L_{T2}^2 L_{T4} + L_{T1}^2 L_{T3}) \\
 L_2 &= -L_T(L_T L_d - L_T L_{T3} - L_d L_{T2} + L_{T1} L_{T3} + L_{T2}^2 - L_{T1} L_{T2}) \\
 L_3 &= -L_T(L_d L_{T2} - L_{T1} L_{T3}) \\
 L_4 &= L_T(L_T L_{T3} - L_{T2}^2) \\
 L_5 &= -L_T(L_T L_d - L_{T1} L_{T2}) \\
 L_6 &= -L_T(L_T L_d - L_T L_{T4} - L_d L_{T1} + L_{T2} L_{T4} - L_{T1} L_{T2} + L_{T1}^2) \\
 L_7 &= -L_T(L_d L_{T1} - L_{T2} L_{T4}) \\
 L_8 &= -L_T(L_T L_d - L_{T1} L_{T2}) \\
 L_9 &= -L_T(L_T L_4 - L_{T1}^2) \\
 L_{10} &= -L_T^2(L_T L_d^2 - L_T L_{T3} L_{T4} - 2 L_d L_{T1} L_{T2} + L_{T2}^2 L_{T4} + L_{T1}^2 L_{T3}) \\
 L_{11} &= -L_T^2(L_d^2 - L_d L_{T2} - L_d L_{T1} + L_{T3} L_{T4} - L_{T2} L_{T4} + L_{T1} L_{T3}) \\
 L_{12} &= -L_T^2(L_d^2 - L_{T3} L_{T4}) \\
 L_{13} &= -L_T^2(L_d L_{T2} - L_{T1} L_{T3}) \\
 L_{14} &= -L_T^2(L_d L_{T1} - L_{T2} L_{T4})
 \end{aligned}$$

Where:

$$\begin{aligned}
 L_T &= L_d + L_{a1} + L_1 + L_{a2} + L_{d4} \\
 L_{T1} &= L_d + L_{a1} \\
 L_{T2} &= L_d + L_{a2} + L_{d4} \\
 L_{T3} &= L_d + L_{d3} + L_s + L_{b2} + L_{a2} + L_{d4} \\
 L_{T4} &= L_d + L_{a1} + L_s + L_{b1}
 \end{aligned}$$

*b) For Figure 4.12 (b), (d), (f) and (h)*

$$\begin{aligned}
 L_1 &= L_d L_{L1} - L_d L_{L3} - L_{T1} L_{L1} + L_{T1} L_{L3} \\
 L_2 &= L_L L_{L3} - L_{L1} L_{L2} \\
 L_3 &= -(L_d L_{L3} - L_{T3} L_{L1}) \\
 L_4 &= L_{T1} L_{L3} - L_{T3} L_{L1} \\
 L_5 &= -L_{L3} (L_d - L_{T1}) \\
 L_6 &= -L_{L1} (L_d - L_{T1}) \\
 L_7 &= -(L_d L_{L2} - L_{T1} L_{L2} - L_d L_L + L_{T1} L_L) \\
 L_8 &= -(L_d L_{L2} - L_{T3} L_L) \\
 L_9 &= -L_{L2} (L_d - L_{T1}) \\
 L_{10} &= -L_L (L_d - L_{T1}) \\
 L_{11} &= L_{T1} L_{L2} - L_{T3} L_L \\
 L_{12} &= -(L_d L_L L_{L3} - L_{T1} L_L L_{L3} - L_d L_{L1} L_{L2} + L_{T1} L_{L1} L_{L2})
 \end{aligned}$$



$$\begin{aligned}
L_{13} &= -(L_d \cdot L_{T2} \cdot L_{L3} - L_{T1} \cdot L_L \cdot L_{L3} + L_d \cdot L_{T4} \cdot L_{L2} - L_{T1} \cdot L_{T4} \cdot L_{L2} - L_d \cdot L_{T2} \cdot L_{L1} + L_{T1} \\
&\quad \cdot L_{T2} \cdot L_{L1} - L_d \cdot L_{T4} \cdot L_L + L_{T1} \cdot L_{T4} \cdot L_L) \\
L_{14} &= -(L_L \cdot L_{L3} + L_d \cdot L_{T2} \cdot L_{L3} - L_{L1} \cdot L_{L2} + L_d \cdot L_{T4} \cdot L_{L2} - L_{T2} \cdot L_{T3} \cdot L_{L1} - L_{T3} \cdot L_{T4} \cdot L_L) \\
L_{15} &= -(L_d \cdot L_{T2} \cdot L_{L3} - L_{T1} \cdot L_{T2} \cdot L_{L3} + L_d \cdot L_{T4} \cdot L_{L2} - L_{T1} \cdot L_{T4} \cdot L_{L2}) \\
L_{16} &= -(L_d \cdot L_{T2} \cdot L_{L1} - L_{T1} \cdot L_{T2} \cdot L_{L1} + L_d \cdot L_{T4} \cdot L_L - L_{T1} \cdot L_{T4} \cdot L_L) \\
L_{17} &= L_L \cdot L_{L3} + L_{T1} \cdot L_{T2} \cdot L_{L3} - L_{L1} \cdot L_{L2} + L_{T1} \cdot L_{T4} \cdot L_{L2} - L_{T2} \cdot L_{T3} \cdot L_{L1} - L_{T3} \cdot L_{T4} \cdot L_L \\
L_{18} &= L_{LL3} \cdot L_{LL} - L_{LL2} \cdot L_{LL1} \\
L_{19} &= L_{LT} \cdot (L_{LL3} - L_{LL1}) \\
L_{20} &= L_{LT3} \cdot L_{LL1} - L_{LL3} \cdot L_{LT1} \\
L_{21} &= L_{LL1} \cdot L_{LT} \\
L_{22} &= L_{LL3} \cdot L_{LT} \\
L_{23} &= L_{LT4} \cdot L_{LL1} - L_{LL3} \cdot L_{LT2} \\
L_{24} &= -L_{LT} \cdot (L_{LL2} - L_{LL1}) \\
L_{25} &= -(L_{LT3} \cdot L_{LL} - L_{LL2} \cdot L_{LT1}) \\
L_{26} &= L_{LL} \cdot L_{LT} \\
L_{27} &= L_{LT2} \cdot L_{LT} \\
L_{28} &= -(L_{LT4} \cdot L_{LL} - L_{LL2} \cdot L_{LT2}) \\
L_{29} &= L_{LL3} \cdot L_{LL} \cdot L_s - L_{LL3} \cdot L_{LT} \cdot L_{L4} - L_{LL2} \cdot L_{LL1} \cdot L_s + L_{LL2} \cdot L_{LT} \cdot L_{L5} + L_{LL1} \cdot L_{LT} \cdot L_{L4} \\
&\quad - L_{LL} \cdot L_{LT} \cdot L_{L5} \\
L_{30} &= L_{LT3} \cdot L_{LL1} \cdot L_{L4} - L_{LT3} \cdot L_{LL} \cdot L_{L5} - L_{LL3} \cdot L_{LT1} \cdot L_{L4} + L_{LL2} \cdot L_{LT1} \cdot L_{L5} \\
L_{31} &= L_{LT} \cdot (L_{LL1} \cdot L_{L4} - L_{LL} \cdot L_{L5}) \\
L_{32} &= L_{LL3} \cdot L_{LL} \cdot L_s - L_{LL3} \cdot L_{LT} \cdot L_{L4} - L_{LL2} \cdot L_{LL1} \cdot L_s + L_{LL2} \cdot L_{LT} \cdot L_{L5} \\
L_{33} &= L_{LT4} \cdot L_{LL1} \cdot L_{L4} - L_{LT4} \cdot L_{LL} \cdot L_{L5} - L_{LL3} \cdot L_{LT2} \cdot L_{L4} - L_{LL3} \cdot L_{LL} \cdot L_d + L_{LL3} \cdot L_{LL} \cdot L_{T1} \\
&\quad + L_{LL2} \cdot L_{LT2} \cdot L_{L5} + L_{LL2} \cdot L_{LL1} \cdot L_d - L_{LL2} \cdot L_{LL1} \cdot L_{T1} \\
L_{34} &= L_{L6} \cdot (L_{LL3} \cdot L_{LL} - L_{LL2} \cdot L_{LL1}) \\
L_{35} &= L_{L6} \cdot L_s \cdot (L_{LL3} \cdot L_{LL} - L_{LL2} \cdot L_{LL1}) \\
L_{36} &= -L_{D3} \cdot (L_{LL3} \cdot L_{LL} \cdot L_s - L_{LL3} \cdot L_{LT} \cdot L_{L4} - L_{LL2} \cdot L_{LL1} \cdot L_s + L_{LL2} \cdot L_{LT} \cdot L_{L5} + L_{LL1} \cdot L_{LT} \\
&\quad \cdot L_{L4} - L_{LL} \cdot L_{LT} \cdot L_{L5}) \\
L_{37} &= L_{D3} \cdot (L_{LT3} \cdot L_{LL} \cdot L_{L5} + L_{LL3} \cdot L_{LT1} \cdot L_{L4} - L_{LL2} \cdot L_{LT1} \cdot L_L + L_{LT3} \cdot L_{LL1} \cdot L_{L4}) \\
L_{38} &= -L_{LT} \cdot L_{D3} \cdot (L_{LL1} \cdot L_{L4} - L_{LL} \cdot L_{L5}) \\
L_{39} &= -L_{D3} \cdot (L_{LL3} \cdot L_{LL} \cdot L_s - L_{LL3} \cdot L_{LT} \cdot L_{L4} - L_{LL2} \cdot L_{LL1} \cdot L_s + L_{LL2} \cdot L_{LT} \cdot L_{L5}) \\
L_{40} &= L_{LT4} \cdot L_{LL} \cdot L_{L5} \cdot L_{D3} + L_{LL3} \cdot L_{LT2} \cdot L_{L4} \cdot L_{D3} - L_{LT4} \cdot L_{LL1} \cdot L_{L4} \cdot L_{D3} - L_{LL3} \cdot L_{LL} \cdot L_{L6} \\
&\quad + L_{LL3} \cdot L_{LL} \cdot L_{D3} \cdot L_d - L_{LL3} \cdot L_{LL} \cdot L_{D3} \cdot L_{T1} + L_{LL2} \cdot L_{LL1} \cdot L_{L6} - L_{LL2} \cdot L_{LT2} \cdot L_{L5} \cdot L_{D3} \\
&\quad - L_{LL2} \cdot L_{LL1} \cdot L_{D3} \cdot L_d + L_{LL2} \cdot L_{LL1} \cdot L_{D3} \cdot L_{T1}
\end{aligned}$$

Where:

$$\begin{aligned}
L_T &= L_d + L_{a1} + L_1 + L_s + L_{a2} + L_{d4} \\
L_{T1} &= L_d + L_{a1} \\
L_{T2} &= L_1 + L_{a1} \\
L_{T3} &= L_d + L_{a1} + L_s + L_{b1} \\
L_{T4} &= L_{d3} + L_s + L_{b2} + L_1 + L_{a1} \\
L_{T5} &= (L_{d3} + L_{b2} + L_1 + L_{a1}) \\
L_{T6} &= (L_{d3} + L_{D3} + L_{b2} + L_1 + L_{a1}) \\
L_L &= -L_1 \cdot L_d + L_{a1} \cdot (L_{d4} + L_{a2} + L_s)
\end{aligned}$$

$$\begin{aligned}
L_{L1} &= (L_d + L_{a1}) \cdot (L_{b2} + L_{d3} + L_s) + L_d \cdot (L_1 + L_{a1}) \\
L_{L2} &= -L_1 \cdot (L_d + L_{a1}) - (L_1 + L_{a1}) \cdot (L_{b1} + L_s) \\
L_{L3} &= (L_{b2} + L_{d3}) \cdot (L_d + L_s + L_{a1} + L_{b1}) + (L_{b1} + L_s) \cdot (L_1 + L_s) + L_s \cdot (L_d + 2 \cdot L_{a1}) \\
&\quad + L_1 \cdot (L_d + L_{a1}) + L_{a1} \cdot (L_{b1} + L_d) \\
L_{L4} &= L_s \cdot (L_d + L_{a1}) \\
L_{L5} &= L_s \cdot (L_d + L_{b1} + L_s + L_{a1}) \\
L_{L6} &= -L_{a1} \cdot (L_s + L_{d3}) \\
L_{L7} &= L_s \cdot (L_{d4} + L_{a2} + L_s + L_1 + L_{a1} + L_d) \\
L_{L8} &= -(L_s \cdot L_{a1} + L_s \cdot L_1 + L_{d3} \cdot L_{a1} + L_{d3} \cdot L_1) \\
L_{L9} &= L_s \cdot (L_1 + L_{a1}) \\
L_{L10} &= L_s \cdot L_{a1} \\
L_{L11} &= L_{d3} \cdot L_s + (L_{d3} + L_s) \cdot (L_1 + L_{d3} + L_{b2} + L_{a1}) \\
L_{LT} &= L_s \cdot L_{L11} \\
L_{LT1} &= L_s \cdot L_{L6} \\
L_{LT2} &= L_{a1} \cdot L_{L11} + L_{T5} \cdot L_{L6} \\
L_{LT3} &= L_s \cdot (L_{L11} + L_{L8}) \\
L_{LT4} &= L_{L11} \cdot L_{T2} + L_{L8} \cdot L_{T5} \\
L_{LL} &= L_{L11} \cdot L_{L4} + L_{L9} \cdot L_{L6} \\
L_{LL1} &= L_{L11} \cdot L_{L5} + L_{L10} \cdot L_{L6} \\
L_{LL2} &= L_{L11} \cdot L_{L7} + L_{L9} \cdot L_{L8} \\
L_{LL3} &= L_{L11} \cdot L_{L4} + L_{L10} \cdot L_{L8}
\end{aligned}$$

c) For Figure 4.14 (b), (d), (f), (h), (j) and (l)

$$\begin{aligned}
L_1 &= L_{L2} \cdot L_L - L_{L1}^2 \\
L_2 &= L_{L1} \cdot L_{T1} + L_L \cdot L_{T2} \\
L_3 &= L_{T6} \cdot L_L + L_{T5} \cdot L_{L1} \\
L_4 &= L_T \cdot L_{L1} \\
L_5 &= L_T \cdot L_L \\
L_6 &= L_{T6} \cdot L_L - L_{L1} \cdot L_{T1} \\
L_7 &= L_{L2} \cdot L_{T1} + L_{L1} \cdot L_{T2} \\
L_8 &= L_{T6} \cdot L_{L1} + L_{L2} \cdot L_{T5} \\
L_9 &= L_T \cdot L_{L2} \\
L_{10} &= L_T \cdot L_{L1} \\
L_{11} &= L_{T6} \cdot L_{L1} - L_{L2} \cdot L_{T1} \\
L_{12} &= L_T \cdot (L_{L2} \cdot L_L - L_{L1}^2) \\
L_{13} &= L_{L2} \cdot L_L + L_{L2} \cdot L_{T1}^2 - L_{L1}^2 + 2 \cdot L_{L1} \cdot L_{T2} \cdot L_{T1} + L_L \cdot L_{T2}^2 \\
L_{14} &= L_{T6} \cdot L_{L1} \cdot L_{T1} + L_{T6} \cdot L_L \cdot L_{T2} + L_{L2} \cdot L_{T5} \cdot L_{T1} - L_{L2} \cdot L_L + L_{T5} \cdot L_{L1} \cdot L_{T2} + L_{L1}^2 \\
L_{15} &= L_T \cdot (L_{L2} \cdot L_{T1} + L_{L1} \cdot L_{T2}) \\
L_{16} &= L_T \cdot (L_{L1} \cdot L_{T1} + L_L \cdot L_{T2}) \\
L_{17} &= L_{T6} \cdot L_{L1} \cdot L_{T1} + L_{T6} \cdot L_L \cdot L_{T2} - L_{L2} \cdot L_L - L_{L2} \cdot L_{T1}^2 + L_{L1}^2 - L_{L1} \cdot L_{T2} \cdot L_{T1} \\
L_{18} &= -(L_{LT3} \cdot L_{LT1} - L_{LT2} \cdot L_{LT}) \\
L_{19} &= L_{LT3} \cdot L_{L8}
\end{aligned}$$



$$\begin{aligned}
L_{20} &= L_{L11} \cdot L_{LT} + L_{LT3} \cdot L_{L9} \\
L_{21} &= -(L_{LT3} \cdot L_{L4} - L_{LT} \cdot L_{L7}) \\
L_{22} &= L_{L8} \cdot L_{LT} \\
L_{23} &= -L_{L10} \cdot (L_{LT3} - L_{LT}) \\
L_{24} &= L_{LT2} \cdot L_{L8} \\
L_{25} &= L_{L11} \cdot L_{LT1} + L_{LT2} \cdot L_{L9} \\
L_{26} &= -(L_{LT2} \cdot L_{L4} - L_{LT1} \cdot L_{L7}) \\
L_{27} &= L_{L8} \cdot L_{LT1} \\
L_{28} &= -L_{L10} \cdot (L_{LT2} - L_{LT1}) \\
L_{29} &= -L_{T10} \cdot (L_{LT3} \cdot L_{LT1} - L_{LT2} \cdot L_{LT}) \\
L_{30} &= -L_{D4} \cdot L_{L8} \cdot (L_{LT3} - L_{LT2}) \\
L_{31} &= L_{D4} \cdot (L_{L11} \cdot L_{LT1} - L_{L11} \cdot L_{LT} - L_{LT3} \cdot L_{L9} + L_{LT2} \cdot L_{L9}) \\
L_{32} &= L_{D4} \cdot (L_{LT3} \cdot L_{L4} - L_{LT2} \cdot L_{L4} + L_{LT1} \cdot L_{L7} - L_{LT} \cdot L_{L7}) \\
L_{33} &= -L_{D4} \cdot L_{L8} \cdot (L_{LT1} - L_{LT}) \\
L_{34} &= L_{D4} \cdot L_{L10} \cdot (L_{LT3} - L_{LT2} + L_{LT1} - L_{LT}) + L_{LT3} \cdot L_{LT1} - L_{LT2} \cdot L_{LT} \\
L_{35} &= -L_{T3} \cdot (L_{LT3} \cdot L_{LT1} - L_{LT2} \cdot L_{LT}) \\
L_{36} &= -L_{L8} \cdot (L_1 \cdot L_{LT3} - L_{LT2} \cdot L_{T1}) \\
L_{37} &= -(L_1 \cdot L_{L11} \cdot L_{LT} + L_1 \cdot L_{LT3} \cdot L_{L9} - L_{L11} \cdot L_{LT1} \cdot L_{T1} + L_{LT3} \cdot L_{LT1} - L_{LT2} \cdot L_{L9} \cdot L_{T1} \\
&\quad - L_{LT2} \cdot L_{LT}) \\
L_{38} &= -L_1 \cdot (L_{LT3} \cdot L_{L4} - L_{LT} \cdot L_{L7}) + L_{T1} \cdot (L_{LT1} \cdot L_{L7} - L_{LT2} \cdot L_{L4}) + L_{LT3} \cdot L_{LT1} - L_{LT2} \cdot L_{LT} \\
L_{39} &= L_{L8} \cdot (L_1 \cdot L_{LT} - L_{LT1} \cdot L_{T1}) \\
L_{40} &= L_{L10} \cdot (L_1 \cdot L_{LT3} - L_1 \cdot L_{LT} - L_{LT2} \cdot L_{T1} + L_{LT1} \cdot L_{T1})
\end{aligned}$$

Where:

$$\begin{aligned}
L_T &= (L_1 + L_d + L_{d3} + L_{D3} + L_{b2} + L_s + L_{d1}) \\
L_{T1} &= (L_1 + L_{b2} + L_{D3} + L_{d3}) \\
L_{T2} &= (L_1 + L_s + L_{b1}) \\
L_{T3} &= (L_{d3} + L_s + L_{a1} + L_1 + L_{b2} + L_{D3}) \\
L_{T4} &= (L_1 + 2 \cdot L_s + L_{a2} + L_{d4} + L_{b1}) \\
L_{T5} &= (L_d + L_s + L_{b1}) \\
L_{T6} &= (L_d + L_{d3} + L_{D3} + L_{b2}) \\
L_{T7} &= (L_1 + L_d + L_{d3} + L_{D3} + L_{b2} + L_{D4} + L_{b1}) \\
L_{T8} &= (L_1 + L_{D4} + L_{b1}) \\
L_{T9} &= (L_1 + L_s + L_{a2} + L_{d4} + L_{b1} + L_{D4}) \\
L_{T10} &= (L_s + L_{D4}) \\
L_L &= (L_{a1} + L_s) \cdot (L_d + L_{b1} + L_s) + (L_{a1} + L_{b1} + 2 \cdot L_s + L_d) \cdot (L_1 + L_{b2} + L_{D3} + L_{d3}) \\
L_{L1} &= (L_{b1} + L_s) \cdot (L_{b2} + L_{D3} + L_{d3}) - L_{a1} \cdot L_d \\
L_{L2} &= (L_{d4} + L_{a2} + L_s) \cdot (L_1 + L_s + L_{b1}) + (L_d + L_{d3} + L_{D3} + L_{b2}) \cdot (L_1 + L_{b1} + L_{a2} + L_{d4} + 2 \cdot L_s) \\
L_{L3} &= L_s \cdot (L_1 + L_{b2}) + L_{D4} \cdot (L_1 + L_d + 2 \cdot L_s + L_{b1} + L_{b2} + L_{D3} + L_{d3}) \\
L_{L4} &= (L_{D4} + L_s) \cdot (L_1 + L_{b2} + L_{D3} + L_{d3}) \\
L_{L5} &= L_s \cdot (L_1 + L_{b1}) + L_{D4} \cdot (L_1 + L_s + L_{b1}) \\
L_{L6} &= L_s \cdot (L_s + 2 \cdot L_{D4}) + (L_s + L_{D4}) \cdot (L_1 + L_{b1} + L_{a2} + L_{d4}) \\
L_{L7} &= L_1 \cdot (L_{D4} + L_s) \\
L_{L8} &= (L_{D4} + L_s) \cdot (L_1 + L_s + L_{a1} + L_{b2} + L_{D3} + L_{d3})
\end{aligned}$$

$$\begin{aligned}
L_{L9} &= -(L_{D4} + L_s) \cdot (L_{a1} + L_s) \\
L_{L10} &= L_{D4} \cdot (L_1 + L_s + L_{a2} + L_{b2} + L_{D3} + L_{d3}) \\
L_{L11} &= (L_{D4} + L_s) \cdot (L_{a1} + L_s + L_{b2} + L_{D3} + L_{d3}) \\
L_{LT} &= L_{L3} \cdot L_{T3} - L_{T1} \cdot L_{L4} \\
L_{LT1} &= L_{L5} \cdot L_{T3} - L_1 \cdot L_{L4} \\
L_{LT2} &= L_{L6} \cdot L_{T3} - L_1 \cdot L_{L7} \\
L_{LT3} &= L_{L5} \cdot L_{T3} - L_{T1} \cdot L_{L7}
\end{aligned}$$

*d) For Figure 4.17 (b), (d), (f), (h), (j), (l) and (n)*

$$\begin{aligned}
L_{18} &= L_d \cdot L_s \\
L_{20} &= L_s + L_{b1} \\
L_{21} &= L_{d3} + L_s + L_{b2} \\
L_{22} &= L_s \cdot L_{20} \\
L_{23} &= L_{20} \cdot L_{21} - L_1 \cdot L_d \\
L_{24} &= L_{L6} \cdot L_{L4} - L_{L5}^2 \\
L_{25} &= L_{T11} \cdot L_{L4} + L_{L5} \cdot L_{T10} \\
L_{26} &= L_{T6} \cdot L_{L5} + L_{L4} \cdot L_{T7} \\
L_{27} &= -(L_{L5} \cdot L_{T10} - L_{L4} \cdot L_{T7}) \\
L_{28} &= -(L_{T11} \cdot L_{L4} - L_{L5} \cdot L_{T6}) \\
L_{29} &= L_{T5} \cdot L_{L5} \\
L_{30} &= L_{T5} \cdot L_{L4} \\
L_{31} &= L_{T11} \cdot L_{L5} + L_{L6} \cdot L_{T10} \\
L_{32} &= L_{T6} \cdot L_{L6} + L_{L5} \cdot L_{T7} \\
L_{33} &= -(L_{L6} \cdot L_{T10} - L_{L5} \cdot L_{T7}) \\
L_{34} &= -(L_{T11} \cdot L_{L5} - L_{L6} \cdot L_{T6}) \\
L_{35} &= L_{T5} \cdot L_{L6} \\
L_{36} &= L_{T5} \cdot L_{L5} \\
L_{37} &= L_{T5} \cdot (L_{L6} \cdot L_{L4} - L_{L5}^2) \\
L_{38} &= -L_{T11} \cdot (L_{L5} \cdot L_{T6} + L_{L4} \cdot L_{T7}) - L_{L6} \cdot (L_{T10} \cdot L_{T6} - L_{L4}) - L_{L5} \cdot (L_{L5} + L_{T10} \cdot L_{T7}) \\
L_{39} &= L_{L6} \cdot (L_{L4} + L_{T6}^2) - L_{L5} \cdot (L_{L5} - 2 \cdot L_{T7} \cdot L_{T6}) + L_{L4} \cdot L_{T7}^2 \\
L_{40} &= -L_{L6} \cdot (L_{T10} \cdot L_{T6} - L_{L4}) - L_{L5} \cdot (L_{L5} + L_{T10} \cdot L_{T7}) + L_{T7} \cdot (L_{L5} \cdot L_{T6} + L_{L4} \cdot L_{T7}) \\
L_{41} &= -L_{T11} \cdot (L_{L5} \cdot L_{T6} + L_{L4} \cdot L_{T7}) + L_{L6} \cdot (L_{L4} + L_{T6}^2) - L_{L5} \cdot (L_{L5} - L_{T7} \cdot L_{T6}) \\
L_{42} &= L_{T5} \cdot (L_{L6} \cdot L_{T6} + L_{L5} \cdot L_{T7}) \\
L_{43} &= L_{T5} \cdot (L_{L5} \cdot L_{T6} + L_{L4} \cdot L_{T7}) \\
L_{44} &= L_{LT} \cdot L_{LL} - L_{LT1} \cdot L_{LL1} \\
L_{45} &= L_{L12} \cdot L_{LL} + L_{LT1} \cdot L_{LT3} \\
L_{46} &= L_{LT4} \cdot L_{LT1} + L_{L8} \cdot L_{LL} \\
L_{47} &= L_{L7} \cdot L_{LL} \\
L_{48} &= L_{LT5} \cdot L_{LT1} \\
L_{49} &= L_{LT4} \cdot L_{LT1} - L_{L12} \cdot L_{LL} \\
L_{50} &= L_{LT6} \cdot L_{LT1} + L_{L13} \cdot L_{LL} \\
L_{51} &= L_{LT3} \cdot L_{LT} + L_{LL1} \cdot L_{L12}
\end{aligned}$$



$$\begin{aligned}
L_{52} &= L_{L8} \cdot L_{LL1} + L_{LT4} \cdot L_{LT} \\
L_{53} &= L_{L7} \cdot L_{LL1} \\
L_{54} &= L_{LT5} \cdot L_{LT} \\
L_{55} &= L_{LT4} \cdot L_{LT} - L_{L12} \cdot L_{LL1} \\
L_{56} &= L_{L13} \cdot L_{LL1} + L_{LT6} \cdot L_{LT} \\
L_{57} &= L_{44} \cdot L_{L7} \\
L_{58} &= L_{45} \cdot L_{L8} - L_{51} \cdot L_{L9} - L_{44} \cdot L_{T18} \\
L_{59} &= L_{46} \cdot L_{L8} + L_{44} \cdot L_{T18} + L_{L9} \cdot L_{52} \\
L_{60} &= L_{47} \cdot L_{L8} + L_{L9} \cdot L_{53} \\
L_{61} &= L_{48} \cdot L_{L8} + L_{54} \cdot L_{L9} \\
L_{62} &= L_{L8} \cdot L_{49} + L_{L9} \cdot L_{55} + L_{T18} \cdot L_{44} \\
L_{63} &= L_{18} \cdot L_{50} + L_{L9} \cdot L_{56} + L_{D3} \cdot L_{44} \\
L_{64} &= L_{L8} \cdot L_{46} + L_{L9} \cdot L_{52} + L_{T18} \cdot L_{44} \\
L_{65} &= L_{T18} \cdot L_{44} \cdot L_{57} \\
L_{66} &= L_{D3} \cdot (L_{51} \cdot L_{57} - L_{58} \cdot L_{44}) \\
L_{67} &= L_{D3} \cdot (L_{44} \cdot L_{59} - L_{52} \cdot L_{57}) \\
L_{68} &= L_{D3} \cdot (L_{44} \cdot L_{60} - L_{53} \cdot L_{57}) \\
L_{69} &= L_{D3} \cdot (L_{44} \cdot L_{61} - L_{54} \cdot L_{57}) \\
L_{70} &= L_{D3} \cdot (L_{55} \cdot L_{57} - L_{44} \cdot L_{62}) \\
L_{71} &= L_{D3} \cdot (L_{56} \cdot L_{57} - L_{44} \cdot L_{63}) \\
L_{72} &= L_{D3} \cdot (L_{52} \cdot L_{57} - L_{44} \cdot L_{64}) \\
L_{73} &= L_{D3} \cdot (L_{53} \cdot L_{57} - L_{44} \cdot L_{60}) \\
L_{74} &= L_{LL5} \cdot L_{LL2} \cdot L_{LL3}^2 \\
L_{75} &= L_{LT16} \cdot L_{LL3} - L_{LL5} \cdot L_{LT7} \\
L_{76} &= L_{LT17} \cdot L_{LL3} + L_{LL5} \cdot L_{LT8} \\
L_{77} &= L_{LT9} \cdot L_{LL5} \\
L_{78} &= L_{LT9} \cdot L_{LL3} \\
L_{79} &= L_{LT18} \cdot L_{LT10} \cdot L_{LL3} \\
L_{80} &= L_{LT19} \cdot L_{LL3} + L_{LL5} \cdot L_{LT11} \\
L_{81} &= L_{LT16} \cdot L_{LL2} + L_{LL3} \cdot L_{LT7} \\
L_{82} &= L_{LT17} \cdot L_{T22} + L_{LT8} \cdot L_{LL3} \\
L_{83} &= L_{LT9} \cdot L_{LL3} \\
L_{84} &= L_{LT9} \cdot L_{LL2} \\
L_{85} &= L_{LT18} \cdot L_{LL2} + L_{LT10} \cdot L_{LL3} \\
L_{86} &= L_{LT19} \cdot L_{LL2} + L_{LT11} \cdot L_{LL3} \\
L_{87} &= L_{74} \cdot L_{L17} \\
L_{88} &= L_{75} \cdot L_{L18} - L_{74} \cdot L_{T25} + L_{L19} \cdot (L_{LL2} \cdot L_{LT16} + L_{LL3} \cdot L_{LT7}) \\
L_{89} &= L_{76} \cdot L_{L18} + L_{74} \cdot L_{T25} + L_{L19} \cdot (L_{LT22} \cdot L_{LT17} + L_{LL3} \cdot L_{LT8}) \\
L_{90} &= L_{77} \cdot L_{L18} + L_{LT9} \cdot L_{LL3} \cdot L_{L19} \\
L_{91} &= L_{78} \cdot L_{L18} + L_{LT9} \cdot L_{LL2} \cdot L_{L19} \\
L_{92} &= L_{D4} \cdot L_{74} + L_{79} \cdot L_{L18} + L_{L19} \cdot (L_{LL2} \cdot L_{LT18} + L_{LL3} \cdot L_{LT10}) \\
L_{93} &= L_{D3} \cdot L_{74} + L_{LT19} \cdot (L_{LL3} \cdot L_{L18} + L_{LL2} \cdot L_{L19}) + L_{LT11} \cdot (L_{LL5} \cdot L_{L18} + L_{LL3} \cdot L_{L19}) \\
L_{94} &= L_{74}^2 \cdot L_{L17} \cdot L_{T25} \\
L_{95} &= -L_{D3} \cdot L_{74} \cdot (L_{75} \cdot L_{L18} - L_{74} \cdot L_{T25})
\end{aligned}$$

$$\begin{aligned}
L_{96} &= L_{D3} \cdot L_{74} \cdot [L_{76} \cdot L_{L18} + L_{74} \cdot L_{T25} + (L_{L19} - L_{L17}) \cdot (L_{LT17} \cdot L_{T9} + L_{LT8} \cdot L_{LL3})] \\
L_{97} &= L_{D3} \cdot L_{74} \cdot [L_{77} \cdot L_{L18} + L_{LT9} \cdot L_{LL3} \cdot (L_{L19} - L_{L17})] \\
L_{98} &= L_{D3} \cdot L_{74} \cdot [L_{78} \cdot L_{L18} + L_{LT9} \cdot L_{LL2} \cdot (L_{L19} - L_{L17})] \\
L_{99} &= -L_{D3} \cdot L_{74} \cdot [L_{D4} \cdot L_{74} + L_{79} \cdot L_{L18} + (L_{L19} - L_{L17}) \cdot (L_{LT18} \cdot L_{LL2} + L_{LT10} \cdot L_{LL3})] \\
L_{100} &= -L_{74} \cdot L_{D3} \cdot [L_{74} \cdot L_{D3} + L_{LT9} \cdot (L_{LL3} \cdot L_{L18} + L_{LL2} \cdot L_{L19} - L_{LL2} \cdot L_{L17}) + L_{LT11} \\
&\quad \cdot (L_{LL5} \cdot L_{L18} + L_{LL3} \cdot L_{L19} - L_{LL3} \cdot L_{L17})] - L_{74}^2 \cdot L_{L17} \\
L_{101} &= -L_{D4} \cdot L_{74} \cdot [L_{75} \cdot (L_{18} - L_{17}) - L_{74} \cdot L_{T25} + L_{L19} \cdot (L_{LL2} \cdot L_{LT16} + L_{LL3} \cdot L_{LT7})] \\
L_{102} &= L_{D4} \cdot L_{74} \cdot [L_{76} \cdot (L_{18} - L_{17}) + L_{74} \cdot L_{T25} + L_{LT17} \cdot L_{L19} \cdot L_{T22} + L_{LT8} \cdot L_{LL3} \cdot L_{L19}] \\
L_{103} &= L_{D4} \cdot L_{74} \cdot [L_{77} \cdot (L_{18} - L_{17}) + L_{LT19} \cdot L_{LL3} \cdot L_{L19}] \\
L_{104} &= L_{D4} \cdot L_{74} \cdot [L_{78} \cdot (L_{18} - L_{17}) + L_{LT19} \cdot L_{LL2} \cdot L_{L19}] \\
L_{105} &= -L_{74} \cdot L_{D4} \cdot [L_{74} \cdot L_{D4} + L_{79} \cdot (L_{L18} - L_{L17}) + L_{L19} \cdot (L_{LT18} \cdot L_{LL2} + L_{LT10} \cdot L_{LL3})] \\
&\quad - L_{74}^2 \cdot L_{L17} \\
L_{106} &= -L_{74} \cdot [L_d \cdot (L_{D3} \cdot L_{74} + L_{LT19} \cdot L_{LL3} \cdot L_{L18} + L_{LL19} \cdot L_{LL2} \cdot L_{L19} + L_{LT11} \cdot L_{LL5} \cdot L_{L18} \\
&\quad - L_{LT11} \cdot L_{LL3} \cdot L_{L19}) - L_{D4} \cdot (L_{LT19} \cdot L_{LL3} \cdot L_{L17} + L_{LT11} \cdot L_{LL5} \cdot L_{L17})]
\end{aligned}$$

Where:

$$\begin{aligned}
L_{T5} &= (L_1 + L_d + L_{a2} + L_{a1} + 2 \cdot L_s + L_{d4}) \\
L_{T6} &= (L_d + L_s + L_{a1}) \\
L_{T7} &= (L_d + L_s + L_{a2} + L_{d4}) \\
L_{T8} &= (L_d + L_{a1} + 2 \cdot L_s + L_{b1}) \\
L_{T9} &= (L_d + L_{a2} + L_{d3} + 2 \cdot L_s + L_{d4} + L_{b2}) \\
L_{T10} &= (L_1 + L_s + L_{a2} + L_{d4}) \\
L_{T11} &= (L_1 + L_{a1} + L_s) \\
L_{T12} &= (L_1 + L_d + L_{d3} + L_{D3} + L_{b2} + L_s + L_{b1}) \\
L_{T13} &= (L_d + L_s + L_{b1}) \\
L_{T14} &= (L_d + L_{d3} + L_{D3} + L_{b2}) \\
L_{T15} &= (L_{D3} + L_s) \\
L_{T16} &= (L_d + L_{b1} + 2 \cdot L_s + L_{a1}) \\
L_{T17} &= (L_d + L_{d3} + L_{D3} + L_{b2} + L_s + L_{a2} + L_{d4}) \\
L_{T18} &= (L_{D3} + L_s) \\
L_{T19} &= (L_1 + L_d + L_{d3} + L_{D3} + L_{b2} + L_{D4} + L_{b1}) \\
L_{T20} &= (L_d + L_{D4} + L_{b1}) \\
L_{T21} &= (L_d + L_{d3} + L_{D3} + L_{b2}) \\
L_{T22} &= (L_{D3} + L_{D4}) \\
L_{T23} &= (L_d + L_{D4} + L_{b1} + L_3 + L_{a1}) \\
L_{T24} &= (L_d + L_{d3} + L_{D3} + L_{b2} + L_3 + L_{a2} + L_{d4}) \\
L_{T25} &= (L_3 + L_{D3}) \\
L_{L4} &= L_{b1} \cdot (L_1 + L_{a2} + L_{d4}) + (L_1 + L_{a2} + L_{d4} + L_{b1}) \cdot (L_d + 2 \cdot L_s + L_{a1}) + L_s \cdot (2 \cdot L_d + 3 \cdot L_s \\
&\quad + 2 \cdot L_{a1}) \\
L_{L5} &= L_1 \cdot L_d + (L_{a1} + L_s) \cdot (L_s + L_{a2} + L_{d4}) \\
L_{L6} &= (L_{b2} + L_{d3}) \cdot (L_1 + L_d + L_{d4} + L_{a2} + L_{a1} + 2 \cdot L_s) + L_s \cdot (L_d + 3 \cdot L_s) + (L_{d4} + L_{a2}) \cdot (L_1 \\
&\quad + L_{a1} + 2 \cdot L_s) + (L_1 + L_{a1}) \cdot (L_d + 2 \cdot L_s) \\
L_{L7} &= (L_s + L_{D3}) \cdot (L_1 + L_d + L_{d3} + L_{b2} + L_s + L_{b1}) + L_{D3} \cdot L_s
\end{aligned}$$



$$\begin{aligned}
L_{L8} &= (L_s + L_{D3}) * (L_d + L_s + L_{b1}) \\
L_{L9} &= (L_s + L_{D3}) * (L_d + L_{d3} + L_{b2}) + L_{D3} * L_s \\
L_{L10} &= L_d * (L_s + L_{D3}) \\
L_{L11} &= (L_s + L_{D3}) * (L_d + L_{d3} + L_{b2} + L_s + L_{a2} + L_{d4}) + L_{D3} * L_s \\
L_{L12} &= (L_s + L_{D3}) * (L_1 + L_{d3} + L_{b2}) + L_{D3} * L_s \\
L_{L13} &= L_{D3} * (L_d + L_s + L_{b1}) \\
L_{L14} &= -(L_s + L_{D3}) * (L_s + L_{a1}) \\
L_{L15} &= (L_s + L_{D3}) * (L_d + 2 * L_s + L_{b1} + L_{a1}) \\
L_{L16} &= L_{D3} * (L_d + 2 * L_s + L_{b1} + L_{a1}) \\
L_{L17} &= L_{D3} * (L_3 - L_{D4}) + (L_3 + L_{D3}) * (L_1 + L_d + L_{d3} + L_{b2} + L_{D4} + L_{b1}) \\
L_{L18} &= L_3 * (L_d + L_{D4} + L_{b1}) + L_{D3} * (L_{b1} + L_{D3} + L_{D4}) - L_{D4}^2 \\
L_{L19} &= L_3 * (L_1 + L_{d3} + L_{D3} + L_{b2}) + L_{D3} * (L_{d3} + L_{D3} + L_{b2}) \\
L_{L20} &= (L_{a1} + L_3) * (L_3 + L_{D3}) + (L_{D3} + L_3) * (L_d + L_{D4} + L_{b1}) - L_{D4}^2 \\
L_{L21} &= L_d * (L_3 + L_{D3}) \\
L_{L22} &= (L_3 + L_{D3}) * [(L_{d4} + L_{a2}) + (L_d + L_{d3} + L_{b2})] + L_3 * (L_3 + 2 * L_{D3}) \\
L_{LT} &= L_{T16} * L_{L7} - L_{T13} * L_{L8} \\
L_{LT1} &= L_{T13} * L_{L9} - L_d * L_{L7} \\
L_{LT2} &= L_{T16} * L_{L9} - L_d * L_{L8} \\
L_{LT3} &= L_{T18} * L_{L7} - L_{T18} * L_{L9} \\
L_{LT4} &= L_{T18} * L_{L9} \\
L_{LT5} &= L_{T186} * L_{L7} \\
L_{LT6} &= L_{D3} * (L_{L9} - L_{L7}) \\
L_{LT7} &= -L_{T25} * (L_{L18} - L_{L17}) \\
L_{LT8} &= L_{T25} * L_{L18} \\
L_{LT9} &= L_{T25} * L_{L17} \\
L_{LT10} &= L_{D4} * (L_{L18} - L_{L17}) \\
L_{LT11} &= L_{D3} * L_{L18} \\
L_{LT12} &= -L_{T25} * (L_{L20} - L_{L18}) \\
L_{LT13} &= L_{T25} * L_{L20} \\
L_{LT14} &= L_{D4} * (L_{L20} - L_{L18}) \\
L_{LT15} &= L_{D3} * L_{L20} \\
L_{LT16} &= -L_{T25} * (L_{L19} - L_{L17}) \\
L_{LT17} &= L_{T25} * L_{L19} \\
L_{LT18} &= L_{D4} * L_{L19} \\
L_{LT19} &= L_{D3} * (L_{L19} - L_{L17}) \\
L_{LL} &= L_{L7} * L_{L11} - L_{L9}^2 \\
L_{LL1} &= L_{L8} * L_{L9} - L_{L7} * L_{L10} \\
L_{LL2} &= L_{L20} * L_{L17} - L_{L18}^2 \\
L_{LL3} &= -(L_{L21} * L_{L17} - L_{L18} * L_{L19}) \\
L_{LL4} &= -(L_{L21} * L_{L18} - L_{L19} * L_{L20}) \\
L_{LL5} &= L_{L22} * L_{L17} - L_{L19}^2
\end{aligned}$$

e) For Figure 5.8 (b), (d), (f) and (h)

$$\begin{aligned}
 L_1 &= L_{L2} \cdot L_{L1} - L_L^2 \\
 L_2 &= L_{T6} \cdot L_{L1} + L_{T5} \cdot L_L \\
 L_3 &= L_T \cdot L_L + L_{T3} \cdot L_{L1} \\
 L_4 &= L_{T2} \cdot L_L \\
 L_5 &= L_{T5} \cdot L_{L2} + L_{T6} \cdot L_L \\
 L_6 &= L_{T3} \cdot L_L + L_T \cdot L_{L2} \\
 L_7 &= L_{T2} \cdot L_{L2} \\
 L_8 &= L_{T2} \cdot L_1 \\
 L_9 &= L_1 \cdot L_2 \cdot L_{T3} \cdot L_5 \cdot L_T \\
 L_{10} &= L_3 \cdot L_{T3} + L_6 \cdot L_T + L_1 \\
 L_{11} &= L_4 \cdot L_{T3} + L_7 \cdot L_T \\
 L_{12} &= L_{L3} \cdot L_{L1} - L_L^2 \\
 L_{13} &= L_{T2} \cdot L_{L1} \\
 L_{14} &= L_{T5} \cdot L_{L3} + L_{T6} \cdot L_L \\
 L_{15} &= L_{T3} \cdot L_L + L_T \cdot L_{L3} \\
 L_{16} &= L_{T2} \cdot L_{L3} \\
 L_{17} &= L_{T2} \cdot L_{12} \\
 L_{18} &= L_{12} \cdot L_2 \cdot L_{T3} \cdot L_T \cdot L_{14} \\
 L_{19} &= L_3 \cdot L_{T3} + L_{15} \cdot L_T + L_{12} \\
 L_{20} &= L_{13} \cdot L_{T3} + L_4 \cdot L_T \\
 L_{21} &= L_4 \cdot L_{T3} + L_{16} \cdot L_T
 \end{aligned}$$

Where:

$$\begin{aligned}
 L_T &= L_d + L_{a2} + L_{d4} \\
 L_{T1} &= L_d + L_{d3} + L_s + L_{b2} + L_{a2} + L_{d4} \\
 L_{T2} &= L_d + L_{a1} + L_{f1} + L_{a2} + L_{d4} \\
 L_{T3} &= L_d + L_{a1} \\
 L_{T4} &= L_d + L_{a1} + L_{D4} + L_{b1} \\
 L_{T5} &= L_{f1} + L_{a1} \\
 L_{T6} &= L_{f1} + L_{a2} + L_{d4} \\
 L_{T7} &= L_d + L_{a1} + L_s + L_{b1} \\
 L_L &= L_{a1} \cdot (L_{a2} + L_{d4}) - L_{f1} \cdot L_d \\
 L_{L1} &= L_{T1} \cdot L_{T2} - L_T^2 \\
 L_{L2} &= L_{T4} \cdot L_{T2} - L_{T3}^2 \\
 L_{L3} &= L_{T7} \cdot L_{T2} - L_{T3}^2
 \end{aligned}$$

f) For Figure 5.11 (b), (d), (f), (h) and (j)

$$\begin{aligned}
 L_1 &= L_{L2} \cdot L_L + L_{L1} \cdot L_{L3} \\
 L_2 &= L_{T6} \cdot L_L + L_{T7} \cdot L_{L3} \\
 L_3 &= L_d \cdot L_{L3} + L_{T8} \cdot L_L \\
 L_4 &= L_T \cdot L_{L3}
 \end{aligned}$$



$$\begin{aligned}
L_5 &= L_{T7} \cdot L_{L2} - L_{T6} \cdot L_{L1} \\
L_6 &= L_d \cdot L_{L2} - L_{T8} \cdot L_{L1} \\
L_7 &= L_T \cdot L_{L2} \\
L_8 &= L_T \cdot L_1 \\
L_9 &= L_1 + L_5 \cdot L_{T1} - L_2 \cdot L_{T2} \\
L_{10} &= L_6 \cdot L_{T1} + L_1 \cdot L_3 \cdot L_{T2} \\
L_{11} &= L_7 \cdot L_{T1} - L_4 \cdot L_{T2} \\
L_{12} &= L_{L7} \cdot L_{L4} - L_{L6}^2 \\
L_{13} &= L_{T16} \cdot L_{L4} + L_{T15} \cdot L_{L6} \\
L_{14} &= L_{T10} \cdot L_{L4} - L_{T11} \cdot L_{L6} \\
L_{15} &= L_{T9} \cdot L_{L4} \\
L_{16} &= L_{T15} \cdot L_{L7} + L_{T16} \cdot L_{L6} \\
L_{17} &= L_{T10} \cdot L_{L6} - L_{T11} \cdot L_{L7} \\
L_{18} &= L_{T9} \cdot L_{12} \\
L_{19} &= L_{12} - L_{13} \cdot L_{T10} - L_{16} \cdot L_{T11} \\
L_{20} &= L_{14} \cdot L_{T10} + L_{17} \cdot L_{T11} + L_{12} \\
L_{21} &= L_{15} \cdot L_{T10} + L_{L8} \cdot L_{T11} \\
L_{22} &= L_{L7} \cdot L_{L5} - L_{L6}^2 \\
L_{23} &= L_{T16} \cdot L_{L5} + L_{T15} \cdot L_{L6} \\
L_{24} &= L_{T11} \cdot L_{L6} + L_{T10} \cdot L_{L5} \\
L_{25} &= L_{T9} \cdot L_{L5} \\
L_{26} &= L_{T9} \cdot L_{L5} \\
L_{27} &= L_{T15} \cdot L_{L7} + L_{T16} \cdot L_{L6} \\
L_{28} &= L_{T10} \cdot L_{L6} + L_{T11} \cdot L_{L7} \\
L_{29} &= L_{T9} \cdot L_{L7} \\
L_{30} &= L_{T9} \cdot L_{22} \\
L_{31} &= L_{22} - L_{23} \cdot L_{T10} - L_{27} \cdot L_{T11} \\
L_{32} &= L_{24} \cdot L_{T10} + L_{28} \cdot L_{T11} + L_{22} \\
L_{33} &= L_{25} \cdot L_{T10} + L_{29} \cdot L_{T11} \\
L_{34} &= L_{26} \cdot L_{T10} + L_{25} \cdot L_{T11}
\end{aligned}$$

Where:

$$\begin{aligned}
L_T &= L_d + L_{d3} + L_{D3} + L_{b2} \\
L_{T1} &= L_d + L_{D4} + L_{b1} \\
L_{T2} &= L_T + L_{D4} + L_{b1} \\
L_{T3} &= L_d + L_s + L_{a1} + L_{D4} + L_{b1} \\
L_{T4} &= L_{D4} + L_{b1} \\
L_{T5} &= L_{b1} + L_{D4} + L_T + L_{a2} + L_{d4} \\
L_{T6} &= L_{a2} + L_{d4} \\
L_{T7} &= -(L_{d3} + L_{D3} + L_{b2}) \\
L_{T8} &= L_d + L_{d3} + L_{D3} + L_{b2} + L_{a2} + L_{d4} \\
L_{T9} &= L_d + L_{a1} + L_T + L_{a2} + L_{d4} \\
L_{T10} &= L_d + L_{a2} + L_{d4} \\
L_{T11} &= L_d + L_{a1}
\end{aligned}$$

$$LT_{12} = L_d + L_{a1} + L_{D4} + L_{b1}$$

$$LT_{13} = L_d + L_{a1} + L_s + L_{b1}$$

$$LT_{14} = L_d + L_{d3} + L_s + L_{b2} + L_{a2} + L_{d4}$$

$$LT_{15} = L_r + L_{a2} + L_{d4}$$

$$LT_{16} = L_r + L_{a1}$$

$$L_L = LT_3 \cdot L_T \cdot LT_1 \cdot L_d$$

$$L_{L1} = LT_2 \cdot L_d \cdot LT_4 \cdot L_T$$

$$L_{L2} = LT_5 \cdot L_T + LT_2 \cdot LT_6$$

$$L_{L3} = LT_4 \cdot L_T + LT_1 \cdot LT_6$$

$$L_{L4} = LT_9 \cdot LT_{12} - LT_{11}^2$$

$$L_{L5} = LT_9 \cdot LT_{13} - LT_{11}^2$$

$$L_{L6} = LT_{10} \cdot LT_{11} - L_d \cdot LT_9$$

$$L_{L7} = LT_9 \cdot LT_{14} - LT_{10}^2$$

$$L_{L8} = LT_9 \cdot L_{L6}$$



## THE MECHANICAL ARRANGEMENT OF POWER SEMICONDUCTORS IN CONVERTERS

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UPEC 87

INTRODUCTION

High power DC choppers and DC-AC converters employing forced commutated thyristors or transistors can be considerably simplified by using gate turn-off thyristors (GTOs) as the switching devices. This allows the elimination of auxiliary commutating components which, together with faster turn-off properties of GTOs, provides a reduction in circuit losses, or alternatively the use of higher switching frequencies. However, the difficulties of coping with the induced voltage transients produced by high rates of change of current in the stray circuit inductances are exacerbated. As the stray inductances are directly dependent on the power circuit configuration, the layout of the power components and their interconnection is of the utmost importance. The stray inductance within the gate drive circuit is also important.

As with all power semiconductor devices, GTOs must be protected against overvoltages, overcurrent and spurious pulses in the control leads. In contrast, inductance is necessary to limit the rate of current rise under fault condition to allow the overcurrent protection time to operate.

The concepts that follow are generally applicable to power semiconductor circuits, although the description and experimental results relate to GTO circuits.

CIRCUIT MODELS AND STRAY INDUCTANCE EFFECTSGate Drive Circuit

It is advantageous to keep low the on-drive circuit inductance (Fig.1) in order to obtain a short risetime gate current for fast turn-on, good anode current  $di/dt$  performance, and lowest turn-on losses. Similarly at GTO turn-off, the gate drive inductance (Fig.1) should be minimised for fast turn-off. Along with the gate drive voltage, which must be limited to the low value of about 10-12 V, the inductance controls the  $di/dt$  of the rising negative gate current, the GTO storage time, the peak gate current and the anode current fall time for an individual device, as demonstrated by the oscillograms of Fig.2.

Chopper Circuit

A DC chopper circuit is shown in Fig.3. The turn-off capability of the GTO can be fully utilised only with limited anode voltage  $dv/dt$ ; this is controlled by the familiar snubber circuit. During the anode current fall time, the anode current is diverted extremely quickly into the snubber circuit, resulting in the parasitic inductance ( $L_2+L_3$ ) of the GTO to snubber loop, and the finite turn-on time of the snubber diode, generating a voltage spike (Fig.4) which must not exceed about  $1/3$  of the voltage rating (Peppel et al (1)). At the end of anode current fall, the voltage spike collapses to the accumulated voltage across the snubber capacitor.

With the device now blocking current, voltage builds up across it as the diverted anode current charges the snubber capacitor during its fall to zero, (Fig.4). Correspondingly, the GTO thyristor voltage rises further with a quarter-cycle of damped oscillation to a peak overshoot (Hall (2), Hall et al (3)).

The aforementioned applies for both resistive and inductive loads except for the following main points with the inductive loads:

- (i) After the spike, a linear voltage rise to the supply voltage level takes place, whereas it is the early part of a sinewave for a resistive load (Fig.4). Little difference in the waveform shape results.
- (ii) The overshoot voltage peak is higher, as the damping effect of the load resistance is absent due to the freewheeling path. It will be higher still if the ( $L_1+L_3+L_4+L_d$ ) stray is higher than ( $L_1+L_3+L_d$ ) for resistive load.
- (iii) The voltage overshoot energy is transferred into the snubber capacitor from the stray inductances after the capacitor voltage has risen to the supply voltage level; with resistive load, this transfer commences immediately after the voltage spike.

Single-phase Bridge Inverter Circuit

Fig.5 shows the circuit with lumped stray inductances. It is capable of operating as a 4-quadrant DC chopper, or a single-phase inverter, the latter being considered here. To terminate a supply voltage half-cycle to the load, with say GTOs A1 and A2 conducting, there are two alternatives:

- (i) To turn off one device, say A2; the inductive load current then freewheels through D3 and A1;
- (ii) To turn off both A1 and A2, the load current then feeds back the inductive load energy to the DC supply through D3 and D4.

To investigate both types of commutation, the sequence here is to first turn off A2 and then, before the freewheeling current has fallen to zero, turn off A1. Similarly with B2 and B1 for the opposite half-cycle. Always when a switching device turns off, the load current transfers to the diode of the bridge arm immediately above or below, as appropriate.

The effects of the stray inductance components are considerably more complex than in the chopper. When A2 turns off:

- (a) the load current divides between charging the A2 snubber capacitor and discharging the B2 snubber capacitor which has been holding the supply voltage; when the A2 overshoot is completed, the full load current will have transferred to D3, the overshoot amplitude depending on ( $L_d+L_3+L_{D3}+L_{B2}+L_{A2}+L_{D4}$ );
- (b) if the source inductance  $L_d$  is considerably higher than the sum of those round the bridge loop, the A2 overshoot is conductively coupled round the outside of the bridge and felt across the blocking B1 device; expressed alternatively, most of the A2 overshoot is generated by  $L_d$  and the voltage across B1 rises from the supply voltage level to the overshoot value; the oscillograms of Fig.6 demonstrate this well;

When, later, A1 turns off, the load current divides between charging its snubber capacitor and discharging that across B1, before falling to zero at peak overshoot and reversing in the DC source, D4 then conducting. Since a lower current is being switched off by A1, then switching stresses are lower than



when A2 is turned off.

Additional points relating to the waveforms of Fig.6 are:

- (i) the effect of the A2 snubber diode reverse recovery is observable immediately following the overshoot voltage peak across A2;
- (ii) a little later, the B1 snubber diode reverse recovery is observable in the A2 voltage waveform;
- (iii) the subsequent voltage 'undershoot' felt across A2 is also seen across B1;
- (iv) the  $dv/dt$  following the undershoot can trigger a blocking device and therefore be dangerous, i.e. leave both A1 and B1 conducting;

A further type of current transfer occurs in pulse-width-modulated (pwm) inverters where, instead of the quasi-squarwave output voltage, each positive or negative half-cycle comprises a series of pulses of differing widths to produce a desired fundamental component. In addition to relinquishing the load current to either a freewheeling or feedback path as above, each GTO must pick up the current again from that path. There will be a tendency for the voltage across a diode to overshoot as its parallel snubber capacitor charges, but it will not be as severe as at GTO turn-off.

#### METHODS OF MINIMISING PARASITIC TRANSIENT EFFECTS

##### Introduction

The limitation of transient voltages which stress the active circuit components can be approached in terms of the choice of components and the arrangement of the active and passive components in the circuit. These are perhaps best expressed in the form of general rules. It is desirable that current transfers into the alternative paths take place as quickly as possible to avoid additional device switching losses which occur; for example, due to a transient shoot-through condition as a GTO picks up feedback or freewheeling current from the diode immediately above or below it in a pwm inverter, since both diode and thyristor are conducting together owing to their finite switching times.

##### Choice of Components

Relating to the drive circuit:

- The final switching devices should be very fast - FETs are usual;
- The gate pulse energy storage capacitor(s) should have low internal equivalent series inductance (ESL);

Relating to the power circuit:

- All power semiconductors should be of the fast turn-off type, including feedback and snubber diodes whose reverse recovery transients can be very detrimental; ideally the diodes should be fast turn-on also, but this is unfortunately incompatible with fast turn-off (Grant and Carrol (4));
- All capacitors should have very low inductance (ESL); the input filter capacitor ESL can contribute significantly to the source inductance;
- The technique of using paralleled capacitors to reduce overall ESL, thereby also increasing C is generally useful (Gibson and Ballad (5));
- The snubber capacitor should be as low as is acceptable for safe GTO turn-off to limit the loss in the snubber resistor, and hence its size.
- The snubber resistance should adequately limit the discharge of the capacitor into the GTO at turn-on and no more, as its IR drop contributes to the voltage undershoot which occurs after snubber diode reverse recovery at GTO turn-off.

##### Circuit Configuration

The overriding theme in circuit layout for transient

overvoltage limitation is to minimise the stray inductances.

Relating to the gate circuit:

- The gate driver should be close to the GTO;
- The gate and cathode control leads should be short, twisted pairs or coax;

Relating to the power circuit:

- The length of all interconnectors should be a minimum with their cross-sectional area as large as feasible;
- Loop areas should be as small as possible;
- The semiconductors in each switching branch-GTO, freewheeling diode and snubber diode- should be mounted on the same cooling fin;
- The upper and lower switching arms of an inverter bridge should be very close together;
- The supply reservoir capacitor should be right across the input terminals;
- In a chopper, the freewheeling diode should be connected across the GTO cathode and supply negative so that the stray lead inductance to the perhaps remote load is incorporated in the load inductance.

#### CONFLICTING FEATURES

A number of possible requirements conflict with the concept of a compact circuit layout in practice.

These are:

- Mechanical convenience of electrical connections and accessibility for maintenance;
- The need to include extra, possibly large, passive components for device protection (see next section) and filtering;
- With air cooling, the heatsink size often prohibits the mounting of snubber capacitors adjacently with the GTOs; this is less of a problem with liquid cooling;
- The space required for pipework if liquid cooling is used;
- Adequate separation for airflow with natural or forced air cooling;
- Electromagnetic compatibility (EMC): the two distinct areas of electromagnetic interference (EMI) are disturbance of the control electronics due to pick-up within the equipment, and disturbance caused to other external equipment;
- Conductors of large area in close proximity have not insignificant stray capacitance; when their relative potentials change suddenly due to device switching, capacitive currents flow between them and must return through some stray path, perhaps the equipment case; local screening is necessary to provide a controlled safe path for such currents to avoid interfering conduction paths and radiation;
- High rates of change of magnetic field produce parasitic induced emfs in local circuitry and the metal equipment cubicle; again screening is necessary, particularly for the control electronics;
- Frequently space must be found for EMI filters to cover the radio frequencies in addition to the lower frequency power harmonic filters, for limitation the conducted EMI outside the equipment.

#### FAULT CURRENT LIMITATION AND DEVICE PROTECTION

Mention has been made of ~~the need for device overcurrent protection~~ / Minimisation of stray inductances offsets their beneficial effect in limiting a rising current  $di/dt$ , either at switching device turn-on or under short-circuit fault. Conventional thyristors and GTOs can be protected by fuses; transistors cannot. Transistors must be, and GTOs can be, turned off by base/gate turn-off signals generated after very fast detection of a rising fault current. In practice the  $di/dt$  must then be limited by an extra, relatively large air-cored, inductor in series with each switching device. The tremendous prospective overshoot voltages then can be suppressed by a diode and resistor in parallel with each inductor to dissipate its stored energy.



An L-C input filter is invariably used. The inductor will limit the  $di/dt$  from the source but the stored energy in the capacitor will usually 'kill' the semiconductors without the protection of a suitable fuse or active turn-off system as outlined.

### CONCLUSIONS

The deleterious effects of stray inductances in power converter circuits, sometimes fractions of a microhenry in practice, have been described and confirmed experimentally. General guidelines for minimising these strays have been put forward, covering both choice of components and compact circuit layout. However, practical designs introduce opposing factors, such as the need to provide filtering and screening for EMI suppression, and to accommodate overcurrent protection components.

Detailed consideration of such stray inductances is therefore worthwhile as there is no prospect of them being eliminated. The best that can be hoped for is to limit the consequences.

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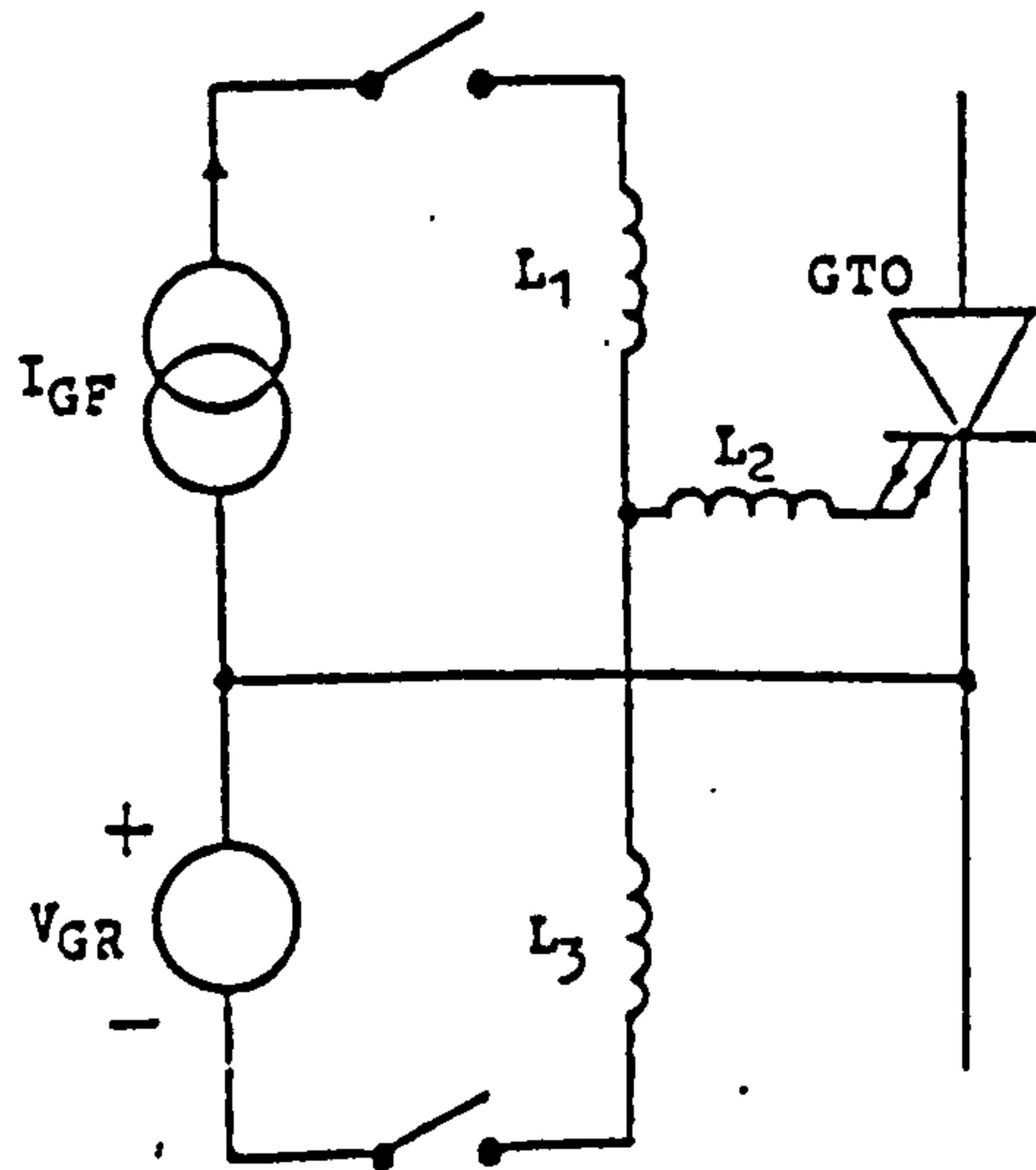
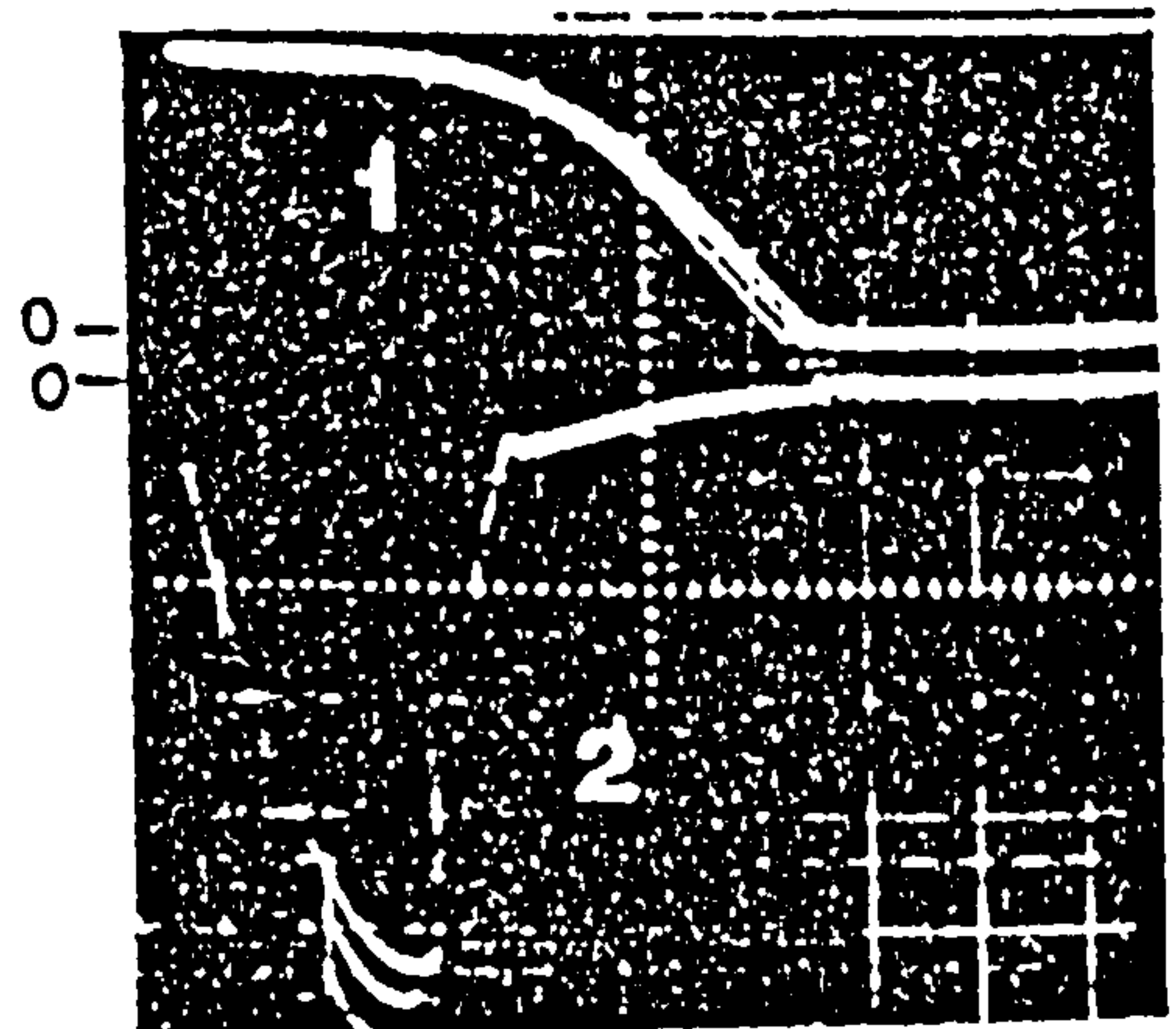


Figure 1 Gate drive circuit stray inductances  
 $L_1$ ,  $L_2$  and  $L_3$  are stray inductances

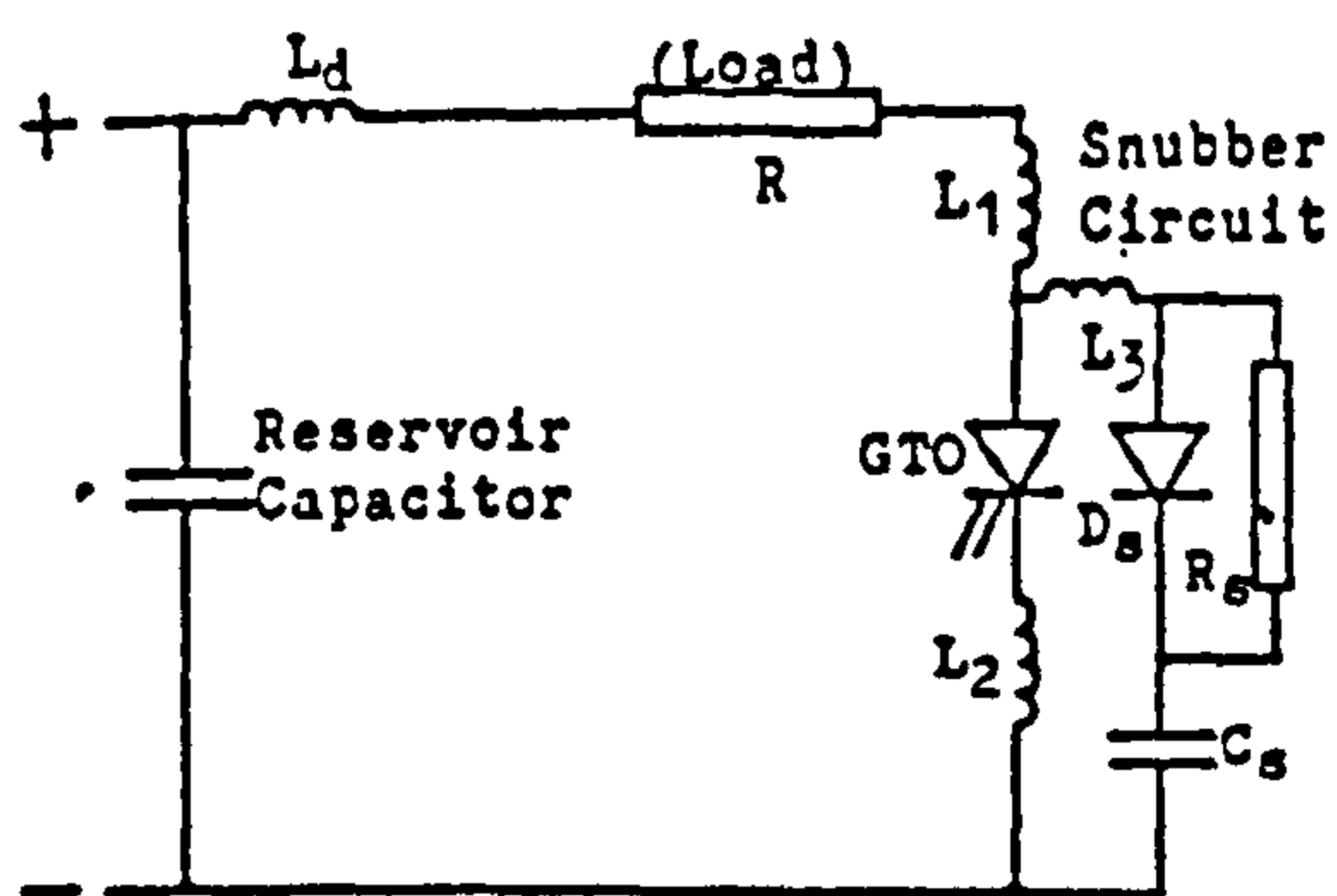
### ACKNOWLEDGEMENT

Acknowledgement is made for the provision of experimental facilities by the Department of Electronic and Electrical Engineering, Loughborough University of Technology.

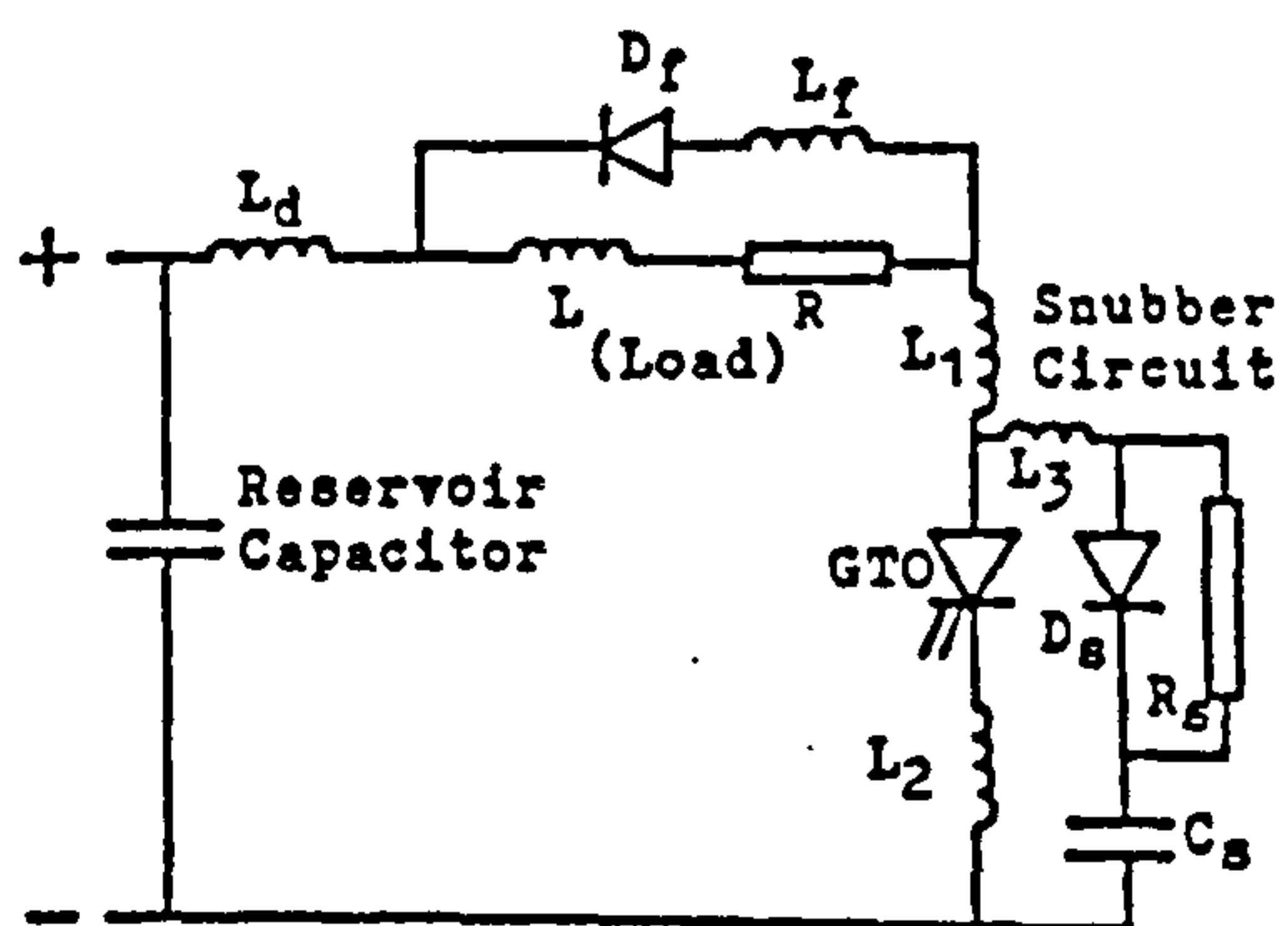


(1) Load Current 200A/div.  
(2) Gate Current 20A/div.  
Time Scale 2μSec/div.  
Circuit Conditions as for figure 4

Figure 2 Effect of varying  $di/dt$  on turn-off time and turn-off gain

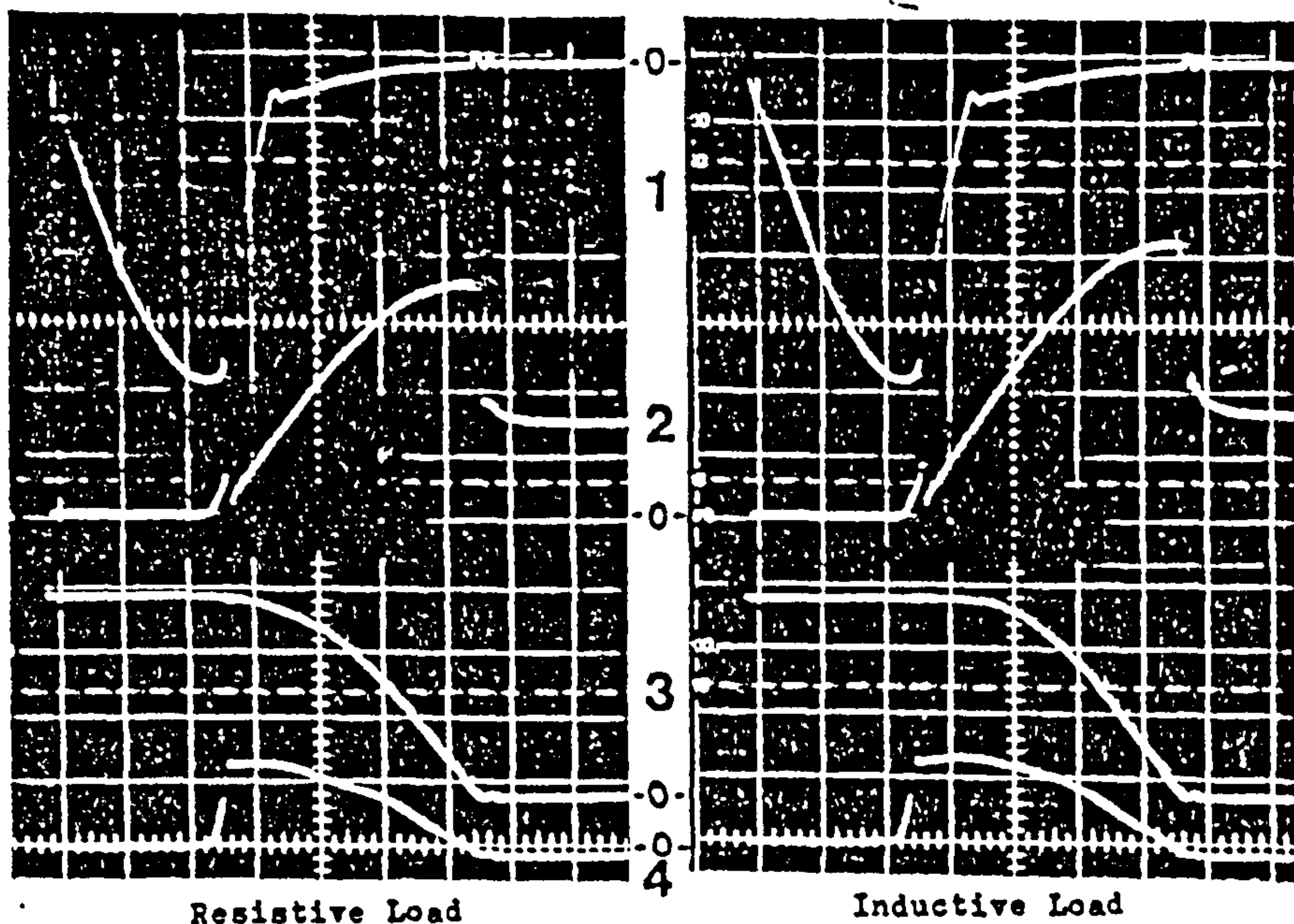


Chopper with resistive load



Chopper with inductive load and freewheeling path

Figure 3 GTO thyristor chopper circuits with lumped stray inductances



- (1) Gate Current 20A/div.  
 (2) Anode-Cathode Voltage 200V/div.  
 (3) Load Current 200A/div.  
 (4) Snubber Current 400A/div.

Time Scale 2μSec/div.

Circuit Conditions: Chopping Frequency 100Hz  
 Chopping Duty Cycle 6%  
 Snubber Capacitance 4μF  
 Snubber Resistance 8Ω  
 Load Resistance 0.5Ω  
 Load Inductance 65μH  
 Gate Current Slope 26A/μSec

Figure 4 GTO thyristor waveforms during turn-off

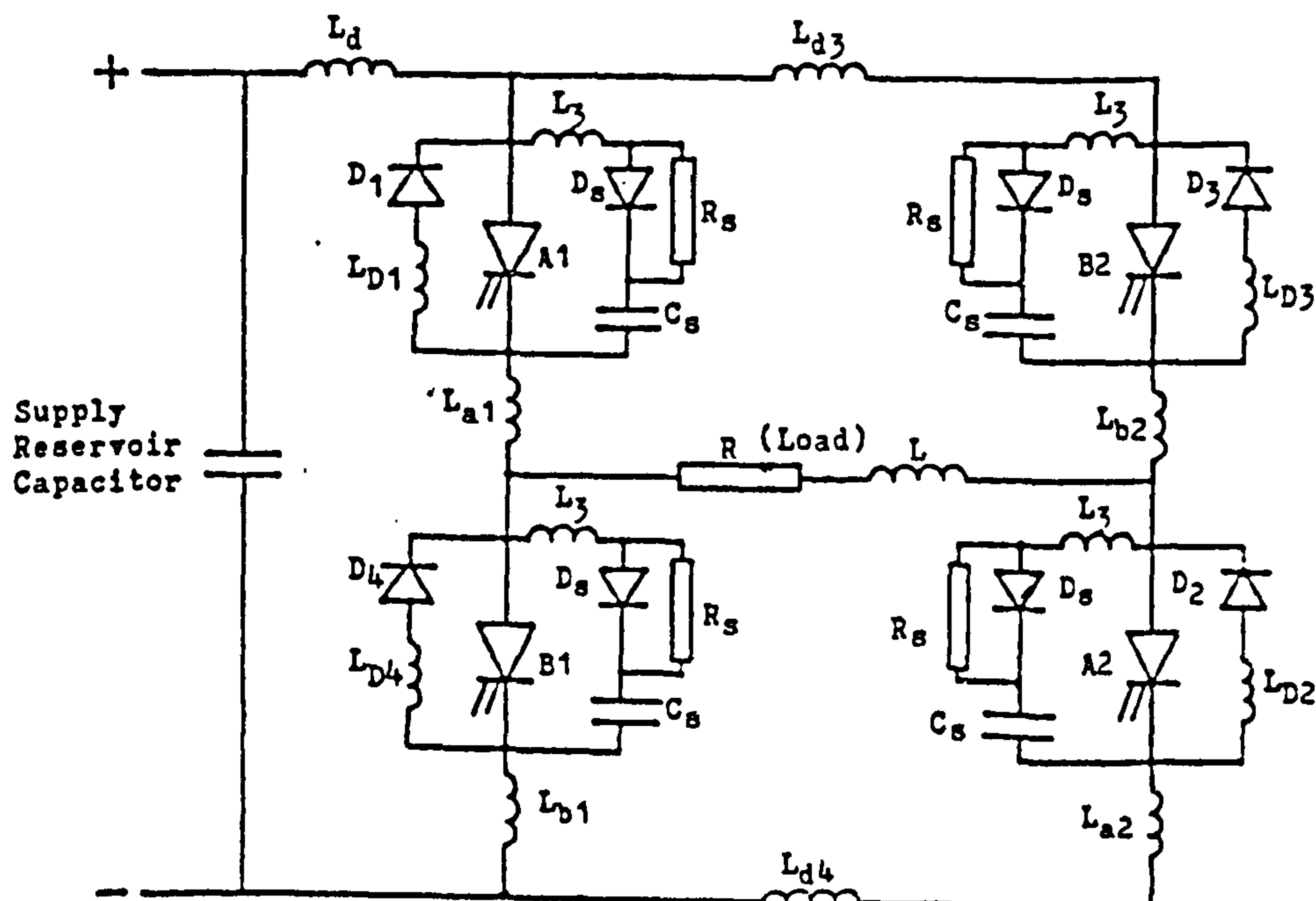
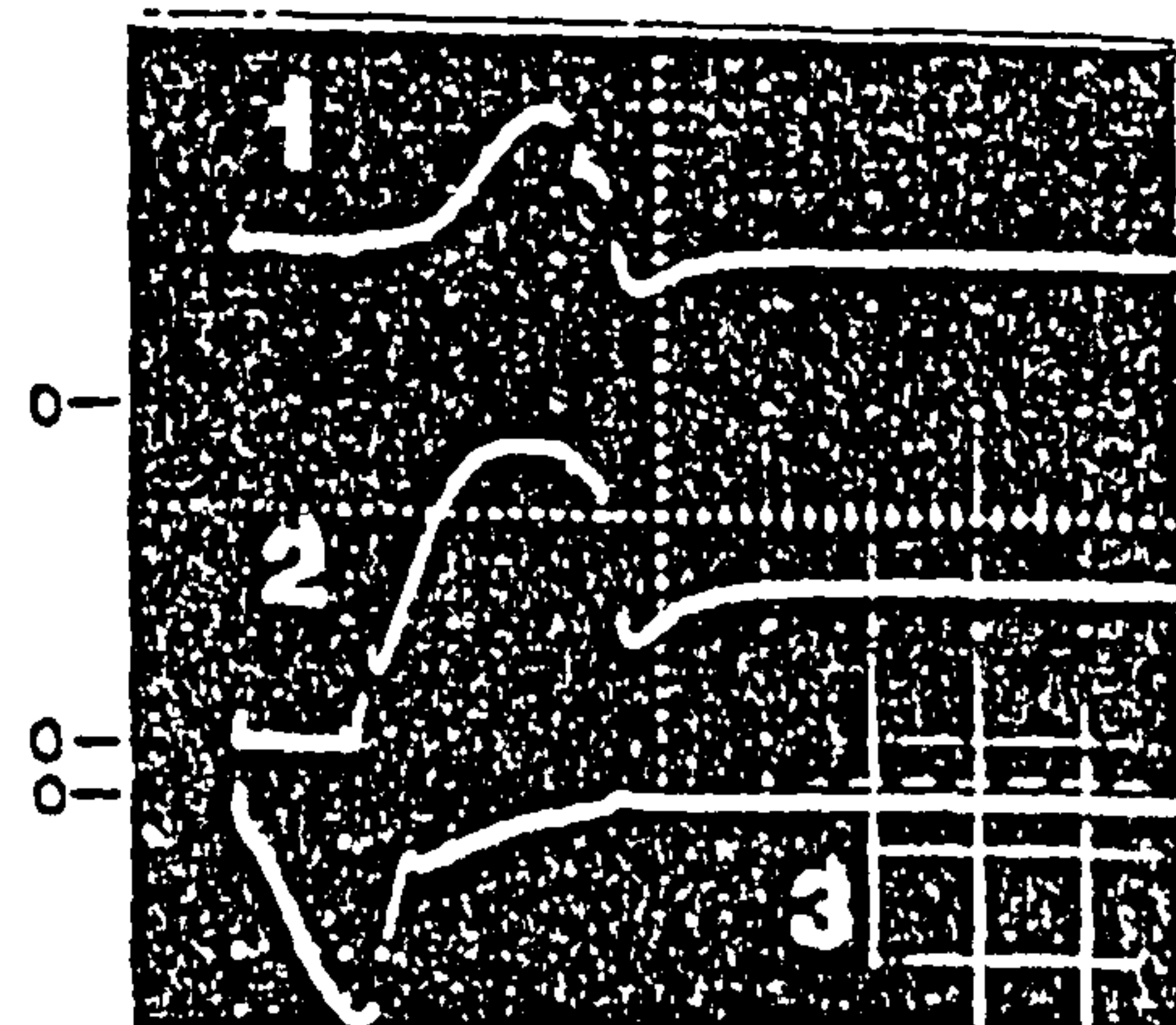


Figure 5 Inverter circuit with lumped stray inductances



- (1) B1 anode-cathode voltage 100V/div.  
 (2) A2 anode-cathode voltage 100V/div.  
 (3) A2 gate current 20A/div.

Time scale 2μSec/div.

Figure 6 Coupled overshoot voltages in the GTO bridge inverter



## INTRODUCTION

Gate turn-off thyristors (GTOs) interrupt current at such tremendously high rates of fall, typically approaching 4000A/μs in high power types, that the voltages induced by stray inductances as low as a fraction of a microhenry can be damaging. This necessitates the connection of a snubber network across each GTO, into which its anode current is diverted at turn-off. Even then, the stored energy in the stray inductances is transferred into the snubber capacitor resulting in appreciable voltage overshoot which must be limited to an acceptable value in relation to the GTO voltage rating by suitably increasing the capacitance. The resulting disadvantages are increased snubber losses and/or limitation of switching frequency, increased snubber component ratings and size, and a consequent increase of snubber loop inductance and higher induced voltage spike across the GTO during its anode current fall as current transfers to the snubber.

Here some results are presented from a study into the relative importance of the various lumped circuit path stray inductances in generating these overshoot voltages. Mutual coupling effects are ignored for simplification. The widely used circuits of the DC step-down chopper and the H-bridge are considered, the latter being capable of operation as a four-quadrant chopper or a single-phase inverter, with the current paths at commutation being dependent on the switching pattern employed.

Determination of the most significant stray circuit inductances has implications for the power circuit layout.

## CHOPPER

An inductive load with freewheeling diode has been adopted for the step-down chopper circuit. This is shown in Figure 1(a) which includes stray path inductances. The aforementioned voltage spike across the GTO can be estimated from:

$$V_{sp} = 1.6(L_2+L_3) I_T/t_f + 0.15 I_T t_f / C \quad (1)$$

where  $(L_2+L_3)$  is the GTO - snubber loop inductance,  $t_f$  is the GTO current fall time,  $I_T$  is the interrupted current and  $C$  is the snubber capacitance. This equation is generally applicable to any circuit. The spike is illustrated in Figure 2(2) which also shows the overshoot which follows.

On collapse of the voltage spike to the accumulated capacitor voltage,  $C$  is charged linearly by the constant load current to the supply voltage  $E_d$  when the load freewheeling diode  $D_f$  commences conduction, the complete transfer of load current from the snubber into  $D_f$  being controlled by the stray inductances during which time the voltage across  $C$  overshoots to a peak value given (neglecting losses) by:

$$V_{pk} = I_T \sqrt{L/C} + E_d \quad (2)$$

where  $L = L_1+L_3+L_d+L_f$  (defined by Figure 1(a)). The overshoot time  $t_{os} = \pi/\sqrt{LC}/2$ .

The reverse recovery of the snubber diode  $D$  follows as  $C$  discharges back into the DC source, the process then being completed through resistor  $R$  as a damped

oscillation, the capacitor voltage finalising at the  $E_d$  value. It is necessary to employ a fast recovery snubber diode and a relatively low value for  $R$  (with low self inductance) to avoid the GTO voltage seriously undershooting  $E_d$  with possible  $dV/dt$  triggering on its rise (Gibson and Pallad (1)).

For a resistive load,  $L_f$  is absent and the overshoot is damped significantly by the load resistance.

If a  $di/dt$  limiting inductor with its own free-wheeling diode is included in series with the GTO and snubber, it is treated as above.

## H - BRIDGE

Figure 1(b) shows the bridge circuit with stray inductances included; again the load is inductive. It is operated as a single phase inverter in order to incorporate all the alternative current transfer paths by using appropriate GTO switching patterns. The output voltage waveform may be of two basic types.

## Quasi-square Output Voltage

Turning off one of the two diagonal conducting GTOs to end a half-cycle gives freewheeling of the inductive load current through the other GTO and the diode of the complementary bridge arm, above or below as appropriate, that which turned off. The voltage across the load is zero during freewheeling, neglecting device conduction drops. Turning off both conducting GTOs produces feedback of the load current to the DC supply through the diodes of the two complementary bridge arms. The voltage across the load reverses during feedback. The next GTOs to be turned on are those of the complementary bridge arms, the first pair both being turned off.

## Output Voltage with Pulse Width Modulation (PWM)

Either of the previous techniques may be used for turn-off. At the end of a half-cycle, the next GTOs to be gated will be the complimentary diagonal pair to those previously conducting, as above. Additionally with PWM, the switching within a half-cycle requires current to be returned from the freewheeling/feedback diode to the GTO of the complementary bridge arm, above or below, from whence it came.

## Turn-off Transients

At single GTO turn-off. Referring to Figure 1(b), let GTOs A1 and A2 be conducting. If A2 is turned off, load current transfers from A2 to D3. Initially the load current divides to discharge the B2 snubber capacitor and charge the A2 snubber capacitor, the latter current falling from the value diverted from A2 to  $I_o$  as the capacitor charges to the supply voltage  $E_d$  (Figure 3(1)). Diode D3 then commences conduction and the A2 capacitor voltage overshoots due to the stray inductances. The capacitor then discharges back into the supply, firstly through its snubber diode reverse recovery and then through the associated resistor, as in the chopper. The peak voltage across A2 at overshoot is given by equation (2), but with  $I_T$  replaced by  $I_o$ . Now the effective inductance  $L = 2L_d + 3L_3 + L_{b1} + L_{b2} + L_{a2} + L_{d3} + L_{d4} + L_{p4}$ .

However, the induced voltage across the source inductance  $L_d$  during this oscillation lifts the DC voltage across the bridge, causing the blocking GTO B1



capacitor to charge above  $E_d$ . This too is followed by discharge through its snubber diode reverse recovery which is completed marginally later than that of A2 which, however, experiences both, as shown by Figure 3(2). It is apparent therefore, that overshoot transients from one device in the bridge are coupled conductively to others. The higher ( $L_{d3}+L_{d4}$ ) in relation to  $L_d$ , the lower will be the coupled overshoot.

At second GTO turn-off following the first. After A2 turn-off has produced freewheeling, subsequent turn-off of the second GTO A1 will produce feedback of load current when current transfers to D4. Initially load current divides between the snubber capacitors of A1 which charges and B1 which discharges. When the latter voltage falls to zero, current transfers into D4, the strays  $L_3$  and  $L_{D4}$  controlling the rate. A1 capacitor voltage overshoots followed by a damped discharge to  $E_d$  as usual. The peak voltage at overshoot across A1 follows the same equation as for A2 above, although its magnitude is lower because it turns off a lower current, decay having occurred during free-wheeling, and the effective inductance is lower with  $L = L_d + L_{a1} + L_{b1} + L_3 + L_{D4}$ .

At turn-off of both GTOs together. The load current transfers from A1 and A2 to the D3 and D4 feedback path without an intermediate freewheeling stage. The snubber capacitors of the various arms charge and discharge as before, those across A1 and A2 experiencing voltage overshoot followed by damped discharge to voltage  $E_d$ . If stray inductances  $L_{d3}$  and  $L_{d4}$  are relatively small, the peak voltages across A1 and A2 are nearly the same and given approximately by:

$$V_{pk} = \frac{I_o}{\omega C} \left[ 2 - \frac{\pi}{2} + \frac{L_1}{L} \right] + E_d \quad (3)$$

where  $\omega = \sqrt{2/LC}$ ,  $L_1 = 2L_d + 2L_3 + L_{a2} + L_{d4} + L_{a1}$

$L = 4L_d + 3L_3 + L_{a1} + L_{a2} + L_{b2} + L_{d4} + L_{D3} + L_{D4}$

Appropriate waveforms are given in the oscillograms of Figure 4.

#### Turn-on-Transients

GTOs gated with zero load current. If the load current falls to zero during freewheeling or feedback, all four GTOs are blocking prior to turn-on, each supporting half the supply voltage ( $E_d/2$ ). When GTOs A1 and A2 are turned on, their parallel snubber capacitors discharge locally through them while the B1 and B2 snubber capacitor voltages rise to  $E_d$  and, owing to the stray inductances, overshoot by up to a maximum of  $E_d/2$ . Hence the maximum peak voltage across the non-conducting GTOs at turn-on of the other pair is  $3E_d/2$ .

GTOs gated from the freewheeling condition. This is not valid because all GTOs must be turned off before a new pair can be gated so that a shoot-through condition (say A1 and B1 conducting together) is avoided. Load current will then feed back to the source before an incoming GTO pair is next turned on.

GTOs gated from the feedback condition. Here there will be no transients. The load voltage reversal occurs when D3 and D4 take the load current from A1 and A2. The current reversal instant depends on the load time constant and, providing GTOs B1 and B2 are already gated, they will automatically come into conduction then, with the circuit potentials already having been established.

Single GTO turn-on from freewheeling within a half cycle for PWM. Let A1 have been turned off so that current freewheels through A2 and D4. A1 is now turned on again to pick up the current from D4. It discharges its snubber capacitor, and current transfer takes place with the D4 current fall having a cosine form (Figure 5(3)). This is due to the bridge voltage being depressed by  $L_d di/dt$  and the B2 snubber

capacitor discharging through its resistor R, A1 and the path inductances. When D4 ceases conduction, B1 snubber capacitor charges through A1 with the DC rail voltage depressed until peak A1 current is reached, after which overshoot of both B1 and B2 capacitor voltages occurs, peaking at different instants owing to the different path inductances.

The process contains a number of consecutive circuit effects making the complex solution for the voltage overshoot magnitude hardly worth quoting. It can be seen from the oscillograms of Figure 5 that the highest overshoot is about 60% felt across B2.

Double GTO turn-on from feedback within a half-cycle for PWM. Let A1 and A2 have been turned off with feedback current therefore flowing through D3 and D4. A1 and A2 are then gated to pick up the current from the diodes, and their parallel snubber capacitors discharge through them. B1 and B2 snubber capacitors charge to  $E_d$  and overshoot by a voltage which will not exceed  $E_d$ . The effective inductance  $L = 4L_d + 3L_3 + L_{a1} + L_{a2} + L_{b1} + L_{b2} + L_{d3} + L_{d4}$

#### SIGNIFICANCE OF STRAY INDUCTANCES

It is stating the obvious that the deleterious effects of induced voltage spikes and overshoots would be absent if the stray inductances could be eliminated, as would the slow down in current transfers between the semiconductor devices. However in this latter respect, since device switching is not instantaneous, it is advantageous, by suitable arrangement of the bridge arms, to provide stray inductance between a GTO and the feedback diode above or below, to limit the transient shoot-through current caused by overlapping GTO turn-on and diode reverse recovery times. Additional di/dt limiting reactors may be necessary.

Further points to be noted are:

- (i) The GTO - snubber capacitor loop inductance should be minimal to give a low GTO voltage spike during the anode current fall time.
- (ii) The GTO voltage overshoot depends on the effective inductance comprising the various lumped strays in the current paths which are governed by the particular devices being switched. In a number of these cases, the source inductance  $L_d$  appears multiplied by a factor of 2 or 4.
- (iii) Whenever the source current rises or falls during bridge supply or feedback, the induced  $L_d di/dt$  depresses or lifts the bridge DC rail potential, giving oscillatory overshoots across blocking devices whether they are switching or not. The bridge DC rail inductance reduces this a little across those devices remote from the input.
- (iv) Hence the source inductance is especially important and should be minimised by positioning the input capacitor(s) as close to the circuit as possible. Reducing stray inductances within the circuit assembly is usually easier than for the supply.
- (v) With the chopper, the stray connector inductance should be incorporated in the load circuit as far as possible by positioning the freewheeling diode (itself having short connectors) adjacent to the GTO and input capacitor.
- (vi) For minimising stray inductances the usual techniques of using short length, large rectangular cross section conductors, with go and return mounted close together, should be used. Capacitors and resistors should have low self inductance, and paralleling of capacitors is a useful aid.

#### CONCLUSIONS

This necessarily concise account includes simplified and approximate equations from those obtained by a deeper mathematical treatment. They show the stray inductances relating to the various switching opera-



tions, and give guidance for estimation of the over-voltages, whose accurate prediction is not possible in practice as the stray inductances cannot be calculated or measured with certainty. The reasoning can be extended to the three-phase bridge circuit.

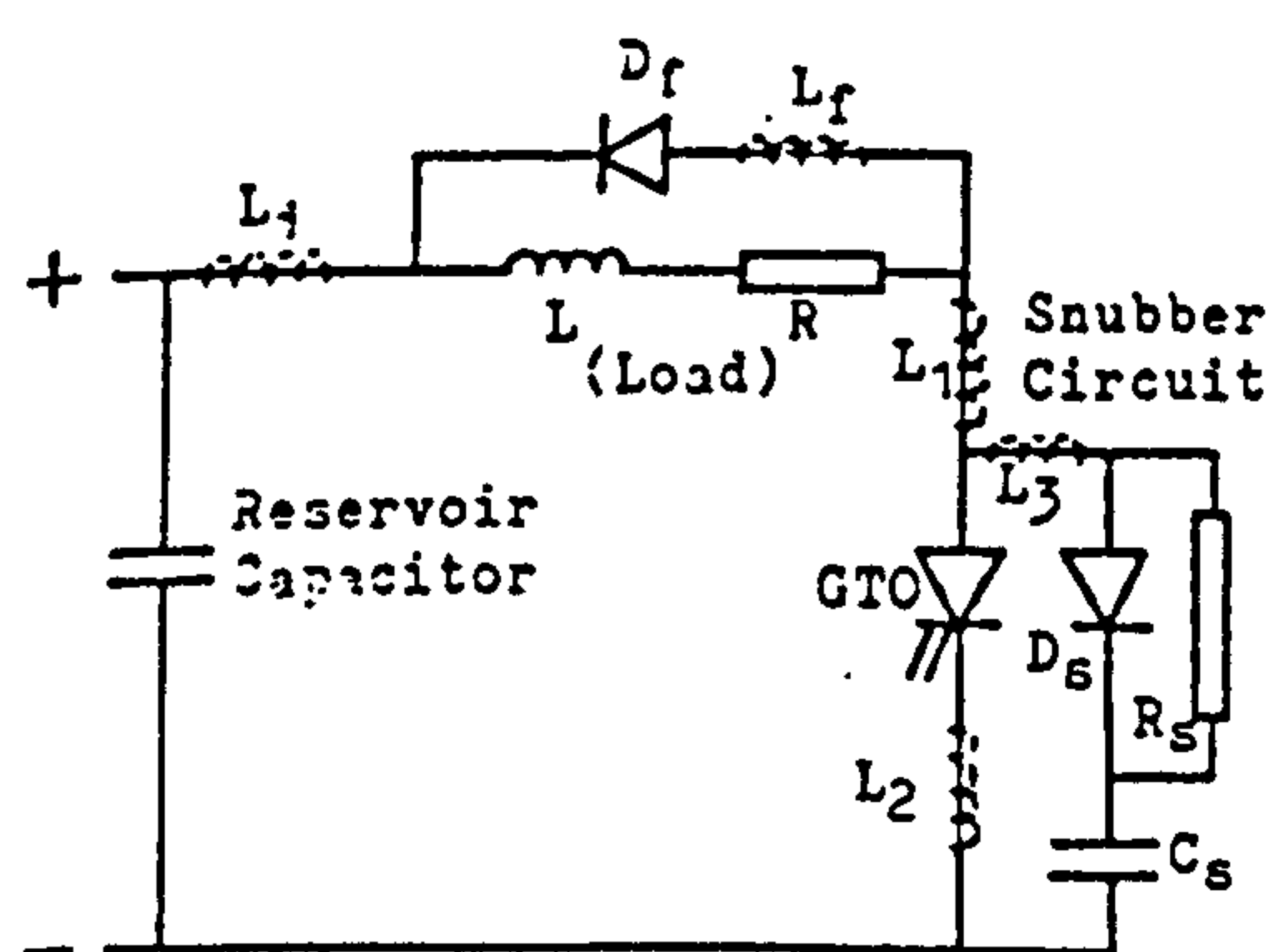
The importance of particular stray inductances has direct relevance to power circuit layout, although this cannot be considered in isolation. Other constraints apply; for example, available space and its shape, cooling measures, mechanical considerations of strength, shock and vibration withstand.

#### REFERENCE

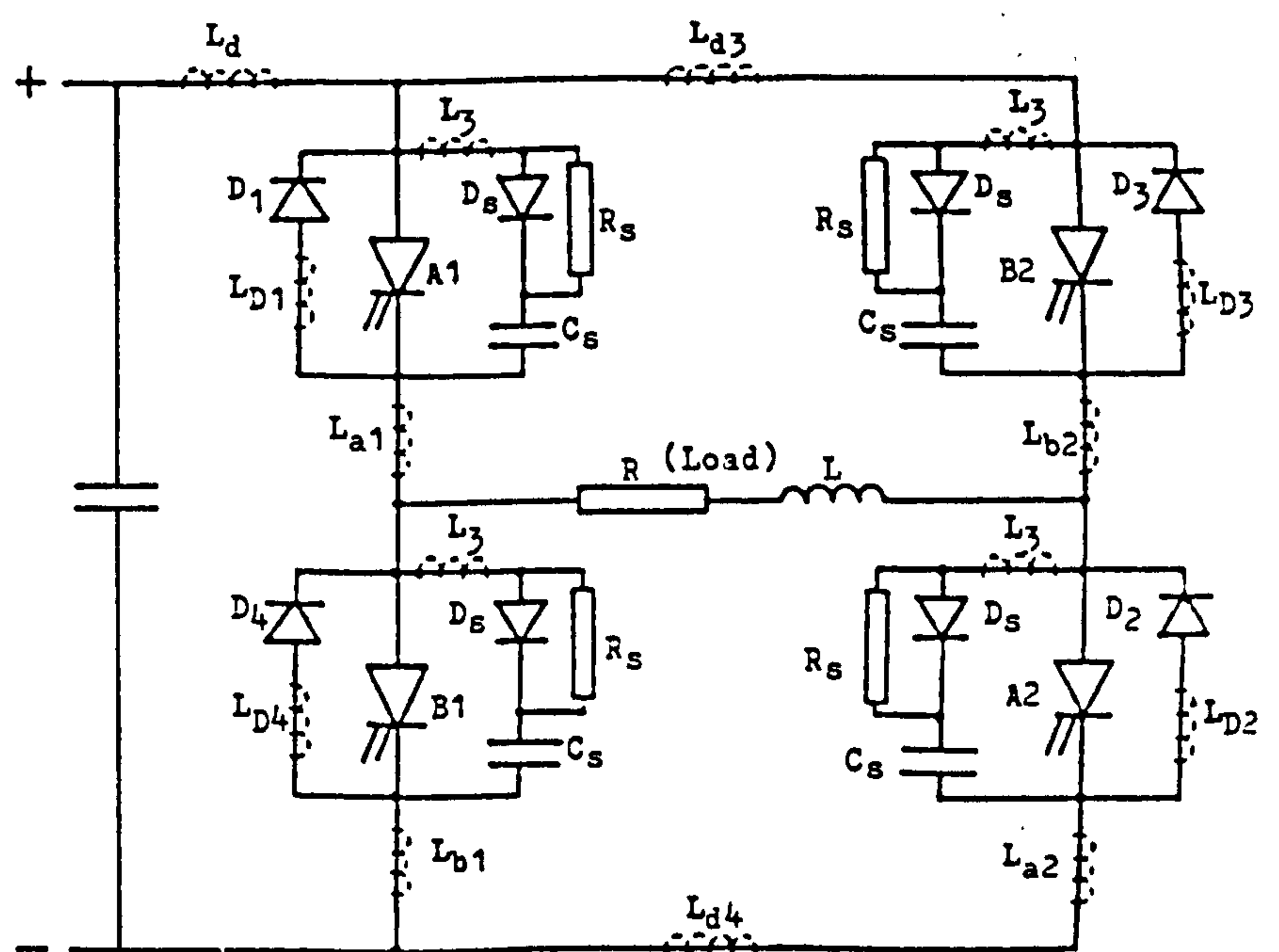
1. Gibson, H., and Ballard, J. P., 1985, "Circuit and component constraints on high current GTO turn-off"; IEE Colloquium Digest No. 1985/56.

#### ACKNOWLEDGEMENTS

Acknowledgements are made to the Department of Electrical Engineering, Loughborough University of Technology, for the provision of experimental facilities. Also to colleagues at GEC TDPL, Stafford, where these matters were discussed among many others during one author's recent sabbatical year.



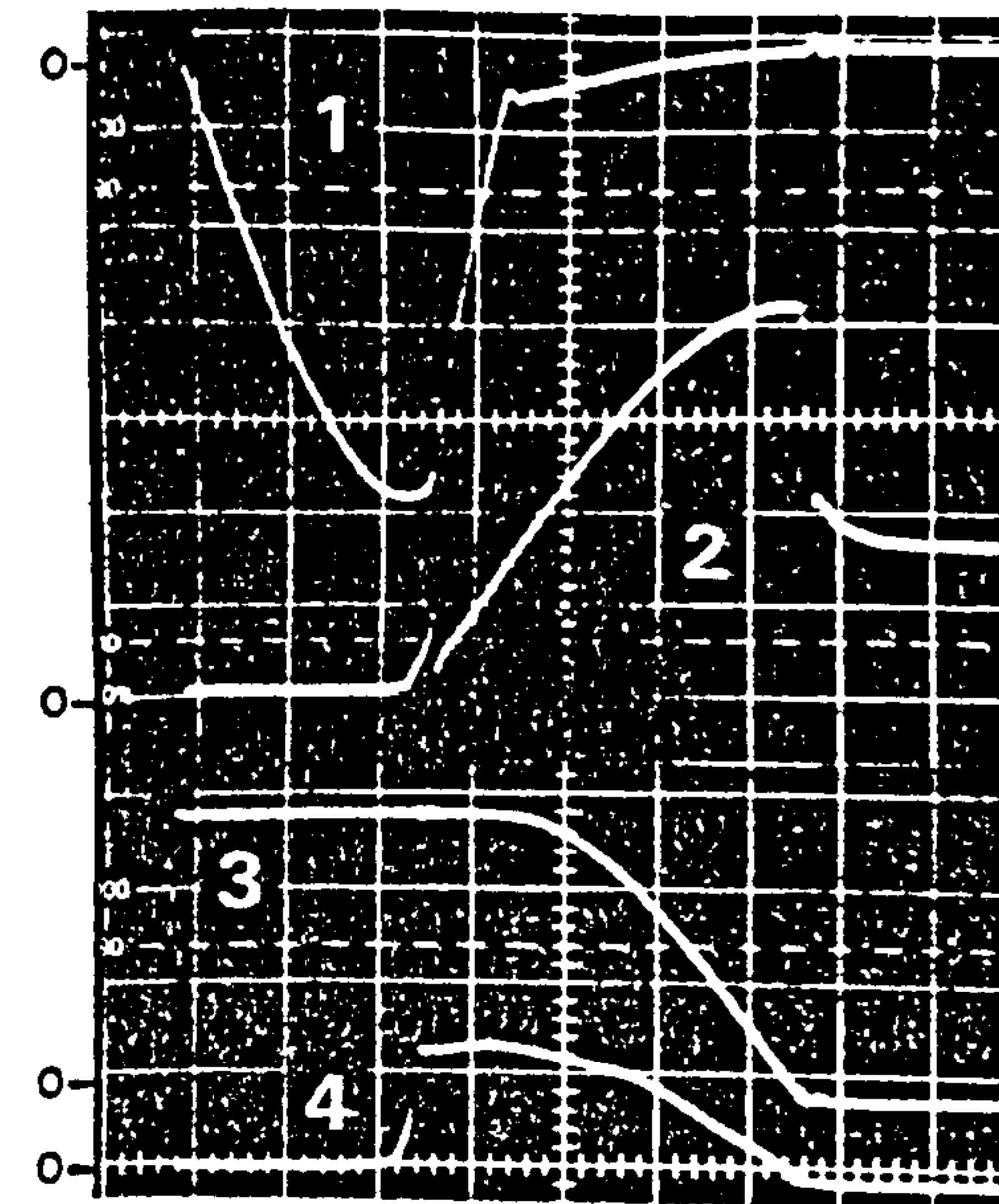
(a) Chopper with inductive load and freewheeling path



(b) Single phase inverter

Figure 1 GTO thyristor circuit with lumped stray inductances (shown as  $L$ )



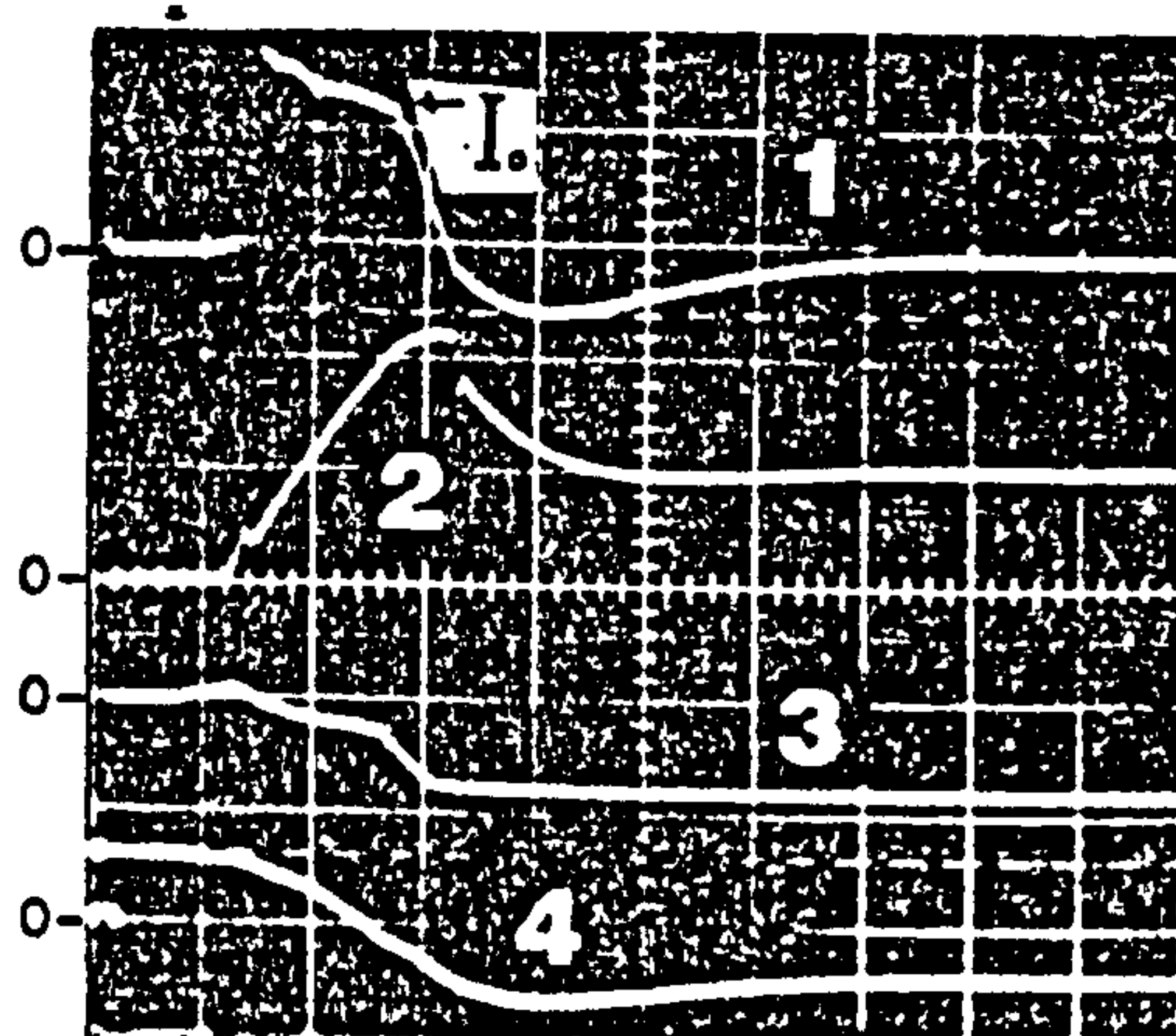


- (1) Gate current 20A/div.  
 (2) GTO voltage 200V/div.  
 (3) Load current 200A/div.  
 (4) Snubber current 400A/div.  
 Time scale 2 $\mu$ Sec/div.

Circuit conditions:

Operating frequency 100Hz  
 Load resistance 0.5 $\Omega$   
 Load inductance 65 $\mu$ H  
 Snubber resistor 8 $\Omega$   
 Snubber capacitor 4 $\mu$ F  
 Duty cycle 6%

Figure 2 Chopper waveforms during turn-off

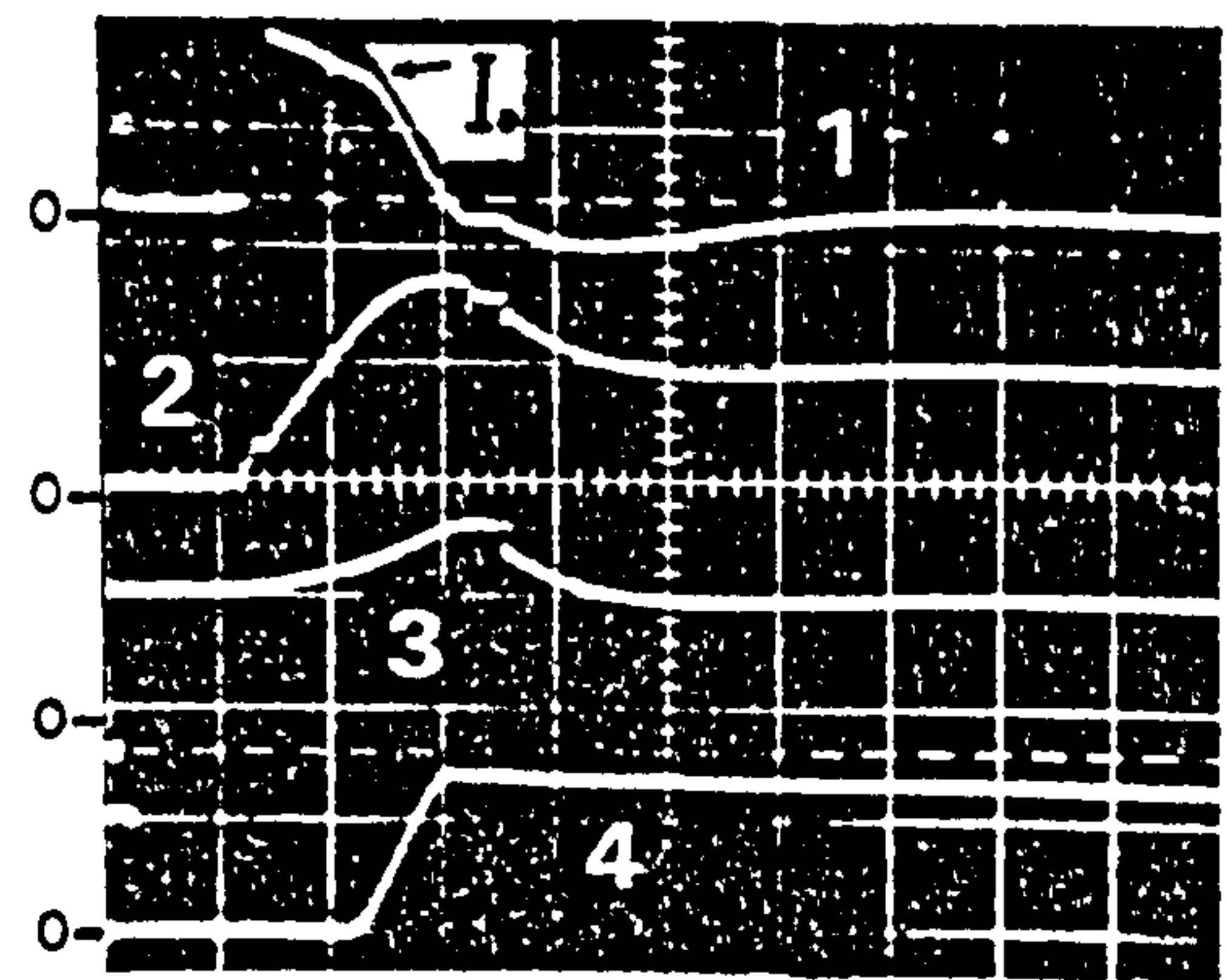


- (1) A2 snubber current 50A/div.  
 (2) A2 A-K voltage 200V/div.  
 (3) B2 branch current 100A/div.  
 (4) Supply current 200A/div.  
 Time scale 2 $\mu$ Sec/div.

Circuit conditions:

Operating frequency 100Hz  
 Load resistance 2 $\Omega$   
 Load inductance 590 $\mu$ H  
 Snubber resistor (each) 5 $\Omega$   
 Snubber capacitor (each) 0.5 $\mu$ F

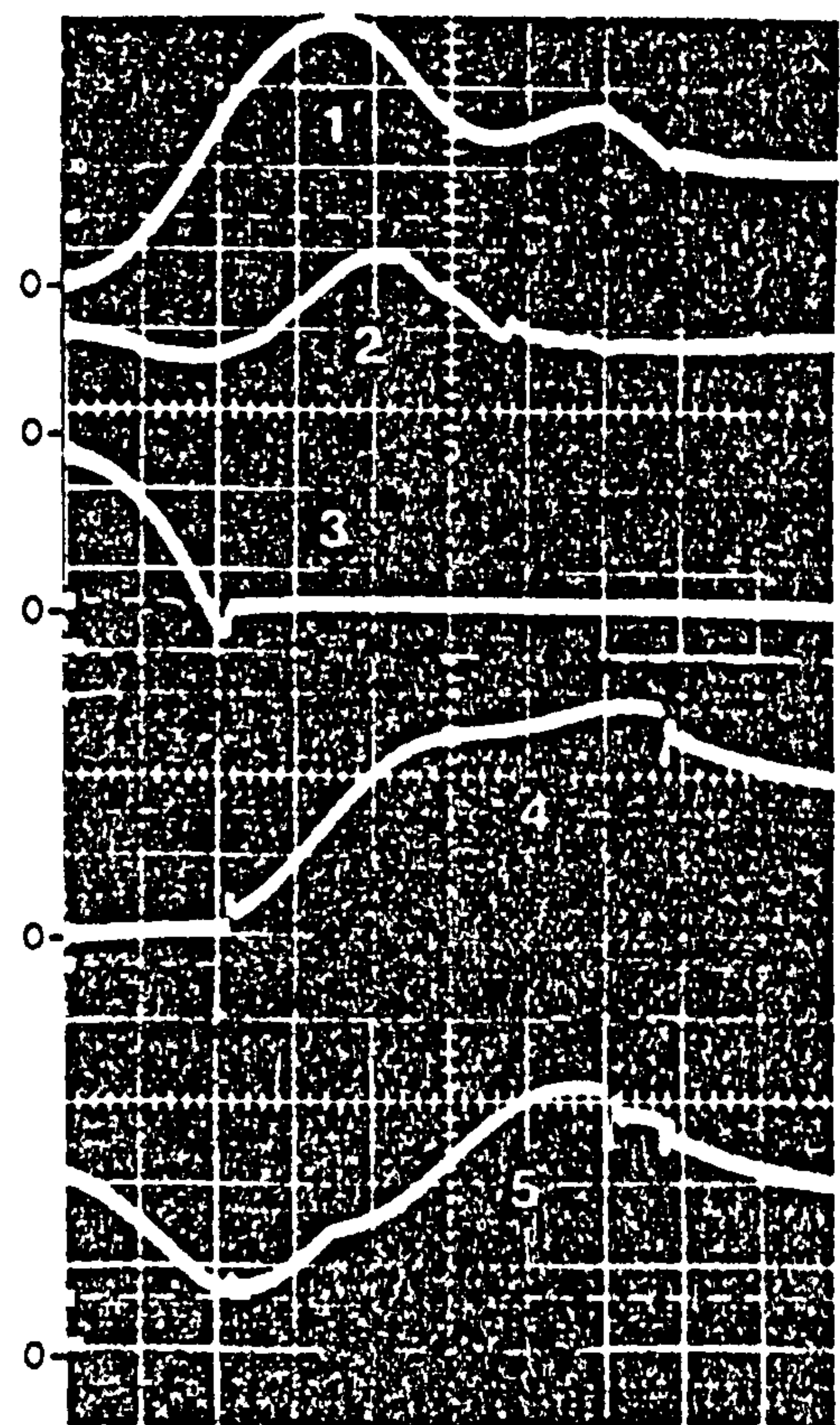
Figure 4 Bridge waveforms at A1 and A2 turn-off



- (1) A2 Snubber current 50A/div.  
 (2) A2 A-K voltage 200V/div.  
 (3) B1 A-K voltage 200V/div.  
 (4) D3 current 50A/div.  
 Time scale 2 $\mu$ Sec/div.

Circuit conditions as in figure 4

Figure 3 Bridge waveforms at A2 turn-off



- (1) A1 arm current 20A/div.  
 (2) A2 arm current 30A/div.  
 (3) D4 current 20A/div.  
 (4) B1 A-K voltage 50V/div.  
 (5) B2 A-K voltage 50V/div.  
 Time scale 1 $\mu$ Sec/div.

Circuit conditions:

Carrier frequency 600Hz  
 Modulating frequency 75Hz  
 Peak load current 50A  
 Snubber resistor 5 $\Omega$   
 Snubber capacitor 0.5 $\mu$ F  
 Load resistance 2 $\Omega$   
 Load inductance 590 $\mu$ H

Figure 5 Bridge waveforms at A1 picking up load current from freewheeling path



# INTRODUCTION

Gate turn-off thyristors (GTOs) interrupt current with such high rates of fall that voltage spikes and overshoots produced due to the stored energy in the stray inductances must be limited to acceptable levels in relation to the GTO thyristor voltage ratings. The connection of snubber circuits across the GTO(s) is essential, but even so, overvoltages caused by GTO switching, both ON and OFF, can be coupled to other blocking devices in the circuit as well as the switching ones. The dependence of such overvoltages on the distribution of these stray inductances, in DC chopper and H-bridge inverter circuits, are modelled by solving, with the aid of a digital computer, the system equations using numerical methods. The computed simulations are compared with experimental measurements. Outline analysis and experimental results have already been reported, Hall and Al-Hakim (1) and (2).

## APPROACH USED FOR CIRCUIT MODELLING

The transient analysis of most systems in engineering gives rise to differential equations. These are often of 1st order, or if they are of higher order, they may be reduced to a set of 1st order equations. To analyse the transient performance of an electrical network, methods such as the Laplace transform may be useful, but this becomes more complex as the number of branches and energy storage elements in a circuit topology increases. The employment of numerical methods with a digital computer then becomes essential.

The set of the differential equations associated with the network can be written as  $\frac{dX}{dt} = AX + Bx(t)$ , and the fourth-order Runge Kutta method is used here to solve these equations with given initial conditions, over a period of time (i.e. over a number of steps). This provides a high accuracy with an acceptable amount of computational effort. The algorithm is:

$$Y_{n+1} = Y_n + \frac{1}{6} (K_1 + 2K_2 + 2K_3 + K_4)$$

where

$$\begin{aligned} K_1 &= hf(X_n, Y_n) \\ K_2 &= hf(X_n + h/2, Y_n + K_1/2) \\ K_3 &= hf(X_n + h/2, Y_n + K_2/2) \\ K_4 &= hf(X_n + h, Y_n + K_3) \end{aligned}$$

and h is the step size.

The following simplifying assumptions are made:

- The switching device itself is taken as a non-ideal switch but having the terminal characteristics representing the GTO thyristor in the circuit;
- The 'snap-off' of diode reverse recovery

current is instantaneous.

- Mutual inductive coupling effects are neglected.

## MODELLING OF THE DC CHOPPER

Fig.1(a) shows the circuit with lumped stray inductances.

The GTO turn-off process is divided into five time intervals. Fig.2(a) and (b) shows these intervals and the waveform effects.

### Interval $t_1$

This is the GTO anode current fall time, during which the load current is rapidly diverted from the GTO into its parallel snubber. The anode current fall with time t is represented empirically by:

$$i_a = I_A (1 - \frac{t^2}{T_0^2}) \quad (1)$$

$$T_0 = t_f / \sqrt{1 - I_T / I_A} \quad (2) \quad \text{Ohashi (3)}$$

$$i_s = I_A - i_a \quad (3)$$

where  $I_A$  = anode current to be interrupted;  
 $I_T$  = peak tail current, approximately 10-20% of  $I_A$ .

$i_a$  = instantaneous anode current;  
 $i_s$  = instantaneous snubber current;  
 $t_f$  = anode current fall time.

A possibly dangerous voltage spike is induced across GTO by the high rate of rise of current in the stray GTO-snubber loop inductance ( $L_2 + L_3$  in Fig. 1(a)).

### Interval $t_2$

This is the time taken for the snubber capacitor voltage to rise almost linearly from the accumulated value at the end of the spike to just above the supply voltage  $E_d$ , the equivalent circuit being as Fig. 1(b). The system equations are:

$$\begin{bmatrix} Di_s \\ Di_t \\ DV_{cs} \end{bmatrix} = \begin{bmatrix} -R/L_4 & -R/L_4 & -1/L_4 \\ 0 & 0 & 0 \\ 1/C_s & 0 & 0 \end{bmatrix} \begin{bmatrix} i_s \\ i_t \\ V_{cs} \end{bmatrix} + \begin{bmatrix} E_d t_t + 0.2 I_A L_5 \\ \frac{t_t L_4}{-0.2 I_A / t_t} \\ 0 \end{bmatrix}$$

where  $i_t$  is the instantaneous tail current (assumed to decay linearly),  $t_t$  is the tail current decay time ( $= t_c + t_o/s$ , Fig.2(b)),  $t_c$  is the near constant current charging time,  $t_o/s$  is the oscillatory overshoot time  $= \pi \sqrt{LC_s}/2$ , D is the operator d/dt.

$$L = L_d + L_{df} + L_1 + L_3, \quad L_4 = L_d + L_2 + L_1 + L_3, \quad L_5 = L_d + L_2 + L_1.$$

### Interval $t_3$

The equivalent circuit is shown in Fig.1(c). The freewheeling diode  $D_f$  commences conduction, taking over the load current flow from the snubber circuit, this being completed at the end of the interval. The capacitor voltage overshoots the supply voltage due to the



### Transients at turn-off of Both Conducting GTOs

When switching off A1 and A2 together, the bridge operates symmetrically and the usual GTO voltage spikes and oscillatory overshoots occur.

The load current divides between the upper and lower branches at the nodes at both sides of the bridge instead of one. There is no independent blocking GTO to experience a cross-coupled voltage spike as above.

A practical feature likely to occur is some turn-off time difference between the two GTOs being switched. This can result from GTO turn-off time differences and/or timing inaccuracies of the gate drive applied (Fukui, Amano and Mlyu, 4). The waveforms of Fig. 5 apply to such a situation with A2 turning off  $1.2\mu s$  before A1. The result is that conditions of a single GTO turning off occur for this short interval before those of the two GTO turn-off, giving some small asymmetry transient waveforms. Fig. 5 shows relevant waveforms. The commencement of B1 snubber capacitor overcharging through A1 after A2 has turned off (at the commencement of its tail current) is evident. This results in A1 having to turn off increased current which could be dangerous if it is operating near its turn-off current limit. Once A1 has turned off (start of its tail), B1 snubber capacitor current falls and reverses as the capacitor discharges through the snubber diode then its parallel resistor. However, since this capacitor originally blocked voltage  $E_d$ , but finally must block voltage  $E_d/2$  with both A1 and B1 off, its discharge current builds up for a longer interval to effect this.

### Transients at single GTO turn-on from freewheeling

Consider, for a change, A2 being permanently on with A1 switched alternately on and off. With A1 off, load current freewheels through A2 and D4. A1 picks up the current from D4 when switched on. The A1 snubber capacitor, previously charged to  $E_d$ , discharges locally through  $R_s$  and A1. B1 snubber capacitor must be charged from zero to  $E_d$ , which it does oscillatorily through  $L_d$  and A1 which, however, depresses the bridge DC rail voltage. There is thus a coupled transient across blocking GTO B2 whose snubber capacitor discharges oscillatorily but must then recharge with an opposite half cycle giving voltage overshoot, the DC rail voltage then being lifted. Figs. 6 (a) and (b) show the voltages across B1 and B2 which demonstrate this. B2 snubber diode reverse recovery occurs before that of B1, GTO B1 exerting a hold-up effect on B2 voltage until B1 snubber diode reverse recovery, after which both potentials subside to  $E_d$ .

An important feature is diode D4 reverse recovery, during which a temporary shoot-through condition occurs across the DC rails. Inductances  $L_d$ ,  $L_{a1}$  and  $L_{b1}$  exert a limiting influence on the current rise, and frequently the  $L_a$  and  $L_b$  inductances are enhanced by added inductors, usually with their own freewheeling diodes.

### Transients at double GTO turn-on from feedback

Turn-on of previously conducting GTOs. Letting GTOs A1 and A2 turn on identically, they

will pick up current from feedback diodes D4 and D3 respectively. Operation is symmetrical in the bridge, but the above shoot-through and capacitor overcharge features are present. B1 and B2 snubber capacitors charge from zero voltage, overshooting  $E_d$  due to the summed stray inductances in their current paths. Their voltages then decay to  $E_d$  by discharge through the connected resistor  $R_s$ . Slight differences of turn-on time do not give rise to possibly dangerous conditions.

Turn-on of the alternative GTO diagonal pair. Following A1 and A2 conduction, and subsequent feedback through diodes D3 and D4, when GTOs B1 and B2 are turned on they take over conduction from their antiparallel diodes D3 and D4 following the load current zero crossing. There is no change of voltage distribution across the snubber capacitors and no transients occur.

### COMPARISON BETWEEN COMPUTED AND OBSERVED WAVEFORMS

Generally, the computed and observed waveforms compare very well. The assumption of snubber diode reverse recovery snap off gives rise to small differences, this being particularly demonstrated in Fig. 2 where the computed voltage undershoot did not occur experimentally. Fast recovery diodes were used. Only a few relevant sample waveforms can be presented.

### CONCLUSIONS

The analysis satisfactorily models the circuit behaviour under transient switching conditions when representative GTO thyristor and diode terminal characteristics, and stray path inductances are used. The device characteristics are somewhat approximated, for example by using a linear fall of GTO current and instantaneous snap-off of diode reverse recovery current. It was not intended to model the GTO by active and passive components, such as by using SPICE software. A separate small-scale exercise in the respect did not give very satisfactory results.

The important practical features demonstrated are:

- (i) Stray path (including component) inductances should be minimised, especially that of the source;  
For the H-bridge,
- (ii) When turning off two diagonal GTOs together, any difference of turn-off time results in the slower device having to turn off increased current which can be potentially dangerous;
- (iii) Under certain switching conditions, overvoltages and snubber diode reverse recovery transients can be coupled across the bridge and felt across other blocking devices.

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stored inductive energy. The system matrix is

$$\begin{bmatrix} Di_s \\ Di_t \\ Di_f \\ DV_{Cs} \end{bmatrix} = \begin{bmatrix} -RL_{df}/L_1^2 & -RL_{df}/L_2^2 & -RL_{df}/L_3^2 & -L_6/L_2^2 \\ 0 & 0 & 0 & 0 \\ -RL_7/L_2^2 & -RL_7/L_3^2 & -RL_7/L_4^2 & -L_1/L_2^2 \\ 1/C_s & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_s \\ i_t \\ i_f \\ v_{Cs} \end{bmatrix} + \begin{bmatrix} E_d t_c L_6 - 0.2 I_A L_2^2 \\ -0.2 I_A / t_c \\ -E_d t_c L_1 + 0.2 I_A L_4^2 \\ 0 \end{bmatrix}$$

where  $i_f$  = instantaneous freewheeling current  
 $L_6 = L_1 + L_{df}$ ,  $L_7 = L_d + L_1 + L_3$ ,  $L_8 = (L_4 L_6 - L_1^2)$ ,  $L_9 = (L_2^2 - L_5 L_6)$ ,  $L_{10} = L_1 L_3$ .

#### Interval $t_4$

The small GTO tail current and capacitor overshoot current having fallen to zero, the snubber capacitor  $C_s$  discharges back through  $D_f$  to the supply via the snubber diode during its reverse recovery, (Fig.1d). This is represented by the equations.

$$\begin{bmatrix} Di_s \\ Di_f \\ DV_{Cs} \end{bmatrix} = \begin{bmatrix} 0 & -RL_{df}/L_{12}^2 & -L_6/L_{12}^2 \\ 0 & -RL_{11}/L_{12}^2 & -L_{df}/L_{12}^2 \\ 1/C_s & 0 & 0 \end{bmatrix} \begin{bmatrix} i_s \\ i_f \\ v_{Cs} \end{bmatrix} + \begin{bmatrix} E_d L_6 / L_{12}^2 \\ E_d L_{df} / L_{12}^2 \\ 0 \end{bmatrix}$$

where  $L_{11} = L_d + L_{df} + L_1 + L_3$ ,  $L_{12}^2 = (L_{11} L_6 - L_{df}^2)$

#### Interval $t_5$

On completion of the snubber diode reverse recovery, the capacitor discharge current diverts into the parallel resistor  $R_s$ , a sudden voltage drop appearing across the GTO.

Thereafter the voltage across the GTO falls to the supply value  $E_d$  (Fig.2b). If the reverse recovery is slow, or abrupt snap-off of reverse recovery current occurs, an 'under-shoot' may take place (Fig.2b) which is undesirable and possibly dangerous. The equivalent circuit is shown in Fig. 1(e) and the system matrix is

$$\begin{bmatrix} Di_s \\ Di_f \\ DV_{Cs} \end{bmatrix} = \begin{bmatrix} -R_s L_6 / L_{12}^2 & -RL_{df}/L_{12}^2 & -L_6/L_{12}^2 \\ -R_s L_{df} / L_{12}^2 & -RL_{11}/L_{12}^2 & -L_{df}/L_{12}^2 \\ 1/C_s & 0 & 0 \end{bmatrix} \begin{bmatrix} i_s \\ i_f \\ v_{Cs} \end{bmatrix} + \begin{bmatrix} E_d L_6 / L_{12}^2 \\ E_d L_{df} / L_{12}^2 \\ 0 \end{bmatrix}$$

#### MODELLING OF THE H-BRIDGE

The procedure for obtaining and solving the system equations for the H-bridge, Fig.3, is similar to that of the DC chopper. The bridge is far more complex with many more equations, and it is appropriate to give only a descriptive treatment here leading to computed and experimental waveforms.

#### Basic Switching Patterns

The versatile H-bridge is capable of operating in a number of ways. Neglecting the effects of the snubbers for the moment, a fundamental feature of the operation with an inductive load is that when a GTO switches off (say A2 in Fig.3), the load current diverts into the diode of the arm above or below it as appropriate (D3), these diodes being termed freewheeling or feedback diodes.

**Freewheeling.** With load current supplied from the source through say A1 and A2, by turning off one GTO (say A2), current is diverted through the freewheeling path D3 and A1, the supply current-falling to zero. The voltage across the load is zero, neglecting A1 and D3 conduction drops.

**Feedback.** If two GTOs are turned off (A1 and

A2), the inductive load current is fed back to the source via D3 and D4, the supply current therefore reversing. The polarity of the load voltage also reverses.

**Turn-on from freewheeling.** By turning on the previously conducting GTO (A2), the situation reverts to a DC source supplied load (through A1 and A2). This is appropriate for bridge operation as a DC chopper or a pulse-width modulated inverter switching within a half-cycle. There is no load voltage polarity reversal. Note that it is not allowable to switch on the complementary diagonal pair of GTOs (B1 and B2) as a DC supply short circuit would result (through A1 and B1).

**Turn-on from feedback.** Here there is the choice of switching on the previously conducting GTO pair (A1 and A2), and reverting to the original load polarity appropriate for a DC chopper or PWM inverter again, or of switching on the alternate pair (B1 and B2) to reverse the load polarity. In fact, this polarity is already reversed by the feedback action, and the GTOs will take over conduction from their antiparallel feedback diodes only when the inductive load current reverses naturally. Such operation is typical of the reversal at the end of a voltage half-cycle in either quasi-square or PWM inverters.

Such basic switching operations are greatly complicated by the effects of the stray inductances, snubbers and device imperfections.

#### Transients at Turn-off of One Conducting GTO

On turning off GTO A2, its anode current is diverted into its snubber, as in interval  $t_1$ , for the chopper, producing the same voltage spike across A2. As the A2 snubber capacitor voltage builds up, the B2 snubber capacitor (originally charged to supply voltage  $E_d$ ) discharges, the constant load current dividing between the A2 and B2 branches suitably to effect this. The rising upper branch current freewheels through A1, the supply current falls and the induced voltage across source inductance  $L_d$  lifts the bridge supply rail voltage, giving an oscillatory overcharging above  $E_d$  of B1 snubber capacitor through GTO A1. This is demonstrated by the waveforms of Fig.4.

When the A2 snubber capacitor voltage reaches  $E_d$ , D3 commences its conduction, taking over the rising branch current flow from the parallel snubber capacitor. The A2 snubber capacitor current perceptibly falls at an increased rate as its voltage overshoots  $E_d$ . Since the diversion of current into free-wheeling is now more rapid, the B1 voltage overshoot current is increased. At the peak of the A2 voltage overshoot oscillation, its snubber capacitor current reverse to discharge through its snubber diode reverse recovery, then the resistor as usual. However, a very rapid voltage fall is prevented by the overcharged B1 snubber capacitor voltage being coupled to A2 via the DC rails, A1 and D3, and 'holding-up' the A2 voltage for a short interval. B1 capacitor current naturally falls,  $L_d$  effectively isolating the source, until it reverses to discharge through its snubber diode reverse recovery. This ends the 'hold-up' interval. B1 and A2 snubber capacitors then discharge through their snubber resistors to blocking voltage  $E_d$ .

The most influencing stray inductances are those of the source and the bridge rails.



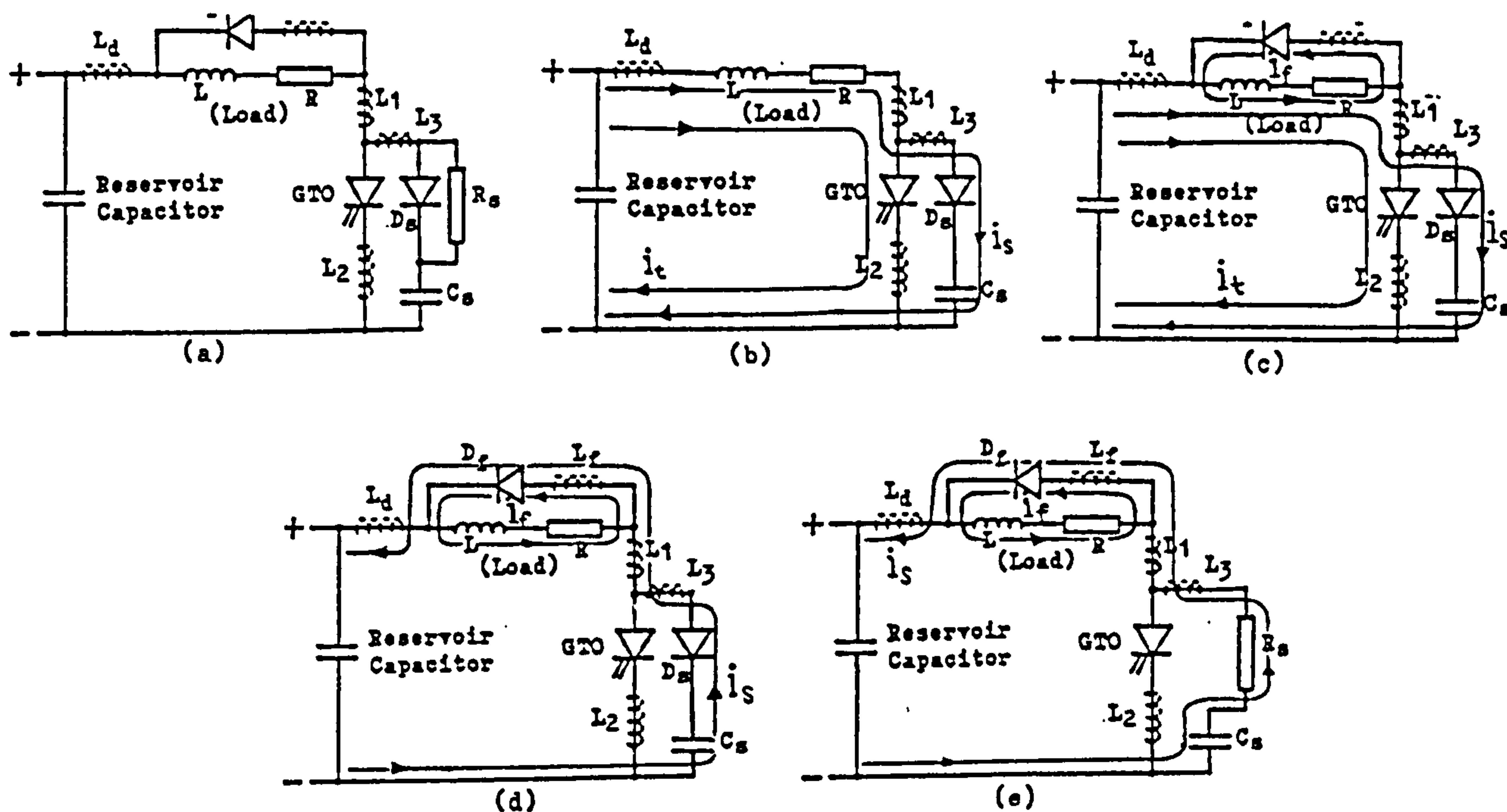


Figure 1 DC chopper circuit and equivalent circuits for GTO thyristor turn-off intervals with stray inductances shown dashed

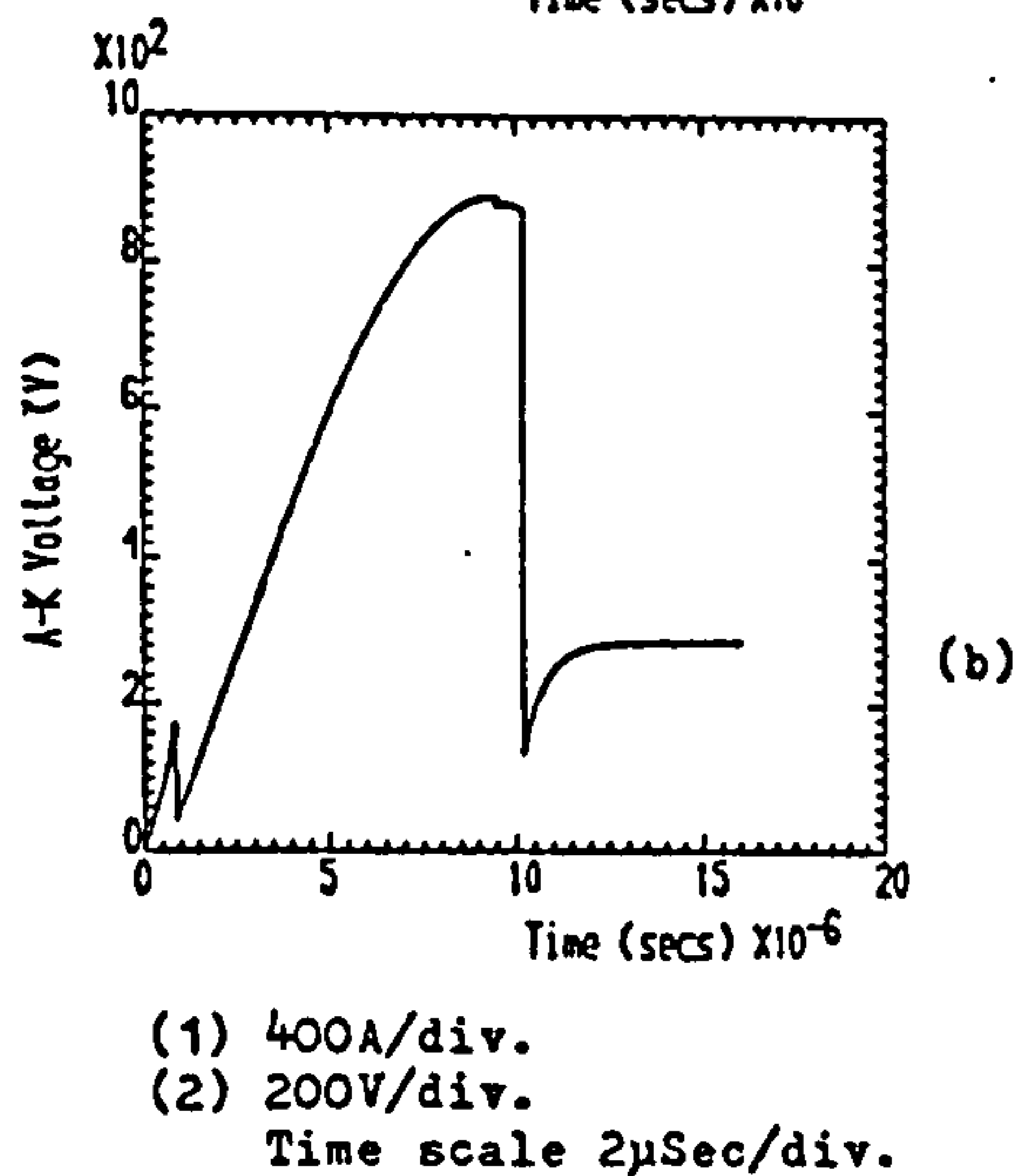
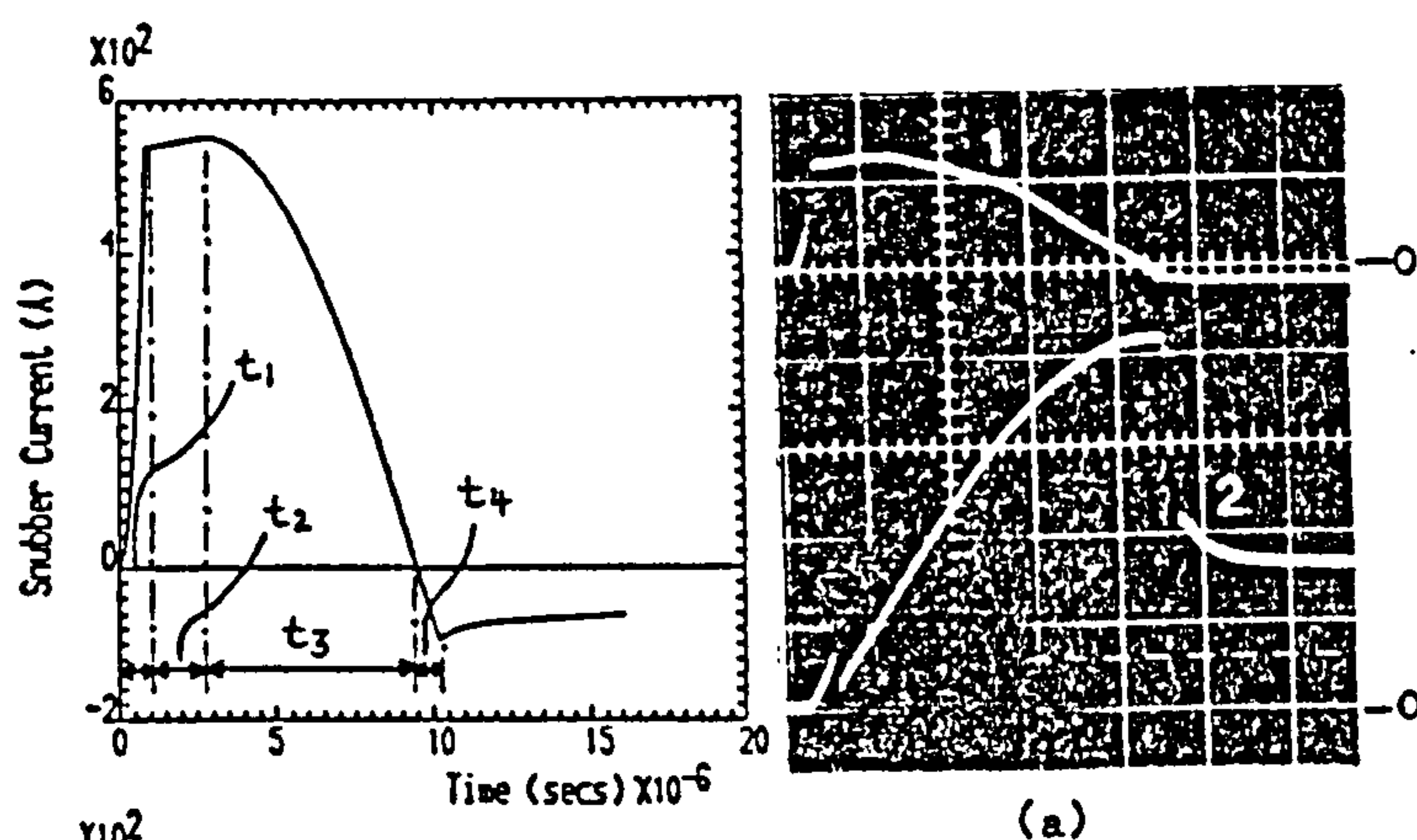


Figure 2 Computed and observed waveforms at GTO thyristor turn-off in DC chopper

Circuit conditions:	DC Chopper	H-Bridge	
		Quasi-Square	PWM
Operating frequency(Hz)	100	100	-
Carrier frequency(Hz)	-	-	600
Modulating frequency(Hz)	-	-	75
Supply voltage Ed(V)	300	200	200
Snubber resistor(Ω)	8	5	5
Snubber capacitance(μF)	4	0.5	0.5
Load resistor(Ω)	0.5	2	2
Load inductance(μH)	65	590	590

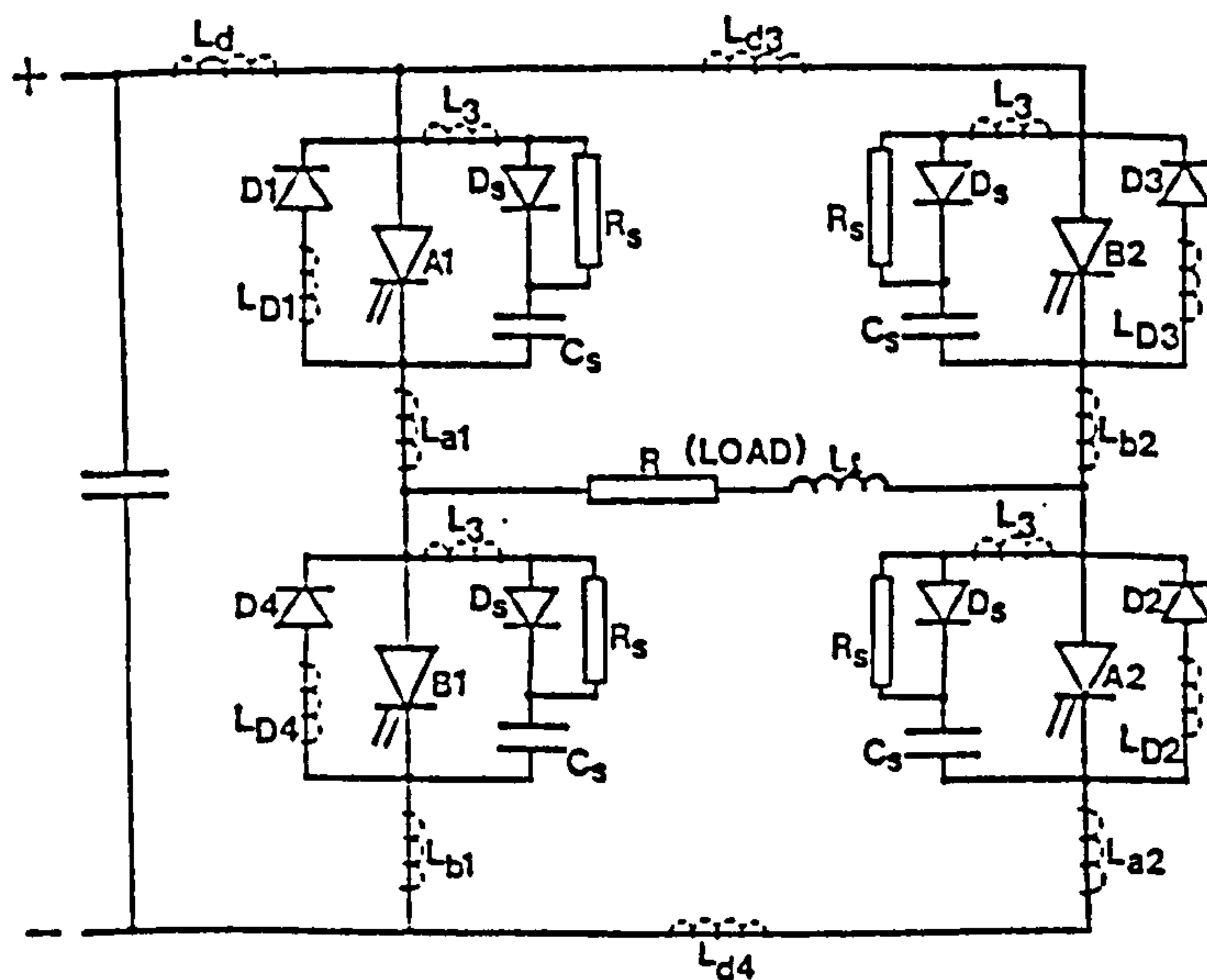
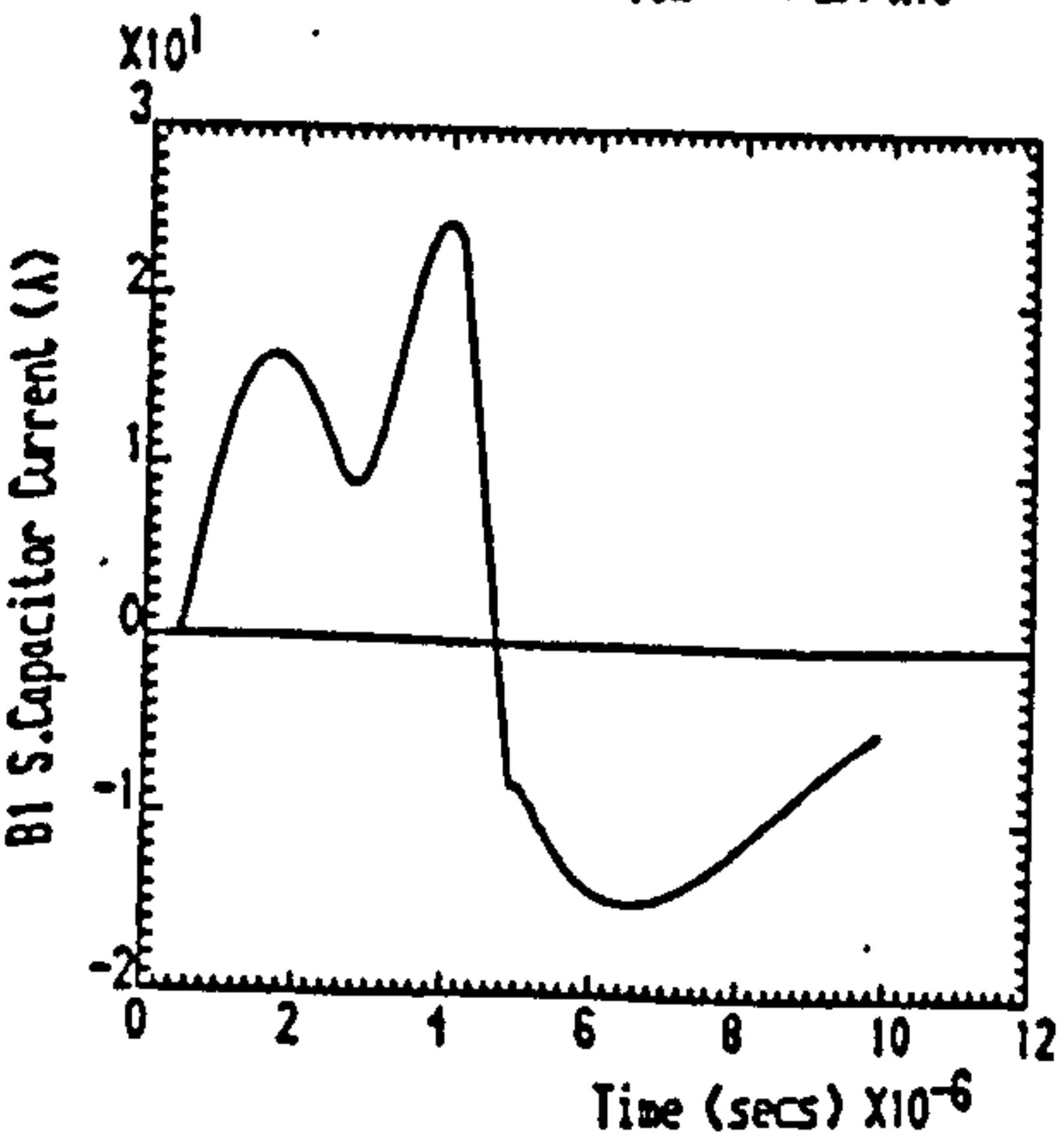
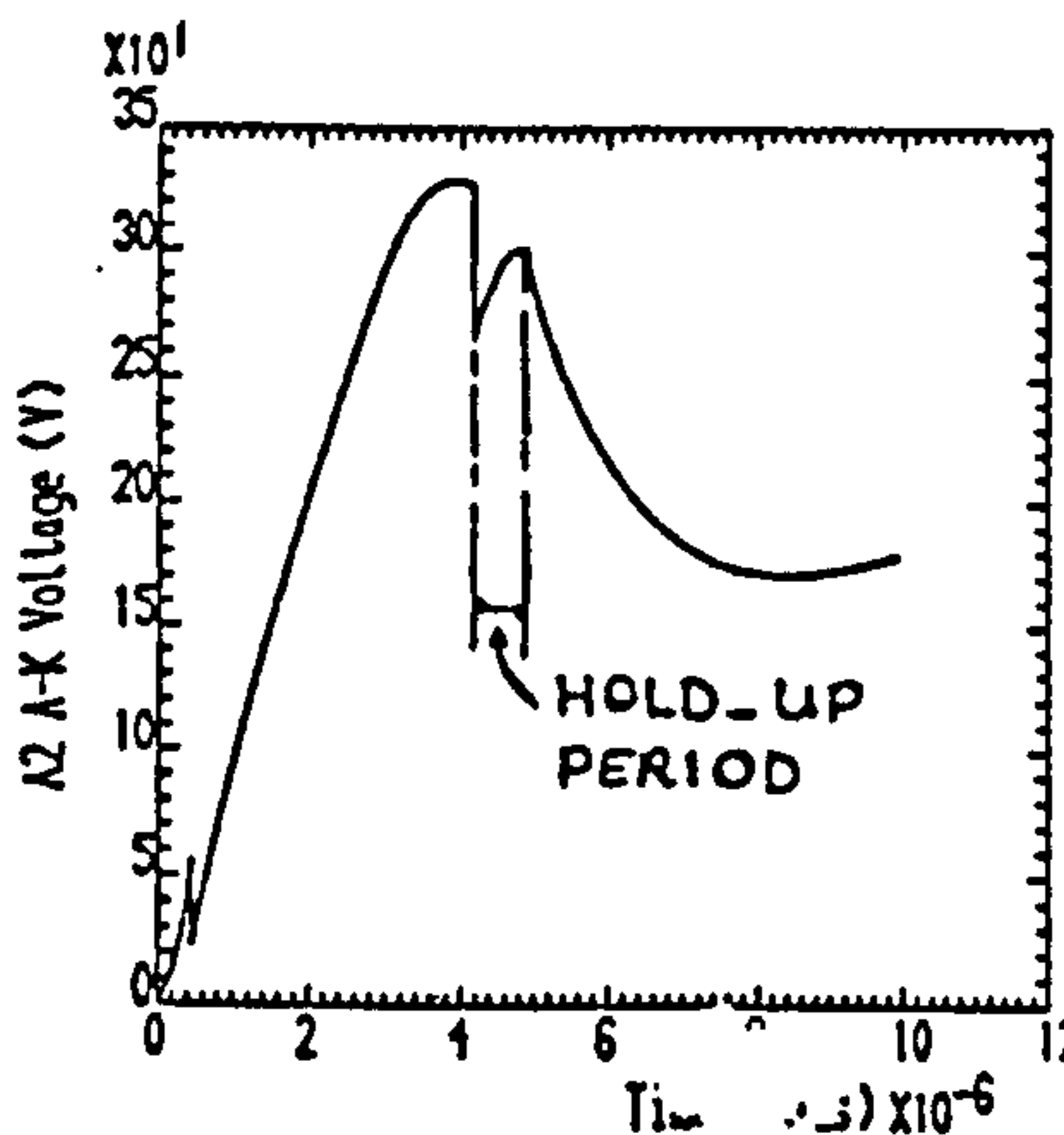
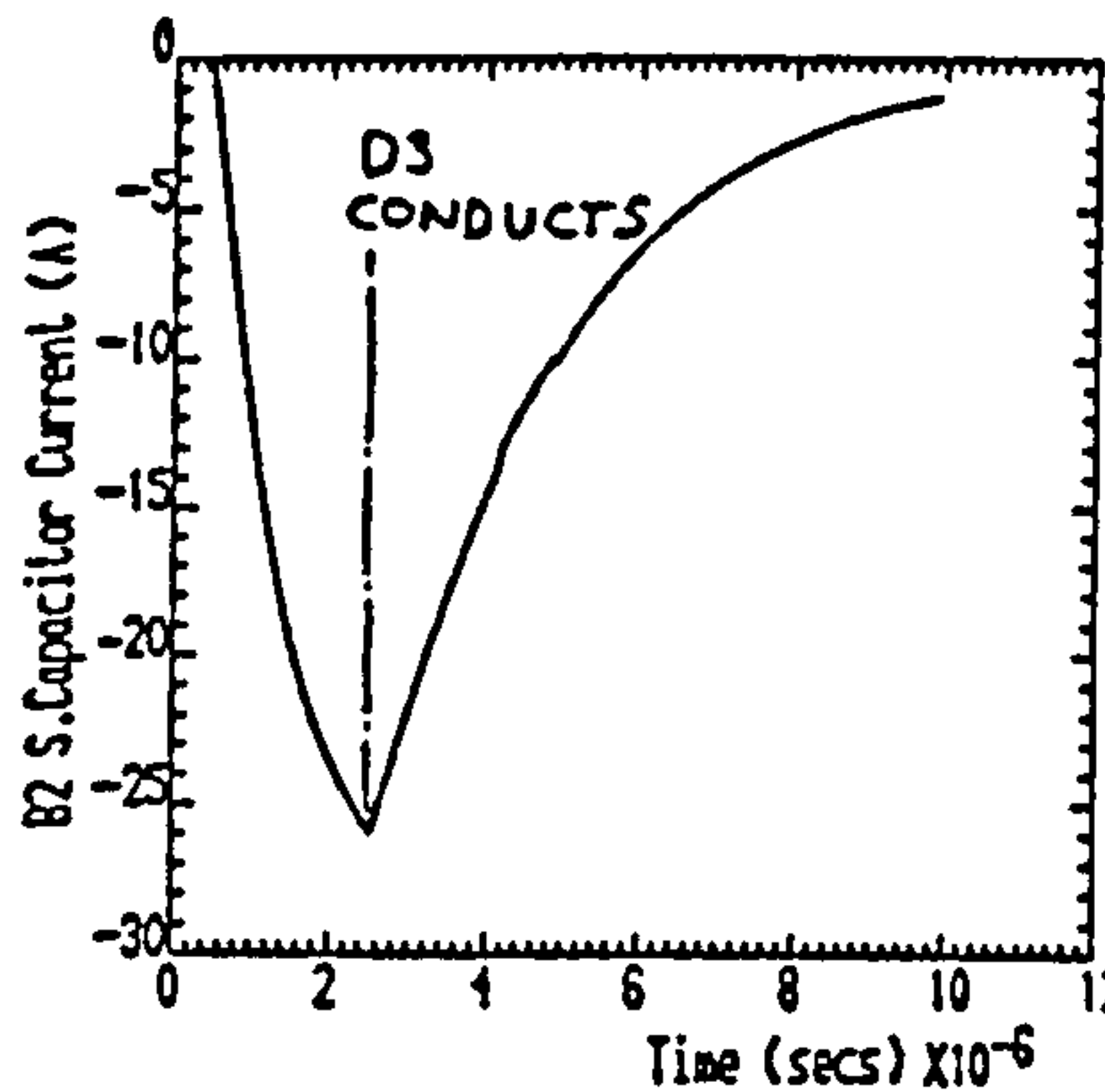
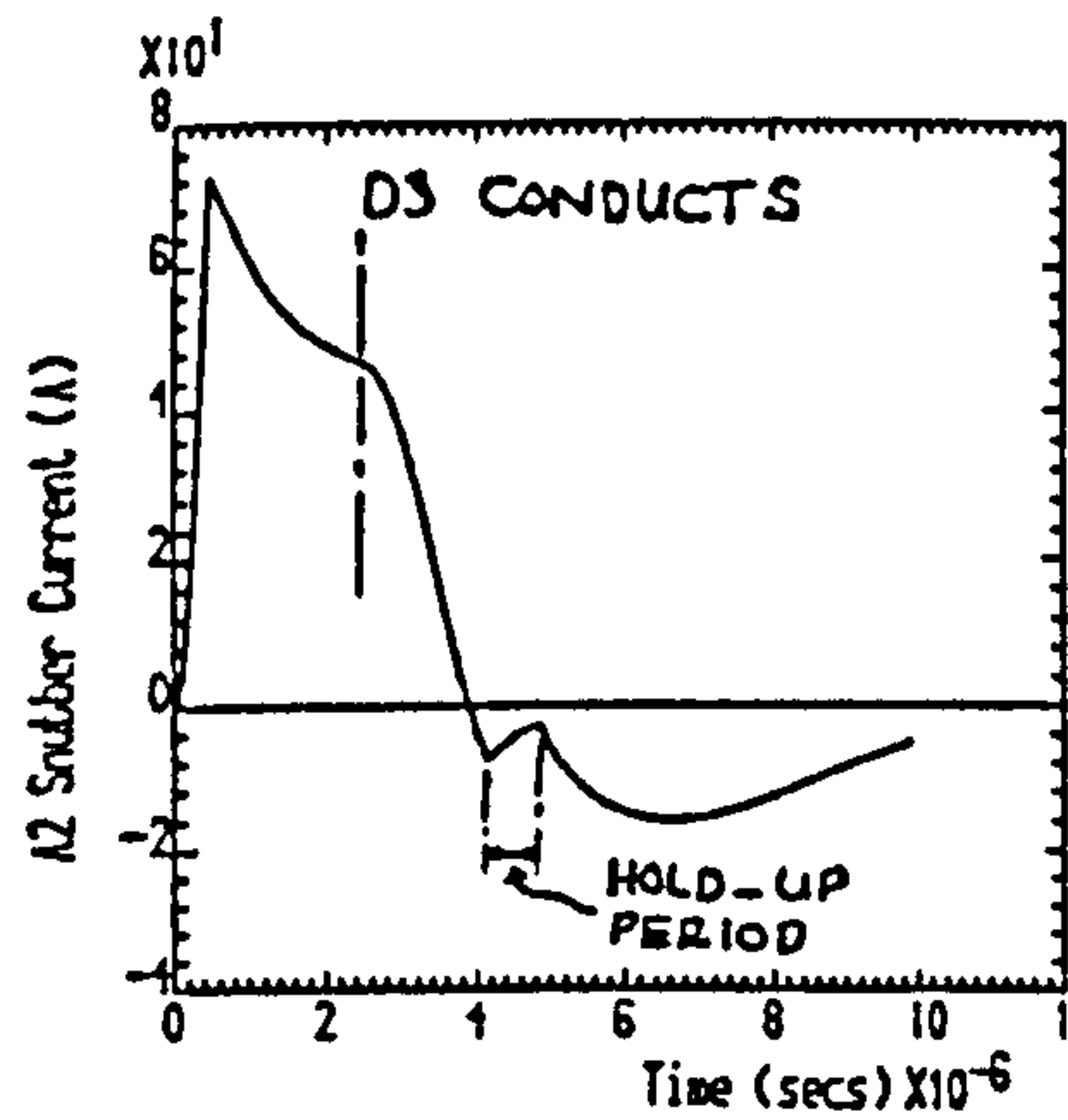


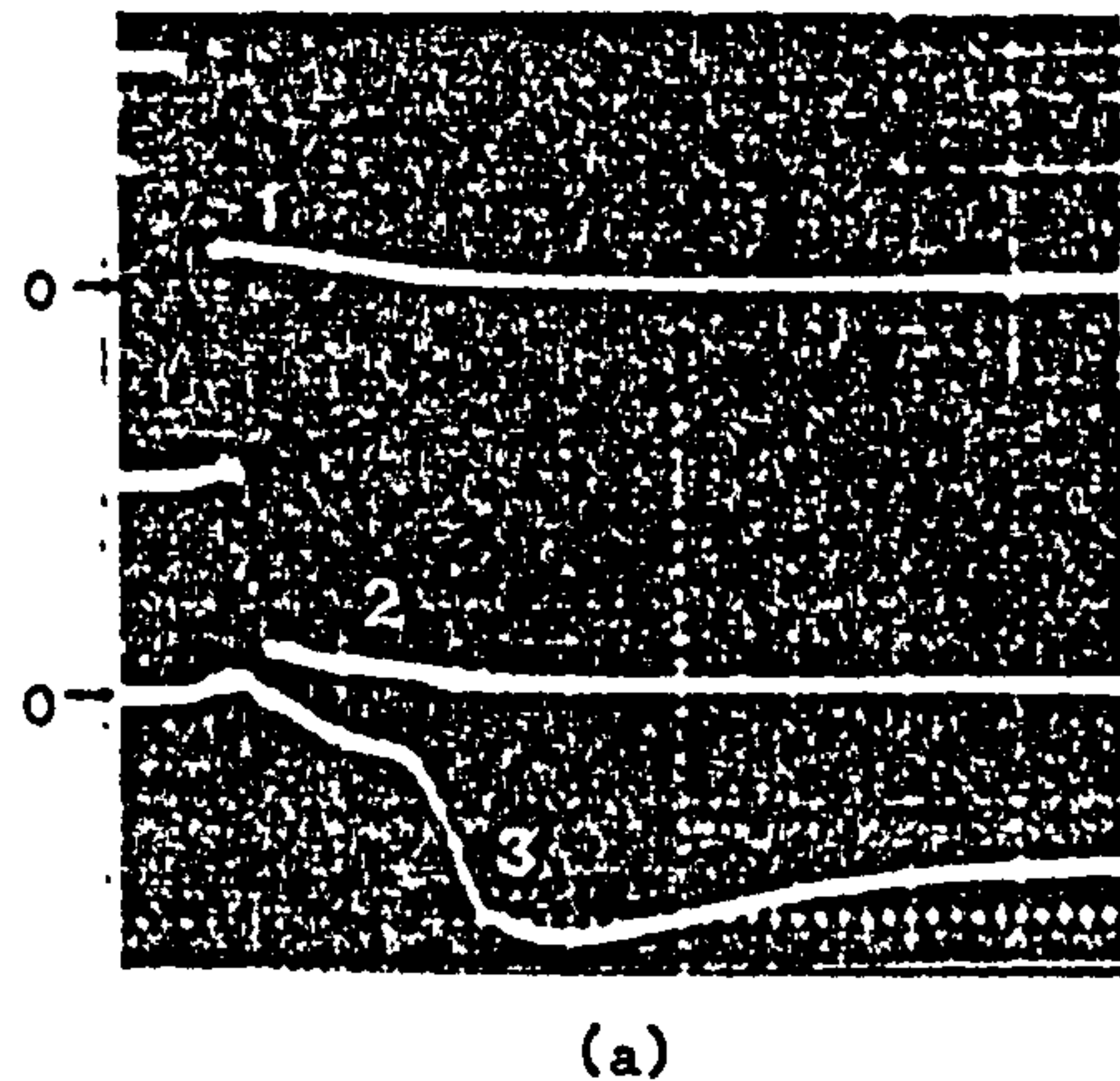
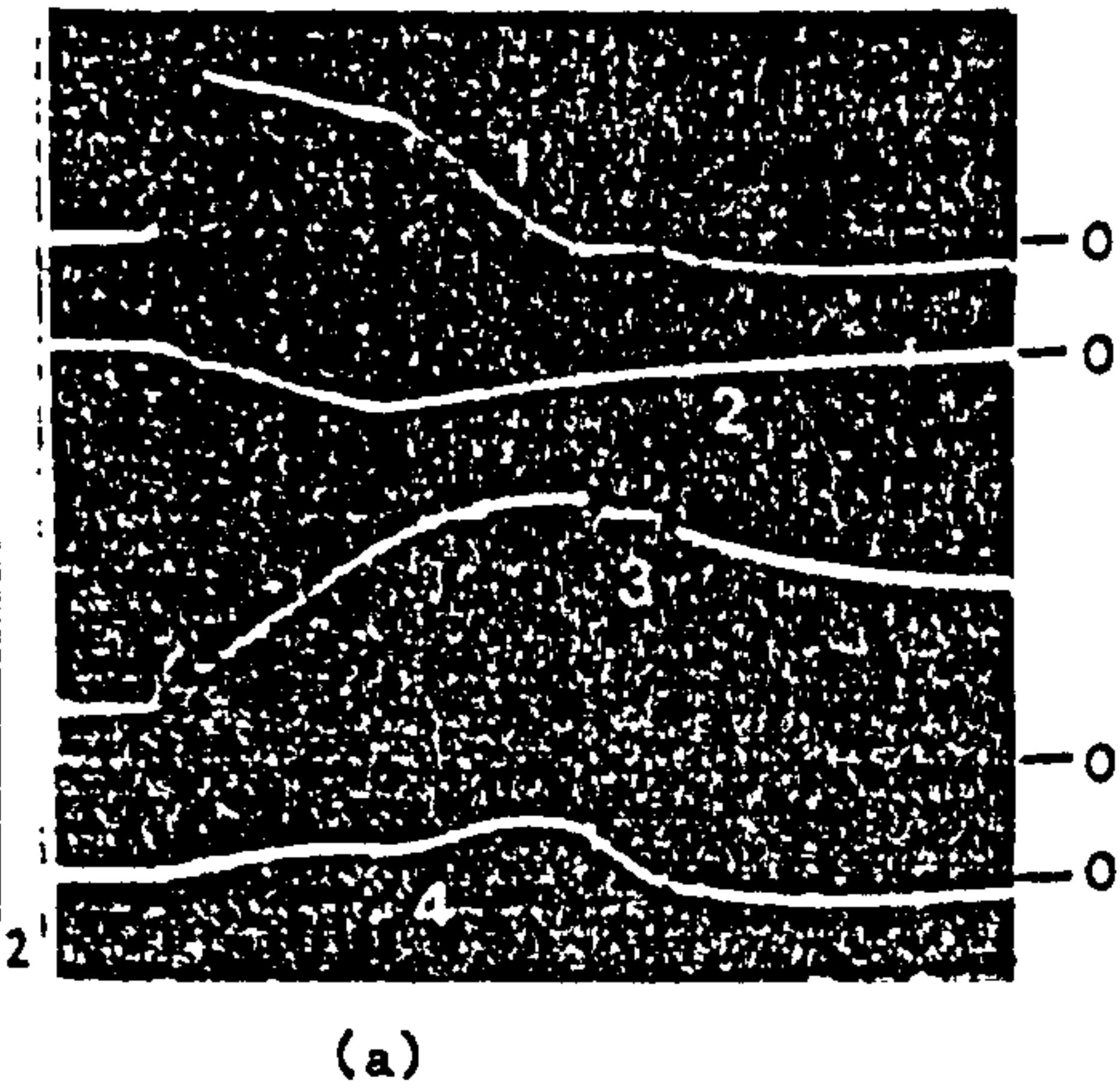
Figure 3 H-Bridge with lumped stray inductances shown dashed



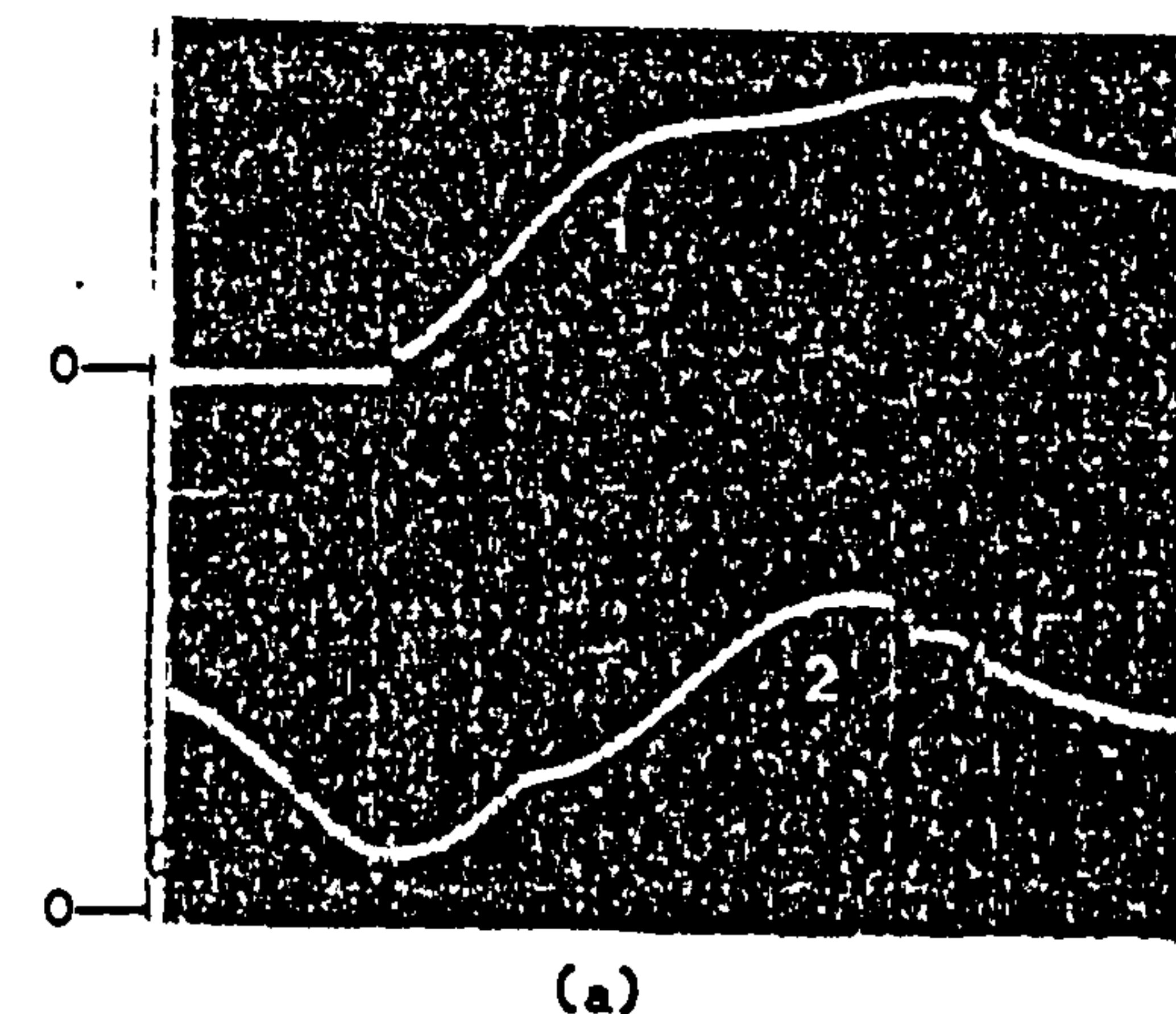


- (1) 50A/div.  
(2) 50A/div.  
(3) 200V/div.  
(4) 50A/div.  
Time scale 1μSec/div.

Figure 4 Computed and observed waveforms at GTO A2 turn-off first

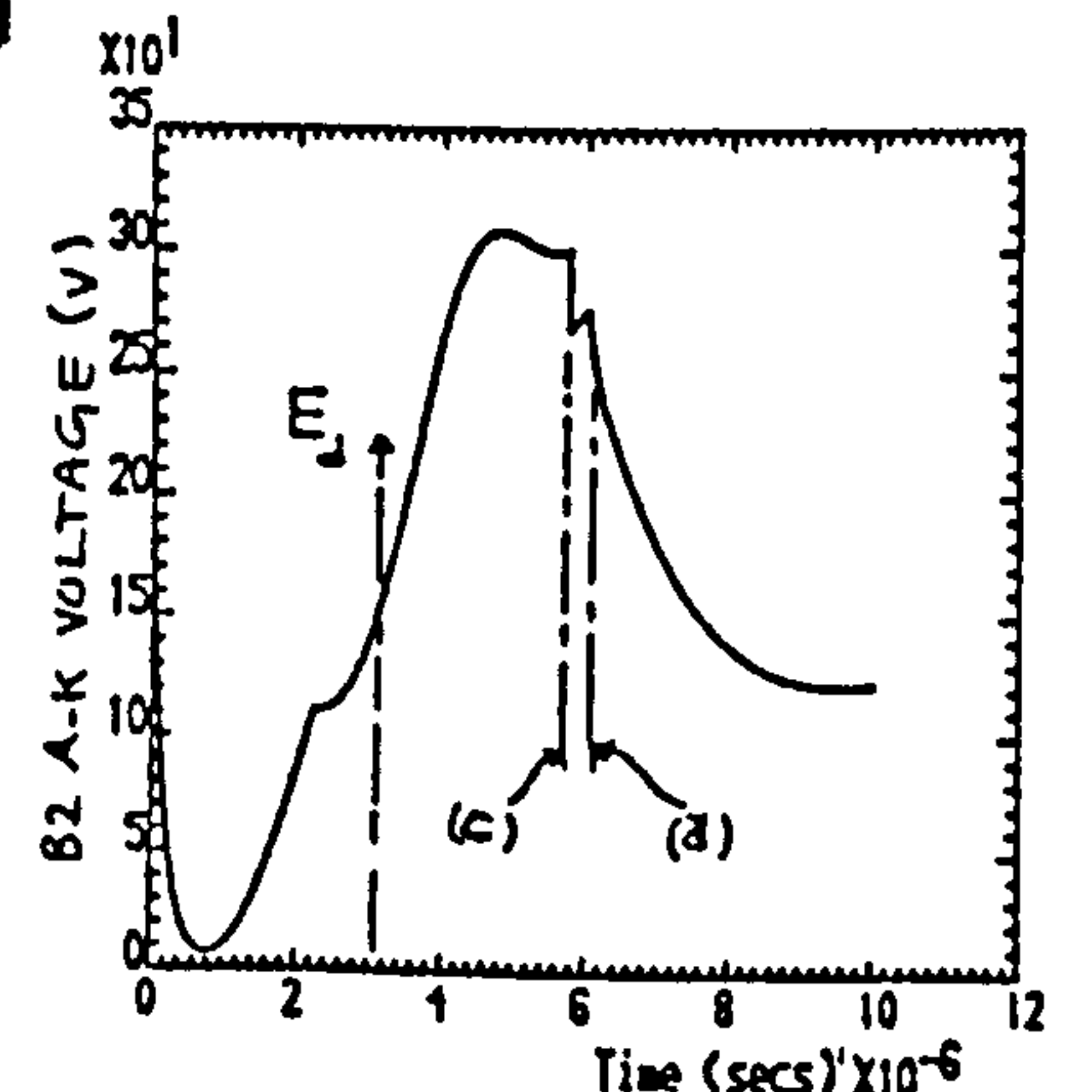
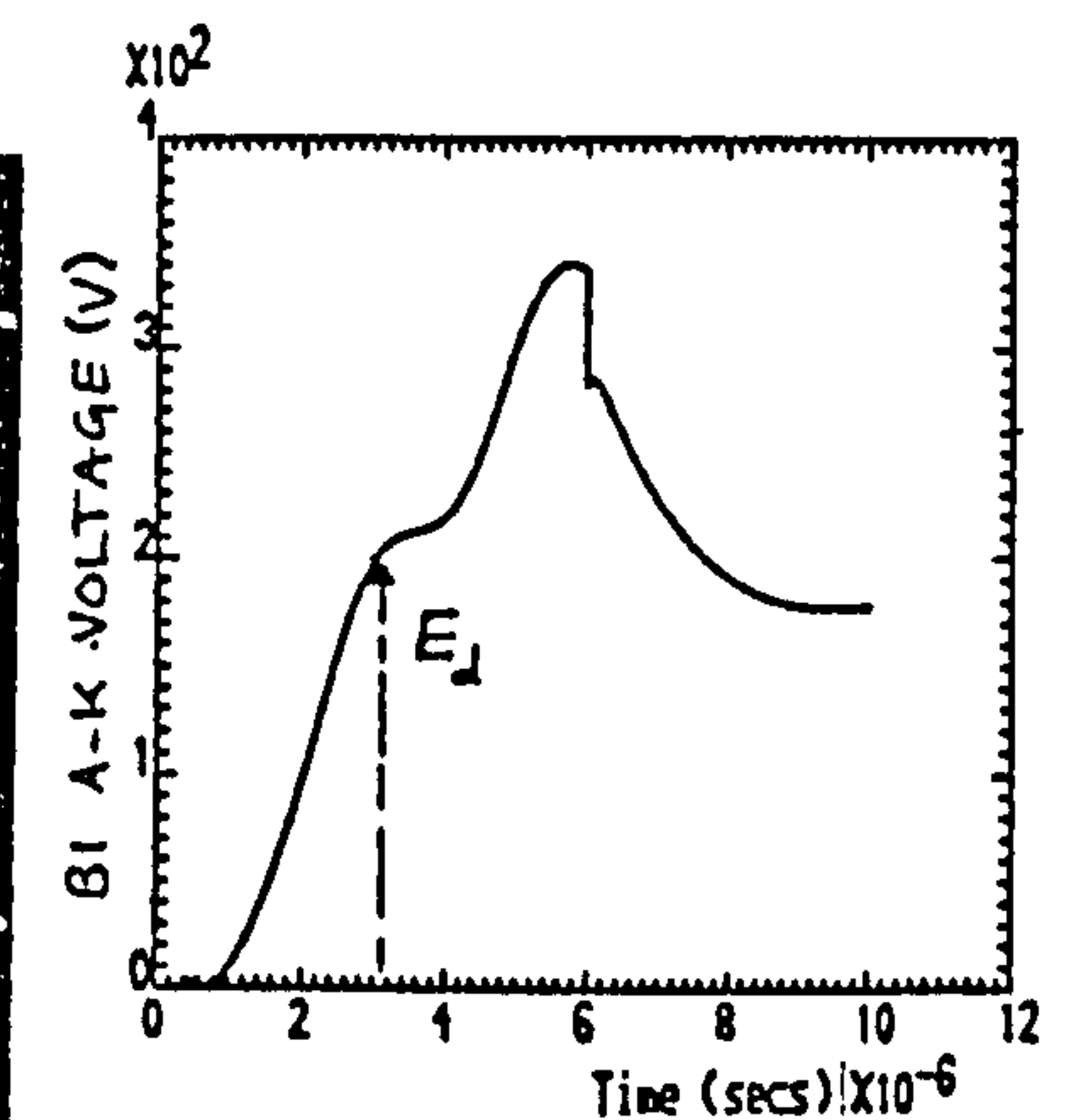
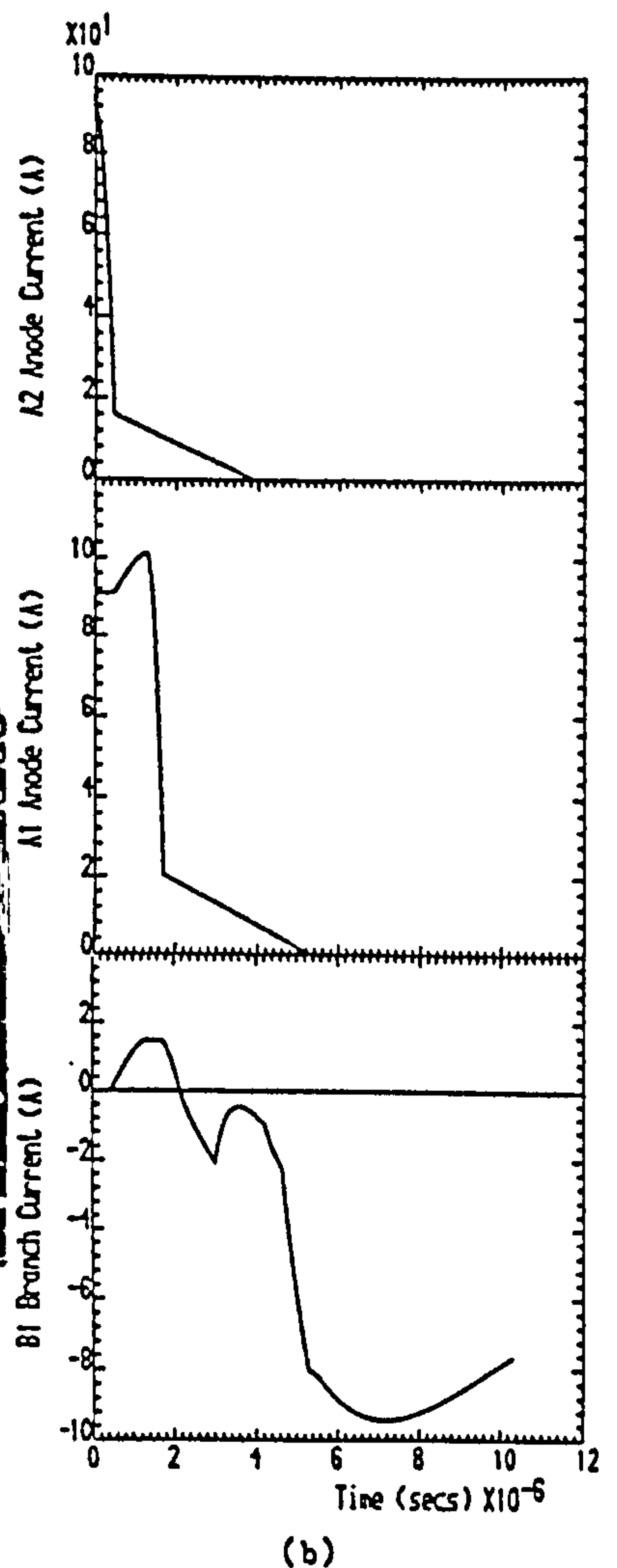


- (1) 50A/div.  
(2) 50A/div.  
(3) 50A/div.  
Time scale 2μSec/div.



- (1) 100V/div.  
(2) 100V/div.  
Time scale 1μSec/div.

Figure 6 Computed and observed waveforms at GTO A1 turn-on from freewheeling(GTO A2 conducting)



- (c) B2 DIODE r.r  
(d) B1 DIODE r.r