Microstructural and mechanical characteristics of micro-scale intermetallic compounds interconnections

Microstructural and Mechanical Characteristics of Micro-Scale Intermetallic Compounds Interconnections

By

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A Doctoral Thesis

Submitted in Partial Fulfilment of the Requirements

For the Award of

Doctor of Philosophy of Loughborough University

December 2016

LOUGHBOROUGH UNIVERSITY

WOLFSON SCHOOL OF

MECHANICAL AND MANUFACTURING ENGINEERING

Dated: December 2016

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Abstract

Following the continually increasing demand for high-density interconnection and multilayer packaging for chips, solder bump size has decreased significantly over the years, this has led to some challenges in the reliability of interconnects. This thesis presents research into the resulting effects of miniaturization on the interconnection with Sn-solder, especially focusing on the full intermetallics (IMCs) micro-joints which appear in the 3D IC stacking packaging. Thereby, systematic studies have been conducted to study the microstructural evolution and reliability issues of Cu-Sn and Cu-Sn-Ni IMCs micro-joints.

(1) Phenomenon of IMCs planar growth: The planar IMCs interlayer was asymmetric and composed of $(Cu,Ni)_6Sn_5$ mainly in Ni/Sn (2.5~5 μm)/Cu interconnect. Meanwhile, it was symmetric two-layer structure in Cu/Sn (2.5~5 μm)/Cu interconnect with the Cu_3Sn fine grains underneath Cu_6Sn_5 cobblestone-shape-like grains for each IMCs layer. Besides, it is worth noticing that the appearance of Cu-rich whiskers (the mixture of $Cu/Cu_2O/SnO_x/Cu_6Sn_5$) could potentially lead to short-circuit in the cases of ultra-fine (<10 μm pitch) interconnects for the miniaturization of electronics devices.

(2) Microstructural evolution process of Cu-Sn IMCs micro-joint: The simultaneous solidification of IMCs interlayer supressed the scalloped growth of Cu_6Sn_5 grains in Cu/Sn (2.5 μm)/Cu interconnect during the transient liquid phase (TLP) soldering process. The growth factor of Cu_3Sn was in the range of 0.29~0.48 in Cu-Cu_6Sn_5 diffusion couple at 240~290 °C, which was impacted significantly by the type of substrates. And the subsequent homogenization process of Cu_3Sn grains was found to be consistent with the description of flux-driven ripening (FDR) theory. Moreover, Kirkendall voids appeared only in the Cu_3Sn layer adjacent to Cu-plated substrate, and this porous Cu_3Sn micro-joint was mechanically robust during the shear test.

(3) Microstructural evolution of Cu-Sn-Ni IMCs micro-joint: There was obvious inter-reaction between the interfacial reactions in Ni/Sn (1.5 μm)/Cu interconnect. The growth factor of $(Cu,Ni)_3Sn$ on Cu side was about 0.36 at 240 °C, and the reaction product on Ni side was changed from Ni_3Sn_4 into $(Cu,Ni)_6Sn_5$ with the increase of soldering temperature. In particular, the segregation of Ni atoms occurred along with phase transformation at 290 °C and thereby stabilized the $(Cu,Ni)_6Sn_5$ phase for the high Ni content of 20 at.%.

(4) Micro-mechanical characteristics of Cu-Sn-Ni IMCs micro-joint: The Young's modulus and hardness of Cu-Sn-Ni IMCs were measured by nanoindentation test, such as 160.6±3.1 GPa/ 7.34±0.14 GPa for $(Cu,Ni)_6Sn_5$ and 183.7±4.0 GPa/ 7.38±0.46 GPa for $(Cu,Ni)_3Sn$, respectively. Besides, in-situ nano-compression tests have been conducted on IMCs micro-cantilevers, the fracture strength turns out to be 2.46 GPa. And also, the ultimate tensile stress was calculated to be 2.3±0.7 GPa from in-situ micro-bending tests, which is not sensitive with the microstructural change of IMCs after dwelling at 290 °C.

Keywords: Intermetallics, Microstructure, Phase transformation, Electron backscatter diffraction (EBSD), In-situ micro-mechanical test

Publications

1. L. Mo, F. Wu, and C. Liu, "Microstructural evolution and *in-situ* nanomechanical testing on Cu-Sn-Ni IMCs microjoints, " 2016, **pending**
2. L. Mo, F. Wu, and C. Liu, "Planar growth of intermetallics in micro-scale Cu/Sn/Cu structure," 2016, **pending**
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Acknowledgements

This research is funded through LU-HUST joint research degree program, and financially supported by a Marie Curie International Research Staff Exchange Scheme Project within the 7th European Community Framework Program, No. PIRSES-GA-2010-269113, entitled “Micro-Multi-Material Manufacture to Enable Multifunctional Miniaturized Devices (M6)” and a China-European Union technology cooperation project, No. 1110.

I would like to acknowledge both of my supervisors, Prof. Changqing Liu from Loughborough University and Prof. Fengshun Wu from Huazhong University of Science and Technology, for their guidance and help in my study. They are always patient and left a thinking space to me, which is beneficial to improve my capability as a real researcher. And, it is very grateful that I have been involved in the cooperative project, then I could take the great opportunity to experience a different life in UK.

Many thanks are given to the all technicians. Their support are important for the carrying out of my experiments. Especially, I appreciated that the demonstration and supervision I have received from Geoff West and Keith Yendall in Loughborough Materials Characterisation Centre (LMCC), which enabled me to operate FIB and FEG-SEM. Meanwhile, it is also thankful to conduct the in-situ micro-testing within the help from Dr. Chaowei Guo in the Center for Advancing Materials Performance from the Nanoscale, Xi’an Jiaotong University.

Finally, I would like to express the thanks to all my friends and colleagues for their kind company and help to cheer me up in the difficulties during the period of my PhD study. And the most importance is the free and unreserved supports from my families in economic and spirit. Their love makes me here.

Liping Mo

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List of Abbreviations

2.5D	2.5 Dimension
3D	3 Dimension
AFM	Atomic Force Microscopy
Ag	Silver
Al	Aluminium
at.%	Percentage of atoms
Au	Gold
BGA	Ball grid array
BIF	Brittle Intergranular Fracture
BSE	Back-scattered electron
C4	Controlled-collapse chip connection
CGA	Column grid array
CoC	Chip-on-Chip
CP	Copper pillar
CTE	Coefficient of thermal expansion
Cu	Copper
EBSD	Electron backscattered diffraction
EDX	Energy dispersive X-ray
EM	Electromigration
FDR	Flux-driven ripening
FEG-SEM	Field emission gun-scanning electron microscope
FIB	Focus ion beam
GB	Grain boundary
GSO	Grain shape orientation map
IC	Integrated Circuit
IMCs	Intermetallics compounds
I/O	Inputs/outputs
IPF	Inverse Pole Figure [001] quick map
IQ	Image Quality (IQ) quick map
KV	Kilovolt
LGA	Land grid array

LSW	Lifshitz-Slezov-Wahner theory
MCM	Multichip module
MLC	Multilayer ceramic
mm	Millimetre
MPa	Mega pascal
nA	Nano- ampere
Ni	Nickel
nm	Nanometre
Pt	Platinum
PH	Potential Of Hydrogen
R.T.	Room temperature
SCM	Single-chip module
SE	Secondary electron
SLC	Surface laminar circuit
SLID	Solid-liquid interdiffusion bonding
SLT	Solid Logic Technology
SOH	Stand-off height
SOP	System-on-Package
sp. gr.	Specific gravity
Sn	Tin
TAB	Tape-automated bonding
T_B	The bonding temperature
t_d	Dwell time
TEM	Transmission Electron Microscopy
TLP	Transient liquid phase
T_M	The melting point temperature
TSV	Through Silicon Via
Ti	Titanium
UBM	Under bump metallurgy/metalization
WB	Wire bonding
wt.%	Percentage of weight
XRD	X-ray diffraction

Chapter 1 Introduction

1.1 Background

1.1.1 Flip-chip technology in chip-level packages

In the last decades, the satisfaction for requirements of individual electronics is the main driving force for the development and improvement made in semiconductor industry. With the increasing demand for multifunctional and miniaturized electronic manufacturing, chip-level packages (first-level packages) have been widely used in the electronic devices. Furthermore, there are three main methods to achieve the interconnection between chip and substrate, such as wire bonding (WB), tape-automated bonding (TAB), and flip-chip (FC) technology, shown in Figure 1-1. Herein, flip-chip technology refers to the chip surface (circuit) facing down on the carrier substrate, which was firstly fabricated by IBM with the controlled-collapse chip connection (C4) technology in their solid logic technology (SLT) hybrid modules for the System/360 [1, 2]. Many advantages have been gained by the application of flip-chip technology, including lower inductance, higher frequencies, better noise control, higher number of inputs/outputs (I/O) and future electronic devices miniaturization availability [3-5]. Therefore, the flip-chip technology has become the most popular method amongst all interconnection technologies.

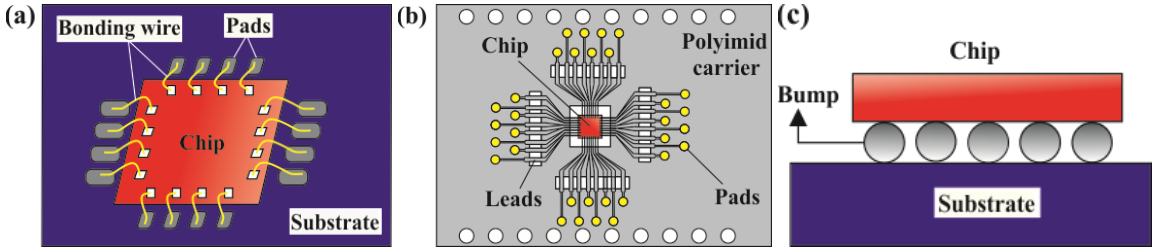

Figure 1-1 schematic images of primary interconnection technologies for chip-level packages: (a) wire bonding, (b) tape-automated bonding, and (c) flip-chip bonding

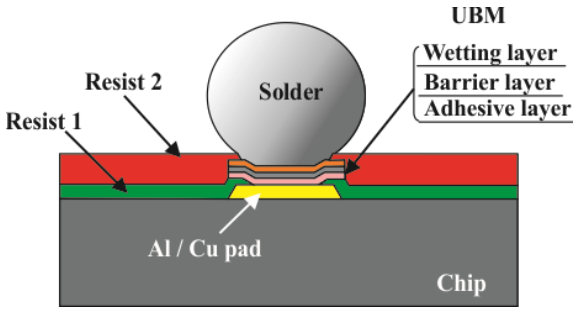

Figure 1-2 schematic image of the traditional under bump metal (UBM) structure

The traditional process of the flip-chip bonding consists of under bump metallurgy (UBM) and solder bump fabrication, die alignment, and reflow process, resulting in a robust interconnection between the chip and substrate. The UBM is manufactured to obtain a better integration between the solder bumps and the wafer or chip with the thickness of appropriate 1 μm [6]. There are usually three functional layers composing of the UBM, namely an adhesive layer, a diffusion barrier layer and a wetting layer [7], as exhibited in Figure 1-2. The adhesive layer provides a good adhesion to the metal surface on the chip, while the second barrier layer prevents the device from being contaminated by the diffusion of solder components, and the wetting layer is for the following solder fabrication. Subsequently, the solder bumps can be fabricated by evaporation or electrodeposition of Sn-based alloys, or dispersing solder paste through screen printing. Finally, after the die is aligning on the carrier substrate,

the assembly process is finished by experiencing a high-temperature reflow in oven. During this process, the metallurgical reactions happen between the solder bumps and the adjacent metal pads to achieve permanent and robust bonding. Then, the solder joint will play a vital role in the following service life of the devices, which creates the conductive path to realize the electrical connection between circuit on wafer and the carrier substrate. Simultaneously, they can also be treated as a structural module to provide mechanical support in the whole package, and help conduct the heat energy produced by the working circuit.

Nowadays, there is a growing demand for smaller and higher performance integrated IC electronics, and fine pitch or ultra-fine pitch flip-chip packaging with higher I/O density is becoming increasingly compulsory to meet this challenge. However, the traditional fabrication method of solder bumps for flip-chip packaging is becoming more and more difficult to achieve the ultra-fine pitch and high-count integration due to the increasing possibility of short circuits which may occur during the reflow process [8]. Therefore, several new methods have been established leading to a much lower dimension and better electrical, thermal performance semiconductor packaging [9-11]. For example, the optimized micro-C4 technology is first utilized in the fine pitch interconnection. And combining with through silicon via (TSV) technology, the micro-C4 has become one of the main challenges in the multichip module packaging area [5, 12]. Besides, some innovative interconnects such as the copper pillar bump bonding, the direct copper bonding, and nano-metal connection have also been researched and developed [13].

1.1.2 Copper pillar bump bonding in 3D integration

In the chip-level package, the concept of multichip module (MCM) packaging is defined with the classification of chips number mounting in an electronic package. With the comparison of single chip module (SCM), the fundamental characteristic of MCMs is owning the powerful substrate, which should has the ability to afford all the electrical connection paths for the multi-chips (or dies), including four conductive layers and 100 I/O leads for the minimum requirement [14]. As a result, the MCM technology extraordinarily improves the interconnecting density in per package

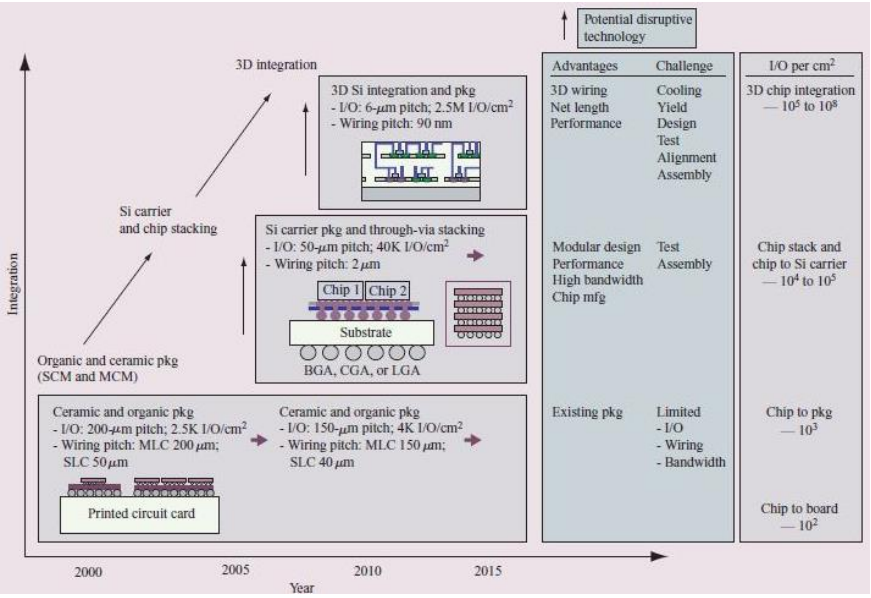

Figure 1-3 silicon integration roadmap from board-level integration to 3D chip integration (SCM- single chip module; MCM- multichip module; LGA- land grid array; BGA- ball grid array; CGA- column grid array; MLC- multilayer ceramic; SLC- surface laminar circuit) [15]

Furthermore, a new configuration to achieve the MCM packaging as 3D integration has emerged, which utilizes the space effectively and adequately within the package, especially in the vertical direction. 3D integration technology is a profound revolution of architecture within one package. It breaks the limitation of Moore's law, bringing more function with lower volume in a single package than the conventional ones [16]. The I/O density has increased significantly from 10^2 per cm^2 in the chip to board level packaging to the10^5~10^8 per cm^2 in 3D chip integration, as illustrated in Figure 1-3 [15]. Several different 3D integrated structures have been classified, namely 3D wafer-level packaging, 3D ICs stacking, 3D heterogeneous and systems integration. Also, the 2.5D and 3D integration based on interposer technology are included [17].

In the aspect of manufacturing technology, the copper pillar bump technology is one promising approach to satisfy the ultra-fine pitch interconnection on silicon packages [18, 19], which has attracted increasing interest and been suggested as the most promising next generation technology to achieve multichip module (MCM) packaging and in particular of 3D integration. Under 150 μm, traditional solder bump shows limitations to meet the specifications of increasing integrated circuit performances and integration scheme. Indeed, their electrical characteristics and stand-off during reflow do not allow to implement them in these new applications. Meanwhile, copper pillar bump has an outstanding performance in that area. As shown in Figure 1-4, the advantages of the copper pillar bump are obvious such as the high stand-off height to enable the fine pitch possibility, and also the solder can be controlled in a limited area with the restricted volume, instead of spreading out on wettable surfaces too much during the bonding process. However, in other aspect, the reduced collapse of solder in the copper pillar bump has become the potential main disadvantage. An extra necessary coplanarity control of bumps should be implemented to prevent the probable non-wetting with the shorter bumps [20].

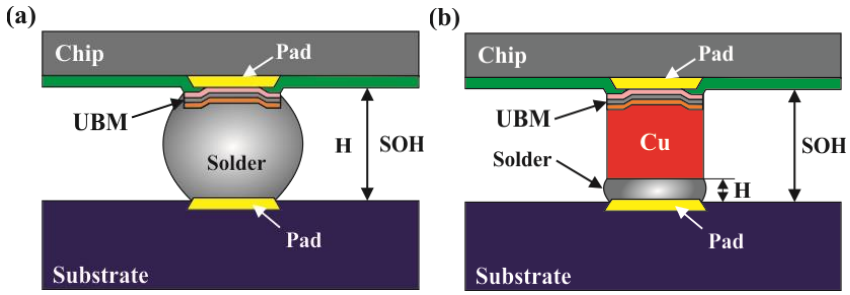

Figure 1-4 comparison between two bonding structures (a) solder bump, and (b) copper pillar bump (H-Interconnected Height, SOH-Stand-off Height)

1.2 Problem statement and research motivation

A. Multi-soldering in 3D IC stacking

Compared with wire bonding and other contact interconnection methods, solder has a much broader application in electronic packaging area, especially in the growing 3D multilayer integration. However multi-reflow processes are implemented to achieve the numbers of layers interconnection on vertical direction in 3D stacking packages, and these reflow processes will result in re-melting of the residual Sn-based solder. Then, overflow will happen in the remelted solder, which increases the possibility of inaccurate contraposition or short-circuit to occur.

B. Full intermetallic joints formed under the miniaturization

Considering the dramatically scaling down of solder interconnection, the reaction between UBM and solder forming the intermetallic compounds (IMCs) is becoming increasingly important. For the chips with ultra-fine

pitches ranging from 20 to 10 μm, the micro-interconnection is only comprised of IMCs after reflow process without any solder residue, as shown in Figure 1-5. The typical micro-bump is under 10 μm thick, and it is quite easy for the entire solder volume to be totally transformed into an intermetallic bump [21]. Therefore, the characterisations of the IMCs itself are the dominant parameter to govern the reliability of the final interconnection. Then, in order to fabricate the reliable new generation application specific integrated circuit (ASIC) devices supported by the 3D stacking technology, the properties of the micro-IMCs interconnection must be investigated systematically to allow fundamental understanding of the interfacial bonding mechanisms.

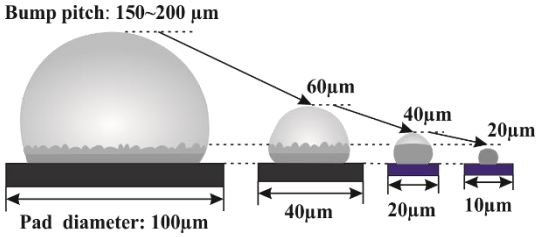

Figure 1-5 microstructural evolution within solder joint scaling [21]

First of all, thermo-compression method is selected to realize the miniaturized connections, instead of the conventional reflow process. The typical description of the metallurgical reaction during this soldering process is solid-liquid interdiffusion (SLID) bonding [22, 23] or transient liquid phase (TLP) soldering [24, 25]. Whilst different parameters used in this process as time, temperature, and pressure, play a significant effect on the microstructure of IMC joints [26, 27]. It requires a much further study in order to improve the reliability of final interconnection. The minimum thickness of initial solder layer needed to form a pore-free joint has also been discussed in Bosco's work [28], where at least 10 μm of initial Sn layer was suggested in his work. However the estimation was primarily based on the growth of the Cu_6Sn_5 grain without considering the growth of Cu_3Sn, which presents an obvious shortcoming, thus unrealistic for the case where the Sn layer is even thinner than 10 μm and the growth of Cu_3Sn layer can be comparable against the Cu_6Sn_5 layer.

Due to the further reduction of joint size, not only the manufacturing process of the IMC joints, but also the reliability of such formed joints are to be concerned ever more,. For instance, Kirkendall voids are normally found in Cu_3Sn layer or near the interface between Cu_3Sn and plated Cu substrate after aging or during the service period [29-31], which will strongly impact the reliability of the IMC interconnection. Moreover, the IMCs are considered to be brittle since the cleavage morphology is often observed at the IMC fractured surfaces. Ghosh [32] has microscopically seen some slip bands appeared in Cu_3Sn during the indentation test, which indicates the question whether the IMC is really brittle or not is still under debate [33].

1.3 Research aims and objectives

This project aims to promote the application of full IMCs micro-joints which may be viable for the miniaturized 3D integration. In order to guarantee the quality of interconnection accomplished by IMCs, the relationship between microstructural characteristics of these IMCs micro-joints and the issues of reliability should be established. Therefore, the aims and objectives of this project can be identified as follows:

(1) To develop an appropriate method to prepare IMCs micro-interconnection reliably and cost-effectively, with a thickness of no more than 10 μm in laboratory. These samples should be easy to prepare and observe, meanwhile they should be representative and reflecting the true solder interconnection and miniaturization.

(2) To reveal the effect of parameters of soldering process on the microstructural structure of IMCs micro-joints. This should be carried out by understanding the mechanism of interfacial reactions occurring in these micro-

joints.

(3) To elaborate the process of formation and microstructural evolution to the terminal full IMCs micro-joint with stable and homogenous composition. To gain an insight into the relevant characteristic features of the interconnected microstructure.

(4) To establish a reliable system to estimate the quality of IMCs micro-joints, such as mechanical properties, with an appropriate testing method designed purposely.

(5) To study an alternative structure of IMCs interconnection, which may possess further advantages in terms of electrical or mechanical performance.

1.4 Statement of main innovation and contributions

(1) The phenomena of planar growth of IMCs has been observed. This appearance cannot be neglected and treated as the overflow of melting Sn-solder or the volume expansion of IMCs phase transformation.

(2) The mechanism of microstructural evolution in the Cu-Sn IMCs micro-joints has been proposed in detail. The flux-driving theory has been applied to describe the homogenizing process of Cu_3Sn micro-joint, where the growth and repining occurred simultaneously.

(3) An alternative sandwich structure as Ni/Sn/Cu has been recommended to realize the full IMCs interconnection in 3D integration. The interaction between two different interfacial reactions (Cu/Sn and Ni/Sn) has been discussed, wherein the phenomenon of Ni segregation has been observed in the Cu-Sn-Ni IMCs interlayer and the process of that has been demonstrated with the analysis of the diffusing paths of Cu and Ni atoms.

(4) Specific types of IMCs micro-cantilevers have been designed and fabricated by focus ion beam (FIB), which makes it feasible to measure the mechanical properties of IMCs through in-situ nano-compression and nano-bending tests.

1.5 Thesis structure

This thesis is constituted with eight chapters, which includes three major sections, as shown in Figure 1-6. The first section contains the **chapter 1** Introduction and **chapter 2** Development of solder micro-interconnection technology. The second section is the experimental investigation focusing on the growth behaviour of IMCs and the mechanical testing, including the **chapter 3~7**. Then, the summary is given as the third section in the **chapter 8** Conclusions and future work.

In the first section, the background and the literature review have been presented, mainly focusing on the solder-copper pillar bump as the new generation of interconnection used for 3D integration. And the literatures on the common Cu-Sn and Ni-Sn intermetallics also have been introduced in chapter 2.

In chapter 3, the experimental methodology has been described. The sandwich structures as Cu/Sn/Cu and Ni/Sn/Cu have been prepared by the method of electroplating. Through the transient liquid phase (TLP) soldering, the interconnected specimens have been made as the full IMC micro-joints.

According on the growth direction of IMCs in micro-joints, there are two main sections have been included to focus on planar and perpendicular growth. Chapter 4 concentrates on the planar growth of IMCs in Cu/Sn/Cu and Ni/Sn/Cu sandwich structures. And the other perpendicular growth of IMCs has been studied in chapter 5, chapter 6 and chapter 7. Particularly, the phase transformation in Cu-Sn IMCs micro-joints has been observed in

Chapter 5, and the homogenizing process of Cu_3Sn joint has been analysed by electron backscattered diffraction (EBSD) in chapter 6, where the process of microstructural evolution in Cu-Sn IMCs micro-joints has been investigated. In Chapter 6, the results from shear testing conducted by nanoindentation machine is also described. Besides, for the Ni/Sn/Cu structure, the formation and microstructural evolution have been elaborated in chapter 7. The diffusion behaviour of Ni in these IMCs micro-joints has been discussed. And the in-situ nano-mechanical system has been selected to measure the mechanical properties of Cu-Sn-Ni IMCs.

Finally, the major findings from the study are concluded in chapter 8, with some recommendations of future work and potential research.

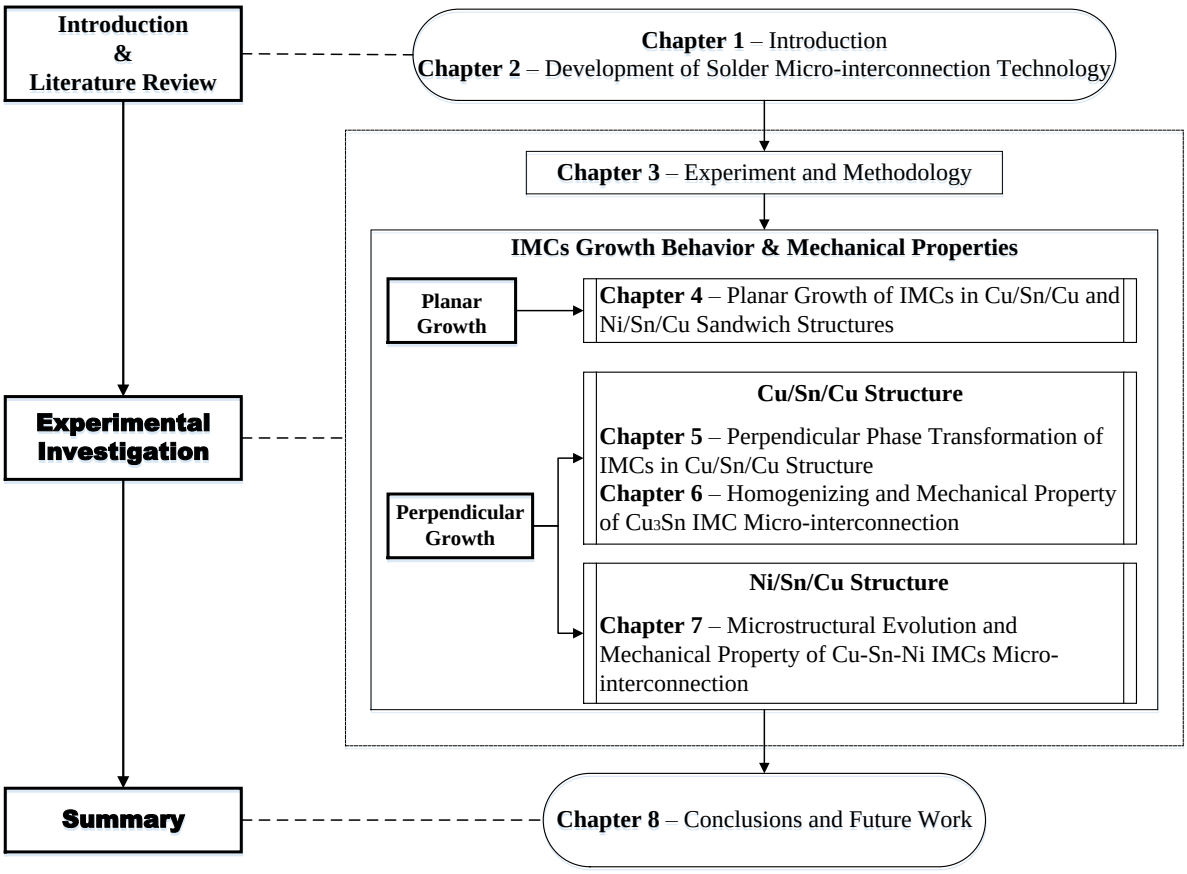

Figure 1-6 the blueprint for the whole thesis

Chapter 2 Development of Solder Micro-interconnection Technology

2.1 Solder bump bonding

The fabrication of solder bump is critical in the manufacture of micro-interconnection. The stencil printing technology and electroplating solder alloys are the two popular methods to manufacture the solder bump on UBM or Cu pads.

2.1.1 Stencil printing technology

When the bump pitch is around 200 μm or higher, the stencil printing method is an efficient, low cost, and high reliability way to manufacuture the solder bump, and the basic principle is shown in Figure 2-1. The process starts with the fabrication of under bump metalization (UBM) structure, usually electrolesss plating a layer of nickel and gold. Then the solder paste is stencil printed on the UBM layer. Finally, the solder bump is formed after a relfow process, following by the flux residule cleaning. There are many parameters impacting the solder quality, such as the stencil design, viscosity of the paste, percentage of the flux, and the printing angel. With all these parmeters well controlled and optimized, the stencil printing technology has been successfully applied for several decades to achieve the good soldering quality [34-36].

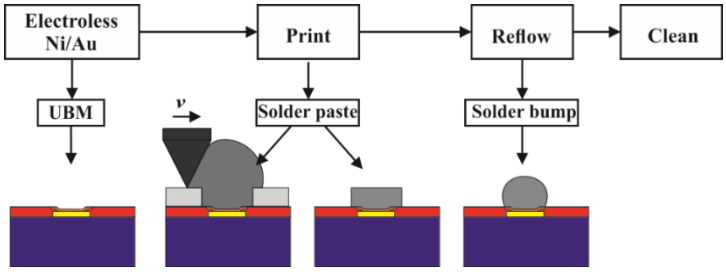

Figure 2-1 diagram of stencil printing process to make solder bump

D. Manessis [36] can fulfil the solder fabrication with 80 μm bump pich using the optimised traditional stencil printing process, however it still cannot meet the continually increasing demand for fine pitch and high density interconnection. The fine pitch between the bumps has almost reached to the limitation of stencil printing method, considering the stencil manufacturing limitations, maximum solder paste volume, and the minimum separation distance to avoid the increased possibility of short circuit.

2.1.2 Micro-C4 technology

The micro-C4 technology needs a new plating method to fabricate the micro-bumps. Electroplated bumping is the most common method to manufacture the bumps on wafers, because of its advantages of highest yields at tight bump pitches. As illustrated in Figure 2-2, the general solder bump is fabricated with the electroplating method. Different layers of materials are sputtered on the silicon water creating the UBM layer. At the second stage, the UBM opening surrounding is manufactured by spinning a photoresist and followed photoetching. The key process is the electroplating the solder, and the final solder bump is completed due to the surface tension force during the reflow.

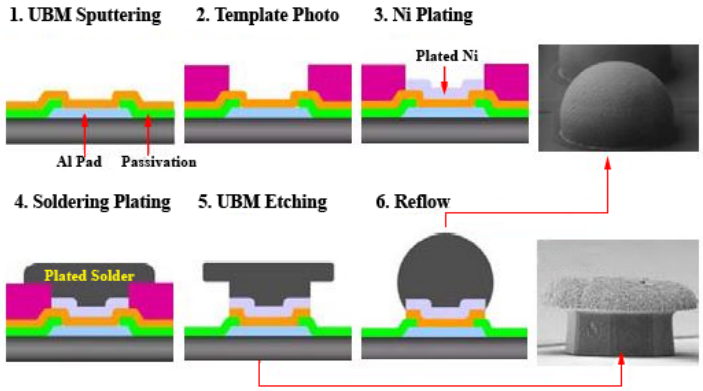

Figure 2-2 fabrication process of solder bump by micro-C4 technology [9]

2.2 Copper Pillar Bump Bonding

Fundamentally, the mechanism of the solder bump forming in micro-C4 method is the same with the stencil printing technology. The improvement is the replace the stencil and solder paste with photoresist and electroplating materials respectively, enabling the fabrication of much smaller solder bump with finer bump pitch. However the short circuit is still much likely to occur during the solder collapse in the reflow process [8], which limits the micro-bump to the area of ultra-fine pitch 3D chip stacking. Thus, copper pillar bumping emerged as a promising method, and has attracted much interest since it was published [37, 38]. The fabrication of copper pillar bump is similar with the micro-C4 bump process, as shown in Figure 2-3, and the main difference is that a thick layer of copper (about 30 μm) is electroplated before the plating of solder.

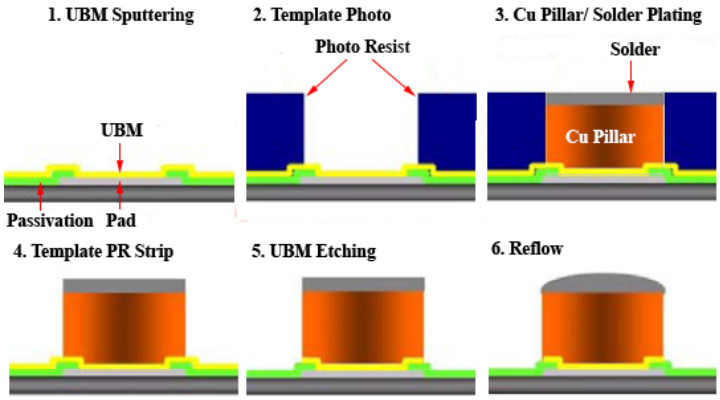

Figure 2-3 process flow for making Cu pillar bump [9]

Based on the electroplating method, the fabrication process of copper pillar bump is made up of four main steps:

- A thin adhesion layer, which is composed by Cr, Ti or Ni layer with the thickness of 0.15~0.2 μm [6], is sputtered to cover the chip pad and overlap onto the chip passivation.
- A barrier layer is sputtered as the second layer of UBM to prevent diffusion contamination between the solder and pad. This layer is usually 1 μm thick Ni layer.
- A conductive layer of copper is sputtered as the seed layer which enables the following fabrication of copper pillar.
- The copper pillar is formed by electroplating copper on the seed layer. And then the solder is plated on top of the pillar as followed, which will form a solder bump after reflow.

The extensive study of copper pillar bump interconnection has demonstrated numerous advantages when compared to traditional solder bump, as shown in Table 2-1. The first is the copper pillar bump enables the fine or ultra-fine pitch capability. Samsung Electronics. Co. achieved the chip-on-water bonding with the 40 μm pitch interconnection through the copper pillar bump technology [10]. Chiang-Kuan Lee [39] and Yuki Ohara [40] even fulfilled the wafer bumping assembly on 5 μm pads with 10 μm pitch using the copper pillar bump. Obviously, the copper pillar bump has provided a better way to achieve the ultra-fine pitch interconnection. However, it also significantly improves the requirment of high accuracy of die alighment. The reason is that the effect of self-alignment helps to solve the problem of misalignment for the tradional solder bump by the surface tension during the reflow rocess, however the limited volume of solder in copper pillar bump declines the self-alighment effect during the bonding process [41].

Table 2-1 application characteristics of solder bump and copper pillar bump interconnection [9]

Application Characteristics	Solder bump	Copper pillar bump
Pitch	~140 μm	60 μm
Stand-off height (SOH)	Low	High
Under filling	Limit	Easy
EM and thermal performance	Lower	Higher
Multiple IC stacking	Unfavourable	Favourable

Meanwhile, the thermal issue is becoming an indispensable problem especially in the multichip module (MCM) where many layers of chips are stacked together in order to achieve the better electrical calculation performance. The high stand-off height of the copper pillar bump increases the distance between multiple dies, which greatly improves the efficiency of heat transfer in the entire bonding [42]. Underfill (UF) plays an important role in the flip-chip packaging process due to its significant influence on the reliability of joint, and it becomes a challenge with the decreasing gap between the chips or chip and substrate. The high stand-off height of copper pillar bump also simplified the underfilling process, and the high conductivity and high electromigration resistance of the copper enhances the reliability of the bonding [43].

As shown in Figure 2-4, the packaging process using copper pillar bumps mainly consists with the die alignment and reflow process [20]. This soldering process has been accomplished with the implementing of common reflow profile, but adding a loading force simultaneously, called as thermo-compression bonding [40, 44]. It is necessary to guarantee the quality of interconnection when the size of solder bump decreased for the fine-pitch application.

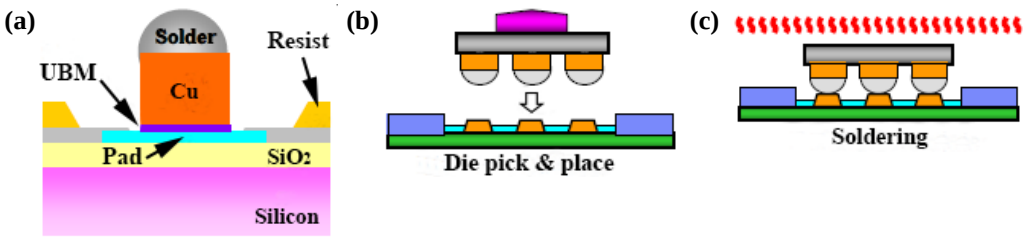

Figure 2-4 IC packaging process with copper pillar bumps: (a) sechmatic image of the copper pillar bump, (b) die alignment, (c) relfow process [11]

The microsystems packaging research centre at GaTech (GT-PRC) suggested that the interconnect paradigm for water level packaging is changing from the current 150~255 μm to the fine pitch level ranging 20 μm to 50 μm, and will still tend to the ultra-fine pitch around 10 or under 10 μm [45]. The continually decreasing pitch and

bump size are more likely to induce the full intermetallic compounds (IMCs) interconnection. Particularly the shrinkage of solder volume appearing both in the micro-C4 and copper pillar bump bonding significantly increases the possibility of full IMCs interconnection.

2.3 Intermetallic Compounds Interconnections

2.3.1 Reaction and Formation of IMCs

Copper is applied in the manufacture of circuit widely for its excellent conductivity. As the interconnected path in packaging, the reaction between Cu pad and Sn-solder has been investigated well in the past decades. In order to get a robust interconnection, various types of lead-free Sn-based solders have been developed [46-48]. Sn-Ag-Cu solder has become the most popular one with the melting point temperature of 217 °C [49]. To realize the interconnection between pad and solder, the reflow process is the necessary step, the general profile of which is shown in Figure 2-5. Then, a thin layer of Cu-Sn IMCs is formed on the interface between Cu pad and Sn-solder to signify the success of interconnection. The common types of Cu-Sn IMCs in room temperature are η'-Cu_6Sn_5 and ε-Cu_3Sn, referred from the binary Cu-Sn phase diagram in Figure 2-6.

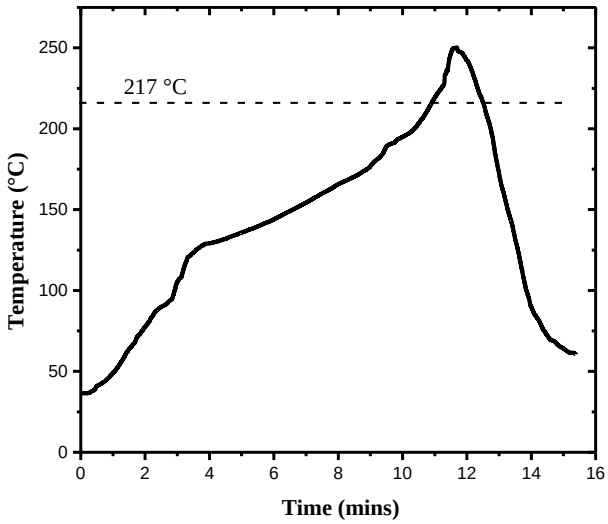

Figure 2-5 the general reflow profile for Sn-Ag-Cu solder

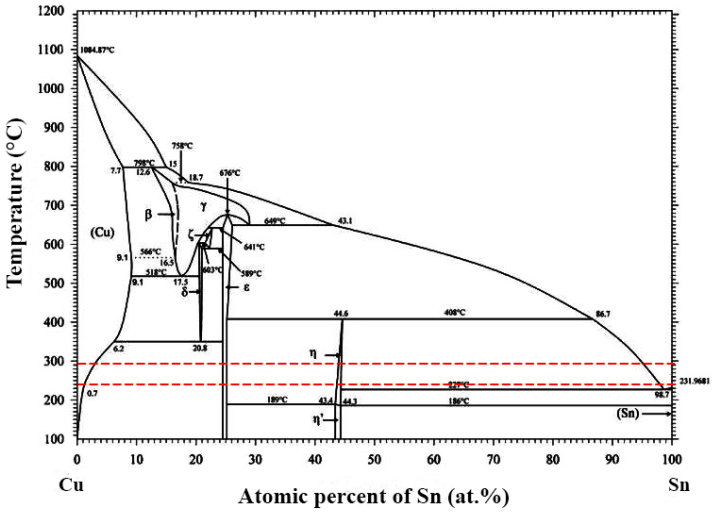

Figure 2-6 Cu-Sn binary phase diagram [50]

Many research have been done on the growth behaviour of Cu-Sn IMCs [51-53]. The η-Cu_6Sn_5 is usually

described as scallop-like in the reaction between liquid solder and solid Cu substrate [54, 55]. As the Cu_3Sn is too thin to be detected in the interconnection after first reflow, the Cu_3Sn layer normally appears in the joints which has experienced multi-times reflow or been aged for a long time [56-58]. The manner of Cu_3Sn growth is always considered as planar. Furthermore, an empirical power law (equation 2-1) is used to evaluate the thickness of IMC layer versus isothermal dwell time. Where, Δd^2 is the change of square of IMC thickness in the joints formed with dwell time (t); and the coefficient of IMC layer growth (K) is concerned with the absolute temperature (T), the frequency factor (k_0) and activation energy (E), which can be derived from the Arrhenius equation (2-2). The growth factor of IMC layer is represented by n. When n equals to 0.5, it means that the growth of IMC layer is controlled by the mechanism of grain boundary diffusion; and n is less than 0.5 indicating that the growth velocity of IMC layer would be limited by the rate of chemical reaction [59]. Some representative value of n are exhibited in table 2-2 for IMCs layer in different structures.

$$\Delta d^2 = d_t^2 - d_0^2 = Kt^{2n} \tag{2-1}$$

$$\sqrt{K} = k_0 \exp\left(\frac{-E}{RT}\right) \tag{2-2}$$

Table 2-2 the growth factor (n) of IMCs in different diffusing structures

Sample structure	Temperature (T/°C)	Growth factor (n)
Sn/Cu [60]	170	Cu_3Sn: 0.33±0.06
Sn-3.5Ag/Cu [61]	70~170	0.463~0.679
Sn-3.5Ag/Cu [62]	170, 205	0.42
Electroplated Sn/Cu [63]	150~225	0.5
Electroplated Cu/Sn/Cu [64]	150~300	0.5

In particular, the Cu/IMC/Cu micro-structure was suggested to form through the approach of transient liquid phase (TLP) bonding, and it is found in Bosco's work that the thickness of Sn-based solder layer is critical to form the intact IMC joints [28]. The minimum required thickness of Sn-solder has been calculated under the two different growth manner of IMCs. However, as the appearance of Cu_3Sn can always be neglected after the first reflow, the primary factor in this case is the growth of scalloped Cu_6Sn_5 grains. If the thickness of Sn-solder was not thick enough, the scalloped Cu_6Sn_5 grains from two sides would touch each other, and isolate the melting Sn-solder locally, as shown in Figure 2-7. Then, the voids will produce for the shrinkage of Sn-solder in the solidification process. Therefore, the sufficient thickness should be thicker than the double size of the average of these scalloped Cu_6Sn_5 grains, which has been recommended to be around 6 μm.

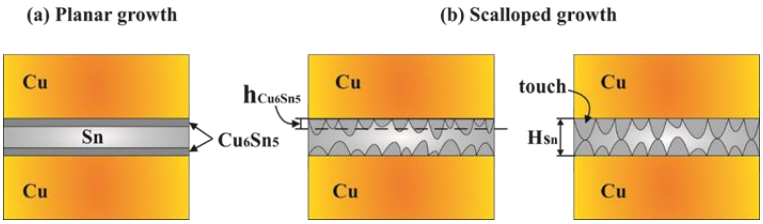

Figure 2-7 relationship between the growth manner of interfacial IMC and the thickness of Sn-solder

Besides, another interconnecting format used in practice is Ni/Sn/Cu sandwich structure for the Ni layer is popularly applied as the UBM layer to retard the excessive growth of interfacial IMCs. Thus, the Ni-Sn reaction should also be considered in the soldering process. From the Ni-Sn phase diagram in Figure 2-8 [65], the Ni_3Sn_4,

Ni_3Sn_2 and Ni_3Sn IMCs and the eutectic phase are commonly observed in the Sn-Ni alloy. In fact, the sponge-like Ni_3Sn_4 IMC has been observed on the Sn/Ni interface after soldering [66] and the Ni_3Sn_2 became much thicker for the solid diffusion in aging stage [67, 68]. Moreover, there is an obvious interfacial interaction between the two different interfaces (Cu/Sn and Ni/Sn) in Ni/Sn/Cu micro-interconnection for the decreasing stand-off height. And the Cu-Sn-Ni ternary reaction would occur and be more complicated than the Cu-Sn or Ni-Sn binary reaction. In the soldered Ni/Sn/Cu micro-joint, the main types of IMCs formed on Cu-side are Cu_3Sn and $(Cu,Ni)_6Sn_5$, where the growth of Cu_3Sn has been supressed [69]. Meanwhile, as the reaction rate of Ni-Sn is much lower than that of Cu-Sn reaction, the Cu atoms diffusing from the Cu-side reaching the Ni-side has made the IMC layer on Ni-side to be transformed into $(Cu,Ni)_6Sn_5$ mainly. And sometimes, a thin layer of $(Ni,Cu)_3Sn_4$ or $(Ni,Cu)_3Sn_2$ would also appear between the $(Cu,Ni)_6Sn_5$ and Ni UBM layer [64, 70-72], as illustrated in Figure 2-9. Previous research has found that the addition of Ni element in Cu_6Sn_5 IMC has brought some considerable effects on its formation process and properties [73, 74]. When the content of Ni in Cu_6Sn_5 is only 1 at. %, the transition of Cu_6Sn_5 from high-temperature phase (η-Cu_6Sn_5) to low-temperature phase (η'-Cu_6Sn_5) will be prevented [75, 76]. And morphologies of interfacial IMCs in Ni/Sn/Cu micro-joint are different with that in Cu/Sn/Cu micro-joints, the details are shown in Figure 2-10.

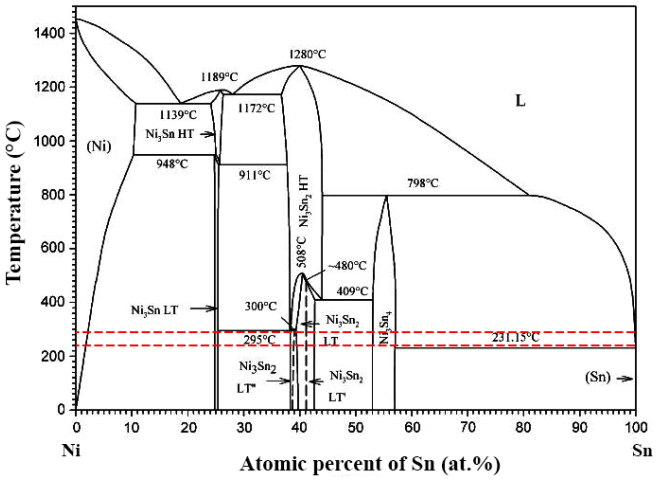

Figure 2-8 Ni-Sn binary phase diagram [65]

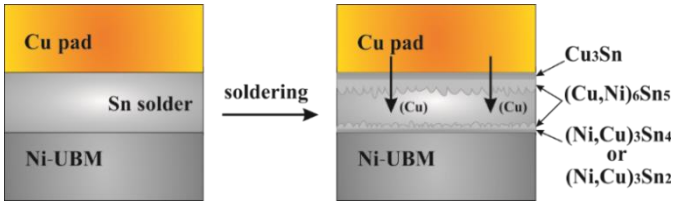

Figure 2-9 schematic diagram for the microstructure of Ni/Sn/Cu joint after soldering

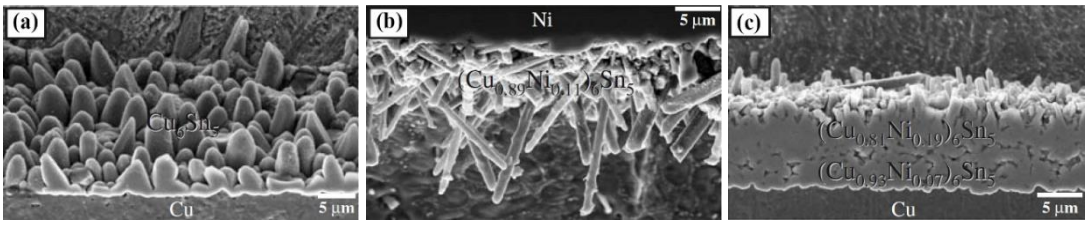

Figure 2-10 IMCs morphologies (a) Cu_6Sn_5 in the Cu/Sn3.5Ag; (b) $(Cu,Ni)_6Sn_5$ on Ni-side and (c) $(Cu,Ni)_6Sn_5$ on Cu-side from Ni/Sn3.5Ag/Cu structures after soldering [77]

In addition, more Sn-Ni and Sn-Cu-Ni alloy solder have also be developed to make good use of Ni atoms in

suppression of interfacial Cu_3Sn growth [78-80]. The effect of processing parameters of directional solidification on microstructure of Sn-Ni alloys has been investigated by Peng-Peng [81], where the relationship between micro-hardness and growth rate of Ni-Sn IMCs (Ni_3Sn_2 and Ni_3Sn_4) is consistent with the Hall-Petch formula. Especially, the metastable $NiSn_4$ has been found in the as-cast Sn-Ni alloy with 0~0.45 wt.% Ni under high cooling rates [82]. And the appearance of interfacial Ni_3Sn_4 was beneficial to the formation of $NiSn_4$. Besides Lin [83] has observed the equilibrium phases of Sn-Cu-Ni alloys at 240 °C, the typical microstructure as IMCs mixture produced from Sn-50 at.% Cu-10 at.% Ni alloy is displayed in Figure 2-11. Moreover, with the basis of experimental results and thermal kinetics calculation, Yu [84] has proposed that the relationship of Ni content in $(Cu,Ni)_6Sn_5$ phase and the neighbouring $(Cu,Ni)_3Sn$ phase as shown in Figure 2-12 can be achieved in the local equilibrium situation.

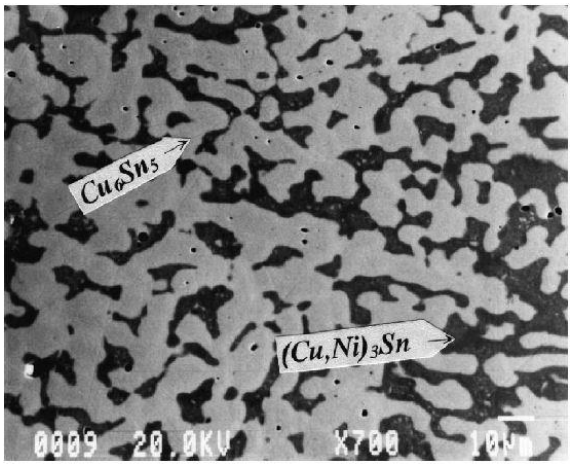

Figure 2-11 microstructure of Sn-50 at. % Cu-10 at. % Ni alloy after equilibrium solidification [83]

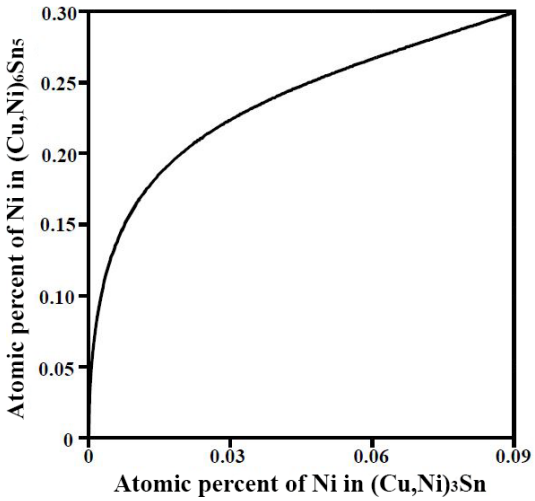

Figure 2-12 relationship of Ni atomic percent in $(Cu,Ni)_6Sn_5$ and $(Cu,Ni)_3Sn$ for balance [84]

2.3.2 Properties of Intermetallic Compounds

The properties of certain IMC (Cu_6Sn_5, Cu_3Sn and Ni_3Sn_4) have been widely studied, such as the crystalline structure, the melting points, Young's modulus, Coefficient of thermal expansion (CTE) and so on. This kind of knowledge can significantly help to understand the basic principle of micro-solder joints' formation and analyse their failure mechanism as well.

There are already some research conducted regarding to the intermetallics, such as Cu_6Sn_5, Cu_3Sn and Ni_3Sn_4,

which are very common through the using of Sn-solder in the electronic packaging. And lots of interest has also been attracted in terms of the phase transformation process about Cu_6Sn_5. The high temperature phase η-Cu_6Sn_5 with hexagonal structure will be transformed into the monoclinic η'-Cu_6Sn_5 phase, when the temperature decreases to lower than 180~187 °C. And a volume expansion of 2.15% is produced by that transformation [85]. At room temperature, the crystal structures of Cu_6Sn_5 and Cu_3Sn are shown in Figure 2-13 [86]. Particularly, the complete crystalline parameters of Cu_3Sn were detected by X-ray precession diffraction, which has been reported by Watanabe [87]. And a large ratio of crystal constant *b/a* was discovered for Cu_3Sn. In general, the Cu_3Sn is thought to be orthorhombic structure, but after a long time annealing (1000 h) at 170 °C, the Cu_3Sn is detected to be hexagonal structure by the means of X-ray diffraction [88].

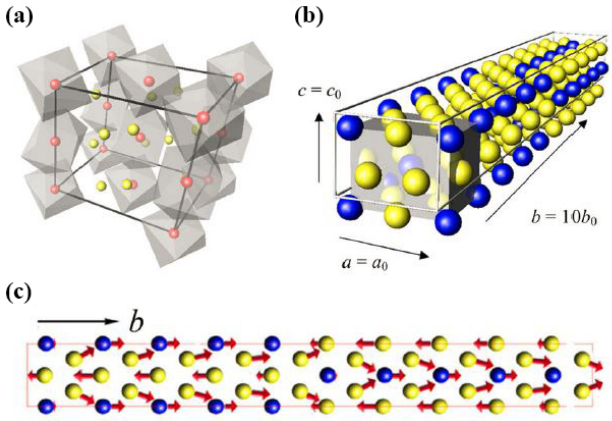

Figure 2-13 lattice structure of Cu_6Sn_5 and Cu_3Sn [86]

Because of the asymmetric lattice structures, the single grain of Cu_6Sn_5 or Cu_3Sn exhibits anisotropic characteristics to some extent. For example, the Young's modulus and hardness of Cu_6Sn_5 are various along the different growth directions, and the maximum values turn out on the c-axis as shown in Figure 2-14 [89]. Moreover, the anisotropy of Cu_3Sn has also been discussed basing on the density functional theory. Voids were induced by strain during interfacial inter-diffusion, which can be fundamentally explained as the different bonding strength of Cu-Cu and Sn-Cu atoms in Cu_3Sn [86]. And Ching-Feng Yu [90-92] have applied the molecular dynamics method to characterize the material properties of Cu_3Sn as mono- or poly-crystalline. It has been found that both the ultimate tensile strength and shear strength of Cu_3Sn crystal increased with the rising of stain rate.

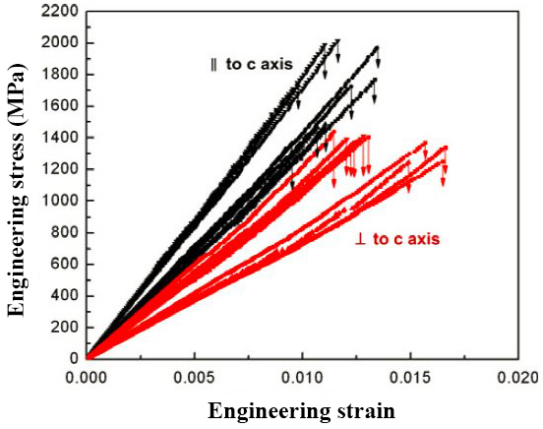

Figure 2-14 results from compression test on Cu_6Sn_5 single crystal [89]

However, there are always polycrystalline IMCs layers formed in micro-joints and the properties of IMCs layers demonstrate isotropy. Jiunn Chen [93] has applied the first principle calculation to obtain the Young's modulus of polycrystalline Cu-Sn IMCs, as 125.98 GPa for Cu_6Sn_5 and 134.16 GPa for Cu_3Sn. Except of that, the properties of IMCs are mainly experimentally measured by nanoindentation tests, and the maintained results are listed in Table 2-3. It is worth noticing that although the $(Cu,Ni)_6Sn_5$ has the similar crystal structure to Cu_6Sn_5, the Young's modulus of $(Cu,Ni)_6Sn_5$ is larger than the value of Cu_6Sn_5 and the reduced modulus of $(Cu,Ni)_6Sn_5$ from nanoindentation tests vary with the Ni content in the range of 124.3±7.9 ~ 139.5±4.9 GPa [94, 95]. Under the condition of isothermal annealing at 125 °C, the Young's modulus of Cu-Sn-Ni IMCs decreased from 207 GPa to 165 GPa as a consequence of phase transition from $(Cu,Ni)_6Sn_5$ to $(Ni,Cu)_3Sn_4$ [96]. Besides, the addition of Ni also makes the coefficient of thermal expansion (CTE) of $(Cu, Ni)_6Sn_5$ smaller than Cu_6Sn_5 [97], and change the location of crack initialled in Cu_6Sn_5 IMC [98].

Table 2-3 material properties of some typical IMCs

IMCs	Young's modulus (GPa)	Hardness (GPa)	Poisson ratio	Types of the testing samples
Cu_6Sn_5	96.9	-	0.309	Casted block material after aging [32]
	125±6.8	6.10±0.53	-	Sn-3.5Ag/Cu aged at 240 °C/2 h [99]
	134±7	6.5±0.3	-	Sn/Cu aged at 200 °C/341 h [100]
	119±1.9	6.45±0.14	-	Sn/Cu aged at 150 °C/1000 h [101]
Cu_3Sn	123.2	-	0.312	Casted block material after aging [32]
	135.7±5.9	5.69±0.58	-	Sn-3.5Ag/Cu aged at 240 °C/2 h [99]
	160±8	6.2±0.4	-	Sn/Cu aged at 200 °C/341 h [100]
	132.2±3.6	6.34±0.14	-	Sn/Cu aged at 150 °C/1000 h [101]
$(Cu_{1-x}Ni_x)_6Sn_5$	206.8±5.5	10.07	-	SnAgCu/Ni soldered at 125 °C/0 h [96]
$(Cu_{1-y}Ni_y)_3Sn_4$	164.9±3.1	8.65	-	SnAgCu/Ni aged at 125 °C/260 h [96]
Ni_3Sn_4	133.3±5.6	-	0.33	Casted block material after aging [32]
	142.7±9.2	8.12±0.62	-	Sn-3.5Ag/Cu aged at 240 °C/24 h [99]
	145.8±3.3	7.31	-	SnAgCu/Ni aged at 125 °C/500 h [96]
	140.3±4.3	6.33±0.21	-	Sn/Cu aged at 150 °C/1000 h [101]

2.3.3 Reliability analysis

(1) Mechanical properties

The results of the previous research revealed that the percentage of Cu-Sn IMCs in solder joints increases from 9% to 36% when the interconnected height of the joint decreases from 100 μm to 10 μm. As a consequence, the fractural modes under monoaxial stretching are also changed from the ductile fracture to brittle fracture, whilst the nucleation of the fracture transfers from the interior of the solder to the IMCs interface, and the ultimate tensile strength increases from 35 MPa to 47 MPa [102, 103].

Therefore, the IMCs layer as the unique connecting part in the full IMCs joints is expected to be critical with the quality of interconnection, which would bring a great challenge to the reliability and lifetime of electronic products. First of all, the concentrated stress is generally to be found around their interface because of the different crystal structures between substrate and IMCs. In the full IMCs joints, solder layer has been consumed completely

which acted as a buffer layer in the conventional interconnection. Thus, the high stress will distribute through the whole connected area in full IMCs joints. Besides, the scaling down of the interconnected stand-off height (SOH) will change the constrained-state of micro-joints in the structure of devices, which has a serious relationship with mechanical property of micro solder joints [104]. Furthermore, in the multichip module (MCM), the gap between the chips is mainly determined by the SOH of the bump. The low SOH is likely to lead the severe voids formed during the standard underfilling process, and full IMCs joints have to experience the increased shear force on the joints from the surrounding thermomechanical stress [20, 105, 106]. Unfortunately, the poor mechanical properties of IMC have been discovered due to its brittleness [107], which would weaken the reliability of the interconnection considerably.

Byunghoon Lee [108] has fabricated the IMCs micro-joints with initial structure as Cu bump/10 μm thick Sn bonding layer/Cu bump through adding different pressure in the soldering process. In the following shear tests, a sudden increase of shear strength has been observed in the microjoints, where the structure was changed from Cu/IMCs (Cu_3Sn and Cu_6Sn_5)/Cu to the single Cu_3Sn joints. Nevertheless, more efforts are still needed to demonstrate systematically about the relationship between the microstructure and mechanical properties of these full IMCs interconnections.

(2) Electromigration Reliability

Electromigration (EM) is a mass transport phenomenon, which has been caused by multi-factors, such as electro wind force, Joule heating, and direct electrostatic force [109]. With the decreasing size of micro-bumps, the current densities will be higher in the working devices than before.

A Kelvin test structure was designed to investigate the performance of Cu-Sn IMCs interconnects in air and nitrogen ambient with testing temperature in the range of 175 ~ 350 °C [110]. The failure caused by EM was observed in these joints, as illustrated in Figure 2-15. The migration of Cu pad occurred together with the formation of voids, then the interruption of interconnection was generated as a result.

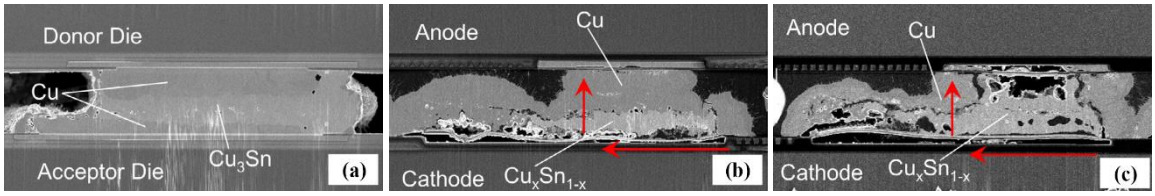

Figure 2-15 the failure of Cu_3Sn joints under EM testing (a) before testing, (b) the early failure (c) the final failure mode [110]

However, comparing with the conventional solder interconnects, a prominent EM resistance has been achieved on these bumps with the diameter of 25 μm and bump height of 10 μm, and the reason is that the bumps were transformed into Cu-Sn full IMC joints after soldering [111]. It has been found that the Cu-Sn IMCs micro-joints can sustain the current densities of 1.1×10^3 A/μm^2 for 1000 h at 200 °C, while the conventional solder joints have been damaged by the EM testing with 16 A/μm^2 at 120 °C after 137 h [112]. And more similar results have also been reported by other researchers [110, 113-115]. In a Chip to Chip structure, the IMCs micro-bumps were constituted with the middle layer Cu_6Sn_5 with the thickness of 4.8 μm, and two 2.6 μm thick Cu_3Sn layers on both side connecting with the Cu pads [116]. Both the experimental and modelling results under EM testing proved that the absence of Sn-solder can improve the reliability of the joints. Besides, the superior electromigration resistance of Ni_3Sn_4 IMC joints has also been discovered. The experimental result shows that when the current density of 596 A/μm^2 has been applied on the Ni_3Sn_4 IMC joints for 500 h under 150 °C, the

failure happen for the damage of Cu pads while the Ni_3Sn_4 interconnecting part was still intact [117]. The good performance of IMCs joints in EM test was contributed to the higher melting temperature of IMCs than the solder, as proposed in the references [118, 119].

Moreover, the Cu pillar bump interconnection was also found to have some advantages in EM test. Generally, the phenomenon of EM taking place in solder bump joints is attributed to the appearance of current crowding on the entering corner of solder bump, where the local high current density makes the solder migrated easily. However, in the Cu pillar bump interconnection, the crowned current can be redistributed within the whole Cu pillar before reaching the low-melting solder [118], as shown in the Figure 2-16. Therefore, it is reasonable to believe that when the Cu pillar bump interconnection transforms into full IMCs for the extended soldering time or elevated temperature, that kind of interconnection will perform an excellent EM resistance.

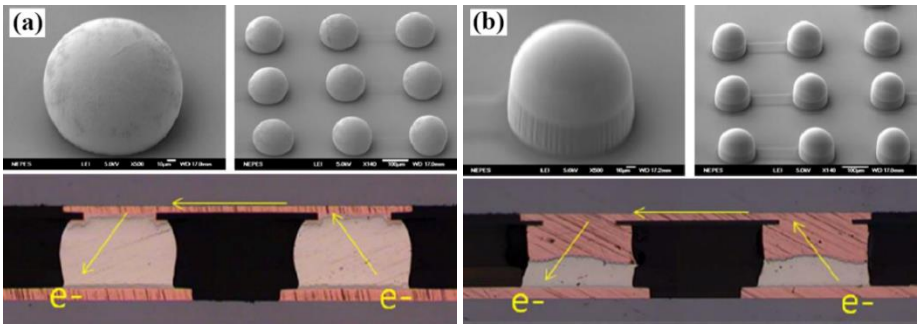

Figure 2-16 over-view of interconnects and the corresponding EM tests
(a) solder bump and (b) Cu pillar bump [118]

2.4 Summary

Compared with traditional C4 technology, micro-C4 and copper pillar bump provide the new promising methods to achieve the high density and fine or ultra-fine pitch interconnection in the MCM packaging. The manufacture process of the copper pillar bump is much similar with that of micro-C4 bump using the electroplating and evaporation method. However, the outstanding advantages of copper pillar bump including the ultra-fine pitch availability and high electromigration resistance make it been the most popular technology for the advanced interconnection.

The decreasing bump size and solder volume both in the micro-C4 and copper pillar bump has significantly increased the possibility of full IMCs interconnection, which is the main focus in this thesis. Although the type of Cu-Sn IMCs joint has been provided in the literature, more alternative connected formats are still needed for the miniaturized interconnection. And the issues about the acceptable and stable microstructure of IMCs for the final application have not been understood completely. Thus, more attention should be paid on the relationship between the microstructure and reliability of those full IMCs micro-joints.

Chapter 3 Experiment and Methodology

3.1 Preparation of IMCs interconnection

The sandwich structure as substrate/Sn-based solder/Cu pad is widely used to realize the interconnection in electronic packaging. Accompanying with the miniaturization in electronic industry, the scaling down of the interconnected height and pitch has become a great challenge for electronic integration. Thus, in this project, the micro-joints used for interconnection have been studied. The initial structure of interconnection was fabricated as substrate/Sn/Cu, as shown in Figure 3-1, where the method of continuous electroplating was applied. Firstly, a uniform and consistent Sn layer acting as the solder layer was electroplated on the polished substrate. Then, a Cu layer was plated on the top of the Sn layer as followed. In particular, the thickness of plated Cu layer should be thick enough to satisfy the requirement of converting the whole Sn layer into IMCs.

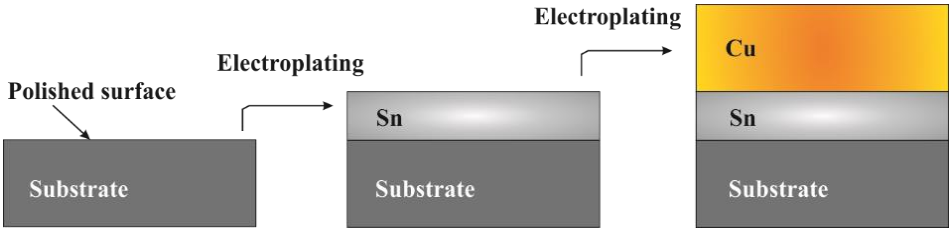

Figure 3-1 substrate/Sn/Cu structure prepared through the continuous electroplating method

3.1.1 Electroplating tin and copper

(1) Plating tin

The tin electroplating formula employed in this study was recommended by *MacDermid Company* [120] as shown in Table 3-1. Tinmac Stannolyte is a kind of acid solution which can produce the bright electroplated tin effectively. In details, this type of Sn electroplating solution was prepared in the procedure as following:

- The beaker was treated with the diluted sulphuric acid (2% concentration with water) and cleaned by water, then filled the beaker with deionised water.
- Poured the certain amount of sulphuric acid into the water with constant stirring.
- Dissolved the stannous sulphate in the solution.
- Added the Tinmac Stannolyte Initial and deionised water to the targeted volume of electrolyte.

Table 3-1 solution make up for electroplating tin

Solution Make Up	Stannous Sulphate SF41751 (50%)	Sulphuric Acid (pure) sp.gr. 1.84	Tinmac Stannolyte Initial EU 86305	Water (deionised)
Option 1	60 g	70 ml	40 ml	
Option 2	30 g	100 ml	50 ml	
Current density	1.5 to 2.0 A/dm^2 for Option 1; 1 to 1.5 A/dm^2 for Option 2.			
Voltage	1 to 5 V			to 1 L
Temperature	15~30 °C			
Rate of deposition	Average 10 μm in 11 mins at 2 A/dm^2			

Afterwards, a type of commercial rolled copper and nickel with 99.99 wt.% (degree of purity) were selected and used as the substrate. First of all, these substrates were polished well and cleaned with liquid detergent (*Fairy Original Washing Up Liquid*) to take away the general contamination. Then, used acetone solution to spray the surface and submerged the substrates in the acetone solvent under ultrasonic cleaning for 5 mins. After that, dried the samples with cold air. And secondly, the adhesive tape with chemical resistance from *3M Company* was chosen to cover the specific surface of substrate and thus only the effective area for electroplating was exposed. Before electroplating, the exposed surface of substrate was immerged into the diluted sulphuric acid (2% v/v) to take away the oxide, and cleaned by deionized water immediately. Finally, used one clamp to clip the certain holding area on copper foil, then put the sample into the electrolyte. Meanwhile, the other clamp clipped one piece of pure tin sheet with the thickness of 1.0 mm as anode, and the area of tin sheet is 1.5 times that of the plating surface on the cathode. After inserting the anode into solution, aligned it with the cathode, then the electroplating process was ready to start. The apparatus for electroplating is demonstrated as Figure 3-2.

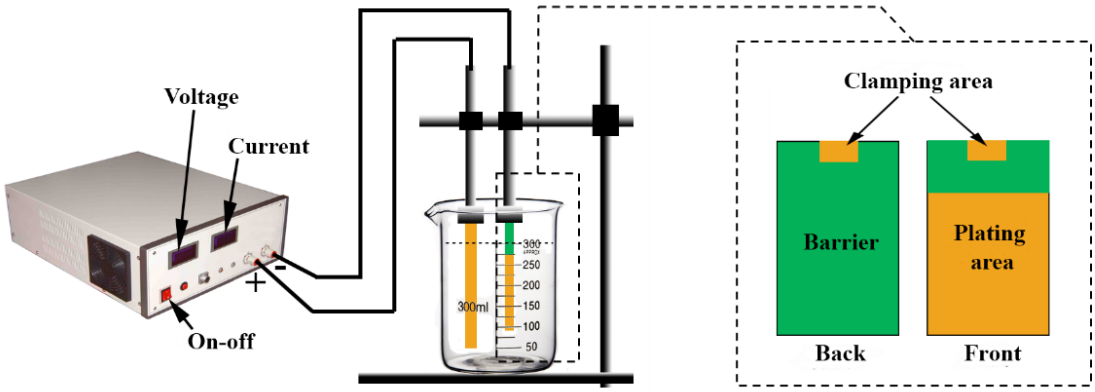

Figure 3-2 schematic images of the electroplating apparatus

In order to get the certain thickness of plated layer, the value of current density on cathode and plating time should be strictly controlled. And the voltage has to be high enough to guarantee the stability of current in the whole process. When the electroplating was finished, took out the sample, washed it by deionized water and dried by cooling wind.

(2) Plating copper

The copper layer is the essential part of the sandwich structure of micro-interconnect. It was also made by electroplating on the top of the plated Sn layer. In this case, the potential corrosion of the prior Sn layer causing by the copper plating solution should be considered significantly. Therefore, a kind of alkalescent electrolyte was selected for electroplating copper. The solution was prepared with the chemicals, which are given in Table 3-2. All the chemicals were brought from the *Sigma-Aldrich* or *Fisher Scientific Company*. The details of making up is clarified below:

- Added the specified amount of potassium pyrophosphate in deionised water at 40~50 °C to approximately 2/3 objective volume in the beaker.
- Dissolved the copper pyrophosphate and added water to the working volume.
- Dropped the 50% v/v sulphuric acid in the solution to adjust the pH value to 8.8.
- When the solution was cooled down to 50~55 °C, then added the diluted ammonia (50% v/v) as appointed.

It is worthy to emphasise that the agitation should be added when plating copper. If not, the quality of copper plated layer would not be good. Some dark dots appeared, which might be caused by current congregation along

with high temperature produced locally.

Table 3-2 solution make up for electroplating copper

Solution Make Up	Copper Pyrophosphate Trihydrate	Potassium Pyrophosphate	Ammonia 0.880 sp. gr.	Water (deionised)
Range	70~86 g	240~320 g	2~4 ml	
pH		8.6~9.2		
Current density		3.0~6.0 A/dm^2		to 1 L
Temperature		50~60 °C		
Rate of deposition		Average 10 μm in 11 mins at 4 A/dm^2		

3.1.2 Transient liquid phase (TLP) bonding

The TLP bonding is defined as a method, where a thin liquid interlayer is formed in the joint at bonding temperature, and then becomes solid isothermally. TLP bonding has been widely applied in heterogeneous metals, titanium alloys or aluminium alloys etc., which are difficult to join through conventional welding methods [121]. Many investigations have been carried out in that domain, however, the TLP bonding is still a relative new concept emerging for electronic packaging in recent decades [25, 122]. Accompany with the decreasing size of solder bump from hundreds to several micrometres, the interlayer of micro-joints (usually Sn-based solder) is more likely to be consumed completely and the full IMCs interconnection is obtained in the soldering process. This metallurgical process is thus described as the TLP bonding. In the conventional reflow stage, the highest temperature is about 250 °C and little time upon the melting point of solder is kept to prevent the aggressive growth of IMC layer [123]. Whereas, in the TLP process, the samples can be sharply heated up to a relatively high bonding temperature in the range of 275~350 °C, compared with the melting point of tin (232 °C). Afterwards, a long time dwelling at the bonding temperature is needed to make sure the fully reaction between copper and tin [124]. In general, several stages can be divided for the TLP bonding process as illustrated in Figure 3-3.

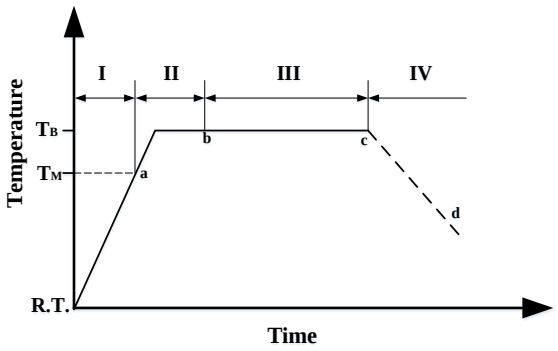

Figure 3-3 different stages of TLP bonding process (R.T.-room temperature, T_M-the melting point of solder, T_B-the bonding temperature)

Stage I: The temperature is increased from room temperature to the melting point temperature of solder. And the heating rate is important to determine the minimum require of the interlayer thickness. During this stage, interdiffusion is started between the solder and Cu pad (and substrate).

Stage II: As the temperature is elevated to be higher than the melting point of solder, the solder turns to be liquid. The Cu pad (and substrate) around the contact interface will dissolve in the liquid solder. Once the concentration is satisfied to form the IMCs, the solidification will happen gradually. At the end of this stage, the liquid solder will disappeared and transformed into solid IMCs totally.

Stage III: The homogenization occurs immediately after the isothermal solidification. As the diffusion-controlled mechanism is predominant, the distribution of elements is related with distance from interface. After this stage, the microstructure of interlayer will become consistent and stable.

In order to get a qualified joints, the parameters of TLP bonding process should be optimized. When one kind of Sn-based solder is chosen to be interlayer, the suitable bonding temperature, heating rate and the enough dwell time at bonding temperature all need to be considered carefully. Particularly, there are two major kinds of IMCs (Cu_6Sn_5 and Cu_3Sn) existed during the TLP bonding of Cu pad (substrate) and Sn-based solder, which should be paid more attention to get a good full IMCs micro-joint.

3.1.3 Formation of IMCs interconnection

Two types of ovens have been used, as shown in Figure 3-4. Aiming to make samples with full IMC directly, the profile of TLP soldering was set up in T-track oven shown in Figure 3-5(a). A thermocouple was applied to double check the temperature on the area where the samples had been placed in the T-track oven. The heating rate was 50 °C/min, and a short keeping stage was added with 2 mins around 200±2 °C, before the temperature reaching the melting point of Sn solder (T_M=231 °C). Then, different bonding temperature (T_B) was specified as 240±2 °C, 260±2 °C and 290±2 °C respectively to prepare different groups of samples. In order to investigate the effect of dwell time at bonding temperature on the microstructural evolution of micro-joints, the samples were took out from oven after experiencing different dwell time (0/5/15/25 mins), then all these samples were quenched in cold water. Those samples have been applied in Chapter 5 and Chapter 7.

Beside, a vacuum chamber was also selected to reduce the influence of oxidation. Parts of specimens were soldered in the vacuum chamber at 260±2 °C with 93 KPa absolute pressure, and followed by an isothermal storage process with different dwell time (10/30/50/70 mins) as illustrated in Figure 3-5(b). Finally, the specimens were removed from the vacuum chamber and cooled down to room temperature (R.T.) in air. This soldering process can also be described as TLP method. Since the heating rate is quite slow compared with the T-track oven, these specimens were mainly applied for the study on isothermal homogenization of IMCs micro-joints, which have been observed and analysed in Chapter 4 and Chapter 6.

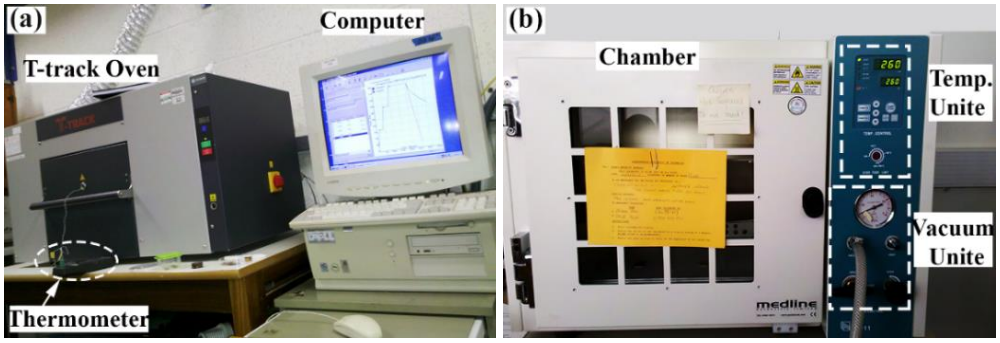

Figure 3-4 images of two types of ovens used in experiment (a) T-track oven (b) vacuum oven

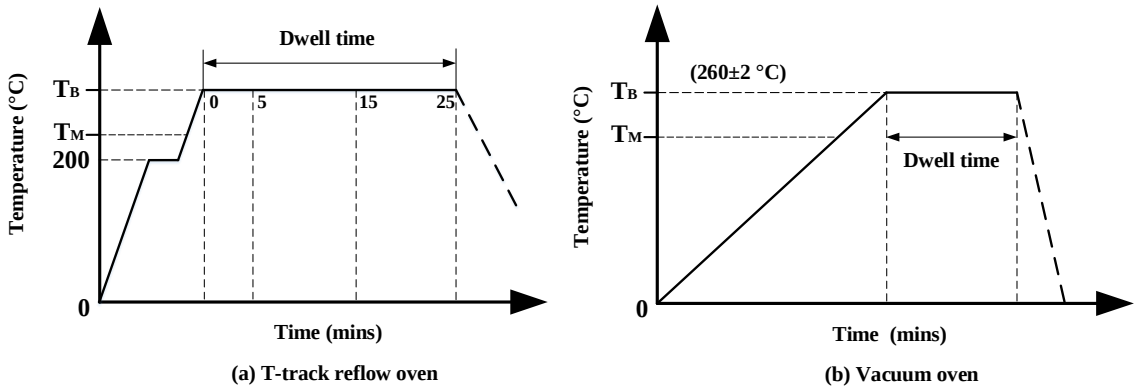

Figure 3-5 TLP profiles used in T-track reflow oven and vacuum chamber

3.2 Metallographic observation and analysis

3.2.1 Metallographic sample preparation

After soldering, most of the samples turned to be full IMCs joints, where the melting points temperature of IMCs are 415 °C for Cu_6Sn_5 and 676 °C for Cu_3Sn. To conveniently observe the cross-section of micro-joints, samples were mounted in epoxy resin. This cold mounting approach does not need an external heating source and the temperature is less than 80 °C during the whole solidification process. It can be guaranteed that the mounting process has not brought any interference on the microstructure of samples. Afterwards, the general grinding procedures were carried out on the abrasive papers, and then these cross-sections of samples were polished well in assistance of polishing slurry with Al_2O_3 particles of 1 μm diameter.

In order to improve the conductivity of mounted samples, sputtering a very thin gold layer on the observed surface was required as the pre-treatment. Then, the cross-section were ready to observe by field emission gun-scanning electron microscope (FEG-SEM). However, the mounted samples were not suitable for further analysis in focus ion beam (FIB) machine, since the peripheral resin will block the ion beam in the remachined process. Therefore, some of samples were clamped tightly by a designed metal holder to solve this issue. When the grinding and polishing work was finished, these samples can be took out easily from the metal holder.

3.2.2 Microstructural characterization and analysis

(1) Microstructural observation

Because the stand-off height of IMCs micro-joints were in the range of 1~6 μm, and the thickness of each IMC layer would be less than 1 μm sometimes, thus FEG-SEM (*Carl Zeiss (Leo)-1530VP* and *Nova NanoSEM 450*) was chosen to observe the cross-sectional characteristics of micro-joints, and three main functional modules have been used:

- Back-scattered electron (BSE) imaging: In order to capture images with high quality, BSE enables to enhance the contrast between different phases, which was preferred to distinguish the different layers of IMCs on cross-section rather than the high resolution secondary electron (SE) mode.
- Energy dispersive X-ray (EDX) analysis: To check the component of IMCs and the amount of each element changed with distance in micro-joint, three different detection modes were used, such as point, line scan and mapping.
- Electron backscattered diffraction (EBSD): On the basis of the microstructural-crystallographic technique,

EBSD can be applied to determine the phase distribution, lattice orientation, grain boundaries, and etc.[125, 126]. Besides, it can also be used to measure the grain size, observe the slip system and analyse the fracture with practical resolution less than 1 μm [127]. Nevertheless, the specimen preparation for EBSD is critical, thus the ion milling was proposed to furnish the observed surface by FIB technique [128, 129].

(2) X-ray diffraction

X-ray diffraction (XRD) is a powerful method to provide some quantitative structural information of materials, such as the lattice parameters, crystal structure, phase identity, grain size, and etc. In the project, this approach was applied to identify the types of IMC phases in Chapter 6 and Chapter 7, using the machine *XRD-7000s, Shimadzu, Japan*. After removing the top Cu layer by polishing, the XRD detection with a copper target was conducted in the top view at 40 KV, 30 mA and 3°/min to obtain the spectrum in the range of 20°~80°, and by following the indexing procedure the IMC phases were identified using MDI/Jade6 software.

3.3 Measurement of IMCs mechanical properties

Nanoindentation was applied to measure the Young's modulus and hardness of IMCs at room temperature, using *Hysitron TI750 Ubi system* [130] with force and displacement resolutions of 3 nN and 0.006 nm, respectively. And a Berkovich triangular-pyramidal indenter was used. In this part, the top Cu layer of the sandwich-like Cu/IMCs/substrate samples were removed by polishing. Then, the interesting IMC layers were exposed for the indenter loading along the perpendicular direction. As the thickness of different IMCs layers was only 1~2 μm in micro-IMCs joints, the multiple loading with displacement control method was selected to conduct the testing to avoid the effect of substrate. Therefore, the loading curve was set up as Figure 3-6(a), with 20 times loading cycles within 60 s and the maximum loading depth of 200 nm. For each IMC layer, 3~6 points were tested.

As a comparison, the similar measurement has been implemented on the Cu plated layer and Ni substrate. Both of them were thick, and then the conventional loading method with force control was used to complete the test, as shown in Figure 3-6(b). The time for loading and unloading process are the same as 5 s, while the constant force is 2000 μN for Cu and 5000 μN for Ni with dwell time of 2 s. Except of that, the creep properties of IMCs has also been evaluated at room temperature with the condition of 2000 μN loading for 30 s.

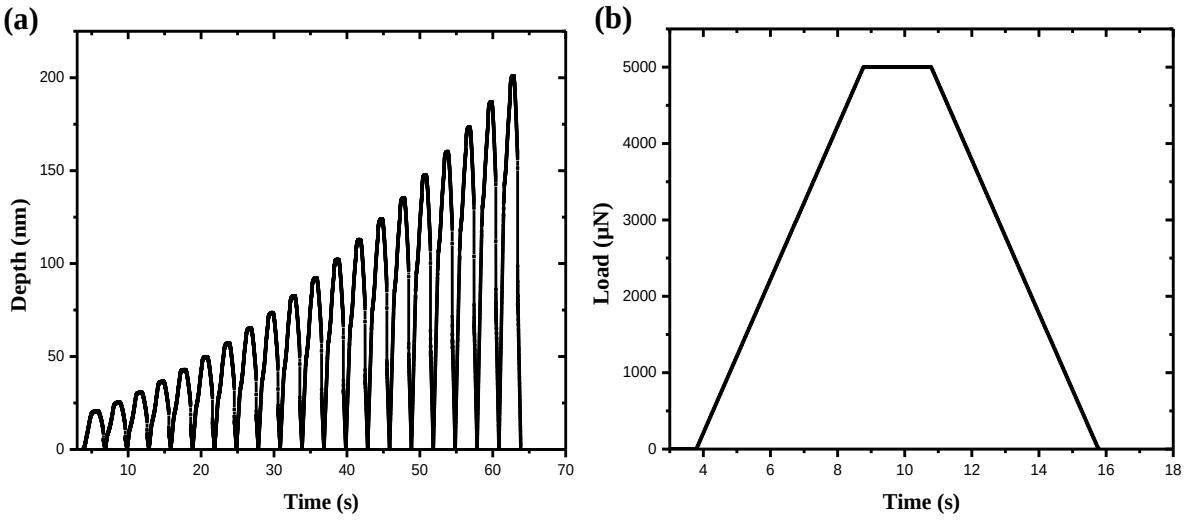

Figure 3-6 the loading curves applied in nanoindentation test (a) multiple loading with displacement control, (b) loading with force control

3.4 Micro-mechanical testing

3.4.1 Fabrication of micro-cantilever by FIB

In this project, three types of micro-cantilevers were fabricated by FIB micromachining (*FEI-Nova 600 Nanolab Dual Beam*). The first type of micro-cantilevers (Type I) was designed along the perpendicular direction, which can reveal the interface between two phases conveniently. The size of this micro-cantilever is around 5 μm×5 μm×10 μm. In order to guarantee the height of the micro-cantilever and make sure the interesting area exposed, the processing sequence of micro-milling by FIB should be considered seriously and illustrated in Figure 3-7. At the beginning, a thin Pt layer of 1.5 μm was deposited on the top of Cu-plated layer to protect the micro-cantilever from damage by ion beam. In the fabrication stage, the value of current is a critical factor to determine the processing speed and the roughness of the machined surfaces. While the voltage of ion beam was 30 KV, the current of 20 nA was applied to conduct the primary milling of the parts ① ② ③ shown in Figure 3-7(b), and then rotated and tilted the sample, the current of 7 nA was used to cut the part ④ in Figure 3-7(c). Finally, all the machined surfaces of micro-cantilever were re-treated by ion beam of 1 nA to be more smooth. In the later shearing test, the indenter will be loaded from horizontal direction as shown in Figure 3-7(d).

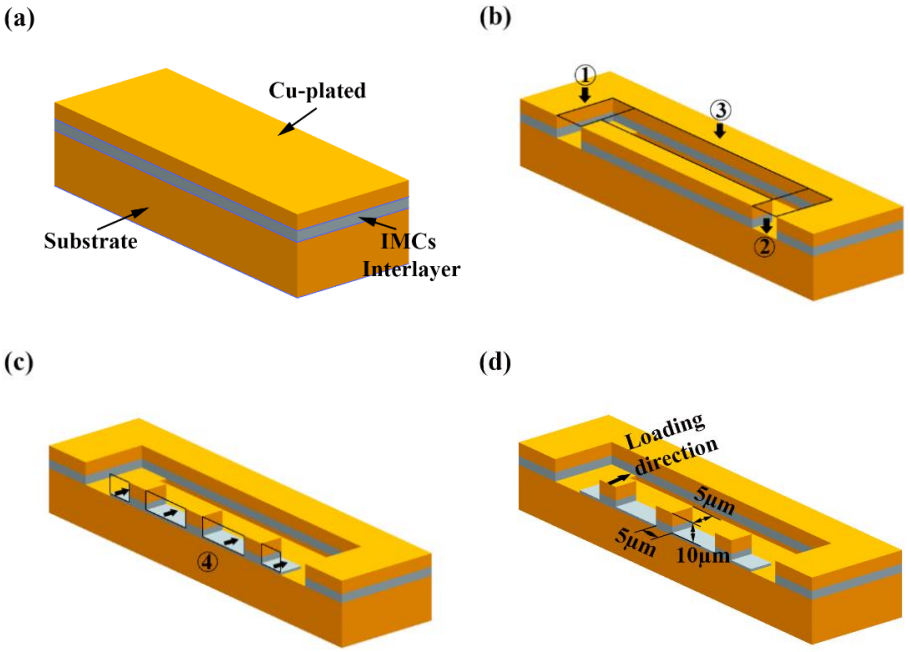

Figure 3-7 processing sequence of micro-cantilever used for shearing test (Type I)

The second type of micro-cantilevers (Type II) was within the IMCs interlayer along horizontal direction, about 1 μm×1 μm×3 μm. The fabrication process by FIB is shown in Figure 3-8. First, ion beam milling with the current of 7 nA was used to remove the Cu plated layer and substrate surrounding IMCs interlayer (parts ① and ②); and next, the platform was rotated and tilted to cut off the area of part ③ and polished the surfaces with low current values of 2.8 nA and 93 pA in sequence. Then rotated the tilted the sample again to smooth the other two sides of micro-cantilever with 93 pA ion beam current as demonstrated in Figure 3-8(c). For the mechanical test, the nano-compression force will be loaded along the length of this IMC micro-cantilever.

The third type of micro-cantilevers (Type III) was fabricated for the in-situ nano-bending test (~1 μm×1 μm×5 μm), the structure and manufacturing procedure of which are projected in Figure 3-9. For the start of machining, ion beam of 7 nA was selected to etch the area ① and ② in the direction perpendicular to the substrate. After

that, the low current of 2.8 nA was used to remove the parts ③ and ④ in Figure 3-9(b), and then the final cutting and refining work was followed with the current of 93 pA. To accomplish the nano-bending test, the imposed load will come from the vertical direction as indicated in Figure 3-9(d).

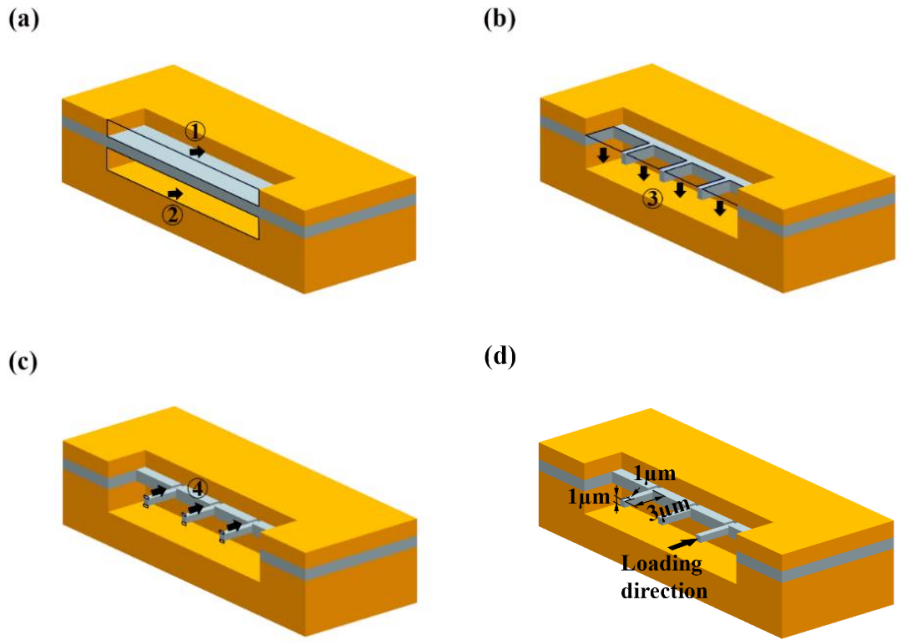

Figure 3-8 processing sequence of IMCs micro-cantilever for nano-compression test (Type II)

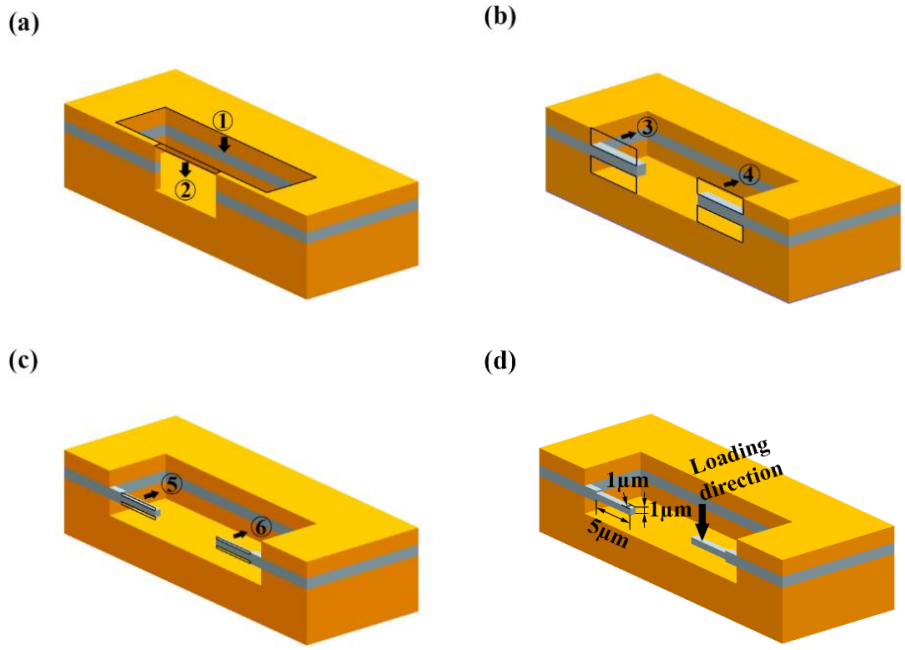

Figure 3-9 processing sequence of IMCs micro-cantilever for nano-bending test (Type III)

3.4.2 Micro-mechanical tests

Two equipment were employed to fulfil the micro-mechanical tests. The characteristics of each machine and the corresponding application are listed in Table 3-3. In consider of the low magnification of optical microscopy

mounted in *Micro Materials Nano Test600*, this machine was used to complete the shearing test on the micro-cantilevers with relative large size (~5 μm×5 μm×10 μm). However, it is difficult to align the indenter onto micro-cantilevers with the width of 1 μm precisely. Therefore, the *Hysitron PI 87 SEM PicoIndenter* which can be installed in FIB/SEM chamber, was applied to conduct the in-situ nano-compression/ nano-bending tests on the tiny micro-cantilevers.

Table 3-3 characteristics and corresponding application of the micro-mechanical testing equipment

Model	Characteristics	Application
Micro Materials NanoTest 600	• Optical microscopy • Translation stages: X, Y, Z • Flat indenter size: 5 μm×5 μm • Loading direction: Horizontal • Loading range: 0~500 mN • Maximum displacement: 20 μm	Shear testing on the micro-cantilever of ~5 μm×5 μm×10 μm for Chapter 6
Hysitron PI 87 SEM PicoIndenter [131]	• FIB/SEM • Degrees of freedom: X, Y, Z, Tilt, Rotation • Flat indenter size: 5 μm×5 μm • Loading direction: Horizontal • Loading range: 0~30 mN • Maximum displacement: 5 μm	In-situ nano-compression/ nano-bending on the micro-cantilever of ~1 μm×1 μm×3 μm ~1 μm×1 μm×5 μm for Chapter 7

Chapter 4 Planar Growth of IMCs in Cu/Sn/Cu and Ni/Sn/Cu Sandwich Structures

4.1 Introduction

Soldering with Sn-based solder for interconnection has played a vital role in the electronics manufacturing industry. And the growth of intermetallic compounds (IMCs) during the soldering process can provide a potential proof for robust bonding as the metallurgical reaction happened. Therefore, the growth dynamics of Cu-Sn IMCs have been widely studied, representing a parabolic relationship with time during the isothermal aging process [132, 133]. Besides, different kinds of material migration behaviours have also been observed in the joints, such as the growth of tin whiskers [134-136], electro-migration, and thermo-migration [137] or the migration caused by stress [138]. These behaviours could possibly impact the reliability of electronic devices, causing the short circuit between the joints, rapid dissolution of copper pads and some voids or cracks in the joints [139, 140]. However, these previous studies mainly focused on the vertical growth of IMCs, which is perpendicular to the Sn-based solder/Cu pad interface. Since the miniaturization of electronics constantly promotes the diminution of the interconnecting height and the pitch between joints, the growth process of IMCs becomes much more critical to decide the reliability of interconnections directly and predominantly. Therefore, not only is the growth of IMCs on the vertical direction important, the planar growth of IMCs also requires more attentions and should be studied comprehensively.

4.2 Experimental procedures

4.2.1 Sample preparation

Two kinds of initial structures were designed to prepare the micro-joints. One is a basic sandwich structure as (Cu or Ni) substrate/Sn/Cu in Figure 4-1(a). In this situation, 99.99 wt.% pure copper (or nickel) foil with size of 30 mm×15 mm×1 mm (0.125 mm) was selected as substrate. Then, the uniform and consistent Sn layer with the thickness of 2.5 μm or 5 μm, which will serve as bonding solder, was placed on the Cu substrate through electroplating method. Subsequently, a Cu layer with thickness of 10 μm was plated on the top of the Sn layer, which is thick enough to satisfy the requirement of Cu-Sn reaction, even if the Sn layer transforms into IMCs completely. To study the morphologies in these structures, the samples were firstly cross-sectioned through a metallographic grinding and polishing procedure. After that, FIB was employed to further clean the cross-section before soldering.

Moreover, in order to better simulate and investigate the interconnection environment in the miniaturized devices, another initial structure as the Cu/Sn/Cu micropillars were fabricated by FIB. The diameters of these micropillars were designed as 5, 10, 15 (±2) μm, respectively. Finally, all these samples were soldered in a vacuum chamber with bonding temperature of 260±2 °C and dwell time of 30 mins. After the soldering process, the interfacial reaction between Cu and Sn happened, and the IMCs (Cu_6Sn_5 and Cu_3Sn) were expected to form.

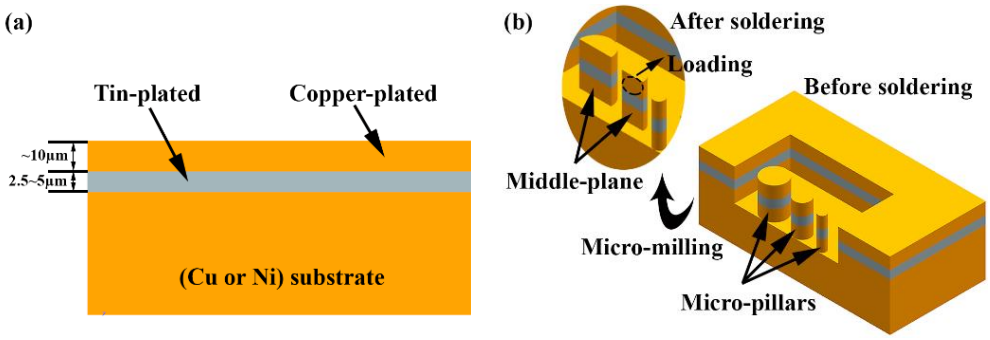

Figure 4-1 (a) schematic diagram of (Cu or Ni) substrate/Sn/Cu structure; (b) micropillars remachined by FIB

4.2.2 Testing and analysis

With the help of the micro-milling function of FIB, the inner structure of these micro-joints was exposed and observed after soldering process. Crystalline property of IMCs on the middle-plane was analysed by EBSD. Using a nanoindentation system (NanoTest 600, Micro Materials Ltd, UK), the mechanical test on the semi-micropillar joints was performed with the loading rate of 0.02 mN/s, as illustrated in Figure 4-1(b). After the mechanical testing, the fracture surfaces were observed by FEG-SEM while the components were detected by the module of EDX.

4.3 Results and discussion based on Cu/Sn/Cu structure

4.3.1 Macro-scale planar growth of IMCs

The cross-section morphology of Cu/Sn (2.5 μm)/Cu sandwich structure is shown in Figure 4-2(a), some copper-rich phases emerged in the Sn layer. After soldering, a two-layer structure was observed apparently in Figure 4-2(b), indicating that the IMCs not only grew up perpendicular to the Cu/Sn interface, but also on the planar direction (perpendicular to the cross-section). These two layers were constituted with the cobblestone-like product, grown up from two Cu-Sn interfaces toward each other. Moreover, tin oxide was found to cover the top surface of these two layers. Especially, as shown in Fig. 4-3(a), when the thick covering of tin oxide did not form, the planar growth of IMCs was more exuberant, and some rod-like IMC grains were also obtained. The EDX result of the marked point indicates that the IMC grains were mainly Cu_6Sn_5.

Meanwhile, the similar phenomenon was also observed in the Cu/Sn (5 μm)/Cu structure. There are some Sn-rich substances covering the surface, and the content of Sn can be up to 86.4 at.% in the selected location as white-line rectangle marked in Figure 4-4(a). When the covering was peeled off, the cobblestone-like Cu_6Sn_5 grains underneath can be recognized clearly, and the average size of these Cu_6Sn_5 grains is approximately 2 μm. Moreover, a deep cleaning method has carried out to study the cross-section of interconnection further. These samples have been etched in dilute (5% v/v) HCl-methanol solution with ultrasonic for 5 mins. As a consequence, both the covering and Cu_6Sn_5 IMC were taken away, and then the Cu_3Sn IMC with fine grains emerged from the cross-section, as exhibited in Figure 4-4(b). This layered structure implies that the growth behavior of IMCs along the planar direction is also affected by the copper diffusion distance, which is the same as the situation along the vertical direction in the Cu-Sn sandwich-like joints.

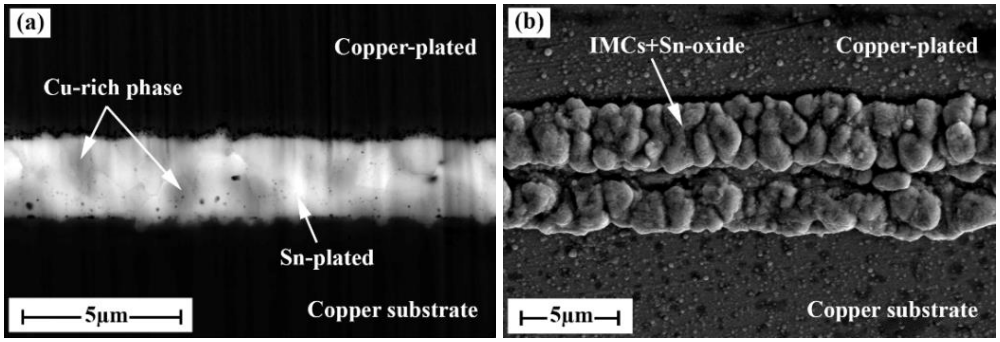

Figure 4-2 morphology of Cu/Sn (2.5 μm)/Cu cross-section (a) before soldering, (b) after soldering

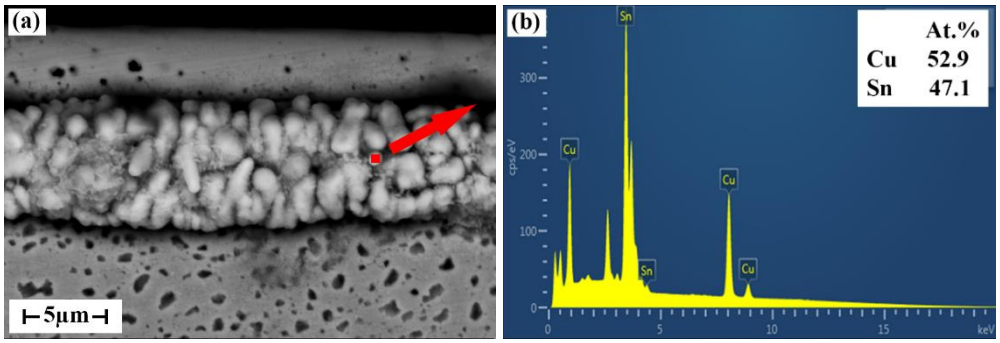

Figure 4-3 (a) morphology of soldered Cu/Sn (2.5 μm)/Cu without oxide covering and (b) the EDX result

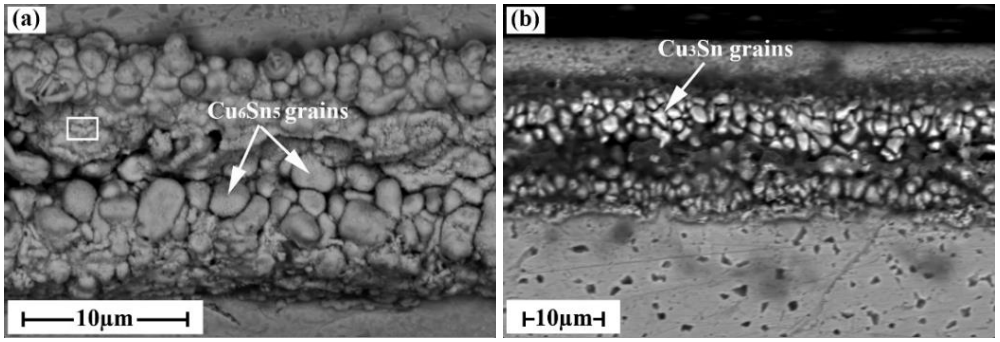

Figure 4-4 morphology of IMCs planar growing in soldered Cu/Sn (5 μm)/Cu structure
(a) the cobblestone-like Cu_6Sn_5 grains, (b) fine Cu_3Sn grains after ultrasonic clean

In addition, it is worth noting that some whiskers appeared on the cross-section of joints in Figure 4-5, especially on the interface between IMC and copper layer or around the defects area (such as voids). The maximum length of these whiskers are approximately 4 μm, which is unacceptable in the fine-pitch interconnection for the high risk of short circuit. Further analysis by EDX mapping on the cross-sections are shown in Figure 4-5(b, d), where the whiskers are displayed as copper-rich compounds. More details on the constitutions of these whiskers provided by EDX results on some certain locations are listed in Table 4-1. Comparing with the content of copper on the general surfaces which is 53.5 at.% on the point II, the ratio of copper element in these whiskers is much higher, even up to 81.1 at.%. Also, a large amount of oxygen in whiskers within the range of 15 at.% to 40 at.% was detected, since the samples were soldered in the vacuum chamber with a relative low vacuum degree and high temperature. Meanwhile, small quantity of tin atoms was existed in the whiskers here, and the general surface of original Sn-oxide covering possessed the much higher amount of tin atoms. Therefore, these Cu-rich whiskers can be regarded as the copper-oxide whiskers which are similar to the ones observed by Barbara [141] on tin-copper alloy coating surface. The whiskers in Barbara's study were produced by the corrosion of Cu_6Sn_5 IMC under the high temperature and humidity, the related chemical reactions were conducted in the form of

equations (4-1) and (4-2). Then the whiskers were identified as a mixture of pure Cu, Cu_2O and SnO_x.

Generally, the growth of whiskers is supposed as the result of the stress releasing process. Many potential factors would increase the compressive stress in the joints inside, leading to the formation of whiskers. These factors might include the stresses induced by electroplating process, thermal stress produced for the mismatch of CTE (coefficient of thermal expansion) between the copper and IMCs in high temperature, and also some stresses caused by the diffusion of atoms and the volume change during the growth and ripening process of IMCs [142-145]. Then, the Cu-rich substance penetrated through the weak covering, and finally forming the whiskers. However, no whiskers were observed after soldering process in the samples with initial structure Cu/Sn (5 μm)/Cu. The possible reason is that the average inner stress tends to be less in the joints for the higher interconnecting height. As a result, there are not enough stress concentration in those joints to motivate the growth of whiskers.

$$Cu_6Sn_5 + \frac{13}{2}O_2 \rightarrow 5SnO_2 + 3Cu_2O \tag{4-1}$$

$$10Cu_2O + Cu_6Sn_5 \rightarrow 26Cu + 5SnO_2 \tag{4-2}$$

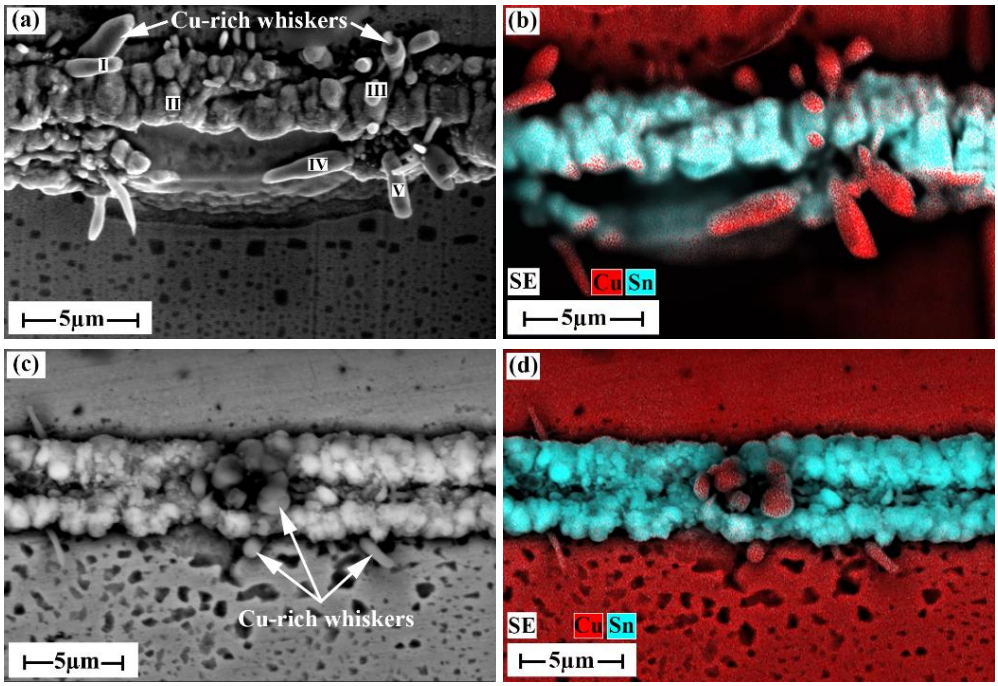

Figure 4-5 planar growth of whiskers in Cu/Sn (2.5 μm)/Cu structure after soldering (a) SEM image on one area, (b) EDX map of (a), (c) SEM image on the other area, and (d) EDX map of (c)

Table 4-1 the EDX results for some certain locations in Figure 4-5(a)

Element (at.%)	I	II	III	IV	V
Cu	81.1	53.5	64.2	75.5	79.2
O	15.7	18.3	20.0	18.2	18.4
Sn	3.3	28.2	15.8	6.2	2.4

4.3.2 Micro-scale planar growth of IMCs

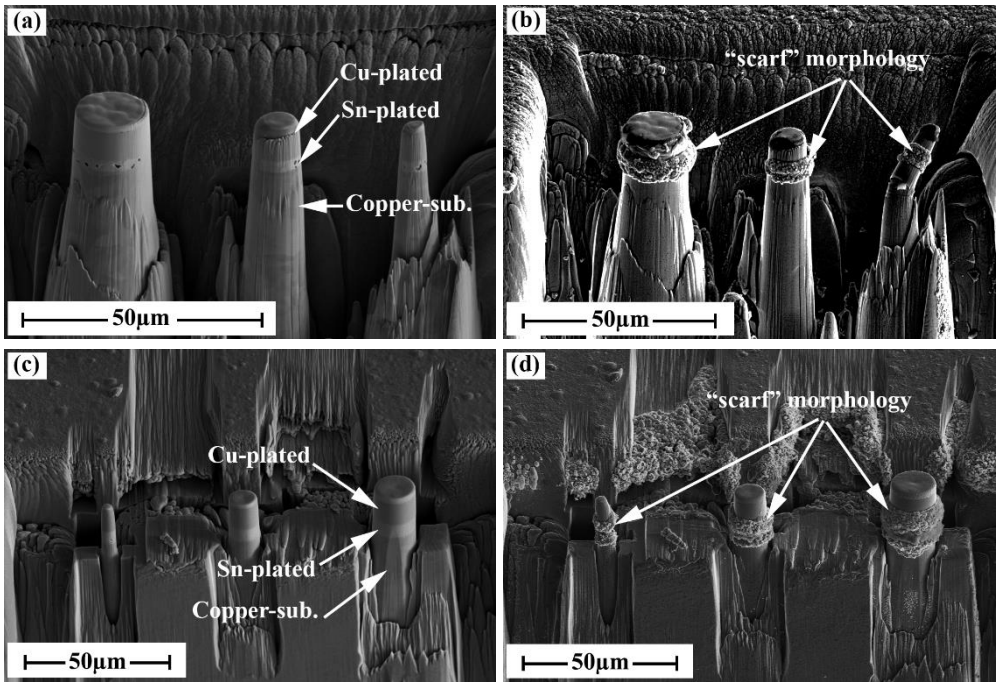

Figure 4-6 two types of micropillars with different diameters before and after soldering (a, b) Cu/Sn (2.5 μm)/Cu; (c, d) Cu/Sn (5 μm)/Cu

Micropillars were fabricated by FIB from the initial sandwich-like samples with the structures of Cu/Sn (2.5 μm)/Cu and Cu/Sn (5 μm)/Cu as shown in Figure 4-6(a) and (c). After soldering, all of micropillar-joints look like being tied with a neck-scarf, which can be observed in Figure 4-5(b) and (d). It means that the planar growth of IMCs occurred during the soldering process, no matter what diameter of the micropillar was. In order to observe the inner side of these micropillar-joints, a re-machining process has been conducted by FIB on micropillar of 15 μm diameter with initial Cu/Sn (2.5 μm)/Cu structure, following the processing steps as depicted in Figure 4-7. Firstly, the peripheral neck-scarf product was removed by FIB. Then, the micropillar looks much smooth and some micro-voids are distributed irregularly in the connected layer. Next, in step2, a half of micropillar was cut away to reveal the inner structure of the micropillar. Then some much bigger voids were found to exist on the cross-section of the semi-micropillar. Besides, the white dotted-line rectangular area in Figure 4-7 was analysed by EBSD, it is evident that the element of copper and huge voids have occupied the interconnecting area of the joint mainly. And the similar result was observed on the semi-micropillar of 10 μm diameter with initial Cu/Sn (5 μm)/Cu structure, as shown in Figure 4-8.

All the phenomena described above indicate a massive material migration occurred during the micropillars soldering process. Because of no constrains existing around the interconnecting part on the planar plane, these low energy free-surface provided the priority for internal stress release. Then, the molten tin flowed from inner side of the pillar to the peripheral area at the beginning of soldering, as illustrated in Figure 4-9. Thereby, the "scarf" morphology formed, leaving some voids or cavity inside. However, some Cu-Sn compounds were also formed at the same time based on the diffusion of Cu atoms into the molten tin layer, and stayed in the inner side of micropillars to the end. With the dwell time increasing, the Cu atoms were kept diffusing into the tin-plated area because of the driving forces of chemical reaction and concentration gradient. At the end, the Cu-Sn IMCs formed around the peripheral area of micropillars showing the characteristic of Cu-Sn reaction along the planar direction. And the Cu-Sn compounds in the middle of micropillar transformed into Cu-rich phase ultimately.

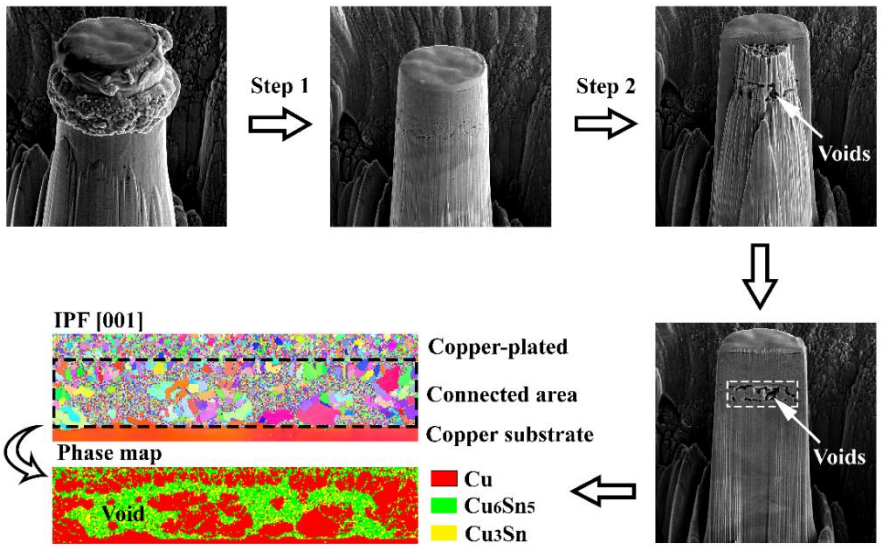

Figure 4-7 FIB remachining on soldered Cu/Sn (2.5 µm)/Cu micropillar and EBSD observation on the white dotted-line rectangular area

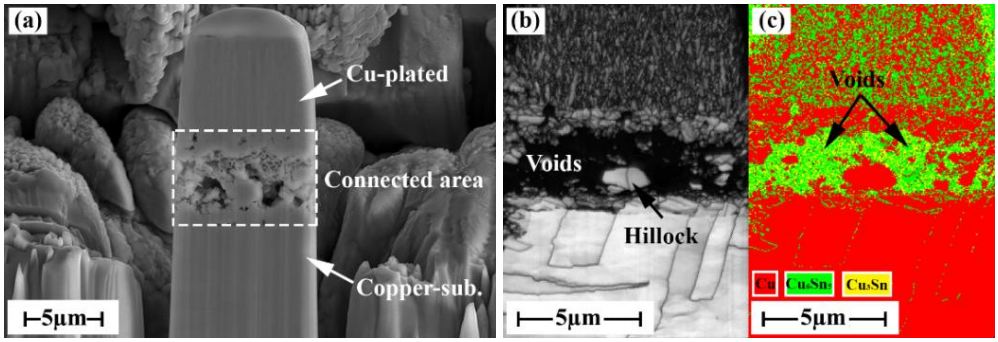

Figure 4-8 (a) mid-plane of soldered Cu/Sn (5 µm)/Cu micropillar of 10 µm diameter; (b) EBSD observation on the white dotted-line rectangular area; (c) phase map of (b)

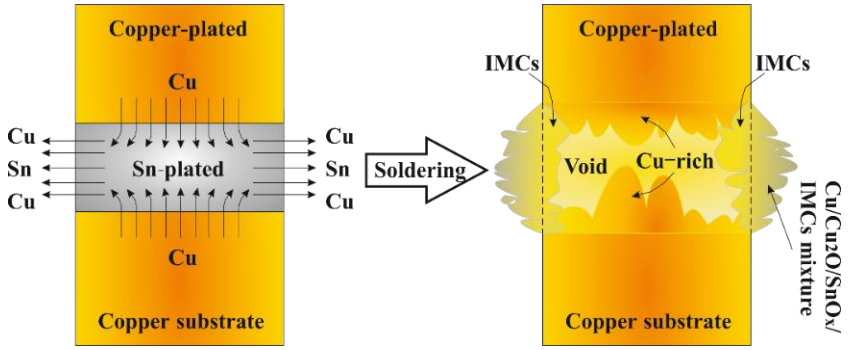

Figure 4-9 diffusing paths of atoms in Cu/Sn/Cu micropillar and the final structure after soldering

4.3.3 Mechanical testing by nano-indentation

A mechanical test has been carried out on the soldered semi-micropillar joints (mentioned in 4.3.2) by a nanoindentation machine. Figure 4-10(a) demonstrates the fracture image of the semi-micropillar produced from Cu/Sn (5 µm)/Cu micropillar of 10 µm diameter. Apparently, there is a hillock surrounded by some huge voids around, located in the middle of the joint along the vertical direction, which means only the peripheral connection

has been achieved. And the components at two individual locations were detected by EDX. Point I is found to be Cu-rich component (97.2 at.% Cu; 2.8 at.% Sn), while the component at point II is supposed to be Cu_3Sn, considering with the EDX results of 73.3 at.% Cu and 26.7 at.% Sn. In addition, the mechanical test result in Figure 4-10(b) shows that, the semi-micropillar fractured suddenly when the loading force only reached 0.1 mN. It is also proved that the extraordinary material migration in the joints along planar direction has weakened the mechanical property of the micropillar interconnection.

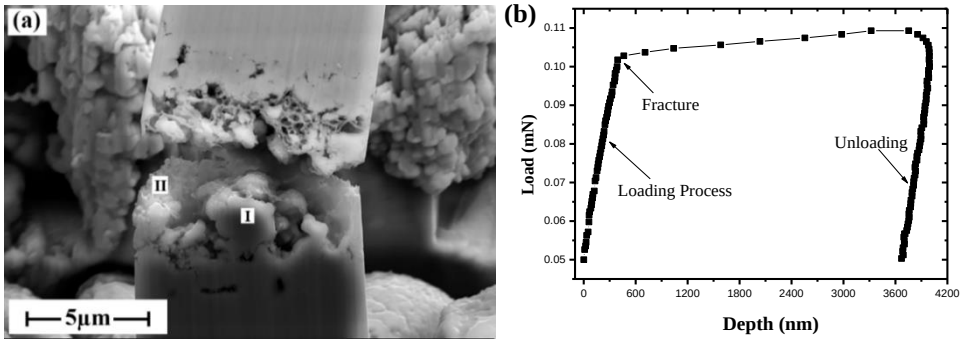

Figure 4-10 (a) fracture image for semi-micropillar produced from Cu/Sn (5 μm)/Cu micropillar after soldering, and (b) the loading-depth curve produced by mechanical testing

4.4 Macro-scale planar growth of IMCs in Ni/Cu/Sn structure

The similar phenomenon of planar growth of IMCs was also observed in the Ni/Sn/Cu structure after soldering, as shown in Figure 4-11. The EDX result from the sample with initial Ni/ Sn(~2.5 μm)/Cu structure shows that the whole interlayer of micro-joint was detected to be $(Cu,Ni)_6Sn_5$ along the planar direction except the Sn-oxide covering on the surface. In contrast, the asymmetric planar growth was observed on the two different interfaces in the sample with initial Ni/Sn (~5 μm)/Ni structure. Obviously, the planar growth of IMCs at the Cu/Sn interface was faster than that around the interface between Sn and Ni substrate. It is the similar tend as the previous reports [146] for the general perpendicular growth of IMCs that $(Cu,Ni)_6Sn_5$ appeared on the Ni-side instead of the Ni-Sn IMCs because of the low reaction rate of Ni-Sn in the Ni/Sn/Cu joints. The growth of $(Cu,Ni)_6Sn_5$ on Cu-side was accelerated by the diffusion of Ni element, called as the cross-interaction [69]. Moreover, it is interesting to find that a gap between the two interfacial IMCs on planar direction has formed, where are also supposed to be $(Cu,Ni)_6Sn_5$. And the content of Ni in there three parts of interlayer was decreased with the increasing distance versus Ni substrate, as shown in Table 4-2.

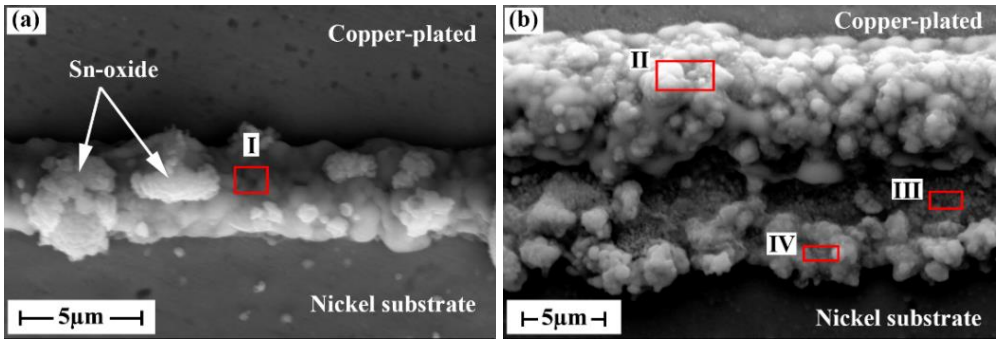

Figure 4-11 morphologies of the two Ni/Sn/Cu structures after soldering
(a) Ni/Sn (~2.5 μm)/Cu; (b) Ni/Sn (~5 μm)/Cu

Table 4-2 the EDX results for certain area in soldered Ni/Sn/Cu structure

Elements (at.%)	I	II	III	IV
Sn	52.9	52.8	57.9	50.7
Cu	44.6	46.3	38.5	34.4
Ni	2.5	0.9	3.6	14.9

4.5 Summary

In this chapter, the planar growth behaviour of IMCs in macro-scale Cu/Sn/Cu and Ni/Sn/Cu plane structures and the corresponding micropillars has been studied. In comparison with the vertical growth of IMCs in micro-joints, the characteristics of IMCs planar growth can be summarized as below:

(1) The IMCs planar growth behaviour existed in the Cu/Sn (2.5 μm or 5 μm)/Cu plane structure after soldering. The cobblestone-like Cu_6Sn_5 grains and fine-size Cu_3Sn grains underneath were detected on the cross-section of samples. It indicates that the growth of IMCs has promoted the migration of material in the planar direction. And some Cu-rich whiskers appear in the samples with initial Cu/Sn (2.5 μm)/Cu sandwich structure, which is likely to lead the short circuit between joints in the fine-pitch application.

(2) The "scarf" morphology was observed around the interlayer of Cu/Sn (2.5 μm or 5 μm)/Cu micropillars after soldering, and a huge cavity in the joint inside was formed as a result. The massive migration of substance along planar direction was caused by the atomic diffusion, chemical reaction and the accompanied volume expansion of product, which significantly weakened the properties of interconnection. Therefore, better process conditions should be proposed to improve the mechanical properties of this kind of ultra-small IMCs interconnection, for example, loading the compressive force in the soldering process.

(3) The planar growth of IMCs the Ni/Sn (5 μm)/Cu plane structure presented obvious non-symmetry. Because of the different rates of interdiffusion and chemical reactions of Cu and Ni in Sn layer, the planar growth of IMCs around Cu/Sn interface was faster than that around Ni/Sn interface. This phenomenon is similar to the perpendicular growth of IMCs in micro-joints. However, more systematic work should be conducted in the future to quantitatively evaluate the planar growth rate of IMCs.

Chapter 5 Perpendicular Phase Transformation of IMCs in Cu/Sn/Cu Structure

5.1 Introduction

3D IC stacking packaging approach has emerged to meet the requirements for portable and multifunctional electronic products, which can provide the smaller outlines and higher I/O than conventional package formats [147]. According to *Yole development 2013*, micro-bumping is one of the major challenges in the flip chip technology for 2.5D & 3D IC devices. The pitch size of lead-free solder micro-bump will continue to decrease to sub-10 μm, as shown in Figure 5-1 [148]. In that case, the solders are likely to react with substrate and be totally consumed to form the full intermetallic compound (IMC) joints. Then the growth of IMCs and phase transformation in the kind of IMCs joints would be in a semi-closed environment for no residual Sn-based solder, however, the correlative research of which has been seldom reported anywhere.

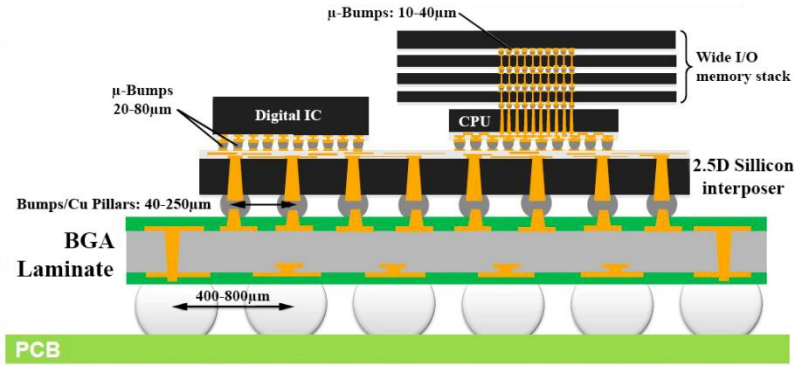

Figure 5-1 the architecture of 2.5D & 3D IC devices [148]

5.2 Experimental procedures

A commercial pure copper-rolled foil (99.99 wt.%) of 12.5 μm thick was used as carrier and substrate in this study. Electroplating method was selected to prepare the initial Cu/Sn/Cu sandwich structure. First of all, a constant and continuous Cu layer of 10 μm was electroplated on the carrier as a kind of substrate, and then a solder layer with uniform thickness of 2.5 μm Sn was electroplated as followed. On top of the Sn layer, another layer of Cu (10 μm thick) was also electroplated to finally get the Cu-plated/Sn/Cu structure. Besides, the other sandwich structure as Cu-rolled/Sn/Cu structure was also fabricated through electroplating Sn and Cu to the pure Cu-rolled foil in sequence. Herein, in order to guarantee the consistency of samples, the copper foil was tailored to be rectangle with the size of 25 mm×40 mm, and divided into 10 mm×10 mm small pieces after completing the sandwich structure fabrication. As shown in the schematic diagram Figure 5-2, the peripheral part was abandoned to avoid the thickness inconsistency of plated layer, which is usually caused by the edge effect of substrate. Then, the original samples were ready to be soldered.

Different types of specimens were successfully prepared through the soldering process in T-track oven as described in section 3.1.3. After that, the specimens were mounted with epoxy resin, and the grinding and polishing procedures were conducted to prepare the cross-sections for further analysis. Then the morphology of these micro-joints was observed by FEG-SEM, and also the thickness of different IMC layers was measured. For the fluctuant profile of Cu/IMCs interface, the thickness of IMCs interlayer was defined as the average of maximum and minimum values. Meanwhile, several times measurements have been conducted to reduce the

error. In particular, more attention have been paid to the single-side thickness of Cu_3Sn layer on different Cu substrates (Cu-rolled and Cu-plated substrates). When the IMCs interlayer of micro-joints turned to be Cu_3Sn only, its ½ thickness was selected to compare with the others.

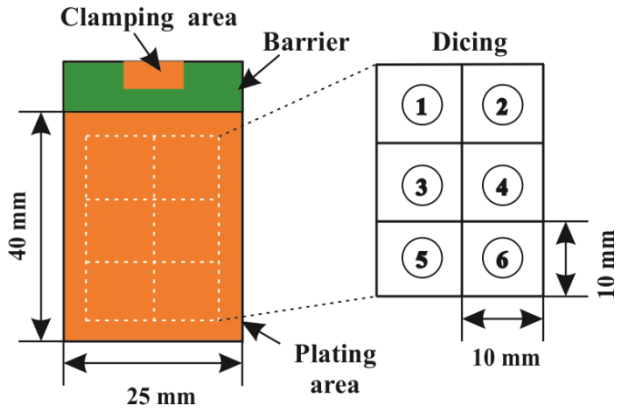

Figure 5-2 schematic diagram of the electroplated sample and the dicing method

5.3 Microstructural observation on the micro-IMCs-joints

5.3.1 Formation process of micro-IMCs-joints

In this project, all the sandwich samples were prepared through electroplating different layers in sequence. Then, once the Sn layer was plated on the Cu substrate (Cu-rolled or Cu-plated), the diffusion between Sn and Cu triggered automatically. As a result, Cu-rich phase was observed in the Sn-plated layer close to Cu substrate. While the Sn-plated layer is covered by the top Cu-plated layer later, the phenomenon of diffusion on the top interface between Cu-plated layer and Sn-plated layer was not that obvious. As shown in Figure 5-3 (a), when the sandwich structure is constituted with the Sn-plated interlayer around 5.5 μm, about 1.6 μm thick Cu-rich phase (the dark grey layer) was formed on the former interface. The composition of Cu-rich phase is close to the Cu_6Sn_5 while the light grey layer contains the amount of Cu atoms as 14.8 at.%. Furthermore, when the thickness of the Sn-plated interlayer was reduced to 2.5 μm, the effect of the preliminary diffusion between Sn-plated layer and Cu substrate should be significantly considered. As revealed by Figure 5-2(b), most of the Sn-plated interlayer were occupied by the Cu-rich phase. Although some Sn-rich area still remain, the Cu-rich phase seems to bridge the up and down interfaces. It indicates that through the electroplating method to make the Cu-plated/Sn (2.5 μm)/Cu structure, a high concentration of Cu atoms will be achieved in the whole Sn-plated interlayer.

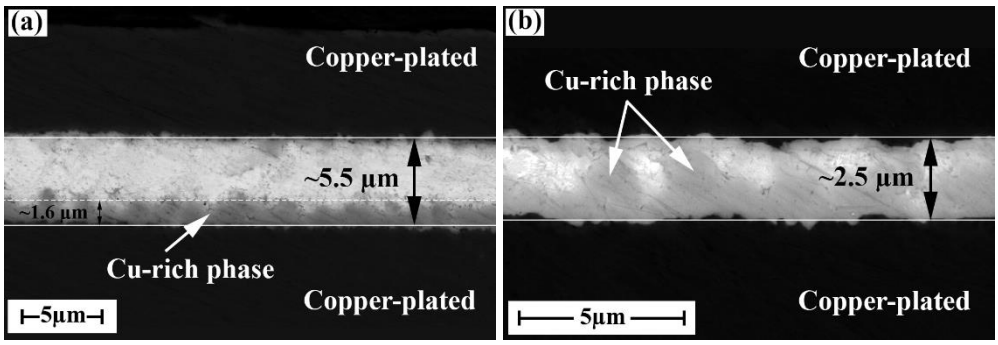

Figure 5-3 SEM images on the initial samples after plating (a) Cu/Sn (~5 μm)/Cu; (b) Cu/Sn (~2.5 μm)/Cu

It has been pointed out in Bosco's paper [28] that the minimum requirement for the thickness of Sn-based solder to form a pore-less micro-IMCs-joint is about 6 μm. As described in Section 2.3.1, the growth of scalloped Cu_6Sn_5

IMC started from the Cu/Sn interface toward to the middle-plane of Sn solder layer. When the thickness of Sn solder layer is not thick enough, the scalloped grains from two opposite interfaces would merge each other, then the un-reacted Sn will be separated by the bridged grains. Besides, the solidification of these isolated Sn caused by the peripheral Cu-Sn reaction cannot fill in these spaces. Then lots of voids will form around the middle-plane of interlayer, which is demonstrated well in experiment here (shown in Figure 5-4). This sandwich micro-joint was prepared in T-track oven by heating up to 230 °C with 50 °C/min, the initial Sn-plated layer was about 3 μm thick. The EDX result shows that the two scalloped Cu_6Sn_5 grains were merging while the Sn-rich area still remained. As previously predicted, the voids appeared within the samples where the thickness of Sn-plated interlayer is only 3 μm.

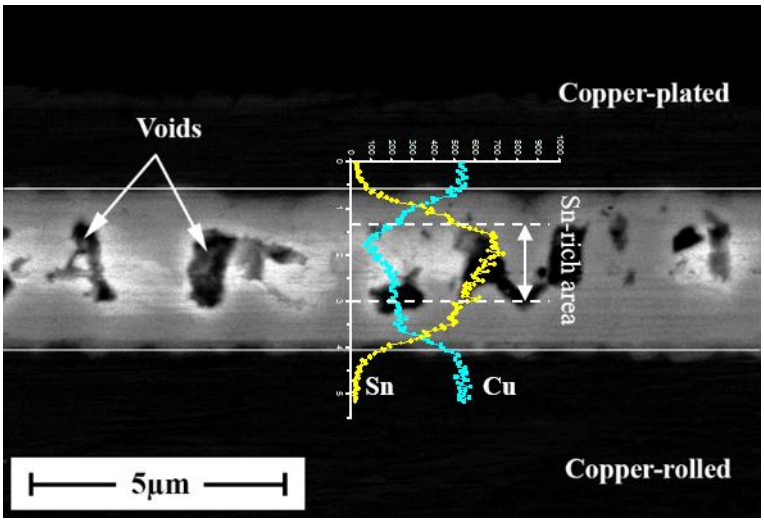

Figure 5-4 voids formed by scalloped Cu_6Sn_5 merging in the Cu-rolled/Sn (~3 μm)/Cu structure after heating to 230 °C with 50 °C/min in T-track oven

However, no such voids were found in all the below Cu/Sn (~2.5 μm)/Cu structures after soldering, which can be interpreted for a new formation process occurred. Generally, the distribution of Cu atoms in a relative thicker Sn-plated interlayer is prone to be different along distance versus to Cu side, which is the result from the diffusion control mechanism. Moreover, the diffusion rate of Cu along grain boundary is quicker than that of the bulk diffusion. Therefore, the inhomogeneous distribution of Cu atoms will cause the scalloped growth of Cu_6Sn_5 in soldering. That would be the reason why the compact micro-joints were not produced using the initial structures with 3~10 μm Sn-plated interlayer. Oppositely, sufficient Cu atoms dissolved in the Sn-plated interlayer after electroplating when the thickness of interlayer was reduced to ~2.5 μm as shown in Figure 5-3(b). During the heating stage, the distribution of Cu and Sn atoms became homogeneous shortly, then the isometric crystal would form in the solidification process while the scalloped growth of Cu_6Sn_5 IMC grain was suppressed.

5.3.2 Effect of substrates on the microstructure

Figure 5-5 shows the cross sectional microstructure of the two types of sandwich joints formed on different substrates, such as the Cu rolled/IMCs/Cu structure (left) and Cu-plated/IMCs/Cu structure (right). Both these two groups of joints were bonded at the temperature of 240 °C, but with different dwell time ranging from 0 to 25 mins. It is obvious to see that some Sn-rich area still remained in the joint formed on copper-rolled substrate, while the Sn layer was totally transformed into Cu_6Sn_5 IMC in the joint formed on copper-plated substrate with the dwell time of 0 min. Once the dwell time lasted longer from 5 mins to 25 mins, the Cu_3Sn layers appeared at the interface between Cu and Cu_6Sn_5, and became thicker accompany with the thinner Cu_6Sn_5 layer. Meanwhile,

the thickness of the Cu_3Sn layers on copper-plated substrate was thicker than that on the copper-rolled substrate. And lots of micro-voids (the black dots in the images) emerged in the Cu_3Sn layers in the Cu-plated/IMCs/Cu micro-joints with 5 mins dwelling. This phenomenon appeared later in the Cu-rolled/IMCs/Cu micro-joints which were dwelled at 240 °C more than 5 mins.

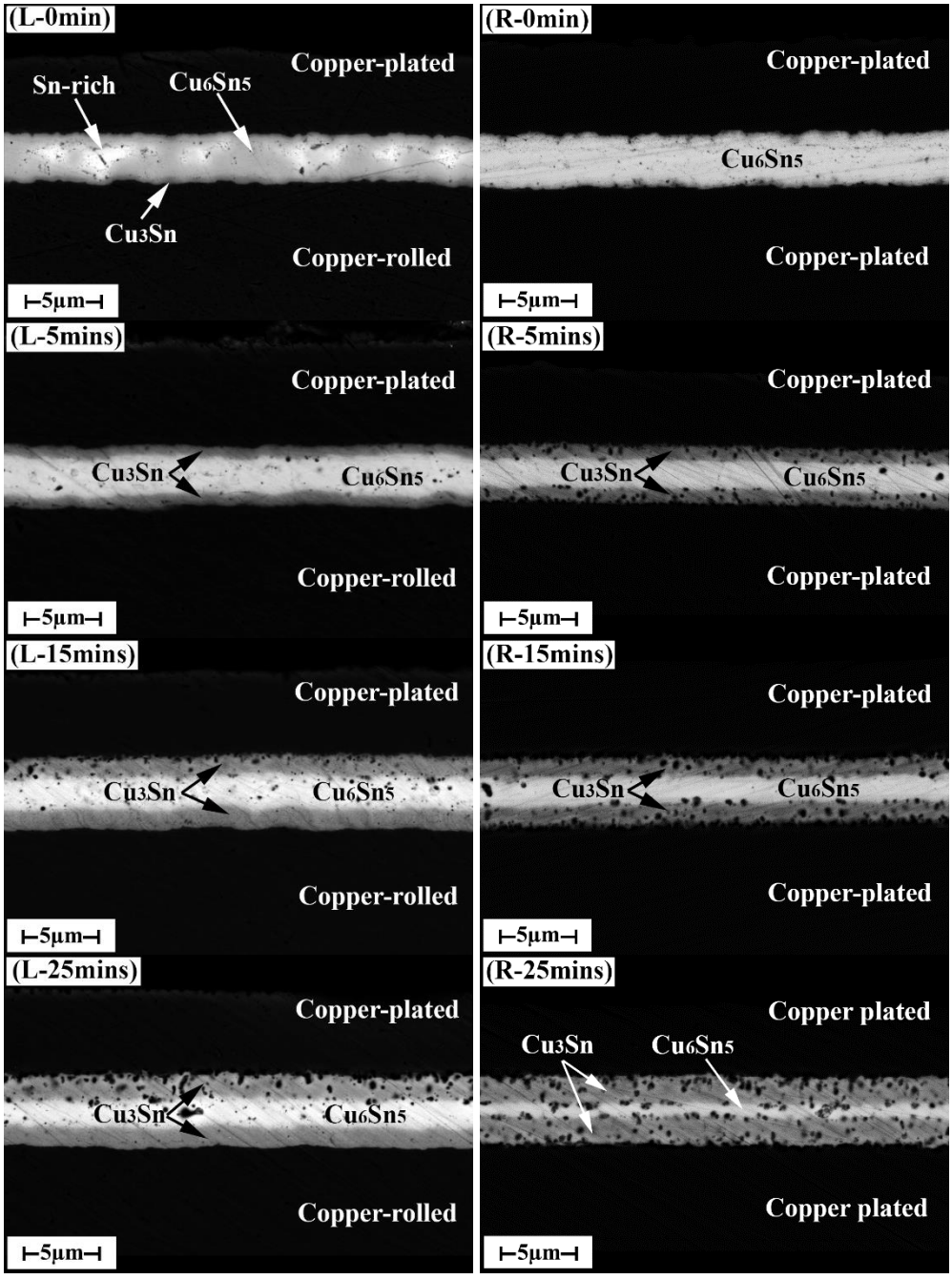

Figure 5-5 morphologies of IMCs interlayer on two types of Cu substrates soldered at 240 °C with different dwell time (L-Cu rolled/IMCs/Cu structure; R-Cu-plated/IMCs/Cu structure)

5.3.3 Effect of temperature on the microstructure

The similar appearance was also observed in those samples formed on Cu-rolled and Cu-plated substrates under 260 °C with different dwell time as displayed in Figure 5-6. Particularly, a tiny and wavy Cu_3Sn layer was generated on the interface between Sn and Cu-plated substrate at the beginning of the temperature approaching

to 260 °C. Afterwards, the morphology of Cu_3Sn layers tended to be planar. Besides, after the same dwell time, the proportion of Cu_3Sn layers in the micro-joints soldered under 260 °C was higher than that of micro-joints under 240 °C. And when the dwell time increased to 25 mins, only a thin layer of Cu_6Sn_5 remained on the centre-line of interlayer for the both groups of samples with different substrates.

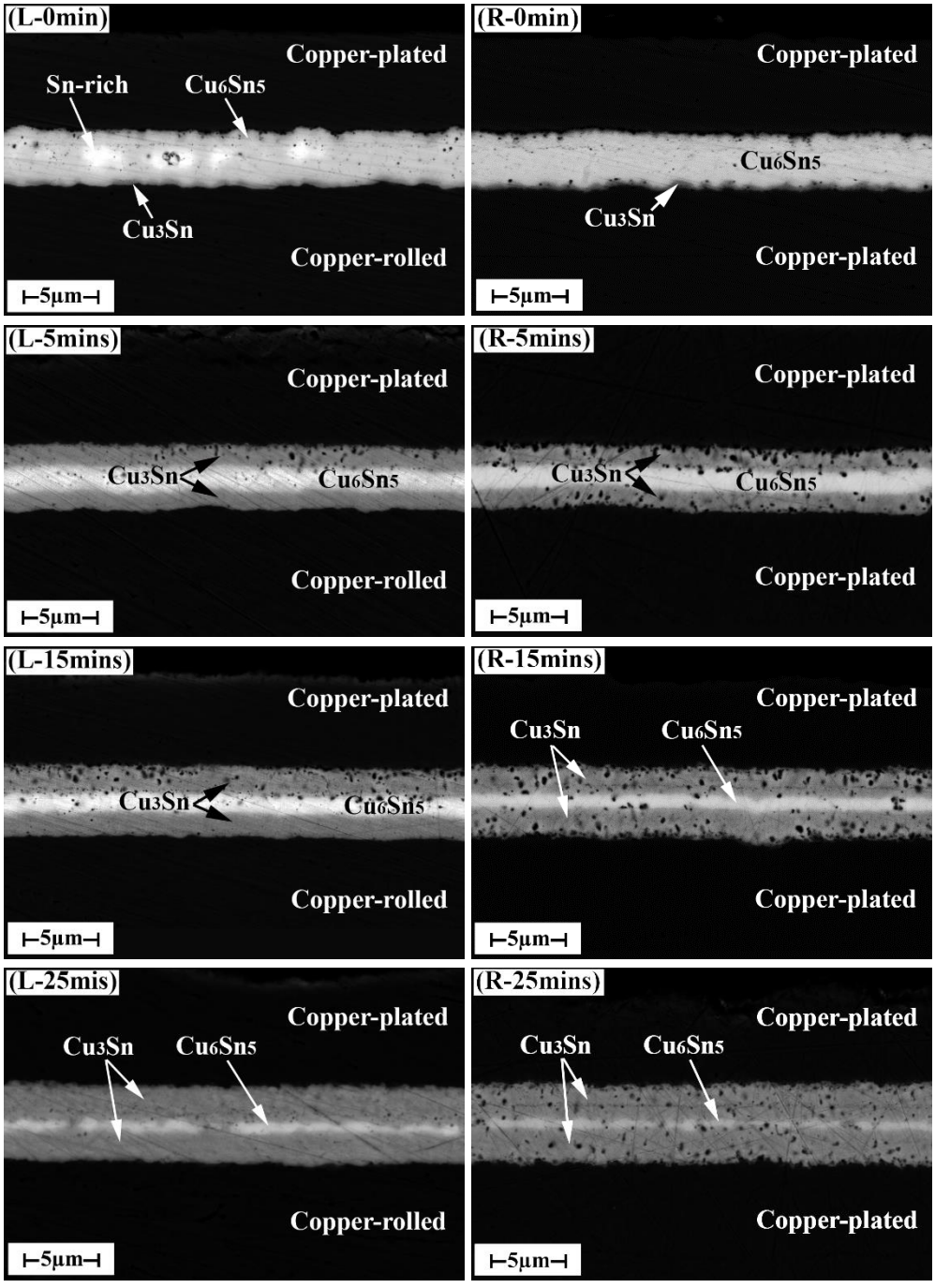

Figure 5-6 morphologies of IMCs interlayer on two types of Cu substrates soldered at 260 °C with different dwell time (L-Cu rolled/IMCs/Cu structure; R-Cu-plated/IMCs/Cu structure)

Figure 5-7 shows the microstructure of joints evolved with the increase of dwell time at the temperature of 290 °C. Since the temperature was higher than 260 °C, only the IMCs interlayer without any residual Sn-rich phase appeared in the micro-joints for 290 °C 0 min dwelling, and also the Cu_3Sn layers were observed clearly in these joints, no matter what kinds of substrates were used. After dwelling for 25 mins, the interlayers of Cu_6Sn_5 IMC

on copper-rolled substrate was almost converted into Cu_3Sn IMC layer. However, it took less than 15 mins dwell time to allow Cu_6Sn_5 fully transferred into Cu_3Sn on copper-plated substrate. And some micro-voids formed around the center-line of Cu_3Sn interlayer as the result of phase transformation.

Because the bonding layer (Sn layer) was thin enough (around 2.5 μm), the full IMCs joint tends to be formed even at the low bonding temperature on the copper-plated substrate: the Cu_6Sn_5 IMC joint can be obtained once the temperature reach 240 °C, and the Cu_3Sn IMC joint can be made by keeping 15 mins dwell time at 290 °C. All the observation above implicates that the Cu-Sn reaction or the Cu-Cu_6Sn_5 reaction was quicker on the copper-plated substrate than that on the copper-rolled substrate.

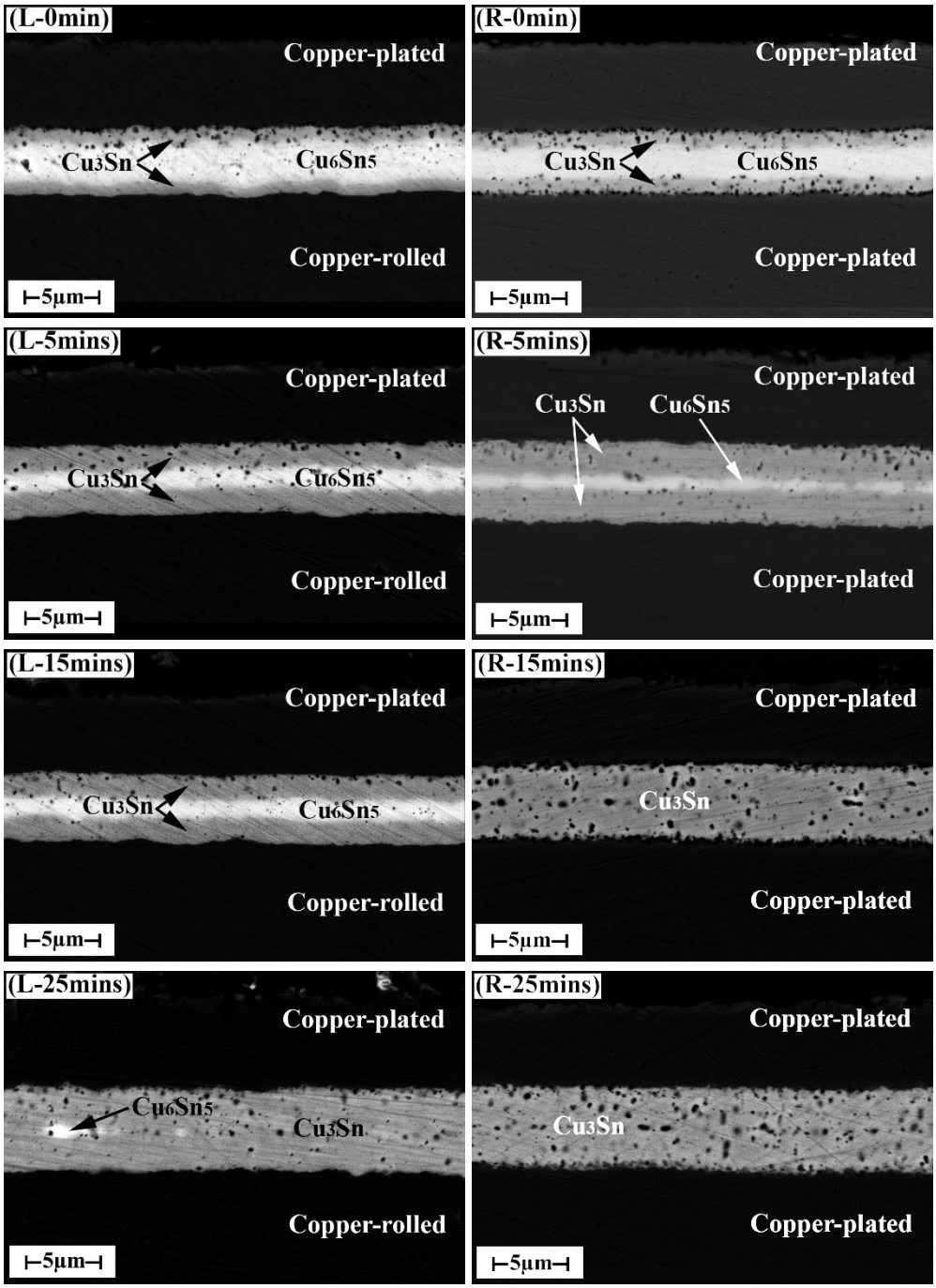

Figure 5-7 morphologies of IMCs interlayer on two types of Cu substrates soldered at 290 °C with different dwell time (L-Cu rolled/IMCs/Cu structure; R-Cu-plated/IMCs/Cu structure)

5.4 Kinetics study on the growth of Cu-Sn IMCs

According to the mass balance:

$$\frac{N_{Cu}}{N_{Sn}} = \frac{n_{Cu}}{n_{Cu}} = \frac{S \times d_{Cu} \times \rho_{Cu}}{S \times d_{Sn} \times \rho_{Sn}} \times \frac{M_{Sn}}{M_{Cu}} \tag{5-1}$$

Where, N_X is the number of X atoms, n_x is the molar number of mass (x), S is the contacting reaction area, and the dx is the thickness of x which has participated in the reaction. ρ_x and M_x are the mass density and molar mass of x, respectively. Herein, the value used are M_{Cu}=63.5g/mol, M_{Sn}=118.7g/mol, ρ_{Cu}=8.96g/cm^3, ρ_{Sn}=7.28g/cm^3.

For the Cu_6Sn_5,

$$\frac{d_{Cu}}{d_{Sn}} = \frac{6}{5} \times \frac{M_{Cu} \times \rho_{Sn}}{M_{Sn} \times \rho_{Cu}} \approx 0.5 \tag{5-2}$$

For the Cu_3Sn,

$$\frac{d_{Cu}}{d_{Sn}} = 3 \times \frac{M_{Cu} \times \rho_{Sn}}{M_{Sn} \times \rho_{Cu}} \approx 1.3 \tag{5-3}$$

If ignoring the volume change caused by difference of crystalline types during the phase transformation process, then the Sn layer has been totally transformed into Cu_6Sn_5 and the growth of Cu_3Sn was neglected, the thickness of IMC (Cu_6Sn_5) is calculated to be 3.75 μm for the 2.5 μm Sn layer participated in the reaction. Besides, once the Sn layer has been transformed into Cu_3Sn completely, the thickness of this IMC (Cu_3Sn) interlayer is about 5.75 μm. Therefore, in the case of both the two kinds of IMCs (Cu_6Sn_5 and Cu_3Sn) contained in the connecting area, the thickness of IMCs should be in the range of 3.75 μm to 5.75 μm as long as the Sn layer is consumed completely.

As shown in Figure 5-8, there is a clear relationship between the thickness of IMCs interlayer in the joints and the soldering temperature and dwell time. The experimental data falls within the calculated range of 3.75 μm to 5.75 μm, except the samples which were soldered at 240 °C with the dwell time of 0 min. The thickness of total interlayer in the Cu-rolled/IMCs/Cu micro-joint formed at 240 °C/0 min is about 3.26 μm. Although the Cu-plated/IMCs/Cu joint does not contain the residual Sn-rich phase, the reaction may not be sufficient at the low soldering temperature as 240 °C. Thus the one in Cu-plated/IMCs/Cu micro-joint is also less than 3.75 μm. Besides, the thickness of IMCs in all kinds of micro-joints increased with the prolonged dwell time. In the micro-joints of Cu-rolled/IMCs/Cu, the thickness of interlayer soldered at 240 °C and 260 °C tended to be similar after 5 mins dwelling as reflected in Figure 5-8(a). However, the more obvious increase of total thickness of interlayer with the elevated temperature can be observed in Cu-plated/IMCs/Cu micro-joints (Figure 5-8 b). And the thickness difference of interlayer in these two kinds of structures is not significant under the corresponding soldering condition.

Moreover, the phase transformation of Cu_6Sn_5 into Cu_3Sn is the main reaction in the dwelling stage, following which, the growth behaviour of Cu_3Sn layer on different substrates has been paid more attention. The thickness of single-side Cu_3Sn layer on Cu-rolled and Cu-plated substrate were measured and given in Figure 5-9. Obviously, the Cu_3Sn layer is thickening with the increase of dwelling temperature. Meanwhile, the thickness of Cu_3Sn layer increases quickly with the dwell time increased from 0 min to 5 mins. When the dwell time is more than 5 mins, the growth of Cu_3Sn layer is slowed down and close to be linear with the dwelling time. Especially,

there is an apparent error on the Cu_3Sn thickness of Cu-rolled/IMCs/Cu micro-joint formed at the condition of 290 °C dwelling 15 mins. In that case, the value was modified with the linear interpolation method as shown in Figure 5-9(a), which will be used in the subsequent further analysis instead of the actual value.

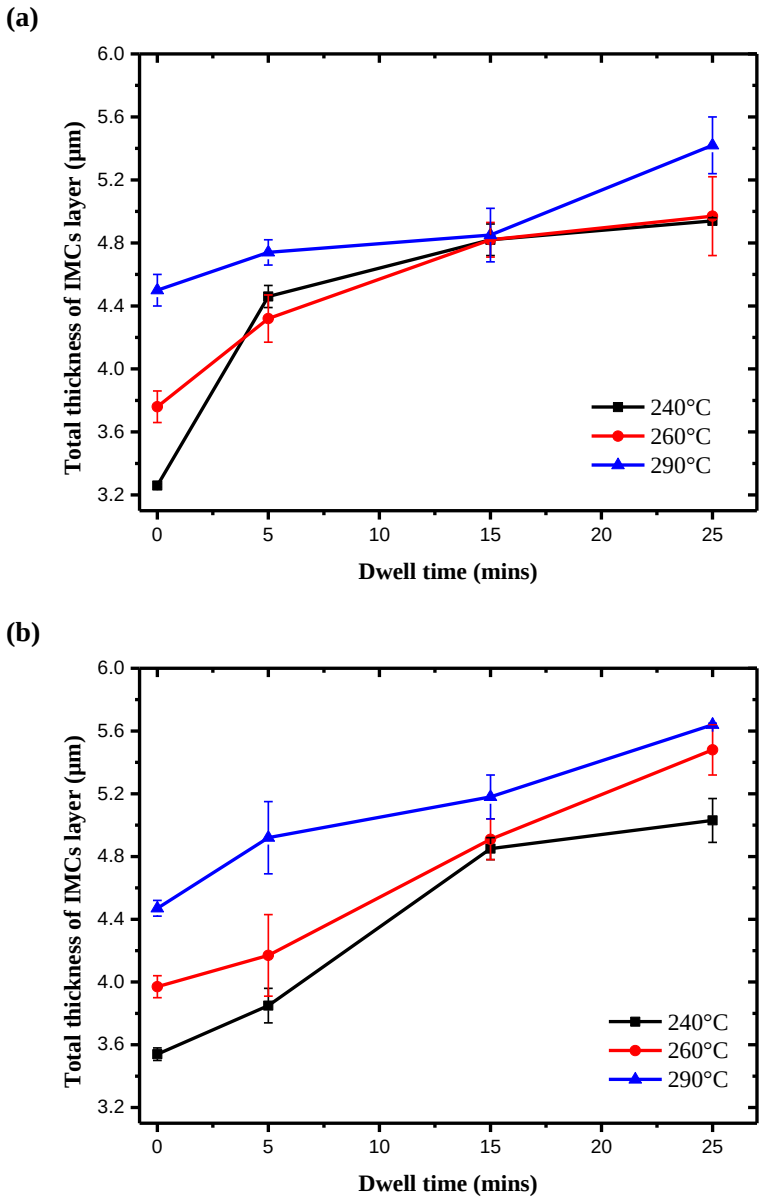

Figure 5-8 total thickness of IMCs interlayer in the two types of micro-joints (a) Cu-rolled/IMCs/Cu; (b) Cu-plated/IMCs/Cu

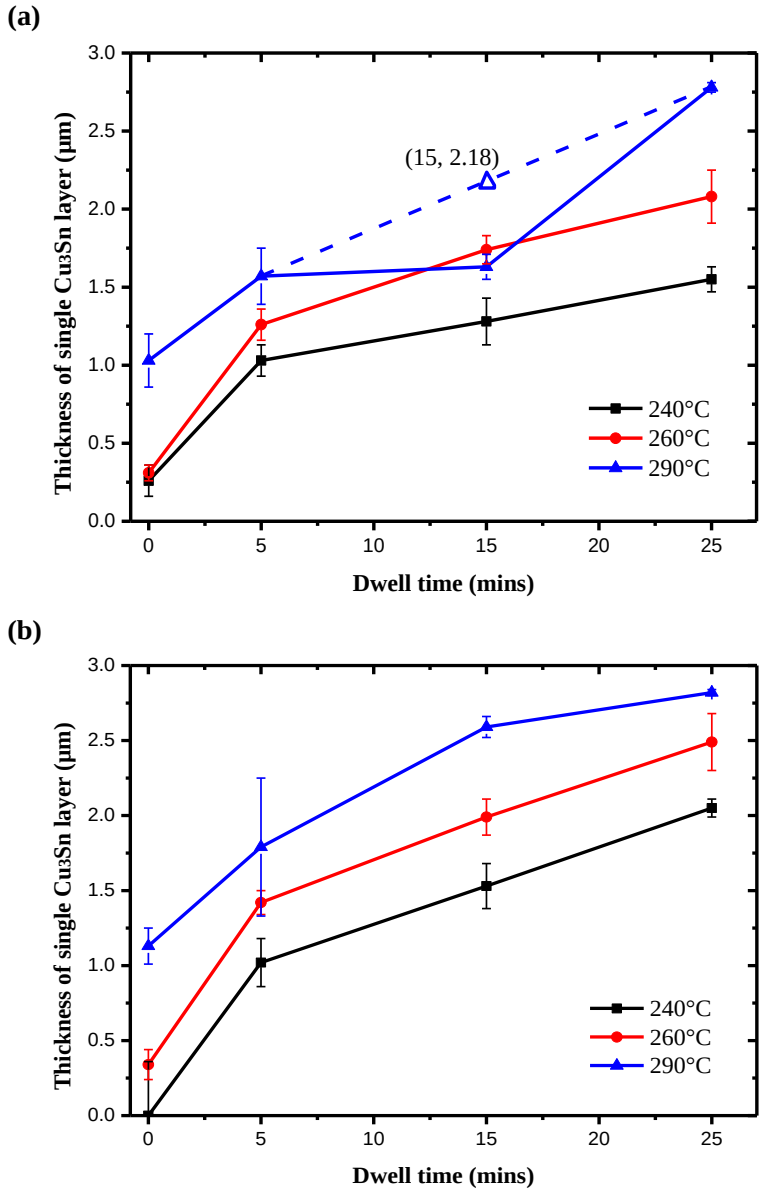

Figure 5-9 thickness of single Cu_3Sn layer on different Cu substrates within IMCs micro-joints (a) Cu-rolled substrate; (b) Cu-plated substrate

The changes of square of Cu_3Sn thickness on different Cu substrates have also been discussed using the empirical power law of (2-1). Then, the fitting lines plotted to describe the experimental results are projected in Figure 5-10. The growth factor (n) increases from 0.29 to 0.47 in the Cu-rolled/IMCs/Cu structure, while the value of n decreases from 0.48 to 0.34 in the Cu-plated/IMCs/Cu structure. When the soldering temperature is 240 °C, the growth rate of Cu_3Sn on Cu-plated substrate is controlled by the atomic diffusion rate along grain boundary since the n is close to 0.5. With the increase of soldering temperature, the reaction between Cu-plated substrate and Sn layer has become much quicker, hence, the thicker Cu_3Sn layer appears even with the short dwell time and extends the distance of Cu atoms from substrate to the middle Cu_6Sn_5 layer. At the same time, the middle Cu_6Sn_5 layer has been consumed gradually, where the concentration of Cu atoms was raised along with the decline of Sn concentration. Therefore, the atomic diffusion rate driving by the concentration gradient has been reduced in these semi-closed Cu-Cu_6Sn_5 diffusion couple. Then as a result, the growth rate of Cu_3Sn layer on Cu-plated substrate is corresponding decreased. When the soldering temperature is 290 °C, n = 0.34 indicates that the

growth rate of Cu_3Sn layer is controlled by rate of the atomic volume diffusion. The reaction rate between Cu and Cu_6Sn_5 layer has a critical influence on the growth of Cu_3Sn by now.

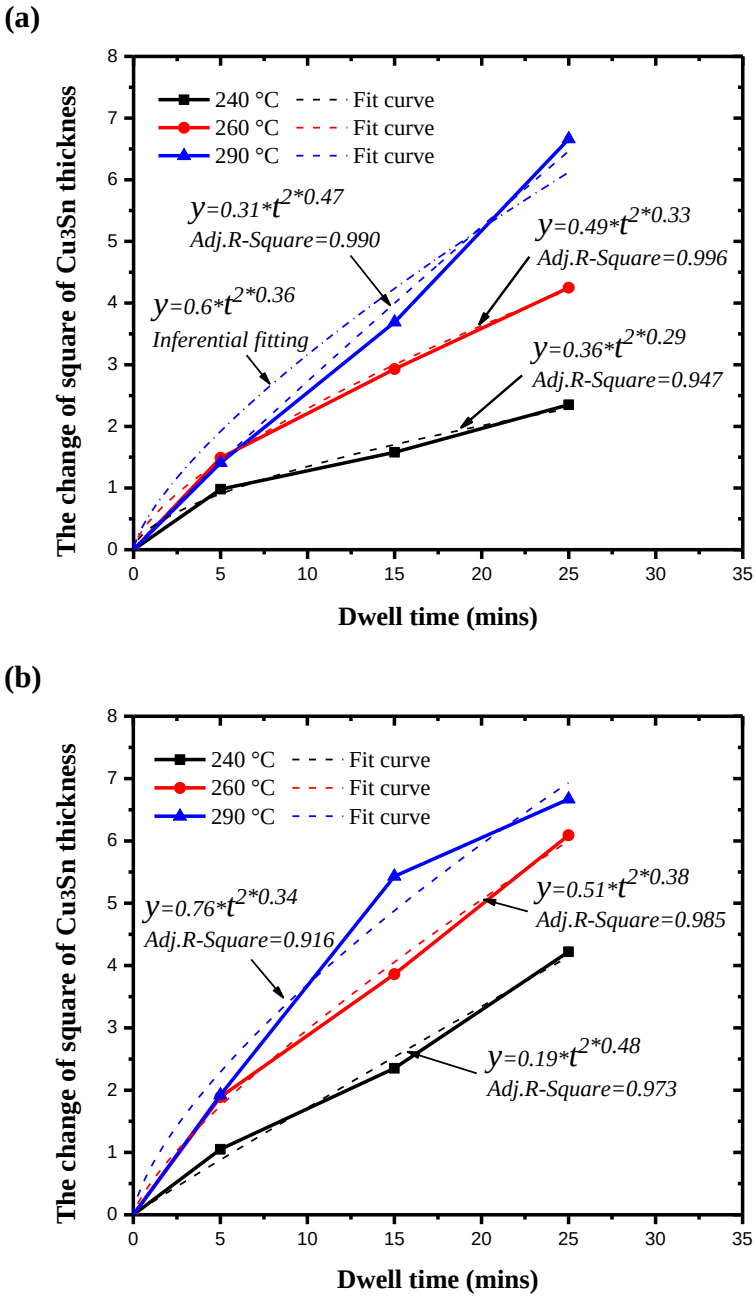

Figure 5-10 the change of square of Cu_3Sn thickness on different Cu substrates
(a) Cu-rolled substrate; (b) Cu-plated substrate

In the Cu-rolled/IMCs/Cu structure, the value of *n* is only 0.29 at 240 °C which is attributed to the microstructural difference between the two types of Cu substrates. Compared with the Cu-plated substrate, there is relative less number of grain boundaries in the Cu-rolled substrate with bigger grains. Thus the volume diffusion of Cu atoms is the main pattern within this kind of substrate, as well as the only providing resource of Cu atoms for the phase transformation, the growth rate of Cu_3Sn layer has been constrained on the Cu-rolled substrate. However, the atomic diffusion rate has been increased accompany with the improvement of atomic activities at the elevated soldering temperature, then the growth factor of Cu_3Sn layer on Cu-rolled substrate is increased. Particularly, on

the basis of observation in Figure 5-6 and Figure 5-7, it is worth noticing that the microstructure of Cu-rolled/IMCs/Cu structure at 290 °C falls in between the microstructure of Cu-plated/IMCs/Cu structures at 260 °C and 290 °C. Therefore, the growth factor of Cu_3Sn on Cu-rolled substrate at 290 °C is referred in the range of 0.34~0.38. In Figure 5-10(a), the analysis has been conducted using the modified value of Cu_3Sn thickness under 290 °C 15 mins. The corresponding growth factor turns to be 0.47 which reflects the trend of increasing, but is much higher than the prediction. Herein, the growth factor of Cu_3Sn on Cu-rolled substrate at 290 °C is supposed to be 0.36, and the inferential fitting line is also drawn in the Figure 5-10(a). Then, a deduction can be made as the coefficient of Cu_3Sn growth (K) has increased from 0.36 to 0.6 on Cu-rolled substrate and from 0.19 to 0.76 on the Cu-plated substrate when the soldering temperature increased from 240 °C to 290 °C. Meanwhile, the value of *K* in two types of micro-joints seems to be similar at the same temperature, which shows a strong temperature dependence.

5.5 Discussion on the Kirkendall phenomenon in micro-IMCs-joints

It is generally known that in Cu-Sn and Cu-Cu_6Sn_5 diffusion couple, Kirkendall voids are the result of the different diffusion rate of Cu and Sn within the Cu_3Sn layer [30, 149]. Because of the rapider diffusion of Cu than Sn in Cu_3Sn layer, vacancies have been created by the migration of Cu which have not been filled by the Sn atoms, thus aggregated as micro-voids. In the micro-IMCs-joints, no Sn solder has been left and the volume of Cu_6Sn_5 layer is limited. The Cu-Cu_6Sn_5 diffusion couple is in the semi-closed environment, where the diffusing Sn atoms are from the reaction $Cu+Cu_6Sn_5 \rightarrow Cu_3Sn+Sn$ [150]. Therefore, it is reasonable to believe that the Kirkendall effect in the micro-IMCs-joints would be exacerbated.

In the experiment, micro-voids were mainly found to be adjacent to Cu_3Sn/Cu interface or distributed in the Cu_3Sn layers which formed on Cu-plated substrate. Oppositely, no Kirkendall voids were observed clearly in the Cu_3Sn layer on Cu-rolled substrate. Since the Cu atoms have been supplied only by the copper substrate to participate in the $Cu_6Sn_5 \rightarrow Cu_3Sn$ transformation, the providing capability of substrate should be the critical factor to determine the diffusion rate of Cu. However, there is obvious difference between the Cu-rolled and Cu-plated substrates in microstructure. Because the Cu-rolled substrate is constituted with several big grains, the volume diffusion of Cu is the main mechanism. The low diffusion rate of Cu in Cu-rolled substrate has restricted the providing amount of Cu atoms, but leaded to the diffusing balance between Cu and Sn in the Cu_3Sn layer. That is the reason why the compact Cu_3Sn layer formed on the Cu-rolled substrate. In contrast, there are nano-grains and lots of grain boundaries in the Cu-plated substrate. The Cu atoms are diffusing through grain boundaries in Cu-plated substrate, which results in the bigger diffusion flux of Cu than Sn, and then provided the essential condition for the formation of Kirkendall voids.

Moreover, the high soldering temperature is also benefit to the formation of Kirkendall voids. Other studies have found that the diffusion coefficient of Cu atoms in Cu_3Sn is about 17 times higher than that of Sn atoms at 25 °C through molecular dynamics simulation [151]. And also, Paul [132] reported that the diffusion coefficient of Cu is about 30 times as that of Sn at the temperature ranging from 225 °C to 350 °C. This indicates that the higher temperature contributes significantly to the formation of Kirkendall voids. In the Cu-plated/IMCs/Cu structure, the thickness of Cu_3Sn layer has increased with the increase of soldering temperature, which has extended the diffusing distance of each atoms and enhanced the difference of diffusion coefficients. Therefore, the Kirkendall effect is much obvious in the Cu_3Sn layer on Cu-plated substrate at 290 °C.

5.6 Summary

Two types of sandwich structures as Cu-rolled/Sn (2.5 μm)/Cu and Cu-plated/Sn (2.5 μm)/Cu were selected to

produce micro-IMCs-joints through the TLP soldering process in this chapter. The microstructure of these micro-IMCs-joints formed after different dwell time at the soldering temperature of 240/260/290 °C have been observed. And also, the effect of different types of substrates on the growth of IMCs layer has been discussed. Therefore, some summaries about the formation process and the growth mechanism of Cu-Sn IMCs in these micro-joints can be made as the following:

(1) Because of only 2.5 μm thick Sn-plated solder layer in the two interconnecting structures, the high content of Cu atoms was achieved in that interlayer before soldering. Hence, the growth of Cu_6Sn_5 on the Cu/Sn interfaces was not been constrained by the Cu diffusion in vertical direction completely. In the solidification stage, the whole Sn-plated interlayer has transformed into Cu_6Sn_5 isometric crystals quickly instead of the scalloped grains. As the result, the compact Cu-Sn IMCs (Cu_6Sn_5 mainly) micro-joints can be fabricated.

(2) The phase transformation of Cu_6Sn_5 into Cu_3Sn is the primary reaction in the Cu-Sn IMCs micro-joints. With the increase of soldering temperature or the dwell time, the thickness of IMCs interlayer in the Cu-rolled/IMCs/Cu and Cu-plated/IMCs/Cu structures has increased. In particular, the progress of phase transformation in Cu-plated/IMCs/Cu structure is much faster than that in the Cu-rolled/IMCs/Cu structure. After soldering at 240 °C for 0 min, the Sn-plated layer on Cu-plated substrate has become Cu_6Sn_5 totally to form the full IMCs micro-joint. Besides, the initial Cu-plated/Sn/Cu structure has been changed as the Cu-plated/Cu_3Sn/Cu joint under the soldering condition of 15 mins dwelling at 290 °C.

(3) No matter the Cu-rolled or Cu-plated substrate is, the Cu_3Sn layer has thickened with the prolongation of dwell time, and the growth of Cu_3Sn has been accelerated for the high soldering temperature. Furthermore, the growth behavior of Cu_3Sn has been studied in kinetics, such as the growth factor of Cu_3Sn on Cu-plated substrate decreases from 0.48 to 0.34 while that of Cu_3Sn on Cu-rolled substrate increases from 0.29 to 0.36 with the bonding temperature elevated from 240 °C to 290 °C. The growth of Cu_3Sn mainly depends on the types of substrates at 240 °C, it is the release rate of Cu atoms from substrate into interlayer. For the soldering temperature improved, the thick Cu_3Sn layer has formed at the early stage and prolonged the diffusion time of atoms to the reaction interfaces afterwards. Therefore, the growth rates of Cu_3Sn on the two types of substrates are constrained by the thickness of itself, although the diffusion rates of each atoms have been promoted by the high temperature.

(4) Lots of Kirkendall voids prefers to emerge in the Cu_3Sn layer on Cu-plated substrate rather than Cu-rolled substrate. One of the reasons is the diffusing flux of Cu atoms from Cu-plated substrate into interlayer was much more than that from the Cu-rolled substrate. And the other main reason is that the diffusing Sn atoms were only provided by the reaction $Cu+Cu_6Sn_5 \rightarrow Cu_3Sn+Sn$ in the Cu-Cu_6Sn_5 diffusing couple. Thus, the supply of Sn atoms could not fill the vacancies for the Cu atoms left. Moreover, the diffusion rate differences between Cu and Sn in Cu_3Sn layer were enlarged at the high temperature, then the amount of Kirkendall voids has increased with the thickening of Cu_3Sn with dwell time.

Chapter 6 Homogenizing and Mechanical Property of Cu_3Sn IMC Micro-interconnection

6.1 Introduction

The packaging and integration using micro-bumps to connect the through-Si-Vias (TSVs) chips in vertical direction are often required distinctive features from the conventional package formats. And, ensuring the reliability of these micro-joints (<10 μm) has become one of the major challenges in the 3D integration [147, 152, 153]. Sn or Sn-based solder may be completely consumed with the scaling down size of joints during the stacking process, to form the entire intermetallic compounds (IMCs) interconnection. The formation and microstructural evolution of the solder joints at a relative large scale (e.g. >50 μm) during the reflow and thermal aging process have been well studied [154-156]; however, further investigations are still needed to establish on the full IMCs interconnection without existence of any remnant solders, in particular, the discontinuity that are associated with the crystallite microstructure and mechanical integrity.

In order to achieve the reliable miniaturized interconnections for 3D stacking of ICs, the crystallites features of Cu-Sn IMCs and the effect of growth process including the transformation between different IMC phases and morphological evolution of IMCs are yet to be understood. In this work, EBSD was selected to observe the microstructural change with phase transformation from Cu_6Sn_5 into Cu_3Sn IMCs, and the homogenization process in the Cu_3Sn IMC joints.

6.2 Experimental procedures

6.2.1 Preparation of Cu/IMCs/Cu test structure

In this study, polycrystalline oxygen-free rolled copper (30 mm×15 mm×1 mm) was employed as substrate. A thin layer of Sn approximately 2.5 μm thick was first electroplated on the substrate after pre-treatment of acid washing process, then a copper layer of ~10 μm was electroplated on the top of the plated Sn to create an initial Cu/Sn/Cu sandwich test structure, as shown in Figure 6-1(a). Such sandwich structure was heated up to 260±2 °C to allow Sn melting and reacting with surrounding Cu in a vacuum chamber, and followed by an isothermal storage process with different dwell time (10/30/50/70 mins) as illustrated in Figure 3-5(b).

6.2.2 Microstructural analysis of IMCs

The type of IMCs phases was identified by XRD method, and more details of the Cu/IMCs/Cu interconnections at crystallite level were further observed and analysed by EBSD module in the FIB system. As the IMCs formed under high temperature with a long dwell time, thus both the Cu_6Sn_5 and Cu_3Sn are hexagonal structure [88, 157]. To facilitate the EBSD characterization, the Orientation Imaging Microscopy (OIM) software was utilized to collect the data with a 30 KV beam. The Image Quality (IQ) quick map and Phase Quick map were plotted using OIM Analysis software to observe the microstructure and the phase distribution of joints. Inverse Pole Figure [001] (IPF) quick map and the discrete IPF of Cu_3Sn were also derived to display the orientation distribution of Cu_3Sn grains in micro-joints with 70 mins dwell time. Besides, the phase ratios of each phase, the distribution of misorientation angle and grain size were estimated from the selected IMCs interlayer. Moreover, grain shape orientation (GSO) map referring to the angle of the major axis from the horizontal, where the shape of grains can be fitted by ellipses, was obtained from the OIM Analysis software to gain the evolution trend of Cu_3Sn grain shape with the prolonged dwell time. In addition, TEM was applied to observe the microstructure of IMCs interlayer on the vertical section, which was extracted from the micro-joint with the dwell time of 30 mins through

the FIB machining process. Therefore, the microstructure of IMCs interconnection can be analysed from the three dimensions.

6.2.3 Micro-mechanical testing

Mechanical testing was conducted by nano-indentation machine on the sample with the dwell time of 70 mins. Firstly, a micro-cantilever of ~5 μm×5 μm cross-sectional area was fabricated by FIB from Cu_3Sn IMC with voids included, as shown in Figure 6-1(a). Secondly, a flat diamond indenter with diameter of 5 μm was used to shear the micro-cantilever completely, aiming at the Cu_3Sn layer as shown in Figure 6-1(b). The loading rate 0.05 mN/s was applied in the shearing until the fracture occurred. Finally, the fracture surfaces were observed using FEG-SEM.

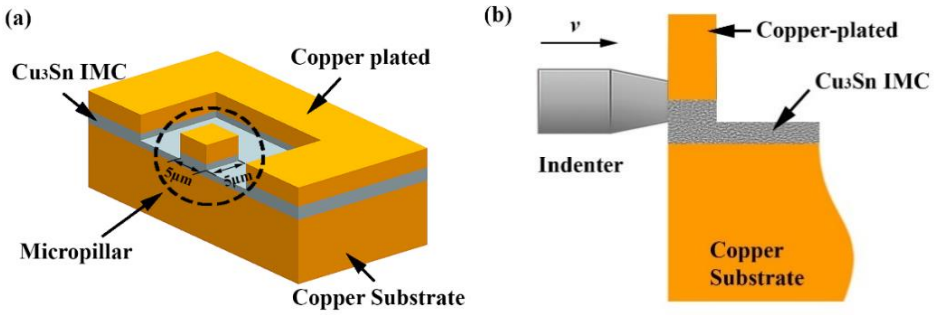

Figure 6-1 schematic illustration: (a) testing micro-cantilever fabricated by FIB; (b) mechanical testing on micro-cantilever by nanoindenter

6.3 Homogenizing process of Cu_3Sn in micro-joints

6.3.1 EBSD analysis of Cu/IMCs/Cu interconnects

The microstructure and phase distribution on Cu/IMCs/Cu cross-section from the samples reflowed at temperature of 260 °C for 10 mins and 30 mins are depicted in Figure 6-2 and Figure 6-3, respectively. From the IQ map, the shapes and number of IMC grains consisting of Cu_6Sn_5 and Cu_3Sn are revealed in details. Obviously, the entire IMCs interlayer can be divided into two sub-layers mainly composed by Cu_3Sn, growing and emerging from the two opposite sides of copper base with small amount of remanent Cu_6Sn_5 in the middle. It is worth noticing that a special layer contains some extra-fine equiaxial Cu_3Sn grains accompanied with micro-voids as seen in Figure 6-2 (a), which has been reported by other researchers [158, 159]. Furthermore, the same porous Cu_3Sn layer was also observed on the vertical section of micro-joints with 30 mins dwell time, which was magnified by the TEM observation in Figure 6-4. This layer is only found in adjacent to the electroplated copper, but does not appear on the opposite side of the initial rolled copper substrate.

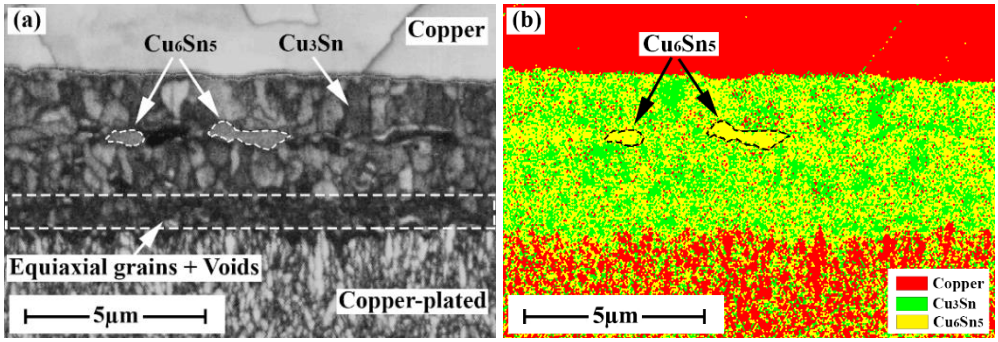

Figure 6-2 EBSD observation on the cross-section of micro-joint with dwell time of 10 mins at 260 °C (a) IQ map (b) Phase map

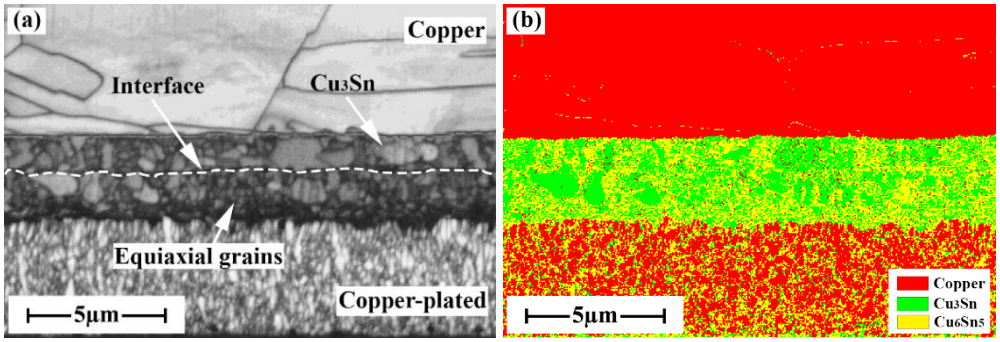

Figure 6-3 EBSD observation on the cross-section of micro-joint with dwell time of 30 mins at 260 °C (a) IQ map (b) Phase map

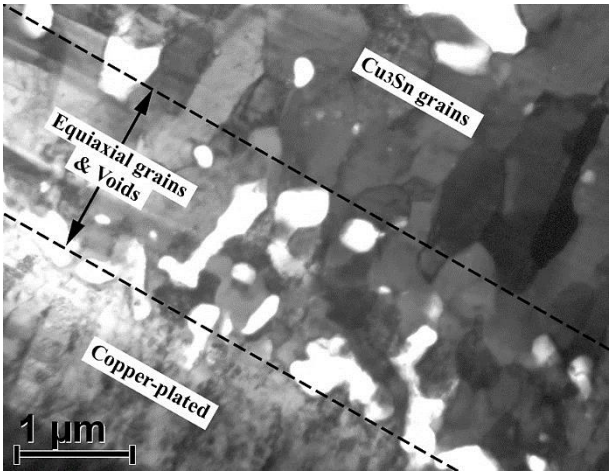

Figure 6-4 TEM bright-field observation on the vertical section of micro-joint with 30 mins dwelling at 260 °C

With dwell time increasing, the Cu_6Sn_5 grains disappeared gradually, and the residual Cu_6Sn_5 phase surrounding the coarse Cu_3Sn phase still remained in Figure 6-2(b), Figure 6-3(b) and Figure 6-5(b). This does not agree with the layer by layer growth of IMCs in conventional soldering joints [24]. The XRD result demonstrated in Figure 6-6 also confirms that the Cu_6Sn_5 phase still existed in the IMCs interlayer, even in the sample after 70 mins of dwell time. Furthermore, the ratio of each phase (Cu, Cu_6Sn_5 and Cu_3Sn) directly obtained from OIM Analysis software is plotted in Figure 6-7. Accordingly, the ratio of Cu_3Sn increased dramatically in the region of IMCs mixture as dwell time increased from 10 to 50 mins. The Cu_3Sn phase can reach approximately 85% in the IMCs layer after 50 mins, and this remained almost the same level with further increase of dwell time up to 70 mins.

The grain orientation of IMC interlayer is displayed by IPF map (Figure 6-5 c) of the sample with 70 mins dwell time, where the different colours represent different orientations of grains. The result indicates that IMC layers near the two types of copper layers did not exhibit any obvious preferential orientations, although the rolled Cu substrate can be locally treated as single crystal. Also, in Figure 6-5(d), the randomly distributed black dots in the discrete IPF of Cu_3Sn IMC means no certain grain orientation preference that can be manifested in the Cu_3Sn IMC growth process even after dwelling for 70 mins, as has been reported elsewhere [157]. However, Zhang's work showed preferred orientation (100) of Cu_3Sn grains in parallel with copper substrate [160]. This may be due to the formation temperature of Cu_3Sn IMC layer in this study which is relatively lower than the temperature (300 °C) used in the Zhang's work, can cause the incomplete process of coarsening and homogenization.

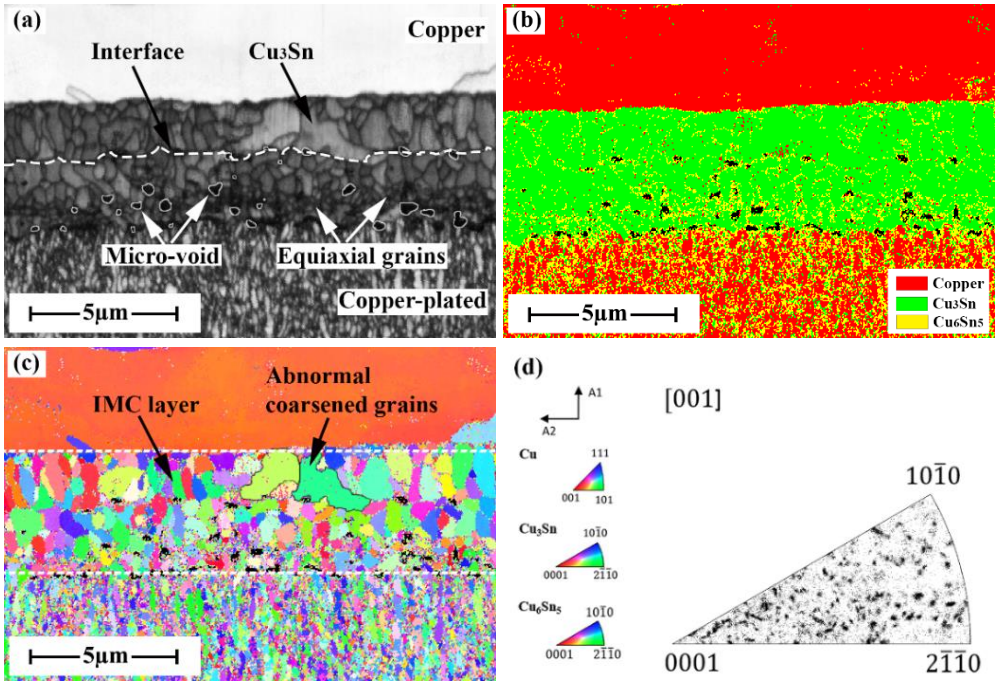

Figure 6-5 EBSD observation on the cross-section of micro-joint with dwell time of 70 mins at 260 °C (a) IQ map; (b) Phase map; (c) IPF map (A1: Rotation direction and A2: Transverse direction) colour codes are given in (d-left) and together with the discrete IPF of Cu_3Sn (d-right)

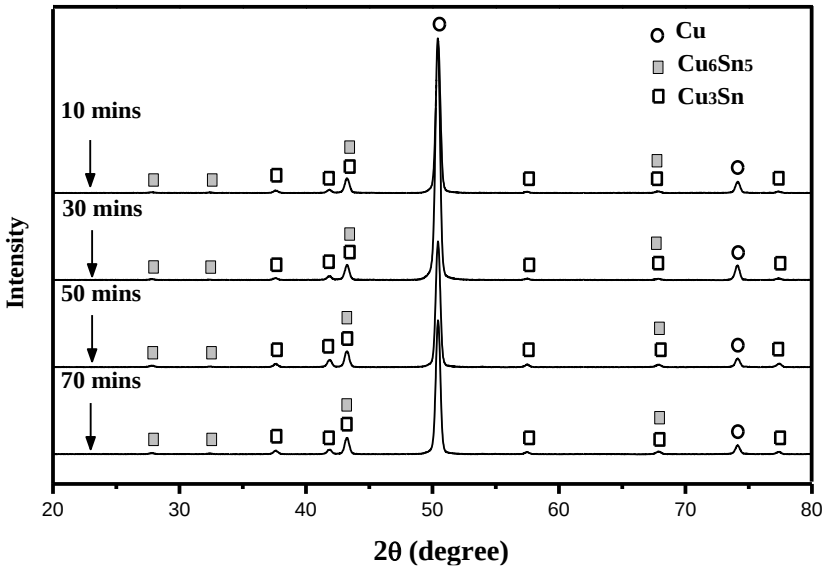

Figure 6-6 IMCs phases identification by XRD

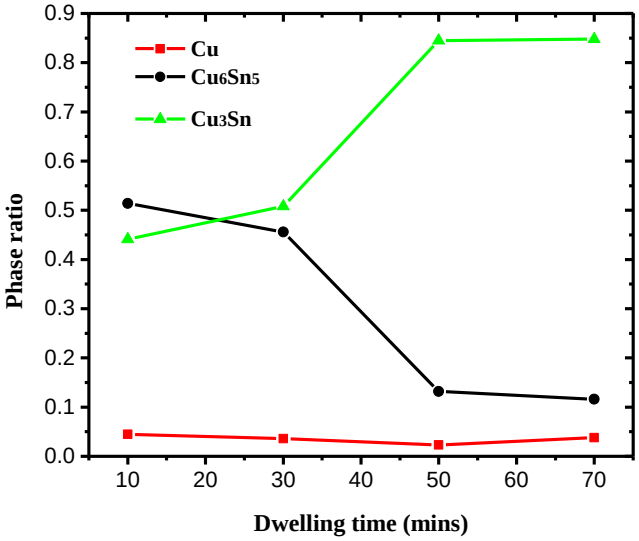

Figure 6-7 the ratio of each phase in IMCs interlayer of micro-joints

6.3.2 Kinetic analysis on IMC grains in micro-joints

As the center Cu_6Sn_5 layer disappeared in the micro-joint within 10 mins dwelling time, the subsequent homogenizing process of IMCs interlayer took place with further prolonged dwell time, which caused the increase of grain size during the ripening process. Lifshitz-Slezov-Wahner (LSW) theory [161] was established to describe the homogenizing process based on the diffusive decomposition in the supersaturated solid solutions, known as the classic Ostwald ripening process through decreasing the interfacial energy between phases in a conservative system. Another Flux-driven ripening (FDR) [162] theory was also developed later to describe the Cu_6Sn_5 ripening process during Cu-Sn solid-liquid reaction, where the growth and ripening of scallop-type Cu_6Sn_5 grains occurred simultaneously. In FDR theory, it is assumed that the Cu atoms diffused from the Cu substrate only lead to the growth of hemispheric Cu_6Sn_5, without considering the Cu_3Sn. The FDR was usually conducted in an open system, thus the volume of IMC layer increased while the surface energy of phase was thought to be consistent, which is different with the LSW theory.

Basing on the EBSD results, the average size of IMC grains was approximately 0.26 μm within the micro-joint after 10 mins dwelling, and it became larger than 0.5 μm with the increase of dwell time more than 50 mins. As shown in Figure 6-8, the mean size of IMC grains is likely linear with the cube-root of dwell time ($\sim t^{1/3}$), then the homogenization of IMC grains seems to obey the LSW theory of ripening. However, the Cu/IMCs/Cu micro-joint was considered to be an open system rather than a close system in LSW theory, since the Cu atoms were kept diffusing from substrate into IMCs interlayer and the phase transformation reaction such as $Cu_6Sn_5 + 9Cu \rightarrow 5Cu_3Sn$ was expected to take place throughout the storage period. Thus, this phenomenon herein is more probably characterized by the FDR theory, where both processes of growth and ripening have occurred simultaneously in the IMCs interlayer. In particular, copper atoms diffused through grain boundaries mainly from copper substrate as a flux resource into IMCs layer during the whole evolution process. Therefore, the microstructural evolution of IMCs interlayer is predominantly controlled by diffusion of Cu atoms at the interface and almost boundaries.

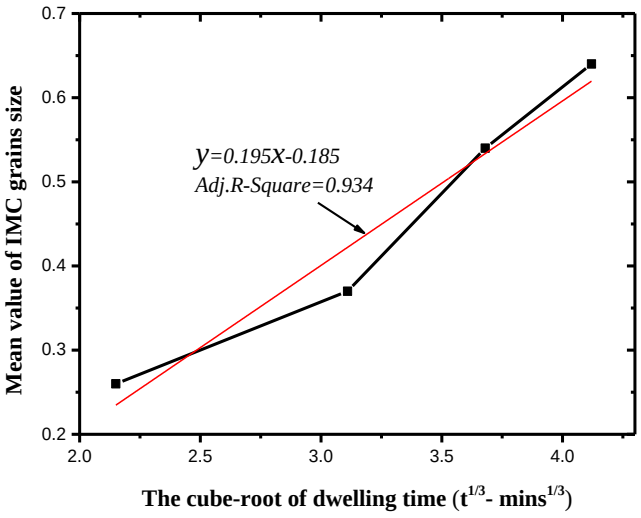

Figure 6-8 linear relationship between mean size of IMC grains and the cube-root of dwell time

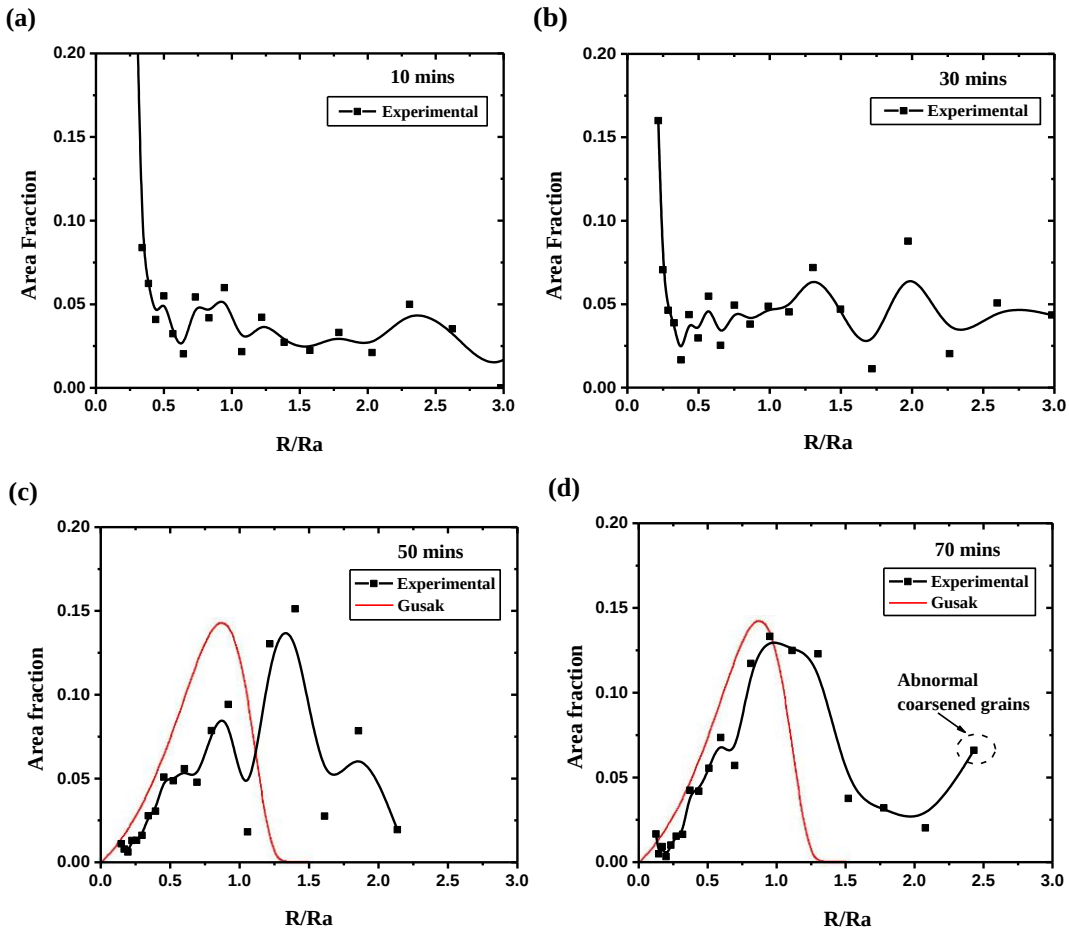

Figure 6-9 normalized grain size distribution of IMC interlayer formed at 260 °C with different dwell time (a) 10 mins; (b) 30 mins; (c) 50 mins and (d) 70 mins

Moreover, Figure 6-9 illustrates the distribution of normalized grain sizes of IMC (R/Ra, R-radius of grain, Ra-the average value of grain radius) as a function of dwell time. In the situations where the samples were kept for a long time, the distribution of normalized grain sizes tends to be regular, which is similar to the FDR distribution

based on Gusak's work, as shown in Figure 6-9(c) and (d). This means the microstructure of IMCs interlayer became much more stable and homogeneous in micro-joints after 50 mins or longer dwell time.

Then, further analysis on the characteristics of IMCs grains was carried out, and the morphologies of the IMC interlayer in both IQ map and GSO map are showed in Figure 6-10 for the specimens dwelled for 50 and 70 mins, respectively. The values of angles are represented by different colours in Figure 6-10 (b) and (d). The light green and yellow represent those grains with shape angles around 90 degrees, which are perpendicular to the copper substrates. It is apparent that the ratio of the amount of those certain grains in Cu_3Sn IMC interlayer after 70 mins dwelling is higher than that after 50 mins. Besides, Figure 6-11 shows the statistical results of misorientation distribution from experimental observation which measures number fraction of the grain boundaries with certain misorientation. Obviously, the low-misorientation grains boundaries are predominant within Cu_3Sn IMC for the samples with dwell time of 50 mins and 70 mins. Based on the analysis in reference [163], the misorientation distribution is primarily concentrated on small misorientation, so the grains tend to be clustered. Therefore, the Cu_3Sn IMC grains have a great tendency to grow along the vertical direction on copper substrates with the increasing of dwell time.

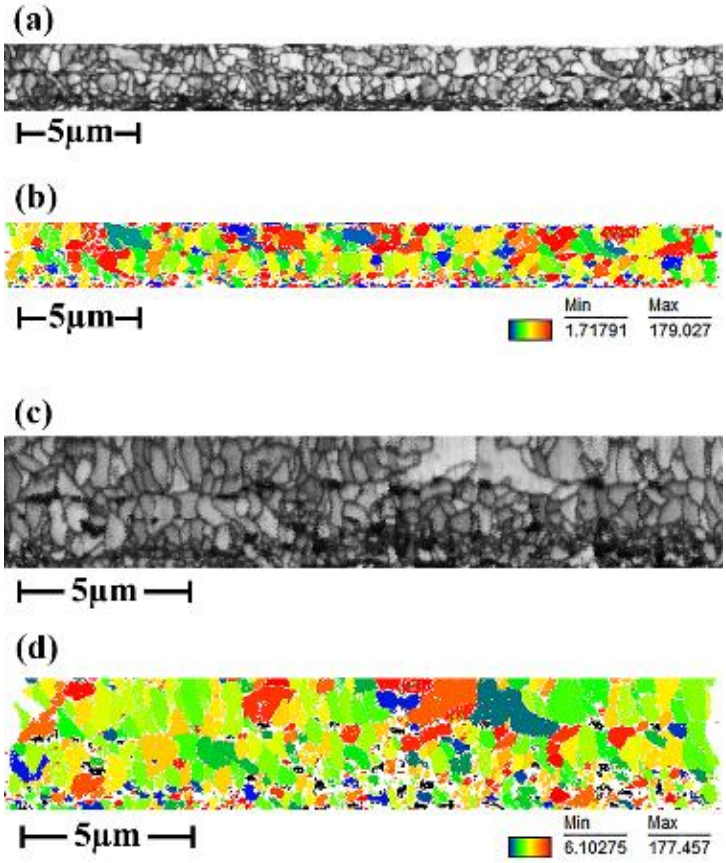

Figure 6-10 EBSD images of Cu_3Sn IMC interlayer formed with dwell time of 50 mins (a) IQ map and (b) GSO map; 70 mins: (c) IQ map and (d) GSO map

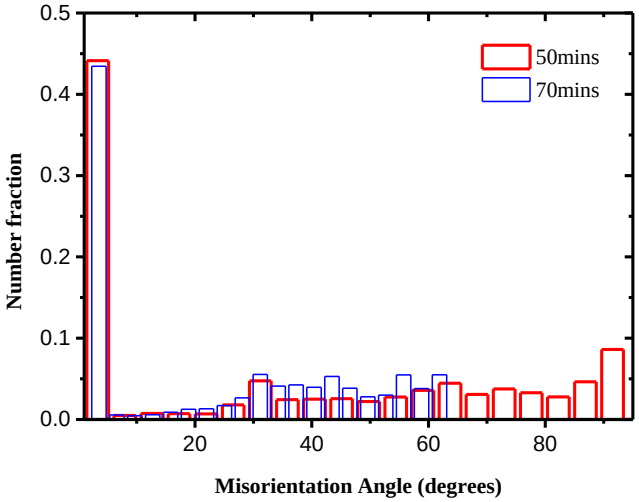

Figure 6-11 statistical results of misorientation distribution of IMC grains after 50 mins and 70 mins dwelling

6.4 Mechanism of microstructural evolution in the IMCs micro-joints

The major characteristics of SLID or TLP method used for soldering can be explained from the following two aspects: (1) the soldering temperature is constant and higher than the melting point of Sn-based solder alloy, leading the solder to becoming liquid phase at the first stage. As a consequence, Cu atoms will be uniformly distributed in the liquid Sn-based solder since a relative higher diffusion ratio of Cu atoms in the liquid solder than solid. (2) The liquid Sn solution will be saturated with copper atoms in a few minutes. Because of the higher melting temperature of the newly formed IMCs, the solidification stage is expected to occur even under the high temperature where the entire solder solution may still remain in a liquid condition, without need of a cooling process. Figure 6-12 reveals the microstructure of Cu_6Sn_5 IMC layer in the sample with initial structure as Cu/ Sn (5 µm)/Cu soldered by TLP method for 30 mins dwell time at 260 °C in vacuum chamber. The Cu_6Sn_5 grains varied and distributed irregularly, especially the ones in the middle or across the whole Cu_6Sn_5 layer appear like columnar grain as highlighted. Thus, when the interconnecting distance of the joint is less than 5 µm, the formation of IMC micro-joints can be articulated as follows: (1) the nucleation and growth of grains will happen simultaneously and quickly in the saturated Sn liquid solution. (2) The neighbouring grains appeared at the same time, so no time left for each grain growing up as a column. Then, the Cu_6Sn_5 layer with equiaxial grains formed in the middle of joints.

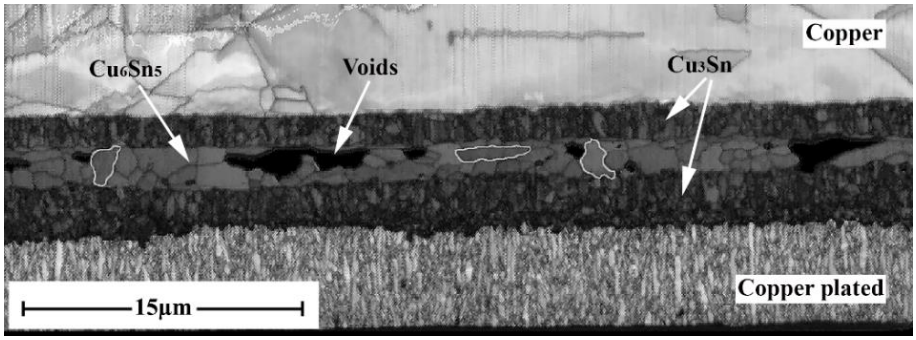

Figure 6-12 IQ map on cross-section of Cn/Sn (~5 µm)/Cu sandwich structure after soldering

Therefore, the IMCs microstructure which is evolving with dwell time can be considered as Figure 6-13(a-f), concerning at grain level systematically. First of all, due to the very thin interconnected thickness, the sandwich IMCs joint structure consisting of $Cu/Cu_3Sn/Cu_6Sn_5/ Cu_3Sn/Cu$ tends to be formed after TLP soldering as shown

in Figure 6-13(a). And the Cu_6Sn_5 grains are always larger than Cu_3Sn grains resulted from the Cu-Sn reaction. However, such joint structure is relatively unstable for the existence of Cu_6Sn_5 layer. At the interface close to Cu substrate, the concentration gradient and chemical reaction driving force cause the Cu atoms flux to diffuse from copper substrates into IMCs layer, as such the phase transformation of Cu_6Sn_5 into Cu_3Sn continues (Cu_6Sn_5 + 9 Cu → 5 Cu_3Sn). Meanwhile, these additional diffused Cu atoms can also further lead Sn atoms to be separated from Cu_6Sn_5 phase for an incomplete reaction, i.e. Cu_6Sn_5 + Cu → Cu_3Sn + Sn [150]. Then, Sn atoms are migrating toward to the Cu_3Sn layer or copper substrates. Thereby, the reaction such as 6 Cu + 5 Sn → Cu_6Sn_5 may take place within the Cu_3Sn layer to a certain extent. This is the primary reason why a mixture of Cu_6Sn_5 and Cu_3Sn IMCs phases was formed and observed in the experiments above.

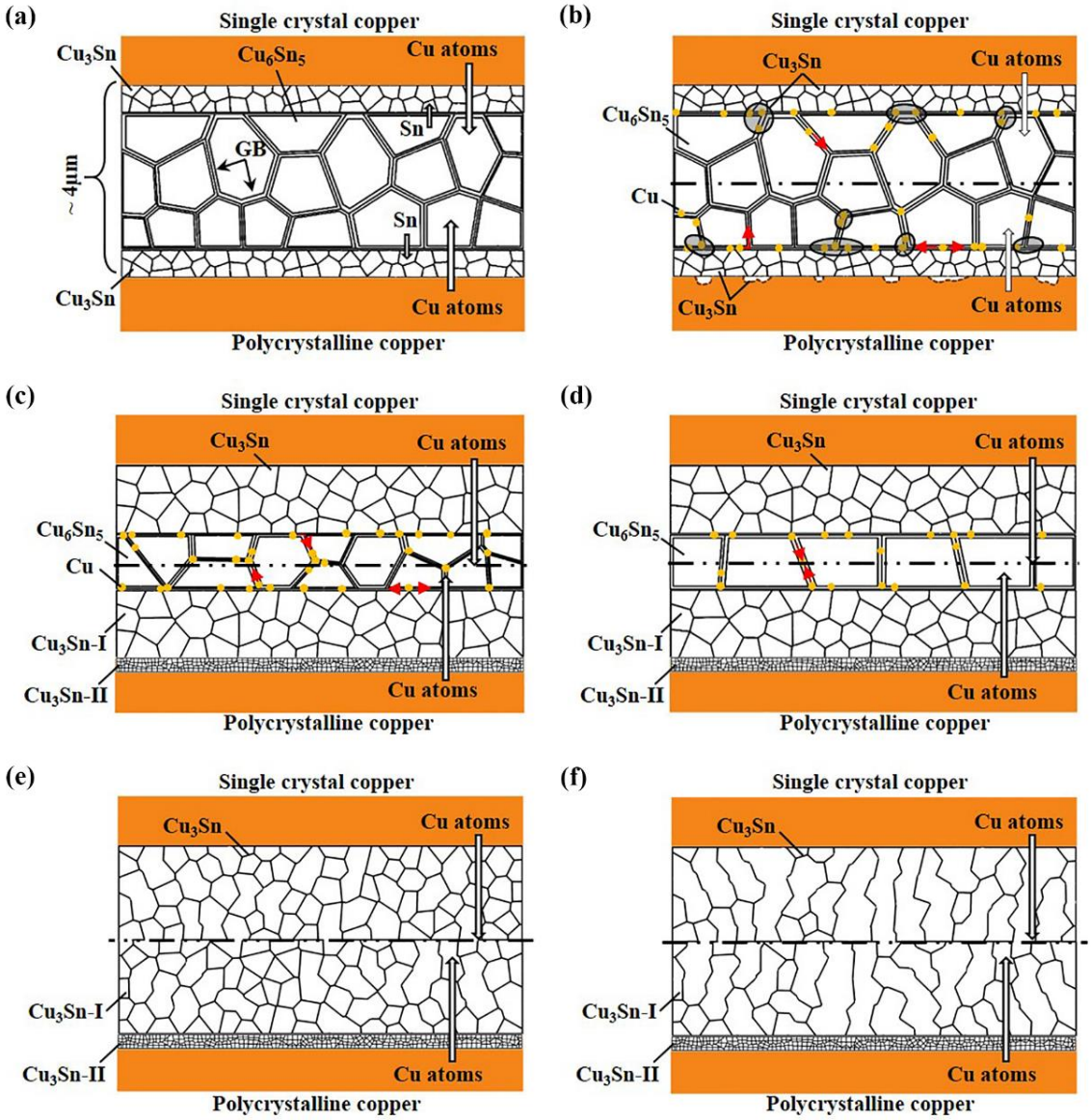

Figure 6-13 the schematic diagram to ascribe the microstructural evolution process of Cu_6Sn_5 grains in the course of transformation into Cu_3Sn grains: (a) the initial IMCs joints formed; (b) the Cu atoms (yellow dots) diffuse from copper substrate into Cu_6Sn_5 layer through GB and concentrate on the triple junction forming Cu_3Sn grains; (c) with dwell time increasing, the Cu_6Sn_5 layer in the middle consumed while the Cu_3Sn layers grow thicker, and the Cu_3Sn-II layer become continuous, mixing with some micro-voids; (d) another possible route similar to (c) for the Cu_6Sn_5 layer to propagate from (b), but through single crystal vertically; (e) complete Cu_3Sn formed in the joint; (f) the ripening of Cu_3Sn grains controlled by flux diffusion mechanism.

During this solid-solid reaction process, grain boundary diffusion is the predominant mechanism for transporting Cu and Sn atoms through the Cu_3Sn layer and diffusion in the Cu_6Sn_5 layer as the same time. Once the Cu atoms arrive at the interface of Cu_6Sn_5/Cu_3Sn, the reaction (Cu_6Sn_5 + 9 Cu → 5 Cu_3Sn) can be initiated immediately. On some occasions, the Cu atoms may be concentrated in the triple junctions of Cu_6Sn_5 grains by transporting through grain boundaries which act as channels. When the concentration of Cu is high enough at the triple junctions, the reaction can also occur to form Cu_3Sn locally within Cu_6Sn_5 IMC layer, as shown in Figure 6-13(b, c). Nevertheless, due to the shortened diffusing distance, the reaction on these locations in adjacent to Cu_6Sn_5/Cu_3Sn interface is much quicker compared to the places away from interface. Thus, this explains the observation encountered, i.e. with the increase of dwell time, the thickness of Cu_6Sn_5 layer is decreased while the increase of Cu_3Sn layer is taking the planar growth behavior. If the IMCs interlayer is thick enough, the microstructure of Cu_6Sn_5 will be different, as illustrated in Figure 6-13(d). Because the ripening of grains is expected to proceed throughout the whole soldering process, the Cu_6Sn_5 grains are likely to be single crystals in the perpendicular direction bridging the upper and lower Cu substrates. This kind of microstructure has been observed in Zhang's experiment [160, 164].

In addition, a second Cu_3Sn layer (Cu_3Sn-II) has formed between the Cu_3Sn-I layer and Cu substrate, constituting of ultra-fine grains. It is attributed to the numerous grain boundaries existing in the electroplated Cu layer due to the formation of finer grains, which can subsequently act as many nucleation sites and provide lots of the diffusing paths for Sn atoms at the same time. Thus, the Cu-Sn reaction on electroplated Cu layer is accelerated. The number of Cu_3Sn-II grains can dramatically increase, but unable to grow up under the restricted available spaces. As a result, the Cu_3Sn-II layer is constituted with equiaxial-grains which has been observed in the experiment. With the dwell time increasing, the Cu_3Sn-II layer can grow thicker and become more continuous towards the electroplated copper substrate. Meanwhile, the diffusion rate of Sn atoms is much slower than the rate of Cu in the Cu_3Sn layer [151], as such the Kirkendall voids are expected to present as the vacancies left behind the migration of Cu atoms. And, the volume contraction occurs during formation of the IMCs is approximately 7% for the Cu-Sn system [165], which may be the other cause that can contribute to the voids formation in the Cu_3Sn-II layer and Cu_3Sn-I layer.

After completion of the reactions, there will be primarily Cu_3Sn IMC remained at the interconnected joint as presented by Figure 6-13(e-f). The Cu_3Sn grains are more likely to be equiaxial shape, which are mixed with some Cu_6Sn_5 grains surrounding the coarse Cu_3Sn grains. Together with the analysis about gain size of Cu_3Sn IMC shown in Figure 6-9, the ripening of Cu_3Sn grains can proceed as dwell time increases. Since the steepest concentration gradient of Cu atoms is along the vertical direction, which will fundamentally affect the diffusion controlled ripening process in Cu_3Sn layer. Thus, the grain of Cu_3Sn IMC can propagate to be columnar shape when the ripening process of Cu_3Sn grains is completed as shown in Figure 6-13(f).

6.5 Mechanical property of Cu_3Sn IMC micro-joints

A micro-cantilever made by FIB from the sample formed with 70 minutes dwell time has been tested to observe the fracture surfaces after shearing by nanoindentation. The results are shown in Figure 6-14(a) and (b), from which, the details of fracture can be manifested in the enlarged images. The fractured surface on the porous Cu_3Sn presents numerous micro-voids, taking both convex and concave profiles as seen in Figure 6-14(c). On the opposite fractured surface in Figure 6-14(d), it is not surprised to see that voids are also distributed inside the IMC uniformly, and some steps due to the fracture at different height, as well as some intact grains can be clearly seen. This implies that both intergranular and transgranular fractures occurred simultaneously. In addition, the concave formed matches with the convex site on the opposite fracture surface.

From the profile of load versus depth recorded in Figure 6-15, the ultimate shear strength was calculated from the maximum loading force divided by the actual fractured area, which is approximately 176 MPa. This is much less than the calculated strength of single-crystal Cu_3Sn (>1.7 GPa) [92], but this is two times higher than the value according to Lee's work [108]. This drastic increase in strength can be attributed to the existence of finer grains of the Cu_3Sn layer, through the mechanism known as fine-grain strengthening [166]. Besides, considering low loading rate applied, there may be enough time left for the crack propagating along adjacent grain facets, then, the Brittle Intergranular Fracture (BIF) [167] occurred. Also, the interlocking effect among these multi-prismatic grains can further increase the shear strength, which tends to be ignored in the conventional solder joints with relative larger size of grains and tested under higher loading rate.

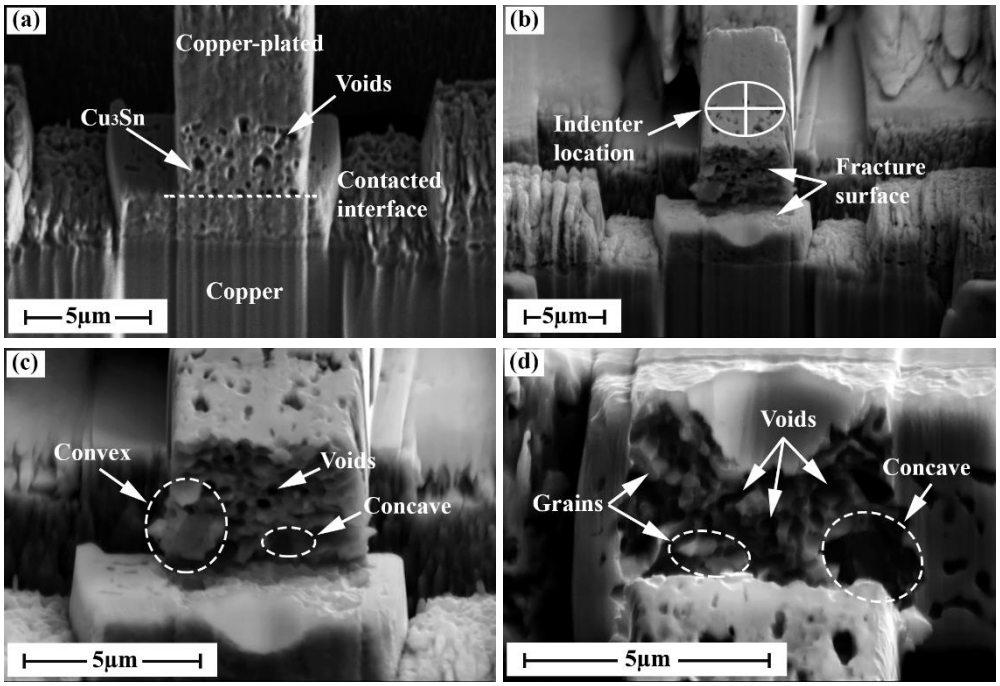

Figure 6-14 SEM images of micro-cantilever made by FIB before and after shearing by nanoindentation (a) micro-cantilever before test; (b) indenter location and micro-cantilever after test; (c) the upside fracture surface; (d) the downside fracture surface

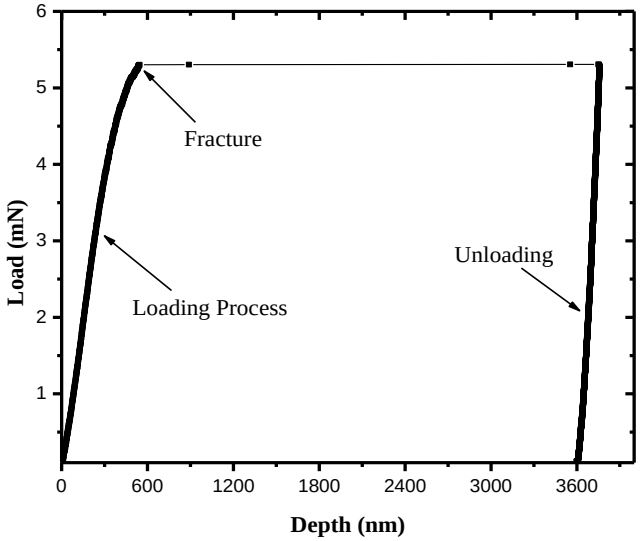

Figure 6-15 load-depth curve during the shear testing by nanoindentation

6.6 Summary

The results obtained from the experiments revealed the phase transformation process from Cu_6Sn_5 to Cu_3Sn with the increases of dwell time at the given temperature of 260 °C. It was found that the Cu_6Sn_5 grains initially formed at the interfaces of joints have been consumed gradually and subsequently converted into Cu_3Sn grains, and became a single Cu_3Sn IMC interconnect along with a homogenizing process under sufficient dwell time. The experimental result above can be summarised as the following:

(1) There were two layers of Cu_3Sn IMC growing continuously from both sides of copper substrates and merging each other along the central line of the joint. Afterwards, the IMCs interlayer was constituted with the coarse Cu_3Sn grains surrounding by thin Cu_6Sn_5 grains as a mixture. Particularly, a second Cu_3Sn thin layer with ultra-fine equiaxial grains and micro-voids appeared adjacent to the electroplated copper layer, which was not observed on the opposite side of interconnection near the oxygen-free rolled copper substrate.

(2) On the basis of the grain-boundary diffusion mechanism, the growth process and ripening of Cu_3Sn grains took place simultaneously with the depletion of Cu_6Sn_5 phase in the IMCs interlayer of the micro-joints. Therefore, this homogenization process of Cu_3Sn interlayer presented to obey the FDR theory well. With the increase of dwell time, Cu_3Sn grains tend to take columnar shape in perpendicular to the interface of IMC/Cu substrate at the end.

(3) The result derived from the shear test by nanoindentation indicates a relatively high shear strength of the IMC joints, though it involved with the porous Cu_3Sn layer. Both intergranular and transgranular fracture occurred in the Cu_3Sn micro-joint, which may reflect the implications of different fracture mechanisms at different locations.

Chapter 7 Microstructural Evolution and Mechanical Property of Cu-Sn-Ni IMCs Micro-interconnection

7.1 Introduction

With the miniaturization of electronics boosted by the 3D IC stacking packaging in recent years, a lower height of interconnection is needed than the solder bump using in conventional flip-chip before. A type of Cu-pillar bumps capped with Sn-based solder has been applied to realize the 3D interconnection less than 10 μm. However, as the volume of Sn-based solder is quite small, the complete consumption of solder would happen instead of the corrosion of Cu pads, which also accompanied with Kirkendall voids in the intermetallic compounds (IMCs) interlayer. Therefore, the Ni layer has also been suggested to use as a barrier in this situation [168, 169]. Since almost the prior investigations were proceeded in the joints with adequate Sn-solder, the situation where the micro-joint was completely transformed into the full Cu-Sn-Ni IMC interconnection has not been investigated much further. Some differences are expected to exist in the Cu-Sn IMCs joint with the addition of Ni. Thus, a systematic study has been done on the Cu-Sn-Ni IMCs micro-joints in this chapter, including the preparation of this type of micro-joints and the microstructural evolution within the Cu-Sn-Ni IMCs interlayer.

7.2 Experimental procedures

A commercial pure (99.9 wt.%) nickel-rolled foil with the size of 30 mm×15 mm×0.125 mm was used as substrate. The details about the procedures of electroplating to prepare the Ni/Sn/Cu sandwich structure was described in Chapter 3. According to the prior reports about Sn-Ni reaction [146], the reaction rate of Sn-Ni is much slower than the rate between Sn and Cu. Thus, in order to form the full IMCs micro-joints, the thickness of Sn-plated interlayer was designed to be around 1.5 μm for these Ni/Sn/Cu samples, which is thinner than that used for the investigation of Cu/Sn/Cu structure. And the soldering process was accomplished in the T-track oven following the profile shown in Figure 3-5(a).

The cross-section of these samples were polished well through the general grinding and polishing procedures. Afterwards, the morphology of IMCs on the cross-section of micro-joints was observed by FEG-SEM. Because the thickness of each IMC layer is less the 2 μm in these micro-joints with low stand-off height, which is approaching the resolution limit of the FEG-SEM imaging, thus both the methods of EDX and XRD have been utilized to identify the compositions of IMCs interlayer in this chapter. Furthermore, the morphology of Cu-Sn-Ni IMCs in vertical direction were revealed by the TEM observation.

In addition, the mechanical properties of Cu-Sn-Ni IMCs have been characterized through the nanoindentation machine, and the creep properties were also discussed. Moreover, the IMCs micro-cantilevers (Type II and III) designed in section 3.4.1 were fabricated by FIB and applied to conduct the in-situ nano-mechanical tests on the Cu-Sn-Ni IMCs layer, then the maximum fractural stress was calculated.

7.3 Microstructural evolution of Cu-Sn-Ni IMCs micro-joints

7.3.1 Formation process of Cu-Sn-Ni IMCs micro-joints

Figure 7-1(a) demonstrates the cross-section morphology of the Ni/Sn/Cu substrate sample heated up to 230 (±2) °C in T-track oven with the rate of 50 °C/min. A consistent IMCs interlayer has formed to connect the copper-plated layer and nickel substrate. Comparing the two interfaces (Cu/Sn and Sn/Ni), the up-interface was quite flat while some tiny IMC grains appeared on the down interface growing toward to the nickel substrate. This

phenomenon is supposed to be the result from different dissolution rates of Cu and Ni atoms in the melted Sn-plated layer. During the soldering process, the interfacial Cu dissolved in the melted Sn quickly, then the interface between the solid Cu-plated layer and the melted Sn layer kept smooth and straight. Meanwhile, Ni atoms entered the melted Sn in a low speed through the Sn/Ni interface. Then, it became clear that Sn atoms diffused into the Ni substrate along the grain boundaries preferentially.

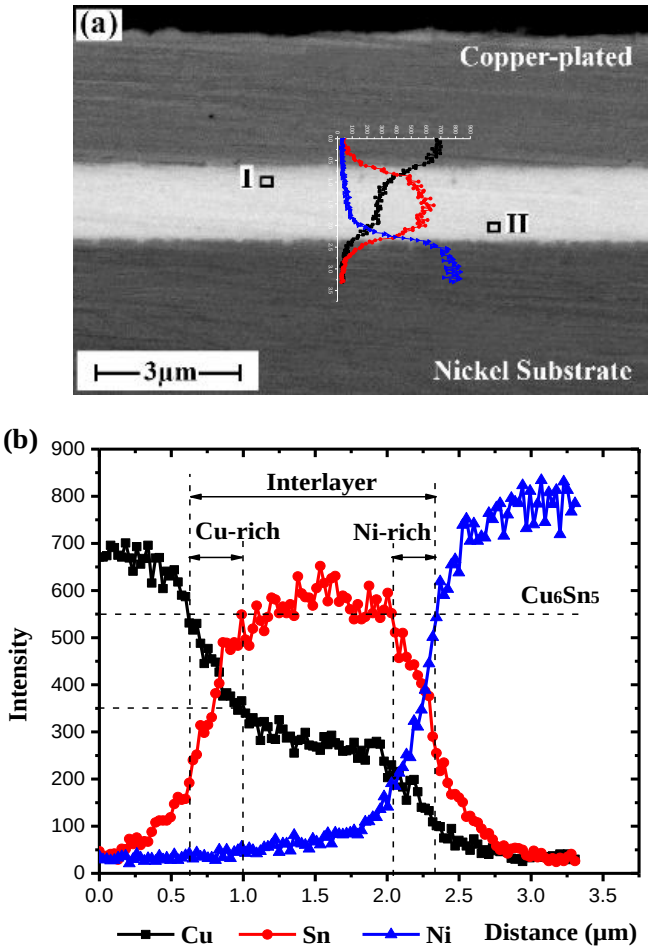

Figure 7-1 Cu-Sn-Ni IMCs micro-joint formed after 230 °C soldering
(a) FEG-SEM image (b) EDX line-scan result

In particular, the elements change of IMCs interlayer was detected by EDX line-scanning, the result is shown in Figure 7-1(b). Herein, the ratio between each elements can be calculated according to the formula (7-1), where, the N_x, M_x and I_x represent the amount of atoms, the molar mass and the intensity of EDX detection about the element of x (Cu, Sn or Ni) respectively. Then, a reference line is defined as the ratio of Cu and Sn atoms near the Cu-plated layer reaching the value of 6:5 for the first time.

$$N_{Cu} : N_{Sn} : N_{Ni} = \frac{I_{Cu}}{M_{Cu}} : \frac{I_{Sn}}{M_{Sn}} : \frac{I_{Ni}}{M_{Ni}} \tag{7-1}$$

When I_{Sn}≈550 and I_{Cu}≈350, N_{Cu}:N_{Sn}≈1.2, then the interlayer is divided into three parts, such as the Cu-rich area near the Cu-plated layer, the Ni-rich area close to the Ni substrate, and the Sn-rich area in the middle. Because this sample has been soldered at a low temperature and without the dwelling stage, thus both the Cu-rich and Ni-rich area are very thin (<0.5 μm) and it is difficult to distinguish from the interlayer in Figure 7-1(a). Even though,

the line-scanning result shows that the Cu-rich area is slightly larger than the Ni-rich area. Moreover, the compositions of the Sn-rich middle area have been analysed by EDX, which are Cu-59.46 at.%, Sn-35.46 at.%, Ni-5.08 at.% for the location I and Cu-46.00 at.%, Sn-41.78 at.%, Ni-12.22 at.% for the location II. It indicates that the interlayer is mainly constituted with $(Cu,Ni)_6Sn_5$, although the concentration of each elements is diverse to some extent.

On the basis of observation above, the formation mechanism of Cu-Sn-Ni IMCs micro-joints can be proposed. Since the interconnecting height of the sandwich structure has been minimized to 1.5 μm, the Cu and Ni atoms diffusing into the melted Sn-plated layer can be easily distributed homogenously across the whole interlayer. Then, $(Cu,Ni)_6Sn_5$ IMC is preferred to solidify simultaneously across the whole interlayer, rather than the directional solidification to form the scalloped IMCs grains.

7.3.2 Diffusion and growth behaviour in micro-joints

Different with the Cu/Sn/Cu structure, the interaction would happen for the existence of two types of interfaces (Cu/Sn and Ni/Sn) in the Ni/Sn/Cu structure. It is emphasized by the prior researchers that Ni atoms diffusing from Ni substrate to Cu/Sn interface will bring an effect on the Cu-Sn reaction [70, 72]. In this experiment, $Ni/(Cu,Ni)_6Sn_5/Cu$ micro-IMCs-joints have formed at the very early soldering stage. However, the interaction phenomenon is still supposed to reflect on the aspects of the subsequent atomic diffusion and IMCs growth behaviour in these Cu-Sn-Ni IMCs micro-joints. Therefore, the distribution of each elements and the thickness change of IMCs layers have been studied and analysed in the Cu-Sn-Ni IMCs micro-joints formed at 240 °C with different dwell time.

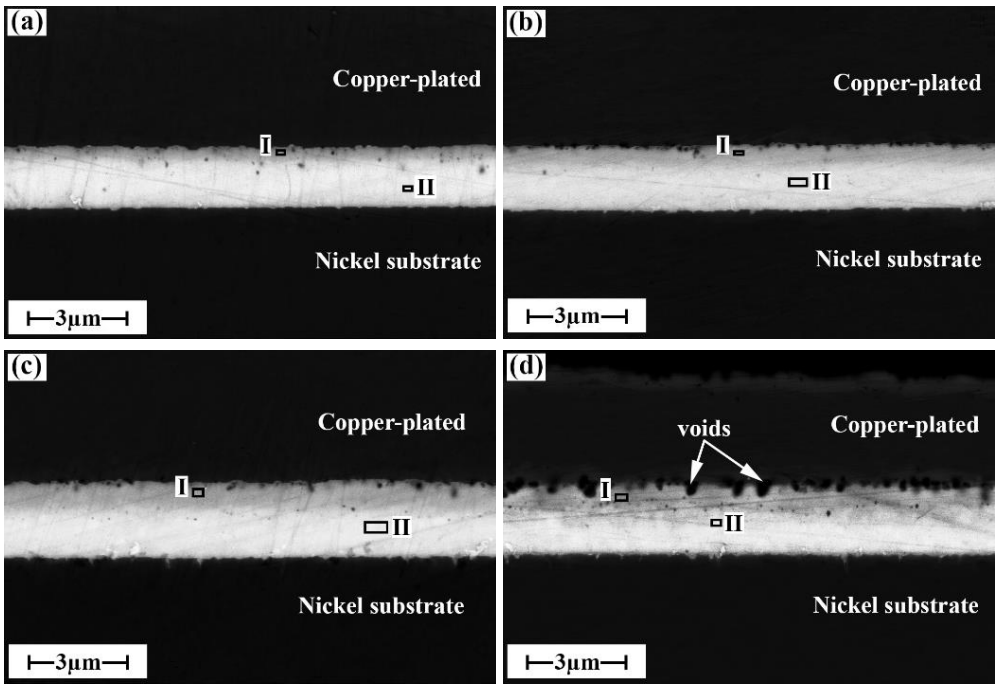

Figure 7-2 cross-section morphologies of Cu-Sn-Ni IMCs joints formed at 240 °C with different dwell time (a) 0 min; (b) 5 mins; (c) 15 mins; (d) 25 mins

Figure 7-2 presents the cross-sectional morphologies of micro-IMCs-joints which were soldered under 240 °C with 0, 5, 15 and 25 mins dwell time. Apparently, a dark-grey layer near the Cu-plated side has thickened with the increase of dwell time and where some of micro-voids have formed gradually, especially in the micro-joint with the dwell time of 25 mins (Figure 7-2 d). Then, with the help of EDX analysis, the compositions of each

IMCs layers have been detected and the results are listed in table 7-1. The dark-grey layer close to Cu-plated layer is mainly constituted with $(Cu,Ni)_3Sn$, while the other greyish layer is suggested to be $(Cu,Ni)_6Sn_5$. In General, Ni_3Sn_4 or Ni_3Sn_2 IMC layer would appear on the Ni/Sn interface, but which cannot be observed in these samples. With the prolongation of dwell time from 0 min to 25 mins, the amount of Ni atoms dissolved in the dark-grey Cu_3Sn layer has increased slightly from 2.5 at.% to 3.2 at.%, and a relatively large amount of change in the greyish Cu_6Sn_5 layer has been observed from 4.9 at.% to 8.5 at.%. However, the content of Ni atoms in these two types of Cu-Sn-Ni IMCs does not keep consistent with the relationship described by Yu [84] (Figure 2-12). This difference can be attributed to the thin $(Cu,Ni)_3Sn$ layer with the thickness of 0.5 ~1 μm, which is close to the resolution limit of FEG-SEM, and makes it possible that the EDX result on $(Cu,Ni)_3Sn$ contains the additional Ni atoms from the adjacent $(Cu,Ni)_6Sn_5$. And also, the other reason might be that the equilibrium status between $(Cu,Ni)_3Sn$ and $(Cu,Ni)_6Sn_5$ have not been achieved in the micro-joints formed at 240 °C.

Table 7-1 EDX results from FEG-SEM observation on IMCs interlayer formed at 240 °C

Dwell time	**0 min**		**5 mins**		**15 mins**		**25 mins**	
Atomic percent (at.%)	**I**	**II**	**I**	**II**	**I**	**II**	**I**	**II**
Cu	77.0	52.4	71.3	50.0	73.1	52.7	72.0	55.1
Sn	20.6	42.7	25.8	42.2	24.4	40.3	24.8	36.3
Ni	2.5	4.9	2.9	7.7	2.5	7.0	3.2	8.5

In order to better understand the microstructure of Cu-Sn-Ni IMCs micro-joints, the diffusion behavior of atoms in the IMCs interlayer has been analysed. Figure 7-3 illustrates the distribution of each elements in the micro-joints formed at 240 °C with the dwell time of 0 min and 25 mins. From the discrete images of FEG-SEM mapping, it is clear that the IMCs interlayer is homogeneous and the Cu and Sn atoms are the dominating composition. In the sample without any dwelling, the diffusion of Ni atoms is also observed, however, which is mainly concentrated around the Ni/Sn interface. When the dwell time has been prolonged to 25 mins, lots of Cu atoms have diffused into interlayer further, meanwhile, Sn atoms have diffused towards to Cu-plated layer and Ni substrate. Obviously, the Cu/Sn interface has become much fuzzy in Figure 7-3(d) than that in Figure 7-3(a), and the interfacial line seems to shift towards the Cu-plated layer. Comparing Figure 7-3(f) with (c), more Ni atoms can be found within the interlayer for longer dwell time, but the morphologies of Ni/Sn interfaces still do not change too much in both of the samples. All of the above signifies that the diffusion behaviours of each atoms have been kept with the increase of dwell time driving by the chemical concentration gradient. However, the degree of interfacial interaction between Cu and Sn is much more serious than that on the Ni/Sn interface.

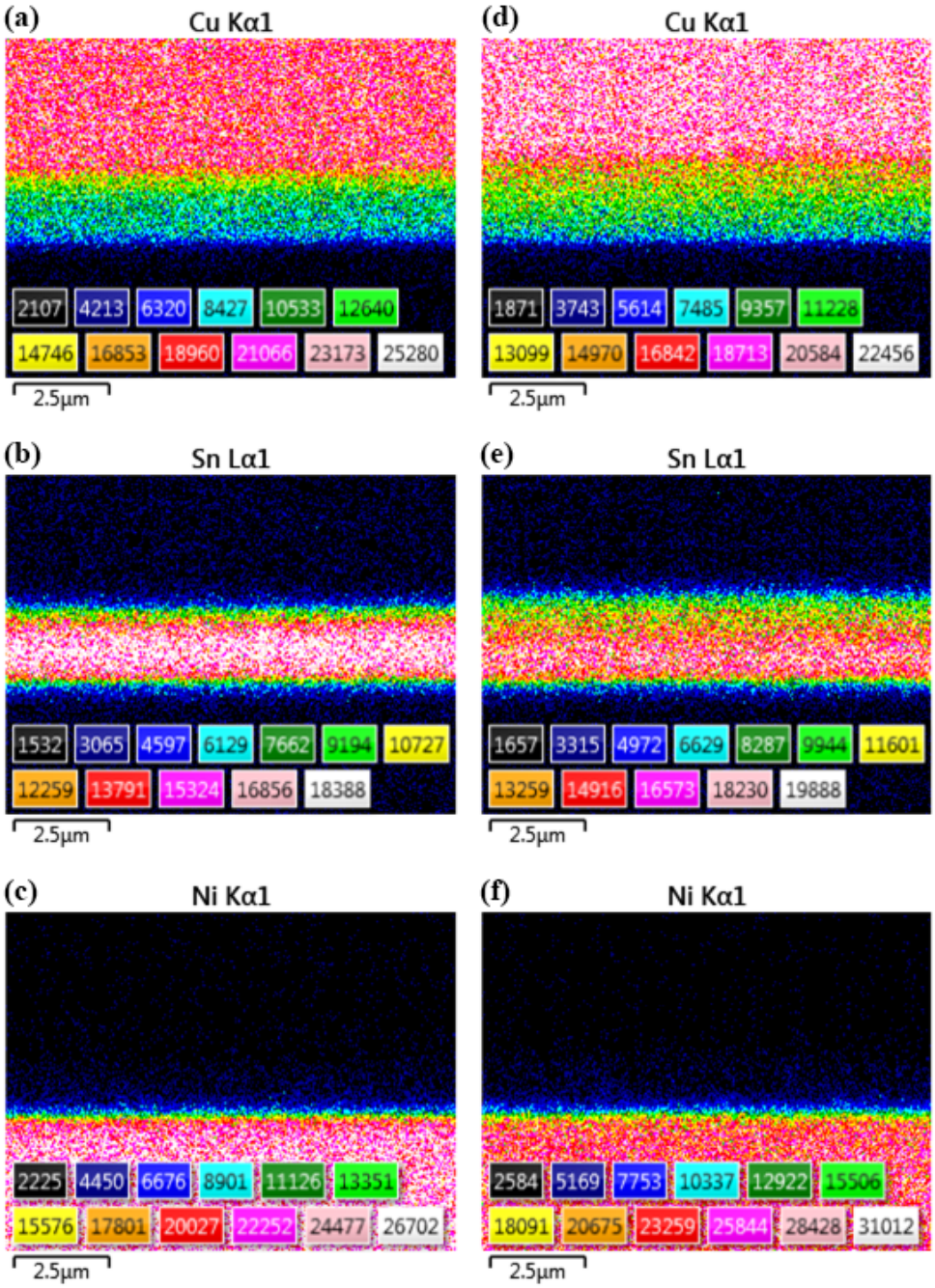

Figure 7-3 FEG-SEM discrete mapping on Cu-Sn-Ni micro-joints formed at 240 °C with different dwell time (Left: a-c) 0 min; (Right: d-f) 25 mins

With the assistance of EDX line-scanning analysis, the growth of each IMCs layers has been studied within the micro-joints formed at 240 °C with different dwell time. Using the same method introduced in section 7.3, the interfaces between each IMC layers are defined as shown in Figure 7-4.When I_{Sn}≈15000, I_{Cu}≈10000, and then the ratio of N_{Cu} to N_{Sn} is calculated to be around 1.2. That is the Cu_6Sn_5 IMC formed near the Cu-plated layer without the consideration of Ni atoms. In the Cu-rich area, the concentration of Cu atoms drops sharply versus the distance away from the Cu-played layer. Meanwhile, the amount of Sn atoms increases quickly and the addition of Ni atoms cannot be recognized easily. Together with the observation from FEG-SEM images, the Cu-rich layer is corresponding to the dark-grey area in the micro-joint, i.e. $(Cu,Ni)_3Sn$ or Cu_3Sn. Moreover, the

content of Sn and Cu atoms seems to be stable in the Sn-rich middle layer, and the amount of Ni atoms has some obvious increase. From the FEG-SEM images, this Sn-rich layer is thought to occupy the majority of the light-grey area, hence treated as the Sn-rich Cu_6Sn_5 layer. Besides, a thin Ni-rich layer close to the Ni substrate is also distinguished for the high content of Ni atoms, however, both the amount of Sn and Cu atoms deceases significantly, and the color of Ni-rich layer is quite similar with the Sn-rich Cu_6Sn_5 layer in these FEG-SEM images.

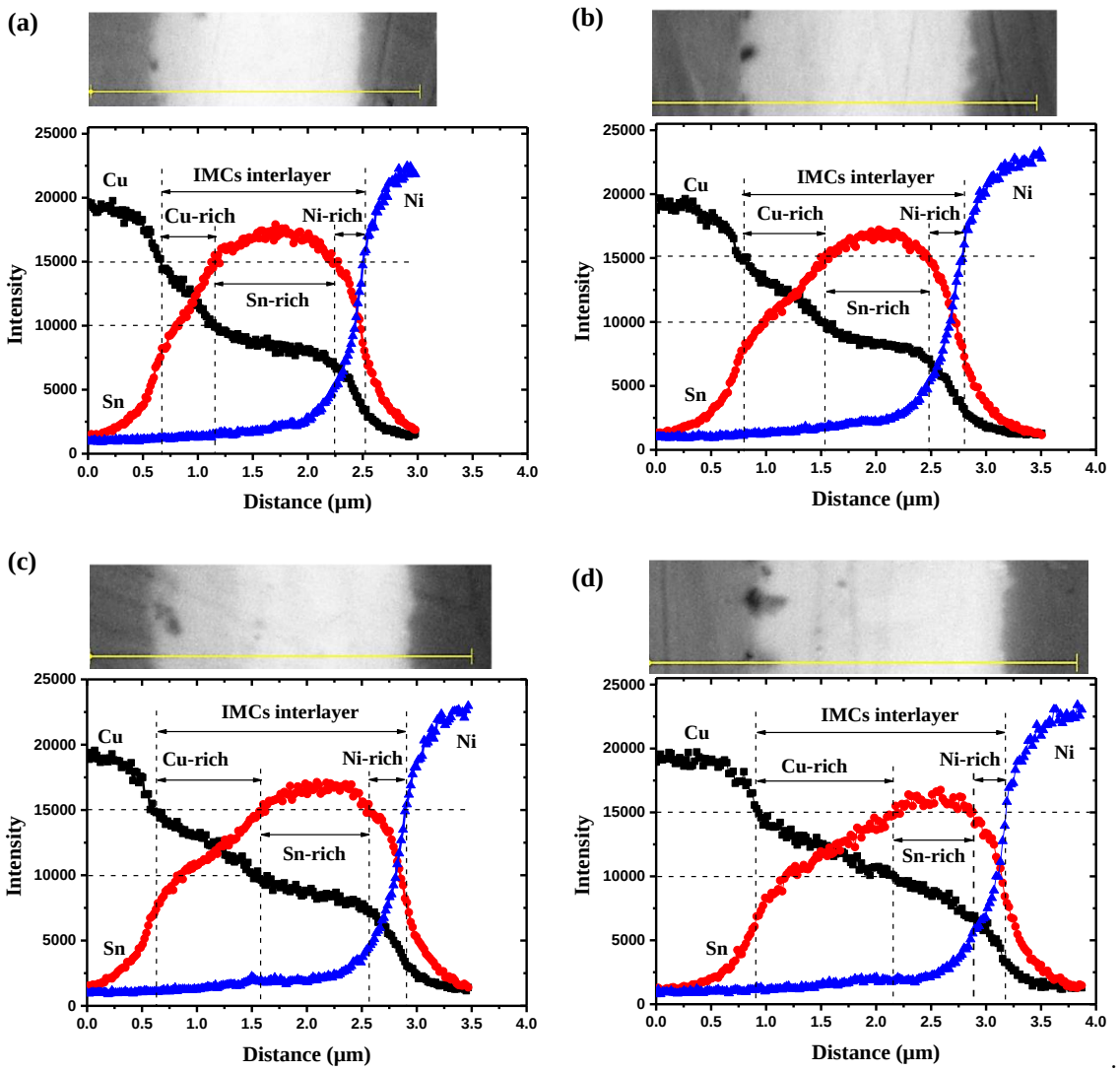

Figure 7-4 line-scan results of Cu-Sn-Ni IMCs micro-joints formed at 240 °C with different dwell time (a) 0 min; (b) 5 mins; (c) 15 mins; (d) 25 mins

Therefore, the thickness of each IMC layers within these micro-joints has been measured, and the results are given in Figure 7-5. The Cu_3Sn layer on Cu-plated side has thickened along with the increase of dwell time, whilst the increase of Ni-rich layer thickness is approximately negligible. At the start of dwelling stage from 0 min to 5 mins, the thickness of Sn-rich Cu_6Sn_5 layer has an obvious decrease, and then it keeps stable in the following 10 mins. Afterwards, the thickness of Sn-rich Cu_6Sn_5 drops again with the dwell time extended from 15 mins to 25 mins. On the whole, the total thickness of IMCs interlayer increases with the dwell time, and be fixed in these micro-joints after 15 mins dwelling. Therefore, two reasons are deduced for the growth of Cu_3Sn layer in the early dwelling stage (<5 mins): one is the Sn atoms diffusing into the Cu-plated layer made the

reaction of Sn + Cu→ Cu_3Sn happened; the other is the addition of Cu atoms into Cu_6Sn_5 layer promoted the phase transformation of Cu_6Sn_5 into Cu_3Sn. For those micro-joints experiencing a long dwell time at 240 °C, the thick Cu_3Sn layer increased the diffusing distance of Sn and Cu atoms. And the diffusion rate of Sn in Cu_3Sn layer is slower than that of Cu in Cu_3Sn. As a result, the major reaction occurred in the IMCs interlayer is Cu + Cu_6Sn_5 → Cu_3Sn, then the Cu_3Sn layer has thickened with the consumption of Cu_6Sn_5 layer.

Furthermore, the empirical power law was used to analyse the growth of Cu_3Sn on Cu-side in the Ni/Sn/Cu structure as shown in Figure 7-6. Comparing the situation on the Cu/Sn/Cu-plated structure under 240 °C, the growth factor (n) of 0.36 indicates the growth of $(Cu,Ni)_3Sn$ IMC was controlled mainly by the reaction, which is smaller than 0.48 getting from Cu/Sn/Cu-plated structure for only one side providing Cu atoms for reaction. And the growth coefficient (k) of 0.12 which is slightly lower than 0.19 from Cu/Sn/Cu-plated structure. The reason is that the Ni accelerated the diffusion of Sn in Cu_6Sn_5 [69] and the growth of Cu_3Sn has been suppressed to a certain extent.

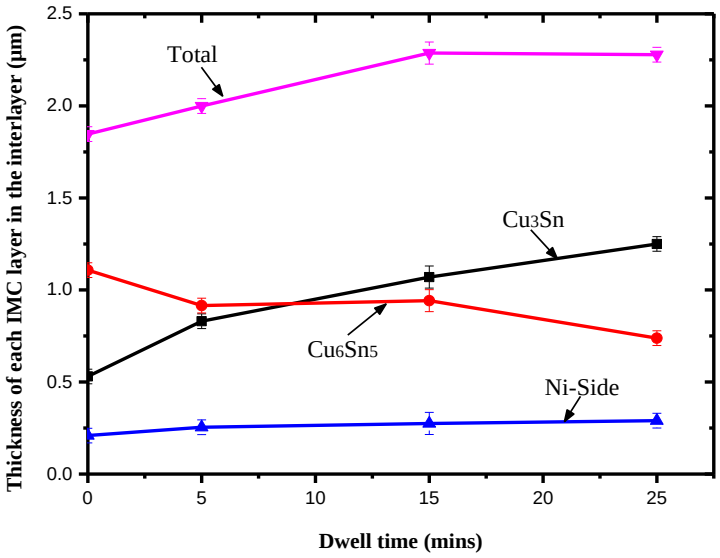

Figure 7-5 thickness of each layers in IMCs interlayer formed at 240 °C with different dwell time

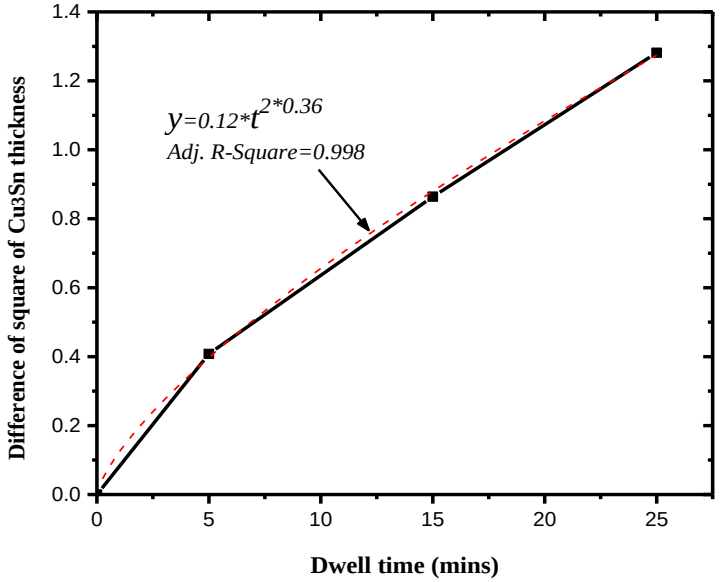

Figure 7-6 interfacial growth kinetics of $(Cu,Ni)_3Sn$ fitted by empirical formula

7.3.3 Effects of temperature and dwell time on microstructure

The cross-sectional images of the Cu-Sn-Ni IMCs micro-joints soldered at 260 °C are exhibited in Figure 7-7 and the EDX line-scanning results are provided by Figure 7-8. No obvious layers have been distinguished in the interlayer from the FEG-SEM images of micro-joints. However, there are still three layers which can be divided in chemical composition. The thickness of each layers in the micro-joint after 25 mins dwelling is visibly thicker than that in the micro-joint without dwelling, and the whole IMCs interlayer is about 2.4 μm. In particular, the Ni content within the Sn-rich area has increased while the amount of Sn has relatively reduced to be consistent with the ratio of Sn in Cu_6Sn_5. This Sn-rich area is likely to be homogenous as $(Cu,Ni)_6Sn_5$.

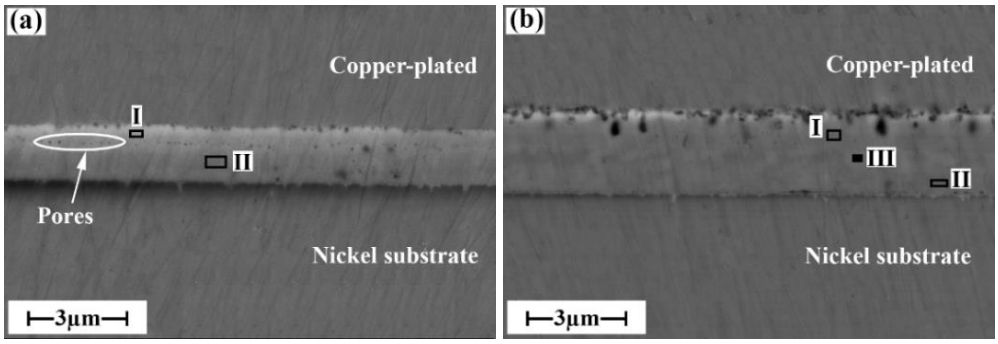

Figure 7-7 cross-sectional morphologies of Cu-Sn-Ni IMCs joints formed at 260 °C with different dwell time (a) 0 min; (b) 25 mins

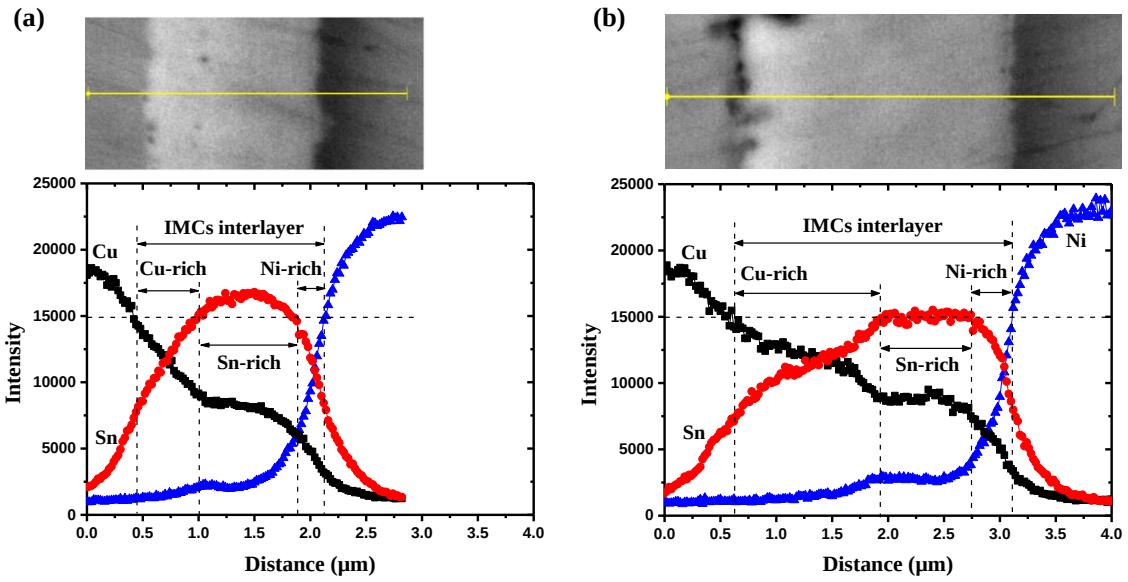

Figure 7-8 line-scanning results of Cu-Sn-Ni IMCs micro-joints formed at 260 °C with different dwell time (a) 0 min; (b) 25 mins

The constituent of some selected area on Figure 7-7 has been analysed by EDX and results are listed in table 7-2. The major layers as $(Cu,Ni)_3Sn$ on Cu-plated side, and $(Cu,Ni)_6Sn_5$ near the Ni substrate were detected in the samples with dwell time of 0 min at 260 °C. Especially, some extremely tiny pores arranging along the interface between $(Cu,Ni)_3Sn$ and $(Cu,Ni)_6Sn_5$ can be observed in Figure 7-7(a). These tiny pores may be caused by the different diffusion rate of Cu atoms in $(Cu,Ni)_3Sn$ and $(Cu,Ni)_6Sn_5$ layers, and also the volume shrinkage of IMCs in the process of phase transformation would be the other reason. Since the dwell time increased to 25 mins, plenty of Cu atoms have diffused into the IMCs interlayer which might fill those tiny pores. Thus none of tiny

pores appears in that micro-joint, but some micro-voids have emerged around interface between the $(Cu,Ni)_3Sn$ IMC and Cu-plated layer. Besides, the concentration of Cu and Ni atoms has a slight increase in the $(Cu,Ni)_6Sn_5$ layer accompany with a reduction of Sn atoms below 40 at%. This kind of $(Cu,Ni)_6Sn_5$ grains cannot be stable any longer, and the transformation of phases (Cu_6Sn_5→ Cu_3Sn) may occur locally [170]. In Figure 7-7(b), a mixture structure seems to form in the interlayer, however, none of this evidence has been detected yet in the micro-joint after 25 mins dwelling at 260 °C.

Table 7-2 EDX results from FEG-SEM observation on IMCs interlayer formed at 260 °C

Dwell time	**0 min**		**25 mins**		
Atomic percent (at.%)	**I**	**II**	**I**	**II**	**III**
Cu	72.2	49.2	71.3	51.4	53.8
Sn	24.4	40.9	25.0	34.5	35.1
Ni	3.3	12.3	3.7	14.2	11.1

Figure 7-9 records the cross-sectional morphologies of Cu-Sn-Ni IMCs micro-joints changed with dwell time from 0 to 25 mins at 290 °C. Furthermore, the composition on different areas of these IMCs interlayers have been analysed by EDX (Table 7-3). The layered structure of IMCs interlayer in micro-joint with the dwell time of 0 min (Figure 7-9 a) is similar to those formed at 240 °C, the dark-grey layer on Cu-plated layer is $(Cu,Ni)_3Sn$ and the greyish layer near the Ni substrate is still thought to be $(Cu,Ni)_6Sn_5$. Obviously, the high soldering temperature has accelerated the diffusion of atoms which is benefit for the growth of $(Cu,Ni)_3Sn$ on Cu-side. With the dwell time of 5 mins at 290 °C, the area of IMCs interlayer in this micro-joint has been widened as shown in Figure 7-9(b), and the greyish $(Cu,Ni)_6Sn_5$ IMCs layer becomes much cloudy. Moreover, the constitution of that greyish layer is nearly equivalent to the one soldered at 260 °C for 25 mins. As more and more Cu and Ni atoms have dissolved in the IMCs interlayer, the Sn content decreases to be only 33.77 at.% as a result.

As expected, the phase transformation within IMCs interlayer happened when the dwell time increased to 15 mins. Different with the prior layered structure, the IMCs interlayer turns to be a whole as shown in Figure 7-9(c), and the previous $(Cu,Ni)_6Sn_5$ IMC layer was transformed into $(Cu,Ni)_3Sn$ IMC layer. This new $(Cu,Ni)_3Sn$ IMC layer close to Ni substrate has a lower concentration of Cu atoms and a relative higher amount of Ni atoms and Sn atoms than that in $(Cu,Ni)_3Sn$ IMC layer on the Cu-plated side. Besides, a continuous thin substance with light-grey colour on the top surface of Ni substrate can be noticed in Figure 7-9(c). With the dwell time rising to 25 mins, some Kirkendall voids with a large size have formed on the interface of IMCs/Cu-plated layer as projected in Figure 7-9(d). In particular, the appearance of discontinuous light-grey phases in the middle makes the whole interlayer separated into the up and down two parts. Also, something similar with the light-grey substance can be observed on the Ni substrate.

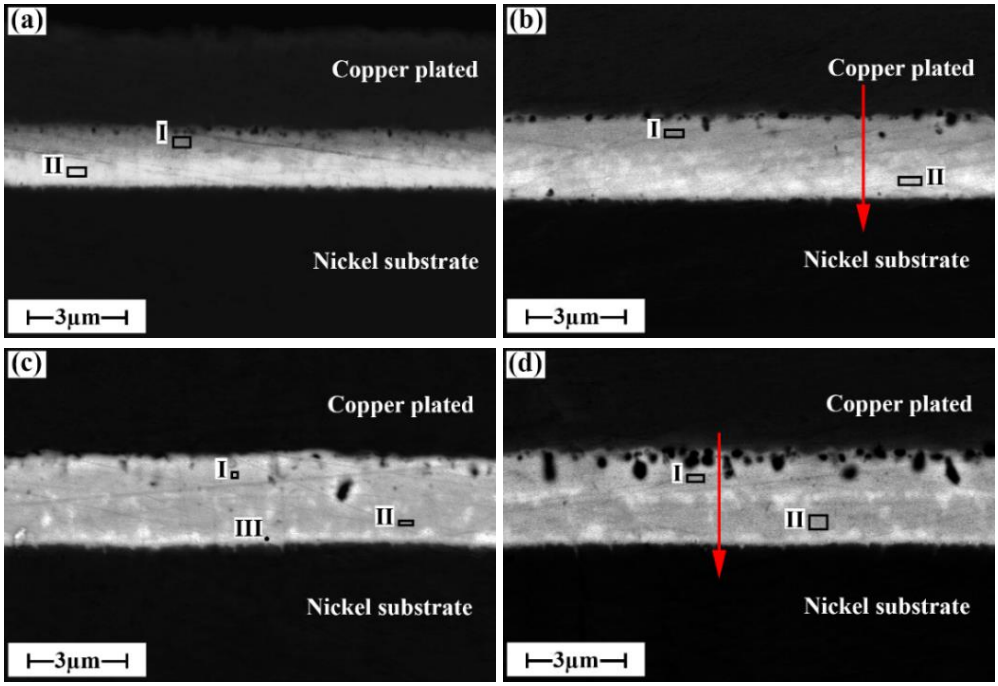

Figure 7-9 cross-sectional morphologies of Cu-Sn-Ni IMCs joints formed at 290 °C with different dwell time (a) 0 min; (b) 5 mins; (c) 15 mins; (d) 25 mins

Table 7-3 EDX results from FEG-SEM observation on IMCs interlayer formed at 290 °C

Dwell time	**0 min**		**5 mins**		**15 mins**			**25 mins**	
Atomic percent (at.%)	**I**	**II**	**I**	**II**	**I**	**II**	**III**	**I**	**II**
Cu	75.0	48.2	74.49	51.22	72.6	66.2	48.4	73.39	59.21
Sn	22.4	39.1	22.67	33.77	24.8	27.6	29.1	23.94	25.3
Ni	2.5	12.7	2.84	15.01	2.6	6.2	22.5	2.67	15.49

Furthermore, the EDX line-scanning has been conducted on the cross-sections of the micro-joints with dwell time of 5 mins and 25 mins. Comparing the Figure 7-10 (a) and (b), the concentration of Cu atoms in the new $(Cu,Ni)_3Sn$ IMC near Ni substrate has promoted to approach the level of Cu atoms in $(Cu,Ni)_3Sn$ IMC on Cu-side with the prolonged dwell time. Thus, it is interpreted that Kirkendall voids appeared on the interface between $(Cu,Ni)_3Sn$ IMC and Cu-plated layer for the migration of massive Cu atoms towards the Ni substrate. Meanwhile, Sn atoms in the down layer near Ni substrate have a tendency to diffuse into the up layer, and to be more homogenous within the whole interlayer for a longer time of heat treatment. In accordance with the observation from FEG-SEM images, a sudden decrease of Cu atoms can be found around the center-line of IMCs interlayer accompany with the increase of Sn and Ni atoms, this phenomenon is reflected clearly in the micro-joint with 25 mins dwelling at 290 °C (Figure 7-10 b).

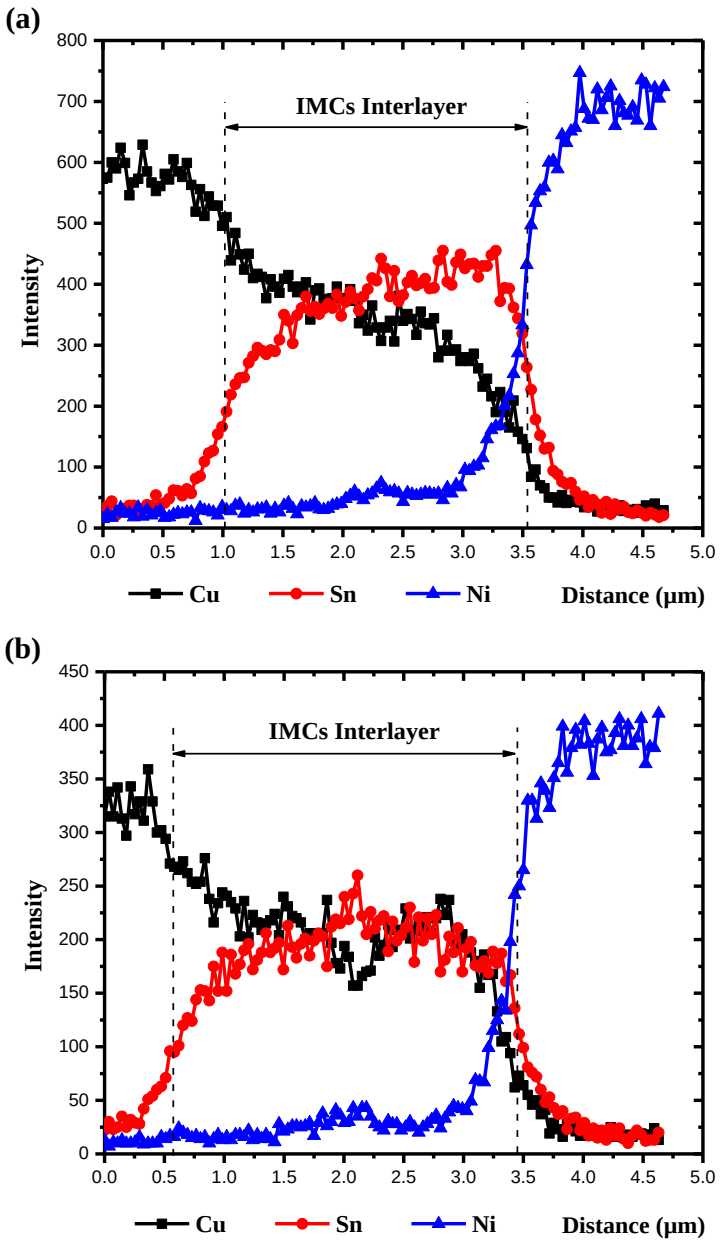

Figure 7-10 line-scan results of Cu-Sn-Ni IMCs micro-joints formed at 290 °C with different dwell time (a) 5 mins; (b) 25 mins

In addition, considering the effect of FEG-SEM electron beam spot size on the accuracy of EDX measurement, the method of TEM has utilized to further analyse the microstructure and composition of IMCs interlayer in micro-joint after 25 mins dwelling at 290 °C. As illustrated in Figure 7-11, some coarse grains exist in the IMCs interlayer, however, the size of them is still less than 1 μm. Bits of IMCs penetrating into the Ni substrate can be observed as well, which is consistent with the description of IMC growth manner on Sn/Ni interface in section 7.3. Moreover, the TEM mapping results are given as the following in Figure 7-12. It is worthy noticing that the segregation of Ni element takes place locally, mainly around the Ni substrate/IMCs interface and the center-line of IMCs interlayer. At the same time, the Cu concentration in those Ni-rich area is less than that none Ni-rich area. And the half of IMCs interlayer close to Cu-plate side nearly does not contain any Ni element. Focusing on the composition of certain area marked in Figure 7-11, the EDX results are provided by table 7-4. It is obvious

that the detected value of Ni content in the selected area as Figure 7-9(d) is higher than what is measured by TEM-EDX. It might be caused by the different magnification and a large area has been included for the measurement by SEM-EDX. In fact, there is a low Ni content in those none Ni-rich area wherever near the Cu-plated side or the Ni substrate.

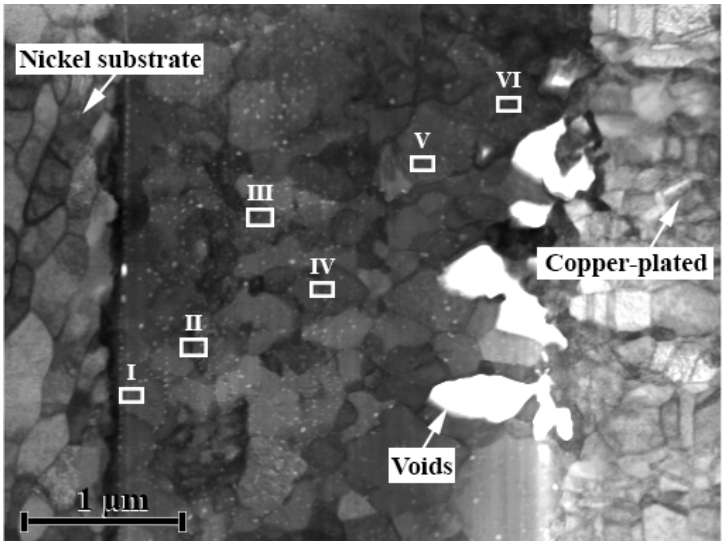

Figure 7-11 TEM bright field image on vertical section of micro-joint formed at 290 °C for 25 mins

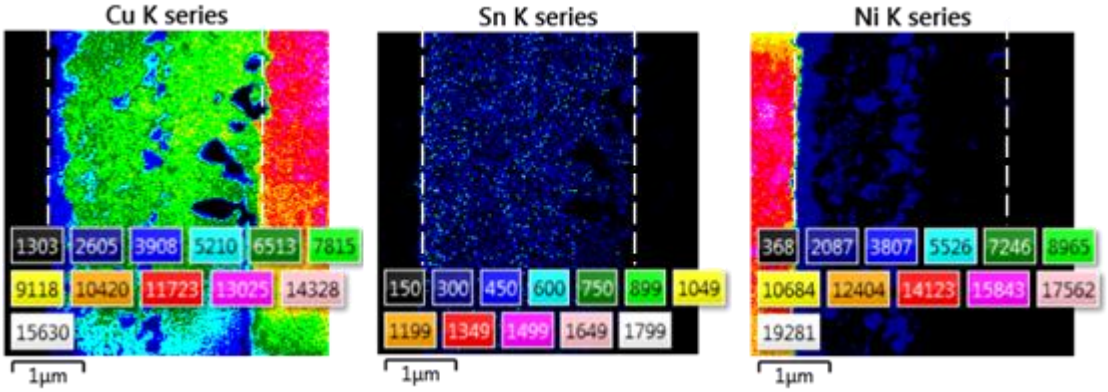

Figure 7-12 TEM discrete mapping images of Cu-Sn-Ni micro-joint formed at 290 °C for 25 mins

Table 7-4 EDX results from TEM observation on IMCs interlayer formed at 290 °C

Atomic percent (at.%)	I	II	III	IV	V	VI
Cu	39.3	65.9	79.7	46.7	79.3	80.5
Sn	39.9	28.9	18.8	33.3	19.7	19.0
Ni	20.9	5.2	1.5	20.1	1.1	0.5

7.3.4 Evolution process of Cu-Sn-Ni IMCs micro-joints

In order to better identify the types of Cu-Sn-Ni IMCs in these micro-joints, XRD detection has been applied on the IMCs interlayers from three representative micro-joints: (1) the one was formed at 240 °C/15 mins, having the typical two-layer structure of IMCs interlayer; (2) the other one was formed at 290 °C/5 mins, where the

interfaces between different IMC layers became fuzzy; and (3) the another one has a longest dwelling at 290 °C for 25 mins, then the Ni segregation appeared in the IMCs interlayer. The corresponding detection results are presented in Figure 7-13. It is evident that the main components of IMCs interlayer in these micro-joints under the soldering temperature of 240~290 °C are $(Cu,Ni)_6Sn_5$ and $(Cu,Ni)_3Sn$, which is consistent with the prior EDX analysis. Especially, Ni_3Sn_4 IMC was detected only in the micro-joints soldering at 240 °C for 15 mins. It means that the Ni-Sn reaction has actually happened between the Ni substrate and Sn solder layer during the soldering process, however it is too thin to be observed by FEG-SEM images. The composition of IMCs interlayer does not change with the dwell time at 290 °C, and any of the Ni-Sn production does not appear even for the micro-joint with 25 mins dwelling.

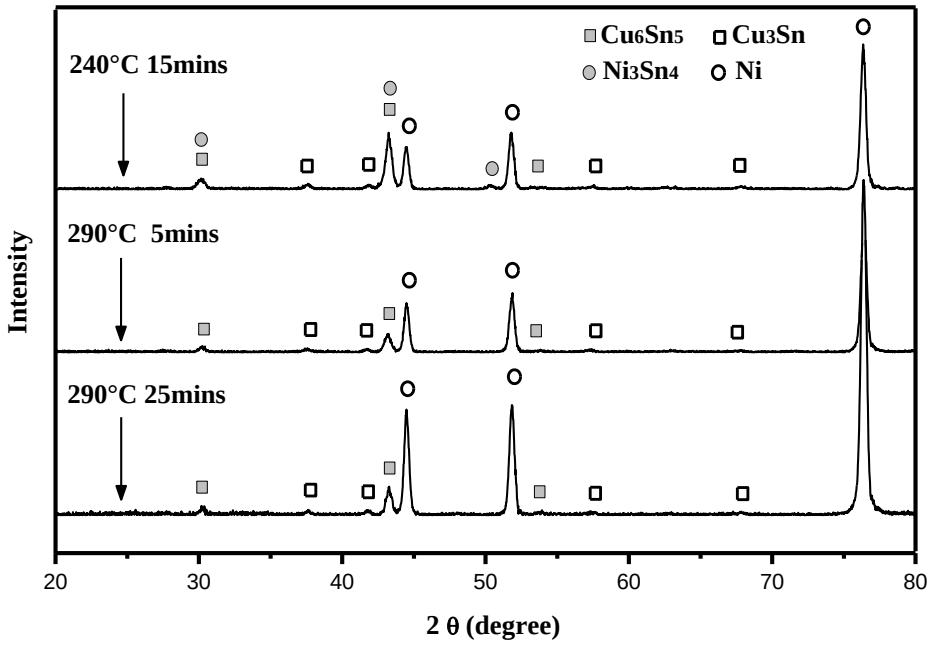

Figure 7-13 XRD detection results of the Cu-Sn-Ni IMCs interlayers

On the basis of Cu-Sn and Ni-Sn binary phase diagrams, the types of reaction and phase transformation are almost constant in the temperature range of 240 °C to 290 °C. Thus the hypothesis is made as the microstructure of micro-joints formed at 290 °C with a certain dwell time will be similar with the micro-joints formed at 240 °C with a relative long dwell time. Then, the experimental data of Cu-Sn-Ni IMCs compositions in those micro-joints have been plotted on the Cu-Sn-Ni ternary phase diagram at 240 °C. As shown in Figure 7-14, the red-triangle points represent the data combining the SEM-EDX and XRD results for micro-joint formed at 240 °C/15 mins, while the blue-diamond points is come from the micro-joint formed at 290 °C/25 mins through TEM-EDX measurement. The dashed lines connecting the different points reveal the diffusion paths of Cu and Ni atoms in these solid Cu-Sn-Ni IMCs micro-joints at 240~290 °C, and the range of IMCs composition is clarified as well. It is no doubt that the diffusion of Cu atoms in IMCs interlayer was much faster than Ni atoms, then the amount of Cu atoms increasing with dwell time makes the microstructure of IMCs interlayer changed dramatically. it is evident that the inter-reaction has taken place in the Ni/IMCs/Cu structure. Since the thin interconnecting height of micro-joints allowed lots of Cu atoms diffusing to the Sn/Ni interface quickly at high bonding temperature, the initial product (Ni_3Sn_4) from Ni-Sn reaction was changed in the way as $Ni_3Sn_4 + Cu \rightarrow (Cu,Ni)_6Sn_5$. Or, the Cu-Sn reaction has become predominant on the Ni substrate which supressed the Ni-Sn reaction, then the $(Cu,Ni)_6Sn_5$ was produced directly for the Cu-Sn-Ni ternary reaction.

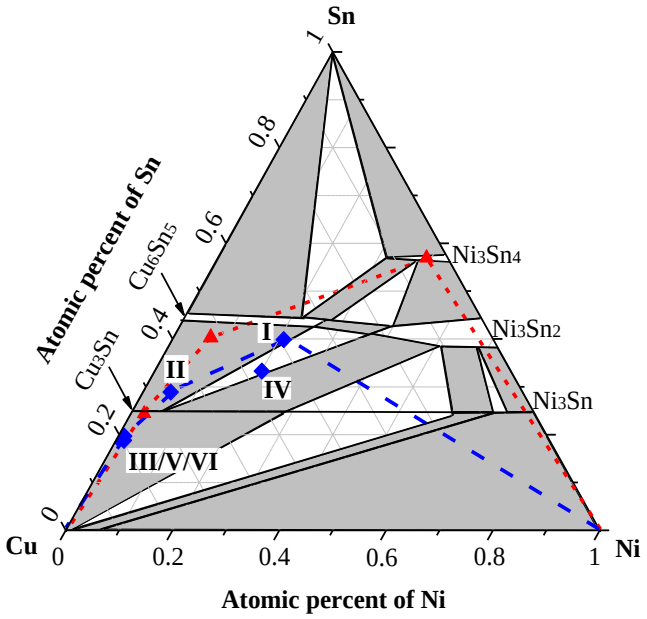

Figure 7-14 the evolution path of Cu-Sn-Ni IMCs in micro-joints under 240~290 °C (▲-the results from the micro-joint formed at 240 °C/15 mins; ◆- the results from the micro-joint formed at 290 °C/25 mins)

Moreover, the microstructural formation process of these Ni/IMCs/Cu micro-joints can be described systematically by Figure 7-15, where the yellow dots are used as the Cu atoms and the grey dots are for the Ni atoms. During the TLP soldering process, both the Cu and Ni atoms have dissolved in the molten Sn-plated layer, and absolutely vast of Cu atoms departed from the Cu-plated layer to reach the opposite Ni substrate in a short time. Meanwhile, few Ni atoms went across the Sn interlayer and arrived at the Cu-plated layer for the low diffusion rate, as shown in Figure 7-15(a). Then, the solidification has proceeded with the formation of IMCs in the micro-joints when the composition of interlayer approached to a certain level. The structure of micro-joints is presented in Figure 7-15(b) like that: Cu-rich $(Cu,Ni)_3Sn$ layer on the Cu-plated layer and the Sn-rich $(Cu,Ni)_6Sn_5$ near the Ni substrate, where a very thin layer of Ni_3Sn_4 is negligible.

Afterwards, the solid diffusion of Cu and Ni atoms is the main mechanism for the microstructural evolution of these micro-joints. Through the reaction of $(Cu,Ni)_6Sn_5$ + Cu → $(Cu,Ni)_3Sn$, the $(Cu,Ni)_3Sn$ layer has thickened in a layer structure. As a result, the thickness of $(Cu,Ni)_6Sn_5$ layer has been correspondingly deceased and the Ni content of $(Cu,Ni)_6Sn_5$ layer has been increased. However, with the increase of dwell time, the interface between two types of IMC layers became ambiguous for the emerging of Ni-rich area around the center-line of IMCs interlayer. One of the reasons is that Ni atoms in the $(Cu,Ni)_3Sn$ layer have been pushed by the diffusing Cu atoms, and then moved out along with the migration direction of Cu atoms. Then, the Ni content around the $(Cu,Ni)_3Sn/(Cu,Ni)_6Sn_5$ interface is much higher than the other area. And the other reason is the lower solid-solubility of Ni in Cu_3Sn than that in Cu_6Sn_5, which makes the redundant Ni atoms excluded from the initial $(Cu,Ni)_6Sn_5$ grains in the phase transformation process, and then the segregation of Ni atoms happened. Since the higher content of Ni atoms makes the $(Cu,Ni)_6Sn_5$ grains more stable in thermal dynamics [84], therefore these Ni-rich $(Cu,Ni)_6Sn_5$ grains have been preserved around the center-line, even though the other $(Cu,Ni)_6Sn_5$ grains have transformed into $(Cu,Ni)_3Sn$, as described by Figure 7-15(c). In addition, because the Ni atoms have kept diffusing from the Ni substrate into IMCs interlayer for the existence of chemical concentration gradient, but having a relative low diffusion rate. Then the thin Ni-rich $(Cu,Ni)_6Sn_5$ layer has formed on the Ni substrate, and the final microstructure of Cu-Sn-Ni IMCs micro-joints turns to be similar with the Figure 7-15(d).

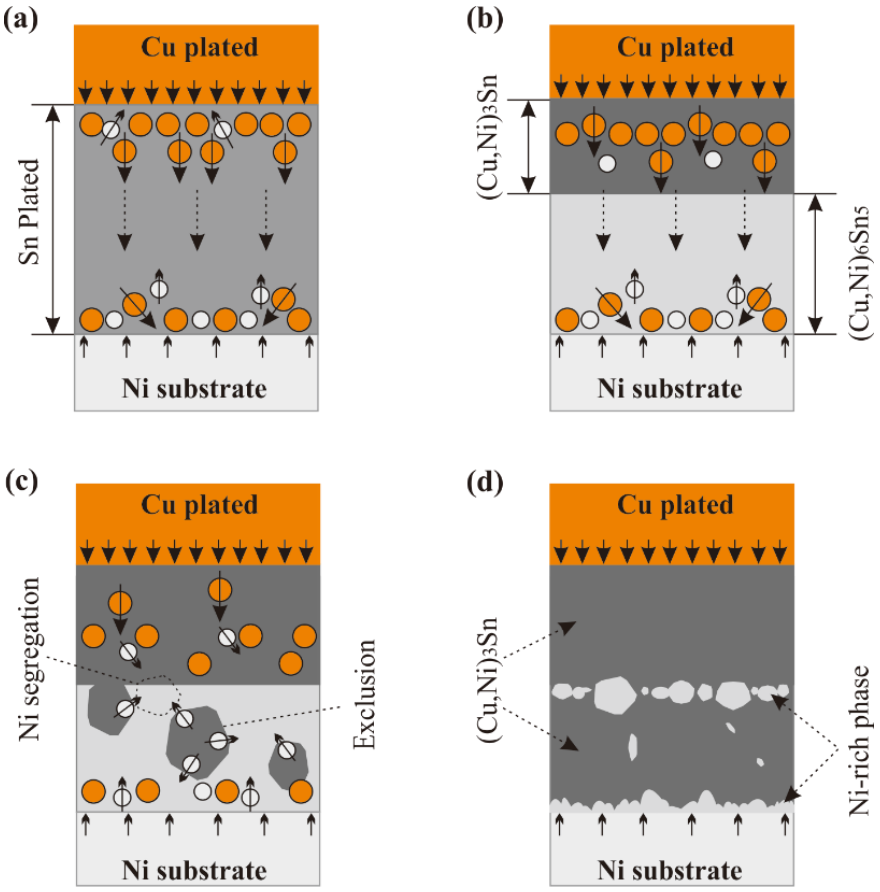

Figure 7-15 microstructural evolution process of Cu-Sn-Ni IMCs micro-joints (●-Cu atom; ○-Ni atom) (a) Cu and Ni atoms diffusing in the molten Sn layer; (b) IMCs interlayer formed containing $(Cu,Ni)_3Sn$ and $(Cu,Ni)_6Sn_5$ mainly; (c) $(Cu,Ni)_6Sn_5$ transformed into $(Cu, Ni)_3Sn$ accompany with the exclusion of Ni atoms and then Ni segregation occurred; (d) Ni-rich phase appeared around the center-line of $(Cu,Ni)_3Sn$ interlayer and adjacent to the Ni substrate

7.4 Mechanical properties of Cu-Sn-Ni IMCs

After removing some of the Cu-plated layer covering on the IMCs interlayer, two types of Cu-Sn-Ni IMCs interlayers have been observed by the optical microscopy, the schematic diagrams of that are shown in Figure 7-16. From the micro-joint formed at the condition of 240 °C/15 mins, two layers can be distinguished as the thick $(Cu,Ni)_6Sn_5$ layer beneath the up layer of thin $(Cu,Ni)_3Sn$. Hence this kind of sample has been used to measure the properties of $(Cu,Ni)_6Sn_5$ through nanoindentation. Besides, there are not obvious different layers to constitute the interlayer in the micro-joints after 5~25 mins dwelling at 290 °C. Thus, these specimens have be selected as the objects to study the properties of $(Cu,Ni)_3Sn$.

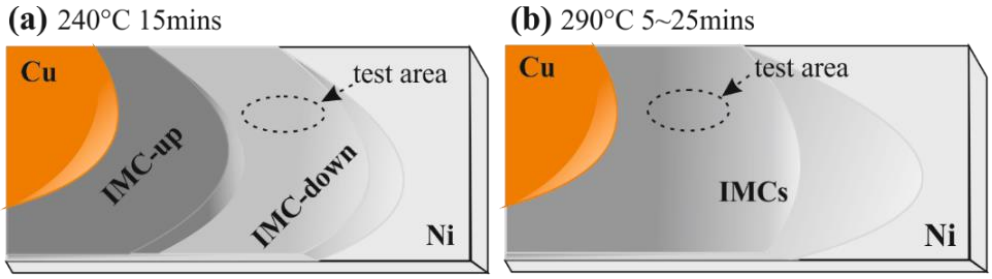

Figure 7-16 diagrams for two types of Cu-Sn-Ni IMCs interlayers under optical microscopy

Dekui Mu [94] has done some research on the mechanical properties and creep of $(Cu,Ni)_6Sn_5$ IMC under the load of 2000 μN with different temperature of 25 °C, 125 °C and 150 °C respectively. It has been pointed out that the creep displacement of $Cu_{5.5}Ni_{0.5}Sn_5$ increases with the rising of temperature, the mechanism of which is changed from the control of dislocation slipping to the diffusing between intergranular atoms. In detail, the creep displacement of $Cu_{5.5}Ni_{0.5}Sn_5$ is in the range of 4~5 nm after keeping the load for 30 s. Then, a similar measurement of creep properties has been conducted on the $(Cu,Ni)_3Sn$ IMC layer at room temperature. Figure 7-17 shows the results on the IMCs interlayer from micro-joints formed at 290 °C with 5 mins and 15 mins dwell time. In the first dwelling time of 2 s under 2000 μN loading, the creep displacement of $(Cu,Ni)_3Sn$ has increased to 3 nm immediately. After that, the increment of displacement has changed slowly. Although the fluctuation of creep displacement appears among the three tested samples for each case, all of the values are in the range of 3.5~5 nm after pressure maintaining for 30 s, which is close to the reported value on $Cu_{5.5}Ni_{0.5}Sn_5$. As the creep deformation of Cu-Sn-Ni IMCs is so small at room temperature, then which will not bring some negative influence on the measurement of young's modulus and hardness later.

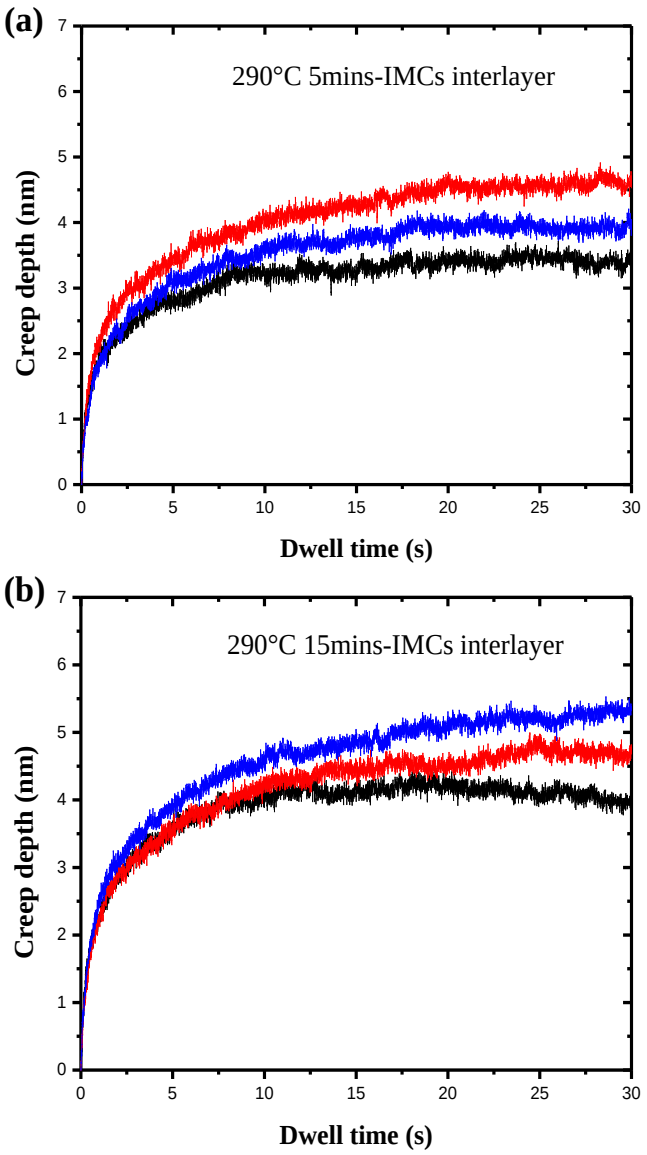

Figure 7-17 creep depth of $(Cu,Ni)_3Sn$ under constant load versus dwell time

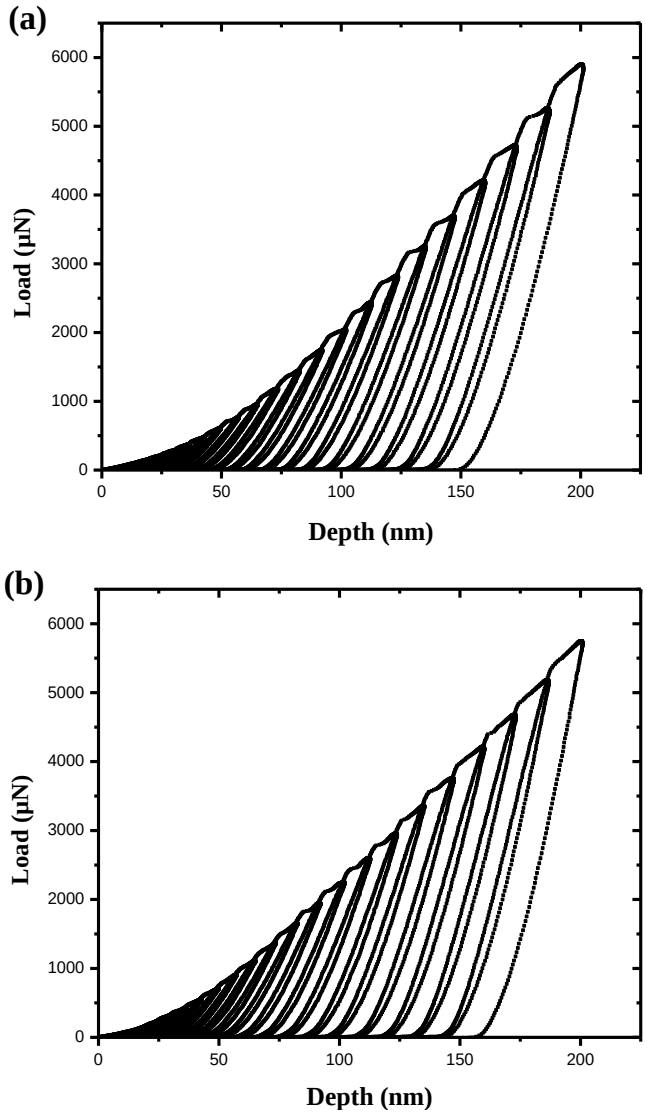

Figure 7-18 load-depth profiles of Cu-Sn-Ni IMCs during nanoindentation test

With the application of displacement-controlled multiple loading method as introduced in section 3.3, the representative load-depth curves of $(Cu,Ni)_6Sn_5$ and $(Cu,Ni)_3Sn$ from the nanoindentation tests are shown in Figure 7-18, and the relevant reduced modulus (E_r) and hardness (H) are provided in Figure 7-19. Apparently, both the results of E_r and H increase steeply at the early stage of testing, which are mainly caused by the formation of stress strengthening layer on the sample surfaces for the mechanical grinding and polishing pre-treatment. Meanwhile, the friction between indenter and sample surfaces will bring some errors to the results [91, 171], especially the area of indentation is calculated when the depth of pressing is small. Therefore, the results from those situations would not be reliable. Once the effective depth is more than 50 nm, the results of measurements trend to be stable. The reduced Young's modulus of $(Cu,Ni)_3Sn$ is slightly higher than that of $(Cu,Ni)_6Sn_5$, while the hardness value of them are almost the same.

In fact, the value of E_r and H are calculated through the formulas (7-2) and (7-3) according the tested results from nanoindentation. The F is for loading force, A is the effective area of indentation, β represents the shape factor of nanoindenter, and S is the contact stiffness. Moreover, E and v are the Young's modulus and Poisson's ratio of the tested material, where the subscript I refers to the intermetallics and *ind* is used as indenter. During the testing,

the diamond indenter has been utilized and the relevant parameters of it are E_{ind}=1140 GPa and ν_{ind}=0.07 [172]. Meanwhile, the Poisson's ratios of $(Cu,Ni)_6Sn_5$ and $(Cu,Ni)_3Sn$ are assumed to be the same with that of Cu_6Sn_5 and Cu_3Sn as 0.309 and 0.328, respectively [92, 95]. Then, the Young's modulus of IMCs can be deduced from the function (7-4).

$$H = F / A \tag{7-2}$$

$$E_r = \frac{S}{2\beta}\sqrt{\frac{\pi}{A}} \tag{7-3}$$

$$\frac{1}{E_r} = \frac{(1-\nu_I^2)}{E_I} + \frac{(1-\nu_{ind}^2)}{E_{ind}} \tag{7-4}$$

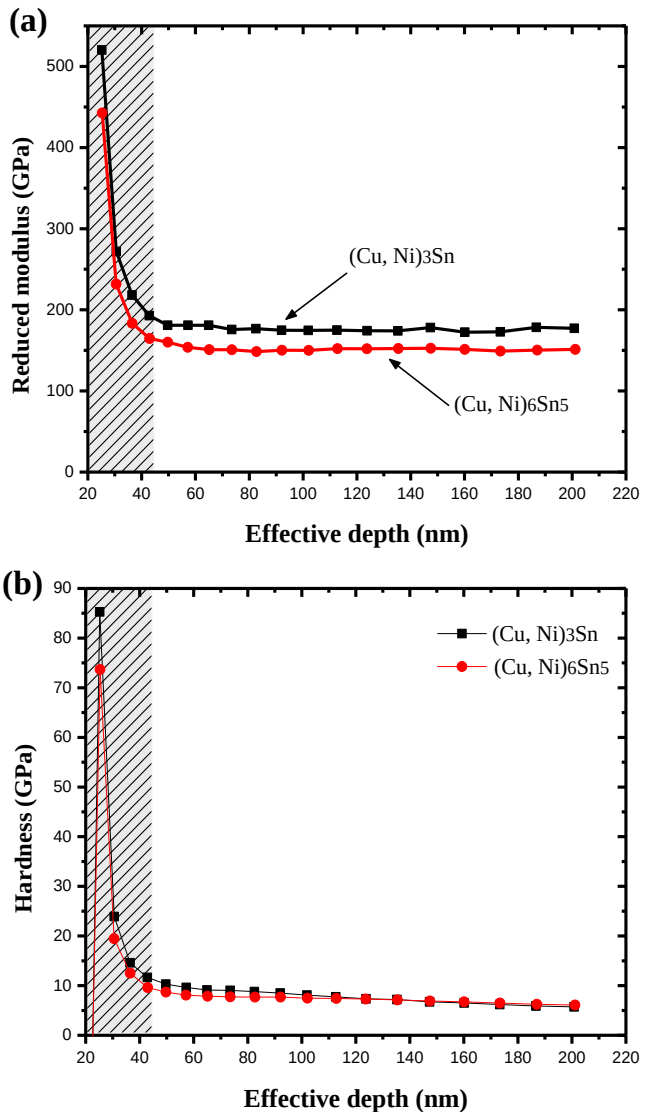

Figure 7-19 results from nanoindentation test on Cu-Sn-Ni IMCs

Through testing for several times, the average value of E and H are 160.6±3.1 GPa and 7.34±0.14 GPa for $(Cu,Ni)_6Sn_5$, while 183.7±4.0 GPa and 7.38±0.46 GPa for $(Cu,Ni)_3Sn$. Besides, the corresponding properties of

Cu and Ni substrate have also been tested with nanoindentation. The *E* and *H* of Cu-plated layer are 104.1 GPa and 3.29 GPa, and that of Ni substrate are 213.4 GPa and 3.29 GPa. Thus, if the top Cu plated layer still remained or the indenter tip penetrated into the IMC layer too deep to reach the bottom Ni substrate, both of that cases would make the measured hardness of IMCs lower than the practical value. Comparing these experimental results with the value listed in Table 2-3, the Young's modulus and hardness of $(Cu,Ni)_6Sn_5$ and $(Cu,Ni)_3Sn$ are generally higher than the value of Cu_6Sn_5 and Cu_3Sn. However, the results of $(Cu,Ni)_6Sn_5$ herein is somewhat less than that of $(Cu_{1-x}Ni_x)_6Sn_5$ like 206.8±5.5 GPa for Young's modulus and 10.07 GPa for hardness. It would be the result from different testing specimens produced through different preparation processes, then the microstructure and Ni content of Cu-Sn-Ni IMCs might be various.

7.5 In-situ mechanical testing on Cu-Sn-Ni IMCs

The novel in-situ nano-mechanical testing system with the Hysitron PI 87 SEM PicoIndenter fixed in the FIB chamber has been proceeded, which enables the uninterrupted observation of the IMC behavior during the mechanical test. It is perfect for the testing in nano-level to satisfy the requirements for high magnification and the accurate loading with the control of displacement. In this section, the in-situ nano-compression test and nano-bending test under different loading rates have been conducted on the Cu-Sn-Ni IMCs from the micro-joint formed at 290 °C with dwell time of 0 min. Besides, the nano-bending test has also been applied on the IMCs interlayer from micro-joint formed after 25 mins dwelling at 290 °C, then the fractural morphologies have been observed as followed.

7.5.1 Nano-compression test

As shown in Figure 7-20, three micro-cantilevers (Type II) have been prepared with the size about 1 μm×1 μm×3 μm for the micro-compression test. By the way, as the top Cu-plated layer was removed by FIB, Kirkendall voids can be observed clearly on the interface between IMCs and Cu-plated layer. However, no voids have been observed within the IMCs micro-cantilevers.

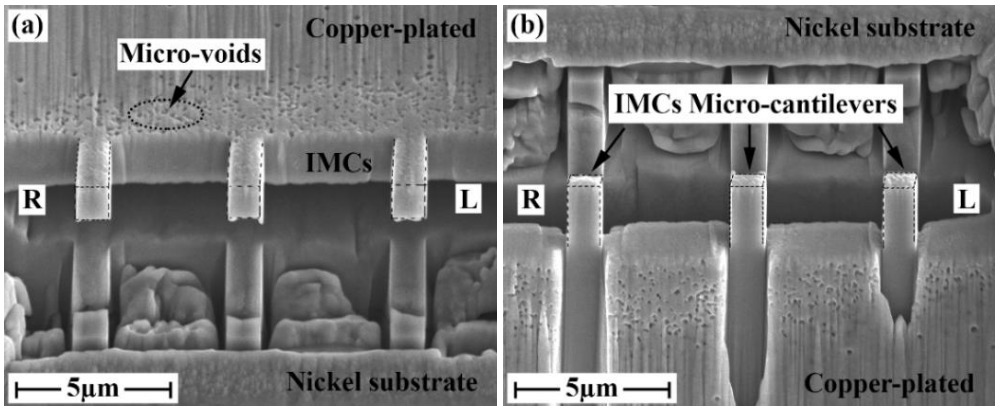

Figure 7-20 images of micro-cantilevers prepared for nano-compression (a) front view and (b) top view

Then, the nano-compression test has been implemented with an indenter of 5 μm×5 μm. This process was controlled by the consistent loading rate of 20 nm/s, and the load was stopped manually when the fracture happened. The whole testing process was recorded as a video, so that any image can be screenshot to illustrate the mechanical test. Figure 7-21 demonstrates three major stages of the testing process on these three micro-cantilevers. At the first beginning, the end face of indenter contacted the top surface of micro-cantilever. And then, along with the indenter moved down, the micro-cantilever was compressed accompany with tiny deformation. Finally, the fracture occurred and movement of indenter stopped immediately. From the record of

images, the fracture of micro-cantilever (L) happened in a similar way to that in micro-cantilever (M). And a different fracture mode was observed in the micro-cantilever (R). After analysing the stress status in rod-like sample under uniaxial-compression, it is found that there is an angel of 45° between vertical plane and the plane where a maximum shearing force existed [173]. Then, a brittle fracture morphology is observed on that plane, attributing to the shearing force. Therefore, the fracture path observed in Figure 7-21(M-3) is a normal one, and the possible reason to produce the fracture mode in other two micro-cantilever was supposed to be the unbalanced loading. Because this test belongs to the nano-level, where the result is sensitive with the factors such as the quality of manufactured surface of micro-cantilever and the local roughness of the end face of indenter. Therefore, some bending force has been introduced in the compression test of that two micro-cantilevers. Then, the fracture was prone to happen around the bottom of micro-cantilever for the concentration of stress.

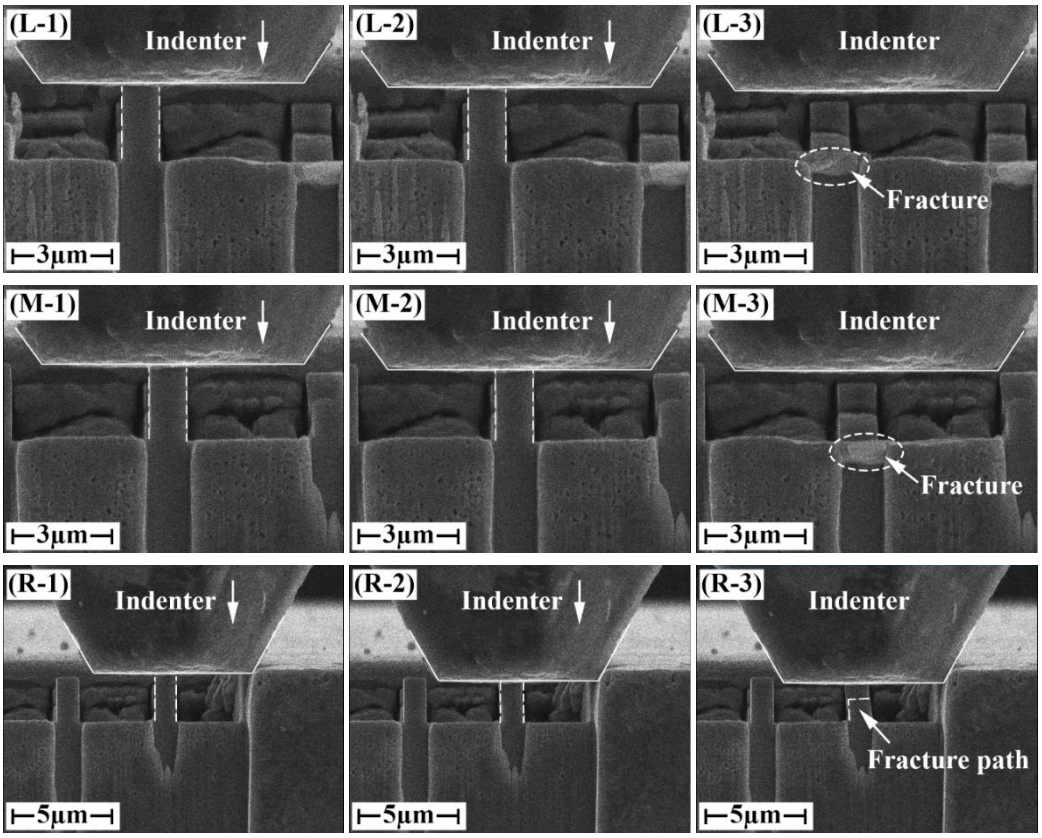

Figure 7-21 three major stages during the nano-compression test on three 290 °C/0 min IMCs micro-cantilevers (1) contact; (2) loading and deformation; (3) fracture

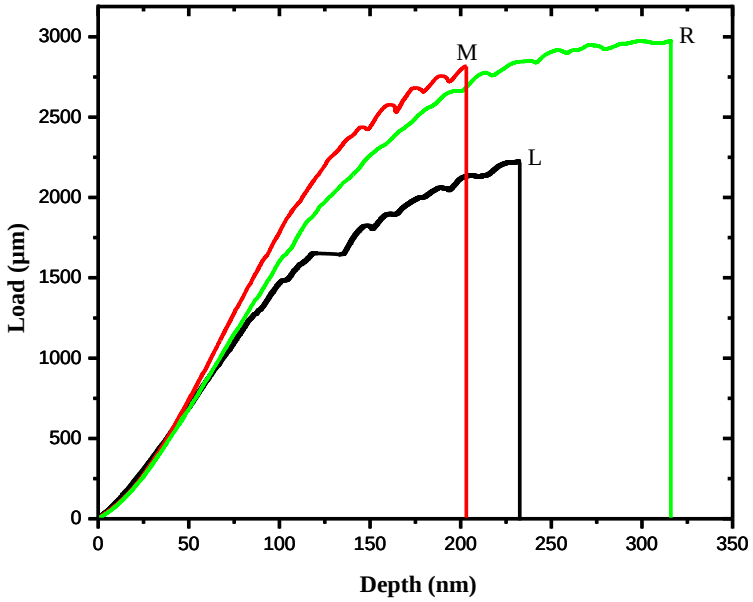

Figure 7-22 load-depth profiles of nano-compression test on three micro-cantilevers

The load-depth profiles of compression test on these three micro-cantilevers are depicted in Figure 7-22. The result shows that the effect of the bending fore included in the testing on micro-cantilevers (L and M) is not significant, but making the fracture happened earlier. Except that, the fluctuation of loading force with the increasing of depth has been observed before the complete fracture in all the situation of three micro-cantilevers. That means a slight slipping has occurred along the fracture face during this compression testing, and which should be reasonable for the two-layered structure of IMCs interlayer in these micro-joints (Figure 7-9 a). Furthermore, the stress-strain profile for the compression testing on the micro-cantilever (R) was given in Figure 7-23. Using the maximum compressive force divided by actual cross-sectional area, the fracture strength was calculated to be 2.46 GPa.

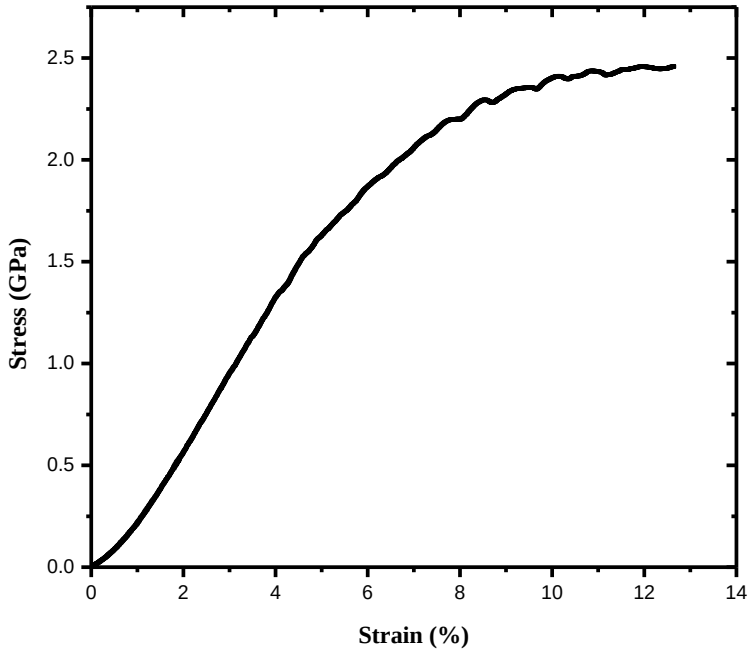

Figure 7-23 stress-strain (%) profile of nano-compression testing on micro-cantilever R

7.5.2 Nano-bending test

(1) IMCs interlayer formed at 290 °C for 0 min

Three groups of micro-cantilevers (Type III) with size of ~1μm×1μm×5μm have been fabricated by FIB for the micro-bending test as shown in Figure 7-24. And the loading process are demonstrated in Figure 7-25 for these three micro-cantilevers as 1-R, 2-L and 3-L. Different with the process of nano-compression above, the bending deformation can be observed clearly from the images recorded. During the bending, different loading rates have been used in the bending of micro-cantilever 3-L as 20 nm/s, while a slower loading rate of 10 nm/s has been applied in the other micro-cantilevers. As a result, the fractured micro-cantilever as 3-R dropped down after testing, and the uncompleted fracture seems to occur in the other two micro-cantilevers. Furthermore, the profiles of load versus depth for each micro-cantilevers are illustrated in Figure 7-26. It can be found that the different loading rate did not bring a great influence in the nano-bending test.

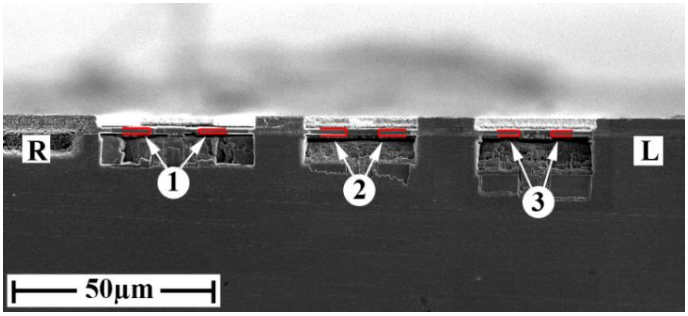

Figure 7-24 three groups of micro-cantilevers prepared in 290 °C/0 min IMCs interlayer for nano-bending test

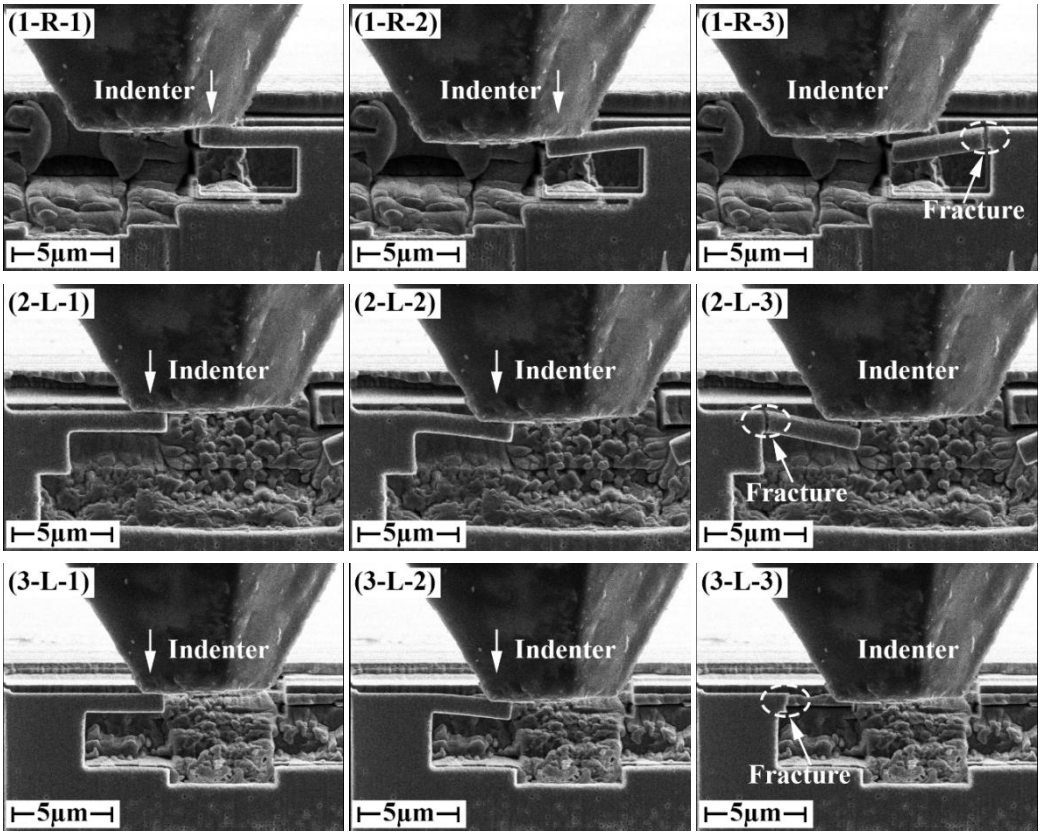

Figure 7-25 three major stages during the process of nano-bending on three 290 °C/0 min IMCs micro-cantilevers (1) contact; (2) loading and deformation; (3) fracture

Although a small amount of deformation has occurred, the Cu-Sn-Ni IMCs micro-cantilevers fractured at last on the root part for its intrinsic rigidity and brittleness. The stress state of these IMCs micro-cantilevers has been analysed through the formula (7-5), where the tip of micro-cantilever has been treated as rigid object, and the -loading force is thought as a concentrated force (F) on the certain location as shown in Figure 7-27. Once the fracture happened, the loading force reached the peak value (F_{max}), then the tensile stress in the horizontal direction (σ) on the root was to be maximum as well. Considering the relevant geometrical factors, such as the arm length (L), the width (b) and the height (h) of micro-cantilever, the ultimate tensile stress (σ_{max}) has been calculated and listed in Table 7-5. The average σ_{max} of this kind of Cu-Sn-Ni IMCs is 2.3±0.7 GPa.

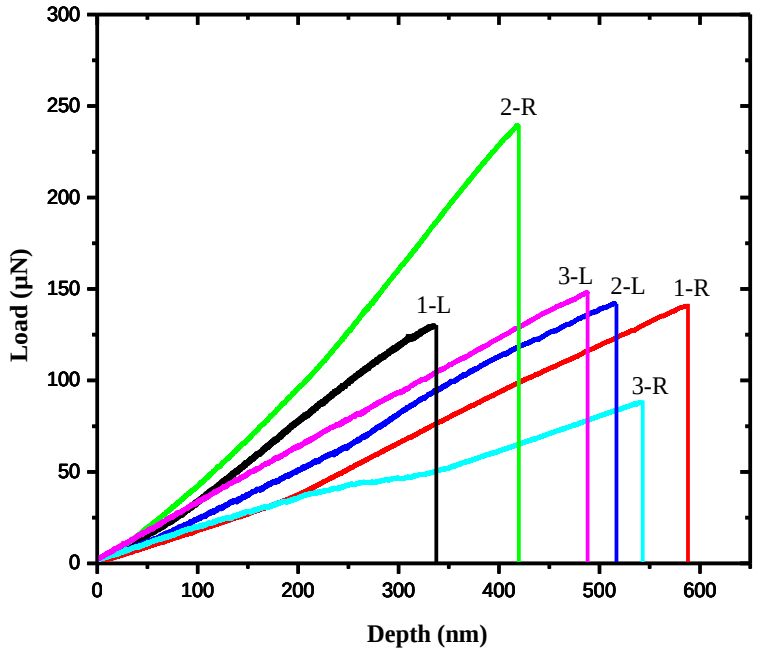

Figure 7-26 load-depth profiles of nano-bending test on all of 290 °C/0 min IMCs micro-cantilevers

$$\sigma_{\max} = \frac{6 \times F_{\max} \times L}{b \times h^2} \tag{7-5}$$

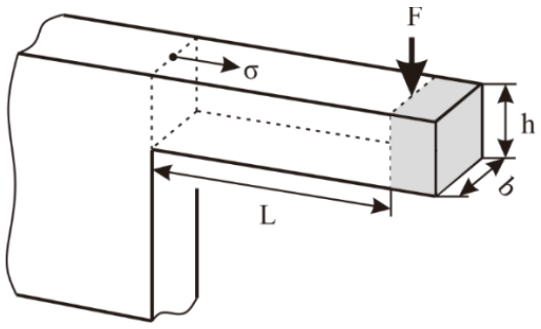

Figure 7-27 parameters for the in-situ bending test on IMCs micro-cantilevers

Table 7-5 parameters of IMCs (0 min) micro-cantilevers and the calculated results of σ_{max}

Parameters	1-R	1-L	2-R	2-L	3-R	3-L
***L* (μm)**	3.32	3.41	3.41	3.32	3.41	3.74
***h* (μm)**	1.07	1.18	1.22	1.05	1.02	1.23
***b* (μm)**	1.22	0.67	1.21	1.12	1.01	1.12
F_{max} **(μN)**	142.32	140.85	129.79	148.20	87.99	239.79
σ_{max} **(GPa)**	2.0	3.1	1.5	2.4	1.7	3.2
$\overline{\sigma_{max}}$ **(GPa)**	2.3±0.7					

(2) IMCs interlayer formed at 290 °C for 25 mins

More nano-bending tests have been conducted on the samples which were soldered with dwelling at 290 °C for 25 mins. After cleaning by FIB on the cross-section, the Kirkendall voids with bigger size were observed clearly on the interface between IMCs and Cu-plated layer in these samples than those soldered with shorter dwell time. And two micro-cantilevers have been made within the Cu-Sn-Ni IMCs interlayer with size around 1 μm×1 μm×5 μm, as shown in Figure 7-28. The bending process for each micro-cantilever is depicted in Figure 7-29, where the loading rate was 20 nm/s.

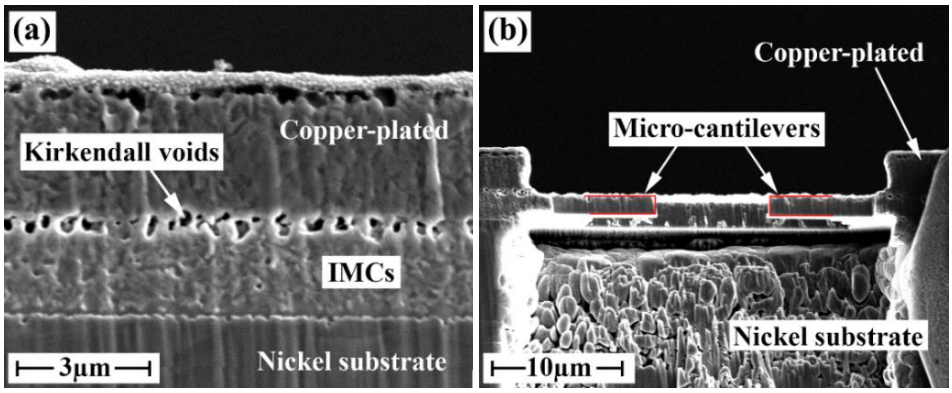

Figure 7-28 IMCs micro-joint formed after 25 mins dwelling and the IMCs micro-cantilevers (a) cross-section morphology; (b) the front view of micro-cantilevers

Afterwards, the fractural morphologies of both micro-cantilevers after testing have been analysed with high magnification SEM, as shown in Figure 7-30. A typical brittle fracture occurred in the two samples after bending. In Figure 7-30(a), a plane of crystal was observed surrounding by other chipped grains, meanwhile the opposite plane also existed in Figure 7-30(b), as circled by white dash line. And, a convex grain was easy to recognize in Figure 7-30(c). It is supposed to be the Ni-rich $(Cu,Ni)_6Sn_5$ grain as observed in this type of micro-joint in Figure 7-9(d). Therefore, both the fracture modes as transgranular and inter-granular fracture are inferred to occur in the Cu-Sn-Ni IMCs. In addition, the load-depth profiles from the testing are shown in Figure 7-31. It seems that loose load appeared in the beginning stage of bending test on the micro-cantilever (L), which might be caused by the uneven surfaces. However, the following test have went smooth. The loading forces of both these micro-cantilevers have increased with the downward displacement of indenter, until the fracture of IMCs occurs. Then, the average of ultimate tensile stress (σ_{max}) for the two micro-cantilevers were calculated about 2.45 GPa, the details are shown in Table 7-6. This result is quite close to that of the samples without dwelling. Obviously, although the microstructure of Cu-Sn-Ni IMCs interlayer changed with the dwell time in the micro-joints

soldered at 290 °C, it did not affect the mechanical property of the IMCs interlayer too much.

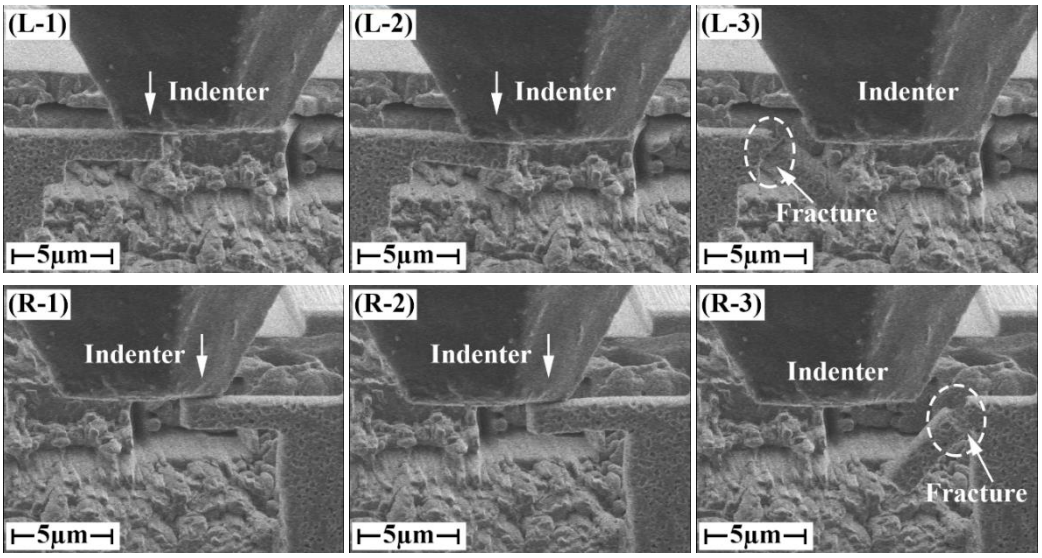

Figure 7-29 three major stages during the process of nano-bending on two 290 °C/25 mins IMCs micro-cantilevers (1) contact; (2) loading and deformation; (3) fracture

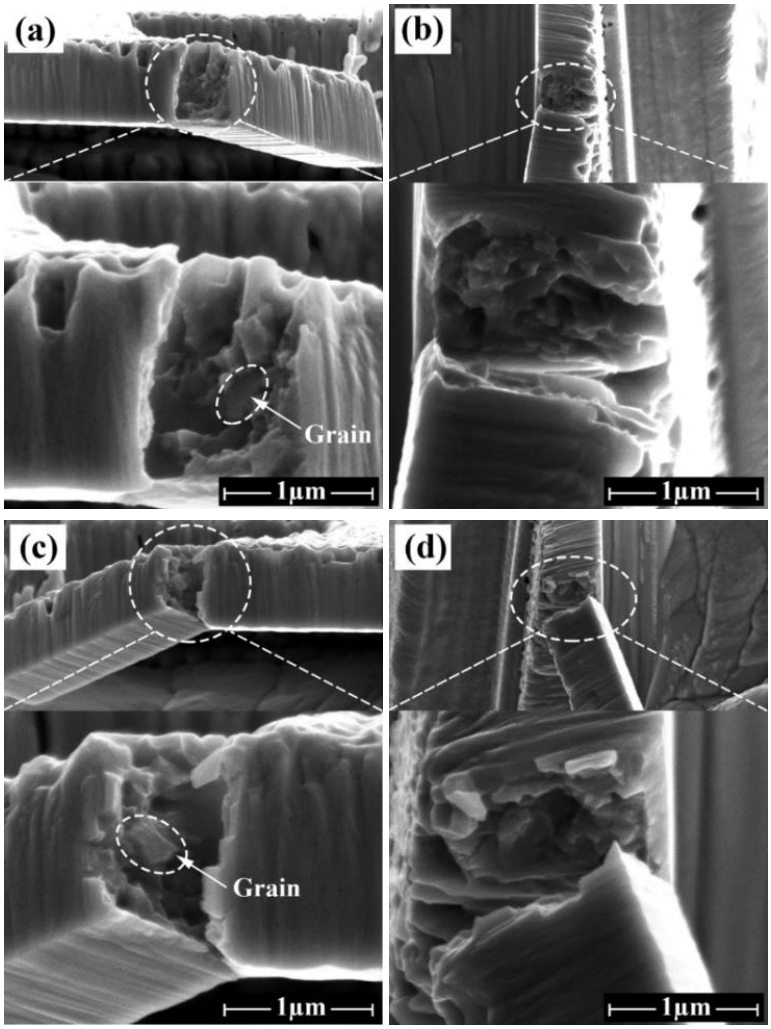

Figure 7-30 fracture morphologies of 290 °C/25 mins IMCs micro-cantilevers after bending test (a, b) for micro-cantilever L; (c, d) for micro-cantilever R

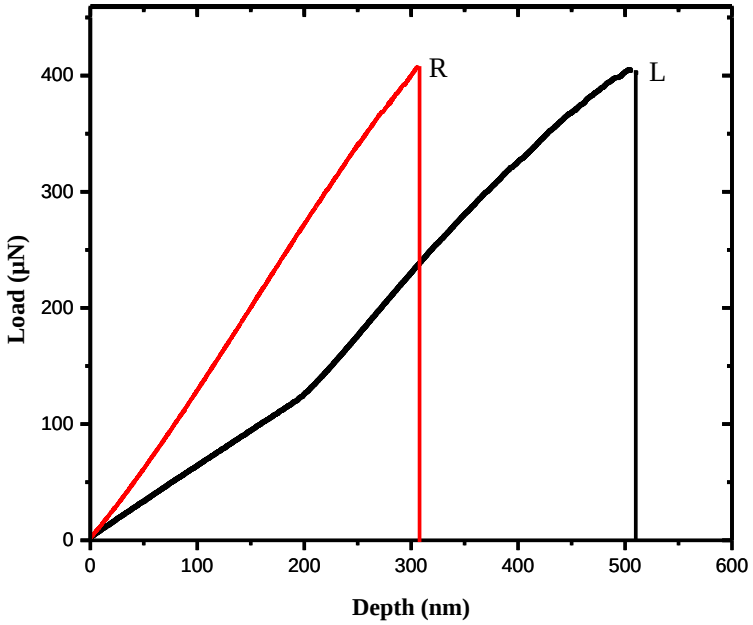

Figure 7-31 load-depth profiles of 290 °C/25 mins IMC micro-cantilevers during in-situ bending test

Table 7-6 parameters of IMCs (25 mins) micro-cantilevers and the calculated results of σ_{max}

IMCs micro-cantilever		L(μm)	h(μm)	b(μm)	F_{max}(μN)	σ_{max}(GPa)
290 °C-25 mins	R	3.01	1.62	1.63	407.98	1.7
	L	3.55	1.32	1.55	402.35	3.2

7.6 Summary

Full Cu-Sn-Ni IMCs interconnection has been fabricated with the Ni/Sn (2.5 μm)/Cu initial structure after soldering in T-track reflow oven. Then the microstructure of these micro-joints has been observed and analysed through the FEG-SEM, XRD and TEM. Based on that, the formation process and the microstructural evolution mechanism have further discussed. Afterwards, the mechanical properties of two major Cu-Sn-Ni IMCs have been measured by nanoindentation, and the in-situ nano-compression and nano-bending tests have conducted on the Cu-Sn-Ni IMCs micro-cantilevers, which are from the micro-joints formed at 290 °C. The relevant results can be summarized as below:

(1) The diffusion of Cu in Sn layer was observed to be much faster than that of Ni in Sn layer, thus the simultaneous solidification occurred for the predominant Cu-Sn reaction in this experiment. Then, the IMCs micro-joints have almost formed at 230 °C. When the soldering temperature was increased to 240 °C, the IMCs interlayer of these micro-joints turns out to be constituted with three sub-layers in chemical composition, such as the Cu-rich $(Cu,Ni)_3Sn$ on Cu-plated layer, the Sn-rich area in the middle and the Ni-rich layer on Ni substrate. The total thickness of IMCs interlayer increases with the dwell time from 0~25 mins. In particular, the growth factor of $(Cu,Ni)_3Sn$ layer near Cu-plated layer is 0.36, which is less than that of Cu_3Sn growing in Cu-plated/IMCs/Cu structure.

(2) With the rise of soldering temperature, the Cu and Ni content of IMCs interlayer have increased, the Sn-rich layer in the micro-joint formed at 260 °C for 25 mins contains the atomic ratio of Cu to Sn as 6:5, then this micro-

joints is exactly the IMCs micro-joints by now. Besides, the process of phase transformation from $(Cu,Ni)_6Sn_5$ into $(Cu,Ni)_3Sn$ has also been promoted by the elevated temperature. The interfaces between each sub-IMCs layers in micro-joints formed at 290 °C have become fuzzy with the prolonged dwell time. Until the dwelling time up to 25 mins, the majority of IMCs interlayer has evolved to be $(Cu,Ni)_3Sn$, except some Ni-rich $(Cu,Ni)_6Sn_5$ still remained around the center-line and close to Ni substrate.

(3) An obvious inter-action exists in the Ni substrate/IMCs/Cu structure. The Ni_3Sn_4 has been detected in the micro-joints formed at 240 °C with 15 mins dwelling by XRD, however, which did not appear in the other micro-joints soldered at higher temperature. It is supposed to be the primary Ni_3Sn_4 layer formed on Ni substrate has transformed into $(Cu,Ni)_6Sn_5$ for the addition of Cu atoms later. Or the content of Cu diffusing to Ni substrate was high enough at the very soldering beginning to make the Cu-Sn reaction predominant, then the $(Cu,Ni)_6Sn_5$ produced directly.

(4) At room temperature, the creep amount of Cu-Sn-Ni IMCs is in the range of 3.5~5 nm under the load of 2000 μN for 30 s. The Young's modulus and hardness were measured by nanoindentation to be 160.6±3.1 GPa/7.34±0.14 GPa for $(Cu,Ni)_6Sn_5$, and 183.7±4.0 GPa/7.38±0.46 GPa for $(Cu,Ni)_3Sn$ respectively. Moreover, in-situ mechanical tests have been conducted on Cu-Sn-Ni IMCs micro-cantilevers in micro-joints formed at 290 °C with 0 min dwelling. The compression fractural stress is about 2.46 GPa, and the ultimate tensile stress is 2.3±0.7 GPa from nano-bending test, where the different loading ratios has not brought a significant influence on the fractural behavior of Cu-Sn-Ni IMCs. Besides, the Ni-$(Cu,Ni)_6Sn_5$ grain and the cleavage plane were observed on the fractural cross-sections of Cu-Sn-Ni IMCs micro-cantilevers in the micro-joint formed after soldering at 290 °C with the dwell time of 25 mins, which indicates that the intergranular and transgranular fracture happened.

Chapter 8 Conclusions and Future Work

8.1 Main conclusions

The works from this thesis have been concerned with the soldering interconnection for the miniaturized electronic packaging. Two types of IMCs micro-joints have been prepared from the initial Cu/Sn/Cu and Ni/Sn/Cu sandwich structures soldering through TLP process, where a thin layer of Sn was electroplated as the solder material with the thickness of 1~5 μm. Then, mechanisms of formation and microstructural evolution of Cu_3Sn IMC micro-joint and Cu-Sn-Ni IMCs micro-joint have been analysed thoroughly. Besides, further efforts have been made to establish the relationship between reliability and microstructure of the IMCs micro-joints basing on the results from micro-mechanical tests by nanoindentation and in-situ nano-mechanical test system. The primary findings and new knowledge on the scientific and technological aspects can be concluded as the follows, which not only provide an insight into the characteristics of these full IMCs interconnections, but also give some useful guidance to industry for the application of 3D IC stacking packaging.

8.1.1 Planar growth of IMCs in micro-interconnect

(1) The Planar growth behaviour of IMCs exists in the micro-structure of Cu/Sn/Cu in the soldering process, which is similar to that growing along the direction perpendicular to Cu/Sn interface. Two-layered IMCs structure appears in the planar direction as the tiny Cu_3Sn grains underneath the cobblestone-like Cu_6Sn_5 grains. In particular, some Cu-rich whiskers with the length up to 4 μm has formed on the cross-section of Cu/Sn (2.5 μm)/Cu structure after soldering, which is the mixture of Cu, Cu_2O, SnO_x and Cu_6Sn_5.

(2) The reasons that interconnecting material has migrated from inside to outside in soldered Cu/Sn/Cu micropillar are due to: First, the growth of IMCs in planar direction was unconstrained for the existence of free surfaces, which was also accompanied by the volume expansion for the IMCs phase transformation; and the other is the internal stress of interconnecting layer increased for plenty of Cu atoms diffusing in with the drive of chemical concentration gradient.

(3) The IMCs on the cross-section of soldered Ni/Sn (2.5 μm)/Cu structure is mainly $(Cu,Ni)_6Sn_5$ as a single layer. Whist the planar growth of IMCs in the soldered Ni/Sn (5 μm)/Cu structure turns out to be asymmetric. It is attributed to the different diffusion rates of Cu and Ni atoms in Sn layer, then the IMCs planar growth is much faster on Cu/Sn interface than that on Ni/Sn interface.

8.1.2 Microstructure and reliability of Cu-Sn IMCs micro-joint

(1) When the interconnecting height (the thickness of Sn layer) is less than 3 μm, the interlayer of Cu/Sn/Cu structure will solidify simultaneously, thus forming the microstructure of isometric crystals. Because the growth of scalloped Cu_6Sn_5 grains has been supressed, the relatively compact Cu_6Sn_5 IMC micro-joints can be made from the Cu-plated/Sn (2.5 μm)/Cu structure after soldering at 240 °C with the dwell time of 0 min. In the dwelling stage, the phase transformation from Cu_6Sn_5 into Cu_3Sn is the major reaction in these Cu-Sn IMCs micro-joints, and the types of substrates and the soldering temperature have some significant influence on that process. The high soldering temperature is benefit to the transformation, meanwhile the growth of Cu_3Sn on Cu-plated layer is much quicker than that on the Cu-rolled substrate. After soldering at 290 °C for 15 mins, the Cu_3Sn has become the only intermedium in the Cu-plated/IMC/Cu micro-joints.

(2) The analysis on Cu_3Sn growth behavior in kinetics shows that: with the soldering temperature from 240 °C rising up to 290 °C, the growth factor (n) of Cu_3Sn in Cu-plated/IMCs/Cu structure drops from 0.48 to 0.34, but

that in Cu-rolled/IMCs/Cu structure increases from 0.29 to 0.36. Under the low soldering temperature, the growth of Cu_3Sn in these IMCs micro-joints is controlled by the diffusion rate of Cu atoms from substrate into the interlayer predominantly. Moreover, since the thickness of Cu_3Sn layer is prone to form in micro-joints under the relatively high temperature, the diffusing distances of Cu and Sn atoms have been extended, thus the growth of Cu_3Sn on Cu-plated layer has slowed down, while that on Cu-rolled substrate has not been affected obviously.

(3) Kirkendall voids have been found only in the Cu_3Sn layer close to the Cu-plated layer. One of the reason is that much more Cu atoms have been escaped from Cu-plated layer than Cu-rolled substrate, and then diffused into interlayer with the driving force of concentration gradient. The other reason is the Cu-Cu_6Sn_5 diffusion couple in these IMCs micro-joints is on the semi-closed status. The limited Sn atoms cannot fill up the vacancies created by the leaving of massive Cu atoms. And also, the diffusion of Cu in Cu_3Sn layer is much faster than that of Sn, hence the amount of Kirkendall voids has increased with the thickened Cu_3Sn layer.

(4) The hybrid-type microstructure has formed in the Cu-Sn IMCs micro-joints along with the consumption of layered Cu_6Sn_5 in the middle, like the coarse Cu_3Sn grains surrounding by lots of tinny Cu_6Sn_5 grains. Furthermore, the homogenization process of these Cu_3Sn IMCs micro-joints has conducted at 260 °C with the prolonged dwell time, which can be described by the Flux-driven ripening (FDR) theory based on Gusak's work. That means the growth and ripening of Cu_3Sn grains have occurred simultaneously under the control of Cu diffusion. After a long dwell time of 70 mins at 260 °C, the columnar-like Cu_3Sn grains have formed along the direction vertical to IMC/Cu interface, however, having none obvious preferential growth orientations. Although this kind of micro-joints is constituted with the porous Cu_3Sn interlayer for Kirkendall effect, the shear strength of which has been tested by nanoindentation to be about 176 MPa. Both intergranular and transgranular fractures have occurred, and also the interlocking effect among the multi-prismatic Cu_3Sn grains have made the micro-joint mechanically robust.

8.1.3 Microstructure and reliability of Cu-Sn-Ni IMCs micro-joint

(1) The Cu-Sn-Ni IMCs interlayer in micro-joints from Ni/Sn (1.5 μm)/Cu structure soldered through TLP process is made up with three different layers in composition, such as the Cu-rich $(Cu,Ni)_3Sn$ on Cu-plated side, the Sn-rich $(Cu,Ni)_6Sn_5$ in the middle and the Ni-rich area on the Ni substrate. In the addition of Ni atoms, the growth factor of $(Cu,Ni)_3Sn$ on the Cu-plated layer is 0.36 which is lower than that of Cu_3Sn in Cu-plated/Sn/Cu structure. Particularly, the Kirkendall voids have concentrated on the Cu-plated layer/IMCs interlayer, but not in the adjacent $(Cu,Ni)_3Sn$ layer. Moreover, the Ni-rich area is thought to be Ni_3Sn_4 as the main product of Ni-Sn reaction in micro-joint after soldering at 240 °C for 15 mins. Because of much more Cu atoms arriving at the Ni substrate shortly at higher soldering temperature, the Cu-Sn reaction has become predominant on this Ni/Sn interface and thus the product has changed to be Ni-rich $(Cu,Ni)_6Sn_5$ correspondingly.

(2) When the dwell time is longer than 5 mins, the IMCs interlayer of micro-joints soldered at 290 °C is composed of $(Cu,Ni)_3Sn$ IMC mostly, and some Ni-rich $(Cu,Ni)_6Sn_5$ grains still remain around the center-line of interlayer and Ni substrate. It can be explained as: some Ni atoms dissolving in Cu_3Sn on Cu-played layer have migrated out by the crash force producing from the diffusing Cu atoms, then aggregated in the $(Cu,Ni)_6Sn_5$ grains around the center-line; meanwhile, the redundant Ni atoms also have been excluded from the initial $(Cu,Ni)_6Sn_5$ grains for the phase transformation into $(Cu,Ni)_3Sn$. Therefore, these Ni-rich $(Cu,Ni)_6Sn_5$ grains have become much stable in thermodynamics, and survived within the $(Cu,Ni)_3Sn$ layer. In the micro-joint after dwelling 25 mins at 290 °C, the Ni content of $(Cu,Ni)_3Sn$ close to Cu-plated layer is only 0.5~3 at.%, while that in the residual Ni-rich $(Cu,Ni)_6Sn_5$ grains can up to 20.9 at.%.

(3) The creep deformation of $(Cu,Ni)_6Sn_5$ and $(Cu,Ni)_3Sn$ IMCs is in the range of 3.5~5 nm, which has been measured by nanoindentation under the condition of 2000 μN loading for 30 s. The Young's modulus of these Cu-Sn-Ni IMCs are 160.6±3.1 GPa for $(Cu,Ni)_6Sn_5$, 183.7±4.0 GPa for $(Cu,Ni)_3Sn$, and the corresponding hardness of them are 7.34±0.14 GPa and 7.38±0.46 GPa respectively. Because of the addition of Ni atoms, the Young's modulus and hardness of Cu-Sn-Ni IMCs are all higher than that of Cu-Sn IMCs, called as the solid-solution strengthening. Moreover, the compression fracture strength of Cu-Sn-Ni IMCs micro-cantilevers in the micro-joint formed at 290 °C is about 2.46 GPa, and their ultimate tensile stress from nano-bending test is 2.3±0.7 GPa which did not be affected significantly by the different loading rates (10 nm/s and 20 nm/s). Both transgranular and inter-granular fracture modes occurred in the Cu-Sn-Ni IMCs of micro-joint soldered at 290 °C for 25 mins, the average of ultimate tensile stress is 2.45 GPa. Therefore, it can be concluded that the fracture behaviour of Cu-Sn-Ni IMCs interlayer doesn't have an obvious relationship with the change of microstructure in these micro-joints soldered at 290 °C with different dwell time.

8.2 Recommendations for future work

There are still many difficulties existing in the way of the miniaturized interconnection. As the size of interconnection becomes smaller, especially reaches to the level of micrometre or even be nanometre levels, it has brought many tremendous challenges in terms of preparation of robust IMCs interconnects, materials characterizations and reliability evaluation of micro-joints in terms of their electrical and mechanical performance. The research work in this area also heavily depends on the research facilities and equipment. Therefore, some issues are still remained and have not been fully investigated yet.

(1) Optimise the procedures to get compact full IMCs micro-joints without voids. Thermocompression is a good alternative soldering method to exclude the voids from micro-joints. The connecting height of these joints investigated in this study is less than 5 μm, the quality of interconnection is thus very sensitive to the surface roughness of substrate. In order to eliminate the effect of surface conditions, a standard photolithography and high resolution image developing technique is suggested to apply and fabricate the samples on polished silicon substrate. Meanwhile, the samples with smaller size will increase the difficulty of subsequent operations, and also some special equipment will be needed to conduct the electrical and mechanical tests.

(2) The electrical property of microjoints is a critical factor to qualify the performance of interconnection. Theoretically, Kirkendall voids are very likely to appear in the interconnection during the service period, and these voids significantly impact the conductivity and reliability of joints. Hence, an accurate electrical module may be designed and fabricated to monitor the real-time change of conductivity under the experimental condition. Then, the electrical stability of these micro-joints composing with the homogenous Cu_3Sn or Cu-Sn-Ni IMCs can be confirmed, which is benefit to evaluate their resistance to the electromigration and thermomigration. Moreover, the effect of voids distribution in micro-joints on the mechanical interconnection strength also needs a further discussed.

(3) Stresses induced by the mismatch of coefficient of thermal expansion (CTE) between different materials and phases can exist commonly in the multi-functional and highly heterogeneous integrated packages. Thus, the full IMCs will experience some mechanical load in the application under the different thermal conditions. Unfortunately, IMCs are always considered to be naturally brittle, which is potentially detrimental to the reliability of the interconnection. However, some new different characterizations have been exploded within the small-size material in recent decades, such as super-plasticity or super-strength. In such case, it can also be expected that some advantages of IMCs would be found in the micro-scale. Up to date, there are still some areas

that have been identified to require a feasible and reliable measuring method, and further attempt is necessary and worth of making efforts to reveal the different properties of IMCs at the micro- or nano-level.

(4) Ni/Sn/Cu sandwich structure was presented in this project as an alternative solution to realize the full IMCs interconnection. The $(Cu,Ni)_3Sn$ can act as the primary part of interlayer in these micro-joints, however, it has rarely been investigated in much details before. An analysis using TEM will be much helpful to better understand the status of Ni atoms dissolved in Cu_3Sn. Besides, the other properties of the $(Cu,Ni)_3Sn$ IMC are also still unknown, which requires advanced metrology to conduct further measurements.

(5) In this work, in-situ nano-compression and nano-bending tests have been performed to measure and calculate the fractural strength of IMCs, which provides the possibility of direct observation of the deformation behaviour of micro-cantilevers prepared by FIB. Although it has a high resolution, further comparing testing with any advanced instruments can be useful to confirm the obtained results, possibly through a new approach.

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