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TRANSISTORISED INDUCTION HEATING POWER
SUPPLIES USING MOSFETS

by

DAVID WALTER TEBB

A DOCTORAL THESIS

Submitted in partial fulfilment of the requirements for the award of
Ph.D. of Loughborough University of Technology 1986.

Supervisor: Dr L. Hobson

Department of Electronic and Electrical Engineering

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SUMMARY

A prototype has been designed and constructed that has fed 3kW into a commercial workcoil at 150 kHz. Another lower power inverter has been built. This was developed with ease of production in mind to aid the transfer of technology to the sponsoring company. The company have adopted this unit and are manufacturing it.

The thesis reviews induction heating power supplies with emphasis on those able to operate above 100 kHz. Members of the MOSFET family are described and critically assessed for the application.

Prototypes of various configurations have been constructed and experience of these has led to the choice of current fed topology as the best for the application.

The design and layout of a three phase current fed full bridge inverter that can feed 5 kW into an industrially relevant coil at 400 kHz and a single phase 2.5 kW version are described. Results of tests carried out on the units are presented.

A microprocessor system has been selected which has been used for closed loop control of power, temperature and housekeeping tasks such as the supervision of interlocks.

Detailed analysis of the current fed topology has been undertaken for design and especially for the suppression of ringing. This has been greatly enhanced by the use of a circuit analysis package called SPICE.

Theory that enables manufacturers' data sheets to be used to derive the values required by the MOSFET models available on SPICE has been put to use. SPICE can model the steady state operation of the inverter but also enables the stresses on MOSFETs during fault conditions and mainsborne transients to be investigated.

ACKNOWLEDGEMENTS

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LIST OF SYMBOLS

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>UNIT</u>
b_n	The coefficient of the nth harmonic term of a Fourier series representing the load current.	A
C'	The capacitor in the filter Z_f	F
C_{BC}	The blocking capacitor in the voltage fed inverter.	F
C_{DS}	The drain source capacitance of a MOSFET.	F
C_{eq}	The equivalent capacitance of the branch in the modified tank circuit containing C_T and L'' .	F
C_f	A filter capacitor connected across the supply of a cycloinverter.	F
C_{GD}	The gate drain capacitance of a MOSFET.	F
C_{GS}	The gate source capacitance of a MOSFET.	F
C_{IP}	The input capacitance of a MOSFET.	F
C_{RFBC}	The radio frequency bypass capacitor in the voltage fed inverter.	F
C_S	The speed-up capacitor.	F
C_T	The tank circuit capacitor.	F
D	The drain terminal.	
f_{res}	The resonant frequency of L_{eff} and the effective drain source capacitance.	Hz
f_{rl}	The lowest parallel resonant frequency of the modified tank circuit	Hz
f_s	The switching frequency of the inversion bridge.	Hz
G	The gate terminal.	
I_{CM}^*	The part of the circulating current that is carried by MOSFETs.	A
I_D	The current in the dc link.	A
I_L	The load current.	A

* Capital I and V represent rms values and small i and v represent instantaneous values.

\hat{I}_M	The maximum part of the circulating current carried by an individual MOSFET.	A
I_{\min}	The minimum value of the dc link current as the frequency of the inversion bridge is varied.	A
L'	An inductor in the filter Z_F .	H
L''	An inductor in the filter Z_F and the modified tank circuit.	H
L_C	The choke in the dc link.	H
L_{eff}	The effective inductance of the filter Z_F above the resonant frequency of L' and C' and also the effective inductance of the modified tank circuit above the resonant frequency of L'' and C_T .	H
L_F	A filter inductor connected in the supply to a cycloinverter.	H
L_S	The inductance of connections between the output terminals of a current fed inverter and the tank circuit.	H
L_T	The tank circuit inductor.	H
n	The harmonic.	
P_C	The conduction losses in a MOSFET.	W
P_D	Power Dissipation.	W
P_{DD}	The losses in the parasitic diode in a MOSFET.	W
P_G	The losses in the internal gate connection of a MOSFET.	W
P_S	The switching losses in a MOSFET.	W
q_g	The charge on the input capacitance of a MOSFET.	C
Q	The Quality factor of a component.	
Q''	The Quality factor of inductor L'' .	
Q_L	The Quality factor of the loaded workcoil.	
Q_u	The Quality factor of the unloaded workcoil.	

R''	The equivalent series resistance of the inductor L'' .	Ω
R_D	The burden resistance connected across the secondary of the current transformer.	Ω
R_{C-S}	The thermal resistance between the case of a MOSFET and a heatsink.	$^{\circ}\text{C}/\text{W}$
R_{DR}	The external resistance in the gate drive circuit of a MOSFET.	Ω
R_{DS}	The drain to source resistance of a MOSFET.	Ω
$R_{DS(ON)}$	The drain to source resistance of a MOSFET when it is in the Ohmic region.	Ω
R_G	The internal resistance of the gate terminal of a MOSFET.	Ω
R_H	The thermal resistance of a heatsink and the heatsink to ambient.	$^{\circ}\text{C}/\text{W}$
R_{J-C}	The thermal resistance between the junction and the case of a MOSFET.	$^{\circ}\text{C}/\text{W}$
R_L	A load resistor.	Ω
R_W	The equivalent series resistance of the workcoil.	Ω
R_W'	A resistor connected in series with the workcoil to represent the lossiness of inductor L'' .	Ω
S	The source terminal.	
t	Time.	s
T	The time period of a periodic waveform	s
t_{DB}	The period in the MOSFET switching sequence in a current fed inverter when all the MOSFETs are on.	s
$t_{D(off)}$	The turn-off delay time of a MOSFET.	s
$t_{D(on)}$	The turn-on delay time of a MOSFET.	s
t_r	The rise time in current.	s
t_{rr}	The reverse recovery time.	s
T_A	Ambient temperature.	$^{\circ}\text{C}$

T_C	The case temperature of a MOSFET.	$^{\circ}C$
T_J	The junction temperature of a MOSFET.	$^{\circ}C$
V_1	The voltage sustained across L_{eff} caused by passing the load current through the modified tank circuit.	V
V_a to V_f	The control voltages in the cycloinverter.	V
V_B	The phase voltage of the blue phase.	V
V_D	The voltage in the dc link.	V
V_{GSD}	The gate source drive voltage of the MOSFET.	V
V_{LT}	The voltage across the tank circuit inductor.	V
V_R	The phase voltage of the red phase.	V
V_T	The threshold voltage of the MOSFET.	V
V_Y	The phase voltage of the yellow phase.	V
Y_{MOD}	The admittance of the modified tank circuit.	Ω
Z_F	The impedance of the filter containing L', L'' and C' .	Ω
Z_D	The impedance of a parallel tank circuit at resonance.	Ω

GREEK SYMBOLS

α	The delay angle after phase crossover in the firing of thyristors in the rectification bridge.	degrees
η_{MTC}	The efficiency of the modified tank circuit.	
η_{WC}	The efficiency of the workcoil.	
ω_1	The radiancy of parallel resonance of filter Z_F .	radians s^{-1}
ω_2	The radiancy of series resonance of filter Z_F .	radians s^{-1}
ω_s	The switching radiancy ($=2\pi f_s$).	radians s^{-1}
ω_{res}	The radiancy at which L_{eff} and the effective drain source capacitance resonate.	radians s^{-1}

CHAPTER 1
INTRODUCTION

An introduction to the types of power supply already used for induction heating applications is presented. The reasons for undertaking this work are given.

INTRODUCTION

The two most important parameters of induction heating power supplies are their frequency and power output.

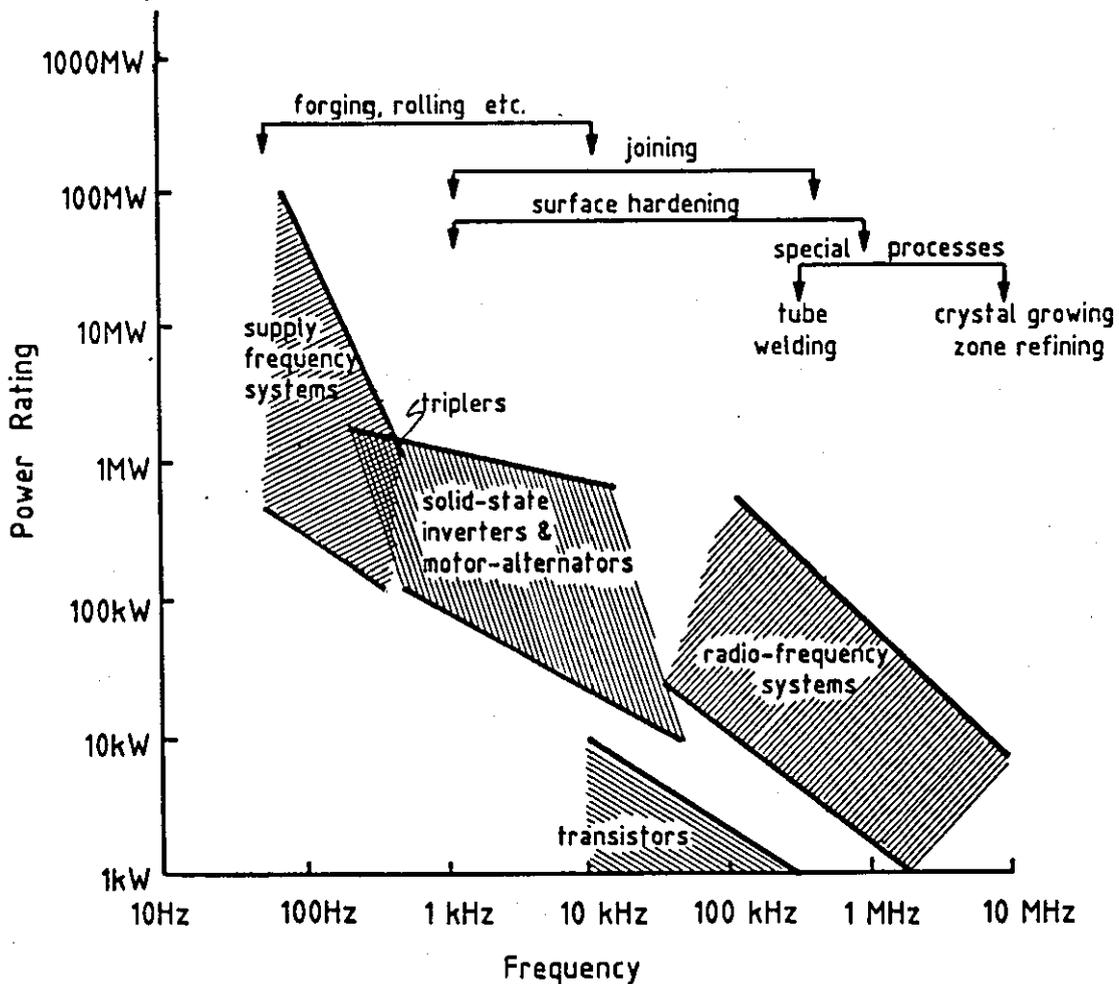


Figure 1.1* - Induction heating supplies and applications and the frequencies and power levels associated with them.

* Figures are referred to by a chapter number followed by the order in which they appear in the chapter.

As can be seen in Fig. 1.1 operating frequencies and power ratings associated with induction heating techniques vary so widely that many different type of power source have been used (Davies et al 1979)*. Mains frequency systems are used for metal melting, heating metal billets prior to forging, rolling or extrusion at powers up to 100 MW. Magnetic frequency multipliers extended the frequency range to 150 Hz by extracting the third harmonic generated when the outputs of three single phase mains frequency transformers were connected in an open delta configuration.

For frequencies between 1 kHz and 10 kHz, motor-alternators were used. These units were extremely robust and reliable but the high maintenance costs and low efficiency, especially at low power outputs, has meant that over the last decade they have been superseded by solid state thyristor inverters. In the last five years advances in device technology and inverter circuitry have raised the operating frequency capabilities of thyristor inverters and units are now available at 1 kHz up to 1 MW, at 10 kHz up to 400 kW and at 50 kHz up to 100 kW (Hobson 1984).

For applications requiring a radio frequency (rf) supply, particularly between 50 kHz and 10 MHz, triode valve oscillator power supplies are almost universally used. A large DC voltage is applied between the anode and the cathode of the valve and the high frequency output is usually fed to a parallel resonant circuit possibly incorporating a matching output transformer. Operating in Class C mode operating efficiencies of valve oscillators rarely exceed 60%. The capital cost of valves has risen sharply over the last decade whereas the cost of solid state devices has fallen and their availability increased. Hence for some years attempts have been made to replace valve oscillators with transistorised power supplies. Units using parallel combinations of bipolar transistors are available within this frequency range but they have limited power output capabilities and poor reliability. They have

* The reader is referred to the References.

made little impact industrially, usually being associated with applications within laboratory type environments.

The development of high power field effect transistors called Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) has made high power solid state units for induction heating feasible. The MOSFET is a majority carrier device and hence has far shorter turn-off times and lower switching losses than bipolar transistors. Turn-off times of less than 200 ns for a device capable of carrying 15 Amps and blocking 400 V are typical.

A MOSFET is switched on by charging up the input capacitance and hence is a voltage driven device. The drive power requirements for a MOSFET are therefore much less than those of a bipolar transistor.

Induction heating applications require relatively large power outputs therefore a major advantage of MOSFETs is that their positive temperature coefficient of resistance facilitates paralleling devices for higher power outputs. MOSFET power supplies are far more reliable than supplies using bipolar transistors which require special circuit configurations to avoid thermal runaway.

An induction heating power supply using MOSFETs is therefore more efficient, more easily controllable and has lower capital cost than existing valve oscillator power supplies.

CHAPTER 2REVIEW

In this chapter the efforts of other workers involved with circuit topologies and switches which are relevant to induction heating power supplies in the frequency range 100 to 400 kHz are described. These results lead to the preliminary investigations in Chapter 3 being focused mainly on a current fed inverter using power MOSFETS.

2.1 REVIEW OF CIRCUIT TOPOLOGIES

To assess a topology it is necessary not only to investigate whether it meets the requirements of the induction heating load but also to assess if it makes full use of the advantages and minimises the effects of the drawbacks of available switches.

Most of the switching configurations described in this chapter have been used in commercial equipment with thyristors operating typically between 1 kHz and 10 kHz. (Tebb et al 1985c).

2.1.1 The Current Fed Topology

The schematic diagram of the full bridge current fed inverter is shown in Fig. 2.1. Operation of the circuit has been described by many authors (Cordier 1977, Landis 1970 and Spash et al 1972) as this is a very common configuration for induction heating power supplies using thyristors.

The three phase supply is full wave rectified. A fully controlled thyristor bridge is used and varying the input voltage to a dc link provides the means of power control. A choke in the dc link smoothes the current so that a rectangular wave of current is fed to the load by the inverting bridge. Most induction heating work coils have a Q greater than 10 so they are resonated in a tank circuit to avoid the supply having to carry large amounts of reactive power. If a series resonant tank circuit was used for the current fed inverter then the high frequency components of the rectangular current wave would see a high impedance and voltage spikes would be produced. Therefore the inverter feeds a parallel resonant circuit. Since the Q of the tank circuit is relatively high the voltage waveform across the tank circuit has a nearly sinusoidal shape. If thyristors are used they are triggered so that the tank circuit is fed above its resonant frequency so that it presents a capacitive load to the inverter. Waveforms of the load current and voltage are shown in Fig. 2.2. This means that if the switch $S1$ is conducting and the thyristor in the same limb of the opposite pole of the bridge, namely $S3$, is triggered then $S1$ will be commutated off by the tank circuit voltage.

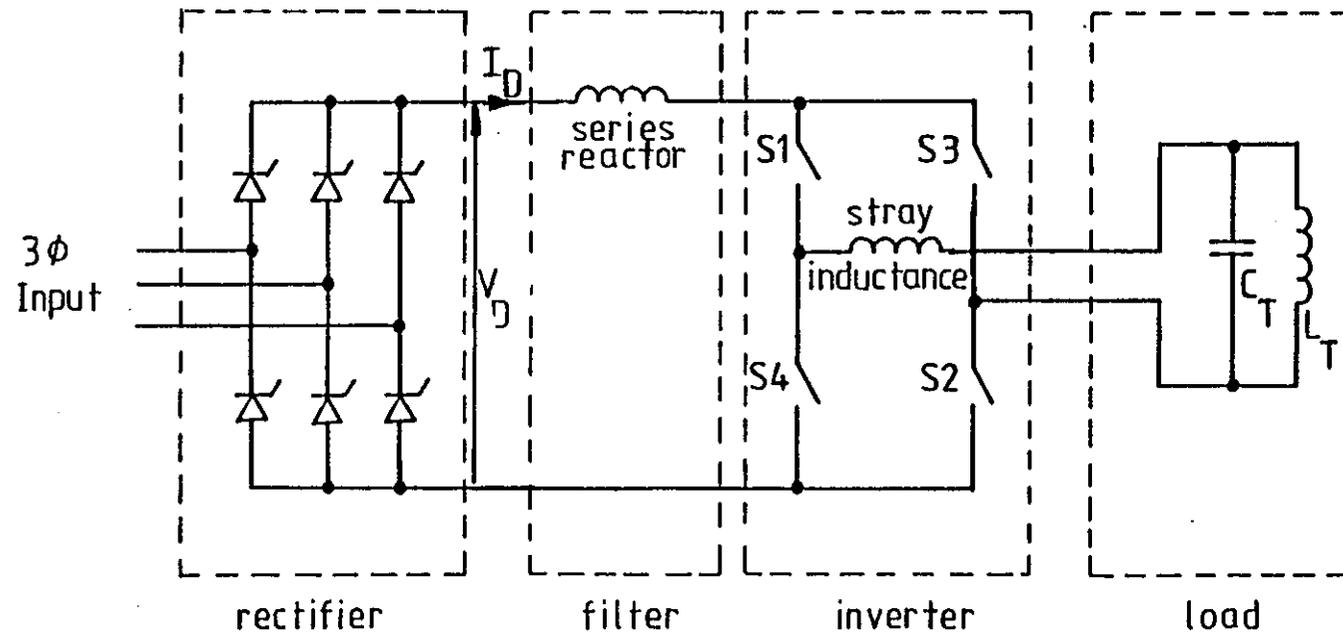


Figure 2.1 - A schematic diagram of the full bridge current fed inverter.

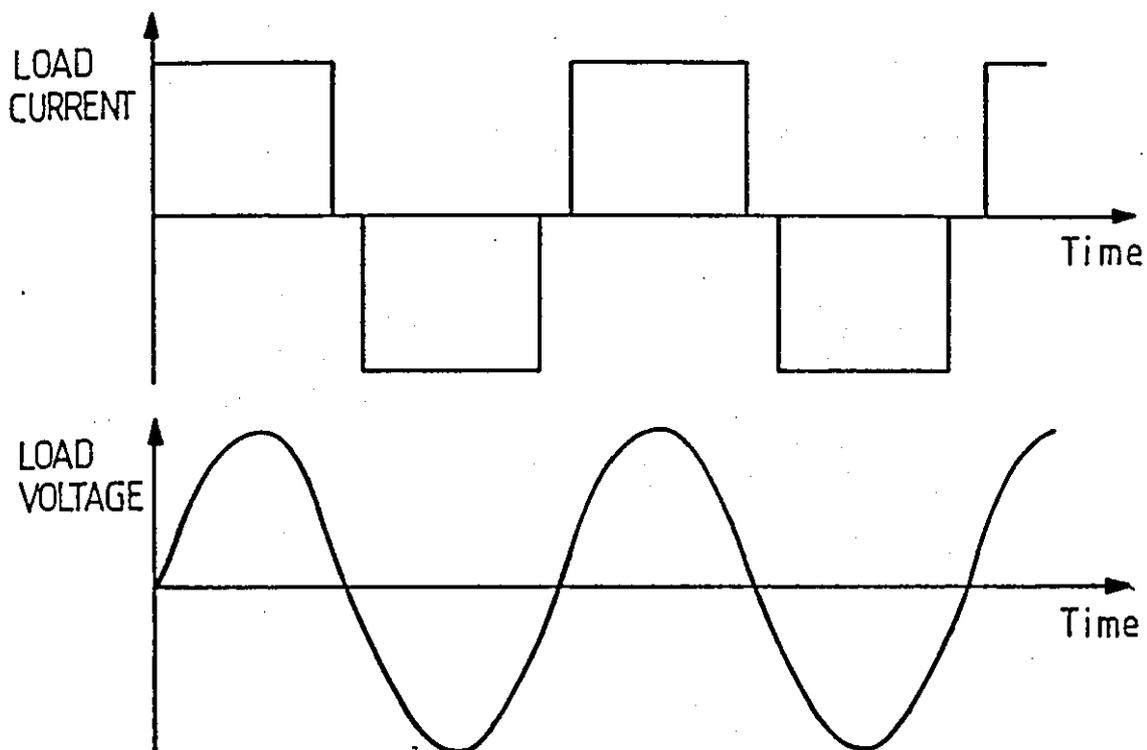


Figure 2.2 - Waveforms of (a) the current through the tank circuit and (b) the voltage across the tank circuit in a current fed full bridge inverter.

The link current is determined by the direct voltage applied to the link and the impedance of the tank circuit at the operating frequency.

The main advantages of the circuit are firstly its inherent short circuit protection which is provided by the smoothing choke. This is very important in induction heating supplies since the workcoil is very prone to being short circuited. Secondly no diodes are required to carry reactive current so the circuit has a low component count. Finally the fundamental frequency of the high frequency ripple on the supply current, which is at twice the switching frequency, will not usually change much and so filtering is easier. (Steigerwald 1984, Jones 1979).

The disadvantages of the current fed inverter are that it has bulky chokes and the method of power control causes the power factor of the equipment to be non-unity and variable. A 'pony' circuit may be needed to start the inverter since initially there is not enough energy in the

tank circuit to ensure safe commutation of thyristors in the inverting bridge.

2.1.2 The Voltage Fed Topology

In the schematic diagram of a voltage fed full bridge inverter in Fig. 2.3 it is seen that the three phase supply undergoes full wave rectification using an uncontrolled diode bridge. The dc voltage is smoothed using a capacitor so that switching in the inverting bridge causes a rectangular wave of voltage to be applied across the load. If the rectangular voltage waveform was developed across a parallel resonant circuit current spikes would have to be carried by switches since the high frequency components of voltage would see a low impedance. Therefore the voltage fed inverter most easily feeds a series resonant circuit. Since the tank circuit has a Q typically greater than 10 the load current will approximate to a sinewave. When the tank circuit is fed off resonance reactive current is carried by diodes connected in parallel with the switches in the inverting bridge. Power control is generally by a swept frequency technique.

The disadvantages of the voltage fed approach are firstly that it has no inherent short circuit protection and so it needs to have fast overcurrent protection. Secondly the impedance at resonance of the tank circuit is only the sum of the series loss components of the reactive elements. This means that a matching transformer is needed if the ratings of commercially available switches are to be fully utilised. If the drive pulses to switches have not got an exactly 50% duty cycle or if the layout is unsymmetrical a direct component of voltage can appear across the primary of the matching transformer. This would cause saturation of the transformer and so yet another component, i.e. capacitor C_{BC} , is needed. Capacitor C_{BC} is connected in series with the transformer as shown in Fig. 2.3. (Frank 1982). Thirdly if a switch is turned on while the diode in parallel with the transistor in the adjacent limb of the same pole of the inverter is conducting, e.g. S4 turned on when D1 is conducting, then a shoot-through is caused. This is caused by the supply being short circuited for the reverse recovery time of the diode (Frank 1982). To overcome this problem the tank

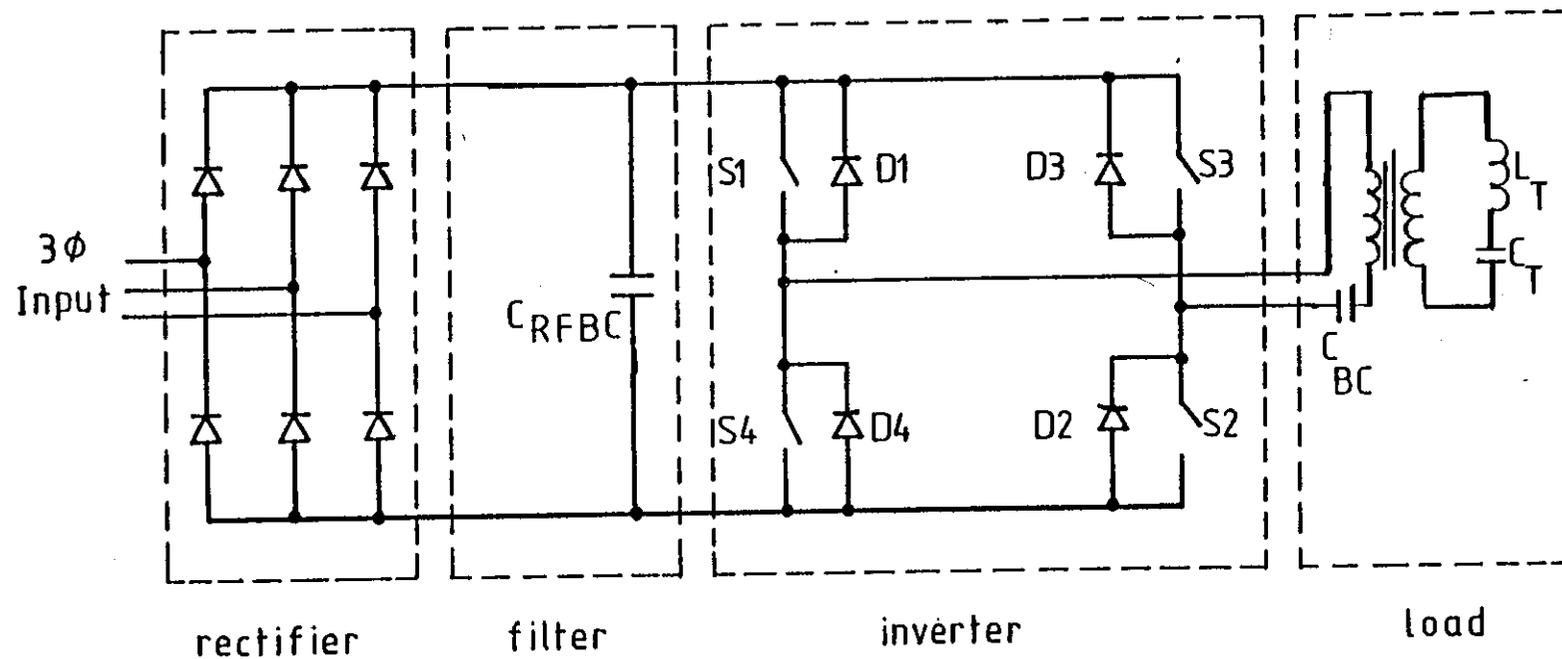


Figure 2.3 - A schematic diagram of the full bridge voltage fed inverter.

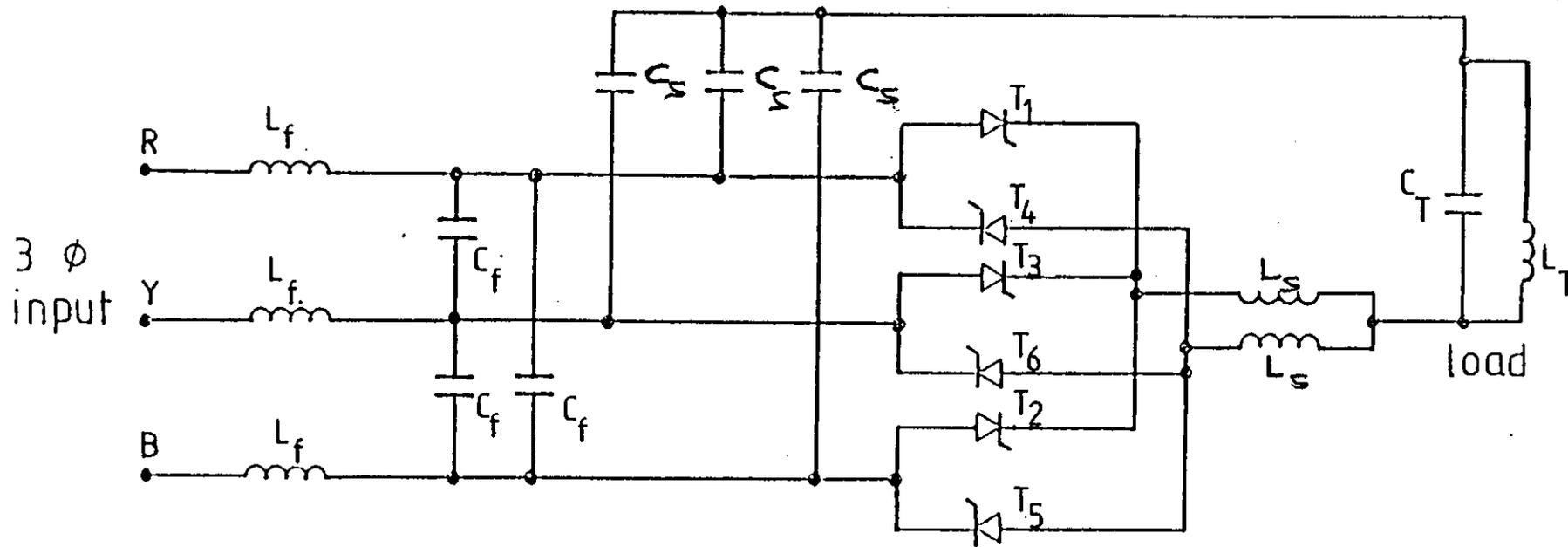


Figure 2.4 - A schematic diagram of a cycloinverter.

circuit is fed above resonance so that switches take over conduction from the diode in parallel with them. Feeding the tank circuit above resonance makes the control electronics more difficult and the switches in the inverting bridge have to handle reactive power. The component count is made larger by the need for parallel diodes, the matching transformer and C_{BC} . Finally with swept frequency power control the frequency of high frequency harmonic currents taken from the supply is continually changing so filtering is more difficult.

2.1.3 The Cycloinverter

The inverters described so far have a dc stage with either a capacitor or inductor to store energy. Another possibility is to convert from mains frequency straight to high frequency. These inverters are similar in principle to cycloconverters which are used for variable frequency drives to induction motors. The supplies for motors are usually at lower frequency than mains whereas the induction heating supplies have much higher frequencies. In industry cycloinverters using thyristors have been used at frequencies up to 3 kHz and power levels over 1 MW largely for induction melting furnaces. During one cycle of output frequency the mains voltage will change negligibly and so for analysis is represented as a direct voltage source. For this reason the high frequency ac-ac supply for induction heating is called the cycloinverter. (Havas et al (1970).

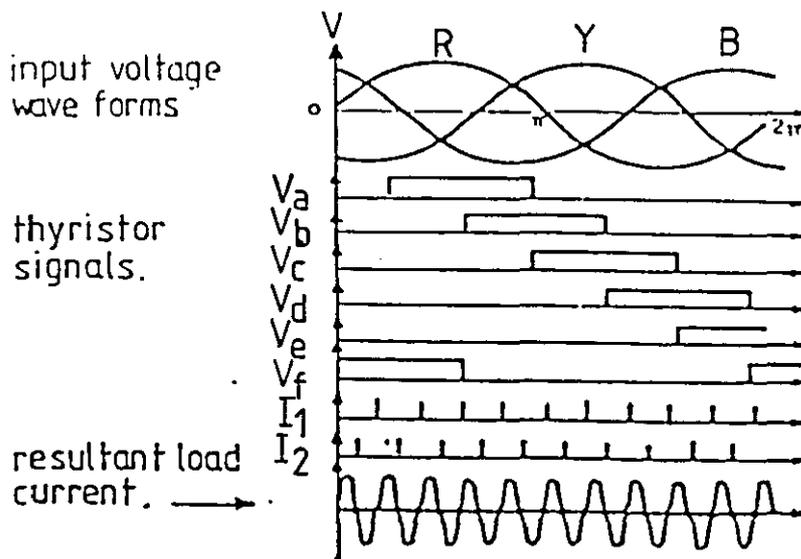


Figure 2.5 - Waveforms associated with the cycloinverter.

The schematic diagram of a cycloinverter using thyristors is shown in Fig. 2.4. Control signals are derived from zero crossings of load current and phase crossings of supply voltage as shown in Fig. 2.5. One signal is provided which is the logic AND of I_1 and V_a , another the AND of I_1 and V_c and another the AND of I_1 and V_e . A thyristor in the positive phase is triggered depending on which of these signals is true e.g. if V_a ANDED with I_1 is true T_1 is triggered. Similar logic controls the firing of the thyristor in the negative phases. To control power the signals derived from phase crossings (V_a to V_f) are delayed.

The advantage of this system is the reduced number of components and so reduced cost and increased efficiency. The disadvantages are that there is a high harmonic content in the supply currents and more complicated control circuitry.

2.1.4 The Class C Amplifier

Above 100 kHz and at power levels of 5 kW and above the triode valve operating in self excited Class C mode has been the main source of power for induction heating loads (Krauss et al 1980). The schematic diagram of the valve operating in Class C mode is shown in Fig. 2.6. The supply voltage is transformed up to typically 2.5 kV for a 1.5 kW valve and then rectified using a diode bridge. High frequency currents are prevented from being fed back to the supply by the air-cored choke. A blocking capacitor (C_B) prevents the workcoil short circuiting the dc supply. During the conduction period of the valve a pulse of current flows from C_B through the valve and the tank circuit. C_B is charged up from the dc link. The conduction angle of the valve is typically 120° and the efficiency of the circuit is usually less than 60%. Three factors mainly contribute to the low efficiency. Firstly the valve sustains a substantial voltage when it is conducting. Secondly the anode voltage needs to remain positive with respect to the grid which limits the peak anode voltage swing. Thirdly only the fundamental component of the current pulse contributes substantially to the power developed in the tank circuit. Solid state switches can dissipate only small amounts of power in themselves relative to the power that valves can dissipate. The Class C amplifier will make poor use of a solid

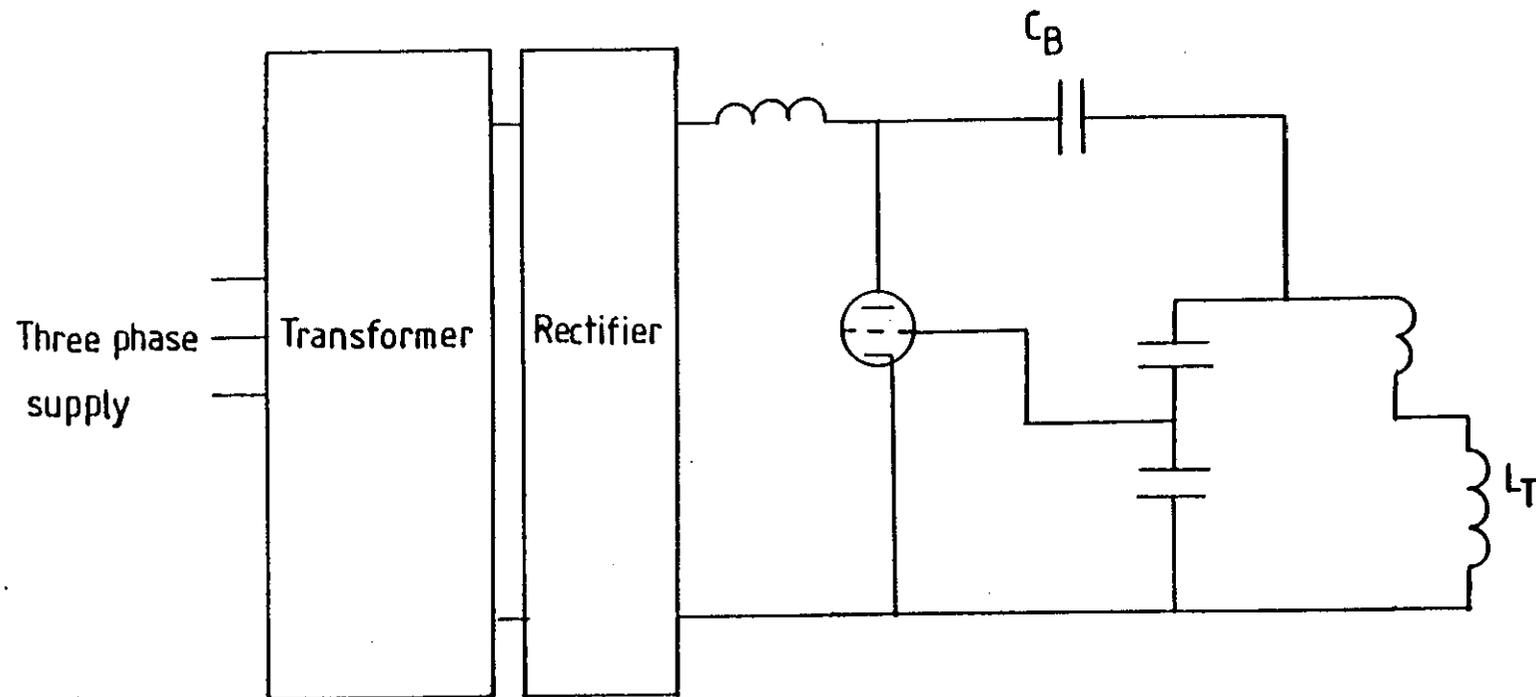


Figure 2.6 - A schematic diagram of a valve oscillator power supply.

state switch's switching capability.

2.2 REVIEW OF DEVICES

The suitability of a device for induction heating at 100 to 400 kHz depends on both its frequency and power handling capabilities. These criteria are affected very much by the particular circuit configuration used. Subjective judgements are needed to assess the performance of a device in a circuit configuration using device characteristics obtained under conditions of standard test circuits. Mindful of these constraints members of the MOSFET family and possible alternatives are now assessed for the application.

2.2.1 The Valve

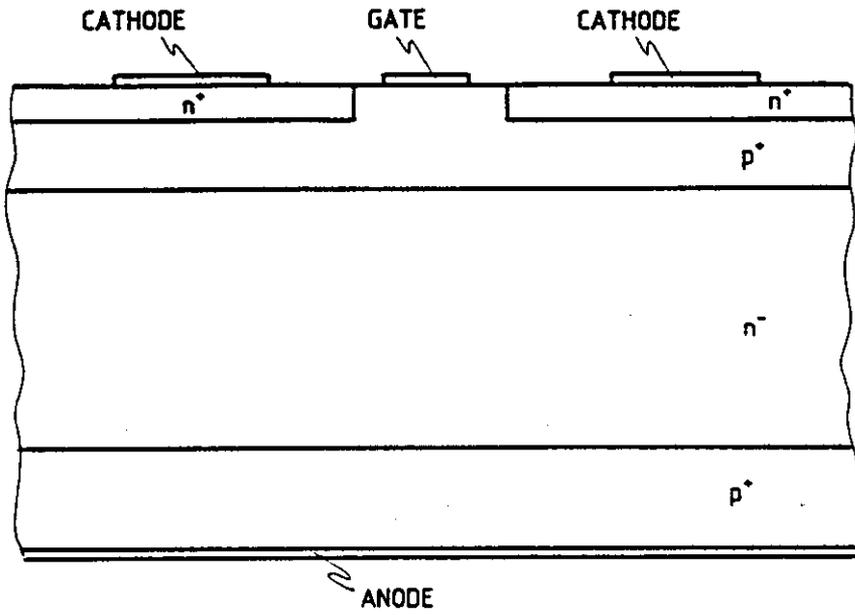
The triode valve used in the Class C Amplifier configuration has for a long time been the main source of power for induction heating above 50 kHz. The triode has three electrodes called the grid, the anode and the cathode (Dittrich 1977). The cathode is heated and has a coating to encourage thermionic emission from its surface. Electrons emitted by the cathode travel towards the anode forming an anode current. The flow of electrons is controlled by both the anode potential and the grid potential. By making the grid very negative with respect to the cathode the anode current can be reduced to virtually zero as happens for part of a cycle in Class C operation. A large cathode surface area is required to achieve even the thermionic emission required for an anode current of 1A so valves are bulky. A 1.5 kW valve will typically have a maximum anode voltage of 2.5 kV and an anode current of less than 1A. This high voltage causes a safety hazard, there are difficulties of corrosion if the valve is water cooled and care has to be taken to ensure that cooling water leaving a valve power supply is not at a dangerous potential. The electrodes are enclosed in a glass envelope making the valve a fragile component. A 1.5 kW valve costs about four times as much as an IRF450 which is a MOSFET with a 6.5 kVA switching capability so valves are expensive compared to solid state switches. Valves also have a shorter life time than is usually expected from a solid state device.

2.2.2 Thyristors

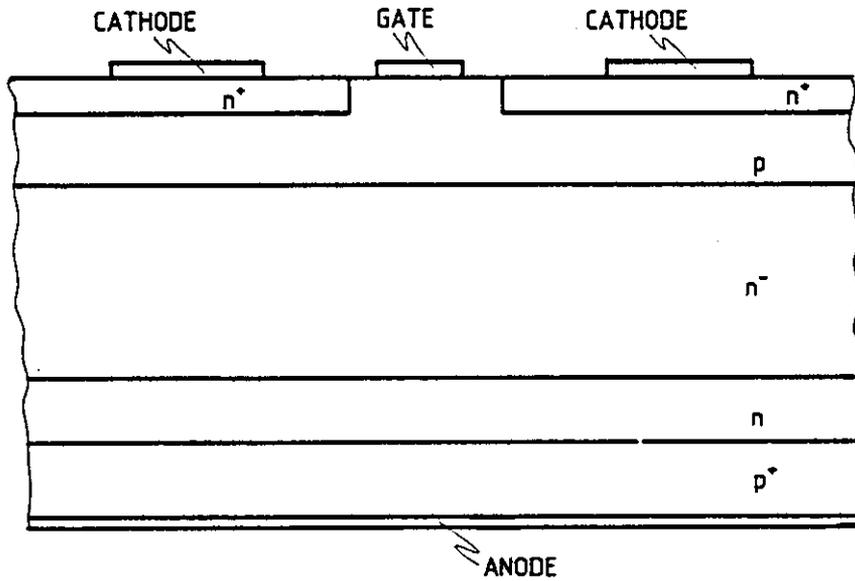
Thyristors are the most widely used solid state switch in induction heating power supplies. Their use in supplies operating above 50 kHz though is extremely limited because of their poor high frequency capability.

2.2.2.1 The Asymmetric Silicon Controlled Rectifier

As can be seen in Fig. 2.7 in an Asymmetric Silicon Controlled Rectifier (ASCR) the doping profile of the n^- region in the conventional SCR is modified and an additional n diffusion is introduced between the n base and the anode emitter. (Burgum et al 1981b). Compared to a conventional thyristor with the same forward voltage rating this modified thyristor would have a lower on-state voltage at the expense of much reduced reverse blocking capability. To manufacture a thyristor with better high frequency performance gold doping of the n^- base is used to reduce the lifetime of minority carriers in the region. The net effect of these changes is a much faster thyristor with reduced reverse blocking capability and a similar on-state voltage drop. Like conventional thyristors there is a minimum time after forward conduction has ceased before the ASCR can block forward voltage. This time is typically greater than 5 μ s so the upper frequency limit of the device is still well below 100 kHz.



(a) The conventional thyristor.



(b) The ASCR.

Figure 2.7 - Schematic diagrams of the structure of
 (a) the conventional thyristor
 and (b) the Asymmetric Silicon Controlled Rectifier (ASCR).

2.2.2.2 The Gate Turn-off Thyristor

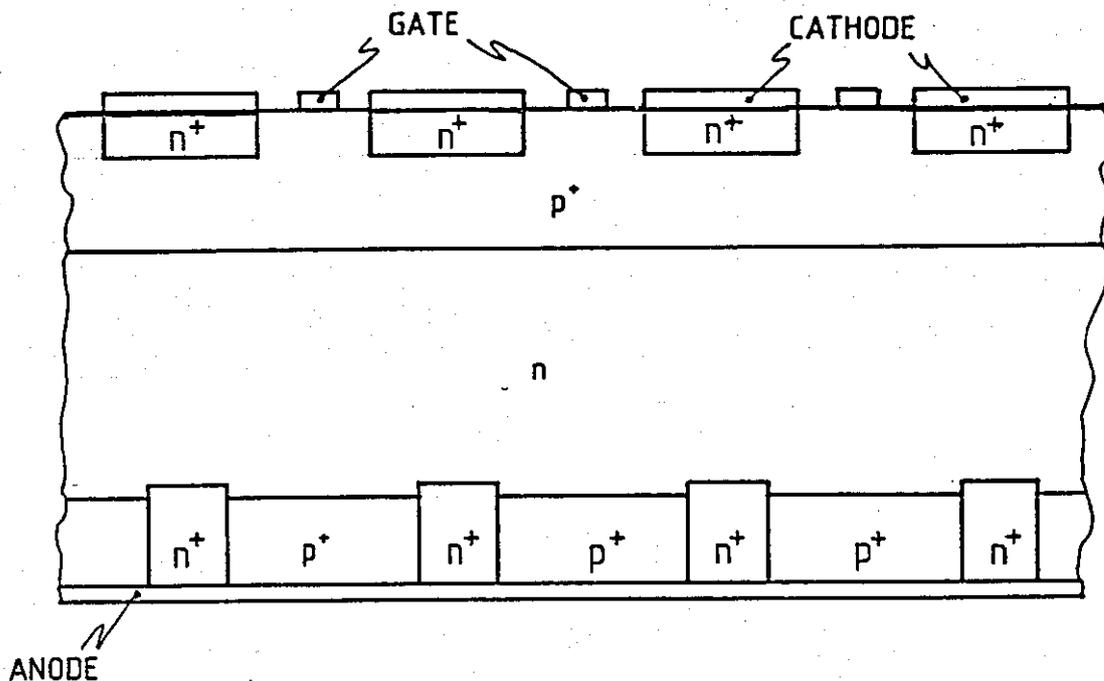


Figure 2.8 - A schematic diagram of the structure of a Gate Turn-Off Thyristor (GTO).

The structure of the Gate Turn-Off Thyristor (GTO) shown in Fig. 2.8 shows that the p^+ emitter region has been modified. A resistor R has been introduced into the two transistor representation of the thyristor as shown in Fig. 2.9. The resistor reduces the gain of the pnp transistor. The gain of this transistor is further reduced by making the base wider and by controlling the carrier lifetime. Careful control of the diffusion profiles maximises the gain of the npn transistor. The advantage of this structure is that negative gate drive can be used to interrupt regeneration and turn the device off. (Burgum et al 1980, Woodworth 1981, Burgum 1981a, Burgum 1982). The maximum frequency of operation of a GTO is 80 kHz so this device is not suitable for

induction heating above 100 kHz.

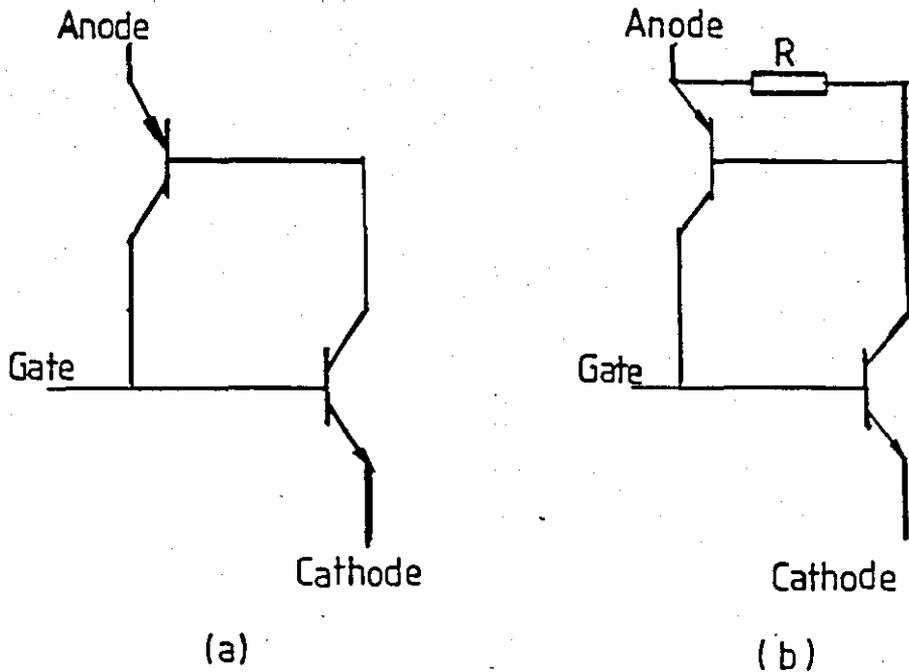


Figure 2.9 - The two transistor equivalent of (a) the conventional thyristor and (b) the Gate Turn-Off Thyristor (GTO).

2.2.3 The Bipolar Transistor

The bipolar transistor is inferior to the MOSFET for induction heating power supplies in the frequency range 100 to 400 kHz with up to 20 kW power output mainly because it is limited in its switching speed if it is going to be capable of handling sufficient power.

Bipolar transistors are minority carrier devices and so have appreciable storage time while minority carriers are swept out of the base region. A typical storage time for a very high speed 400V, 10A device is $1.0\mu\text{s}$ (Fuji Semiconductors, 1985). This is 40% of the time period at 400 kHz and so its use is not practical at this frequency. Although the storage time can be reduced by increasing the negative bias applied at turn-off this can have a detrimental effect on fall time (Motorola 1982). Clamping circuits such as the Baker clamp (Bonkowski 1984) can be used to ensure that the collector base junction does not become forward biased. This however increases the conduction losses and can affect the turn-on time (Taylor 1982). Reverse Emitter Current Drive (REC Drive)

(Rischmuller 1984) can also be employed to extend the frequency range of power devices but this involves elaborate drive circuitry.

Increasing the current rating of a bipolar transistor involves using a larger die. The cost of this transistor will be much greater since the yield will be less and a more expensive package may be needed. (Fuji Electric Company 1981). For this reason paralleling of devices is reluctantly resorted to (Thoma et al 1984). Variations in the characteristics of paralleled devices can cause both static and dynamic unbalance causing greater power dissipation in one device than another. This will cause the kVA switching capability of the paralleled devices to be reduced and can cause device destruction. Of the various factors influencing current balance, differences in the saturated base emitter voltage and the emitter terminal resistance have greater influence than differences in the current gain and collector terminal resistance. The negative temperature coefficient of resistance of the transistor can cause thermal runaway. The problem of static unbalance can be solved by connecting a resistor in the emitter of each paralleled transistor so that a transistor's collector emitter saturated voltage drop becomes an insignificant factor in determining its collector current. This however reduces efficiency. To alleviate dynamic unbalance a 30% derating is usually necessary. If the cost penalty of derating is to be avoided snubbers can be used but these slow the rise of current and the fall of voltage and therefore limit frequency capability. Work has been done to use closed loop control of emitter current during the switching interval (Auckland 1982). Although this equalises the power dissipation between paralleled devices it does not reduce the overall long rise and fall times of bipolar transistor waveforms relative to those of power MOSFETs.

There are problems of paralleling MOSFETs and paralleling bipolar transistors however these problems are much worse with the bipolar transistor because of the possibility of thermal runaway and its poor peak to average current carrying capability.

Bipolar transistors also have larger drive power requirements than power MOSFETs causing lower efficiency of the equipment and more complicated drive circuitry.

2.2.4 The Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

In a Field Effect Transistor (FET) the conductivity of a channel is varied by applying voltage to a control or gate terminal (G). There are two other terminals in most FETs which are connected internally to a channel. These are the source (S) and drain (D) terminals. In an n channel FET the channel is made of n type material and the drain is normally positive with respect to the source. In a p channel FET the drain is normally negative with respect to the source. The gate terminal is taken to a potential nearer that of the drain to reduce the resistance of the channel. An enhancement mode FET is turned off when the gate and source are at the same potential and a depletion mode FET is turned on with gate and source terminals at the same potential. There are two main types of FET called the Junction FET (JFET) and the MOSFET (Siliconix 1984). The schematic representation of the JFET is shown in Fig. 2.10. To modulate the resistance between the drain and source terminals the voltage at the gate terminal is varied which varies the width of the depletion layer which exists mainly between gate and drain terminals.

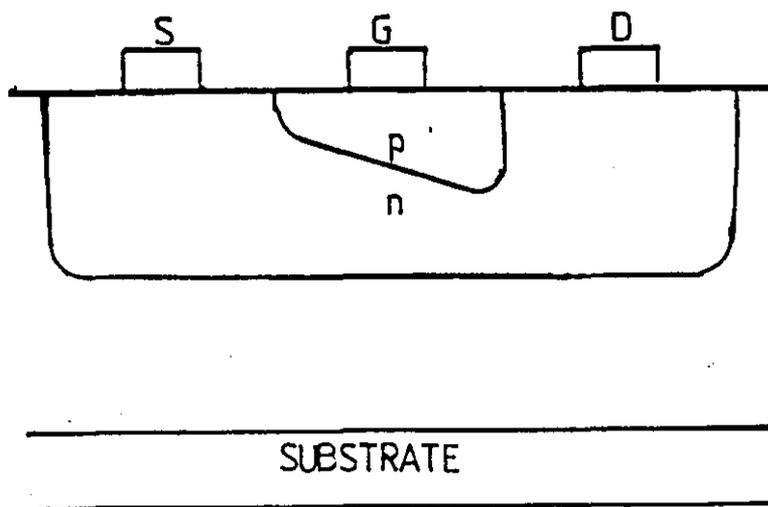


Figure 2.10 - A schematic diagram of the structure of the Junction Field Effect Transistor (JFET).

All JFETs are depletion mode devices because if the gate is made positive with respect to the source excessive current will flow. Depletion mode devices require two power supplies and so are more difficult to use than enhancement mode devices where the gate drive circuit power supply can be derived from the drain source supply rail. The MOSFET has a layer of insulating material between the gate and the channel. Electric field lines caused by charge on the gate cross the insulating layer and vary the channel carrier concentration and so the channel resistance. This is called inversion of the channel.

If a dc voltage source is connected across the drain and source terminals of an n channel enhancement mode MOSFET, with the positive terminal connected to the drain, and the voltage between the gate and source terminals is varied the following changes in drain current will occur. As the gate to source voltage is increased from zero so that the potential of the gate becomes nearer to that of the drain there will be a negligible drain current until a voltage called the threshold voltage (V_T) is exceeded. If the gate to source voltage is now set to a value greater than the threshold voltage and the drain to source voltage is increased from zero the following changes in drain current will be observed. Any increases in drain to source voltage will be accompanied by increases in drain current until a value of drain to source voltage is reached called the pinch-off voltage. Increasing the drain to source voltage above the pinch-off voltage will cause only a small change in drain current. These two regions of operation are called the Ohmic Region and the Saturation Region. The two regions can be seen in a typical DC characteristic of an n channel enhancement mode MOSFET shown in Fig. 2.11.

Present day Power MOSFETs are vertical double Diffused MOSFETs (DMOS). A schematic representation of the MOSFET structure is shown in Fig. 2.12. The idea of a vertical channel MOSFET has been known since the 1930s but it was not until the mid 1970s that the technology of diffusion, ion implantation and material treatment had reached the level necessary to produce DMOS on a commercial scale. The vertical diffusion technique uses technology more commonly associated with large

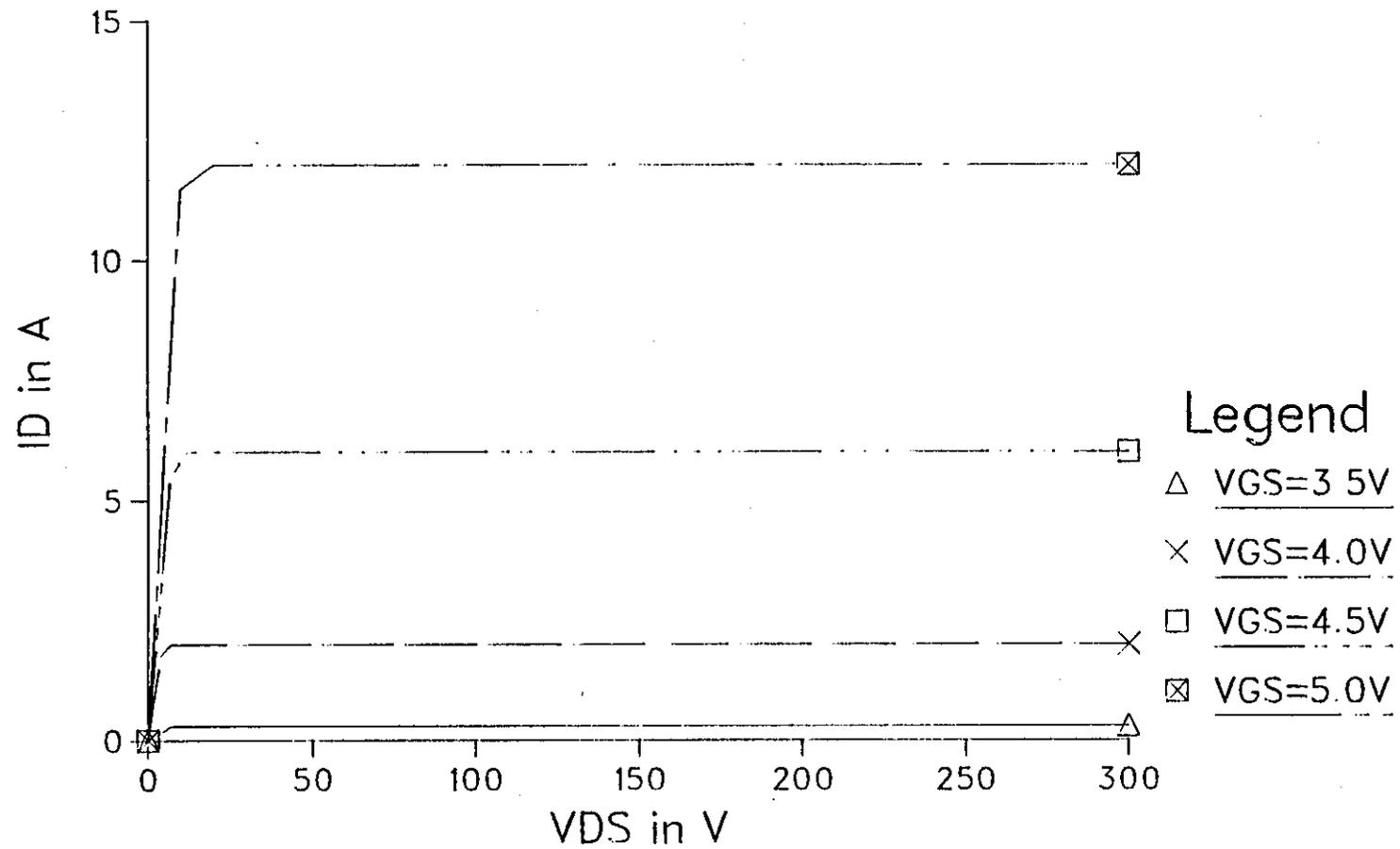


Figure 2.11 - The typical DC Characteristic of an n channel enhancement mode MOSFET.

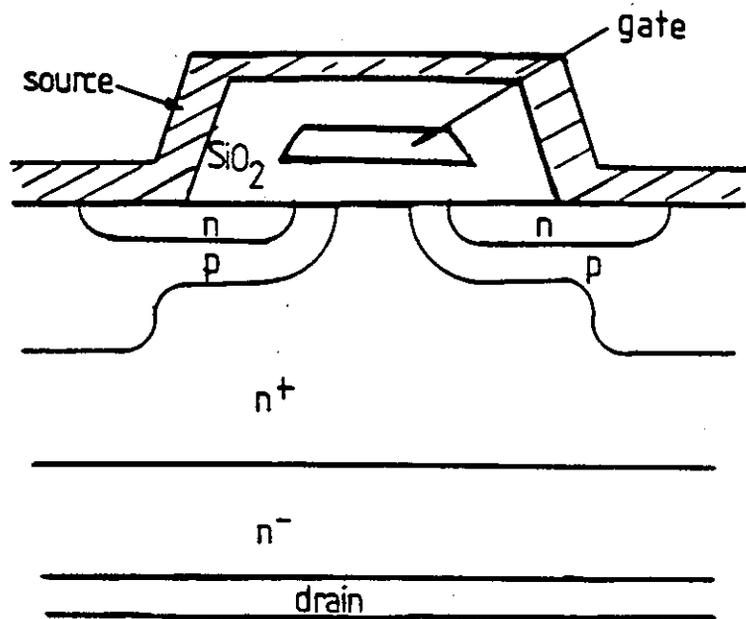


Figure 2.12 - A schematic diagram of the structure of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET).

scale integrated circuit manufacture than traditional power device fabrication.

The first diffusion is that of the p type body region in an n channel device. Next an n type diffusion is done. The channel width can be controlled repeatably at 1 or $2\mu\text{m}$ with diffusion as opposed to 4-5 μm with the photolithographic process used for planar FETs. Initially gate electrodes were made of metal but now they are mostly polycrystalline silicon. This means that interconnections between cells can be diffused rather than having to be made by metallisation and bonding so manufacturing is made easier. A low on-resistance is achieved since many cells are paralleled on the same slice. It can be seen from Fig. 2.12 that there is a parasitic npn transistor inherent in the structure between the source and the drain. The emitter and base are shorted by source metallisation and so this parasitic element manifests itself in device operation as a parasitic diode in parallel with the MOSFET channel. The reverse recovery time (t_{rr}) for this diode in the IRF450 is typically 1300 ns. This t_{rr} value causes problems of shoot-through followed by voltage spikes in lead inductance in some circuits. In current fed circuits the high impedance supply caused by the choke in the link prevents these problems with the parasitic diode.

p channel power MOSFETs are not as attractive for power switching since their on-resistance is higher than n channel MOSFETs. This is because in silicon the hole mobility is much less than the electron mobility.

2.2.4.1 The Safe Operating Area

The Safe Operating Area (SOA) for the IRF450 is shown in Fig. 2.13. The peak pulse current is based on a current above which internal connections may be damaged. The maximum continuous current is limited by the Joule heating increasing the temperature of the silicon so that thermal degradation of the material occurs. This is an rms current limitation rather than an average current limitation in the case of minority carrier devices. For pulses with small duty cycles the permissible pulse amplitude is increased.

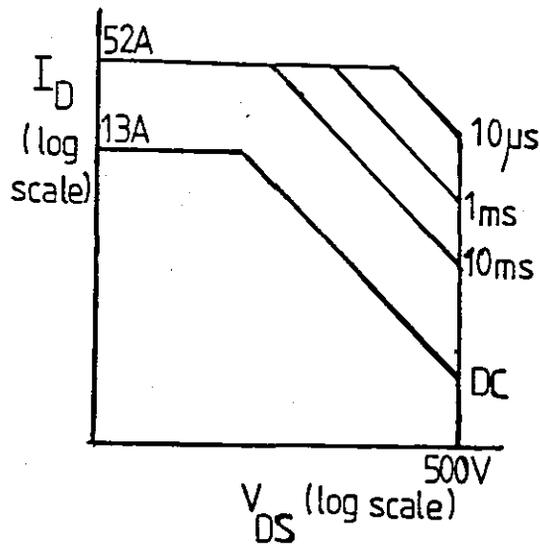


Figure 2.13 - The Safe Operating Area (SOA) of the IRF450.

If the maximum voltage rating of the MOSFET is exceeded avalanche breakdown or drift region depletion layer punch-through will occur. For the smallest on-resistance for a given voltage rating the MOSFET is designed so that these two breakdowns happen at the same voltage (Baliga 1982).

The SOA graph in Fig. 2.13 is useful in illustrating the way in which maximum values of current and voltage and duty cycle of operation constrain device operation. This graph is only valid for a case temperature (T_C) of 25°C and a junction temperature (T_J) of 150°C . For an induction heating supply a junction temperature of 80 to 100°C would be preferable as this will increase the Mean Time Between Failures (MTBF) and so increase reliability. In the industrial environment the induction heating power supply is likely to be short circuited. If a T_J of 80°C instead of 125°C is used the ability of the MOSFETs to withstand a large current spike when the output is short circuited is improved. To calculate the maximum rms current permissible with $T_J = 80^\circ\text{C}$ the

power losses in the device at various levels of current need to be found. This knowledge is combined with information on the thermal impedances of case to heatsink and heatsink to ambient as well as the ambient temperature in order to find the operating current levels.

2.2.4.2 The Losses in MOSFETs

There are four main causes of power dissipation in MOSFETs.

(a) Conduction losses (P_C).

The conduction losses are given by Eqn. 2.1

$$P_C = I_D^2 R_{DS(ON)} \quad (2.1)$$

The on-resistance when the MOSFET is operated in the Ohmic region ($R_{DS(ON)}$) is dependent on the junction temperature (T_J). T_J is a function of the power dissipated in the device so calculating P_C is made more difficult. To make matters more complicated it is not usually possible to express the dependence of $R_{DS(ON)}$ on T_J in a simple equation. For this reason a graphical method is often used to find P_C (Siliconix 1984).

$R_{DS(ON)}$ increases with the voltage sustaining capability to the power of typically 2.6. So increasing the voltage rating of switches in the inverter causes a penalty of increased conduction losses.

$R_{DS(ON)}$ is also a function of V_{GS} and I_D . For this reason in high power units, such as induction heating power supplies, when devices are paralleled for greater power output V_{GS} values as high as 15V are applied to reduce $R_{DS(ON)}$.

For MOSFETs rated above 100V the resistance of the epitaxial layer dominates the on-resistance and has a high positive temperature coefficient of resistance. In low voltage devices the channel resistance, which has a negative temperature coefficient of resistance, has a major effect. This means that the temperature coefficient of

$R_{DS(ON)}$ for a higher voltage device will be larger than for a lower voltage device. Thermal runaway will be better guarded against in a unit using higher voltage devices than in one using lower voltage devices. This is advantageous for a 20 kW induction heating power supply which will have a three phase supply and so will more easily use higher voltage devices.

(b) Switching losses (P_S).

When a MOSFET is turned on or off it carries large currents and sustains a large voltage at the same time and so dissipates a large amount of power. Switching losses are negligible at low frequencies but are dominant at high frequencies. The crossover frequency depends on the circuit configuration. For reasons explained in Section 2.2.4.3 a MOSFET usually turns off more slowly than it turns on so the losses at turn-off will be larger than at turn-on. Switching losses are very dependent on circuit configuration since the turn-off time is affected by the load impedance.

Snubber components can be connected across the MOSFET to reduce turn-off losses (Lockwood et al 1983, Lauritzen et al 1983 and Undeland et al 1984). Inductors, either saturating or not, can also be connected in series to limit the rate of rise of current at turn-on to reduce turn-on losses (Lockwood et al 1983). With resonant loads, such as the current fed inverter feeding a parallel resonant load, switching can take place at a zero crossing in tank circuit voltage so switching losses are very much reduced.

(c) The diode dissipation (P_{DD}).

A good approximation of dissipation in the diode inherent in the structure of the MOSFET is the product of the diode voltage drop, which is typically less than 1.5V, and the average current carried by the diode.

In a voltage fed inverter the internal diode can be used to carry reactive current. If a current fed inverter feeds a parallel resonant circuit below its resonant frequency it looks inductive and so the voltage across a MOSFET tries to reverse. The diode will clamp this excursion. If a simple two element parallel resonant circuit is used and parasitic lead inductance is negligible then the diode will have to carry the circulating current. This is a large current typically greater than ten times the rms current carried by switches when the tank circuit is fed at resonance. One effect of parasitic lead inductance is to reduce the current that the diode carries. A more sophisticated tank circuit investigated in Chapter 4 reduces the diode current even further.

(d) The gate power dissipation (P_G).

If the internal gate resistance is R_G and the external drive resistance is R_{DR} then P_G is given by Eqn. 2.2.

$$P_G = C_{IP} V_{GSD}^2 f \left(\frac{R_G}{R_G + R_{DR}} \right)$$

where V_{GSD} is the gate drive voltage and C_{IP} is the input capacitance of the device. The input capacitance of the device varies greatly with the gate drain voltage so Eqn. 2.3 is more useful.

$$P_G = q_g V_{GSD} f \left(\frac{R_G}{R_G + R_{DR}} \right) \quad (2.3)$$

where q_g is the peak gate charge.

Since the induction heating supply will be working in the range 100 to 400 kHz the f term in Eqn. 2.3 will be large. Induction heating supplies often provide many kW of power so MOSFETs will be paralleled. The peak gate voltage will be as high as 15V to reduce differences in $R_{DS(ON)}$ between paralleled MOSFETs for better sharing and also to reduce

values of $R_{DS(ON)}$ for better efficiency. This means that P_G will be more important than in some other applications.

2.2.4.3 The Switching Characteristics of MOSFETS

In Fig. 2.14 typical gate source and drain source voltages for a MOSFET switching current through a resistive load are shown. The gate source capacitance needs to be charged up to a threshold voltage (V_T) of about 3V before the MOSFET begins to turn on. The time constant for this is $C_{GS}(R_{DR} + R_G)$ and the time taken is called the turn-on delay time ($t_{D(ON)}$). When V_{GS} has passed the threshold voltage the MOSFET starts to turn on and V_{DS} begins to fall. C_{GD} now needs to be discharged as well as C_{GS} being charged so the time constant is increased and the gradient of V_{GS} reduced. As V_{DS} becomes less than V_{GS} the value of C_{GD} increases greatly since it is depletion dependent and a plateau occurs in the V_{GS} characteristic. The time taken for I_D to rise from 10% to 90% of its on state value is called the rise time (t_r). When V_{DS} has collapsed V_{GS} continues to rise as overdrive is applied. Gate overdrive has three benefits:-

- (a) Increase noise immunity
- (b) Reduced spread of on-resistance between parallel devices
- (c) Reduced on-resistance.

It also has the disadvantages of increasing the gate power dissipation and also the turn-off delay time ($t_{D(off)}$).

In turning off the MOSFET the overdrive is first removed. The charging path for C_{GD} and C_{DS} now contains the load resistor (R_L) so the turn-off time will be generally longer than the turn-on time.

The above description is valid for a MOSFET switching a resistive load. For a current fed inverter feeding a parallel resonant load part of the MOSFET drain current will be a sinusoidal charging current for snubber capacitors. It is difficult to extend the idea of a rise time from 10% to 90% of on state current to this circuit.

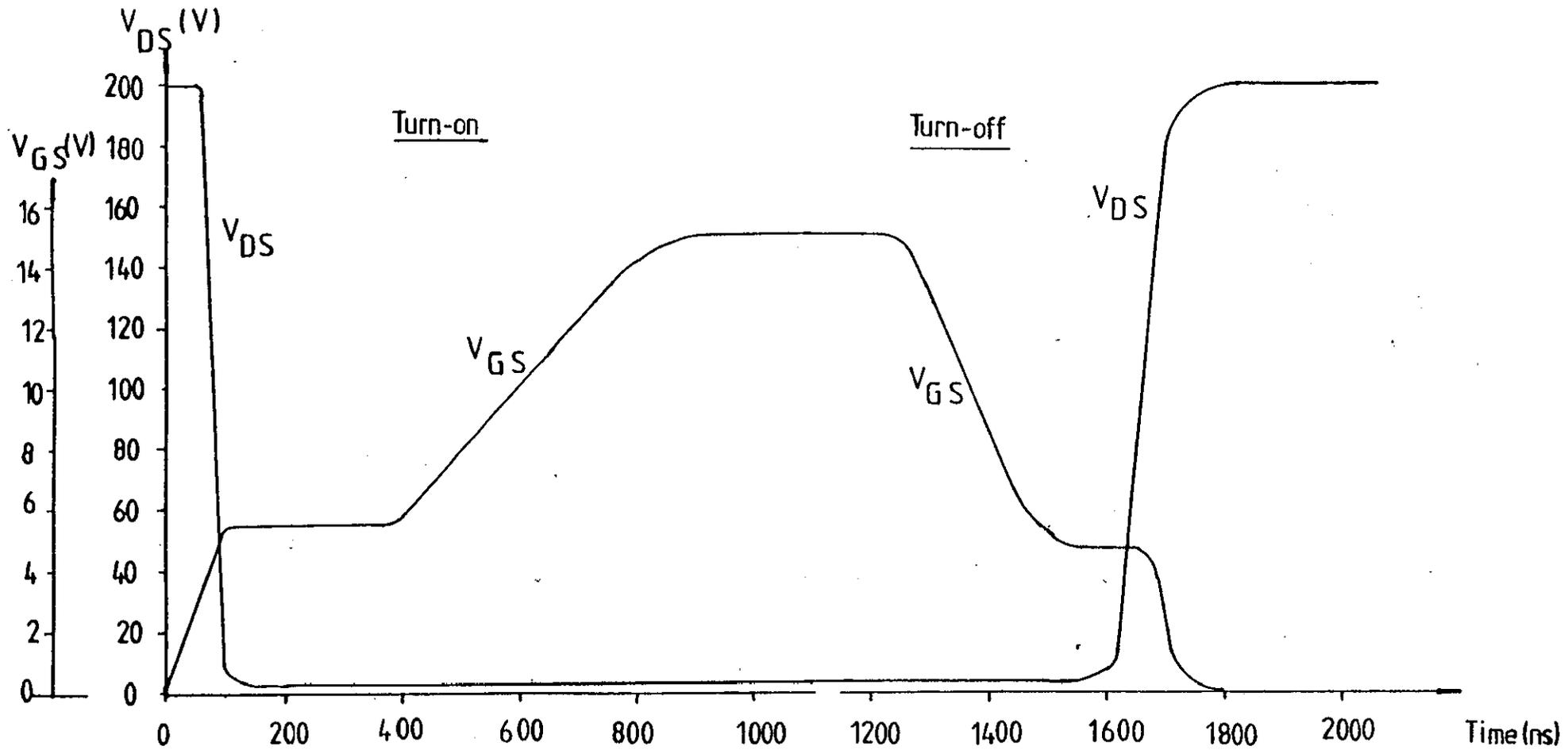


Figure 2.14 - The switching waveforms for a MOSFET.

2.2.4.4 Paralleling of MOSFETs

Induction heating power supplies require larger power outputs than are possible using one MOSFET in each limb of an inverting bridge. To increase the power output devices can be paralleled and this is made easier using MOSFETs because they have a positive temperature coefficient of resistance. If one paralleled MOSFET carries more current than the others it becomes hotter than them. This causes the MOSFET's on-resistance to become greater than the others' and so the current in it reduces. This prevents thermal runaway in one of the devices. The positive temperature coefficient also helps to prevent hot spots within the MOSFET.

There are two aspects to equal current sharing between paralleled MOSFETs. Firstly there is static balance which is equal sharing of current between devices when they have been turned on. There is also dynamic balance which means equal sharing of current between devices when they are turning on or off.

To carry the maximum total current the paralleled MOSFETs need good thermal coupling. (Gauen 1984a, Kassakian 1983). If poor thermal coupling was used and the positive temperature coefficient of resistance was relied on to promote static balance then the transistor with the lowest on-resistance would need a junction temperature much greater than a MOSFET with a higher on-resistance. The lower junction temperature of the MOSFET with higher on-resistance would limit its current carrying capability. Static balance would exist so all the MOSFETs would carry the same current and the total current would be limited. The higher junction temperature of some of the MOSFETs would reduce their reliability. Thus although the positive temperature coefficient of MOSFETs helps to prevent thermal runaway it is not large enough to make static balance practical.

Since a mechanism of equal sharing relying on the positive temperature coefficient of resistance involves the heat capacity of devices it is not quick enough to guarantee dynamic balance. The peak to average current carrying capability of MOSFETs is excellent so, for up to three

paralleled devices, dynamic unbalance is not a problem so long as it is only for a short time. For more devices in parallel some circuits such as the current fed inverter have inherent protection against dynamic unbalance, see Section 8.2.

A large gate overdrive helps static balance by reducing the spread of on-resistances of paralleled MOSFETs. Obviously symmetrical layout improves both dynamic and static balance.

Since MOSFETs have a good high frequency performance parasitic oscillations can occur involving the MOSFET and parasitic reactive elements of both the MOSFET and the circuit. (Kassakian et al 1984). The oscillations usually occur between 1 and 300 MHz and can involve a single device or paralleled devices. Careful layout, e.g. short connections, helps to avoid these oscillations. When devices are paralleled a differential resistor in the gate lead of each device is recommended to increase the damping.

2.2.4.5 dv/dt Turn-On

Unwanted turn-on of a MOSFET can be caused by a fast rate of rise of drain to source voltage (Severns 1981). There are three ways in which this can be caused. Firstly the charging current for the gate drain capacitance produces a voltage drop across impedances in the gate drive circuitry. This can cause the gate to source voltage to be greater than the threshold voltage and the device to turn on.

The second method involves the collector base capacitance and the base to emitter resistance of the bipolar transistor inherent in the structure of the MOSFET. If the charging current for the collector base capacitance is large enough a voltage can be developed across the base resistor that is large enough to turn the bipolar transistor on. Typically a rate of rise of drain to source voltage of 100 V/ns with a peak drain to source voltage of 350V can cause the parasitic bipolar transistor to turn on.

Finally the MOSFET can be damaged when it sustains voltage immediately after the parasitic bipolar transistor has been conducting. If the parasitic transistor had been carrying its rated current before the MOSFET was turned off a rate of change of drain to source voltage of 20 V/ns would be sufficient to cause damage to the device.

To avoid spurious turn-on by the first method the following precautions can be taken. The gate drive impedance should be kept low by choosing a value of external gate resistance less than 100 Ω and connecting a diode in parallel with part of this resistance. The connections from the gate drive circuit to the MOSFET should be twisted and kept as short as possible. Spurious turn-on by the second method is very unlikely since rates of rise of drain to source voltage greater than 100 V/ns are very difficult to obtain.

Problems with dv/dt turn-on are very much reduced if a current fed topology is used. In a current fed inverter used for induction heating the MOSFETs sustain a half sinewave of voltage so the rate of change of drain to source voltage is less than in a voltage fed inverter. If there is a spurious turn-on of a MOSFET then the rate of rise of current will be restrained by the choke in the dc link, so damage to MOSFETs will be avoided. Careful design of matching circuitry and keeping the inverter switching frequency close to the resonant frequency of the tank circuit reduce the current carried by the parasitic bipolar transistor in the MOSFET. Since the parasitic transistor carries less current the likelihood of spurious turn-on by the third method is reduced.

Thus spurious turn-on of MOSFETs can occur but current fed inverters have advantages in reducing the likelihood.

2.2.4.6 Packaging

For 500V MOSFETs rated above 8A the TO204 package (formerly the TO3 package) has been the most frequently used by manufacturers. Compared to such packages as the TO220 it has typically 0.1 times the case to heatsink thermal resistance at the expense of internal drain and source inductances of 1.5 times those of the TO220 package.

During the past few months two other packages for MOSFETs have come onto the market which are the multiple die package and the TO218 plastic package.

The multiple die package typically contains four dice arranged as either four MOSFETs in parallel or one pole of an inverter with 2 MOSFETs in parallel in each limb (see manufacturers' literature). This package has the advantages of an isolated case making construction of equipment easier and it reduces component count. The four dice have similar characteristics since they are taken from the same area of the wafer and will have undergone similar processing. (Gauen 1985, Schultz 1984). This will improve current sharing between the dice. There are six disadvantages of the multiple die package all but one of which will particularly affect high frequency inverters.

- (a) The inductances of internal connecting leads between drain and source terminals are not the same for each die and so there is both dynamic and static unbalance. Therefore the current carrying capability of the package is derated with frequency.
- (b) The input capacitance is approximately equal to the sum of the input capacitances of the individual dice. It is not possible to charge this larger capacitance as fast as four individual drive circuits can drive the four individual dice. This makes switching times longer.
- (c) Making connection to this package presents the problem of selecting leads that can carry 30A at 400 kHz.
- (d) The power dissipation of the multiple die package is 500W compared to 600W of four TO204 packages in parallel. Since there are greater switching losses at higher frequencies the additional dissipation is an advantage.

- (e) The kVA switching capability of a full bridge increases in increments of 22 kVA if say IRFK 20450 modules are used. This large increment can lead to reduced utilisation of a unit.
- (f) The drain-source inductance is typically 20 nH and upwards of 20 A are switched off in times of the order of 100 ns so appreciable voltages are developed across internal inductances. For this reason a derating graph of the rate of change of drain current against V_{DS} is included in data sheets. For a current fed circuit where switching takes place at a zero crossing of voltage this is not a problem.

It would appear that the multiple die package is most suitable for frequencies less than 50 kHz and power levels of many tens of kW.

The T0218 plastic package has the following advantages for use at a power level of 20 kW and in the frequency range 100 to 400 kHz.

- (a) It is easy to mount as only one hole needs to be drilled.
- (b) The terminals are in line so they can easily be connected to a printed circuit board (PCB). The use of a PCB makes connection of protection and snubber components by low inductance connections easier.
- (c) The package is easier to manufacture and so the devices are about half the cost of those in T0204 packages.

The above advantages are achieved while still keeping similar thermal resistances to those of the T0204 package. It is therefore expected that power supplies for induction heating between 100 and 400 kHz will use the T0218 package for switches in the future.

2.2.4.7 A Comparison of Devices from Different Manufacturers

Manufacturers market their devices under a range of trade names such as HEXFETs from International Rectifier, TMOS from Motorola and SIPMOS from Siemens. Most power MOSFETs are vertical devices made by the double diffusion process but differences in structure may exist between devices from different manufacturers such as:-

- (a) In HEXFETs each cell is hexagonal in shape but Motorola use a rectangular structure for the cells in TMOS.
- (b) For larger devices one manufacturer may use one large die whereas another may parallel two in the same package. The single die is preferable since additional gate resistors will have to be included in the two die package to overcome problems of parasitic oscillations (Kassakian 1983) and this will reduce switching times.

When comparing data sheets the most important electrical parameters are breakdown voltage, maximum continuous current, on-resistance and switching times. Comparison of data sheets is made more complicated because different manufacturers measure these important parameters under different conditions. An example of these differing conditions is that switching times may be measured with different gate drive resistances, different on-state currents and different off-state voltages. Some manufacturers give switching times not just for one set of conditions but give graphs showing how switching times vary with drive resistance etc. It is possible therefore to compile Table 2.1 comparing similar devices from different manufacturers. The largest voltage rating of devices without markedly worse on-resistance is 500V. It is necessary in a current fed unit to use the highest possible voltage devices to ease matching so 500V devices are compared. The current ratings of MOSFETs in Table 2.1 are relatively high at between 12 and 20A to reduce component count in the unit. It can be seen from Table 2.1 that the IRF450 compares favourably with other manufacturers' devices. International Rectifier were contacted and kindly provided more than enough IRF450s for the work described in this thesis.

Manufacturer	MOSFET	Drain to Source Breakdown Voltage (V)	Maximum Continuous Drain Current (25°) (A)	$t_{D(on)}$ (ns)	t_r (ns)	$t_{D(off)}$ (ns)	t_f (ns)	maximum $r_{DS(on)}$ (Ω)
International Rectifier	IRF450	500	13	35	50	150	70	0.4
Motorola	MTM15N50	500	15	120	300	400	240	0.4
Siliconix	VNP006A	500	20	70	200	190	160	0.3
Hitachi	2SK313	450	12	20	80	110	60	0.9
Mullards	BUZ 45	500	9.6	50	100	450	100	0.6

Table 2.1 - A comparison of the electrical parameters of similar MOSFETs from different manufacturers.

2.2.4.8 Future Trends in MOSFETs

Research into the structure of power MOSFETs is concentrated in the following areas.

(a) Increased switching speed.

The developments in induction heating power supplies in this work are in the range 100 to 400 kHz so switching losses can be substantial. Increasing switching speed will reduce these losses and so make the equipment more efficient. C_{GD} is a very important determining factor in switching speed so attempts have been made to reduce this (Hinchliffe et al 1986 a,b). These attempts usually involve moving the gate electrode further from the drain or reducing its area. Two examples of reducing C_{GD} by altering the device structure are the Self Aligned Terraced Gate MOSFET (STGMOSFET) (Ueda 1984) and the ISOFET (Moss 1983).

The performance of a MOSFET depends on the material used in its fabrication. The frequency response of the MOSFET increases in proportion to the mobility and the energy band gap of the semiconductor used. Silicon is the best element for use as the semiconductor but the use of binary alloys such as Gallium Arsenide (GaAs) and ternary alloys has been investigated. For instance GaAs has a frequency response over seven times better than that of silicon. There are however problems in the inversion of the GaAs layer and work is being done to overcome these (Baliga 1982).

(b) Increased kVA switching capability.

An increase in the kVA switching capability of a device would reduce the component count, and so the cost, of a unit for a given output power. Field limiting rings are used in higher voltage MOSFETs to prevent excessive electric fields causing breakdown in the silicon. Investigations into the arrangement of these rings have been taking place (Yoshida et al 1983) so that the area occupied by them can be made as small as possible. Thus the number of cells in a die can be increased so that the device can carry more current.

The on-resistance of a MOSFET is inversely proportional to the cube of the energy band gap and inversely proportional to carrier mobility. (Baliga 1982). Therefore investigations into the use of other materials will result in devices with semiconductors such as GaAs which have a kVA switching capability twelve times that of a similar size silicon device.

These areas of research point the way to tomorrow's devices. Power MOSFETs are relatively new on the scene and improvement in switching times and kVA handling can be expected in the future.

Advances are also taking place in putting logic and power switching on the same substrate. (Electronic Engineering 1984, Electronic Engineering 1985). This will give very much enhanced interference free connections which is important in the electrically noisy environment of an induction heating power source.

2.2.5 Bipolar and MOS Combinations

There are three ways in which Bipolar and MOS technologies have been combined. These combinations have either the two technologies resident in the same area of the die, a bipolar and an MOS device side by side in the die or two separate devices interconnected to form a switch. By combining the technologies in this way manufacturers hope to produce a switch with advantages of both technologies. (Hinchliffe et al 1986 a,b).

2.2.5.1 The MOS Thyristor

In the MOS thyristor the n^+ layer adjacent to the drain terminal of the n channel MOSFET is replaced by a p^+ layer and so a four layer device is created. This device is marketed with such trade names as the Insulated Gate Transistor (IGT) from General Electric (General Electric 1983, Chang et al 1983, Baliga et al 1984), the Conductivity Modulated FET (COMFET) from RCA (Marechal 1983, Goodman et al 1983), and the Gate Enhanced MOSFET (GEMFET) from Motorola (Pschaenich 1983, Gauen 1984b). These devices have the disadvantage that there is a storage time in their turn-off caused by the need to remove minority carriers. This means that their turn-off times are typically 4 μ s. This renders them

absolutely no use for induction heating in the range 100 to 400 kHz.

2.2.5.2 The BIMOS Switch

The BIMOS switch described in this section is either a bipolar transistor and a MOSFET on the same die or a MOS Darlington.

The BIMOS switch can be either the uncommitted type or the shunt type (Zommer 1981). The uncommitted type shown in Fig. 2.15(a) can be connected as a shunt type in Fig. 2.15(b) or as a Darlington with the MOSFET driving the bipolar transistor which is described later. In the shunt connection the MOSFET switches on quickly and the bipolar transistor a short time later. The current taken by the pair is designed to be a half sinewave and the bipolar transistor carries the majority of the peak current. The bipolar transistor is then switched off and the MOSFET carries the reduced current while the bipolar transistor turns off. Finally the MOSFET is switched off speedily. The current fed approach has many advantages for induction heating above 100 kHz. This topology does not have a resonant current so the shunt connected BIMOS cannot be used to advantage.

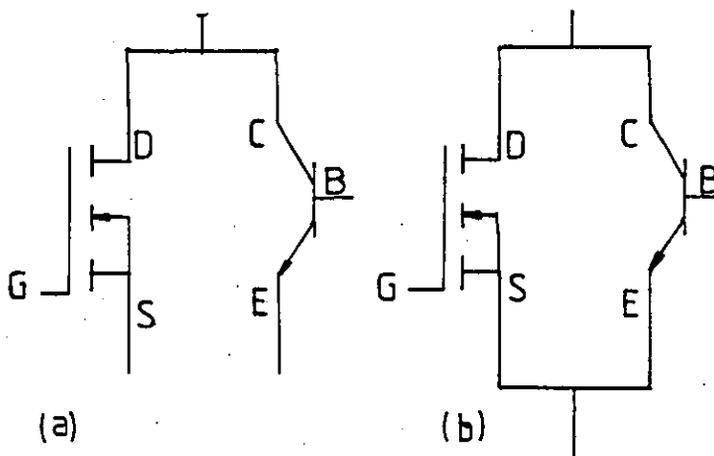


Figure 2.15 - The (a) uncommitted and (b) shunt BIMOS switch.

The MOS Darlington shown in Fig. 2.16 utilises the low drive requirements of the MOSFET and the low saturation voltage of the bipolar transistor to produce a switch with low drive requirements and large kVA switching capability. The combination is limited in turn-off time by the storage time of the bipolar device and so is not suitable for a supply working between 100 and 400 kHz.

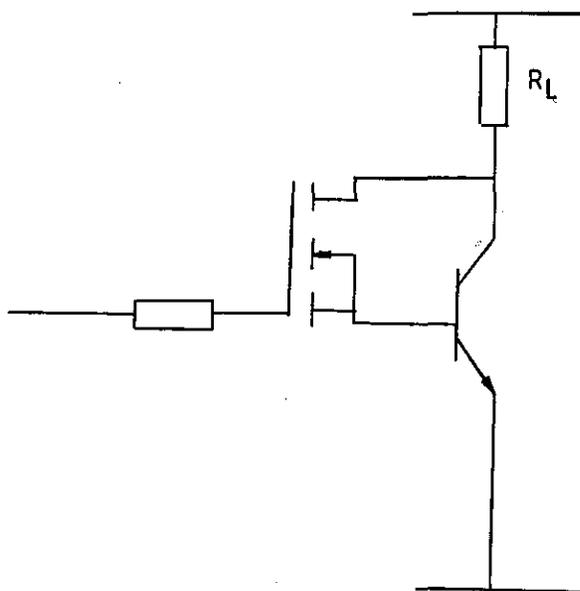


Figure 2.16 - A schematic representation of the MOS Darlington transistor.

2.2.5.3. The Cascode Connection

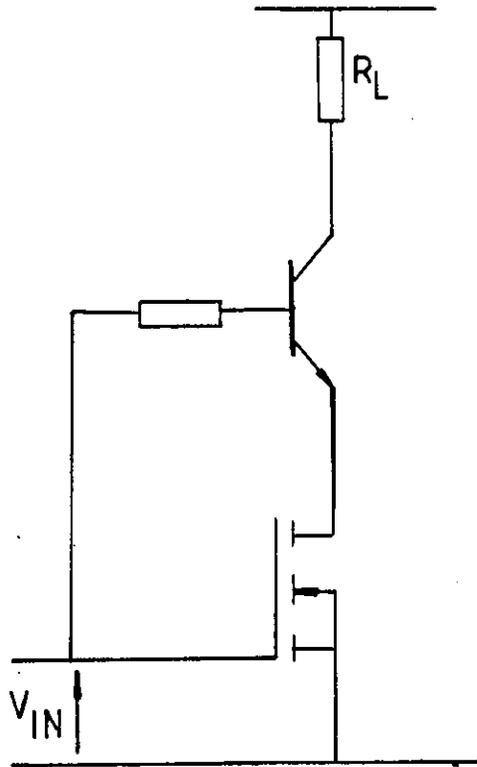


Figure 2.17 The cascode connection

The cascode connection is shown in Fig. 2.17. A bipolar transistor is connected in the common base configuration with a MOSFET in series with its emitter. To turn the combination off the MOSFET is turned off which open circuits the emitter of the bipolar transistor forcing the collector current to flow through the base. This turns the bipolar transistor off quickly. (Taylor 1981, Chen et al 1981). This arrangement would be advantageous for a current fed induction heating inverter as it would enable the tank circuit to be fed at a higher voltage which aids matching. (Tebb et al 1986c). The maximum voltage of the cascode connection is the collector base breakdown voltage with the emitter open circuit. Feeding the tank circuit at a higher voltage would mean a reduction in the size of tank circuit capacitors which are an expensive item at these frequencies. The configuration can be further enhanced by driving the base of the bipolar from a MOSFET. This reduces the drive power requirements.

The MOS and Bipolar combinations discussed so far, with the exception of the cascode and the BIMOS connections, have sacrificed the speed of the MOSFET in order to produce a switch that can handle large powers and yet have low drive power requirements. This sacrificing of switching speed has made them unsuitable for the frequency range above 80 kHz and so for this application.

2.2.6 The Static Induction Transistor

The Static Induction Transistor (SIT) is a majority carrier device and is similar to a MOSFET. The SIT exhibits an unsaturated dc characteristic. It has a low on-state voltage but has disadvantages of low power gain and complicated drive circuitry. Work is being done to overcome these disadvantages, (Gupta 1982, Ueda et al 1985).

2.3 CONCLUSIONS

It has been shown that the current fed inverter has many advantages for induction heating (Tebb et al 1984) and that the MOSFET is the switch most suitable for power supplies of 20 kW output and frequency range of 100 to 400 kHz. The IRF450 compares favourably to similar devices on the market and its ratings of 500V and 13A seem appropriate for

inverters with a three phase supply.

CHAPTER 3
PRELIMINARY INVESTIGATIONS

The suitability of current fed inverters, voltage fed inverters and the cycloinverter for induction heating between 100 and 400 kHz was investigated practically using low power prototypes.

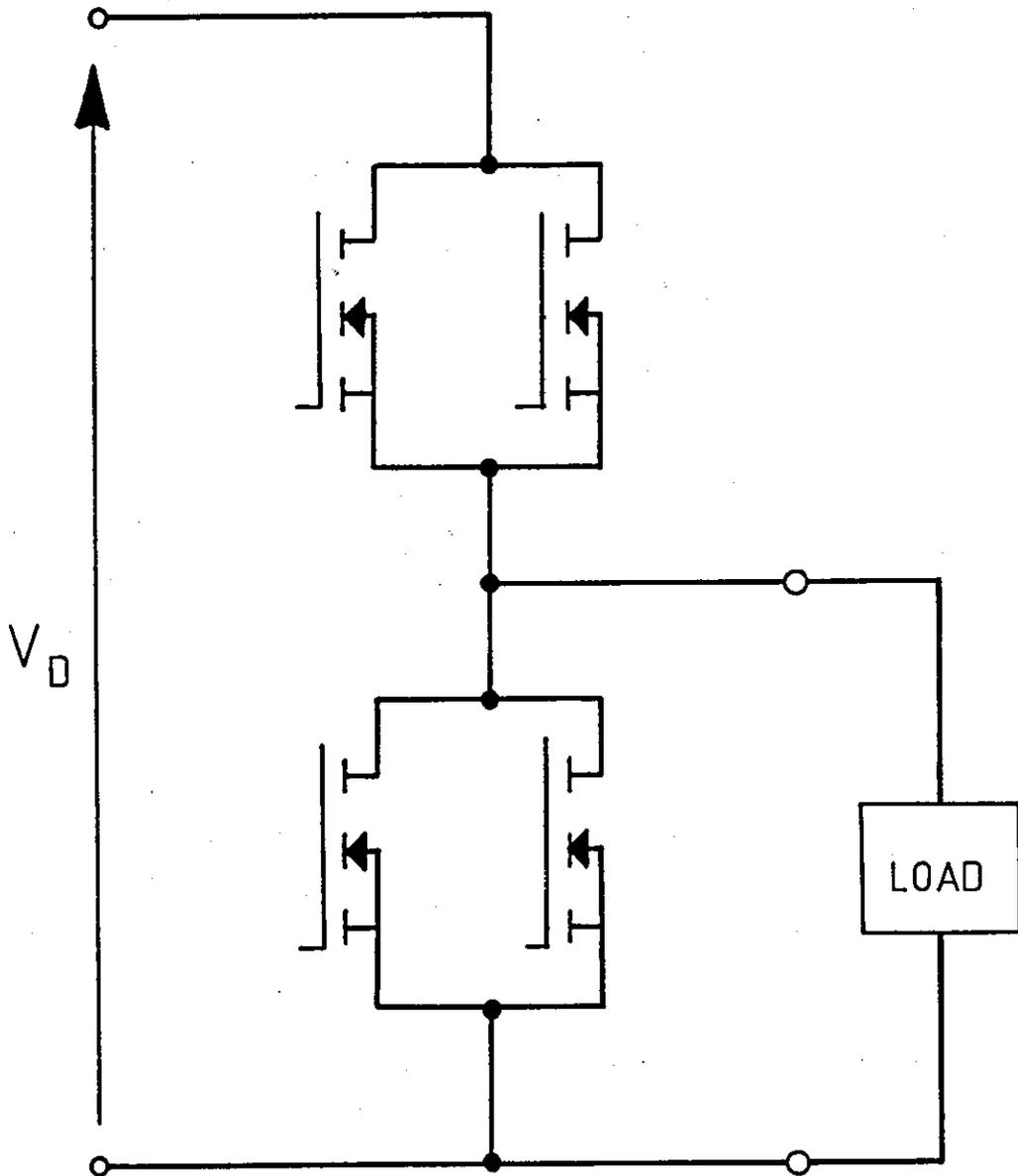


Figure 3.1 - A single ended half bridge.

3. PRELIMINARY INVESTIGATIONS

A practical assessment of possible circuit topologies was carried out in parallel with the assessment described in Section 2.1 which was based on a literature search. Low power prototypes of a cycloinverter and a current fed inverter were designed, constructed and tested. A voltage fed unit was already available. From these trials it was possible to discover the difficulties in design, layout and matching of the different topologies.

3.1 THE VOLTAGE FED INVERTER

Work has been carried out previously at Loughborough on the development of voltage fed inverters for induction heating. (Hinchliffe 1983).

The unit developed by S. Hinchliffe was used to investigate the performance of the voltage fed inverter. The input to the unit consisted of a six pulse diode bridge using standard components and computer grade electrolytic capacitors to act as r.f. bypass capacitors (C_{RFBC} in Fig. 2.3). The inverting section was a single ended half bridge with two MOSFETs in parallel in each leg, type IRF350, as shown in Fig. 3.1. Isolation in the gate drive circuits was provided by pulse transformers. The gate drive circuit used is shown in Fig. 3.2.

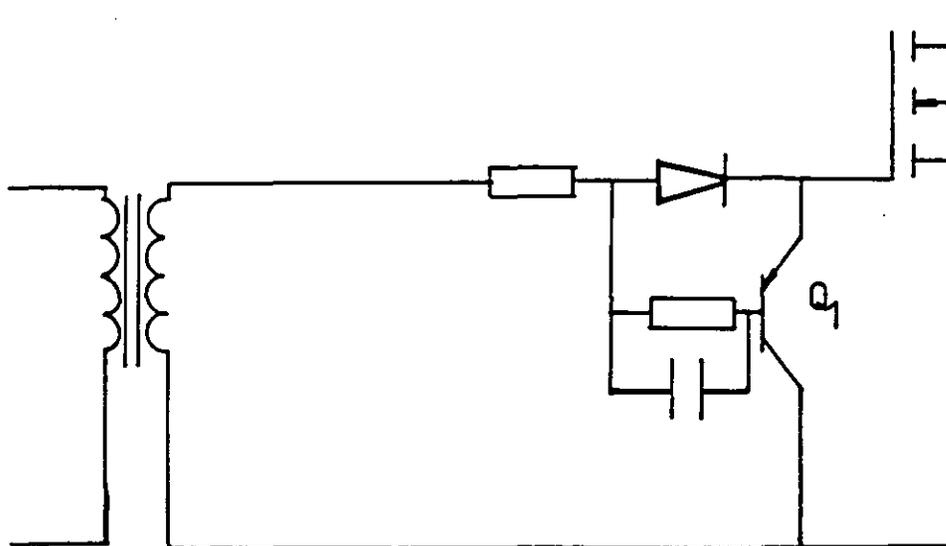


Figure 3.2 - The MOSFET drive circuit used on the voltage fed prototype.

Transistor Q_1 in Fig. 3.2 is necessary to reduce the impedance of the gate drive circuit when the MOSFET is off since problems had been encountered from dv/dt turn-on when other MOSFETs turned on (see Section 2.2.4.5). A control IC (PWM125) was used which provided such facilities as generating two complementary outputs with a presettable deadband which were used as MOSFET drive signals, the frequency of the complementary outputs was variable which was useful for implementing swept frequency power control, the mark space ratio of the outputs could be varied so that Pulse Width Modulated (PWM) power control could be used and there was an emergency shutdown input. There were two levels of overcurrent protection. A current transformer was used to sense the current in the tank circuit. The first level of protection sent a signal to the PWM 125 to take away the drive to the MOSFETs. The second level triggered a crowbar thyristor. A semiconductor fuse then operated to remove the dc supply to the inverting bridge.

The performance of the unit was investigated when it fed a series resonant tank circuit and when the output was short circuited. When the unit fed into the resonant load the switching frequency of the half bridge was above resonance to overcome problems of shoot-through described in Section 2.1.2. The following aspects of design and performance are worthy of note in assessing the unit.

- (a) When the output of the unit was short circuited devices were destroyed. The delay from the time of overcurrent detected by a rise in voltage across the burden resistor of the current transformer to the firing of the crowbar thyristors was 200 ns. The inductance of leads between the rf bypass capacitor and the MOSFETs was kept to a minimum since the current has to reverse quickly in this path. This reversal occurs when MOSFETs are switched off and conduction is taken over by diodes. If the link voltage is 100V and stray inductance is say 100 nH the current through the MOSFET pair will have risen to 200A before the crowbar thyristor is fired. The current will continue to rise during the remainder of the prearcing time of the fuse so it is not surprising that devices were damaged.

- (b) High frequency ringing at about 3 MHz was noticed on the supply rail near the MOSFETs. This was caused by a rapid reversal in the direction of current in the parasitic lead inductance between the rf bypass capacitors and the inverting bridge.
- (c) Since the impedance of a typical series resonant induction heating tank circuit is less than an ohm difficulty in matching was experienced. If the workpiece was suddenly removed then a sustained overcurrent was caused as the impedance of the tank circuit decreased.
- (d) Pick up problems caused the crowbar to be falsely triggered. This was due to fast switching of current near the crowbar when the direction of energy transfer between the rf bypass capacitor and the tank circuit changed abruptly.

3.2 THE CYCLOINVERTER

A low power prototype of the cycloinverter was designed and constructed (Tebb et al 1985a). Cycloinverters have often been used for induction heating but using thyristors as the switches. The same general circuit as shown in Fig. 2.4 was used for the prototype but extra components had to be connected to enable MOSFETs to be used. The control logic for the cycloinverter was more complicated than for other topologies and so careful consideration concerning feedback from the output current and the phase voltages of the three phase supply was necessary.

The switches in the cycloinverter shown in Fig. 2.4 were required to sustain reverse voltage. The parasitic diode in the MOSFET structure clamps reverse voltages so diodes were connected in series with the MOSFETs. Epitaxial diodes with small reverse recovery times of typically 15 ns were used to limit the period of their reverse conduction before a MOSFET in another phase turned on.

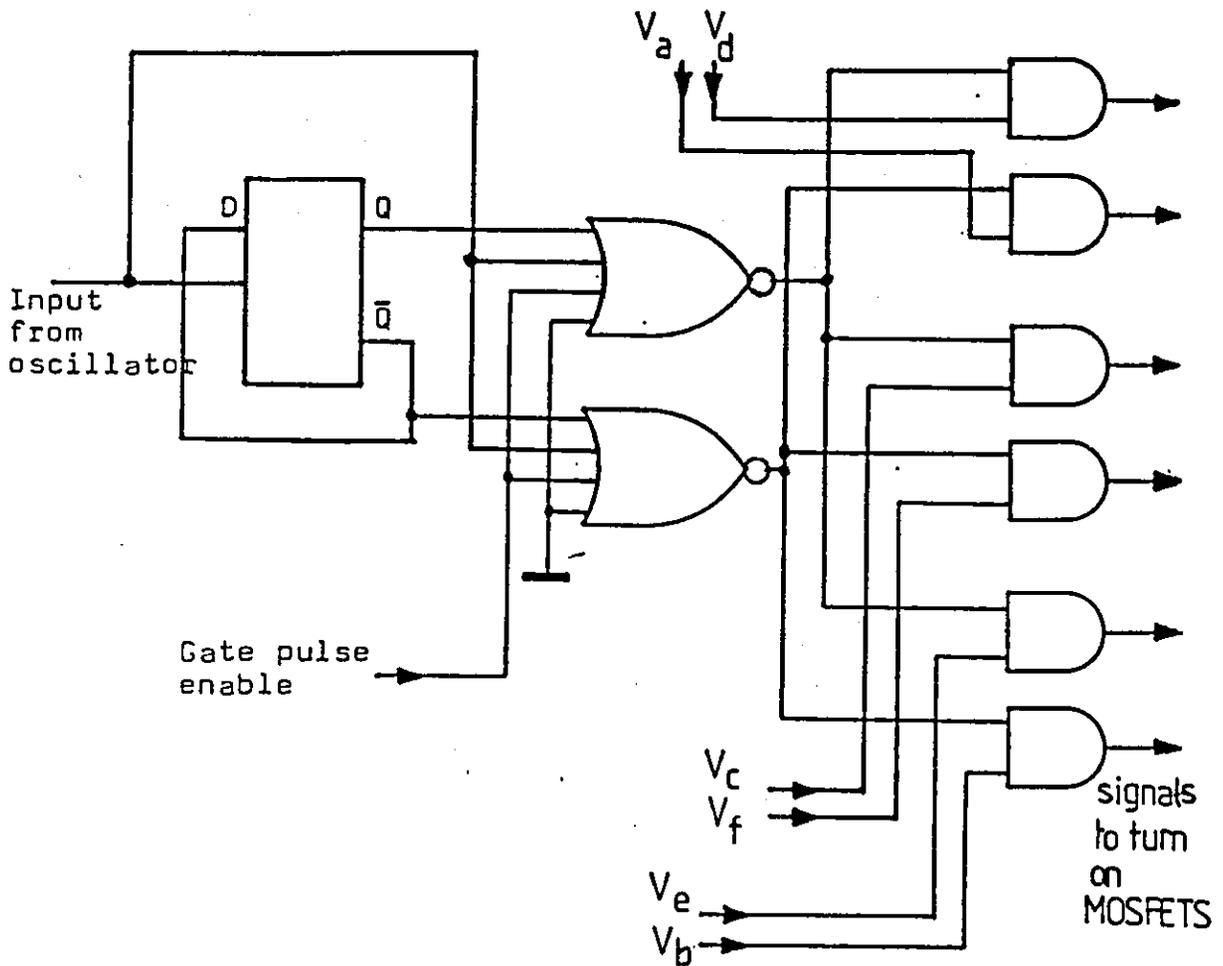


Figure 3.3 - The logic used to generate MOSFET drive signals in the prototype cycloinverter.

The logic used to provide drive signals for MOSFETs is shown in Fig. 3.3. A pulse was generated by a zero crossing detector when the current in the series resonant circuit crossed zero. The rising edge of this pulse was used to toggle the D type flip-loop in Fig. 3.3. The pulse forced the output of the two NOR gates in Fig. 3.3 to zero and so provided a deadband in the turning on of MOSFETs. If the workcoil was short circuited the current carried by MOSFETs could rise very quickly since it would be opposed only by the impedance of connecting leads. A crowbar circuit was used to remove the supply voltage from the switches

when an overcurrent happened. The overcurrent detection and crowbar firing circuitry were very similar to those used in the voltage fed inverter in Section 3.1. Design of the crowbar was more difficult for the cycloinverter because there was a three phase supply to the MOSFETs and connection of a freewheeling diode across the crowbar thyristors was ruled out since the diode would be forward biased for part of the mains cycle. Therefore a triac was connected between each phase and neutral. In the case of overcurrent the triacs would be triggered and semiconductor fuses in each phase would operate. The triggering pulses to the triacs were maintained so that when the fuses had blown the triacs could carry a freewheeling current. In the design and testing of the prototype the following points were discovered.

- (a) When the output of the unit was short circuited the short circuit protection did not act fast enough to save MOSFETs and MOSFETs were destroyed.
- (b) A problem involving matching was encountered. When the current in the series resonant tank circuit went through a zero crossing the voltage across the tank circuit capacitors was a maximum. The voltage across the MOSFETs during the deadband time could be as high as $\sqrt{2} \times Q \times \hat{V}_L$ where \hat{V}_L is the maximum line voltage. The Q of the circuit was typically greater than 10 so the three phase supply would have to be stepped down to about 20V. Thus the MOSFETs had to be rated for the full reactive power in the tank circuit. This caused a very large reduction in power output of the unit compared to the same MOSFETs used in another configuration such as a full bridge inverter.

3.3 THE CURRENT FED INVERTER

A prototype current fed inverter took longer to design and construct because of the logic circuitry required for the fully controlled rectification bridge. Although the design of this circuitry was time consuming it involved well proven technology and the advantages of the current fed approach made construction of a prototype necessary.

A relationship between the dc link voltage and the tank circuit voltage needed to be found in order to determine the maximum link voltage.

If the losses in the dc link and the MOSFETs are assumed to be negligible then, in steady state conditions, the power flowing in the dc link and the power dissipated in the tank circuit can be equated as shown in Eqn. 3.1.

$$V_D I_D = V_{LT} I_L \quad (3.1)$$

Where V_D and I_D are the voltage and current in the dc link. V_{LT} is the voltage across the workcoil and I_L is the current passed through the tank circuit.

The current passed through the tank circuit is a rectangular wave. The Fourier components of a rectangular wave are derived in Appendix 1. Since the Q of the tank circuit will be typically greater than 10 it is reasonable to neglect harmonics of I_L higher than the fundamental and to assume that the tank circuit voltage is a perfect sinewave. The deadband is assumed negligible. Substituting for I_L in Eqn. 3.1 gives the relationship between V_D and V_T shown in Eqn. 3.2.

$$V_D = 0.9 V_T \quad (3.2)$$

The peak voltage across the tank circuit will equal the peak voltage across MOSFETs therefore the peak voltage across a MOSFET is $\sqrt{2} \cdot V_D/0.9 = 1.56V_D$.

The impedance at resonance of a two element parallel resonant circuit (Z_D) is given in Eqn. 3.3.

$$Z_D = \frac{Q}{\omega C} \quad (3.3)$$

If the overlap period in the switching sequence when all the switches are on is assumed to be negligible and only the fundamental component of the rectangular current waveform passed through the tank circuit is considered then the dc link current (I_D) is given by Eqn. 3.4.

$$I_D = \frac{V_T}{0.9.Z_D} \quad (3.4)$$

The unit can be split into four stages; a fully controlled rectification bridge, a dc link, an inverting bridge and a tank circuit.

- (a) A three phase supply at the input to the unit was rectified by a fully controlled 6 pulse bridge. A block diagram of the rectification timing circuitry is shown in Fig. 3.4. The required thyristor firing delay angle was implemented by an 8 bit word which was set up on the front panel using switches. The crossing of the red and blue phases was detected by the circuit in Fig. 3.5. This used a 741 Op Amp as a comparator with hysteresis provided by R_1 and R_2 to reduce the risk of oscillation on the output caused by noise. The phase crossing detect level was converted to a phase crossing detect pulse. This pulse loaded the counter with the 8 bit delay word. When the pulse had fallen to zero the counter counted the cycles of a 10 kHz clock. Six 8-input NAND gates decoded counts corresponding to the delays of the six thyristors in the rectification bridge. These signals were then lengthened using monostables, combined with a clock and fed to pulse amplification circuits which triggered the thyristors via pulse transformers.

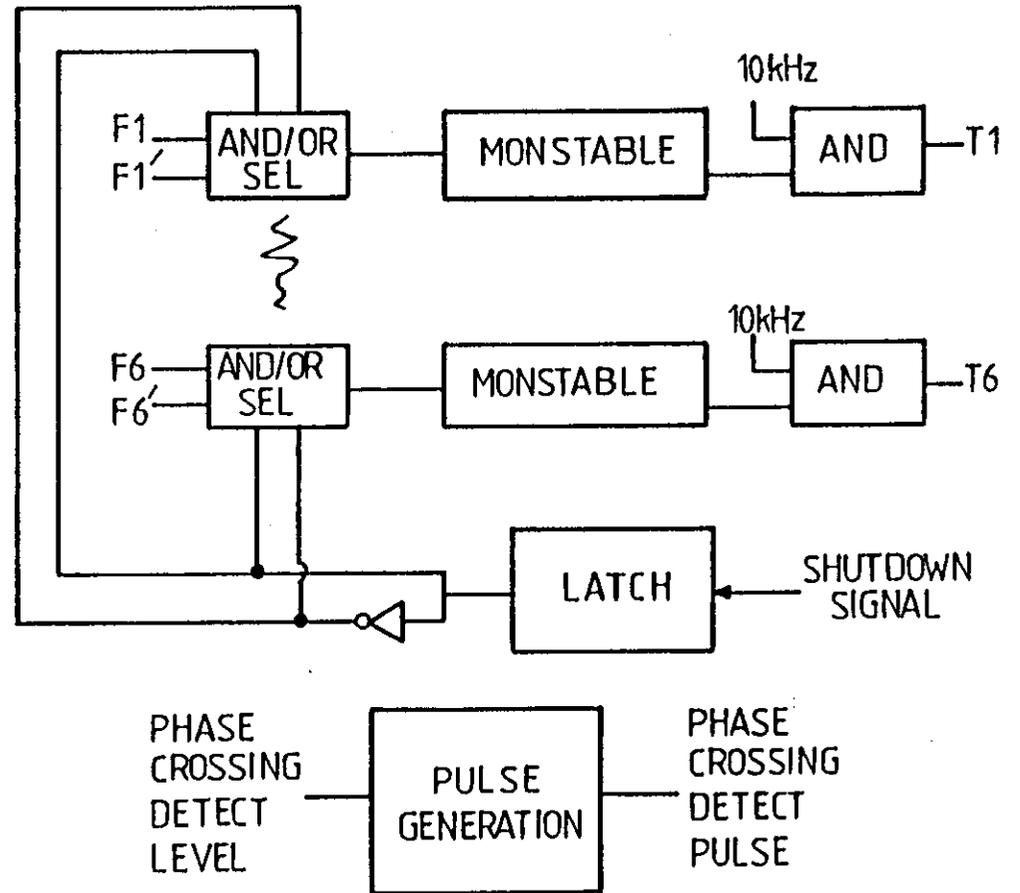
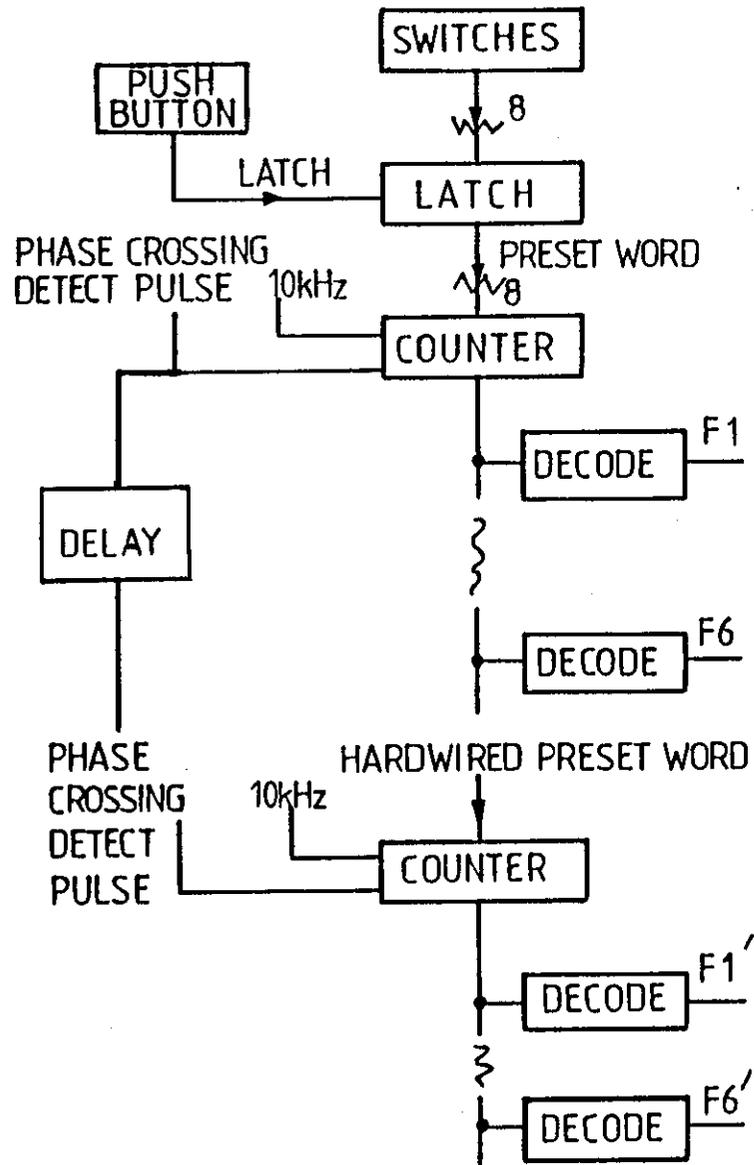


Figure 3.4 - A block diagram of the rectification timing circuitry for the current fed prototype.

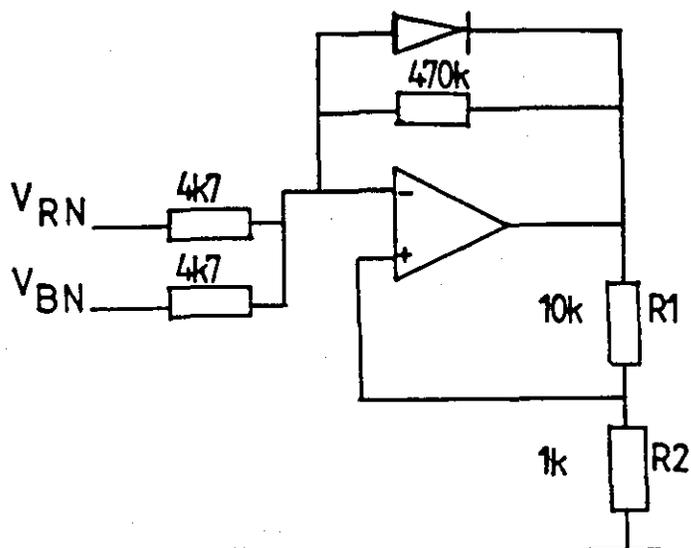


Figure 3.5 - The phase crossing detection circuit.

The maximum delay angle with this circuit was 60° . When an 8 bit word corresponding to a delay greater than 60° was loaded into the counter the counter was reloaded 20 ms later which was before the output of the sixth 8-input NAND gate had gone low. A delay angle greater than 90° was required so that under conditions of severe overcurrent the rectification bridge could be phased back into inversion. The energy could then be drawn out of the choke and the unit shutdown. If a contactor was opened before the energy has been drawn out of the choke a voltage spike would be produced which would damage MOSFETs. To achieve a delay angle greater than 60° the phase crossing detect pulse was delayed by 6.0 ms. This delayed pulse was used to load another counter with a hard-wired delay word corresponding to a delay angle of 170° . 8-input NAND gates were used to time out delays and so another 6 thyristor signals were generated.

The selection of the thyristor firing signals corresponding to a normal working delay angle or a shutdown delay was achieved by logic inserted between the NAND gates and the monostables as shown in Fig. 3.4.

- (b) Two air-cored chokes were constructed from 16 Standard Wire Gauge (SWG) enamelled copper wire which had inductances of 5 mH. These were connected in the dc link. With an input line voltage of 100V these chokes restrained the maximum change in dc link current (I_D) under short circuit conditions to 67A (Appendix 2)*.
- (c) The inverting bridge was a full bridge with two MOSFETs, type IRF450, in each leg.

A block diagram of the drive circuitry used is shown in Fig. 3.6. A minimum overlap period of 200 ns was provided. The overlap period when all MOSFETs were on was needed to prevent the choke being open circuited. An opto-isolator type HCPL 2607 was used for isolation of the drive signal. Like many fast opto-isolators the HCPL 2607 has a maximum supply rail of 5V so level shifting was needed to produce a 15V gate drive signal for the MOSFETs. Since the drive power requirements of MOSFETs are so low the creation of 15V and 4.7V supply rails was done using zener diodes without problems of rails being overloaded. Fig. 3.7 shows the final two stages of current amplification in the MOSFET drive circuit. The six paralleled CMOS inverting buffers shown in Fig. 3.7 provided current amplification to drive the push-pull transistors Q_1 and Q_2 via base resistor R_1 in parallel with the speed-up capacitor C_S . A diode was connected in parallel with the external gate resistor (R_{DR}) to reduce the turn-off time of the MOSFETs. Another resistor was placed in the gate connection to each paralleled MOSFET to prevent parasitic oscillations as described in Section 2.2.4.4. The sources of paralleled MOSFETs were connected by both power connections and also through the isolated zero volt line of the drive circuitry creating a low impedance loop. Flux associated with currents carried by MOSFETs linked with this loop and caused large currents to flow in the loop. This did not cause any problems as regards circuit function but it made measurements on

* The reader is referred to Appendix 2.

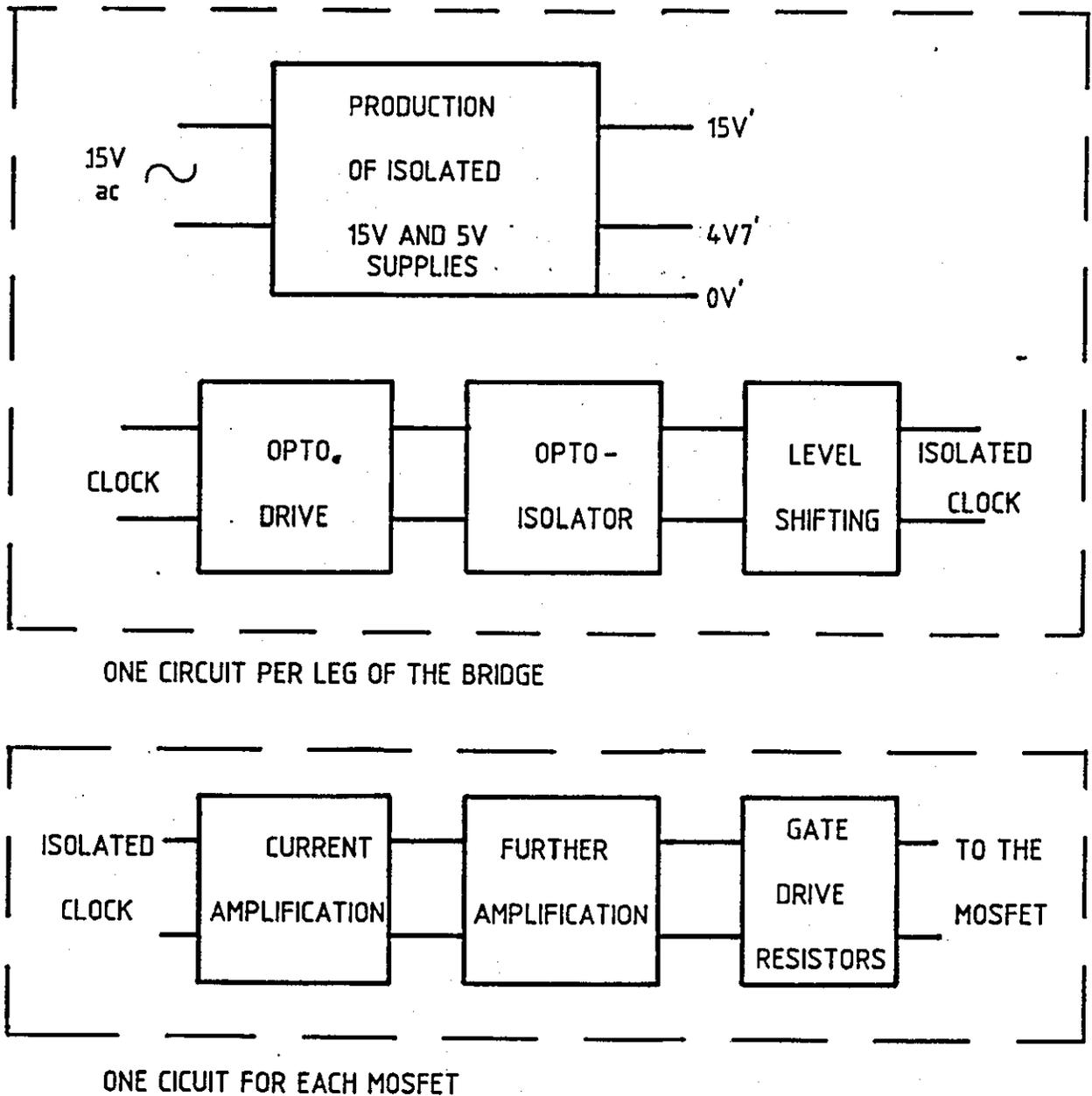


Figure 3.6 - A block diagram of the MOSFET gate drive circuitry.

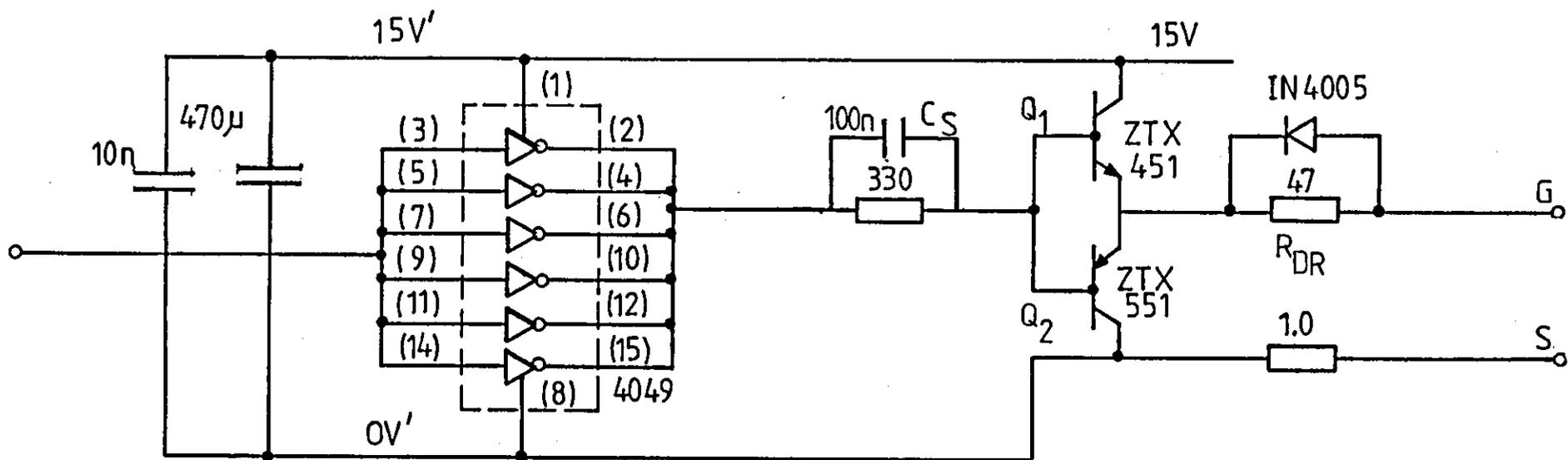


Figure 3.7 - The two stages of current amplification in the MOSFET drive circuit.

gate drive current difficult so a $1\ \Omega$ resistor was placed in the source connection from the drive circuit to prevent the loop current.

- (d) A current transformer was constructed of 25 turns of 25 SWG enamelled copper wire wound on a ferrite ring core type MM623/20/P. One of the connections from the bridge to the tank circuit was fed through the ferrite ring once. The secondary of the current transformer was connected to the overcurrent detection circuit shown in Fig. 3.8. A burden resistor of $10\ \Omega$ was used so that a primary current of 1 Amp would produce a voltage across the burden resistor of 0.4V. IC1 in Fig. 3.8 was an operational amplifier connected in the emitter follower configuration to buffer the voltage across the burden resistor. IC2 acted as a comparator and IC3 had 15V clocked through from its data input to its output when an overcurrent was sensed. The latched overcurrent signal was fed to the rectification timing circuitry to invert the dc link voltage.

The unit was supplied through a variac and turned on at low power. Resonance was found by varying the switching frequency of the inverting bridge until there was a minimum of link current (I_D).

A tank circuit capacitor of 50 nF in parallel with an unloaded workcoil with an inductance of $8.1\ \mu\text{H}$ and a Q of 24 was fed at 250 kHz with a dc link voltage of 28V. Waveforms of voltage and current are shown in Fig. 3.9.

The following advantages were apparent in the design and operation of the prototype.

- (a) The workcoil was short circuited many times and the unit shut itself down safely on all occasions.

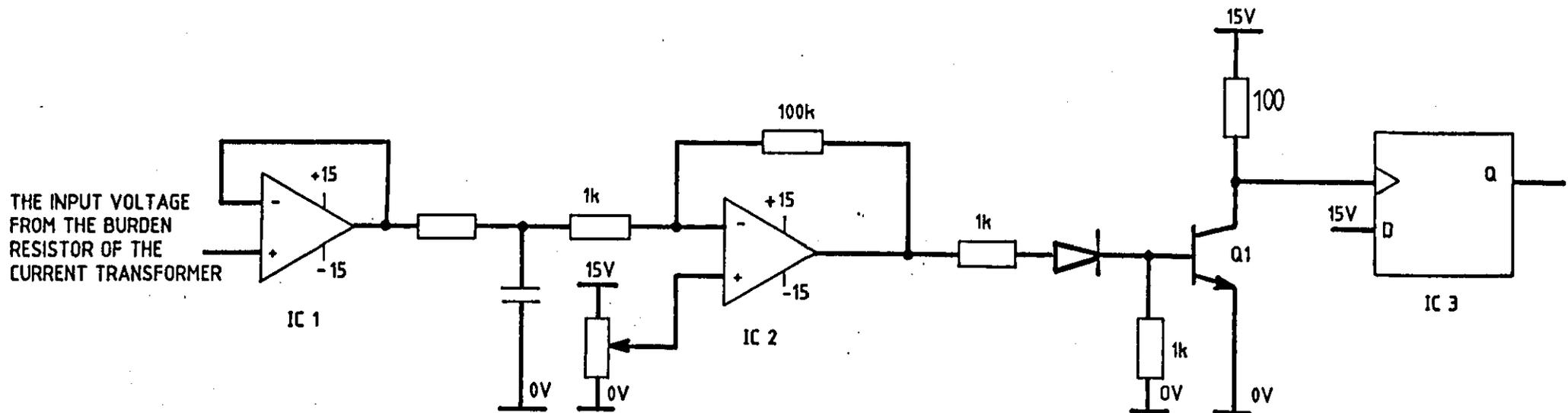


Figure 3.8 - The overcurrent detection circuit used on the current fed prototypes.

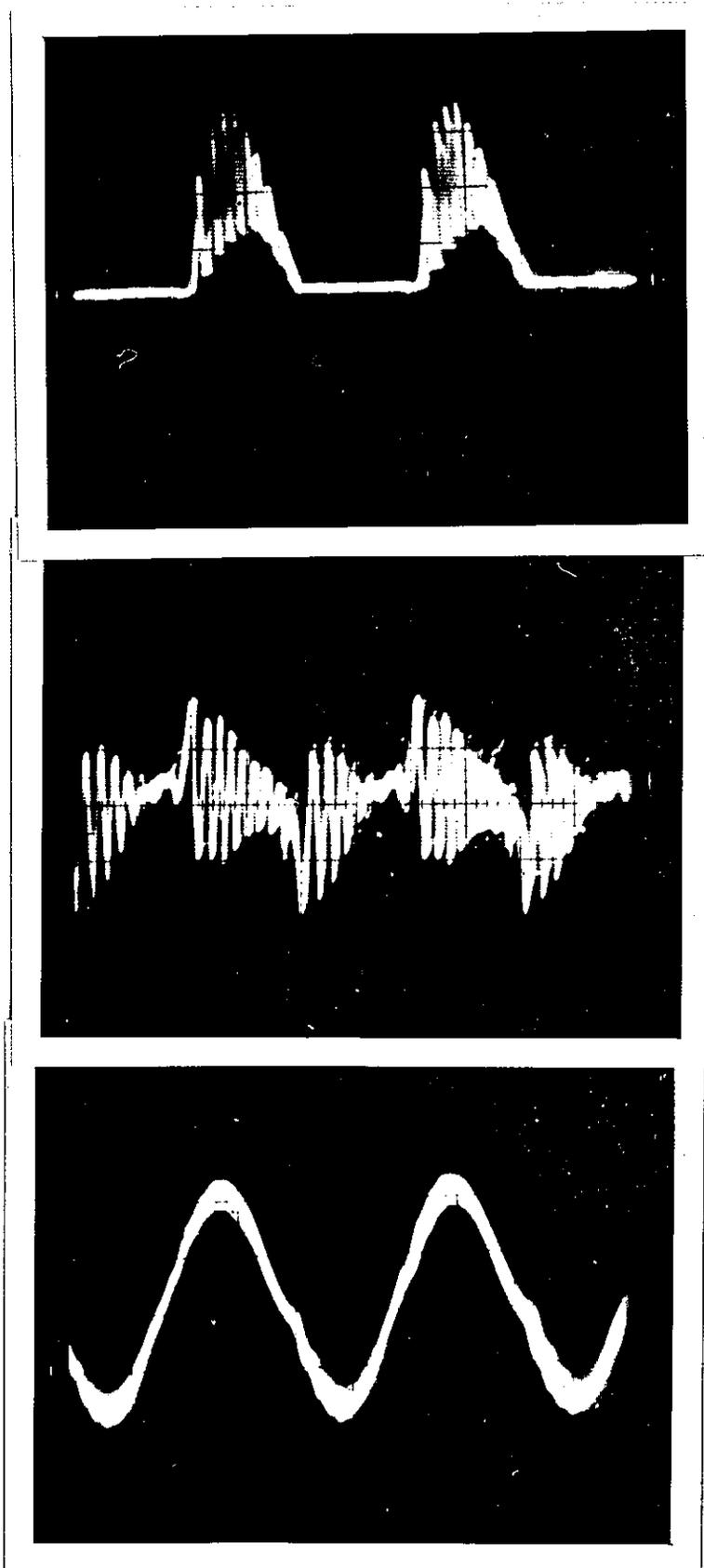


Figure 3.9 - Waveforms of (a) the voltage across the drain to source of a MOSFET (20 V/div, 1 μ s/div) and (b) the drain current of a MOSFET (0.1A/div, 1 μ s/div) and (c) the voltage across the tank circuit (20 V/div, 1 μ s/div) prototype fed into a workcoil.

- (b) The overlap time of MOSFET conduction was found from the drain source voltage waveforms. This period was greater than the overlap time present at the output of the driver transistors Q_1 and Q_2 in Fig. 3.7. Therefore the MOSFET turn-off time being longer than the turn-on time could be relied on to produce overlap of MOSFET conduction. This simplified the MOSFET drive circuitry.
- (c) When a workpiece was suddenly removed from the workcoil no excessive spikes were present on the drain source voltages of MOSFET.
- (d) No problems of interference with shutdown signals were encountered since fast turn-off of currents took place only in the inverting bridge and this could be placed away from sensitive control signals.
- (e) Spurious turn-on of MOSFETs did not cause problems. If the MOSFETs in both upper and lower limbs of the same pole were on together a shoot-through would not occur because the choke would restrain the rise in MOSFET current.
- (f) The design and layout of the gate drive circuitry was not as critical as in the case of the voltage fed inverter. When a MOSFET was turned off its drain to source voltage was a half sinewave. The peak charging current for the gate to drain capacitance was not as large as if its drain to source voltage was a rectangular wave. The danger of dv/dt turn-on described in Section 2.2.4.5 was therefore reduced.
- (g) No problems were encountered with matching the impedance of the tank circuit (Z_D) to the voltage and current ratings of the unit. When the unit fed a poorly coupled workcoil doubling the workcoil inductance and halving the tank circuit capacitance increased Z_D by nearly three times so Z_D could easily be varied.

(h) From the waveforms in Fig. 3.9 it can be seen that the peak of the fundamental component of the tank circuit voltage was about 40V which agreed with Eqn. 3.2. The current in the dc link was 0.1A.

3.4 CONCLUSIONS

The voltage fed inverter and the cycloinverter were very difficult to shut down speedily enough to protect MOSFETs when the output was short circuited. This is very important in an induction heating supply since the workcoil is very likely to be short circuited. The speed of detection of overcurrent could have been improved further by using a faster operational amplifier but the rise of current would still be unrestrained during the prearcing time of the semiconductor fuse. This can be as long as 1 ms.

The current fed inverter was able to cope more easily because of the slower rate of rise of current in the dc link.

The voltage fed inverter feeds into a series resonant tank circuit which has a small impedance at resonance. Therefore very large currents have to be switched by the MOSFETs or a matching transformer needs to be used. The use of a matching transformer increases the cost of the unit and switching larger currents worsens the problem of interference.

The commutating of large currents from one path to another caused interference. This was more of a problem with a voltage fed circuit since current direction in leads near the crowbar protection circuit changed rapidly when the tank circuit was fed off resonance. This caused interference with sensitive protection circuitry and switching larger currents would make this worse. Any filtering to reduce the sensitivity of the protection circuitry would reduce its response time. The current fed inverter had a big advantage here because protection circuitry was placed remote from the area of fast current switching which occurred solely around the inverting bridge.

The drive circuitry for the current fed inverter was a lot simpler because the necessary overlap period in the MOSFET switching sequence was provided by the slower turn-off time of MOSFETs. Problems of spurious turn-on caused by the gate drive circuit not having a small enough drive impedance when the MOSFETs were off were reduced in the current fed inverter. This also simplified the design and layout of the gate drive circuitry.

The current fed inverter and voltage fed inverter are not strictly duals in every way (Kassakian 1982, Kassakian et al 1982). When the load was suddenly removed the impedance of the tank circuit of the current fed inverter increased suddenly. This caused a transient voltage across MOSFETs. The same event however caused a steady state overcurrent in MOSFETs in the voltage fed inverter and so is harder to deal with.

To feed a typical impedance at resonance of a series resonant tank circuit which is less than 1Ω with 20 kW will need a current of more than 140 A to be passed through it. A large number of expensive capacitors would have to be paralleled to produce capacitor C_{RFBC} in the voltage fed inverter in Fig. 2.3. C_{RFBC} would have to have a ripple current rating as high as 70A at 800 kHz for operation of the bridge at 400 kHz. Selection of capacitors for C_{RFBC} would be difficult.

Frequencies in the range 100 to 400 kHz are often used to heat a small workpiece such as a pin or an aluminium shim which is very poorly coupled to the workcoil. It was a lot easier to match the current fed inverter into these poorly coupled workcoils since any variations in the number of turns in the workcoil and the tank circuit capacitance had about twice the effect on Z_D than on the impedance at resonance of a series resonant circuit.

For these reasons the current fed inverter was chosen as the best topology for induction heating between 100 to 400 kHz for power levels up to 20 kW.

CHAPTER 4THE CURRENT FED PROTOTYPE

A high power current fed prototype was designed and constructed with a power output of 5 kW. A novel form of matching using a modified tank circuit was used to suppress ringing on the drain to source voltage of MOSFETs. The performance of this unit feeding induction heating workcoils of commercial significance was then investigated.

4. THE CURRENT FED PROTOTYPE

The aim of the work was to investigate the design of power supplies that could be scaled up to 20 kW. The sponsoring company wanted to assess the performance of the unit when feeding commercially significant workcoils. Two coils that Stanelco Products plc were particularly interested in were a cap sealing workcoil and a vapour deposition workcoil. A prototype inverter with higher power output than the one described in Section 3.3 was designed and constructed to feed the required power into the two industrial workcoils and to gain experience operating at higher power levels. (Tebb et al 1985b, 1986g).

The causes of ringing on the drain to source voltage waveform of MOSFETs as seen in Fig. 3.9 were examined. The use of a novel matching technique was looked at theoretically and experimentally. This matching technique was assessed.

4.1 THE DESIGN, CONSTRUCTION AND TESTING OF THE PROTOTYPE CURRENT FED INVERTER

In a current fed inverter energy is stored in a dc link by a large choke. This choke smoothes the direct current in the link (I_D) so that switching of the MOSFETs in the inverting bridge causes a rectangular wave of current to be fed to the load.

The current fed inverter has many advantages for induction heating particularly the inherent short circuit protection provided by the choke in the dc link.

4.1.1 The Input Transformer

A step down transformer was used at the input to the unit. This reduced the dc link voltage so that the voltage across the tank circuit was within the ratings of MOSFETs with relatively low on-resistance. A variac was used in the laboratory since it enabled initial testing of the unit to be done at low power levels. In industry an isolating transformer would be preferable since the workcoil could then be earthed for safety reasons.

4.1.2 The Rectification Stage

A fully controlled six pulse rectification bridge was used to vary the voltage to the dc link (V_D) and so provide a means of power control.

The maximum rms line voltage at the input to the rectification bridge was designed to be 200V and the repetitive forward blocking voltage of the thyristors was 800V. This safety margin prevented destruction of thyristors by mainsborne voltage spikes. The average current rating of the devices was 26A so the maximum power output of the bridge was about 20 kW. The rectification bridge therefore had sufficient power handling capability for any future prototypes up to 20 kW. The devices were each mounted on 2°C/W heatsinks.

Resistor capacitor snubbers were connected across the anode and cathode terminals to protect against transients on the supply. The capacitor was a film polypropylene capacitor of value 0.1 μ F. The snubber capacitor was chosen for its good high frequency performance since the voltage across a thyristor changes speedily in normal operation and in the presence of mainsborne spikes. The snubber resistor was a low inductance carbon granule type, value 47 Ω . The thyristors were protected by 1000V, 20A semiconductor fuses since the designed output power of the prototype was 5 kW.

The timing circuitry for the firing of thyristors in the rectification bridge was the same as described in Section 3.3.

4.1.3 The DC Link

The purpose of the choke in a current fed inverter is twofold. Firstly it stores energy which it passes onto the tank circuit every half cycle of the inverter switching frequency. If the inverter attempted to draw energy from the supply at twice the switching frequency the distortion of the supply voltage would be enormous. Secondly, if the output of the inverter is short circuited the choke has to restrain the rate of rise of current until the thyristor bridge is phased back into inversion. The second of these requirements is the most demanding and so the value of the choke was chosen so that the unit could be safely shutdown when

it was short circuited.

An air-cored choke was used because it overcame the problems associated with using a high permeability core and it made design more straightforward. The disadvantage of the air-cored choke was that it was heavier and more bulky.

There are two problems with using a high permeability core. Firstly the core has to sustain a voltage whose fundamental frequency is at twice the switching frequency. This will mean sustaining a voltage of typically 100V at a fundamental frequency of 800 kHz. This causes large hysteresis and eddy current losses in the core. Operating at 800 kHz causes overheating in silicon-steel or nickel-steel laminations and powder-iron cores. Ferrite cores are the most suitable but they are expensive and their permeability varies greatly with temperature (Snelling 1982).

Secondly the direct current in the link could saturate the core. A gap in the core overcomes this saturation problem. (Hanna 1927, Thomas 1980). It should be remembered in the design of the choke that when the output of the inverter is short circuited the current in the choke will increase by a large value.

A Direct Current Current Transformer (DCCT) type 50-P0 was used to measure the current in the link. This provided the advantages of isolation between power circuitry and control circuitry and had a negligible effect on efficiency. The circuit diagram of a two core DCCT is shown in Fig. 4.1. Both toroidal cores are saturated by the primary current. When the excitation voltage increases the current through the secondary windings of the toroidal cores increases causing one of the cores to be brought out of saturation and the other to be taken further into saturation. The winding on the core that has been brought out of saturation becomes high impedance and the secondary current stays nearly the same if the primary current is unchanged. The secondary current is monitored by measuring the voltage across the burden resistor (R_b) in Fig. 4.1. The secondary current is related to the primary current by

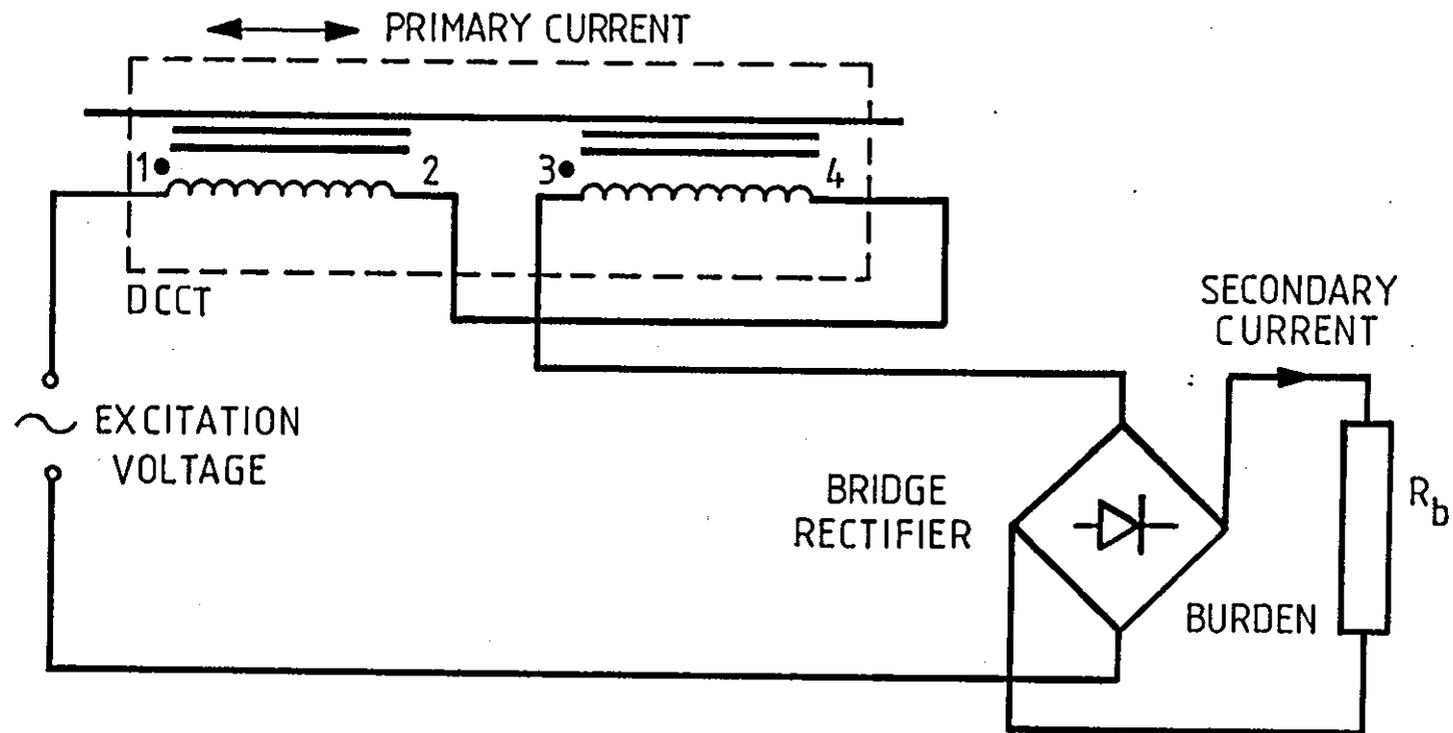


Figure 4.1 - The circuit diagram of a two core Direct Current Current Transformer (DCCT).

the ratio of the number of turns in the primary and secondary windings so the voltage across R_b is proportional to the primary current. Variations in the primary current cause proportionally similar variations in the secondary current. A three core DCCT was used which has a faster response. Typically there is a delay time of $5 \mu\text{s}$ and a rise time of $15 \mu\text{s}$ when there is a step rise in current of 50A in the primary (Edwards 1984). The secondary winding of the third core is connected between the bridge rectifier and the burden resistor. The primary winding carries the current to be measured.

4.1.4 The Inversion Stage

4.1.4.1 The Choice of Inversion Bridge Topology

The choices of configuration for the switches in the inversion stage fall into four categories; the single switch circuit, the push-pull circuit, the half bridge circuit and the full bridge circuit.

(a) The single switch circuit.

One circuit with a single switch is shown in Fig. 4.2(a). The waveforms associated with this circuit are shown in Fig. 4.2(b). This circuit is the dual of a voltage fed circuit which is often used for induction cooking (Sakoguchi et al 1983, Tebb et al 1985d, 1986d). The switch S in Fig. 4.2(a) is open between times t_1 and t_2 when the link current (I_D) flows into capacitor C_T . The switch S is closed at t_2 causing capacitor C_T and the workcoil L_T to resonate. The voltage across C_T then reverses. When the current in L_T tries to reverse it is prevented from doing so by the diode.

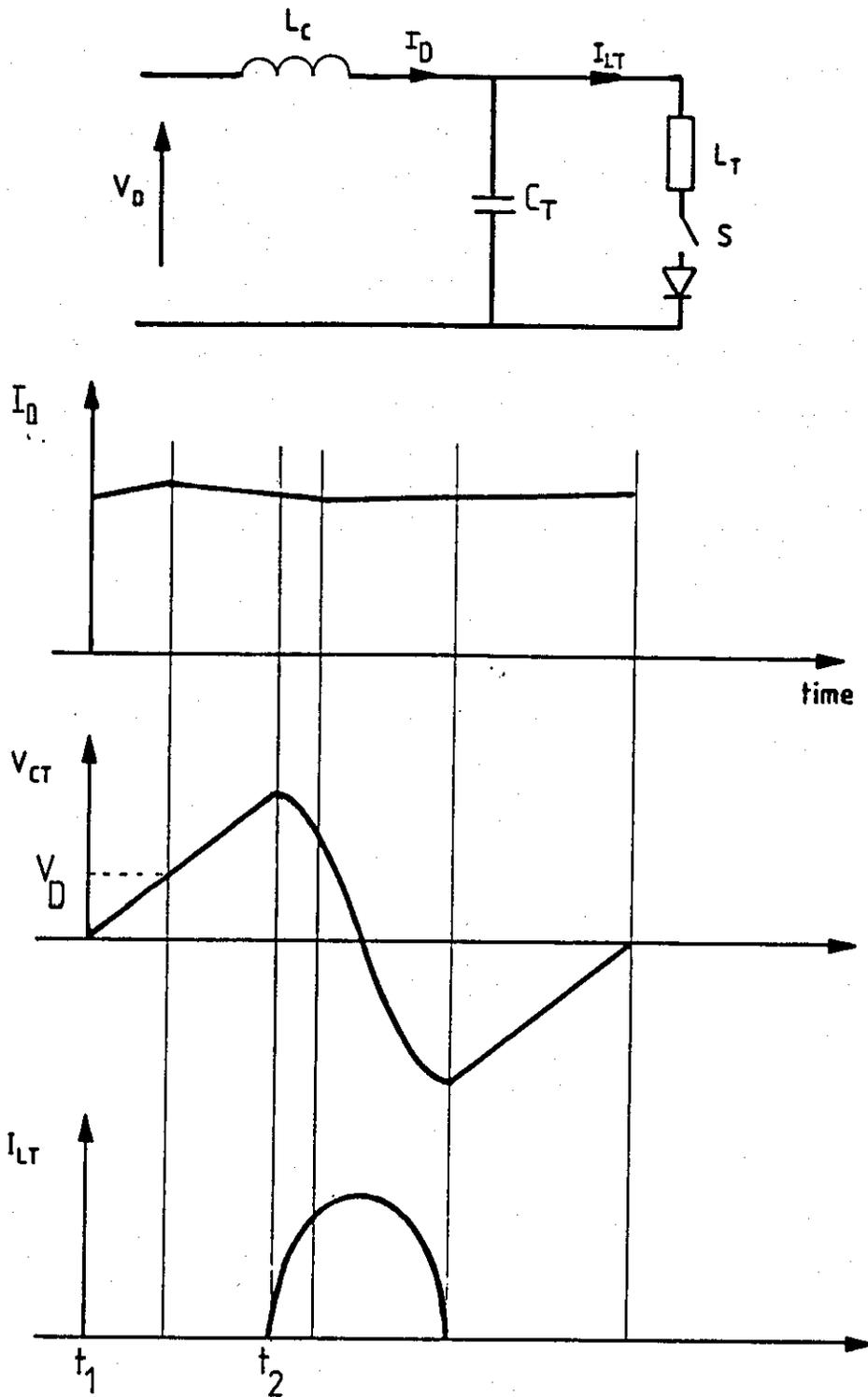


Figure 4.2(a) - An inversion stage topology involving a single switch.

(b) - The waveforms associated with the single switch topology in Fig. 4.2(a).

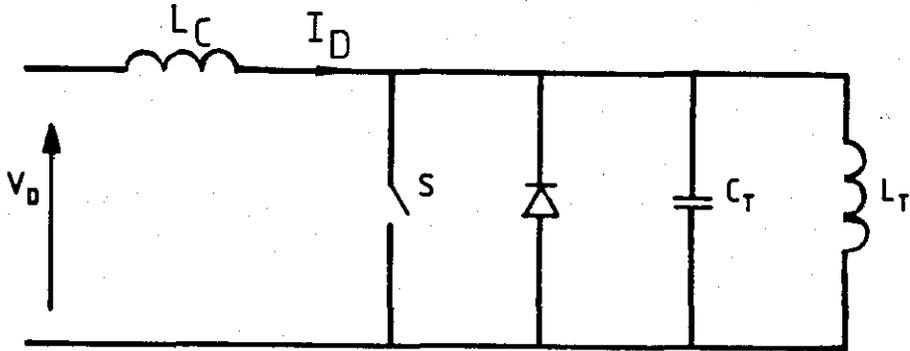


Figure 4.3 - A second example of an inversion stage topology including a single switch

Another circuit which has only one switch is shown in Fig. 4.3. When the switch is open the current in the choke (I_D) flows into the parallel resonant tank circuit. The current I_D reduces slightly during this time. When the switch is closed the voltage across the tank circuit is clamped so the current in L_T cannot flow into C_T . The switch therefore carries a current which is the sum of I_D and the current in L_T . The current in L_T is the circulating current which can be many times greater than I_D . A diode is therefore connected in parallel with the switch so that the switch does not have to be rated for this large current.

Both of these single switch configurations have the big disadvantages that semiconductor switches have to have a kVA switching capability approximately $\sqrt{2} \cdot Q$ times the power output of the unit. Loaded Q values are rarely below 10 for induction heating applications between 100 and 400 kHz so the cost of the unit will be much increased. The circuit in Fig. 4.2(a) does not protect the switch from overcurrent if the workcoil

is short circuited.

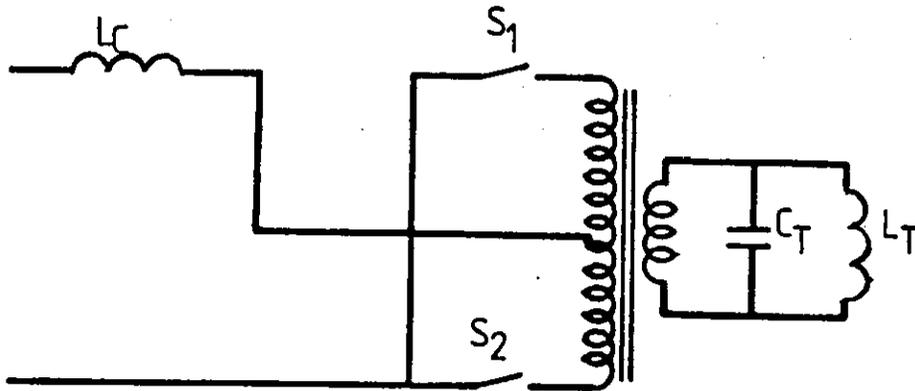


Figure 4.4 - The push-pull circuit

(b) The push-pull circuit.

The push-pull circuit is shown in Fig. 4.4. It has two switches. The switching sequence is as follows. Firstly S_1 is closed. Next there is an overlap period when both S_1 and S_2 are on to prevent the choke being open circuited. Finally just S_2 is closed. The push-pull configuration requires a transformer. This is an expensive component which also degrades the efficiency of the unit. Designing a transformer to work at 20 kW and 400 kHz requires an expensive core material such as ferrite and very careful attention to winding to reduce leakage inductance. The core will have to be cooled since hysteresis losses will be substantial.

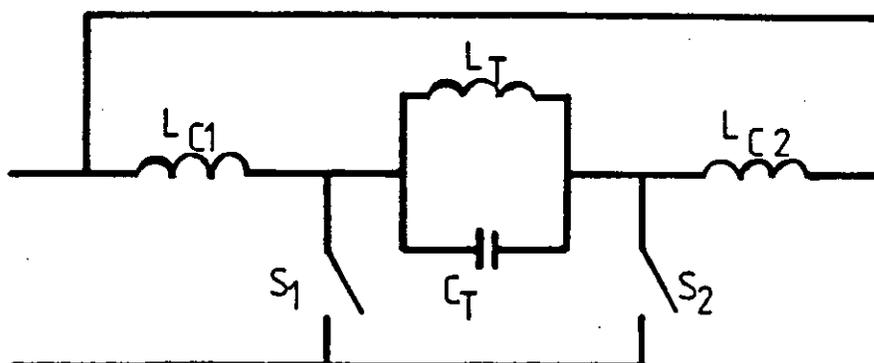


Figure 4.5 - The half bridge circuit

(c) The half bridge circuit.

As can be seen in Fig. 4.5 the half bridge circuit has two switches and two chokes. The choke is one of the bulkiest and heaviest components in the inverter if it is air-cored or one of the most expensive it has a high permeability core. The big disadvantage of the half bridge circuit is that, by having two chokes, it has doubled the requirement for the bulkiest or the most expensive item.

(d) The full bridge circuit.

In this circuit the switches need not handle any reactive power, it can be used without a high frequency transformer and it only has one choke. Therefore a full bridge inverter was used.

4.1.4.2 The Layout of the Inversion Bridge

In a switching power supply operating above 100 kHz using MOSFETs the layout of the circuit is of prime importance.

For the reasons described in Section 2.2.4.4 it is recommended that paralleled MOSFETs are mounted wherever possible on the same heatsink to provide good thermal coupling between them. There were four MOSFETs, type IRF450, in each leg of the full bridge which were mounted on two 1.2°C/W heatsinks; 2 MOSFETs on each heatsink. The two heatsinks were mounted so that they were touching as can be seen in the photograph of the inverting bridge in Fig. 4.6.

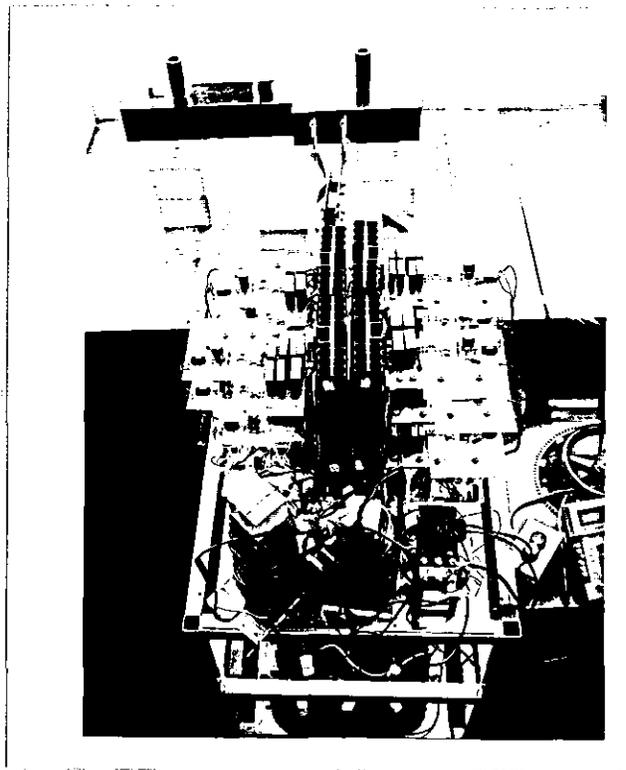


Figure 4.6 - The higher power current fed prototype inverter

Since MOSFETs are capable of switching off very speedily voltage spikes can be caused in parasitic lead inductance. This can cause ringing between parasitic lead inductance and the drain source capacitance of MOSFETs which is a big problem in switching power supplies operating above 100 kHz.

To reduce the problem of ringing the parasitic lead inductances need to be kept to a minimum. This involves keeping the length of connecting leads as short as possible and reducing the area of loops with which the flux linkage will change rapidly. Inspection of the schematic diagram of the current fed full bridge inverter in Fig. 2.1 reveals two loops that need to be kept small. The first of these is contained in the path from the input connection of the link current to the inversion bridge, through S1, the tank circuit, S2, to the return connection of the link current and back to the input connection of the link current. The second loop is similar to the first except that S1 and S2 are replaced by S3 and S4. To reduce the area of these loops the layout of the inversion bridge as shown in Fig. 4.7 was used. The leads connecting S1 and S2 to the tank circuit and also to the dc link were twisted together to reduce the inductance of these connections. Similar connections for S3 and S4 were also twisted. The connections from each MOSFET to the dc link and the tank circuit were made using a separate cable. This improved the symmetry of the connections to each paralleled MOSFET and so the current sharing between the MOSFETs was improved. This was because the impedances of the leads to each MOSFET were very similar and so the adverse effect of differing MOSFET parameters on current sharing was reduced.

The drive circuits were placed within 50mm of the MOSFETs and connections to the gate and source terminals were twisted. These precautions reduced the gate drive impedance so that fast switching times and low switching losses could be achieved.

4.1.4.3 The Heatsink Requirements

The transistors were mounted on heatsinks to prevent the MOSFET dies from reaching a temperature high enough to degrade the silicon.

A major advantage of the current fed inverter is that switching takes place when the voltage sustained by MOSFETs is ideally zero. This means that switching losses are very small and so they can be neglected. The conduction losses were calculated from Eqn. 2.1. Since the MOSFETs were derated by 20% for improved reliability the rms drain current was

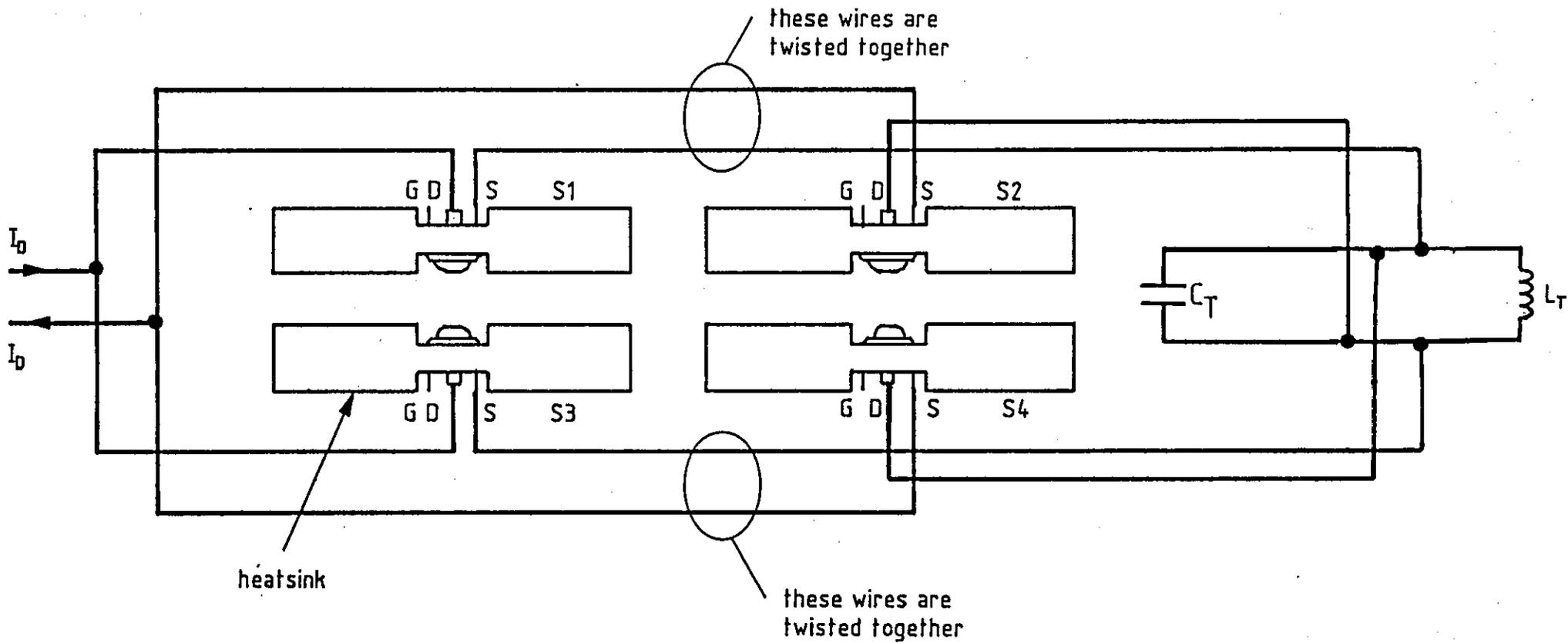


Figure 4.7 - A schematic diagram of the layout of the inversion bridge.

6A at a junction temperature of 100°C. The on-resistance of the IRF450 is typically 0.5 Ω at a junction temperature of 100°C. The conduction losses were calculated as 18W. Since the tank circuit is fed at resonance the parasitic diode does not carry reactive current and so power dissipation in the MOSFETs originating from the parasitic diode is negligible. The gate charge in the IRF450 for a gate to source voltage of 15V is 112nC (International Rectifier 1985). The gate power dissipation at 400 kHz was calculated from Eqn. 2.3 to be less than 0.7W.

The heat flow equation for heat transmitted between the MOSFET junction and the ambient is given in Eqn. 4.1.

$$T_J - T_A = P_D (R_{J-C} + R_{C-S} + R_H) \quad (4.1)$$

where T_J is the junction temperature (°C)

T_A is the ambient temperature (°C)

P_D is the power dissipated in the MOSFET (W)

R_{J-C} is the thermal resistance between the junction and the case of the MOSFET (°C/W)

R_{C-S} is the thermal resistance between the case of the MOSFET and the heatsink (°C/W)

R_H is the thermal resistance of the heatsink (°C/W).

An ambient temperature of 30°C was assumed. The required heatsink thermal resistance was 3.0°C/W. Two MOSFETs were mounted on a 1.1°C/W heatsink since this heatsink was the closest readily available size.

4.1.4.4 The MOSFET Drive Circuitry

The gate drive power requirements for MOSFETs are very low. The danger of dV/dt turn-on caused by the gate drive circuit having too large an impedance when the MOSFET is off is reduced in a current fed inverter (see Section 3.3). These two factors simplify the design of the gate drive circuitry. The same circuits which were described in Section 3.3 were used. The final stages of the drive circuit i.e. the paralleled CMOS inverters and the push-pull transistors were duplicated so that

each MOSFET was driven by a separate pair of push-pull transistors. These CMOS inverters and push-pull transistors were mounted on separate PCBs which were mounted very close to the terminals of the MOSFETs. The supply rails on these PCBs were decoupled by a combination of electrolytic and ceramic capacitors. This meant that the connections from the gate drive circuits to the MOSFETs were short and so the impedance of these connections was small. The connecting leads between the drive circuits and the MOSFETs were twisted to keep their impedance as low as possible. The low impedance of the gate drive connections meant that switching times were faster and dV/dt turn-on was unlikely. Since the push-pull transistors driving each MOSFET were the same distance away from their respective MOSFETs the spread in switching times of paralleled MOSFETs was reduced. This improved dynamic current sharing. Any problems of parasitic oscillations between paralleled MOSFETs (Kassakian 1983) were also overcome by using separate push-pull transistors for each MOSFET. A gate drive voltage as high as 15V was used for the reasons given in Section 2.2.4.3.

4.1.5 Experimentation

The unit was tested by feeding a simple two element tank circuit at 125 kHz. The waveforms are shown in Fig. 4.8. Fig. 4.8(a) shows the voltage at the output of the unit and the voltage across the drain to source of a MOSFET. Fig. 4.8(b) shows the voltage across the tank circuit. A comparison between Fig. 4.8(a) and Fig. 4.8(b) reveals that ringing is present mainly across parasitic lead inductance between the unit and the tank circuit and across the drain to source of MOSFETs. A reduction of the ringing on the MOSFETs' drain to source voltage waveform could increase the utilisation of the MOSFETs' switching capability. Methods of suppression of drain to source ringing were therefore investigated.

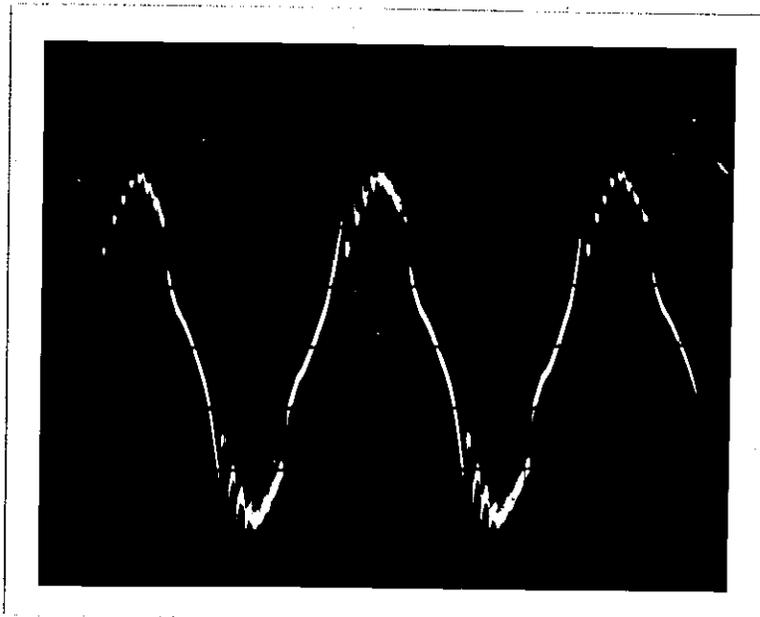
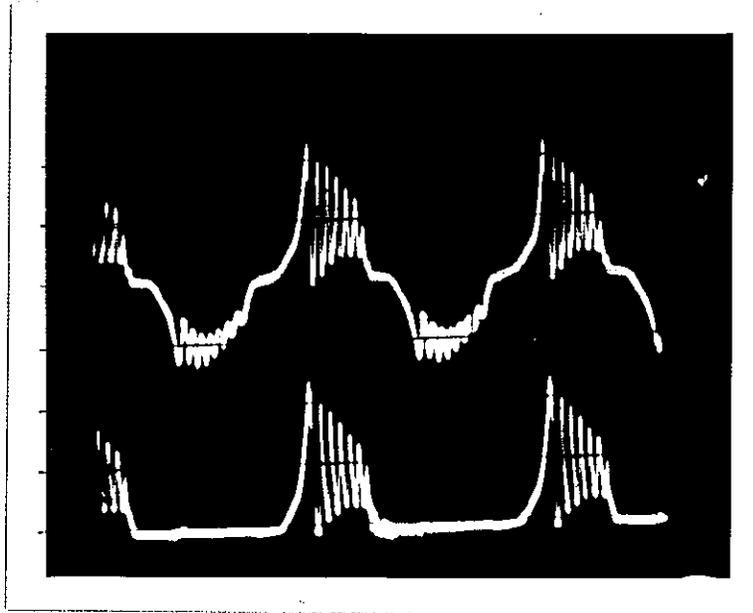


Figure 4.8 - Waveforms of (a) the voltage at the output terminals of the unit (20V/div, 2 μ s/div) and at the bottom the drain to source voltage across a MOSFET (20V/div, 2 μ s/div) and (b) the voltage across the tank circuit (10V/div, 2 μ s/div), when the current fed prototype was tested into an induction heating load.

4.2 THE SUPPRESSION OF RINGING

The ringing on the drain to source voltage of MOSFETs when they are switched off is a major problem with switching power supplies. MOSFETs have more problems with ringing because they switch off very speedily. The ringing on the drain to source voltage means that the power output capability of the supply is reduced.

In the preliminary investigations on the current fed inverter described in Section 3.3 it was mentioned that ringing was observed on the drain to source voltage waveforms of MOSFETs. This was because when MOSFETs were turned off energy stored in parasitic lead inductances was transferred to the drain source capacitance of the turning off MOSFETs by a ringing current. The path of the ringing current when the MOSFETs implementing S1 switched off is shown in Fig. 4.9. There is another possible path for ringing currents including switches in both the upper and lower halves of the inversion bridge and not the tank circuit. However, if the layout of the inversion bridge is symmetrical then the voltages generated in parasitic lead inductances will sum to zero round this loop.

In Section 4.2 possible methods of suppressing ringing are described. The use of a filter Z_f to block ringing currents and snubber capacitors to shunt ringing currents is developed. This method overcomes the disadvantages of the other methods. The effect of the filter and the snubber capacitors is analysed using Fourier Analysis. A novel method of matching is described which incorporates the principles of the filter and the snubber capacitors into an industrial induction heater; this is called the modified tank circuit. A design procedure for the components in the modified tank circuit is given. The suppression of ringing by the modified tank circuit is demonstrated experimentally. (Tebb et al 1986a).

4.2.1 Possible Methods of the Suppression of Ringing

The parasitic lead inductances of connecting leads between the dc link and MOSFETs and between MOSFETs and the output terminals of the supply were kept to a minimum as described in Section 4.1.4.2. In many

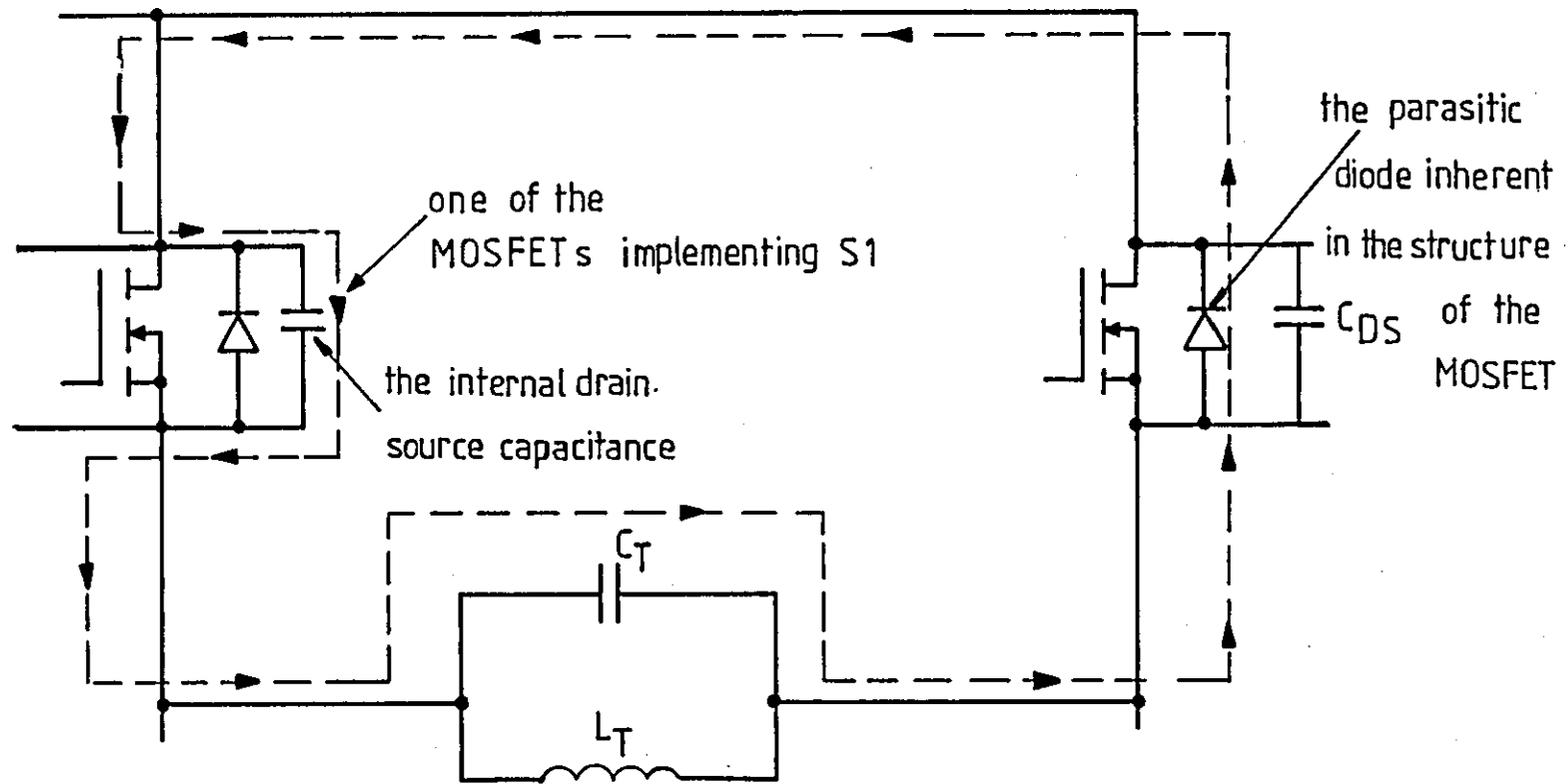


Figure 4.9 - The path of ringing currents when the MOSFETs implementing S1 switch off.

induction heating applications the tank circuit is remote from the supply. This means that the connections between the supply and the tank circuit will have appreciable inductance, typically $> 1 \mu\text{H}$. Therefore the problem of ringing cannot be solved by careful layout alone.

To reduce the voltage spikes across MOSFETs a resistor-capacitor snubber could be used. However the losses at 100 kHz are quite high, e.g. a capacitor of 10 nF in series with only a 1 Ω resistor will cause a power loss of 6.25 W. There are problems of extracting heat from the resistor and of mounting it so that it has short connecting leads and hence low inductance. In selecting a zener diode to clamp the voltage spikes the MOSFETs have to be derated for normal operation by the ratio of the clamping voltage at likely levels of ringing current to the reverse withstand voltage. This ratio is typically about 1.5. Zener clamping also suffers from practical problems of keeping lead lengths short as does the use of Molybdenum Oxide Varistors (Paul 1984).

4.2.2 The Use of a Filter and Snubber Capacitors to Suppress Ringing

If a snubber capacitor alone is used the value required to keep the resonant frequency of itself and typical parasitic lead inductance below the lowest harmonic frequency of the ringing current is very large. By inserting a filter (Z_F) in the path of the ringing current that looked inductive to high frequency harmonics of voltages generated in parasitic lead inductances the size of capacitance needed to be connected across the MOSFETs was reduced. This formed a method of suppression containing both series blocking by the filter connected in the branch containing the tank circuit and shunting by the capacitor. This method was essentially lossless provided that high Q components were used in the filter. The requirement of short lead lengths between the capacitor and the MOSFET was not difficult. The inductance of these leads needed to be small compared to other inductances in the path of the ringing currents. In the case of other methods of suppression this was just parasitic lead inductance but for the filter Z_F described above the lead inductance only needed to be small in comparison with the effective inductance of the filter.

The aim of Z_F was to sustain most of the voltage spikes itself so keeping the spikes away from the MOSFETs. Z_F needed to present a minimum impedance to the switching frequency and a maximum impedance to the higher frequency harmonics. If Z_F was to do this efficiently it had to contain no resistors and use high Q reactive components. A series resonant circuit would meet the above specification with its resonant frequency arranged to be near the switching frequency. The components in the series resonant circuit being C' and L' .

In the current fed inverter there may be different on times for switches caused by differing characteristics of drive circuit components, differing characteristics of the MOSFETs themselves, or slightly different lead lengths from the driver circuits to the MOSFETs. This would lead to a direct current component flowing and charging up C' until its breakdown voltage is exceeded. To overcome this an inductor, L'' , was connected in parallel with the series combination of $L'C'$, thus preventing a direct voltage appearing across C' . This precaution is a dual of that taken when a voltage fed inverter feeds a transformer and a capacitor is connected in series with the primary of the transformer to prevent a direct voltage causing saturation (Frank 1982).

The parallel connection of L'' meant that the effective impedance of Z_F above the series resonant frequency of C' and L' (Z_{eff}) was now given by Eqn. 4.2.

$$Z_{eff} = \frac{\omega L' L''}{L' + L''} = \omega L_{eff} \quad (4.2)$$

The impedance locus of Z_F in Fig. 4.10 shows that there was a parallel resonance at ω_1 and a series resonance at ω_2 .

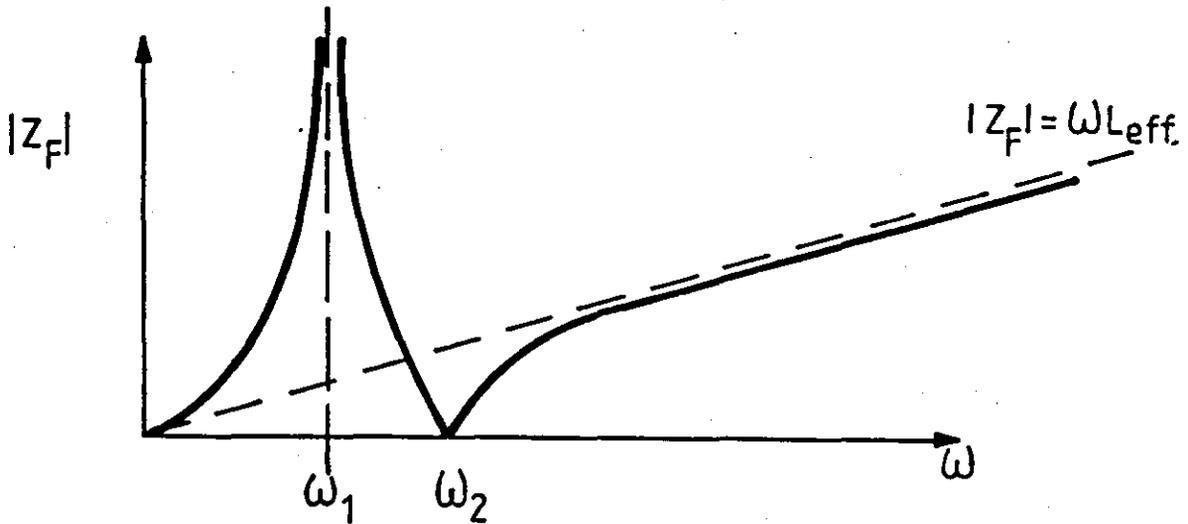


Figure 4.10 - The impedance locus of the filter Z_F

Since the load current was switched through Z_F and Z_F presented an inductance L_{eff} to high frequency harmonic components of this current a voltage spike was created by the presence of the filter, i.e. V_1 . The amplitudes of the harmonics of the current switched through L_{eff} were greater than those switched through most other parasitic lead inductances and L_{eff} was designed to be many times greater than the parasitic lead inductances. This meant that ringing on the MOSFETs caused by the spike created by switching the load current through Z_F was far greater than ringing caused by switching current through parasitic lead inductances. A small capacitance connected across the drain to source of MOSFETs overcame this problem. The internal drain source capacitance of a MOSFET was about 400pF and was small compared to externally connected drain source capacitance.

In essence therefore the matching circuitry was made up of a capacitor connected across the drain to source of each MOSFET together with a resonant circuit of L'' in parallel with a series combination of L' and C' connected in the same branch as the tank circuit and in series with it. Part of the inversion bridge, the filter Z_F and the snubber

capacitors are shown in Fig. 4.11.

4.2.3 A Fourier Analysis of the Effects of the Filter and Snubber Capacitors on the Operation of the Inversion Stage

The performance of the filter and snubber capacitors can be best understood by considering the harmonic components of the voltage generated by switching the load current through the filter Z_F ie. V_1 .

The voltage V_1 produced in Z_F was potentially divided across two circuit elements. The first element was L_{eff} and the second was the lumped capacitances. The capacitances were the tank circuit capacitance (C_T) in series with a parallel combination of eight of the externally connected drain source capacitances. When MOSFETs in two limbs of the bridge were turned on the drain source capacitances in the other limbs were in parallel with the series combination of Z_F and the tank circuit. Thus the total contribution of drain source capacitance was $8C_{DS}$ and the resonant frequency of L_{eff} with the capacitances ($f_{res} = \omega_{res}/2\pi$) was given by Eqn. 4.3.

$$f_{res} = \frac{1}{2\pi \sqrt{L_{eff} \cdot \left(\frac{8C_{DS} \cdot C_T}{8C_{DS} + C_T} \right)}} \quad (4.3)$$

The first harmonic of V_1 was attenuated by the tank circuit which was at the peak of its impedance locus at this frequency. Also Z_F was a low impedance to the switching frequency hence only the second and higher harmonics of I_L contributed appreciable effects to V_1 . A mathematical expression for V_1 is therefore

$$\begin{aligned} V_1 &= \sum_{n=2}^{\infty} \frac{n\omega_s}{\sqrt{2}} L_{eff} \frac{2I_D}{n\pi} \left[\cos \left| \frac{2\pi n}{T} \cdot \frac{t_{DB}}{2} \right| - \cos \left| \frac{2\pi n}{T} \cdot \frac{T-t_{DB}}{2} \right| \right] \\ &= \sum_{n=2}^{\infty} \omega_s L_{eff} \frac{\sqrt{2}I_D}{\pi} \left[\cos \left| \frac{\pi t_{DB}}{T} \right|, n - \cos \left| \frac{\pi(T-t_{DB})}{T} n \right| \right] \quad (4.4) \end{aligned}$$

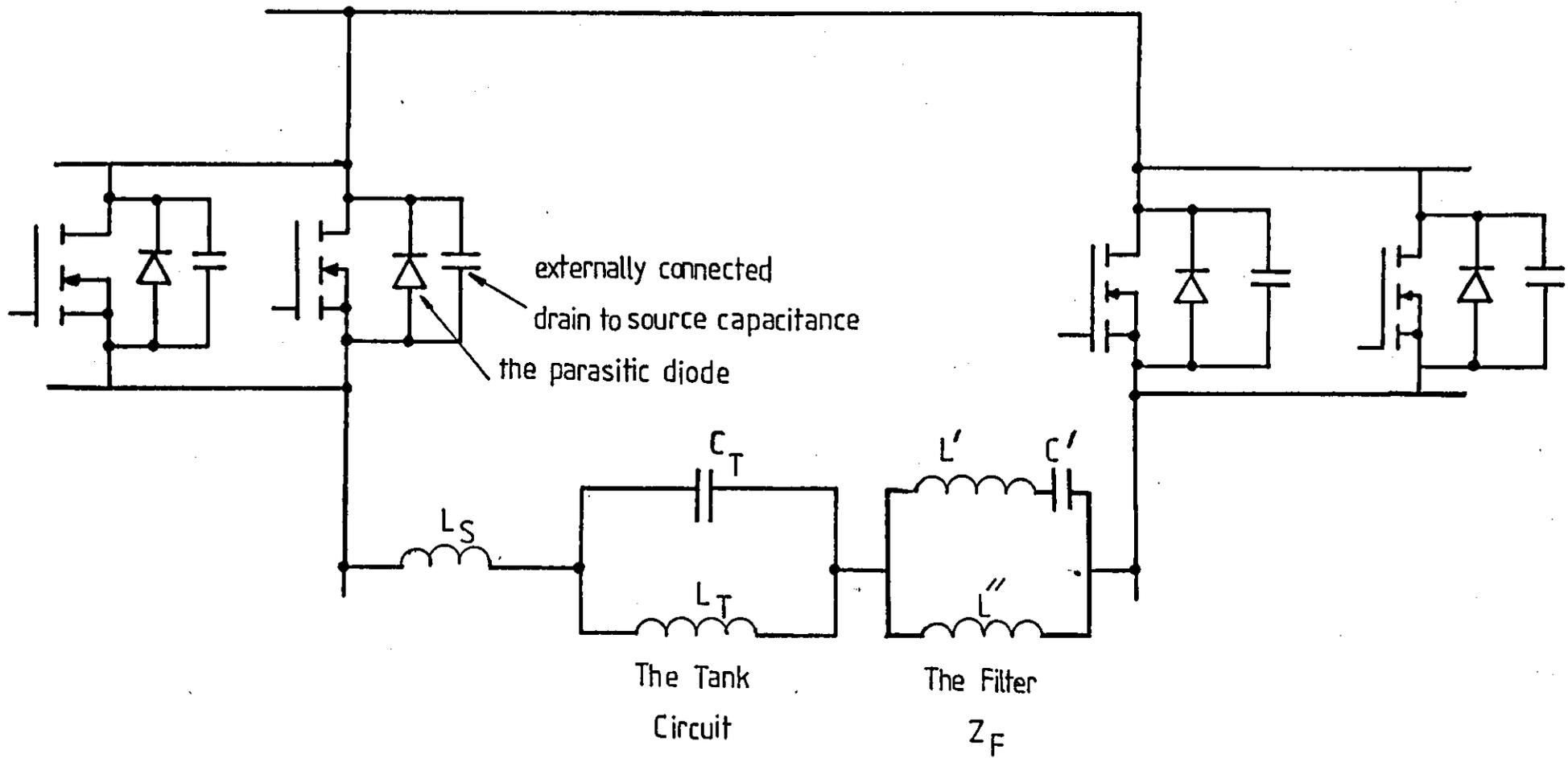


Figure 4.11 - Part of the inversion bridge, the filter Z_F and the snubber capacitors.

Where ω_s is the angular switching frequency.

The term in brackets is derived in Appendix 1 and is the difference between two cosine waves both of magnitude one but at different frequencies. As n varies from $n=2$ to ∞ the maximum magnitude of the term in brackets will be two. The expression will have a magnitude of 2 at a value of n determined by the values of t_{DB} and T . t_{DB} is dependent on the turn-off time of the MOSFETs and so drive circuit and power circuit component values.

The n th harmonic of the ringing voltage across each MOSFET ($V_{DS,n}$) is given by Eqn. 4.5.

$$V_{DS,n} = \frac{V_{1,n}}{1 - \frac{n^2 \omega_s^2}{\omega_{res}^2}} \cdot \frac{C_T}{C_T + 8C_{DS}} \quad (4.5)$$

where $V_{1,n}$ is the amplitude of the n th harmonic of V_1 .

The analysis leading to Eqn. 4.5 provides an understanding into how the filter Z_F and the snubber capacitors affect the circuit. It can be seen from Eqn. 4.5 that if ω_s/ω_{res} is increased then the ringing on the drain to source voltage waveform of MOSFETs will be affected. In particular the amplitudes of harmonic components above ω_{res} will be reduced.

Eqn. 4.5 is based on the assumption that when a MOSFET turns on the voltage across it is zero. If this is not true energy stored in the drain to source capacitance connected in parallel with the MOSFET will be dissipated in the MOSFET. In this case the voltage across capacitors contributing to the $8C_{DS}$ term in Eqn. 4.5 will not be the same immediately before and immediately after switching of MOSFETs takes place. The voltage across MOSFETs will only be zero when they turn on if the combination of the filter (Z_F), the tank circuit and the drain

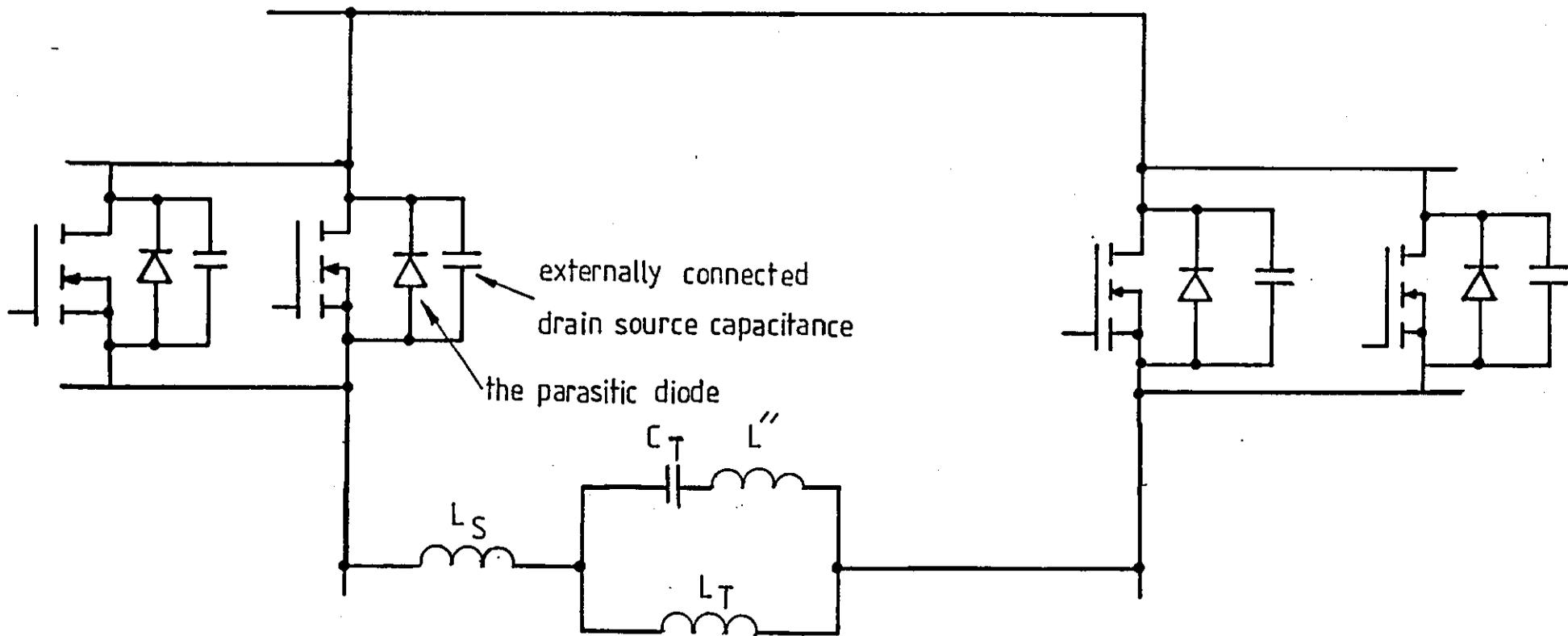


Figure 4.12 - The inversion bridge and the modified tank circuit.

source capacitors (C_{DS}) is fed at its resonant frequency. Even then Eqn. 4.5 will only be strictly true for the first harmonic.

4.2.4 The Modified Tank Circuit

In a commercial induction heating unit the switching frequency of the inverting bridge is varied so that the tank circuit is always at resonance. This variation is necessary because the electrical parameters of the workcoil vary through the heating cycle and change the resonant frequency of the tank circuit. The tank circuit and the filter Z_F were combined to avoid problems of Z_F no longer being low impedance to the switching frequency as this was changed during the heating cycle. Combining Z_F and the tank circuit also reduced the component count. The inversion bridge and the modified tank circuit are shown in Fig. 4.12.

The circuit presented to the fundamental component of the rectangular load current by the modified tank circuit is shown in Fig. 4.13.

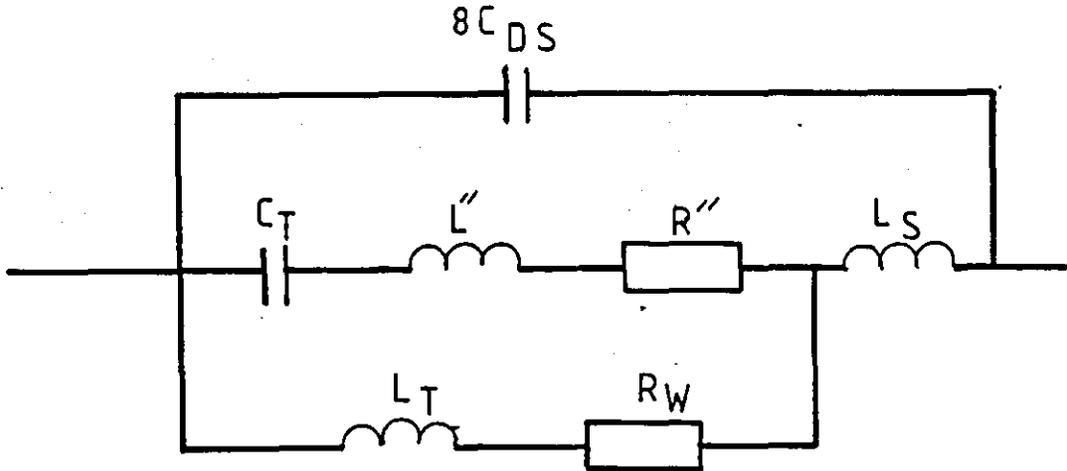


Figure 4.13 - The circuit presented to the fundamental component of the rectangular load current by the modified tank circuit

L_S is the parasitic lead inductance between the output terminals of the supply and the connections to the tank circuit.

The admittance of the modified tank circuit (Y_{MOD}) is given in Eqn. 4.6.

$$Y_{MOD} = \frac{1}{L_T \omega \left(\frac{1}{Q_L} + j \right)} + \frac{1}{\frac{\omega L''}{Q''} + j\omega \left[L'' - \frac{1}{\omega^2 C_T} \right]} + \frac{1}{j\omega \left[L_S - \frac{1}{8C_{DS}\omega^2} \right]} \quad (4.6)$$

where Q_L is the loaded Q of the workcoil and Q'' is the Q of inductor L'' .

Assuming that $\omega L_S \ll 1/8C_{DS}$ and Q_L and $Q'' \gg 1$ between 100 and 400 kHz then the lowest parallel resonant frequency (f_{r1}) the modified tank circuit is given in Eqn. 4.7.

$$f_{r1} = \frac{1}{2\pi} \sqrt{\frac{1}{L_T \left[\frac{C_T}{(1 - \omega_1^2 C_T L'')} \right] + 8C_{DS}}} \quad (4.7)$$

If L_{eff} and $8C_{DS}$ were excited at their series resonant frequency (f_{res}) then large voltages would appear across the MOSFETs. To overcome this problem Eqn. 4.8 must be satisfied.

$$2\omega_S > \omega_{res} \quad (4.8)$$

4.2.5 The Penalties of Using the Modified Tank Circuit

The penalties of reducing ringing in this way were firstly that the total drain source capacitance across MOSFETs was no longer negligible and formed part of the tank circuit. The component of circulating current that flowed in $8C_{DS}$ (I_{CM}) had to be carried by MOSFETs and, if

t_{DB} was assumed negligible, its rms value was given in Eqn. 4.9.

$$I_{CM} = \frac{8C_{DS} Q I_D}{\left[8C_{DS} + \frac{C_T}{1-\omega_S^2 C_T L''} \right] 0.9} \quad (4.9)$$

The current carried by an individual MOSFET had a peak value (\hat{I}_M) in Eqn. 4.10.

$$\hat{I}_M = \frac{I_D}{4} + \frac{\sqrt{2} C_{DS} Q I_D}{\left[8C_{DS} + \frac{C_T}{1-\omega_S^2 C_T L''} \right] 0.9} \quad (4.10)$$

The second penalty of this method was the extra losses in L'' . This penalty was least if L'' had a high Q and the work coil was closely coupled to the load.

4.2.6 The Effect of the Modified Tank Circuit on the Power Dissipation in MOSFETs during the Overlap Period in the Switching Sequence

A major advantage of the modified tank circuit was that it prevented the MOSFETs from carrying the full circulating current during the overlap period in the switching sequence.

If a current fed inverter feeds a simple two element tank circuit when all the MOSFETs are turned on together the voltage across the tank circuit is clamped. The voltage across the tank circuit capacitor cannot change so the current flowing in the workcoil, which is equal to the peak value of the circulating current at the time of overlap, must flow through the parasitic diodes in the MOSFETs and the MOSFETs themselves. This causes a large power dissipation in the MOSFETs. The use of the modified tank circuit overcomes this problem since the voltage across the tank circuit capacitor is no longer clamped during the overlap period. This prevents recourse to connecting diodes in series with MOSFETs to reduce the MOSFET power dissipation during overlap.

4.2.7 A Practical Investigation of the Effect of the Modified Tank Circuit on the Ringing on the Drain to Source Voltage of MOSFETs.

A modified tank circuit was built with $L_T = 8.1 \mu\text{H}$ ($Q = 24$) and $L'' = 9.8 \mu\text{H}$ ($Q = 24$), $C_T = 50 \text{ nF}$ and $C_{DS} = 10 \text{ nF}$. L_S is usually small compared to $1/\omega 8C_{DS}$ between 100 and 400 kHz. Neglecting L_S the lowest parallel resonant frequency of the modified tank circuit was found from Eqn. 4.7 to be 140 kHz. Since the filter Z_F and the modified tank circuit have been combined ω_{res} is now given by Eqn. 4.11.

$$\omega_{\text{res}} = \sqrt{\frac{1}{L_{\text{eff}} \cdot 8C_{DS}}} \quad (4.11)$$

f_{res} was calculated from Eqn. 4.11 to be 267 kHz. Therefore Eqn. 4.8 was satisfied. The unit was tuned to the lowest parallel resonant frequency of the tank circuit. This was found to be at 140 kHz which compared exactly with the calculated value.

Voltages and currents are shown in Fig. 4.14. The waveform of Fig. 4.14(a) shows that the voltage across the MOSFETs was now free from ringing. Comparison of Figure 4.14(a) and Fig. 3.9(b) shows that the incorporation of the filter improved the utilisation of the transistors' voltage sustaining capability by 30%.

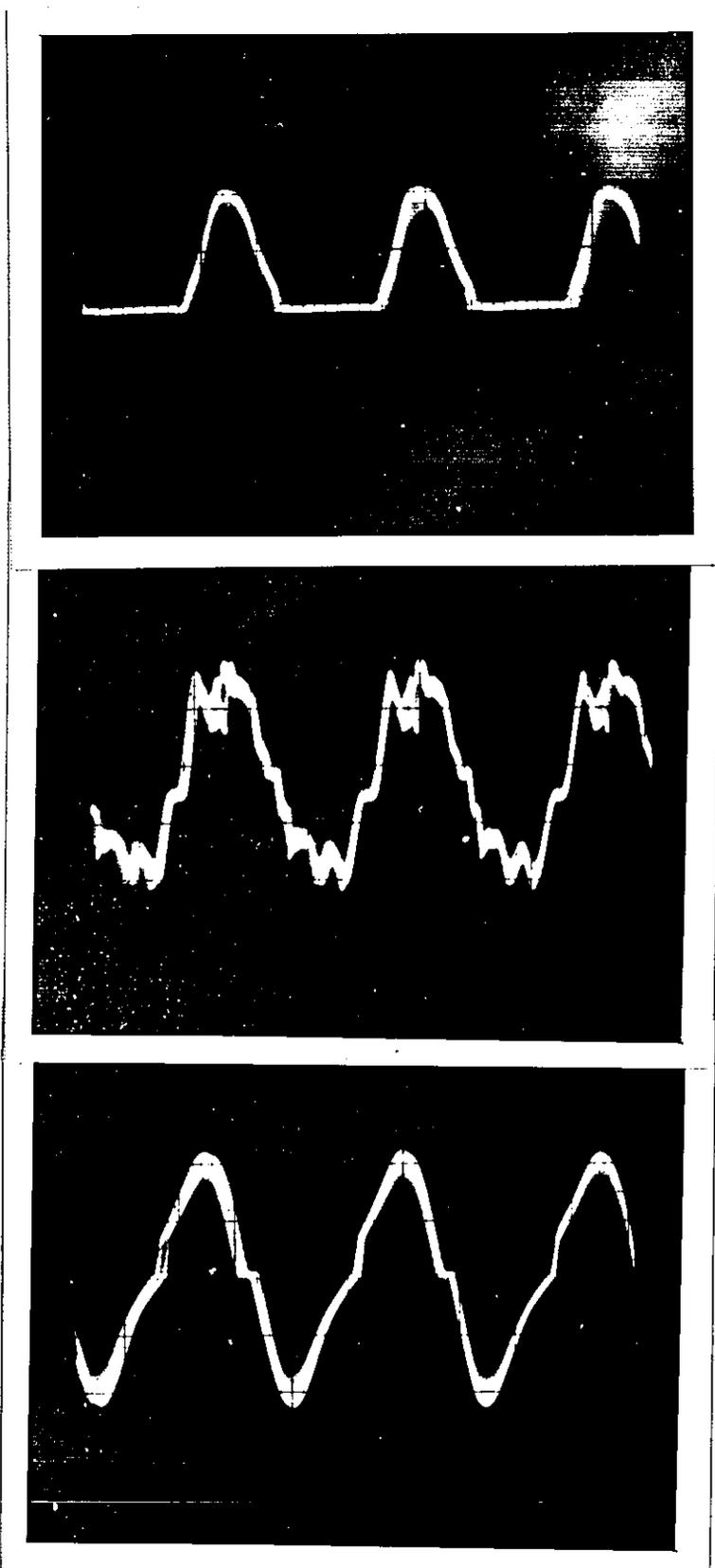


Figure 4.14 - Waveforms of (a) the drain to source voltage across MOSFETs (20V/div, 2 μ s/div), (b) the current in the dc link (0.2A/div, 2 μ s/div), and (c) the voltage across the workcoil (20V/div, 2 μ s/div).

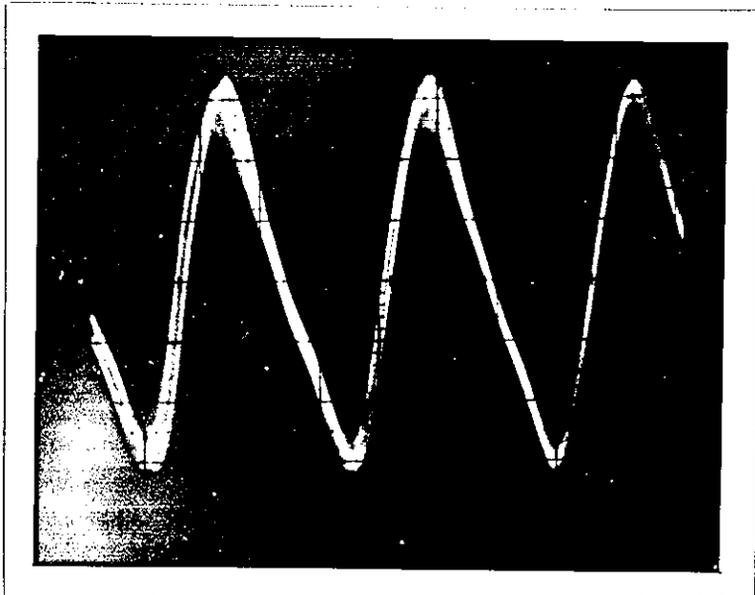
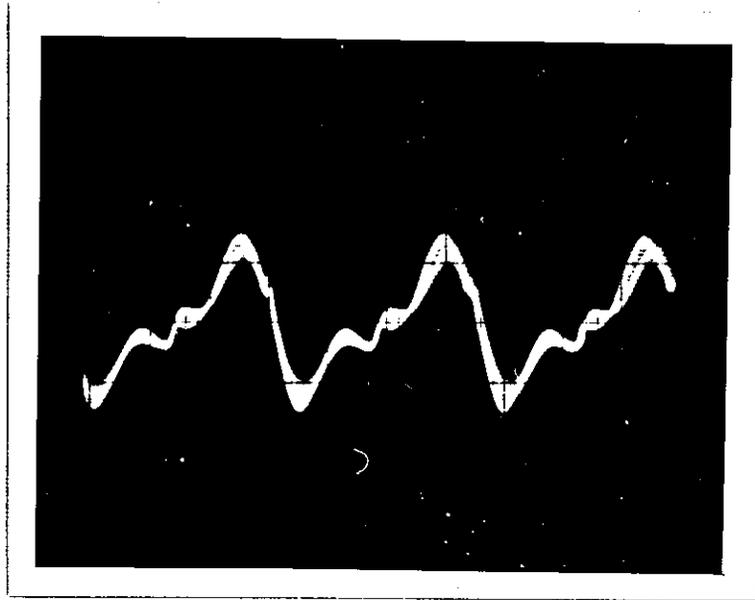


Figure 4.14 - (d) the voltage across inductor L'' (20V/div, 2 μ s/div)
and (e) the voltage across the tank circuit capacitor
 C_T (20V/div, 2 μ s/div) when the current fed inverter
fed a modified tank circuit.

L_S can be estimated from the ratio of the fundamental component of voltage across the drain to source of a MOSFET to that across the workcoil L_T . L_S was found to be 0.7 μ H.

L_S had a reactance at this frequency, which was small compared to the reactance of $8C_{DS}$ e.g. at 140 kHz, 0.6 Ω and 5.5 Ω . This justified neglecting L_S in Eqn. 4.6 when calculating the lowest parallel resonant frequency of the modified tank circuit.

In Fig. 4.14(d) the inductor L'' can be seen to sustain higher harmonic voltages. The capacitor C_T was a low impedance to higher harmonic components and so free of higher harmonic voltages compared to inductor L'' as shown in Fig. 4.14(e).

Since the value of I_D was 0.2 A when feeding the modified tank circuit, \hat{I}_M was calculated from Eqn. 4.10 as 0.3 A which agreed with experimental values (see Fig. 4.14(b)).

The dc link current for the waveforms shown in Fig. 3.9 was 0.1A and for the waveforms in Fig. 4.14 was 0.2A for the same dc link voltage of 28V. This is because the modified tank circuit in Fig. 4.12 was a lower impedance at this parallel resonant frequency than the initial two element tank circuit.

The rms MOSFET drain current in Fig. 3.9(b) is difficult to calculate compared with the waveform in Fig. 4.14(b) but, by inspection, it is approximately half of that in Fig. 4.14(b). Therefore as a result of using the modified tank circuit there was a 30% improvement in the MOSFET's voltage utilisation, a 50% reduction in current utilisation for two times the power into the tank circuit. Overall there was a 30% increase in the utilisation of the MOSFETs' switching capability. There was also a great improvement in the predictability of the drain current waveform making design easier.

Work has also been carried out on an inverter topology that placed all the tank circuit capacitors across the drain to source of MOSFETs (Tebb et al 1986b). This circuit had very good inherent suppression of ringing. It did however require the MOSFETs to carry the full circulating current and so was really 'overkill'. The modified tank circuit is therefore recommended for dealing with problems of ringing.

4.2.8 The Design of Component Values for the Modified Tank Circuit

In practice choosing the components of the modified tank circuit to satisfy Eqn. 4.8 makes the tuning very sensitive. A matching procedure as outlined in the flow diagram in Fig. 4.15 is therefore recommended. C_{eq} is the equivalent capacitance of the branch containing L'' and C_T at the inverter switching frequency (f_s). C_T is chosen to be $0.7C_{eq}$ because the tuning would be too sensitive if C_T was a lot smaller than C_{eq} . Equations for C_{eq} , the efficiency of the tank circuit and the power dissipated in the tank circuit are derived in Appendix 3. A Basic programme was developed on the BBC Microcomputer to implement the flow diagram in Fig. 4.15 and so assist the design of matching circuitry. A listing of the programme is given in Appendix 4.

If greater suppression of ringing is required than that achieved with a modified tank circuit designed by the programme in Appendix 4 C_{DS} can be increased. The impedance of the drain to source capacitors will thus be reduced and they will become more effective at shunting the ringing currents.

If less suppression of ringing than that achieved with a design by the programme is acceptable then C_T can be made larger. The programme will then calculate a value of L'' which is smaller and so the value of L_{eff} will be lower. This will increase f_{res}/f_s and so increase the ringing.

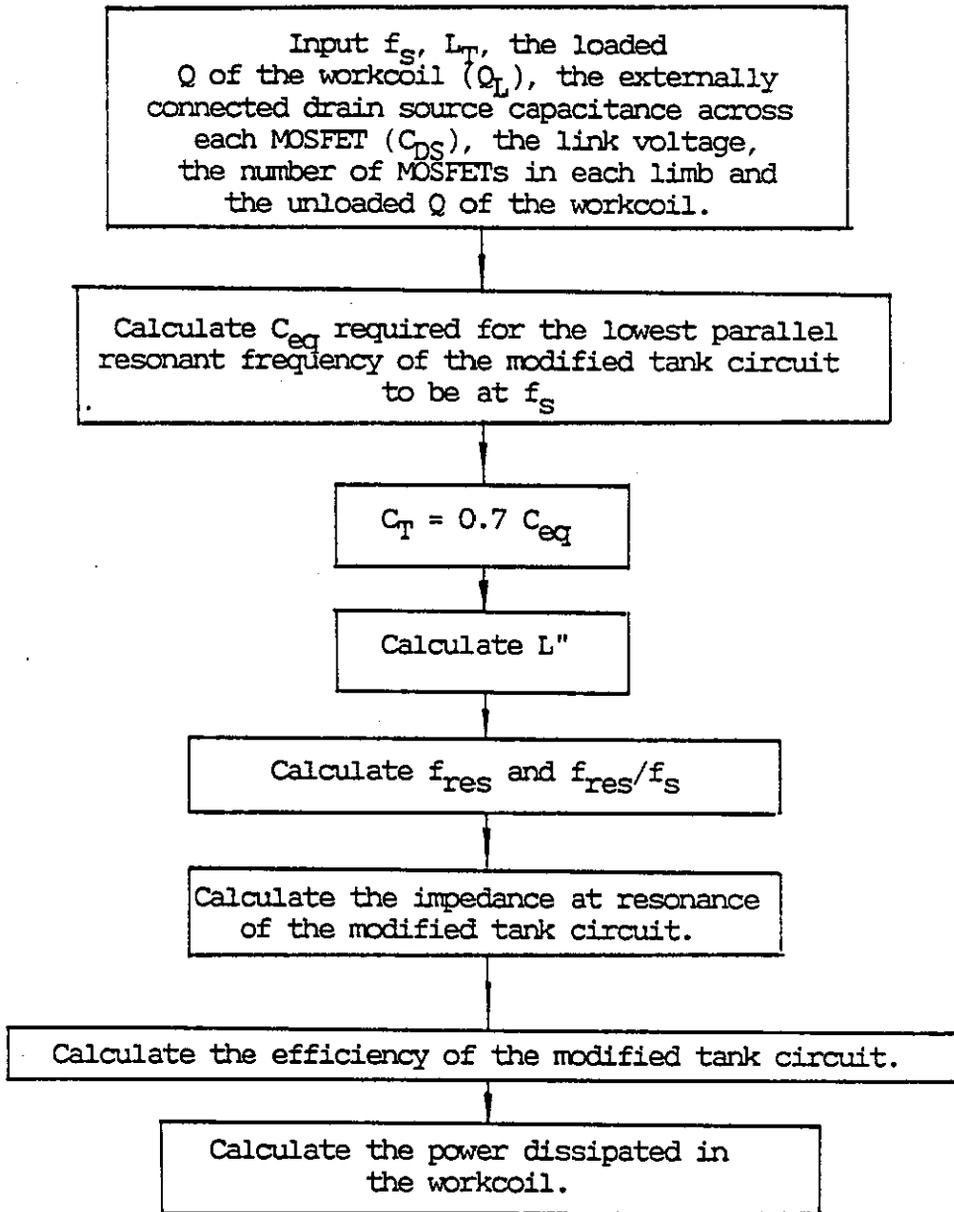


Figure 4.15 - A flow diagram of the design procedure for the modified tank circuit.

4.2.9 Summary of the Suppression of Ringing Using a Modified Tank Circuit

A method of suppression of ringing has been proposed that uses only high Q components. Frequency components of voltage spikes produced by the switching of current in parasitic lead inductances need to be prevented from resonating with the drain source capacitance of MOSFETs for suppression to be effective. The use of the inductor L" has meant that the drain source capacitance required to meet the above criterion is reduced to a convenient value. In practice the lossiness of the workcoil and other circuit components means that the resonant frequency of L_{eff} and $8C_{\text{DS}}$ can be above the second harmonic of the switching frequency and ringing will still be within acceptable limits.

4.3 PRACTICAL INVESTIGATIONS OF THE PERFORMANCE OF THE PROTOTYPE CURRENT FED INVERTER FEEDING INDUSTRIAL WORKCOILS

The unit was used to feed 0.7 kW into a coil of the type usually used industrially for sealing tops on plastic bottles. 2 kW was also fed into a coil the same as those in use commercially for vapour deposition processes.

(a) The cap sealing coil.

Cap sealing is a technique widely used in the pharmaceutical and process industries to create an airtight seal on a container. A thin aluminium disc is contained in the cap of the container. The cap is firmly screwed on to press the container rim and the aluminium disc together. When the container passes through the coil the aluminium disc is heated by its interaction with the magnetic field. The rim of the plastic container in contact with the aluminium disc softens and forms a seal. A frequency of between 100 and 400 kHz is optimum for cap sealing because below 100 kHz the coupling into the aluminium disc is poor and above 400 kHz intense localised heating can result causing burning at any irregularities on the circumference of the disc.

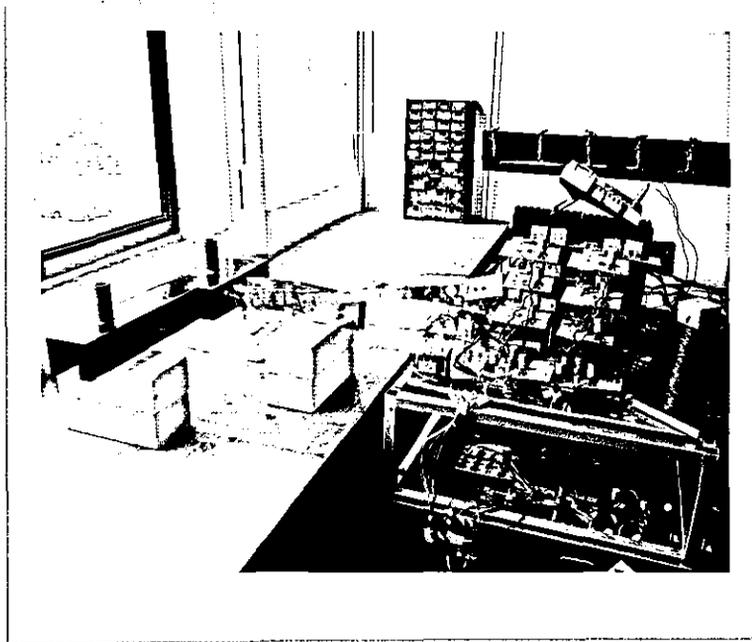


Figure 4.16 - A commercial cap sealing coil

A commercial cap sealing coil shown in the photograph in Fig. 4.16 was used for the experiments. The coil was a skid coil (Hobson 1984) which was water cooled and had been encapsulated in epoxy resin for safety and to support the coil. There was a channel in the underside of the coil assembly just large enough for the caps of the containers to pass through.

The coil was connected in a simple two element tank circuit. From measurements at the parallel resonant frequency of the circuit the inductance of the coil was found to be $4.4 \mu\text{H}$ and the Q of the coil 31.

A modified tank circuit was designed with $L'' = 1.1 \mu\text{H}$, $C_T = 300\text{nF}$ and the external capacitance across each of the sixteen MOSFETs in the inverting bridge was 10nF . The ratio f_{res}/f_s was therefore 5.5. The coil was fed with 0.7 kW at 109 kHz . The link voltage was 200V and the link current was 3.5A . Waveforms around the circuit are shown in Fig. 4.17.

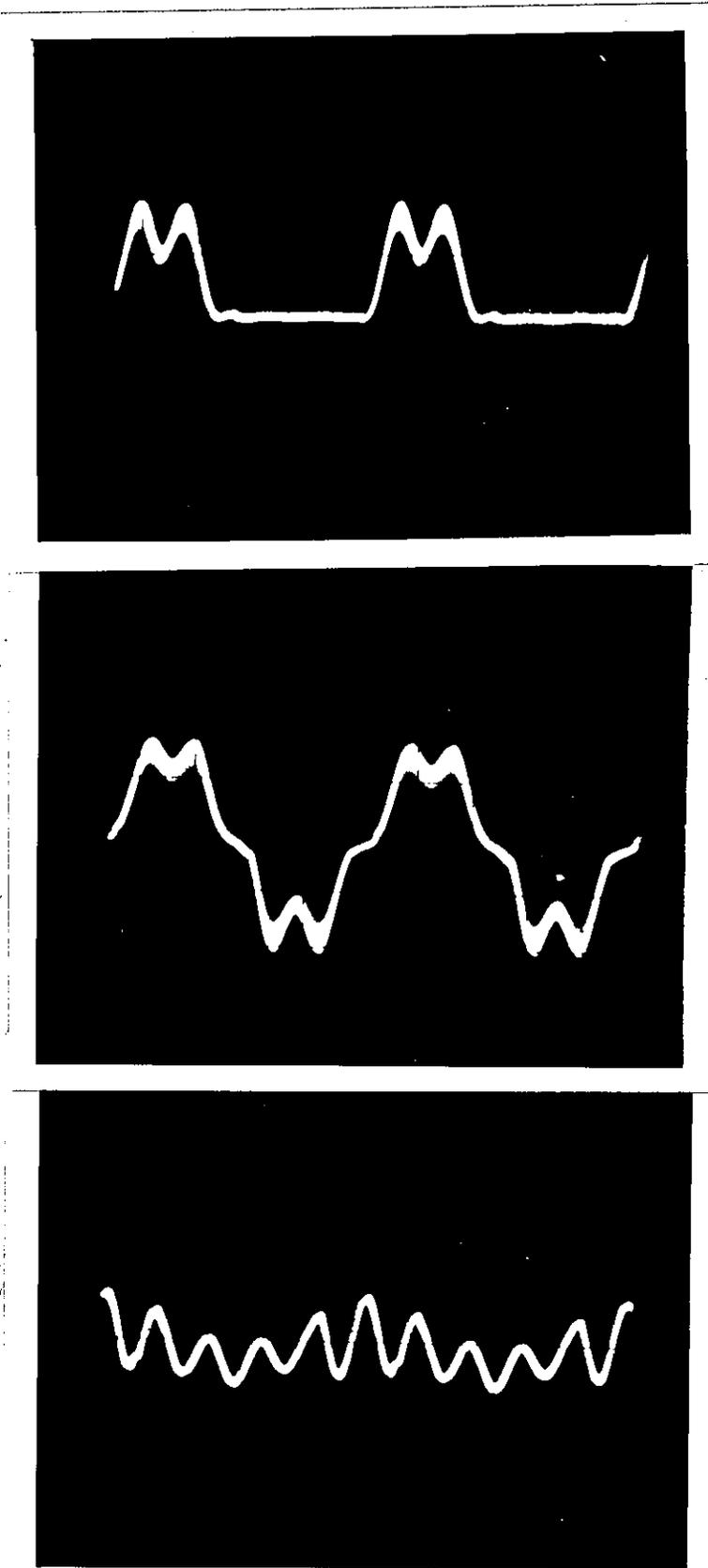


Figure 4.17 - Voltage waveforms across (a) the drain to source of MOSFETs, (b) the workcoil, and (c) inductor L".

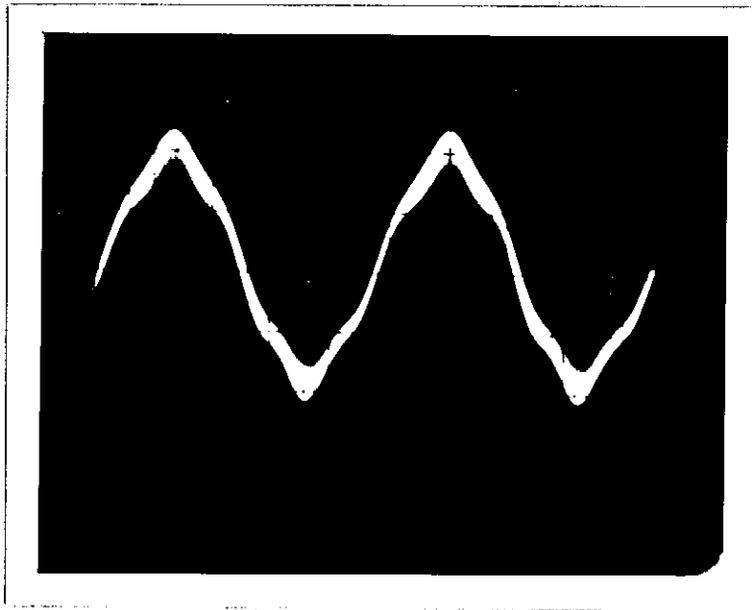


Figure 4.17 - (d) capacitor C_T when the current fed prototype fed a commercial cap sealing coil in a modified tank circuit (200V/div, 2 μ s/div).

The coil was used to seal caps on bottles supplied by the sponsoring company. The caps were properly sealed in 2s. This was fast enough for the application. The distance between the cap and the coil was found to be critical. If the separation was changed from 1 mm to 5 mm the time taken to seal the caps changed from 2s to 8s.

(b) The vapour deposition coil.

In the vapour deposition process the material to be deposited is placed in a graphite boat. The material onto which the deposition is to take place is put, along with the graphite boat, in a gas tight chamber. The gas in the chamber is then evacuated. The graphite is then induction heated by a coil placed round the outside of the chamber. The material in the graphite boat is evaporated and is deposited on the target material.

To simulate the industrial situation a graphite boat identical to those used in industry was placed in a silica glass tube to insulate it from the workcoil. A solenoidal workcoil of 10.5 turns was used. The unloaded inductance of the workcoil was $2.8 \mu\text{H}$ and the unloaded Q was 44. The loaded inductance was $2.7 \mu\text{H}$ and the loaded Q was 15. The efficiency was calculated to be 65%. A modified tank circuit was designed with values $L'' = 1.1 \mu\text{H}$, $C_T = 400\text{nF}$ and the C_{DS} across each MOSFET = 10nF . Therefore f_{res}/f_s was 5.3.

A power of 2 kW was fed into the tank circuit at 120 kHz. The link voltage was 200V and the link current was 11.0A. The current and voltage waveforms around the circuit are shown in Fig. 4.18. The graphite reached a temperature of 850°C in 5 min 30 s which was faster than required for the application.

In both Fig. 4.17 and Fig. 4.18 it can be seen that there is a high degree of second harmonic distortion on the drain to source voltage waveform of MOSFETs. This is because the attenuation of the second harmonic is less than that of high frequency harmonics. This is expected from the analysis in Section 4.2.3.

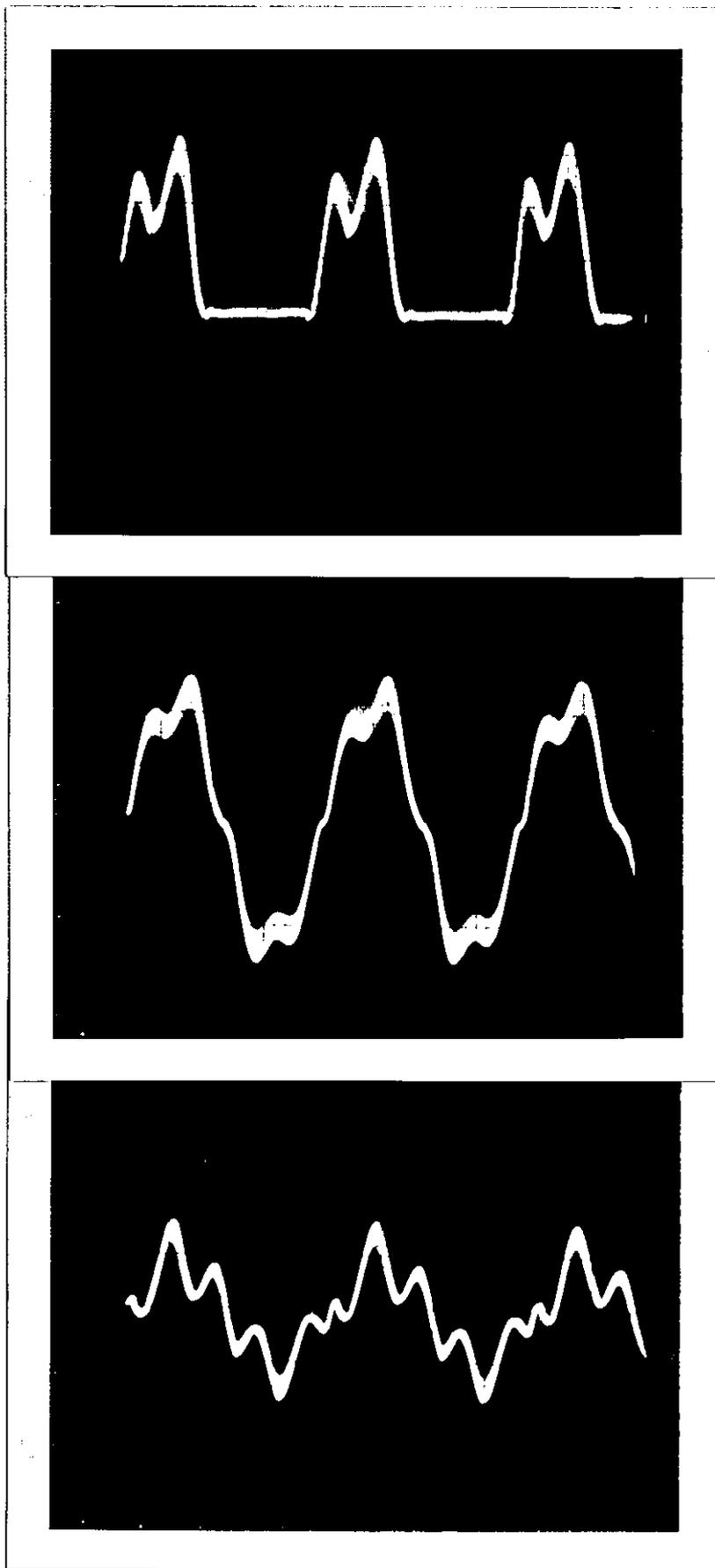


Figure 4.18 - Voltage waveforms across (a) the drain to source of MOSFETs, (b) the workcoil and (c) inductor L".

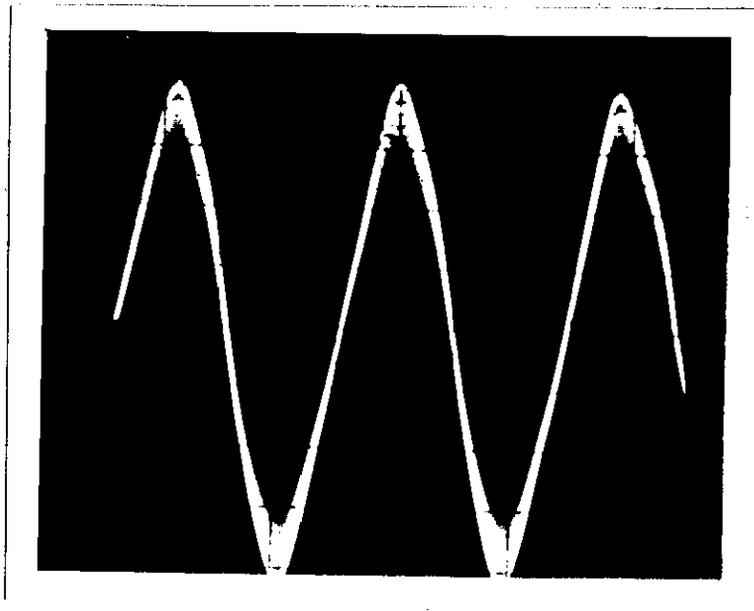


Figure 4.18 - (d) capacitor C_T when the current fed prototype fed a workcoil used for vapour deposition in a modified tank circuit (100 V/div, 2 μ s/div).

(c) Short circuit tests on the prototype.

In a typical induction heating situation the workcoil is very likely to be short circuited. This may be caused by the compression of the coil caused by a misalignment in mechanical handling equipment in an automated production line. It may also be caused by the inadvertent dropping of a metallic object such as a screwdriver onto a workcoil. When the unit was feeding power into both the cap sealing coil and the vapour deposition coil the workcoil was intentionally short circuited. This was done repeatedly when the unit was feeding 1 kW into the cap sealing coil and 3 kW into the vapour deposition coil. The unit shut itself down on all occasions without damage to MOSFETs or any other components.

4.4 CONCLUSIONS

A prototype current fed inverter has been designed and constructed. Problems of ringing on the drain to source voltage of MOSFETs caused by switching current off speedily in parasitic lead inductance have been overcome by the use of a modified tank circuit. The modified tank circuit is a novel idea which has been proved experimentally to be efficient and effective in reducing ringing. The modified tank circuit has also reduced the sensitivity of the tuning of the unit. This facilitated the manual tuning and also the provision of automatic tuning (see Chapter 6). Values of f_{res}/f_s of up to 5.5 have been found to reduce ringing markedly.

Problems of optimisation of circuit layout have been reduced because the drain to source voltage waveform was now dependent on lumped circuit components rather than parasitic lead inductances.

The unit has been used to feed industrial workcoils. The unit has proved experimentally that it is capable of providing the power requirements of these coils. Tests on the short circuit performance of the prototype have shown that the current fed inverter can be shut down without damaging MOSFETs when feeding substantial power into the tank circuit.

CHAPTER 5THE COMPUTER SIMULATION OF A CURRENT FED FULL BRIDGE INVERTER

A computer numerical analysis package called SPICE was used to analyse the operation of the current fed full bridge inverter.

5. THE COMPUTER SIMULATION OF A CURRENT FED FULL BRIDGE INVERTER

An elementary analysis of the current fed full bridge inverter has been given in Section 3.3. A computer simulation of the inverter was attempted to extend this analysis to consider the transient performance of the inverter immediately after switch on. The computer was also used to investigate in more detail the effect of the modified tank circuit.

5.1 THE CHOICE OF OF METHOD OF ANALYSIS

The method of analysis used in Section 3.3 was that of equating power flow in the dc link to power dissipation in the tank circuit. This technique is only valid for steady state conditions and no account is taken of parasitic lead inductances.

A computer simulation using a numerical technique was used. A numerical technique can cater for transient conditions and can easily deal with a circuit representation of the inverter containing many components. Circuit parameters that vary with current and voltage can be included. An example of one of these parameters is the drain current in a MOSFET which varies according to the gate source voltage. The flexibility of computer packages using numerical techniques has led to them being made available on some University computers. These packages use high level languages and so programming is made much easier. Since the user does not get deeply involved in mathematics it is possible to keep an 'engineering feel' of the way the model is behaving. (Bowes 1982).

For the reasons outlined above it was decided to use a numerical simulation package.

For completeness the possibility of using an analytical solution was investigated. This could be more accurate than a numerical solution and it would require only a microcomputer rather than a main frame computer which would be very convenient. The equations governing the operation of the inverter are given in Appendix 5. A solution using Laplace Transforms was used since this can cater with initial conditions more easily than a solution using Fourier Analysis.

It can be seen in Appendix 5 that the solution becomes extremely complex even for relatively simple circuits even though many simplifying assumptions are made.

5.2 SPICE

A computer simulation package called SPICE has been developed to analyse electrical circuits. SPICE was used because it was available as one of the facilities offered to Loughborough University by the University of Manchester Regional Computer Centre (UMRCC). The version of SPICE available was 2G.5.

SPICE contains models of a MOSFET. These models have been developed for transistors used in integrated circuits. Very little work has been done on modelling power MOSFETs. The models of the small signal MOSFETs which are included in the SPICE package require 37 parameters to be specified for a full description of the MOSFET.

To simulate a circuit using SPICE all the nodes are numbered. The circuit components are then described in the programme by reference to the nodes which they are connected to.

The following facilities which are useful in simulating a current fed inverter are offered by SPICE (see the UMROC SPICE manual).

- (a) Passive components, i.e. resistors, capacitors and inductors, are specified by writing one line of the programme for each component. The numbers of the two nodes to which the component is connected are specified. The value of the component is then given. For inductors and capacitors the initial conditions of current, in the case of an inductor, or voltage, in the case of a capacitor, can be specified. These initial conditions are only applied if the Use Initial Conditions (UIC) option is specified.

- (b) DC voltage sources can be specified by providing information on their connecting nodes and their value in the programme. Pulses can also be programmed. The delay time, rise and fall time, width, height and repetition frequency of the pulse are written into the programme.
- (c) The SPICE package contains the models for several semiconductor devices such as the MOSFET and the Bipolar Transistor. There are three different MOSFET models available. (Vladimirescu et al 1980). The first is the Shichman-Hodges model. The second model incorporates most of the second-order effects of small-size devices and the third is a semi-empirical model. The Shichman-Hodges model is the most useful for analysing power electronic circuits. The other two models concentrate on refinements more relevant to integrated circuit design.

When a MOSFET is described in the programme connecting nodes are defined and the user's software refers to information on its parameters. This parameter information is defined elsewhere in the programme for convenience since it may be referred to by many transistors in the circuit. The 37 parameters that can be specified can be divided into electrical or derived parameters, (e.g. threshold voltage), and processing or primary parameters such as the substrate doping level. Electrical parameters will override the values calculated from processing data. The most important electrical parameters are the zero bias threshold voltage (V_{T0}) and the transconductance (KP). The transconduction parameter is defined by Eqn. 5.1.

$$I_D = KP (V_{GS} - V_T)^2 \quad (5.1)$$

- (d) There are many possible options concerning limitations on the numerical iterations that the programme can carry out. Examples of these are $ITL5 = x$ which resets the transient analysis total iteration limit (the default is 5000) $LIMPTs = x$ which resets the total number of points that can be printed or plotted (the default

is 201) and METHOD = name which sets the numerical integration method used. A trapezoidal numerical integration method was used (Froberg 1970), Conte et al 1980). In the trapezoidal method the programme takes points on the waveforms to be integrated. These points are joined by straight lines forming a series of trapezoids. The areas of all these trapezoids are summed to provide an estimate of the integral of these waveforms.

- (e) If a line is included in the programme beginning with .tran then a transient analysis of the circuit is carried out. The line requesting a transient analysis also specifies the time interval between calculations and the time interval between values being printed or plotted. If this line also contains the request UIC then the initial conditions contained in lines specifying passive components will be used.
- (f) The voltages between any nodes can be printed out. To print out a current a voltage source must be connected into the circuit. This is then used as an ammeter.

5.3 THE MODEL OF A POWER MOSFET

The MOSFET model originally incorporated in the SPICE package was designed primarily for integrated circuit design. In the package it is possible to specify many electrical and physical parameters for the MOSFET all of which have default values. The MOSFET model is assumed to have four terminals which are associated with the drain, the source, the gate and the bulk substrate of the device. For power MOSFETs the bulk substrate can be assumed to be connected to the source.

A little work has been done on obtaining values for the electrical parameters of a power MOSFET which can be input to the SPICE model indirectly from manufacturers data sheets (Nienhaus et al 1980, Rashid 1986). Parameters suitable for the SPICE MOSFET model have been obtained from a manufacturer's data (K.A. Amarasinghe 1986). The most important parameters are the transconductance parameter (KP) and the zero bias threshold voltage (VTO). These were set to $55 \text{ V}^{-1} \Omega^{-1}$ and

3.5V respectively. The turn-on and turn-off times of MOSFETs have negligible effect on the transient response of an inverter if they are small compared to the time period of the switching frequency. (Bowes 1982). Since the turn-on and turn-off times of MOSFETs are typically less than 200 ns they are small compared to the time period of the switching frequency at 400 kHz which is 2.5 μ s. The internal capacitances of MOSFETs were not specified in the programmes and were set to default values by the computer. These default values were extremely small so the MOSFET model used was close to an ideal switch with regard to switching performance. The dc output characteristic of the MOSFET model used in the analysis is shown in Fig. 5.1.

5.4 THE SIMULATION OF THE CURRENT FED INVERTER

The use of SPICE means that the performance of any matching circuit can be investigated. SPICE can easily deal with transient conditions and so the performance of a current fed inverter just after power is applied to the dc link can be simulated.

5.4.1 A Simulation of a Current Fed Inverter Feeding a Two Element Tank Circuit

Assuming that the ripple on the voltage in the dc link is negligible then the circuit in Fig. 5.2 accurately represents the current fed inverter described in Section 3.3 and Chapter 4. The circuit in Fig. 5.2 was simulated. The nodes used to define the circuit for SPICE are shown in Fig. 5.2.

The circuit in Fig. 5.2 was simulated with component values $l_c = 10$ mH, $r_c = 0.5$ Ω , $l_{p1} = l_{p2} = l_{p3} = l_{p4} = 50$ nH, $c_{ds1} = c_{ds2} = c_{ds3} = c_{ds4} = 2$ nF, $l_t = 8.1$ μ H, $r_w = 0.53$ Ω , $c_t = 50$ nF, $l_s = 0.7$ μ H, $r_s = 0.1$ Ω and the gate drive voltage was 15V. A listing of the programme is given in Appendix 6. The switching frequency of the inversion bridge was 250 kHz. These values corresponded to the inverter and matching circuitry as tested in Section 3.3.

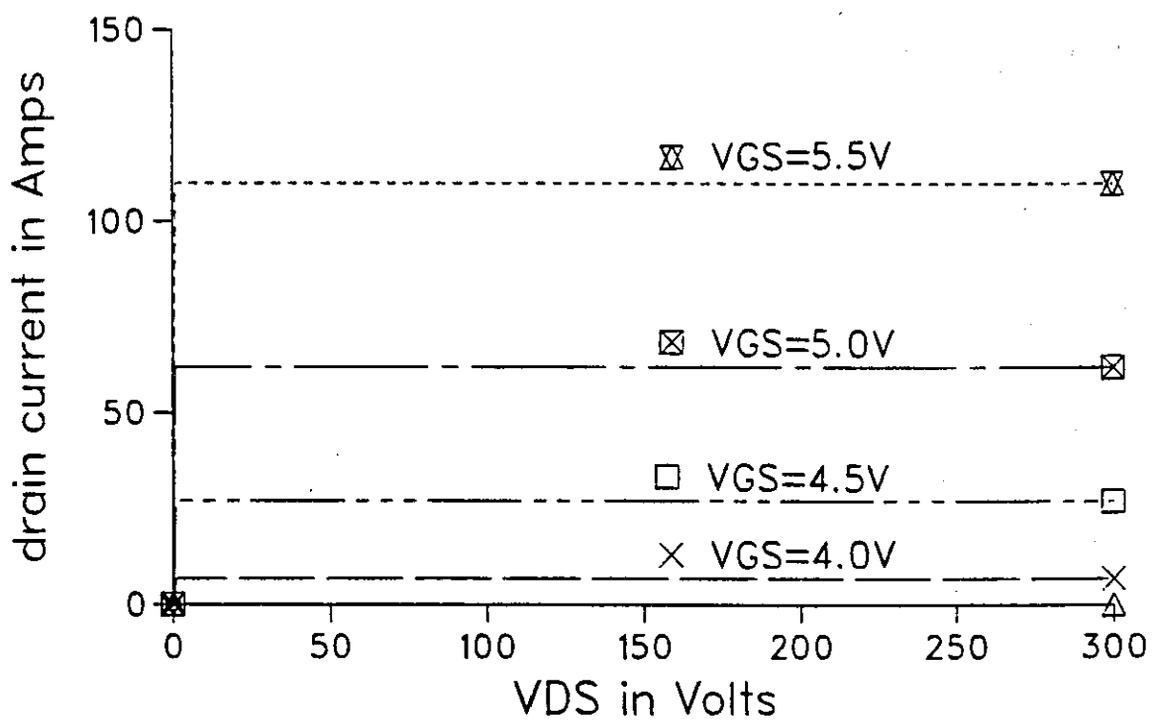


Figure 5.1 - The dc characteristic of the MOSFET model used in analysis using SPICE.

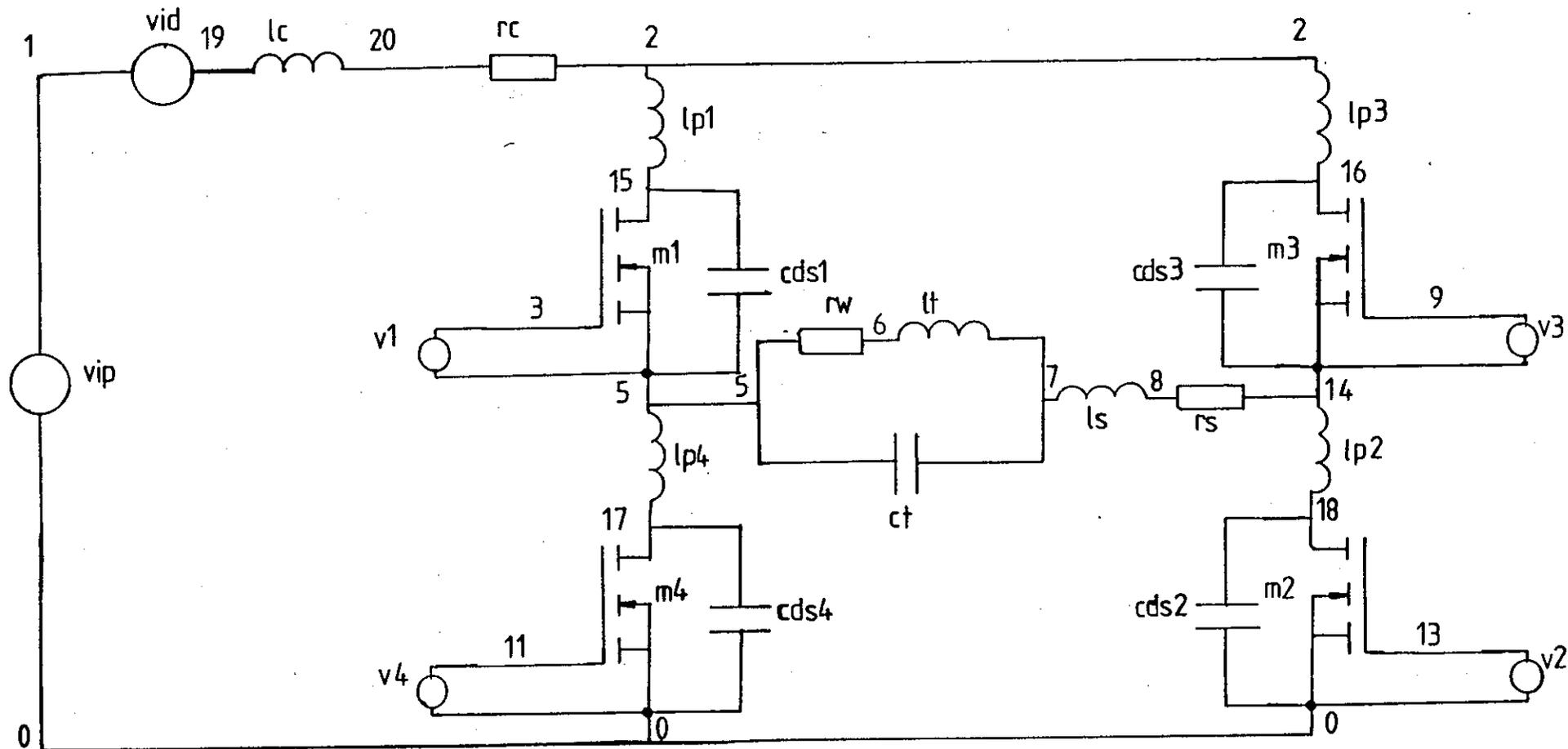


Figure 5.2 - The circuit used to model the inverter feeding a simple two element tank circuit using SPICE.

The steady state waveforms of the circuit were investigated. Initial conditions based on expected values were assigned to capacitors and inductors to speed up the attainment of steady state conditions and so make better use of the computer's processing time. Steady state waveforms of voltages and currents around the circuit are shown in Fig. 5.3. The following details of the waveforms in Fig. 5.3 should be noted.

- (a) The waveforms agree closely with the experimental waveforms in Fig. 3.9.
- (b) The ringing on the drain to source voltage of MOSFETs can clearly be seen. There are about five full cycles of ringing on the half sinusoid of voltage across the drain to source of MOSFETs. The major component of the ringing is therefore at about 2.5 MHz. The analysis in Section 4.2.3 is based on the idea that the components in the path of ringing current shown in Fig. 4.9 determine the extent of ringing. For the circuit in Fig. 5.2 the components determining the extent of ringing when switches S1 and S2 are off are therefore l_{p1} , c_{ds1} , c_t , l_s , r_s , l_{p3} , l_{p2} , c_{ds2} and l_{p3} . Therefore the predicted frequency of the major component of ringing (f_{mring}) is given in Eqn. 5.2.

$$f_{\text{mring}} = \frac{1}{2\pi} \sqrt{\frac{1}{(l_s + l_p)2c_{ds}}} \quad (5.2)$$

The predicted value is therefore 2.9 MHz. This close agreement supports the approach taken in Section 4.2.3 where the path of ringing currents in Fig. 4.9 is investigated to design a modified tank circuit which reduces ringing.

- (c) The voltage across the workcoil is free of ringing. This is because the tank circuit capacitor presents a low impedance to ringing currents relative to other components in the path of the ringing current.

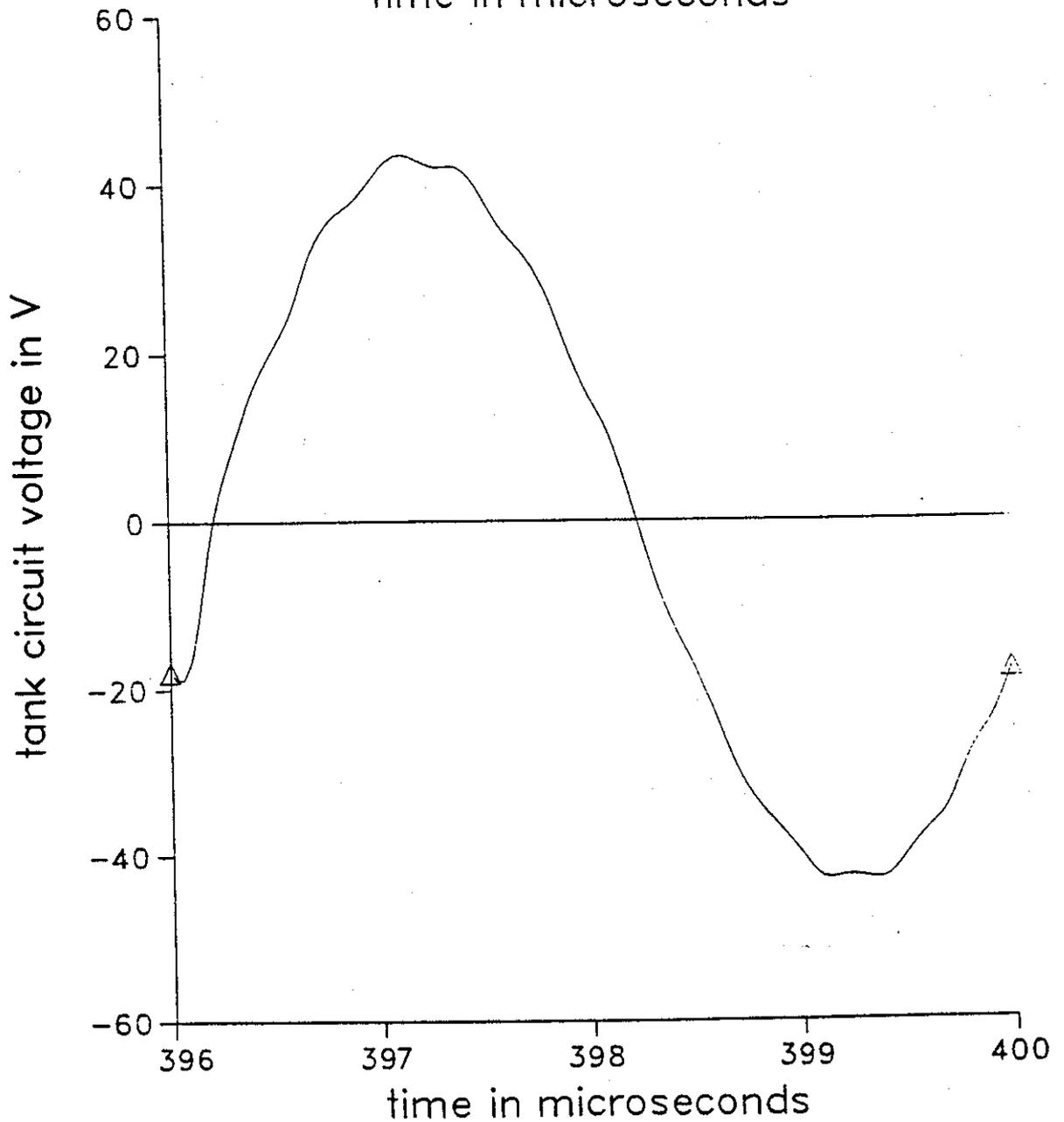
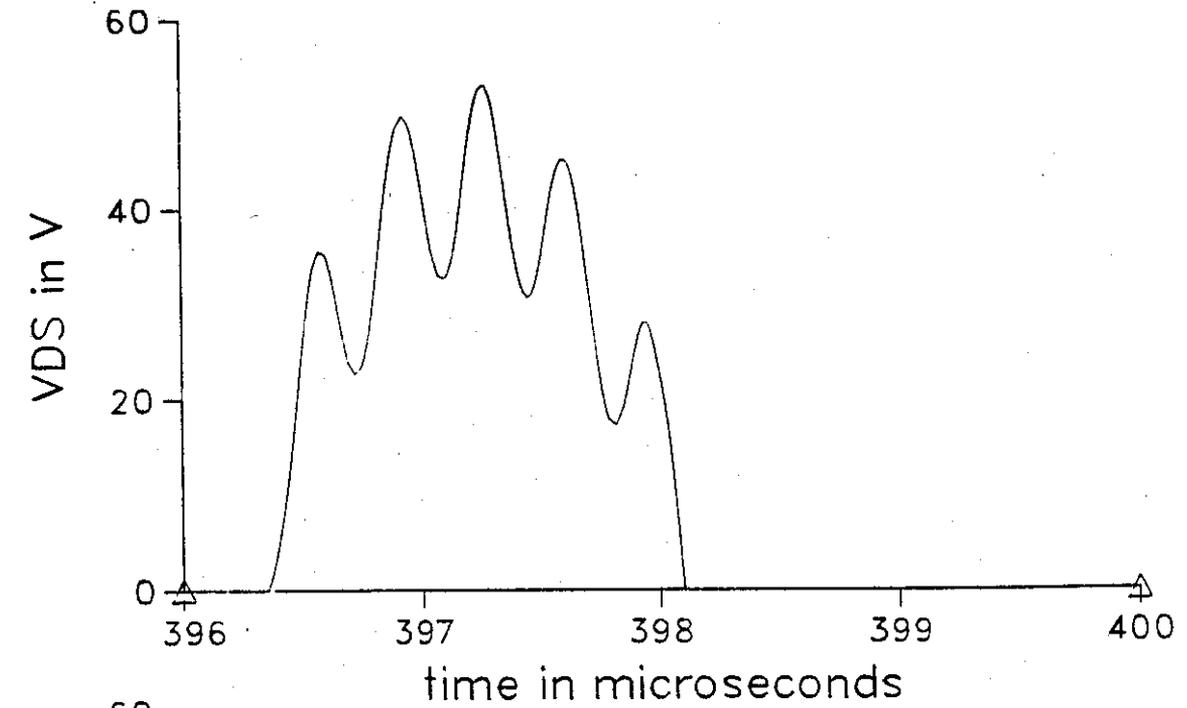


Figure 5.3 - Waveforms of drain to source voltage and tank circuit voltage for a current fed inverter feeding a simple two element tank circuit resulting from an analysis using SPICE

- (d) The peak of the fundamental component of the voltage across the drain to source of MOSFETs is 44 V as predicted from Eqn. 3.2. However the ringing has increased the maximum voltage sustained by MOSFETs to 49 V.

The average value of the current in the dc link was 0.13A which agreed with the practical value. The fundamental component of the rf current in the dc link, which is at twice the switching frequency of the inversion bridge, was 1% of the link current.

5.4.2 A Simulation of a Current Fed Inverter Feeding a Modified Tank Circuit

The inverter circuit node map shown in Fig. 5.2 was extended to include the modified tank circuit as shown in Fig. 5.4. The circuit was simulated with the same component values as in Section ~~4.5.1~~^{5.4.1} except that $c_{ds1} = c_{ds2} = c_{ds3} = c_{ds4} = 40 \text{ nF}$, $l_{ll} = 9.8 \text{ nH}$, $r_w = 0.2\Omega$ and $r_{ll} = 0.25 \Omega$. (Appendix 6). The switching frequency was 140 kHz. These values represented the inverter and matching circuitry tested in Section 4.2.7. Waveforms of voltages and currents around the circuit in steady state conditions are shown in Fig. 5.5. Initial conditions based on expected values were assigned to capacitors and inductors to speed up the attainment of steady state conditions and so make better use of the computer's processing time.

The following points are worthy of note concerning the waveforms in Fig. 5.5.

- (a) The waveforms in Fig. 5.5 can be seen to closely agree with the practical waveforms in Fig. 4.15.
- (b) The ringing on the drain to source voltage of MOSFETs seen in Fig. 5.3 has been attenuated by the modified tank circuit.

The current in the dc link was greater than that associated with waveforms in Fig. 5.3. This was because the impedance at resonance of the modified tank circuit was less than that of the tank circuit in Fig. 5.2.

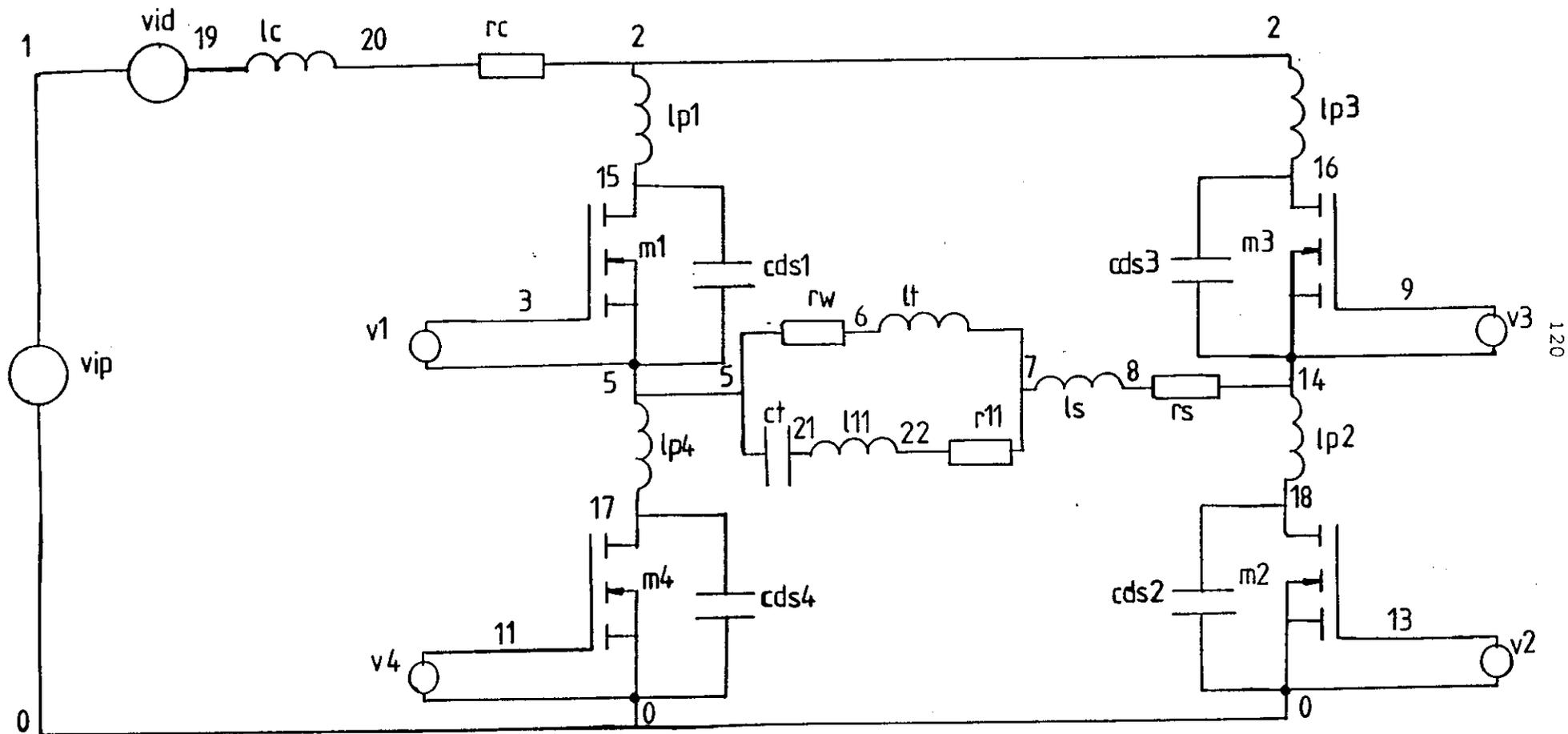


Figure 5.4 - The circuit used to model the inverter feeding a modified tank circuit.

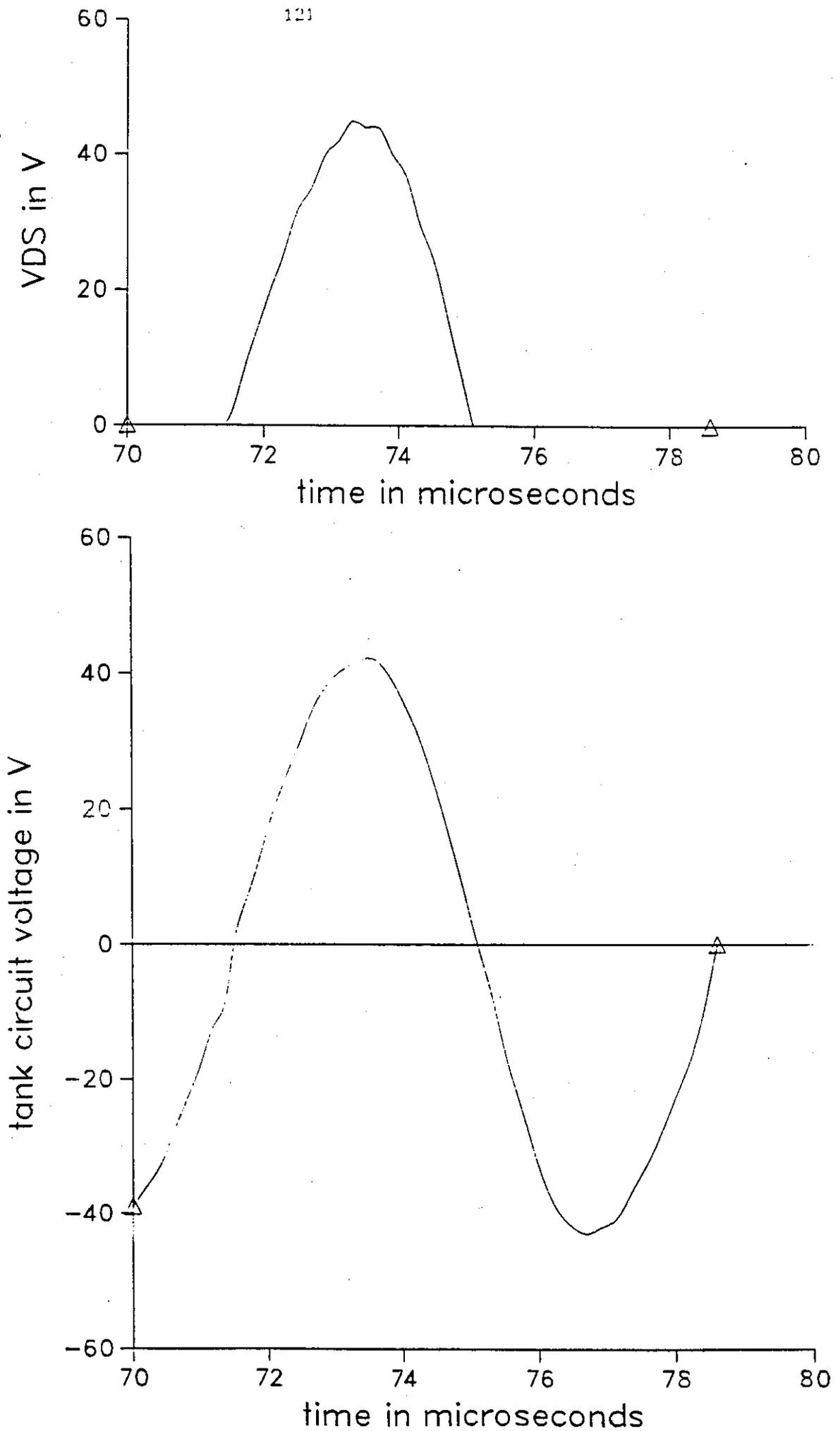


Figure 5.5 - Waveforms of drain to source voltage across and tank circuit voltage for a current fed inverter feeding a modified tank circuit

The initial conditions of voltages across capacitors and currents through inductors for the circuit in Fig. 5.4 were set to zero. The same component values as described above were used. The build up of current in the dc link and peak voltage across the drain to source of MOSFETs was monitored. The results are shown in Fig. 5.6. It can be seen from Fig. 5.6 that if MOSFETs were carrying their rated rms current in steady state conditions then their peak pulse current rating would not be exceeded during start up.

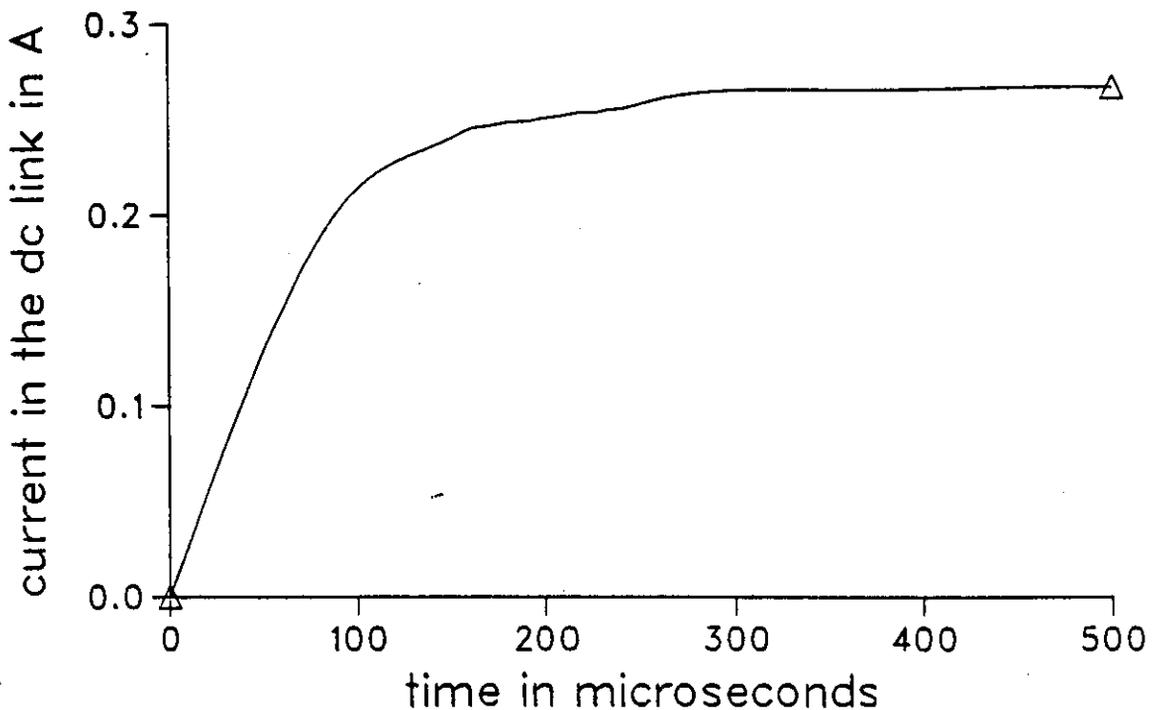


Figure 5.6 - The build up of current in the dc link immediately after switch on resulting from an analysis using SPICE.

5.5 CONCLUSIONS

Computer programmes based on the SPICE numerical package have been developed to model the operation of the induction heating power supply.

The computer simulations have produced results which closely agree with experimental waveforms.

Simulations of the current fed full bridge inverter with both a simple two element tank circuit and with a modified tank circuit have supported practical results by showing that the modified tank circuit suppresses ringing on the drain to source voltage waveform of MOSFETs.

The versatility of this package means that subsequent users may easily extend this work to analyse different matching networks or inversion bridge configurations.

CHAPTER 6MICROPROCESSOR CONTROL OF THE CURRENT FED INDUCTION HEATER

In order to investigate the use of a microprocessor in controlling a current fed induction heating supply using Power MOSFETs a proprietary microprocessor system was interfaced to the induction heater.

6.1 THE ADVANTAGES OF MICROPROCESSOR CONTROL

A microprocessor control system was incorporated into the solid state induction heating power supply in order to achieve more sophisticated power control, increased reliability and improved system efficiency. The microprocessor control system can also monitor the performance of the supply unit and carry out general supervisory tasks such as the continuous control of the temperature and the flow rate of the cooling water. (Tebb et al 1985e, 1986e, Leisten 1986).

6.1.1 Power Control

Even the most straightforward heat treatment applications require some form of process control. A microprocessor control unit can control the power output from the power supply and take it through any predetermined cycle required by the heat treatment process. Secondly, closed loop temperature or power control is also a common requirement for high frequency induction heating applications which can be more easily accommodated using a microprocessor control unit. Thirdly, in many applications the power delivered to the workcoil depends on the rate of material throughput or other external considerations. The use of a microprocessor can easily cater for such situations e.g. cap sealing.

Finally, for the more high technology applications (e.g. crystal pulling and optical fibre production) the induction heating power supply is only a small part of the process equipment and may need to interface with the supervisory control computer. The incorporation of a microprocessor in the induction heater power supply means that it can be programmed with software to support handshaking protocols used on the system bus.

6.1.2 Frequency Control

A microprocessor control system can implement a frequency hunting procedure i.e. the unit will find the desired resonant frequency of the tank circuit and adjust the output of the power supply accordingly. Operation of the power supply at the resonant frequency of the tank circuit reduces the switching and diode conduction losses in the MOSFETs and hence increases the operating efficiency of the inverter. The

subsequent reduction in the semiconductor device junction temperature improves the capability of each device to withstand transient overcurrents and hence improves the reliability of the power supply. Transient overcurrents are, of course, inherent in induction heating applications due largely to short circuits of the work coil or spurious turn-on of devices in the electrically noisy industrial environment in which these power supplies must operate.

6.2 THE MICROPROCESSOR SYSTEM

The system was manufactured by Control Universal Ltd and consisted of a Single Board Computer (SBC) and an input/output extension board called the CUBAN-8 housed in a minirack. A BBC computer was used as a software development tool.

(a) The Single Board Computer.

This is based on the 6502 microprocessor. The input/output facilities of the SBC are based on the 6522 Versatile Interface Adapter (VIA). This has 16 programmable digital input/output lines, 4 control lines and many other useful features such as two internal real time counters and a serial shift register. Any of the four control lines of the VIA can be programmed as interrupt inputs. Two speeds of vectored interrupts are provided. Either interrupt vector may be redirected to an assembly code interrupt routine written by the user and then returned to the vectored memory location. The faster interrupt servicing vector is entered before the operating system has carried out any interrupt processing. In the slower interrupt servicing routine, the user's interrupt routine is carried out after the microprocessor has checked to see if an operating system interrupt has been generated. The various programmed interrupts generated within the 6522 VIA cause flags to be set in its Interrupt Flag Register and so this can be examined by the user's interrupt routine to determine the cause of the interrupt.

(b) The CUBAN-8 input/output extension card.

A 6522 VIA chip on the CUBAN-8 provides 16 programmable input/output lines and 4 control lines as well as other features, two of which were mentioned in Section 6.2 (a). The CUBAN-8 also provides an analogue output channel and 16 multiplexed analogue input lines. The input/output capabilities of the SBC and the CUBAN-8 have not been fully utilised but if many housekeeping tasks and closed loop temperature control were needed the extra capability would be required.

(c) The BBC Computer.

A ROM was fitted into one of the spare sockets on the BBC enabling it to be used as a terminal for the SBC. The BBC's disc drive can also be used for storing programmes. Control Basic is supported by the SBC. This language is very similar to BBC Basic but has additional commands which chiefly are concerned with facilitating the input and output of information.

Once the software has been developed, programmed into an EPROM and the EPROM plugged into the SBC the SBC can operate alone without a terminal or disc drive.

(d) The inverter.

Another prototype full bridge current fed inverter was constructed so that trials on microprocessor control could be carried out in parallel with the developments on the higher power prototype. The inverter is the same design as the prototype described in Chapter 4 and both the inverter and the microprocessor development system are shown in the photograph in Fig. 6.1.

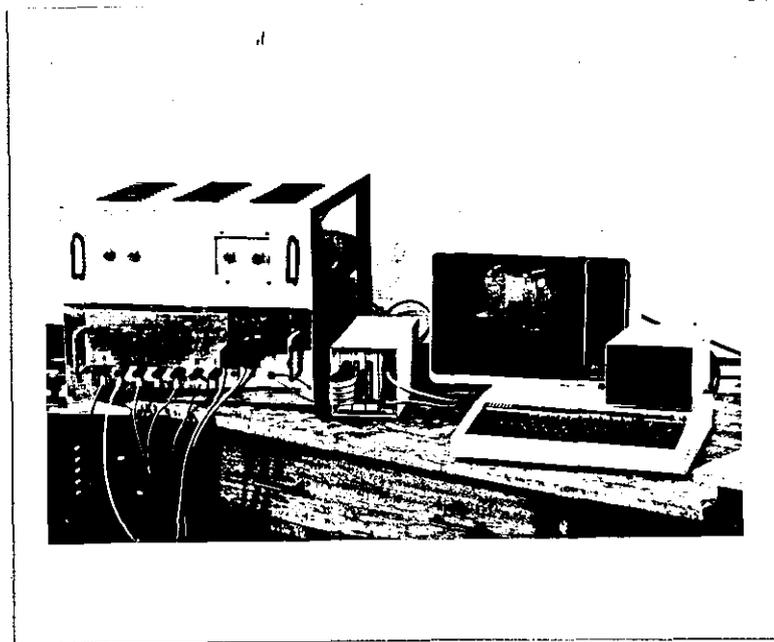


Figure 6.1 - The microprocessor development system and the inverter it controlled

6.3 THE INTERFACE CIRCUITRY

Three separate interface circuits have been designed and included in the unit. These are a thyristor firing pulse interface to the rectification bridge, a programmable frequency synthesiser and a shutdown interface. Steps have been taken to improve the noise immunity of the interfaces since the system would be expected to function in an electrically noisy environment. It is also expected that the inverter will be remote from the microprocessor and therefore long connections will carry signals between them further exacerbating the problem of interference.

6.3.1 The Thyristor Firing Sequence Circuitry

A method of sequencing thyristor firing signals was chosen which utilised the capabilities of the 6522 VIA and so saved on central processor time and external hardware. At the crossing of the red and blue phases a 16 bit word was loaded into one of the counters in the VIA (i.e. TC2) and a delay was timed out. This delay was common to all the thyristors and was determined by the 16 bit word written to the counter

TC2 by the SBC. The delay word loaded into TC2 varied the thyristor delay angle from 0° to 180° . When the counter had counted down to zero an interrupt was generated which caused a 16 bit word to be loaded into the second of the counters in the VIA (i.e. TC1). The VIA was programmed so that when TC1 counted down the most significant bit of a port (PB7) inverted. This meant that a 300 Hz clock was generated at PB7 synchronised to the interrupt generated from the count down of TC2. An 8 bit word was then loaded into the shift register in the VIA. The edges of the 300 Hz clock were used to serially shift the contents of the shift register in the VIA into an external serial-in/parallel-out shift register as shown in Fig. 6.2.

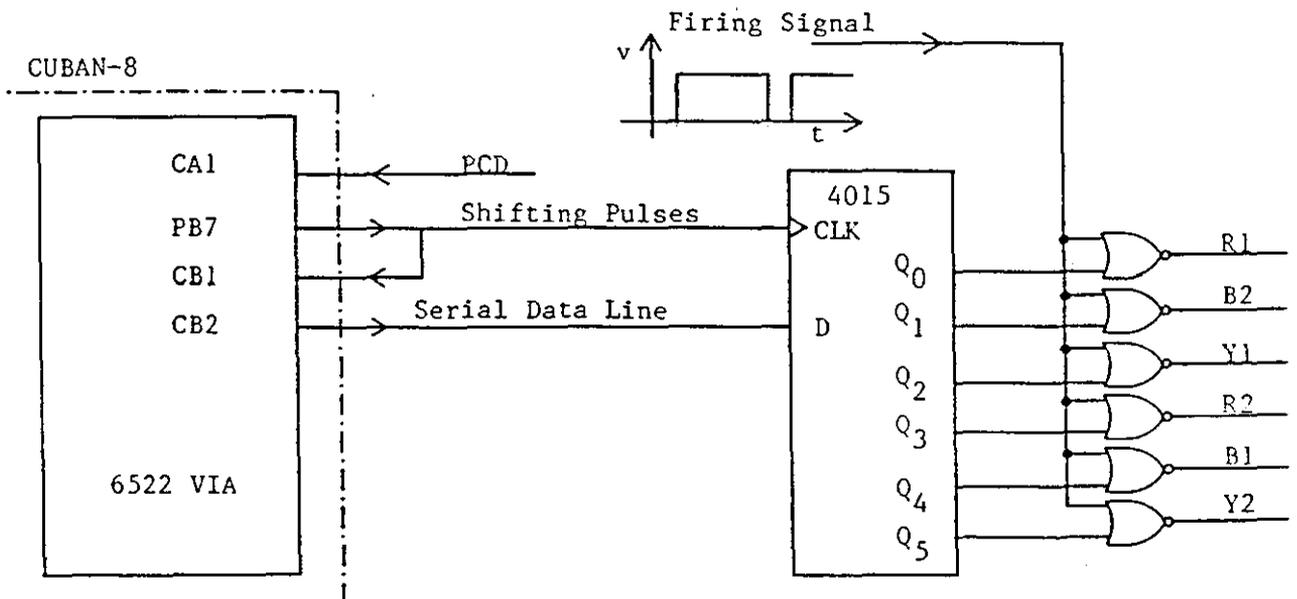


Figure 6.2 - The thyristor firing pulse generation circuit

The crossing of the red and blue phases was detected by the circuit in Fig. 3.6. One of the four control lines of the VIA was programmed to generate an interrupt on the negative going edge of the phase crossing detect signal as shown in the thyristor sequencing timing diagram in Fig. 6.3.

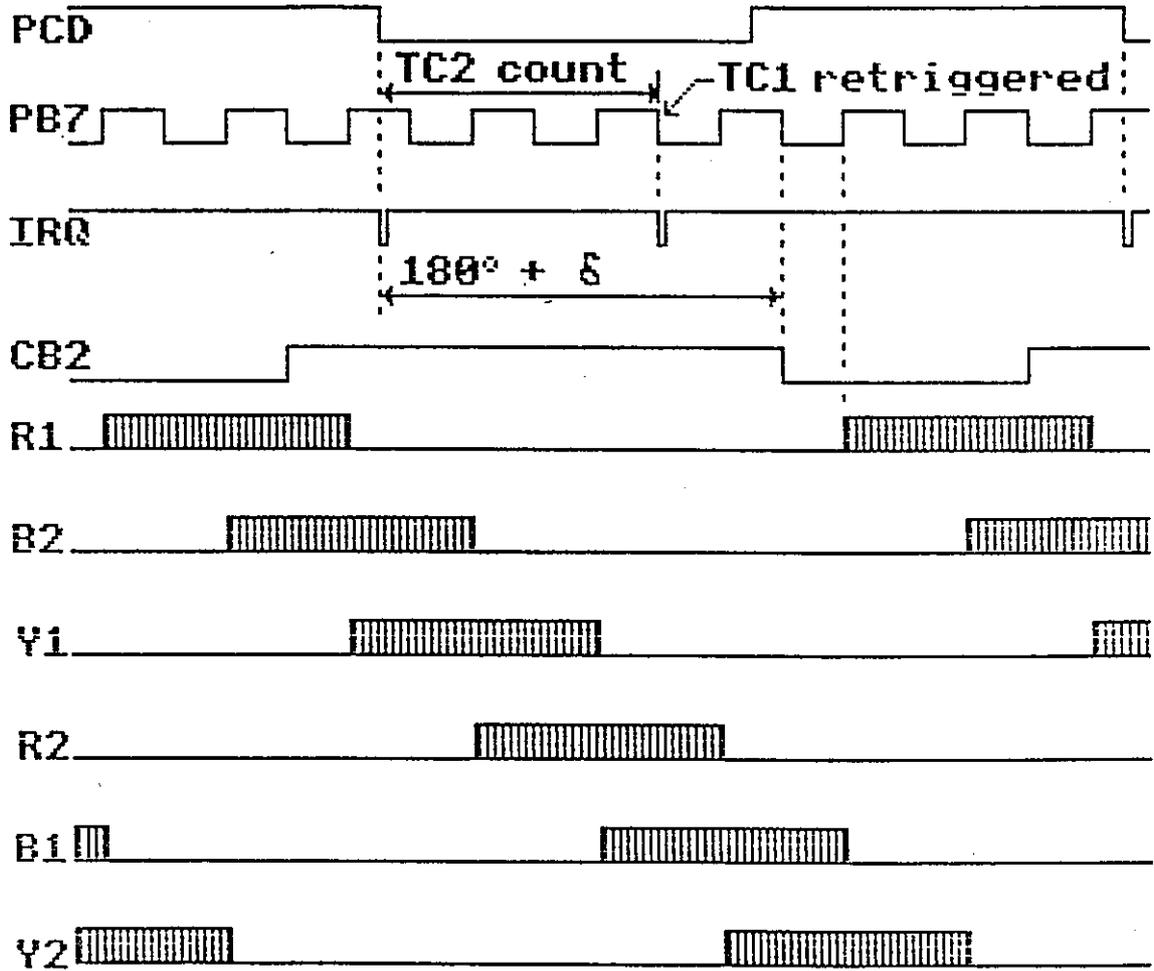


Figure 6.3 - The timing diagram for the thyristor firing pulse generation circuit.

To enable the rectification bridge to be taken into inversion in a maximum of 6.6 ms the thyristor firing signals could be combined (using XOR gates) with a shutdown signal. This way no other thyristors would be triggered after receipt of an overcurrent signal and the two thyristors conducting at that instant would remain conducting. After a maximum of 6.6 ms the output of the rectification bridge would invert, the energy would then be drawn out of the choke and the unit could be safely shut down.

6.3.2 The Programmable Frequency Synthesiser

The microprocessor needed to be able to vary the frequency of the inverter so that the inverter could remain at the required resonant frequency of the tank circuit. A Phase Locked Loop (PLL) frequency synthesiser had advantages over alternative interfaces in that its output frequency was more temperature stable and it did not need adjustment for offsets. A block diagram of the PLL frequency synthesiser is shown in Fig. 6.4.

The microprocessor supplied an 8 bit word to a programmable counter to create a divide by n function. A CMOS chip, the 4046, was used to implement the phase comparator and voltage controlled oscillator. The calculation of the low pass filter component values took into account the required stability of the synthesiser (Gardner 1979).

The transmission of the synthesised MOSFET switching signal to the induction heater distorted its duty cycle. A second PLL was used at the induction heater side of the transmission line to restore a 50% duty cycle.

6.3.3 System Condition Monitoring

Signals from detectors monitoring such parameters as water flow, water conductivity, water temperature etc could cause shutdown of the unit by connecting them to a control line which was programmed to generate an interrupt.

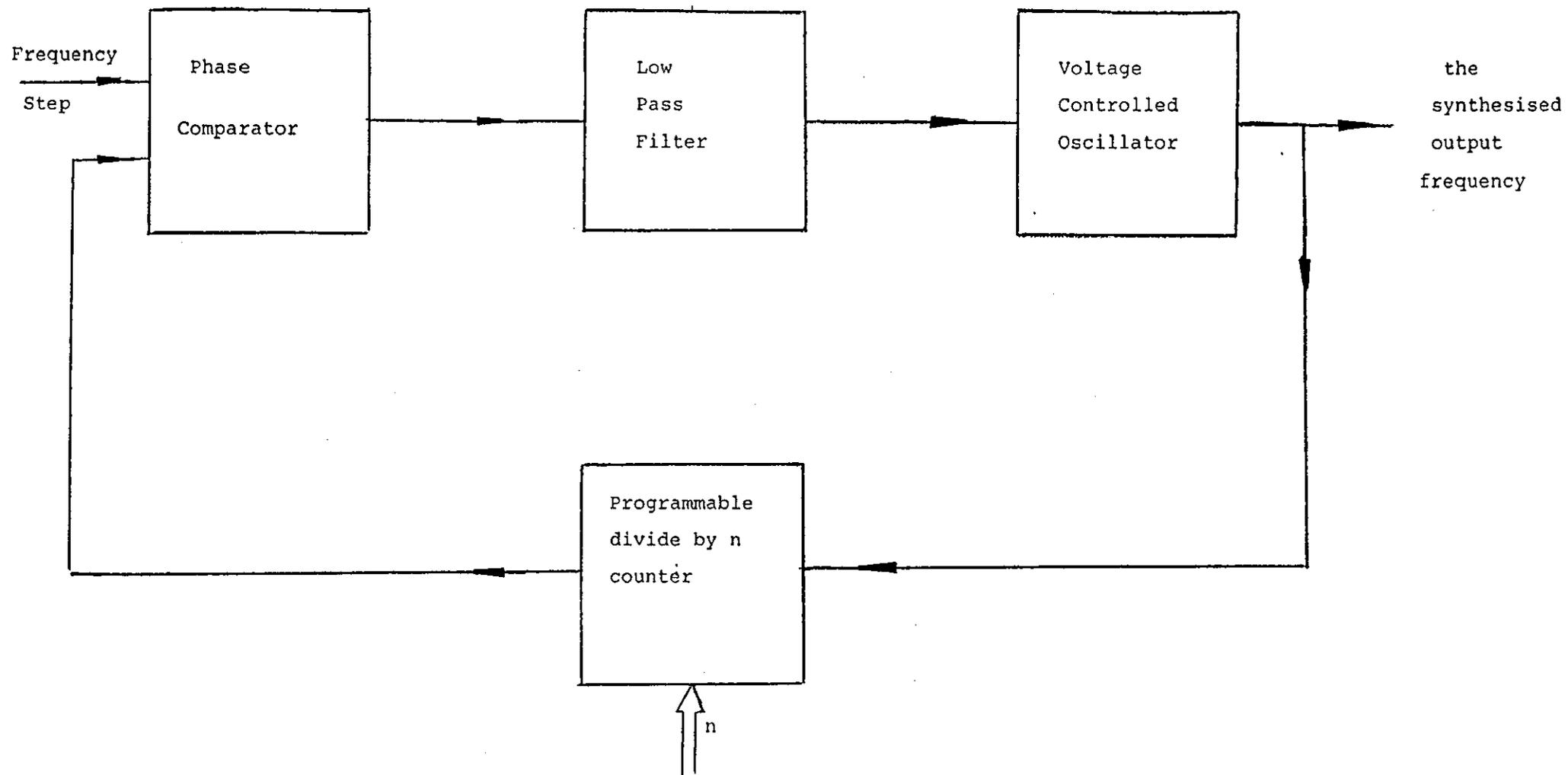


Figure 6.4 - A block diagram of a frequency synthesiser.

The microprocessor could then investigate the reason for the shutdown by examining or polling fault/event inputs. These would be lines on the ports of the VIA programmed as inputs and also connected to the fault signals. A 560 Ω resistor was inserted in these lines to limit the current in the line if they were programmed as outputs by a software fault.

An example of an interrupt driven shutdown interface has been designed and tested and is shown in Fig. 6.5 and Fig. 6.6.

As can be seen in Fig. 6.6 shutdown of the unit could be requested by pressing a push-button. The microprocessor sent a '1' to PB5 and a '0' to PB6 of a VIA to de-energise the coil of the contactor. Two lines were used to operate the contactor coil drive circuit. Except for short transient states (less than 100 μ s) which were too short to activate the contactor, the output lines of the 6522 all passed through the same unknown states during start-up. Therefore using the difference between two output lines overcame the problem of unpredictable states of ports activating the contactor during start-up.

The control line CA2 in Fig. 6.5 was programmed as an interrupt input line. When CA2 received a rising edge at its input an interrupt routine was executed. This routine involved phasing back the thyristors in the rectification bridge for 170° after phase crossover. The foreground programme detected this phasing back and de-energised the contactor coil after a delay long enough for the energy to be drawn out of the choke.

Many housekeeping tasks could be performed by the microprocessor if the inputs from remote sensors such as cooling water detectors were connected to the spare fault/event flags which could be polled regularly.

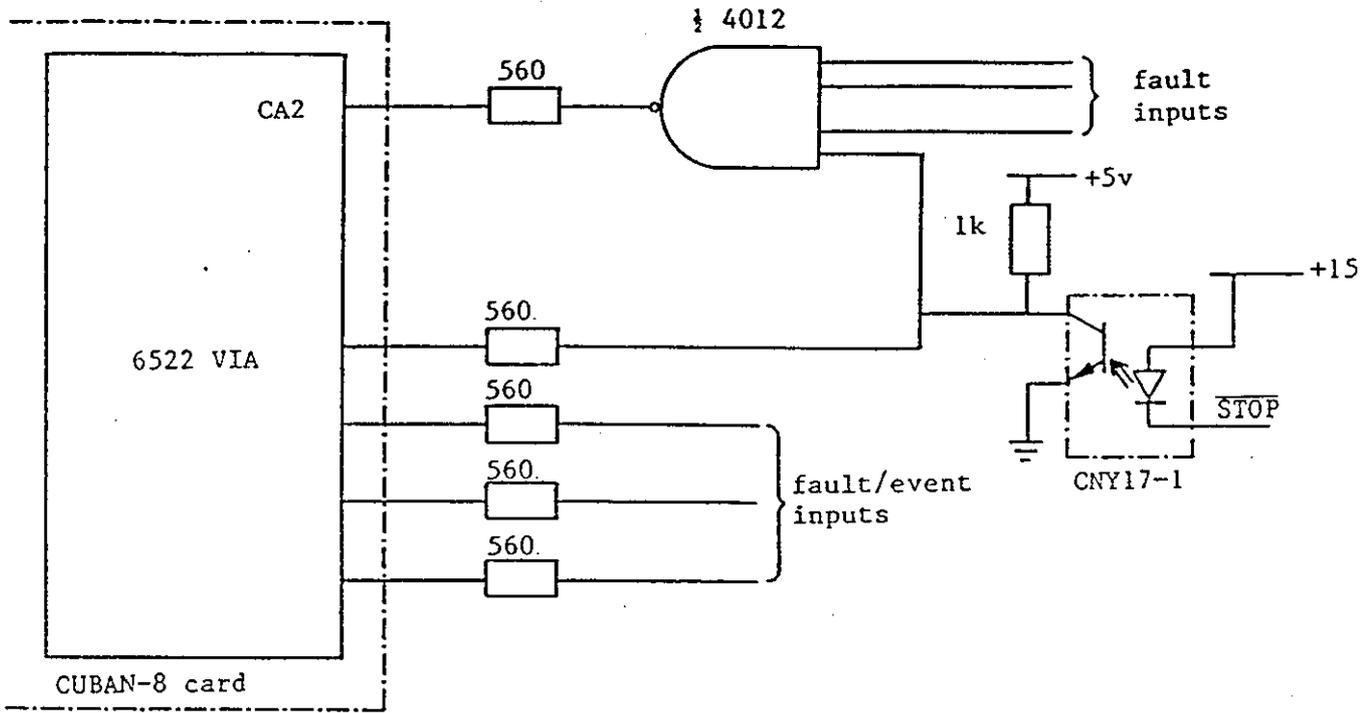


Figure 6.5 - The fault/event monitoring circuit.

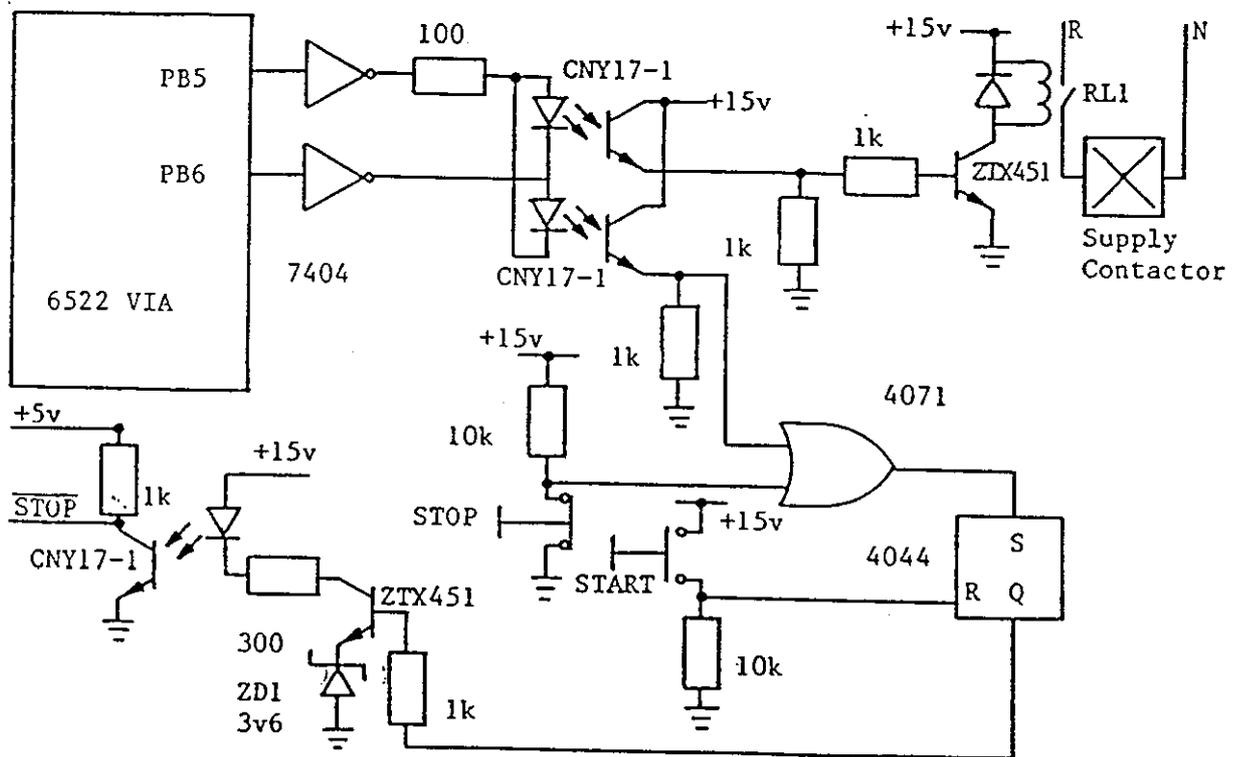


Figure 6.6 - The contactor control circuitry.

6.4 THE TRANSMISSION OF SIGNALS BETWEEN THE MICROPROCESSOR AND THE INDUCTION HEATER

Since the induction heaters often operate in electrically noisy environments careful consideration was given to the noise immunity of data highways. The signals fell into three categories for transmission.

(a) Pulsed signals.

When the thyristor firing lines were active they were pulsed with a frequency of 10 kHz and so pulse isolation transformers could be used to drive the connecting line. Screened Twisted Balanced Pair cables were used to carry the thyristor trigger pulses. The screening protected against electromagnetic and electrostatic interference and twisting the wires reduced magnetic pick-up.

The primary of the pulse transformer was driven directly from a TTL inverter. A differential pulse receiver was used at the induction heater side of the Screened Twisted Balanced Pair line.

The transmitting and receiving circuitry for the MOSFET switching signal was the same as for thyristor triggering pulses except that a higher bandwidth Operational Amplifier was used in the receiving circuit.

(b) Voltage levels that were not isolated from the microprocessor's zero volt line.

Voltage levels that were passed between the induction heater and the microprocessor, such as the shutdown signal from the contactor, were isolated by opto-isolators.

(c) Voltage levels that were isolated from the microprocessor's zero volt line.

The analogue voltage across the burden resistor of the Direct Current Current Transformer (DCCT) was isolated from the zero volt line of the induction heater's control circuit by the DCCT and so could be connected directly to an analogue input channel on the CUBAN-8 board.

6.5 POWER AND TEMPERATURE CONTROL

In many induction heating applications the control of the power input or temperature of a workpiece is of paramount importance. Using the microprocessor control system the output power level could be continuously monitored. A feedback signal from the link current was used to control the firing angle of the thyristor rectification bridge and hence the power output of the unit. A programme was written to implement closed loop power control and the flow diagram of the software is shown in Fig. 6.7. Its position in the overall software is shown in the flow diagram of the main programme in Fig. 6.8. A listing of the main programme and the subroutines is given in Appendix 7.

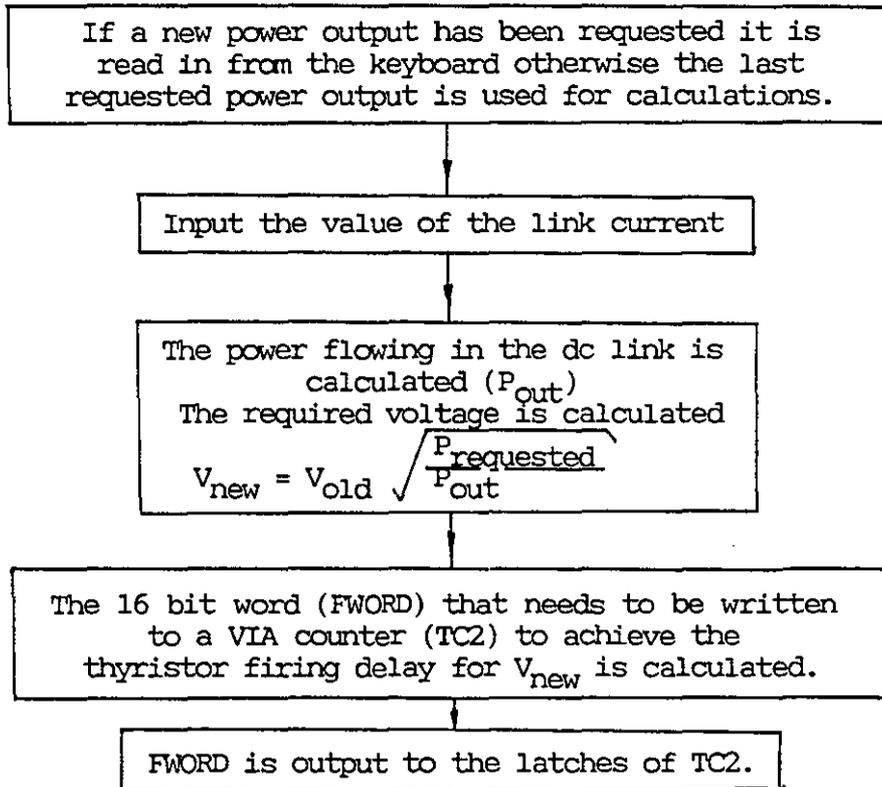


Figure 6.7 - A flow diagram of the procedure used in the main programme to implement closed loop power control.

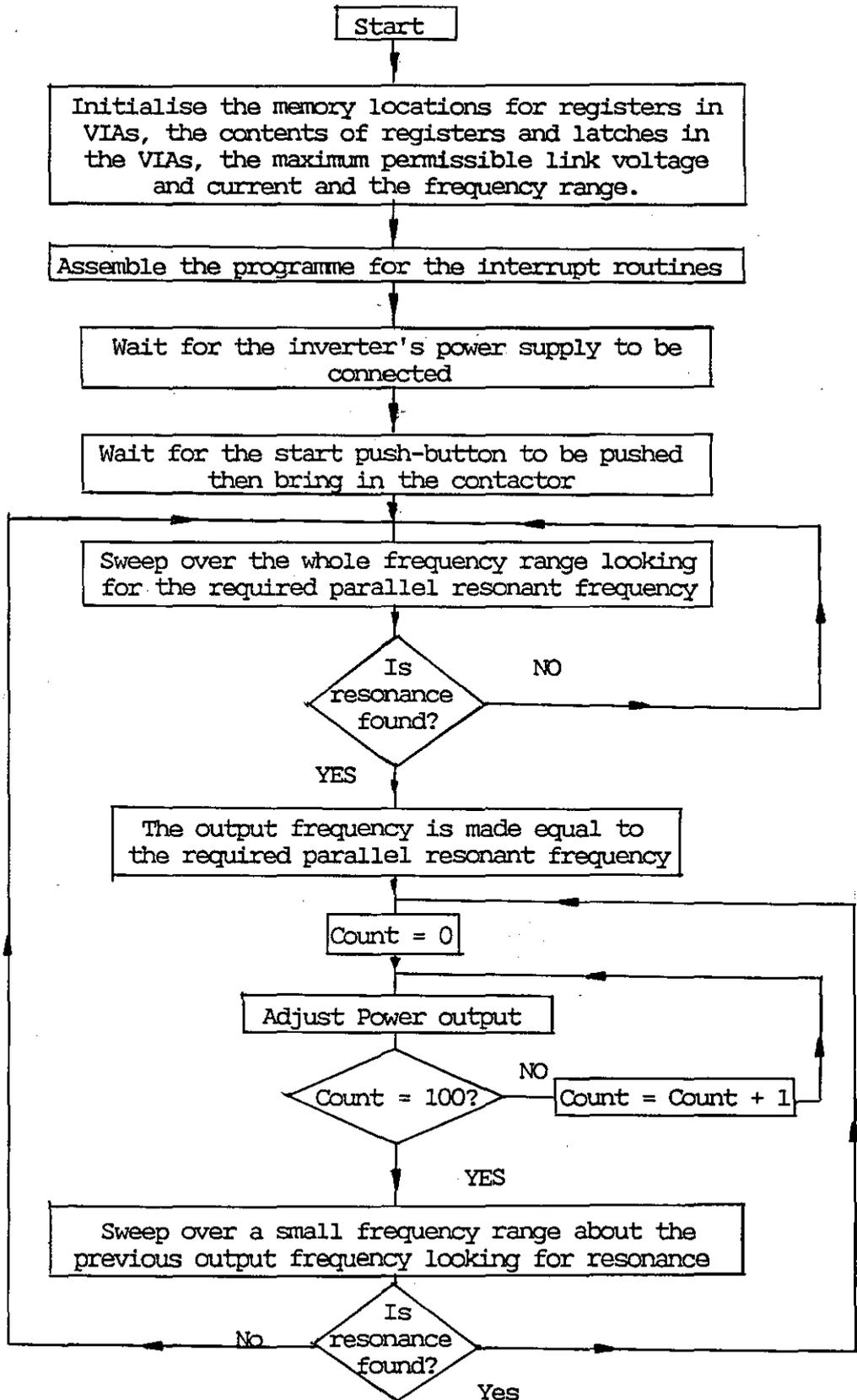


Figure 6.8 - A flow diagram of the main programme.

In this programme the required power demand was input from the keyboard of the BBC. However this could easily be modified so that a programmed heating cycle could be achieved by storing the information about the required cycle in the microprocessor's memory. This would be the case for stand-alone operation of the controller since the terminal would no longer be connected.

The power supply responded to a difference in the actual power and the required power by changing the direct voltage in the link. The time taken from a request for a different power to the time that the voltage in the link changed could be as long as 20 ms. Response times faster than 20 ms are not usually desired by induction heaters since the thermal capacity of the workpiece will damp down fast changes of workpiece temperature.

In any induction heating situation it is the power into the workpiece that needs to be controlled not the link power. An interactive programme was written to find the efficiency of the tank circuit i.e. how much of the power in the tank circuit was developed in the workpiece. The efficiency can be calculated from the unloaded and loaded Q values of the workcoil and the unloaded and loaded values of workcoil inductance (Appendix 3). A scan over the frequency range of the inverter was done when the coil was both unloaded and loaded. Details of the tank circuit capacitance, the inductor L , the number of MOSFETs in each leg and the capacitance across the drain to source of each MOSFET were requested. The efficiency was then calculated. A listing of this programme is given under PROC_Coil_Measts in Appendix 7.

Closed loop temperature control could easily be implemented by replacing the input from the DCCT by the 0-5V obtained from most pyrometers.

6.6 FREQUENCY HUNTING

Controlling the operating frequency of the power supply to keep it at the resonant frequency of the output tank circuit improved the operating efficiency and reliability of the unit. The microprocessor system was programmed to implement what is known as a frequency hunting procedure.

A flow diagram of the programme is shown in Fig. 6.9. The programme scanned the frequency range of the unit in increments of 2 kHz and found a minimum of link current (I_{\min}). The frequency at which I_{\min} occurred (F_{res}) was stored and after the scan the switching frequency of the inverter was set to F_{res} . At intervals during the operation of the unit the scan was repeated over a reduced range about the previous resonant frequency. If the resonant frequency was not found in this reduced range the whole range was scanned again. During these scans the link voltage was reduced to prevent damage to MOSFETs when the inverter was operated above resonance since they would switch on when the capacitor connected across their drain and source terminals was charged.

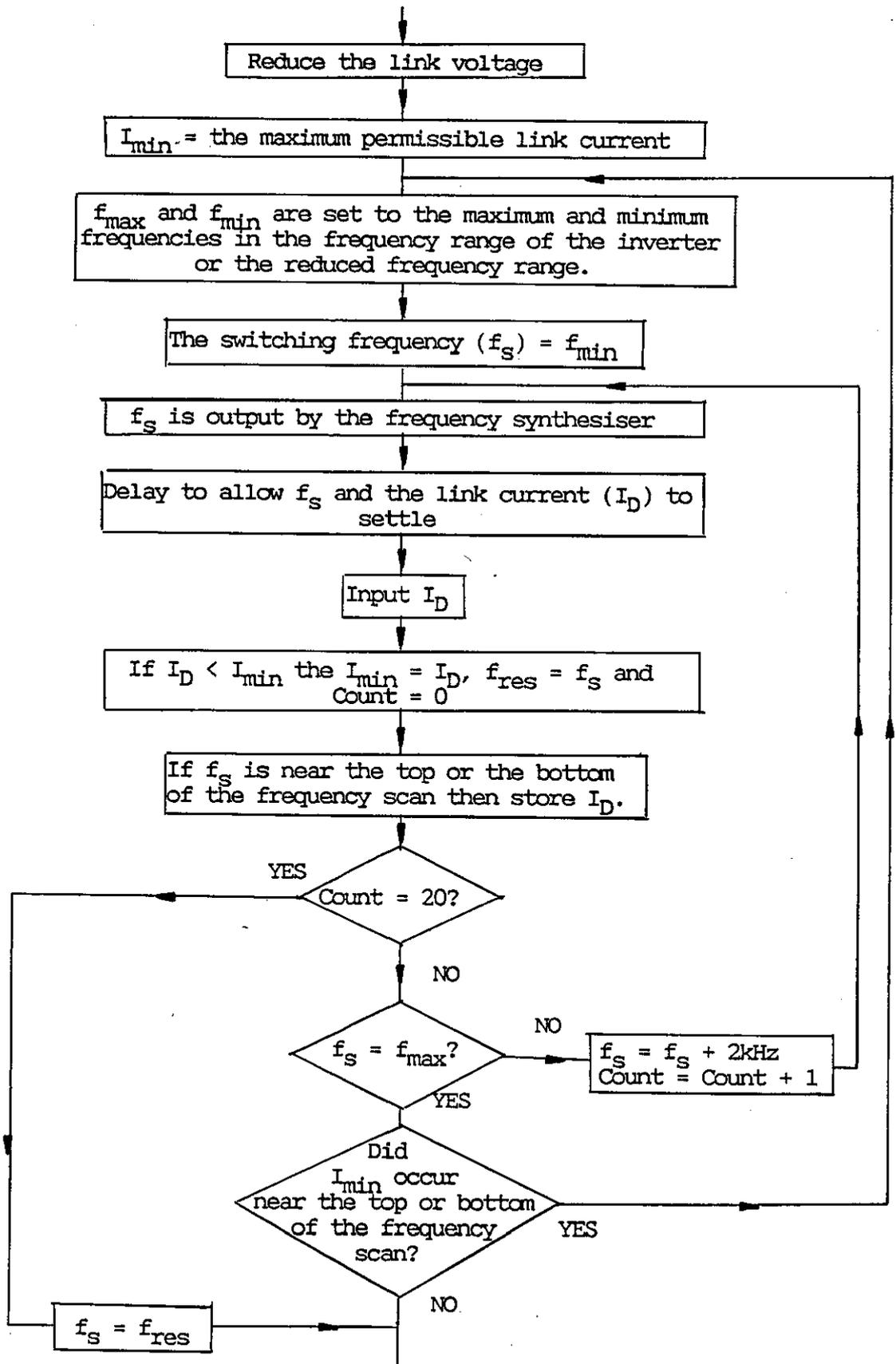


Figure 6.9 - A flow diagram of the procedure used in the main programme to implement frequency hunting.

The modified tank circuit in Fig. 4.12 has two parallel resonant frequencies. This can cause problems for methods of tuning involving only phase measurement (Bottari et al 1985) but can easily be dealt with when using a microprocessor for frequency hunting.

The higher of the two parallel resonant frequencies was associated with a higher impedance. Therefore if both the parallel resonant frequencies were in the range of the unit the simple scanning technique described above would tune the unit to the higher resonant frequency. This was not desirable since the MOSFETs would carry excessive reactive current. To tune the unit to the first parallel resonant frequency of the modified tank circuit the programme waited until there had been no change in I_{\min} for 80 kHz and then took the frequency at which I_{\min} occurred as F_{res} .

If there were no parallel resonant frequencies in the range of the scan and the tank circuit was being fed below its resonant frequencies the scan would return a value of I_{\min} at a frequency close to the top of the scan. By rejecting values of F_{res} near the top of the scan the programme coped with the case of resonance being out of the range. In this event the workcoil inductance needed to be increased to properly match the unit.

6.7 CONCLUSIONS

Three ways of ensuring good noise immunity of data channels between the microprocessor and the induction heater have been demonstrated. Two levels of priority for system condition monitoring have been used. The higher priority involved an interrupt driven response and the lower one involved polling of input lines. The interface circuitry required to implement an interrupt driven alarm has been tested. How the monitoring system could be extended to manage many inputs has been outlined.

Frequency hunting has been successfully implemented and precautions that need to be taken to avoid the unit tuning itself to undesired resonant frequencies has been described.

Both the hardware and software for closed loop power control have been developed. This work can easily be extended to closed loop control of temperature and methods of implementation have been outlined.

CHAPTER 7
THE COMMERCIAL PROTOTYPE

In order to learn more about the required performance of a current fed inverter in the industrial situation a commercial prototype was designed and constructed. This unit underwent trials in industry for a period of 6 months.

7. THE COMMERCIAL PROTOTYPE

There is a large demand for relatively low power units for a chemical separation application. Use was made of this commercial interest so that a 1 kW single phase unit could undergo trials in industry. A single phase unit is easier to manufacture since it has less components and so made the transfer of technology to the sponsoring company easier.

7.1 THE CHEMICAL SEPARATION PROCESS

Only a few details of the process can be given since it is commercially secret. The purpose of the process is to separate two gases. The gases have different boiling points so they are cooled to cryogenic conditions so that they are both in the liquid phase. The temperature of the liquified gases is then raised by 100°C using induction heating to evaporate off one of the gases. Induction heating was used because heat is developed in the containment vessel and passes mainly to the liquified gases. Excess heat dissipated in the cryogenic chamber is removed by circulating liquid helium in the chamber. This cooling system is expensive so stray heating is kept to a minimum.

The gases were contained in a stainless steel container which was a cylinder sealed at both ends except for gas inlet and outlet tubes at the top of the chamber. The height of the cylinder was 960 mm and its diameter 180 mm. A 60 turn workcoil made from 6 mm copper tubing which was 860 mm long and had an internal diameter 190 mm surrounded the cylinder. The workcoil was cooled by passing liquid helium through it. The cylinder and the coil were contained in a cryogenic chamber.

Measurements were made on the workcoil using a Hewlett-Packard HP-4192A Impedance Analyser. The results are shown in Table 7.1. The purpose of measuring the electrical parameters with the workcoil both loaded and unloaded is to calculate the efficiency and the impedance at resonance of possible matching circuits. By measuring the parameters at various frequencies the frequency of the maximum workcoil efficiency can be found. Alternatively the frequency with the best efficiency which enables a given power to be developed in the workcoil can be found.

Frequency (kHz)	Inductance		Q		Efficiency of the workcoil
	Unloaded (μH)	Loaded (μH)	Unloaded	Loaded	
1	153	49	18	2	0.65
10	151	48	65	6.2	0.70
20	150	47	152	9.5	0.80
50	150	45	192	15.2	0.73
80	150	45	196	18.4	0.68
100	150	45	167	20.5	0.59
150	150	44	141	24.7	0.40

Table 7.1 - Measurements of the electrical parameters of the 60 turn chemical separation coil.

7.2 THE DESIGN AND CONSTRUCTION OF THE SINGLE PHASE COMMERCIAL PROTOTYPE

The specification of the single phase commercial prototype was that it had to be able to develop 800 W in the stainless steel container. The workcoil voltage could not exceed 150V because there was a danger of arcing in the cryogenic chamber. One side of the workcoil was earthed.

7.2.1 The Rectification Stage

Since the maximum workcoil voltage was 150V a 230V:130V step down transformer was used at the input to the rectification stage as shown in the block diagram of the unit in Fig. 7.1. An isolating transformer was used since one side of the workcoil was earthed. Bought-in modules were used wherever possible to facilitate production. Therefore a single phase thyristor controller and a full wave rectification module were used to implement power control and rectification since these were available in standard modules.

7.2.2 The DC Link

A DCCT was used to sense the dc link current. An air-cored choke of value 10 mH was used to protect the MOSFETs if the workcoil was short circuited. The maximum time that can elapse between an overcurrent occurring in the dc link and the inversion of the dc link voltage is 10 ms for a single phase inverter. The choke would have to restrain the rate of rise of link current during this period. Rather than incur the penalty of a heavy choke a 10 mH choke was used and a crowbar thyristor was installed. Under conditions of severe overcurrent the crowbar thyristor was fired which caused a semiconductor fuse to operate (Evans 1982) and remove the link voltage.

A 1.5 μ H air-cored inductor was connected in series with the crowbar thyristor to limit the rate of rise of current at turn-on to less than 150A/ μ s. A freewheeling diode was connected in parallel with the 1.5 μ H inductor and the crowbar thyristor. The freewheeling diode provided a path for the link current after the semiconductor fuse had operated. The crowbar thyristor and its firing circuitry were positioned away from the inversion bridge to prevent electrical interference causing

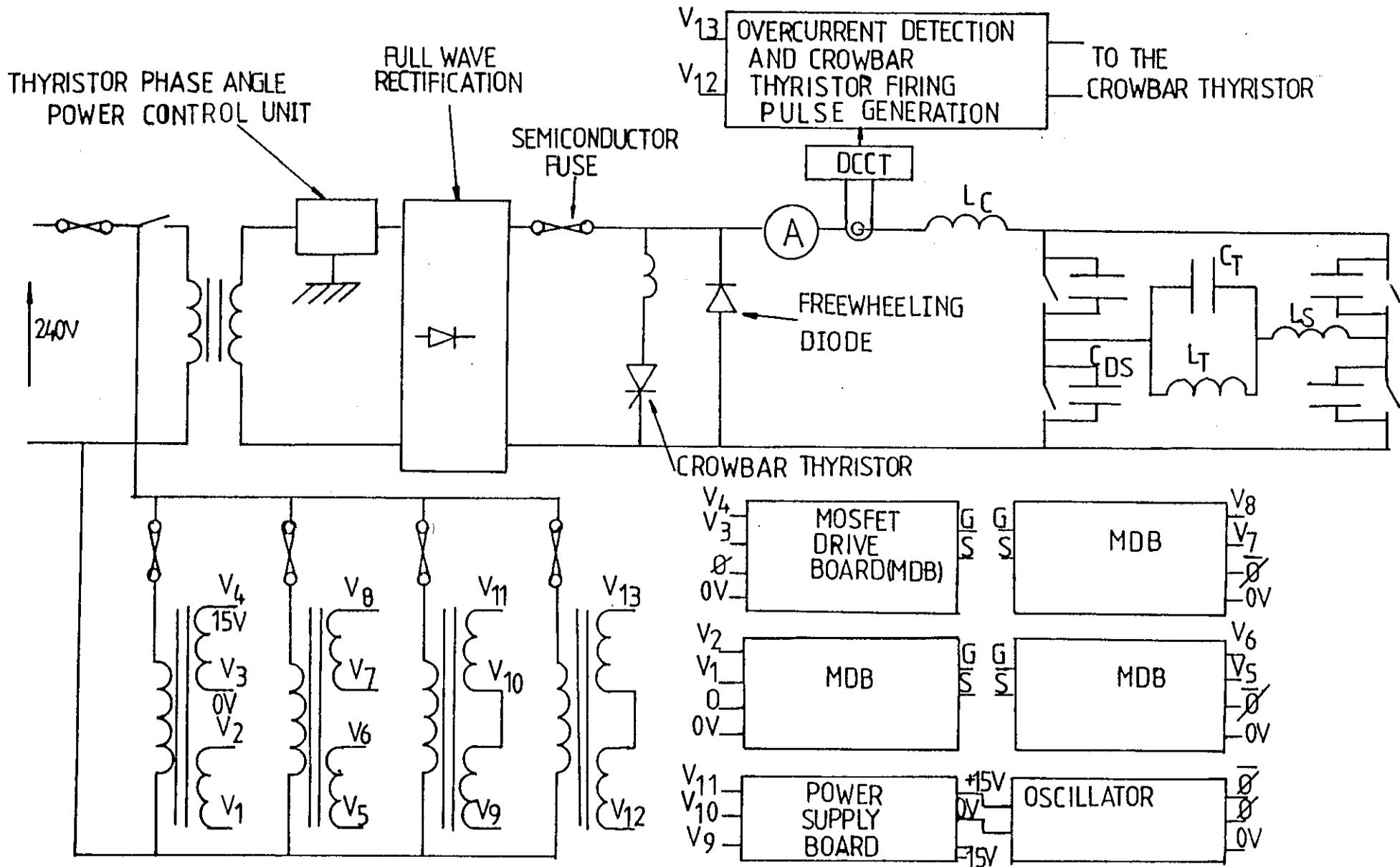


Figure 7.1 - A schematic diagram of the single phase commercial prototype.

spurious triggering of the crowbar thyristor.

7.2.3 The Inversion Stage

Two MOSFETs type IRF450 were connected in parallel in each leg of a full bridge. The voltage rating of the IRF450 is 500V and gave flexibility of matching. This allowed the tank circuit to be fed with inductance connected in series. The series inductance and the drain to source capacitance of MOSFETs would form a series resonant circuit. Thus when the voltage across the workcoil was 150V the voltage across the MOSFETs could be much larger. The MOSFETs were mounted on 1.1°C/W heatsinks; two MOSFETs per heatsink. The MOSFET drive circuitry used is shown in Fig. 3.6 and Fig. 3.7.

7.2.4 Matching

The power developed in a workpiece by a workcoil of inductance L_T , is given by Eqn. 7.1.

$$\text{Power} = \frac{V_{LT}^2 \omega \eta_{wc}}{L_T Q_L} \quad (7.1)$$

where V_{LT} is the voltage across the workcoil and η_{wc} is the efficiency of the workcoil. By substituting values of loaded inductance, efficiency and loaded Q from Table 7.1 into Eqn. 7.1 it was realized that a frequency between 10 kHz and 20 kHz was needed for a power input to the coil of 1 kW.

The workcoil was connected in parallel with a tank circuit capacitance of 5.0 μF . A 5.2 μH air-cored inductor was placed in series with the tank circuit to suppress ringing. Ceramic capacitors of value 100 nF were connected across the drain and source terminals of each MOSFET. The calculated resonant frequency of the tank circuit was 10.0 kHz.

This matching circuit is similar to the modified tank circuit in Fig. 4.12 except that the inductor L'' has been taken out. An inductor is connected between the tank circuit and the terminals of the inverter. This increases the value of L_S . The matching circuit is shown in Fig.

7.1 and can be analysed in a very similar way to the analysis of the modified tank circuit in Section 4.2.3. The advantages of the circuit in Fig. 7.1 over the modified tank circuit is that the inductor L_S does not carry as much reactive current as L'' in Fig. 4.12. The circuit in Fig. 7.1 is therefore more efficient. The main disadvantage of the circuit in Fig. 7.1 is that a large inductive impedance is presented to the fundamental component of the load current as well as to higher frequency harmonics. This means that larger values of drain source capacitance are needed to reduce ringing. The arrangement in Fig. 7.1 was preferred for the chemical separation application since it was difficult to cool inductor L'' . There was no water cooling or compressed air supply already connected to the inverter and the workcoil was remote from the inverter.

7.2.5 Analysis of the Inverter Using SPICE

The circuit in Fig. 5.2 was used to analyse the operation of the single phase inverter. The results are plotted in Fig. 7.2. From Fig. 7.2 the following points are worthy of note.

- (a) There is no excessive ringing on the drain to source voltage waveform of MOSFETs.
- (b) The average current in the dc link is 6.45A.

7.2.6 Construction

The layout of the unit was designed so that parasitic lead inductances in the inversion section were kept to a minimum. Sensitive control circuitry was positioned away from the fast switching inversion section.

A dc ammeter was connected in the dc link and mounted on the front panel. This was used to find a minimum of dc link current as the inverter switching frequency was varied. When the dc link current was a minimum the unit was tuned to one of the parallel resonant frequencies of the tank circuit.

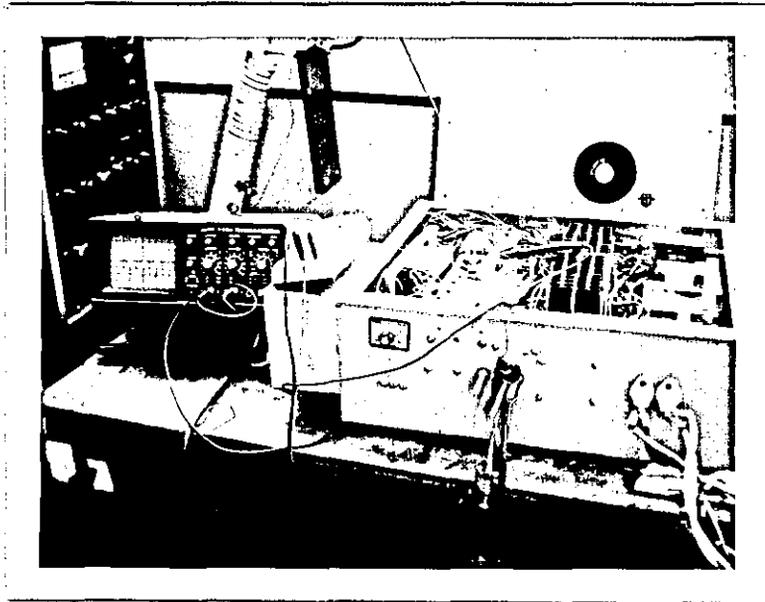


Figure 7.3 - The single phase commercial prototype.

The unit was housed in a cabinet as shown in the photograph in Fig. 7.3. The electronics were mounted on an aluminium base plate. The aluminium plate and the electronics could be lifted out. Connecting leads between the electronics and the front panel were long enough for the electronics to be placed beside the cabinet. This facilitated testing of the unit.

7.3 THE TRIALS ON THE PROTOTYPE

The unit was matched to the workcoil as described in Section 7.2.4. The link voltage was set to 30V to prevent large current spikes in MOSFETs during the initial tuning procedure. These current spikes occurred when the tank circuit was fed above its resonant frequency and so MOSFETs switched on when the externally connected drain source capacitance was charged. The switching frequency of the inversion stage was varied and the link current monitored. The link current was a minimum at a parallel resonant frequency which was 10 kHz. The drain to source waveform of a MOSFET was observed as the switching frequency was reduced below the tank circuit resonant frequency. At 9.5 kHz a period of conduction of the parasitic diode inherent in the structure of the MOSFET was seen on the drain to source voltage waveform before the

MOSFET turned on. The MOSFET could therefore be guaranteed not to be switching on when the external drain source capacitor was charged.

For a period of six months the unit was used repeatedly at the chemical separation plant for stretches of up to seven hours and typically greater than three hours. Typically a link voltage of 120 V and a link current of 6 A (and therefore a link power of 720 W) were used. This link current was predicted using SPICE. A link power of 1 kW was used for similar stretches of time. The ease of power control was demonstrated since programmed heating-up cycles were followed. The unit was subjected to several severe overcurrents and the crowbar circuit acted to save MOSFETs on all occasions. The operator inadvertently fed a tank circuit which had a resonant frequency of 10 kHz at a frequency of 20 kHz. This state lasted for 7 hours with a link current of 8 A. Although the unit became very hot the MOSFETs survived illustrating the excellent pulse to average current carrying capabilities of MOSFETs.

7.4 CONCLUSIONS

The ability of the unit to function for long periods has been well demonstrated. Furthermore the robustness of the power supply has been proved. Even though the unit was operated above the resonant frequency, which caused the MOSFETs to switch on when externally connected drain source capacitance was charged, the MOSFETs were not destroyed. This robustness was attributable to the excellent peak to average current carrying capability of the transistors. There are two other ways in which large current spikes can be caused in MOSFETs. Firstly the workcoil may become disconnected. This is unlikely but an induction heating power supply needs to be able to cope with this event. In this situation the link current will charge up the drain source capacitance of MOSFETs and the tank circuit capacitor. When MOSFETs switch on they will be subjected to current spikes. Secondly if the unit is switched on when there is no workcoil connected then energy will be stored in drain source capacitors and then dissipated in the transistors.

The ability of a current fed circuit to shut down safely under short circuit conditions was demonstrated. The crowbar operated successfully on many occasions. There were no problems of the crowbar being spuriously triggered. This was because the sensitive crowbar firing circuitry was placed away from the MOSFETs.

The unit was matched to the workcoil without the use of a matching transformer. This reduced the cost of the unit and also improved the efficiency. Ringing on the drain to source voltage waveform of MOSFETs was suppressed successfully by connecting a coil in series with the tank circuit.

CHAPTER 8
CONCLUSIONS

The achievements of the work are outlined. Recommendations for the design of a 20 kW unit are given.

8. CONCLUSIONS

The use of the current fed topology for induction heating between 100 and 400 kHz has been developed from the stage of being just an idea right through to the stage when a commercial prototype has worked in industry for 6 months. Units based on the design of the commercial prototype have now been delivered to the customer. A modified tank circuit has been incorporated in the output stage of the inverter. This novel form of matching greatly reduces ringing on the drain to source of MOSFETs. The modified tank circuit also has other important advantages such as obviating the necessity for diodes connected in series with MOSFETs. Other achievements have been the incorporation of a microprocessor for power control and frequency hunting and the use of SPICE to analyse the operation of the inverter. Many of the achievements of the work in this thesis have been published in learned publications. For completeness a list of the achievements is given in this chapter. The work has been carried out with a view to designing a 20 kW unit. Recommendations for the design of larger units are detailed.

8.1 ACHIEVEMENTS

The work described in this thesis includes the following achievements.

- (1) An assessment of the suitability of current fed and voltage fed topologies for induction heating between 100 and 400 kHz at power levels up to 20 kW based on a literature search was done.
- (2) A prototype voltage fed inverter was fed into a resonant tank circuit and its performance critically assessed.
- (3) A prototype cycloinverter was designed, constructed and tested. Its performance was critically assessed.
- (4) A prototype current fed full bridge inverter was designed, constructed and tested. Its performance was critically assessed.

- (5) The experience with the prototype inverters confirmed that the current fed inverter was the most suitable for induction heating between 100 and 400 kHz at power levels up to 20 kW. A higher power prototype was designed, constructed and tested.
- (6) An assessment of different switch configurations for the inversion bridge was done. The full bridge was found to be the most suitable for this application.
- (7) A layout of the inversion bridge that greatly reduced parasitic lead inductances was developed.
- (8) A matching technique involving a modified tank circuit was adopted which suppressed ringing on the drain to source voltage waveform of MOSFETs.
- (9) The modified tank circuit prevented the MOSFETs carrying the full circulating current of the tank circuit when the tank circuit was fed off resonance and during the short overlap period when all the MOSFETs were on. This obviated the need for diodes connected in series with the MOSFETs.
- (10) The modified tank circuit reduced the requirements for expensive tank circuit capacitors to resonate a given workcoil at a given frequency.
- (11) A design procedure for the components in the modified tank circuit was developed. This procedure was programmed onto a BBC microcomputer.
- (12) The higher power prototype current fed inverter successfully fed into two commercially significant workcoils.
- (13) A propriety microprocessor system was used to implement closed loop power control.

- (14) The propriety microprocessor system was also used to implement frequency hunting. This was used to keep the inverter tuned to the required resonant frequency of the tank circuit.
- (15) SPICE was used to analyse the inverter under the following conditions:-
- (a) When feeding a simple two element tank circuit
 - (b) When feeding a modified tank circuit
 - (c) When feeding a two element tank circuit in series with an inductor with external capacitance connected across the drain to source of MOSFETs.
- (16) A commercial prototype current fed inverter was designed and constructed. This unit worked successfully in a chemical separation plant for over 6 months.

8.2 RECOMMENDATIONS

A comparison between the estimated costs of MOSFET power supplies and the costs of valve power supplies indicated that there is a crossover point above which the MOSFET power supply is more expensive. This is because the cost of the valve does not increase pro rata with the power handling capability. At present prices the crossover point is at about 30 kW. Recommendations are now made concerning the design of a 20 kW unit.

Semiconductor fuses need to be used to protect the thyristors in the rectification bridge. Should one of these fuses operate to clear a fault then the current in the choke would be interrupted. The subsequent voltage spike could cause damage to MOSFETs. To prevent this a freewheeling diode should be connected across the output of the rectification bridge. This will mean that the rectification bridge cannot be phased back into inversion to draw energy quickly out of the choke. Instead the current in the dc link will have to freewheel until it decays. The energy stored in a 10 mH choke carrying 100 A is only 50 J so it could be dissipated in just the series resistance of the

choke and the on-resistances of MOSFETs in a few seconds. (Tebb et al 1986f).

Hall effect devices could be used instead of a DOCT to sense the current in the dc link. Hall effect devices do not have the problem of notches in the output waveform. The output of a DOCT has notches which occur at the zero crossing of the excitation voltage. These notches are caused by energy stored in the cores of the DCCT. Filtering of these notches degrades the frequency response of current detection. A Hall effect device, type LT 80-P has been successfully used on the unit. The use of a Hall effect device is therefore recommended.

The use of a crowbar circuit on the unit would reduce the size of the choke in the dc link. This would reduce the mass and volume of the unit. The use of many smaller chokes instead of one choke would reduce problems of dynamic unbalance. Each choke would be connected to the output of the rectification bridge and to three MOSFETs. If one MOSFET turned on before another the maximum current that it would carry would be a fraction of the total current in the dc link. Since MOSFETs have an excellent peak to average current carrying capability devices would not be damaged by this unbalance. Thus problems associated with dynamic unbalance would be overcome.

APPENDICES

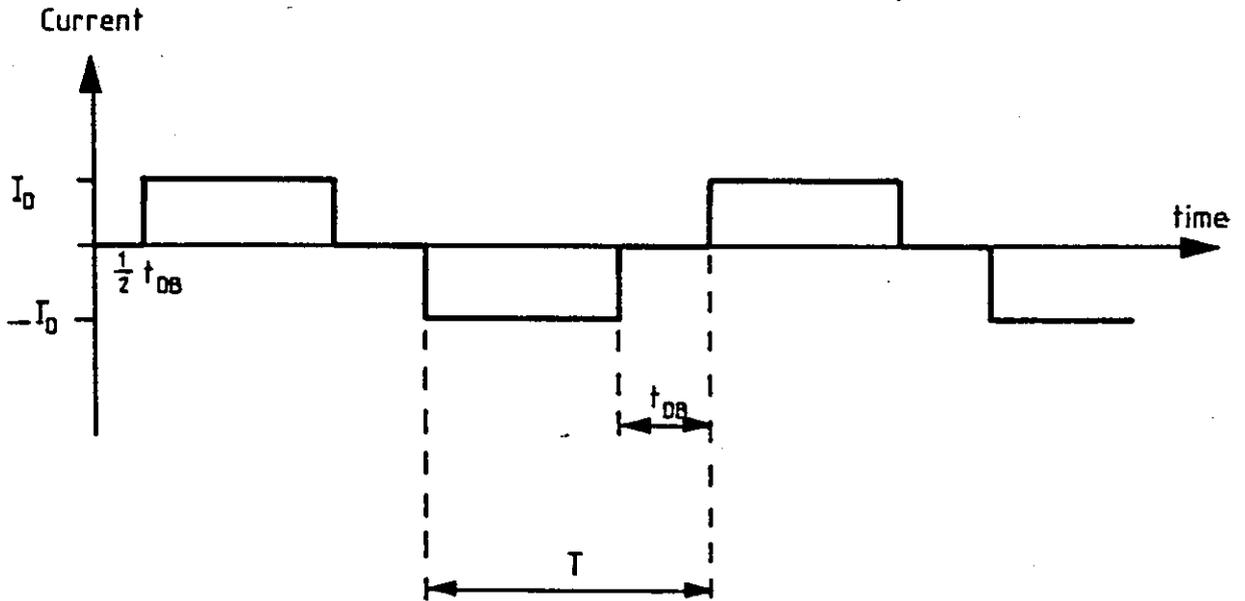
APPENDIX 1A FOURIER ANALYSIS OF THE LOAD CURRENT

Figure A1.1 The waveform of the current passed through the tank circuit in a current fed inverter.

The waveform of the load current shown in Fig. A1.1 can be represented by the series in Eqn. A1.1.

$$i_L = \sum_{n=1}^{\infty} b_n \sin \left[\frac{2n\pi t}{T} \right] \quad (\text{A1.1})$$

where b_n is a constant and is given by Eqn. A1.2.

$$b_n = \frac{2}{T} \int_{-T/2}^{T/2} i_L \sin \left(\frac{2n\pi t}{T} \right) dt \quad (\text{A1.2})$$

Integrating the right hand side of Eqn. A1.2 produces an expression for b_n given in Eqn. A1.3.

$$b_n = \frac{2I_D}{n\pi} \left[\cos \left[\frac{n\pi}{T} t_{DB} \right] - \cos \frac{n\pi}{T} (T-t_{DB}) \right] \quad (\text{A1.3})$$

APPENDIX 2THE DERIVATION OF AN EXPRESSION FOR THE RATE OF RISE OF CURRENT IN THE DC LINK WHEN THE WORKCOIL IS SHORT CIRCUITED

When the workcoil is short circuited the choke limits the rate of rise of current in the dc link. The greatest rise in current will occur if there is zero delay angle for the firing of the thyristors and the short circuit happens immediately after a thyristor has been fired. Fig. A2.1 shows the thyristors in the rectification bridge and the voltage waveforms of the three phase supply. In Fig. A2.1 the voltages at the cathode and anode terminals of the rectification bridge are shown in thick lines. Thyristor T_1 is fired at $\alpha = 0^\circ$ in Fig. A2.1. The workcoil is then short circuited. Thyristors T_1 in the red phase and T_6 in the yellow phase are now conducting. Thyristor T_2 in the blue phase is not fired 3.3 ms after T_1 but is delayed by $> 90^\circ$. The volt second area absorbed by the choke can be readily seen in Fig. A2.1 and is given by Eqn. A2.1.

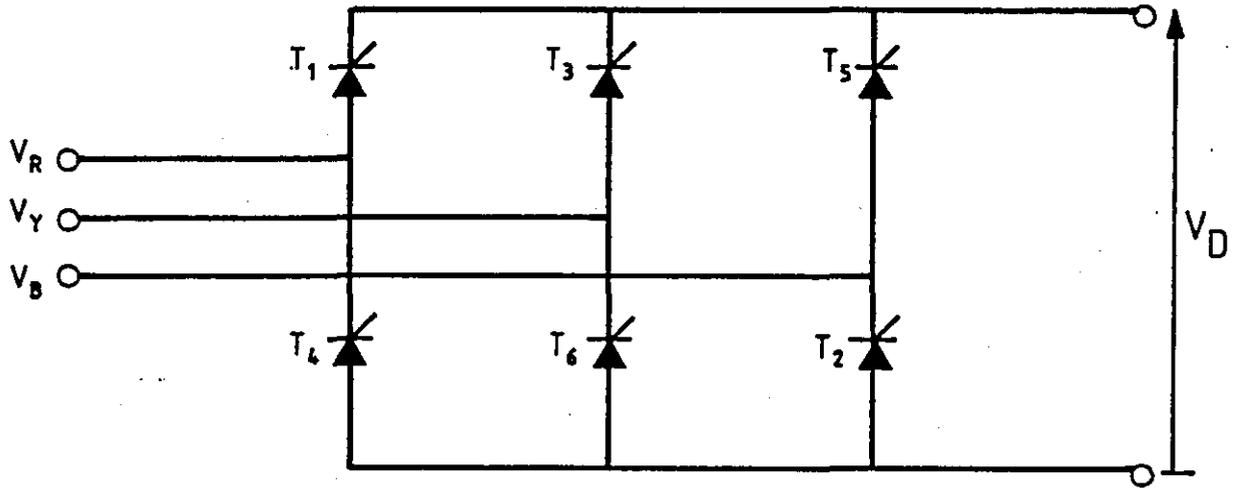
$$\begin{aligned} t &= 150 \cdot \frac{20}{360} \text{ ms} \\ \text{The volt second} &= \int_{t=30 \cdot \frac{20}{360} \text{ ms}}^{\hat{V}_p} [\sin(\omega t) - \sin(\omega t - \frac{2\pi}{3})] dt \quad (\text{A2.1}) \\ \text{area} & \end{aligned}$$

Where \hat{V}_p is the maximum phase voltage of the three phase supply. Integrating Eqn. A2.1 and substituting the limits in produces Eqn. A2.2.

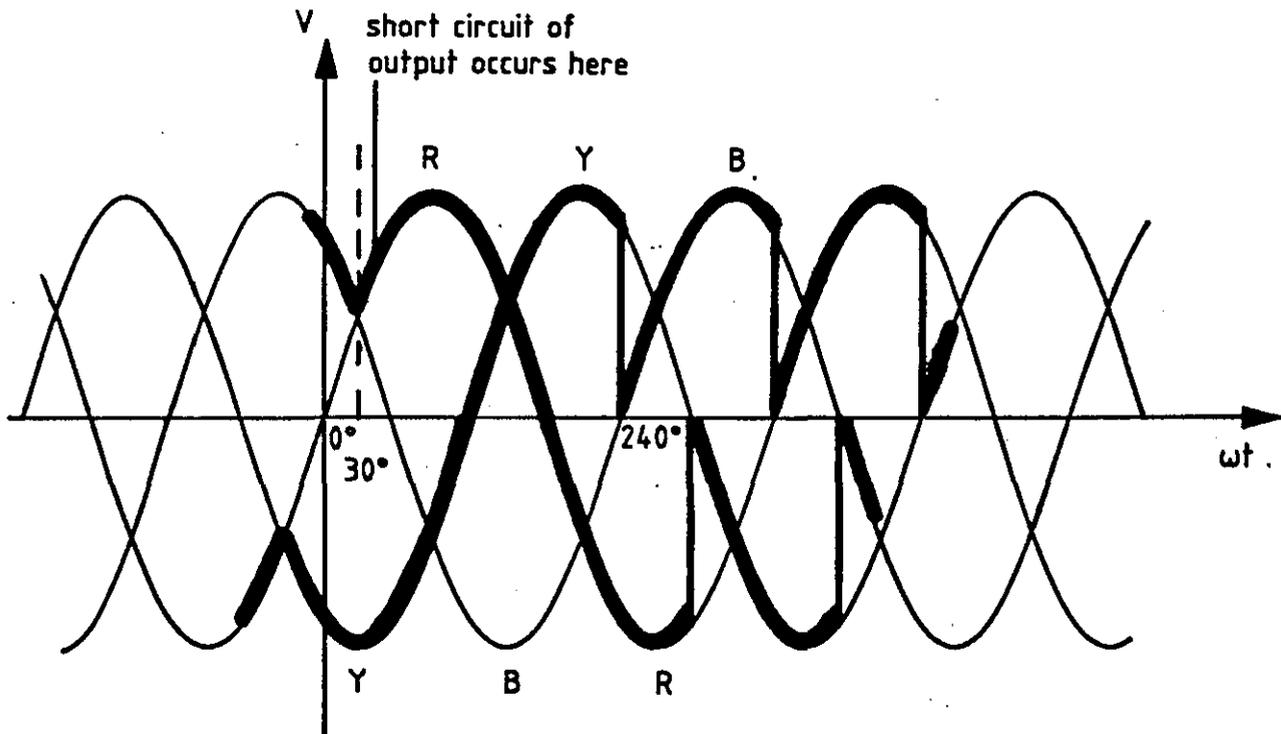
$$\begin{aligned} \text{The volt} &= \frac{3\sqrt{3}}{2\omega} \hat{V}_p \\ \text{second area} & \quad (\text{A2.2}) \end{aligned}$$

The volt second area absorbed by the choke is also equal to the product of the inductance of the choke and the change in current in the dc link. The change in dc link current (ΔI_D) is therefore given by Eqn. A2.3.

$$\Delta I_D = \frac{3\sqrt{3}}{2\omega L_C} \hat{V}_p \quad (\text{A2.3})$$



(a)



(b)

Figure A.2.1 - The rectification bridge and the voltage waveform in the dc link when the firing of thyristors is phased back.

The maximum value of link current equals the value before the short circuit plus ΔI_D . The time taken for the energy to be drawn out of the choke is dependent on how far the firing of thyristors is phased back.

APPENDIX 3THE DERIVATION OF EXPRESSIONS NEEDED FOR THE DESIGN OF THE MODIFIED TANK CIRCUIT

The circuit presented to the fundamental component of the load current by the modified tank circuit is shown in Fig. 4.13. Expressions for the following parameters need to be obtained to enable the selection of components in the modified tank circuit.

- (a) The equivalent capacitance of the branch containing C_T and L'' (C_{eq}).
- (b) The power developed in the modified tank circuit (P_D).
- (c) The efficiency of the modified tank circuit (η_{MTC}).

A.3.1 An Expression for C_{eq}

Since the switching frequency of the inversion bridge is tuned to the lowest parallel resonant frequency of the tank circuit the branch containing C_T and L'' will be capacitive and Eqn. A3.1 can be written.

$$\frac{-j}{\omega_s C_{eq}} = j\omega_s L'' \frac{-j}{\omega_s C_T} \quad (A3.1)$$

Rearranging Eqn. A3.1 produces the expression for C_{eq} in Eqn. A3.2.

$$C_{eq} = \frac{C_T}{1 - \omega_s^2 L'' C_T} \quad (A3.2)$$

A.3.2 An Expression for P_D

The equivalent series resistance of the workcoil (R_W) at the switching frequency is given by Eqn. A3.3.

$$R_W = \frac{\omega_s L_T}{Q_L} \quad (A3.3)$$

The equivalent series resistance of the inductor L'' (R'') at the switching frequency is given by Eqn. A3.4.

$$R'' = \frac{\omega_s L''}{Q''} \quad (\text{A3.4})$$

Where Q'' is the Q of inductor L'' at the switching frequency.

Assuming $\omega_s L'' \gg R''$ and $\omega_s L_T \gg R_W$ then the power dissipated in the modified tank circuit will not be affected if R'' is removed and another resistor (R_W') given by Eqn. A3.5 is connected in series with R_W .

$$R_W' = \sqrt{\frac{C_{eq}}{C_{eq} + 8C_{DS}}} \cdot R'' \quad (\text{A3.5})$$

The impedance of the modified tank circuit (Z_D) is given by Eqn. A3.6.

$$Z_D = \frac{L_T}{(C_{eq} + 8C_{DS})(R_W + R_W')} \quad (\text{A3.6})$$

The power developed in the modified tank circuit is given in Eqn. A3.7.

$$P_D = \frac{V_T^2}{Z_D} \quad (\text{A3.7})$$

If the deadband in the load current is assumed negligible and the Q of the modified tank circuit is high (>10) then the power developed in the modified tank circuit is also accurately given by Eqn. A3.8.

$$P_D = \frac{V_D^2}{0.81 \cdot Z_D} \quad (\text{A3.8})$$

A.3.3 An Expression for η_{MTC}

If Q_u and Q_L are the unloaded and loaded Q factors of the workcoil at the switching frequency then the efficiency of the modified tank circuit is given by Eqn. A3.9.

$$\eta_{MTC} = \frac{\omega_S L_T \left[\frac{1}{Q_L} - \frac{1}{Q_u} \right]}{\frac{\omega_S L_T}{Q_L} + R_W'} \quad (A3.9)$$

A LISTING OF THE PROGRAMME USED TO SELECT COMPONENTS IN THE MODIFIED
TANK CIRCUIT

```

10PRINT"What is the workcoil inductance in microH ";
20INPUT LT:LT=LT/1E6
30PRINT"What is the loaded Q of the workcoil ";
40INPUT QL
42PRINT"What is the unloaded Q of the workcoil ";
44INPUT QU
50PRINT"What is the intended swiwhing frequency in kHz ";
60INPUT FS:FS=FS*1E3
70 PRINT"What is the Cds across each MOSFET in nF";
80INPUT CDS
90PRINT"How many MOSFETS are there in each leg";
100INPUT N
110CDS=N*2*CDS/1E9
116WS=2*3.14159*FS
120CEQ=(1/((WS^2)*LT))-CDS
125PRINT"CEQ = ";CEQ*1E9;"nF"
130CT=0.7*CEQ
140L11=(1-0.7)/((WS^2)*CT)
150 WRES=((LT+L11)/((LT*L11)*CDS))^0.5
160FRES=WRES/(2*3.14159)
165PRINT"FRES = ";FRES/1E3;"kHz"
170PRINT "CT = ";CT*1E9;"nF"
180PRINT "L11 = ";L11*1E6;"microH"
190PRINT "fres/fs = ";FRES/FS
200PRINT "What is the link voltage";
210INPUT VD
220RWU=(WS*LT)/QU
230RW=(WS*LT)/QL
240RW11=(WS*L11)/QU
250RW1=RW11*((CEQ/(CEQ+CDS))^0.5)
260ZD=LT/((CEQ+CDS)*(RW+RW1))
270EFFTC=(RW-RWU)/(RW+RW1)
280P=((VD/0.9)^2)/ZD
290PRINT"The efficiency of the modified tank circuit is ";E
FFTC
300PRINT"ZD = ";ZD;"Ohms"
310PRINT"Output power = ";P;"W"

```

APPENDIX 5AN ANALYSIS OF THE CURRENT FED FULL BRIDGE INVERTER USING LAPLACE TRANSFORMS

The equations necessary for an analytical solution of a full bridge current fed inverter feeding a parallel resonant tank circuit are developed for either one of the two possible states of the switches. Final conditions of currents and voltages for the period when S1 and S2 are on become initial conditions when S3 and S4 are on. Repeating this over many switching cycles the transient and steady state operation of the unit can be investigated. This algorithm can be implemented on a digital computer.

The following assumptions are made.

- (a) The effects of the parasitic lead inductances are swamped by the effects of the lumped components in the modified tank circuit.
- (b) The switches turn on and off instantaneously.
- (c) Two switches turn off as the other two switches turn on i.e. no deadband.
- (d) The dc link current changes negligibly during a half cycle of switching frequency.
- (e) The effects of the 300 Hz ripple on the dc link voltage are negligible.

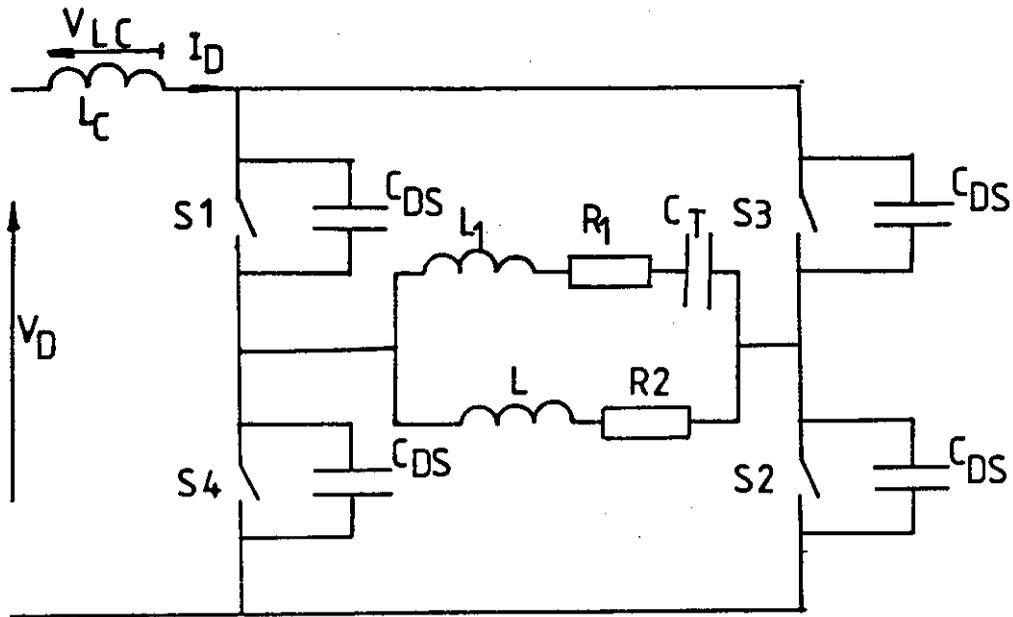


Figure A5.1 - The circuit used for a Laplace Transform Analysis of a full bridge current fed inverter.

The circuit of the inverter used for the analysis is shown in Fig. A5.1. For the half time period analysed switches S_3 and S_4 are turned on and the circuit model in Fig. A5.1 reduces to the circuit in Fig. A5.2.

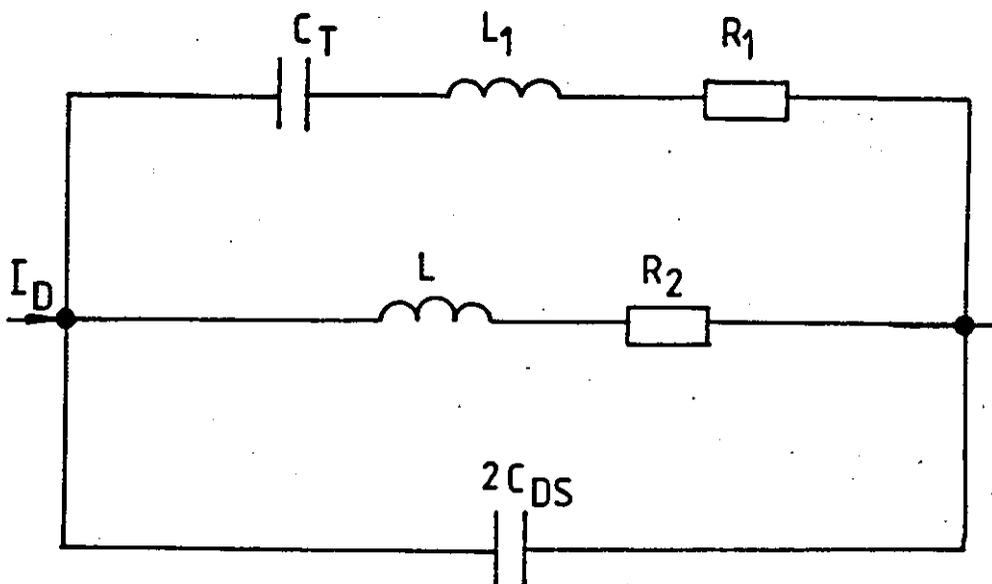


Figure A5.2 - The circuit used for a Laplace Transform Analysis of a full bridge current fed inverter for the period when S3 and S4 are on.

Inserting initial conditions the circuit elements required for a Laplace Transform Analysis are shown in Fig. A5.3.

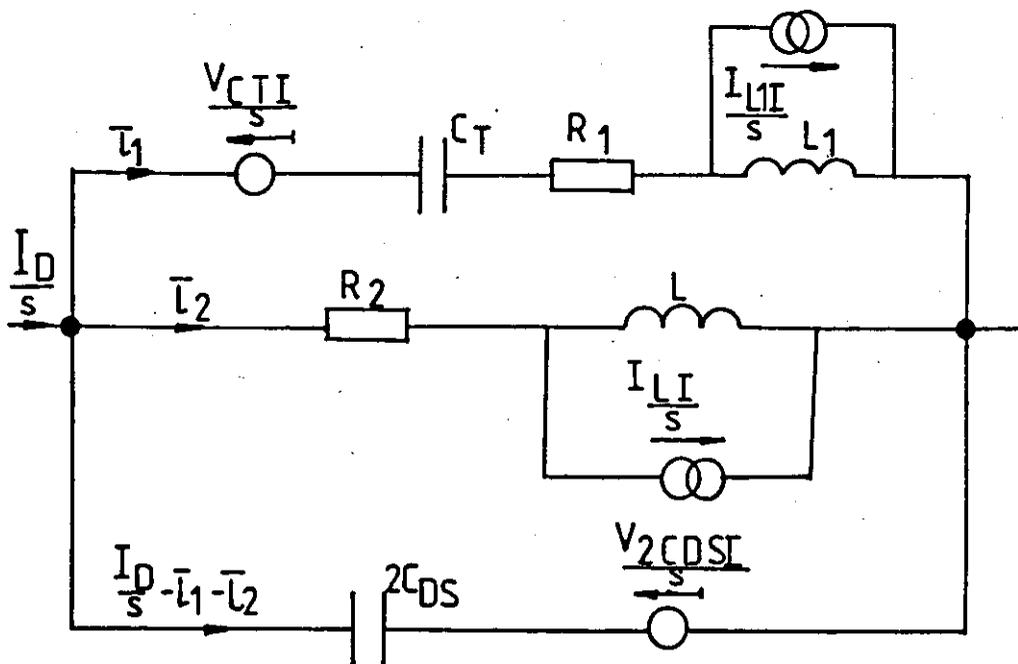


Figure A5.3. - The circuit used for a Laplace Transform Analysis including initial conditions.

Analysis of this circuit produces the expression for i_1 given in Eqn. A5.1.

$$\bar{I}_1 = \frac{K_1 s^3 + K_2 s^2 + K_3 s + K_4}{K_5 s^4 + K_6 s^3 + K_7 s^2 + K_8 s + K_9} \quad (\text{A5.1})$$

Where

$$K_1 = AP + DE$$

$$K_2 = BP + AN + CE + DF$$

$$K_3 = BN + AM + CF + DG$$

$$K_4 = BM + CG$$

$$K_5 = PJ$$

$$K_6 = NJ + PS$$

$$K_7 = MJ + NS + PR - DH$$

$$K_8 = MS + NR - CH$$

$$K_9 = MR$$

and

$$A = I_{L1I} L_1 - I_{LI} L$$

$$B = - \frac{V_{CTI}}{S}$$

$$C = R_2$$

$$D = L$$

$$E = I_{LI} L$$

$$F = V_2 C D S I$$

$$G = \frac{I_D}{2C_{DS}}$$

$$H = - \frac{1}{2C_{DS}}$$

$$J = L_1$$

$$R = \frac{1}{C_T}$$

$$S = R_1$$

$$M = \frac{1}{2C_{DS}}$$

$$N = R_2$$

$$P = L$$

Since the denominator in Eqn. A5.1 is a quartic and constants K_5 to K_9 are real there are three possible cases for the roots.

- (a) 2 sets of conjugate pairs
- (b) 1 set of conjugate pairs and 2 real roots
- (c) 4 real roots.

The form of the solution depends on the values of the constants K_5 to K_9 . Therefore when Partial Fractions are used to find a solution to Eqn. A5.1 the final form of the expression for i_1 will depend on the values of K_5 to K_9 .

The expression for \bar{i}_2 is given in Eqn. A5.2.

$$\bar{i}_2 = \frac{K_{10}s^4 + K_{11}s^3 + K_{12}s^2 + K_{13}s + K_{14}}{s(K_{15}s^4 + K_{16}s^3 + K_{17}s^2 + K_{18}s + K_{19})} \quad (\text{A5.2})$$

Where $K_{10} = EJ$

$$K_{11} = FJ + ES$$

$$K_{12} = GJ + FS + ER + HA$$

$$K_{13} = GS + FR + HB$$

$$K_{14} = GR$$

$$K_{15} = JP$$

$$K_{16} = SP + JN$$

$$K_{17} = SN + PR + MJ - HD$$

$$K_{18} = RN + SM - HC$$

$$K_{19} = RM$$

An inspection of Fig. A5.2 reveals that two branches contain capacitors which will be high impedance to low frequency components of a Heaviside step function of magnitude I_D . As t approaches infinity then i_2 approaches I_D . This is catered for by the s term in the denominator of Eqn. A5.2.

The expressions for \bar{i}_1 and \bar{i}_2 are best solved on a digital computer. Other voltages and currents around the circuit can then be found. At

the end of half a time period of the switching frequency some of the final conditions become the initial conditions of the next half period. The volt second area of the voltage waveform across the inversion bridge can be calculated and thus the change in the dc link current during a half cycle can be found. The dc link current is set to its new value for analysis during the next half cycle.

A LISTING OF THE PROGRAMMES USED TO SIMULATE THE TWO ELEMENT TANK CIRCUIT
 AND THE MODIFIED TANK CIRCUIT USING SPICE.

A6.1 The simple two element tank circuit

```

mosfet inv
vip 1 0 dc 28
vid 1 19
lc 19 20 10m ic=0.1
rc 20 2 0.5
m1 15 3 5 5 mod1
m3 16 9 14 14 mod1
m4 17 11 0 0 mod1
m2 18 13 0 0 mod1
lp1 2 15 50n ic=0.1
lp2 14 18 50n ic=0.1
lp3 2 16 50n ic=0
lp4 5 17 50n ic=0
cds1 15 5 2n ic=0
cds2 18 0 2n ic=0
cds3 16 14 2n ic=0
cds4 17 0 2n ic=0
lt 6 7 8.1u ic=3.4
rw 6 5 0.53
ct 5 7 50n ic=0
ls 7 8 700n ic=0.1
rs 8 14 0.1
v1 3 5 pulse(15 0 0 0 0 2u 4u)
v2 13 0 pulse(15 0 0 0 0 2u 4u)
v3 9 14 pulse(0 15 0 0 0 2u 4u)
v4 11 0 pulse(0 15 0 0 0 2u 4u)
.tran 50n 400u 396u uic
.model mod1 nmos kp=55 vto=3.5
.options limpts=500 itl5=90000
.print tran i(vid) v(5,15) v(5,7)
.end
####

```

A6.2 The modified tank circuit

```

mosfet inv
vip 1 0 dc 28
vid 1 19
lc 19 20 10m ic=0.2
rc 20 2 0.5
m1 15 3 5 5 mod1
m3 16 9 14 14 mod1
m4 17 11 0 0 mod1
m2 18 13 0 0 mod1
lp1 2 15 50n ic=3.2
lp2 14 18 50n ic=3.2
lp3 16 2 50n ic=3
lp4 17 5 50n ic=3
cds1 15 5 40n ic=0
cds2 18 0 40n ic=0
cds3 16 14 40n ic=0
cds4 17 0 40n ic=0
lt 6.2 7 8.1u ic=6.2
rw 6 5 0.2
ct 5 21 50n ic=0
l11 22 21 9.1u ic=3
r11 22 7 0.25
rs 8 14 0.1
ls 7 8 700n ic=3.2
v1 3 5 pulse(15 0 0 0 0 3.75u 7.14u)
v2 13 0 pulse(15 0 0 0 0 3.57u 7.14u)
v3 9 14 pulse(0 15 0 0 0 3.57u 7.14u)
v4 11 0 pulse(0 15 0 0 0 3.57u 7.14u)
.model mod1 nmos kp=55 vto=3.5
.tran 300n 400u 300u 100n uic
.options limpts=1000 itl5=140000
.print tran v(15,5),i(vid)
.end
####S

```

APPENDIX 7

A LISTING OF THE SOFTWARE PROGRAMMED INTO THE MICROPROCESSOR.

```
232REM Main Program Segment
1010PROC_Init
1020PROC_Assemble
1030PROC_Wait_For_PCD_Pulses
1040PROC_Start
1045CLS
1050REPEAT
1060Fmin=100E3:Fmax=Fupper_limit
1065REPEAT
1070PROC_Find_Resonance(Fmin,Fmax,Vout)
1080IF Status=FALSE THEN UNTIL TRUE:UNTIL FALSE
1090IF Status=2 OR Status=3 THEN PROC_Shutdown:PROC_Error
_Message(Status):UNTIL TRUE:UNTIL TRUE:PROC_Init:GOTO 1030
1100PROC_Input_Sample
1105 FOR DO%=0 TO 10
1110PROC_Achieve_Power_Dem(Power_Dem)
1120IF Status=FALSE THEN PROC_Shutdown:PROC_Error_Message
(2):UNTIL TRUE:UNTIL TRUE:PROC_Init:GOTO 1030
1130FOR J=0 TO 100:PROC_Get_Power_Demand:NEXT
1135 NEXT DO%
1140Fmin=Fres-20E3:Fmax=Fres+20E3
1150UNTIL FALSE
1160
1170
1180
1190
1200
1210
10000DEF PROC_Fangle_Write(V)
10010Status=TRUE
10020IF V>Vmax THEN V=Vmax:Vout=Vmax:Status=1
10030Fangle=DEG(ACS(V*K1))
10040Fword=Fangle*K2+K3
10050IF ?FPAT<>&3F THEN Status=FALSE:ENDPROC
10060REPEAT UNTIL ?SR AND &3C=&3C
10070?FANGLE=Fangle
10080?FWORDL=Fword MOD 256
10090?FWORDH=Fword DIV 256
10100ENDPROC
10110
10120
10130
```

```

11000DEF PROC_Freq_Write(F)
11010?OUTREGA=INT(F/2000)
11020ENDPROC
11030
11040
11050
11060
12000DEF PROC_Achieve_Power_Dem(Power_Dem)
12005Current_Limit=FALSE:Voltage_Limit=FALSE
12010REPEAT:Xload=Vout/(Iout+.1)
12020Vnew=SQR(ABS(Xload*(Power_Dem-Pout)+Vout^2))
12025 PRINT TAB(5,8);"Link Voltage=";Vnew
12030IF Vnew/(Xload+.1)>Imax THEN PROC_Error_Message(4):Vnew=Imax*Xload:Current_Limit=TRUE
12040PROC_Fangle_Write(Vnew)
12045IF Status=1 THEN UNTIL TRUE:PROC_Error_Message(1):Iout=FN_Read_Current:Pout=Vout*Iout:ENDPROC
12050IF Status=FALSE THEN UNTIL TRUE:PROC_Error_Message(2):ENDPROC
12060Vout=Vnew
12070Iout=FN_Read_Current
12075IF Status=FALSE THEN PROC_Error_Message(3):Status=1:ENDPROC
12080Pout=Vout*Iout
12085 PRINT TAB(5,12);"Pout=";Pout
12100
12110UNTIL ABS(Vout*Iout-Power_Dem)<=0.05*Power_Dem OR Current_Limit OR Voltage_Limit
12120ENDPROC
12130
13000DEF PROC_Error_Message(Message_No)
13010FOR I%=1 TO Message_No
13020READ Message$
13030NEXT I%
13040PRINTTAB(5,14);Message$+" ":PRINTTAB(0,0);" "
13050RESTORE 13090
13060ENDPROC
13070
13080
13090DATA "VOLTAGE LIMIT","'STOP' SHUTDOWN","OVER-CURRENT SHUTDOWN","CURRENT LIMIT","RESONANCE LOST ","MESSAGE 6","MESSAGE 7","MESSAGE 8","MESSAGE 9","MESSAGE 10"
13100DATA "MESSAGE 11","MESSAGE 12","MESSAGE 13","MESSAGE 14","MESSAGE 15","MESSAGE 16","MESSAGE 17","MESSAGE 18","MESSAGE 19","UNDEFINED MESSAGE "
13110
13120
13130
13140

```

```

14000DEF PROC_Get_Power_Demand
14010REM***** space for expansion ***
14020A$=INKEY$(0)
14030IF A$<>CHR$(&OD) THEN GOTO 14040 ELSE Power_Dem=VAL(P
ower_Dem$):Power_Dem$=""
14035IF Power_Dem<=0 THEN Power_Dem=.1:ENDPROC ELSE ENDPRO
C
14040IF A$=CHR$(&7F) AND LEN(Power_Dem$)>0 THEN Power_Dem$
=LEFT$(Power_Dem$,LEN(Power_Dem$)-1):ENDPROC
14050Power_Dem$=Power_Dem$+A$
14060ENDPROC
14070
14080
14090
14100
15000DEF PROC_Find_Resonance(Fmin,Fmax,Vout)
15010 PROC_Fangle_Write(200)
15020IF Status<> TRUE THEN Status=2:ENDPROC
15030Fout=Fmin
15040Imin=Imax
15041Itop=0
15042Ivntop=0
15043Intop=0
15050REPEAT
15060PROC_Freq_Write(Fout)
15070FOR J=0 TO 50:NEXT
15080Iout=FN_Read_Current
15085IF Status=2 THEN UNTIL TRUE:ENDPROC
15090IF Status=FALSE THEN UNTIL TRUE:Status=3:ENDPROC
15100 IF Iout<Imin THEN Imin=Iout:Fres=Fout:Count=0
15102 PRINT TAB(5,4);"Fout=";Fout
15103 Count=Count+1
15104 IF Fout=Fmin THEN Ibot=Iout
15105 IF Fout=Fmin+2E3 THEN Ivnbot=Iout
15106 IF Fout=Fmin+4E3 THEN Inbot=Iout
15107 IF Fout=Fmax-4E3 THEN Intop=Iout
15108 IF Fout=Fmax-2E3 THEN Ivntop=Iout
15109 IF Fout=Fmax THEN Itop=Iout
15113 Fout=Fout+2E3
15114 IF Count=40 THEN UNTIL TRUE:GOTO 15117
15115 UNTIL Fout>Fmax
15116 IF Imin=Ibot OR Imin=Ivnbot OR Imin=Inbot THEN Statu
s=FALSE:PROC_Error_Message(5):ENDPROC
15117 IF Imin=Intop OR Imin=Ivntop OR Imin=Intop THEN Statu
s=FALSE:PROC_Error_Message(5):ENDPROC
15118 PRINT TAB(5,6);"Imin=";Imin
15119 PRINT TAB(5,4);"Fres=";Fres
15120 PRINTTAB(5,14)" "
15140PROC_Freq_Write(Fres-4E3)
15160PROC_Fangle_Write(Vout)
15170IF Status=FALSE THEN Status=2:ENDPROC
15180IF Status=1 THEN PROC_Error_Message(1)
15190Status=TRUE:ENDPROC

```

```
16000DEF PROC_Init
16010
16020
16030
16040
16050
16060
16070REM**** define memory labels ***
16080OUTREGB=&DB00:OUTREGA=&DB01:DDRB=&DB02:DDRA=&DB03:T1C
LLATCH=&DB06:T1CHLATCH=&DB07
16090SR=&DB0A:ACR=&DB0B:PCR=&DB0C:ITFLAGREG=&DB0D:IER=&DB0
E:T1CH=&DB05:T1CL=&DB04:T2CLLATCH=&DB08:T2CH=&DB09
16110
16120REM**** define memory labels****
16130FWORDL=&80:FWORDH=&81:FANGLE=&82:FPAT=&83
16140
16150?FPAT=&3F:?FWORDL=9998 MOD 256:?FWORDH=9998 DIV 256:?
FANGLE=90
16160REM**** define digital ports ****
16170?DDRB=&EF:?OUTREGB=&20:?DDRA=&FF:?OUTREGA=&3F
16180
16190
16200
16210REM**** define variables ****
16220Fangle=90
16230Power_Dem=10:Power_Dem$="":Pout=0
16240Iout=0
16250Vout=0.1
16260Fres=100E3
16270Fout=100E3
16280K1=PI/(3*SQR(3*2)*110)
16290K2=10000/180:K3=4998
16300Status=TRUE
16310
16320
16330REM**** define limits ****
16340Imax=30
16350Fupper_limit=400E3
16360Foffset=2E3
16370Vmax=257.29994
16380
16390
16400
16410
16420ENDPROC
```

```
17000DEF PROC_Assemble
17010REM PROJECT TEST FOR SERIAL OP
17020DIM GAPX 1000
17030FOR IX=0 TO 2 STEP 2
17040PX=GAPX
17050[OPT IX
17060.INIT
17070SEI
17120LDA £&A2
17130STA IER
17140LDA £&FF
17150STA SR
17160LDA £&81
17170STA T1CLLATCH
17180LDA £&06
17190STA T1CHLATCH
17200LDA £&C6
17210STA PCR
17220LDA £&DC
17230STA ACR
17240LDA &204
17250STA OLDVEC
17260LDA &205
17270STA OLDVEC+1
17280LDA £int MOD 256
17290STA &204
17300LDA £int DIV 256
17310STA &205
17320CLI
17330RTS
17340.int
17350LDA ITFLAGREG
17360AND £&23
17370BNE MYINTS
17380JMP (OLDVEC)
17390.MYINTS
17400\STA ITFLAGREG
17410CMP £&20
17420BEQ T2C_INT
17430CMP £&02
17440BNE ESD
17450.PCD_INT
17452LDA £&02
17454STA ITFLAGREG
17460LDA FWORDL
17470STA T2CLLATCH
17480LDA FWORDH
17490STA T2CH
```

```
17500JMP RETINT
17510.T2C_INT
17512LDA £820
17514STA ITFLAGREG
17520LDA £8C0
17530STA ACR
17540LDA £8DC
17550STA ACR
17560LDA T1CHLATCH
17570STA T1CH
17580LDA FPAT
17590STA SR
17600.RETINT
17610LDA &FC
17620RTI
17625.ESD
17627LDA £801
17629STA ITFLAGREG
17630LDA FPAT
17640CMP £83F
17650BNE RETINT
17660LDA FPAT
17670SEC
17680ROR A
17690STA FPAT
17700LDA FWORDH
17710CMP £820
17720BPL RETINT
17730LDA FPAT
17740SEC
17750ROR A
17760STA FPAT
17770JMP RETINT
17780.OLDVEC EQUW &0
17790]NEXTI%
17800CALL INIT
17810ENDPROC
17820
17830
17840
18000DEF PROC_Wait_For_PCD_Pulses
18010REPEAT:UNTIL ?SR<>&FF
18015PRINT'"INDUCTION HEATER CONTROL UNIT READY"
18020ENDPROC
18030
    120
18050
18060
```

```

19000DEF PROC_Start
19010?OUTREGB=&00
19020REPEAT:UNTIL (?OUTREGB AND &10)=&10
19030?OUTREGB=&40
19040ENDPROC
19050
19060
19070
20000DEF PROC_Shutdown
20010 IF ?FPAT=&3F AND FANGLE<60 THEN ?FPAT=&CF
20020IF ?FPAT=&3F AND FANGLE>60 THEN ?FPAT=&9F
20030FOR J=0 TO 1000:NEXT
20040?OUTREGB=&20
20050ENDPROC
20060
21000DEF PROC_Input_Sample
21010ENDPROC
25020DEF FN_Read_Current
25025IF ?FPAT<>&3F THEN Status=2:=0
25040Itotal=0
25060Iav=0
25080ZX=0
25100TIME=0
25120REPEAT
25140Itotal=Itotal+ADVAL(64)
25160ZX=ZX+1
25180UNTIL TIME>=4
25200I=Itotal/(ZX*2560*2)
25220PRINTTAB(5,10);"Ilink=";I
25240IF I>Imax THEN Status=FALSE ELSE Status=TRUE
25260=I
26000DEF PROC_Coil_Measts
26005 CLS
26010REPEAT
26020 PRINT "Is the coil unloaded?"
26030INPUT A$
26040IF LEFT$(A$,1)="Y" OR LEFT$(A$,1)="y" THEN UNTIL TRUE
:GOTO 26055
26050UNTIL FALSE
26055 CLS
26060PROC_Find_Resonance(1E5,4E5,200)
26061 IF Status=FALSE THEN PROC_Shutdown:PROC_Error_Messag
e(5):ENDPROC
26064 FOR J=0 TO 2000: NEXT
26065 CLS
26070PRINT "The no of MOSFETS in each leg = "
26080INPUT N:FRESU=Fres
26090PRINT "CT in nanofarads ="
26100INPUT CT:CT=CT/1E9
26110PRINT "L11 in microhenries = "

```

```

26120INPUT L11:L11=L11/1E6
26130PRINT"CDS across each MOSFET = "
26140INPUT CDS:CDS=CDS/1E9
26180ZDU=200/(0.81*Imin)
26190CEQU=CT/(1-((2*3.14159*Fout)^2)*L11*CT)
26200QU=ZDU*2*3.14159*Fout*(CEQU+N*CDS*2)
26202 @X=&20207
26210 CLS
26225REPEAT
26226PRINT "Is the coil loaded ?"
26227INPUT A$
26230IF LEFT$(A$,1)="Y" OR LEFT$(A$,1)="y" THEN UNTIL TRUE
:GOTO 26245
26240UNTIL FALSE
26245 CLS
26248PROC_Find_Resonance(1E5,4E5,200)
26249IF Status=FALSE THEN PROC_Shutdown:PROC_Error_Message
(5):ENDPROC
26250 FOR J=0 TO 2000:NEXT
26251 CLS
26252ZDL=200/(0.81*Imin):FRESL=Fres
26253CEQL=CT/(1-((2*3.14159*Fout)^2)*L11*CT)
26254QL=ZDL*2*3.14159*Fout*(CEQL+N*CDS*2)
26255LWCL=1/(((2*3.14159*FRESL)^2)*(CEQL+N*2*CDS))
26256LWCU=1/(((2*3.14159*FRESU)^2)*(CEQU+N*2*CDS))
26257EFF=(LWCL*QU-LWCU*QL)/(QU*LWCL)
26258 CEQU=CEQU*1E6
26259 CEQL=CEQL*1E6
26260PRINTTAB(5,0)"CEQU = ";CEQU;"microF"
26270PRINTTAB(5,4)"ZDU = ";ZDU;"OHMS"
26280PRINTTAB(5,8)"QU = ";QU
26288 LWCU=LWCU*1E6
26289 LWCL=LWCL*1E6
26290PRINTTAB(5,12)"LWCU = ";LWCU;"microH"
26300PRINTTAB(5,14)"LWCL = ";LWCL;"microH"
26310PRINTTAB(5,2)"CEQL = ";CEQL;"microF"
26320PRINTTAB(5,6)"ZDL = ";ZDL;"OHMS"
26330PRINTTAB(5,10)"QL = ";QL
26334FRESU=FRESU/1E3
26335PRINTTAB(5,16)"FRESU = ";FRESU;"kHz"
26339FRESL=FRESL/1E3
26340PRINTTAB(5,18)"FRESL = ";FRESL;"kHz"
26350PRINTTAB(5,20)"EFF = ";EFF
26360ENDPROC
26410 ENDPROC
30000DEF PROC_Manual
30010F=&32
30015PROC_Fangle_Write(150)
30020FOR I=0 TO 10000:?&DB01=F:PRINTF*2E3:A$=GET$:IF A$="U
" THEN F=F+1:NEXT ELSE IF A$="D" THEN F=F-1:NEXT ELSE NEXT

```

A. LISTING OF THE PROGRAMME USED TO SIMULATE THE COMMERCIAL PROTOTYPE USING
SPICE

```
mosfet inv
vip 1 0 dc 125
vid 1 19
lc 19 20 10m ic=0
rc 20 2 0.5
m1 15 3 5 5 mod1
m3 16 9 14 14 mod1
m4 17 11 0 0 mod1
m2 18 13 0 0 mod1
lp1 2 15 50n ic=0
lp2 14 18 50n ic=0
lp3 2 16 50n ic=0
lp4 5 17 50n ic=0
cds1 15 5 200n ic=0
cds2 18 0 200n ic=0
cds3 16 14 200n ic=0
cds4 17 0 200n ic=0
lt 6 7 48u ic=0
rw 6 5 0.49
ct 5 7 5.0u ic=0
ls 7 8 0.7 ic=0
rs 8 14 0.1
v1 3 5 pulse(15 0 0 0 0 50u 100u)
v2 13 0 pulse(15 0 0 0 0 50u 100u)
v3 9 14 pulse(0 15 0 0 0 50u 100u)
v4 11 0 pulse(0 15 0 0 0 50u 100u)
.model mod1 nmos kp=55 vto=3.5
.tran 500n 12m 11.9m uic
.options limpts=500 itl5=90000
.print tran v(5,15),v(15,2),i(vid),v(5,7),v(6,7),v(7,8)
.end
####S
```

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