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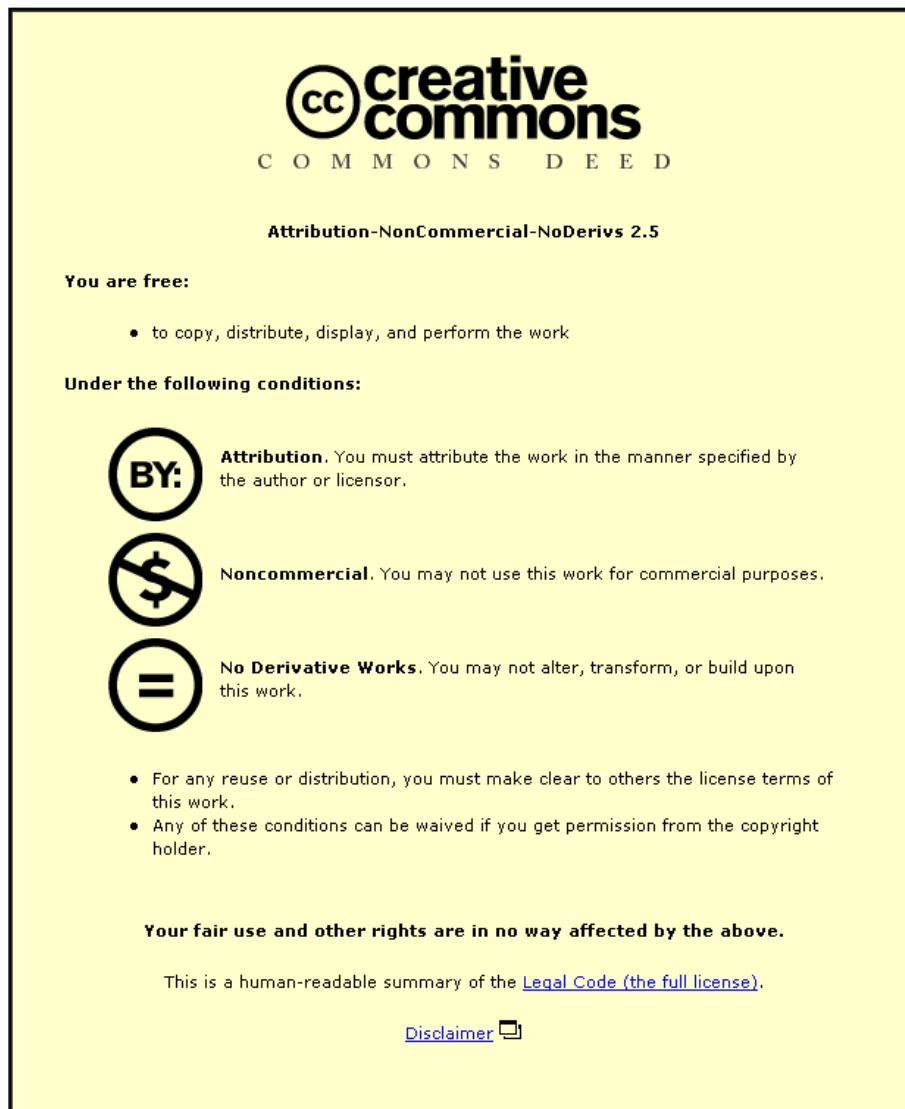
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# **Design & Reliability of Polymeric Packages for High Voltage Power Semiconductors**

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**A Doctoral Thesis**

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for the award of  
**Doctor of Philosophy of Loughborough University**

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## **Abstract**

This thesis focuses on the development of a novel polymer based housing for power thyristor devices typically used in long distance high voltage direct current (HVDC) transmission.

Power thyristor devices used in HVDC power conversion stations are typically packaged in a hermetically sealed ceramic housing and have demonstrated an excellent history of reliability and performance. However, to avoid increasing the number of thyristors in future higher powered HVDC schemes thyristors having higher power ratings at 8.5 kV and sizes at 125 mm and 150 mm diameters are sought for implementation to achieve higher transmission ratings of, for example, 4000 A at  $\pm 800$  kV. The main disadvantages of such large ceramic-based packages are higher processing cost and weight whilst robustness is also a concern. To overcome these issues, replacing the current ceramic housing with a polymeric material has been investigated in this project. The advantages it is anticipated such packages will provide include lower cost, less weight, robustness, recyclability, etc. However, some challenges it will also offer are: non-hermeticity i.e. polymers are moisture and gas permeable, potentially more complex manufacturing routes, and different electrical, mechanical and thermal properties compared to ceramic materials. The work presented in this thesis was part of a larger project where these challenges have been addressed by developing and testing a prototype polymeric thyristor housing. The prototype is aimed at demonstrating that polymer packages can deliver performance and reliability comparable to, if not better than, current ceramic packages.

In this thesis, it is the package development and reliability related studies that are discussed. Because the housings will experience severe electrical stresses and various thermal excursions during their service life, the electrical and thermo-mechanical behaviour of the polymer housing was studied using finite element analysis to gain an understanding of the effects of various design variables and materials properties on performance and the tradeoffs

between performance and manufacturability. From these modelling studies, design guidelines have been established for the future development of polymer housings. On the other hand, to identify the physics-of-failure of the prototype that was manufactured as part of the project, accelerated life tests were performed to study its reliability. The knowledge gained from the polymer prototype development was then applied to the design of a larger 125 mm diameter housing using the Taguchi method of experimental design.

**Keywords:**

High voltage direct current, Power thyristor, Polymer package, Finite Element Analysis, Reliability study, Accelerated Life test, Taguchi method, Partial discharge, Dielectric breakdown

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# **1 Introduction**

## **1.1 Electricity Generation and Transmission**

Since the availability of the first commercial electricity, electrical technology has rapidly expanded to become the backbone of our modern society and is today used in an almost limitless set of applications which include heating, cooking, transport, lighting, IT, etc. Unlike other energy sources, such as oil or gas, electricity cannot be stored easily and economically in sufficient quantities. As a result, it is usually generated and distributed the moment it is needed. Transmitting electricity today requires a rather complex and dynamic infrastructure, whereby the power on the transmission line at any specific time must accommodate changing electricity supply and demand conditions, equipment shutdown and maintenance, weather extremes and fuel shortages among others.

Electricity is generated at power plants from a range of primary sources, e.g. nuclear, coal, hydro, etc. It is then transmitted through transformers and transmission lines, to substations, distribution lines, and finally to the electrical consumer. The distribution along transmission lines can be done in either of two modes - direct current (DC) or alternating current (AC). The choice of these depends on a host of interrelated factors, such as transmission ratings, geographical topography, safety and cost. Although AC transmission tends to be effective for most electrical distribution situations, DC transfer is increasingly adopted for energy transfer between different grids or when transmitting large power ratings over long distances. For example, for a typical 2000 MW transmission, Rudervall et al., 2010 showed that DC transmission becomes more economical than AC when the transmission distance is greater than 800 km. An example of a distribution system containing a high voltage direct current (HVDC) based link is illustrated in Figure 1.1, where AC power generated at a power plant is increased in

voltage using step-up transformers and rectified to direct current at the rectifier station for transport over long distances along either overhead lines on land, or submarine cables across an expanse of sea, to an inverter station where power is needed. Such transmission voltages tend to be around 400 kV. Once at the inverter station, the DC voltage is converted back to AC and decreased in steps to voltages, such as 11 kV for medium to large industries and 230 V for smaller factories and residential areas (Parliamentary Office of Science and Technology, 2001).

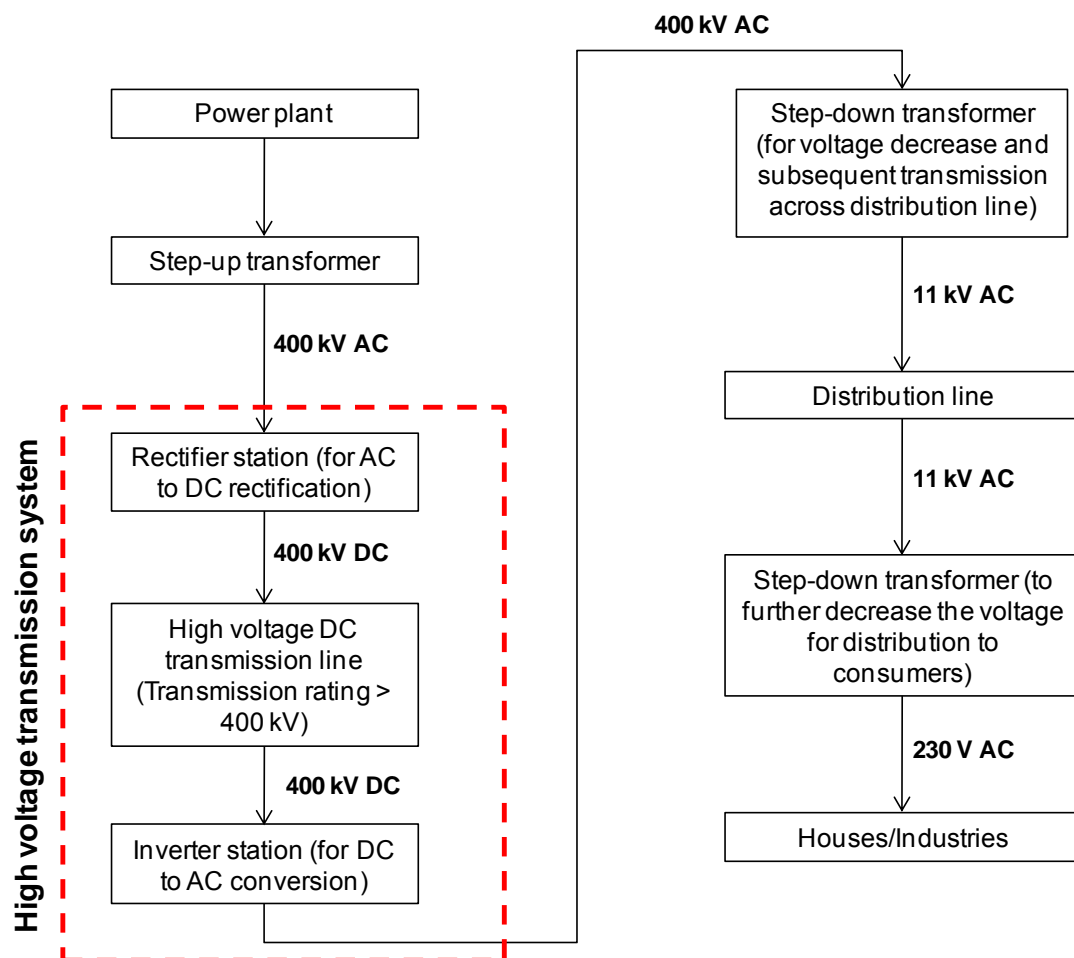


Figure 1.1: Outline of a distribution system containing a HVDC transmission link

## 1.2 HVDC Technology: an overview

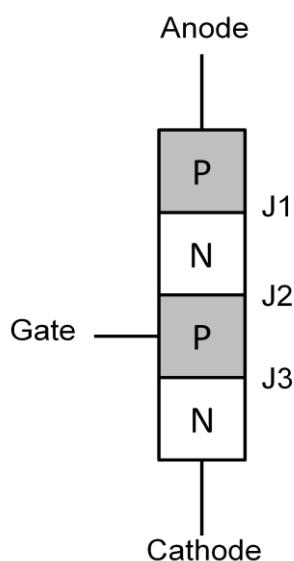
The origin of experimental work on high voltage transmission can be traced back as early as 1881 to the work of Marcel Deprez who published the first

theoretical examination of HVDC power transmission and successfully transmitted 1.5 kW at 2 kV over a distance of 35 miles (Arrillaga, 1998). Since then, different researchers have continued the work of Deprez to attain higher transmission voltages. Compared to DC transmission, the AC method was initially considered the preferred mode of high voltage transmission because it offered better efficiency and less power loss. However with the expansion of long distance and higher voltage transmission over time, AC transmission became inefficient due to stability related problems, such as oscillation of the reactive power between the capacitances and inductances in the system, and the HVDC transmission mode was reconsidered (Arrillaga, 1998). Transmitting DC power at high voltages (i.e. greater than 1.5 kV) and long distances only became possible with the use of the mercury-arc valve in the Gotland link in 1954 (Asplund et al., 2003a). However, with the invention of thyristors in 1957, the HVDC transmission area was offered new possibilities. In fact, since its first implementation in the Gotland link in 1967 when they replaced some mercury arc valves, thyristor valves have been implemented in several HVDC schemes (Asplund et al., 2003b). Because of its reliability and low loss properties, HVDC bulk transmission is expected to increasingly rely on thyristor-based technologies.

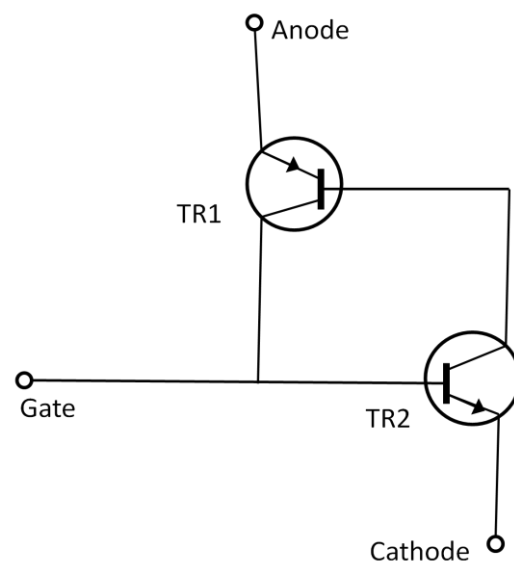
As shown in Figure 1.1, the HVDC transmission system consists of a rectifier unit at the sending end, and an inverter unit at the receiving end. The two ends are connected by a DC transmission line. The rectifier and inverter stations at both the transmission and receiving ends of the link consist of similar equipment. The main components are the thyristor valves, transformers (to adapt the AC voltage level to/from the required DC voltage level), and AC/DC filters to limit the amount of harmonics to the tolerance level of the network. The transmission medium used for bulk transmission over land is frequently a bipolar overhead line, whilst for submarine transmission of HVDC either solid or oil-filled cables are used (Rudervall et al., 2010).

The conversion of the AC to DC at the transmitting end and DC to AC at the receiving end are normally achieved in three ways, namely natural

commutated converters, capacitor commutated converters, and forced commutated converters (Rudervall et al., 2010). Compared to the other two technologies, the natural commutated converters are the most widely used system in HVDC transmission and the main component of the converter station is the thyristor, which is a solid-state semiconductor device similar to a diode with an extra control terminal (the gate). It comprises of four layers of alternating N and P-type material, e.g. P-N-P-N or N-P-N-P. The main terminals, the anode and cathode, are separated by the full four layers, and the gate is attached to the P-type material near the cathode as illustrated in Figure 1.2. Its operation can be understood in terms of a pair of tightly coupled bipolar transistors (Figure 1.3), whereby the emitter of an NPN transistor is connected to the cathode and the second PNP transistor connected to the anode. The gate is connected to the base of the NPN transistor.



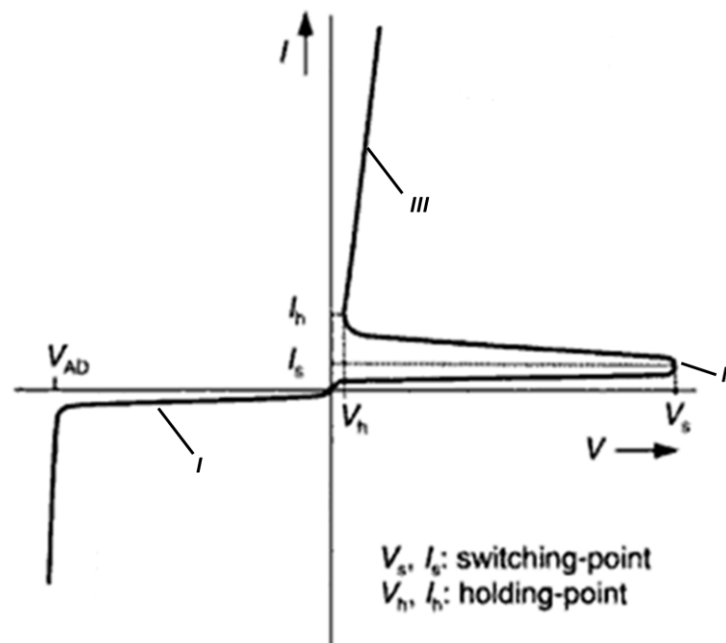
**Figure 1.2: Layer diagram of a thyristor**



**Figure 1.3: Equivalent circuit of a thyristor**

The typical current-voltage characteristic of a thyristor is illustrated in Figure 1.4. From the graph, it can be seen that the device operates in three states, namely (1) reverse blocking mode (*I*), (2) forward blocking mode (*II*), and (3) forward conducting mode (*III*). In the reverse blocking mode, the anode is negatively biased with respect to the cathode, and both PN junction (J1 and J3) are reverse biased. When the polarity is reversed, the thyristor changes to

the forward blocking mode, until a gate signal is applied or the applied voltage exceeds the blocking voltage to trigger the device into the on-state (or forward conducting mode) to behave as a pin diode. The thyristor will remain in a forward conducting mode even if the gate signal is removed (as opposed to a normal bipolar junction transistor). Turn-off of the device can be achieved by reducing the forward current below a threshold value known as the 'holding current'. The forward and blocking capability of the thyristor is determined by the avalanche breakdown of the blocking PN junction and the influence of the current gain,  $\alpha_{pnp}$  and  $\alpha_{npn}$ , of the partial transistors contained in the thyristor (Mitlehner et al., 1988).



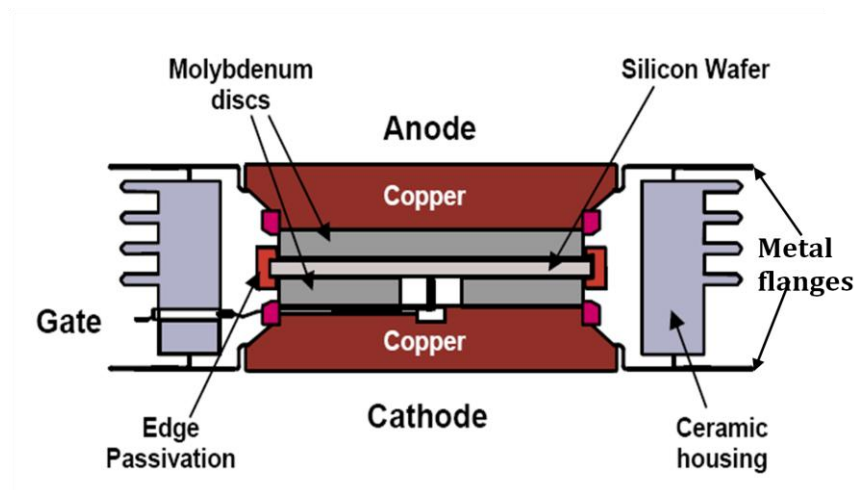
**Figure 1.4: I-V characteristic of a thyristor (Arrillaga, 1998)**

An example of a HVDC thyristor is shown in Figure 1.5. This device is predominantly packaged in a press-pack configuration, and is often referred to as a hockey-puck thyristor. Such a thyristor package comprises of a silicon wafer sandwiched between molybdenum discs and copper electrodes acting as anode and cathode terminals and serving as heat transfer media to cool the device (Figure 1.6). A gate lead is provided to establish connection between the gate electrode of the wafer and an external circuit to trigger the

semiconductor device. The whole assembly is enclosed in a hermetically sealed ceramic housing to prevent environmental attack and provide mechanical robustness.



**Figure 1.5: Photo of a 125 mm hockey-puck thyristor, sourced from Woodhouse, 2007b**



**Figure 1.6: Cross-sectional view of a hockey-puck thyristor, sourced from Woodhouse, 2007b**

To achieve the desired total blocking voltage, a number of these thyristors must be connected in series. A small group, e.g. 6, are normally stacked to form a clamped thyristor assembly structure (Figure 1.7). The thyristor assembly, which is also comprised of nickel-plated aluminium heat sinks connected to the anode and cathode pole pieces of the thyristors for heat removal, is then connected to various other components to form a thyristor module. Such a module, which is typically around 3.3 m x 2.1 m in dimensions, is made up of two identical valve sections A and B, and is comprised of identical components, namely damping capacitors, damping



resistors, gate electronics, a  $di/dt$  reactor and thyristor clamped assembly (Figure 1.8). The schematic diagram of such a valve section is illustrated in Figure 1.9.

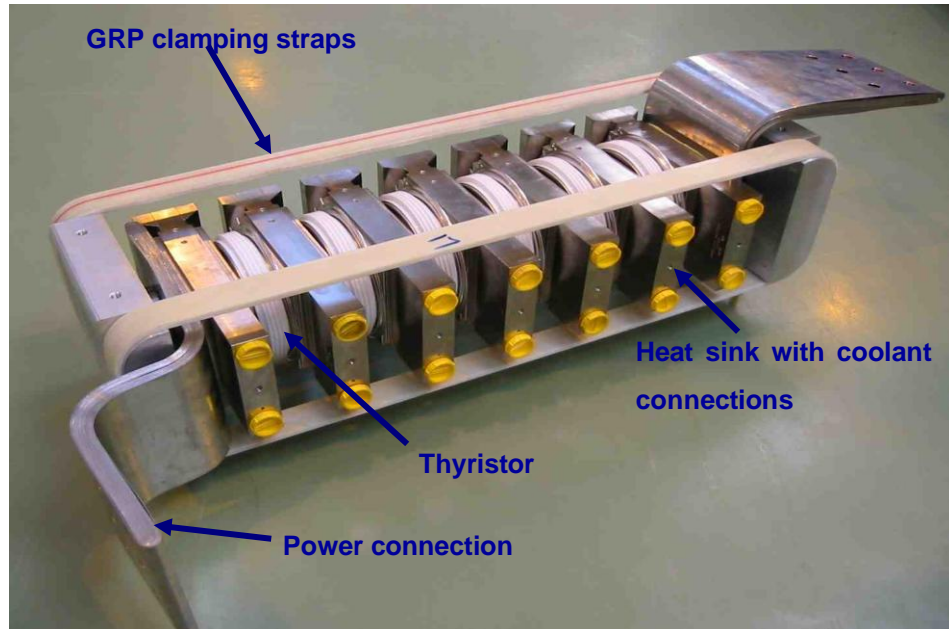


Figure 1.7: Photo of a clamped thyristor arrangement (Woodhouse, 2007b)

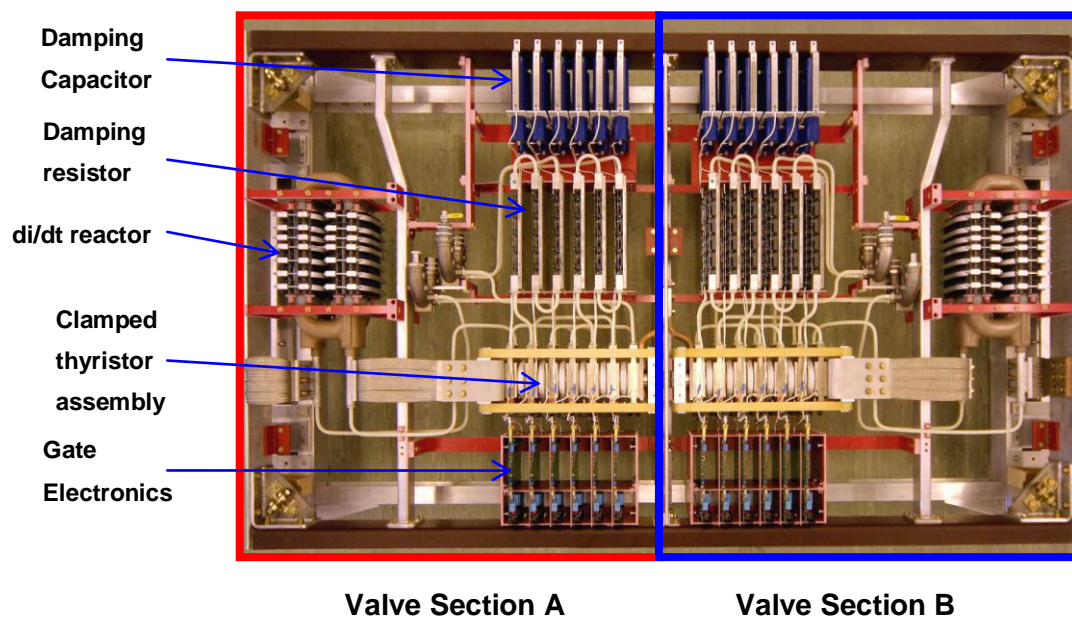
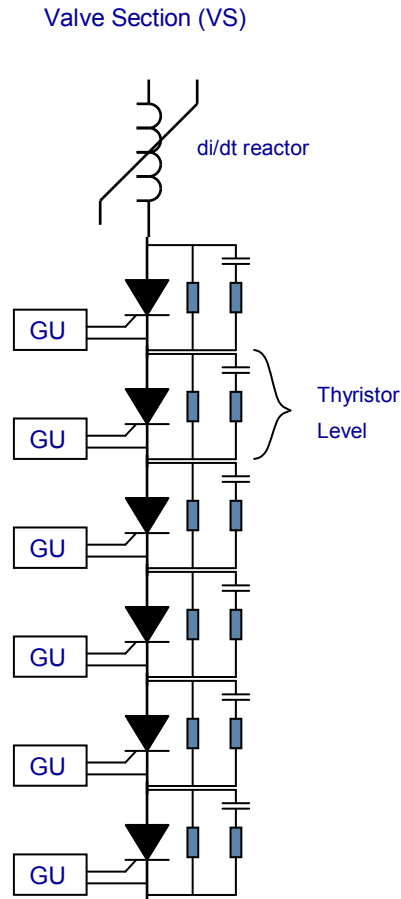


Figure 1.8: Photo of a thyristor module, sourced from Woodhouse, 2007b



**Figure 1.9: Schematic representation of a thyristor valve section, sourced from Woodhouse, 2007b**

Depending on the transmission rating, a number of thyristor modules are then connected in series to form the thyristor valve. These valves are then grouped to form a 12-pulse converter (Figure 1.10) for each pole at each terminal of the DC line for the HVDC conversion. The thyristor valves used in the 12-pulse converter are normally grouped as quadrivalves mainly to economise on insulation and are located in air conditioned buildings known as valve halls. In the valve halls, the valve modules are arranged as stacked structures suspended from the ceiling of the hall to provide mechanical stability with regards to earthquakes, as shown in Figure 1.11 which illustrates a quadrivalve arrangement, while Figure 1.12 shows a schematic of the physical arrangement of the quadrivalve (Stomberg et al., 2010).

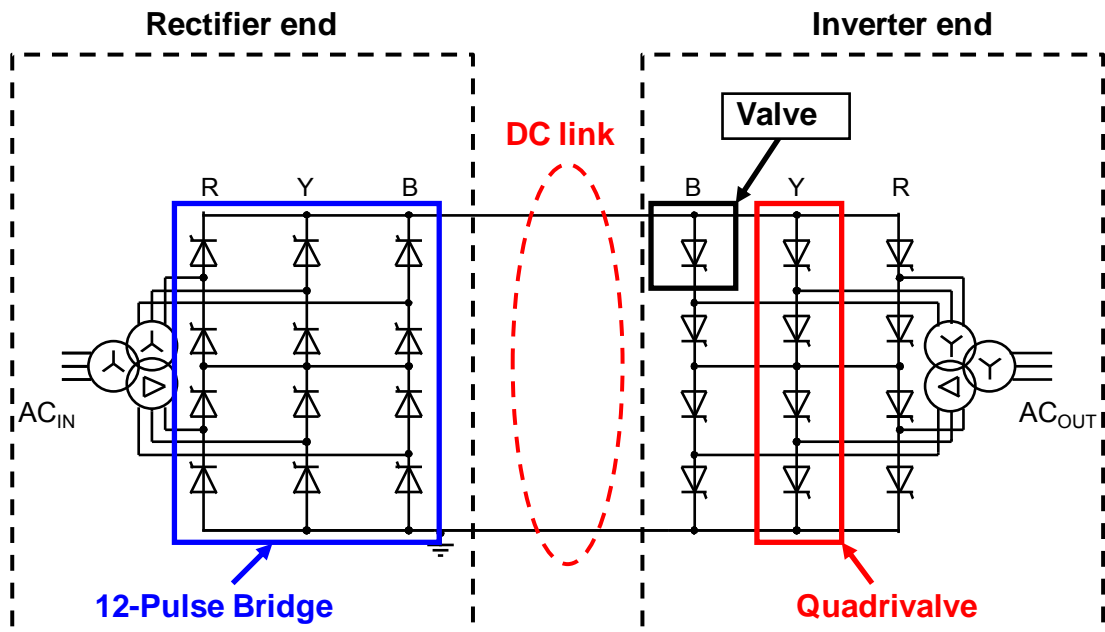


Figure 1.10: Outline of a 12-pulse bridge circuit (Woodhouse, 2007b)

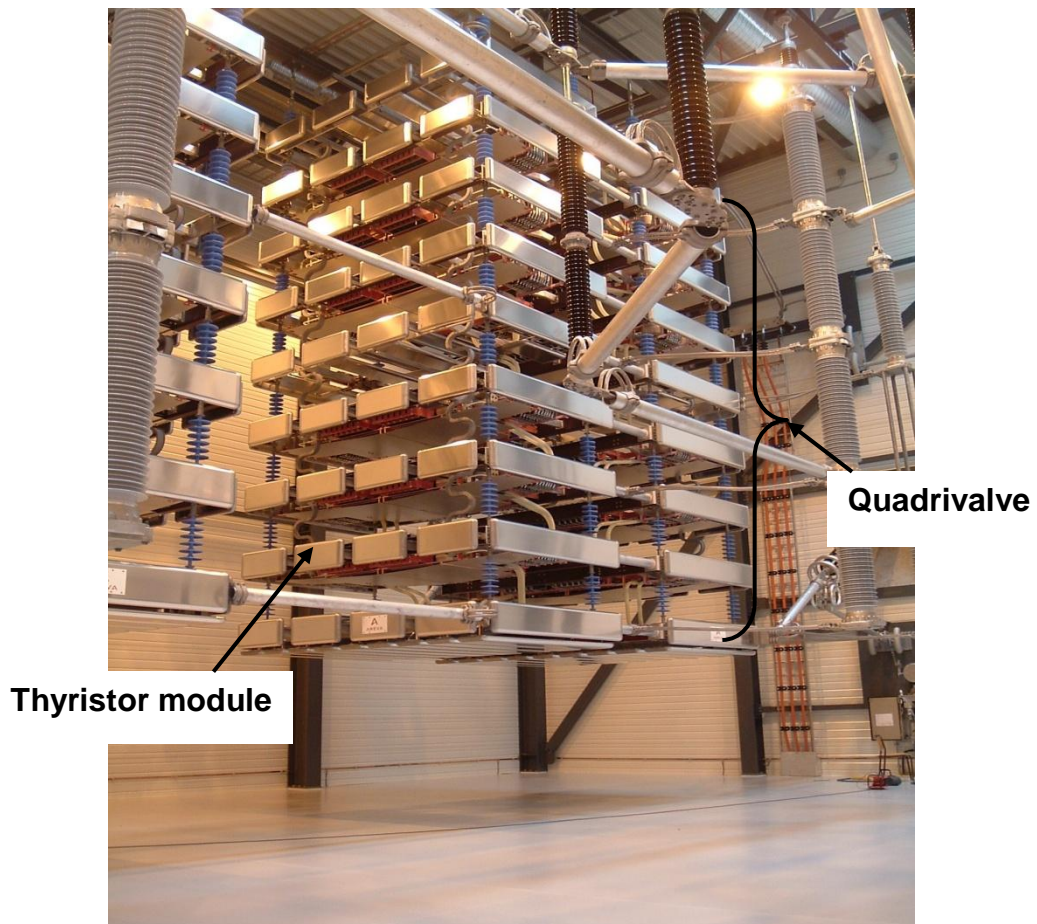


Figure 1.11: Quadrivalve arrangement in valve halls (Woodhouse, 2007b)

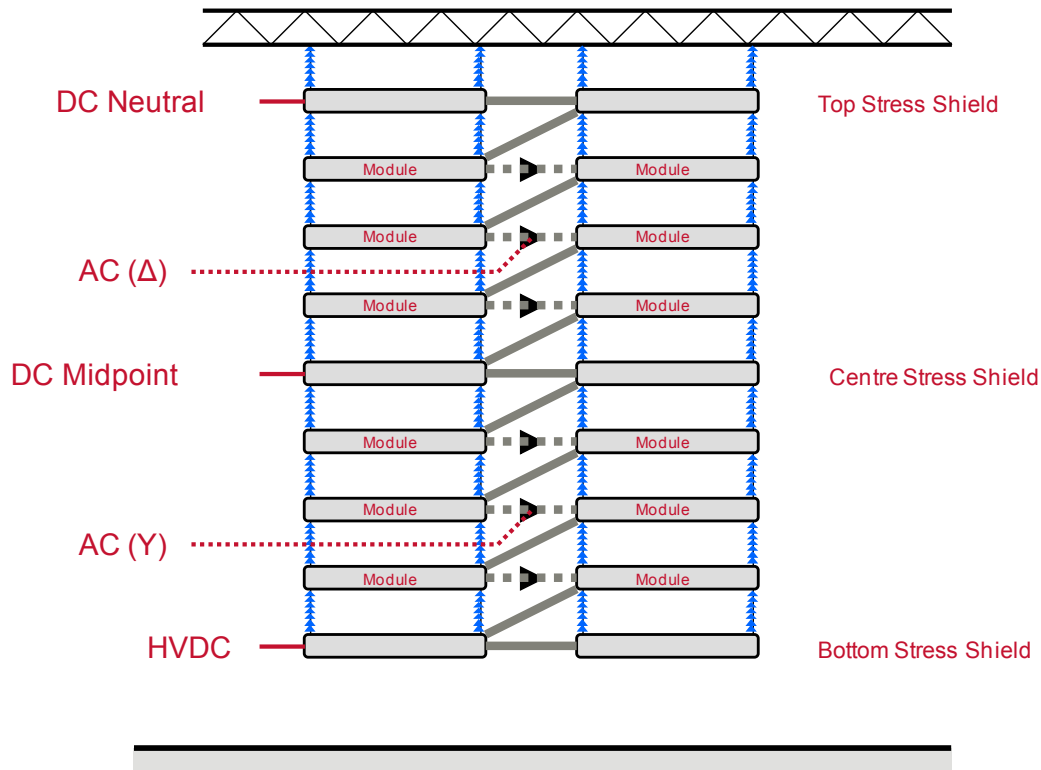


Figure 1.12: Schematic drawing showing the physical implementation of a quadriver

### 1.2.1 Future challenges of power semiconductor devices

With the rapid economic development of large and highly populated countries, such as China, India, Brazil, etc., HVDC transmission is expected to play a major role in their expanding energy demands. Certain studies have actually shown these countries will be better served if the transmission voltage and current is increased above present levels of 3000 A at  $\pm 500$  kV. For example, China is proposing a transmission rating of 4000 A at  $\pm 800$  kV for its future transmission grids (Lescale et al., 2010).

To meet the future challenges in HVDC transmission, many trade-offs and interactions are required to achieve a practical and economic design rating for the thyristor-based converters. For example, this involves optimising the trade-offs between thyristor parameters, the design of solid state valves in which they are fitted, and the design of the converter system in which the valves will be used. However, one important trade-off parameter concerns the

diameter of the silicon semiconductor of the thyristor. For a fixed diameter of silicon, the voltage and current ratings are inversely related. Thus, to achieve a 4000 A capacity rather than 3000 A, a 125 mm diameter silicon wafer would require lowering the voltage rating from the present level to around 7 kV, leading to more thyristors to be connected in series to achieve the given total blocking voltage therefore increasing the cost and size of the HVDC transmission system. To compensate for this trend, thyristors with larger diameters, e.g. 150 mm diameter, are being sought for implementation in the future (Woodhouse, 2007a).

Another alternative route to improve a thyristor performance lies in improving the silicon technology. However, since silicon technology is today considered mature, and major breakthroughs are not anticipated (Linder, 2010a), the attention of engineers is increasingly aimed at developing maintenance-free valves for future transmission schemes. One area, where technological improvement still remains possible, is the design and performance optimisation of the semiconductor device housing. In fact, what was previously considered to be a mere container is today a major limitation and contributes a significant amount of the development cost of power electronic systems (Linder, 2010b). This thesis focuses on package development area for power thyristors that require a high level of reliability.

### **1.3 NEWTON project overview**

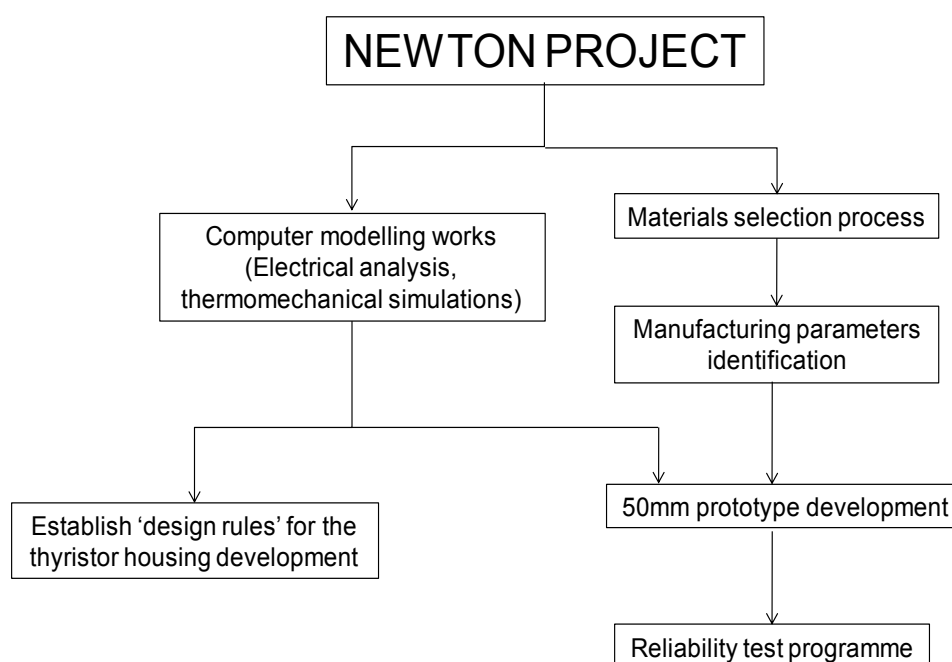
The development trend in high voltage semiconductor packages mirrors in many ways the progress in other areas of the electronics industry, e.g. microelectronics, where the focus is to utilise low cost, light weight, environmentally friendly and high performance materials (Goosey, 1999). However, unlike semiconductor devices used in microelectronics, where miniaturisation of components is the pathway (Test, 1988, Tummala R R, 2005), components for high voltage applications are anticipated to be designed to a larger size and with fewer numbers being used (to minimise cost and complexity) for future high voltage schemes.

As illustrated in Figure 1.5, the thyristor housing has traditionally been made of ceramic materials and has demonstrated an excellent history of reliability and performance because of its hermetic and wear resistant nature (Lips, 1998). Nevertheless, the main disadvantages of ceramic housings today are their processing cost and weight. An alternative material class that can potentially overcome these limitations of the current packages is polymers. Unlike ceramics, some advantages polymers provide are relatively low cost, light weight, good formability and recyclability. However, some drawbacks of using polymers are: (1) they are non-hermetic (Vettraino et al., 1999) – leading to flashover or partial discharge failure in high voltage applications, (2) expensive manufacturing routes, (3) and sometimes varying properties over a wide temperature range.

The NEWTON project (New Thyristors for Transmission & Distribution Applications) was a Technology Strategy Board (TSB) funded project (Ref: H0163B) between Dynex Semiconductors Ltd, Areva T&D UK Ltd and Loughborough University, and aimed at developing a new low cost packaging for fully bonded large area silicon wafers that were under development in a parallel TSB funded programme. The research activities of this project focussed on a 'replacement' hockey-puck type thyristor package, where the ceramic housing was substituted with a polymer material. Although attempts to develop polymer-based thyristor housings had been made previously, the thyristor device being developed here was aimed primarily for use in UHVDC applications (typically for  $\pm 800$  kV requirements) in technologically developing countries, such as China, India, Southern Africa, and South America. This research programme would eventually lead to the development of a new state of the art 150 mm high voltage thyristor device for use in HVDC solutions (Woodhouse, 2007a).

For this project, Loughborough University (LU) was responsible for the material selection of the housing, manufacturing process identification, housing design, and reliability studies for the new polymer-based package.

The different technical activities involved in the project are depicted in Figure 1.13.



**Figure 1.13: Overview of LU technical activities in NEWTON project**

The PhD research project that is reported in this thesis, formed part of these Loughborough University activities and focussed on the study of the polymeric package behaviour and improving its design. The research activities were divided into two main groups, namely (1) computer modelling, and (2) reliability studies. In the computer modelling studies, because the housing would experience electrical stresses and temperature excursions during service, electrical and thermo-mechanical simulations were performed. Together with improving the package design and performance, the studies also aimed to establish design guidelines for future thyristor housing development. On the other hand, to identify whether the polymer material is appropriate for the thyristor housing from both performance and commercial aspects, reliability studies were performed. These tests were carried out on a 50 mm prototype developed in the NEWTON project and aimed at revealing different failure mechanisms that would potentially cause the package to fail. The research findings can be expected to assist in the development of polymeric housings of higher reliability in the future.



To address the different objectives of this research project, this thesis has been structured into four parts, namely (1) project background and research methodology, (2) the prototype development, (3) housing development and reliability investigations, and (4) research conclusions. The project background and research methodology are discussed in Chapters 2 to 5. Chapter 2 describes different thyristor housing designs, while Chapter 3 discusses the different failure modes of thyristor housings. Chapters 4 and 5 respectively overview the general research approach, and the main research methodology (i.e. finite element analysis) used to study the package performance in this project.

The 50 mm prototype development using a series of computer modelling studies is discussed in Chapters 6 to 8. In Chapter 6, the computer modelling studies investigating the electrical behaviour of the 50 mm polymer prototype housing are discussed, while simulation studies aimed at improving the prototype design are reported in Chapters 7 and 8. Because localised electrical stresses were observed to occur in the polymer housing, an electrical modelling study aimed at reducing the electric field magnitude in the regions of concerns is overviewed in Chapter 7. Chapter 8 describes the influence of different housing parameters, such as the flange depth, housing thickness, etc., on the electrical performance of the housing. These results have then been compared with moulding simulation results, before establishing the final design of the prototype. The third part of the thesis describing the reliability investigation on the 50 mm prototype and the development of a larger diameter housing development are respectively highlighted in Chapters 9 and 10. Chapter 9 discusses another simulation-based study to investigate the thermo-mechanical behaviour of the polymer housing, and the reliability of the manufactured 50 mm prototype when it is exposed to different temperature loading conditions. On the other hand, Chapter 10 describes the influence of different geometrical parameters on the electric field magnitude in the housing and discusses the design of a 125 mm housing using the results from early case studies and the Taguchi Method of



Experimental Design. The research conclusions and scope of further work are then finally outlined in Chapter 11.

## **2 Review of thyristor housing designs**

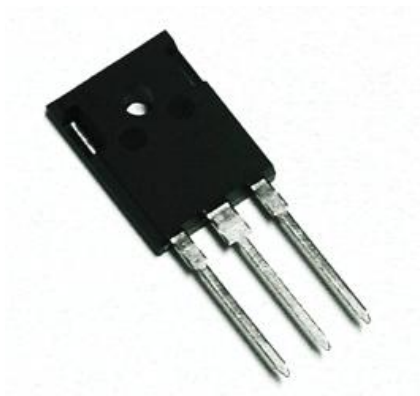
### **2.1 Introduction**

Electronic packaging refers to the integration of semiconductor devices into a robust electronics system that can withstand environmental conditions and perform reliably over a certain period of time (Barlow III, 1999). Compared to traditional mechanical packaging, electronic packaging aims to provide the electronic circuit with power and signal interconnections, a heat dissipation pathway and a protected environment to prevent contamination, mechanical damage and electronic interference. Typical electronic systems are comprised of several levels of packaging, namely (1) the device and carrier, (2) motherboard or printed circuit board, and (3) enclosure, and each packaging level has distinctive types of interconnection devices associated with it. Packaging of electronic systems has evolved to become today a major cross-disciplinary field in engineering. In fact, with packages today moving from bulky expensive materials, such as ceramics and metals, to predominantly plastics and with increasing environmental regulations (Nei et al., 2007), electronic packaging is expected to play a dominant role in the design of electronic systems.

Since their introduction to replace the mercury-arc valves used in HVDC transmission schemes during the late 1960s, high voltage thyristors have also evolved to accommodate higher performance and demanding operating requirements. The thyristors used in high power converter stations are today required to have a very low failure rate. Since the failure rate cannot be zero in practice, a series of redundant devices are normally provided so that a small number of thyristor are allowed to fail without having to immediately shut down the converter station to undertake repair. Any failed devices are then replaced during planned maintenance periods (typically 2 years for HVDC) (Woodhouse, 2007a). In such situations, it is therefore important that the

thyristors have a high level of reliability for long periods of time, and be protected from different failure causes.

Thyristors are available in various package design configurations depending on their power levels. Low power thyristors, as depicted in Figure 2.1 (a), are commonly available as small plastic packages consisting of a silicon chip; medium power thyristors (Figure 2.1 (b)), that comprise of a silicon wafer, are available as stud-mount configurations. For high power applications, e.g. high voltage transmission, press-pack (or hockey-puck) thyristors (Figure 2.1 (c)) are used, because they allow efficient cooling and appropriate stacking for series connection (Rashid, 2007). As shown in Figure 1.6 in Chapter 1, the basic building block of such high voltage thyristors is the silicon wafer. Such wafers (Figure 2.1 (d)) are normally manufactured from highly pure monocrystalline silicon and have an aluminium metal pattern deposited on them. Because the integrity of the silicon wafer (along with its other components) is critical for the long term reliability of a power thyristor, the housing also needs to be reliable to act as an effective barrier to protect the basic unit from ingress of harmful environmental contaminants, and also have appropriate mechanical properties to prevent it from damage due to clamping loads when the thyristors are clamped.



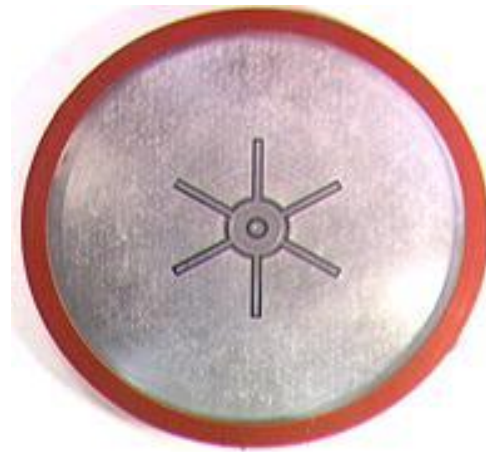
**(a) Low power thyristor**



**(b) Stud-base thyristor configuration**



**(c) Press-pack (or hockey-puck) thyristor construction**



**(d) Photo of a silicon wafer**

**Figure 2.1: Typical thyristor packages types**

An extensive review of the literature was conducted during the initial stages of the NEWTON project to review different thyristor package designs developed in the past. This aimed to assist the development of initial conceptual designs (discussed in Chapters 6 to 8) and also identify potential intellectual property rights issues that may be relevant to the NEWTON developed device. From the literature review, various studies performed in the past, e.g. Tadros et al., 1989, Welleman et al., 2003, N. Monsur et al., 2006, were observed to focus on improving the electrical and thermal performance of high voltage thyristors. Various patents for different thyristor housing designs were also found to have been awarded over the years, as improved performance became necessary. A summary of the patents describing thyristor package designs can be referred to in Appendix 1.

This chapter aims to provide an overview of some of these patents, and identify the design features that improve their performance and reduce failures. Section 2.2 presents examples of some common hockey puck thyristor housing configurations, while key design elements included in the thyristor to improve its design and reduce potential failure causes, e.g. moisture ingress inside the device, are highlighted in section 2.3. Finally,

examples of some patented designs aimed at mitigating common failures due to short-circuit and explosion are reviewed in section 2.4.

## **2.2 Thyristor packages**

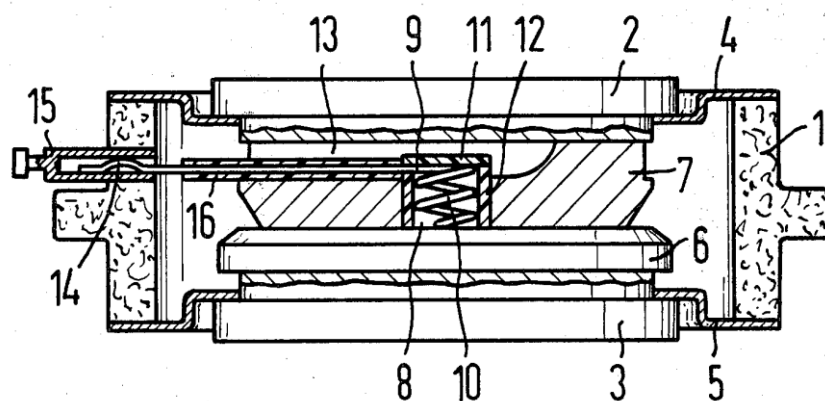
Although a review of different patents has shown the existence of certain non-hermetic thyristor where the main package body is comprised of polymeric materials (e.g. epoxy), the hermetic press-pack configuration made of ceramic has been the dominant technology over the years. A hermetic housing configuration in its simplest definition means being sealed so that a package is gas tight, and prevents intrusion of contaminants, such as liquid, solid or gas, for an indefinite period of time (Madduri et al., 2008). Such packages have traditionally been used in military, aerospace and some commercial applications, and have demonstrated higher performance and long-term reliability, compared to non-hermetic packages which are vulnerable to moisture for example (Ardebili et al., 2009). Traditional materials used to build hermetic housings have included ceramic, metal and glass because of their non-porous characteristics and their consistent properties across a range of temperatures. Examples of some patented hermetic and non-hermetic (polymeric) housings are discussed in sections 2.2.1 and 2.2.2 respectively.

### **2.2.1 Hermetic housing designs**

Figure 2.2 shows an example of a one-part hermetically sealed thyristor housing developed by Bahlinger et al., 1975, while another variant of a hermetic thyristor, a two-part housing described by Cleford, 1970, is illustrated in Figure 2.3. The thyristor assembly shown in Figure 2.2 comprises of two metal cover plates (2, 3), sandwiching the thyristor, and enclosed in an alumina housing (1) to prevent ingress of any harmful contaminants. The metal plates engage respectively the cathode and anode of the thyristor by close pressure contact, while connection to the gate electrode of the thyristor is established by a gate control lead (9) of beryllium bronze.

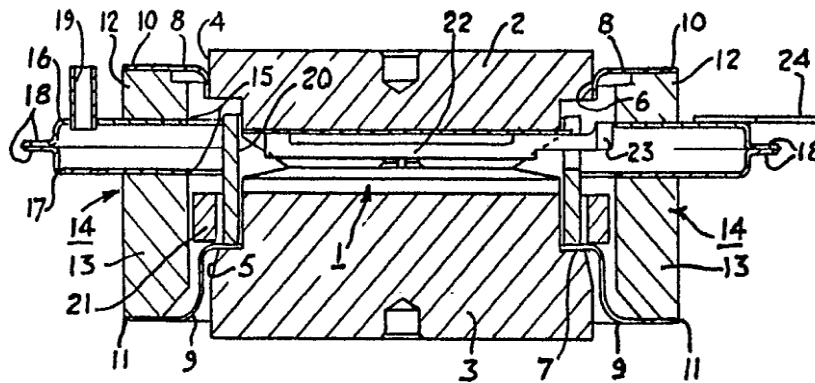
On the other hand, for the two-part housing (Figure 2.3), projecting flanges (16, 17) are welded together on the outside to join together the two separate segments of the housing, while the inner edges of the flanges are sealed to join the housing. In this design, the thyristor element (1) is sandwiched between pairs of copper pole pieces secured to the inner periphery of an annular flange (8, 9), and its outer periphery is secured to a corresponding part of an annular ceramic housing (14).

Commercial HVDC thyristors (Figure 1.6) available nowadays actually also share different features common to the one-part and two-part housings described above. For example, as in the one-part and two-part devices, current thyristor devices are also based on ceramic material. They also consist of anode and cathode copper pole pieces for electrical connectivity and heat removal purposes. The different components in the device, namely the copper pole pieces, the molybdenum discs, and the silicon wafer arranged in a stacked structure, also engage each other by close pressure contact. As in the case of the two-part housing, the thyristor device is also assembled by welding together metal flanges that are part of the housing and copper pole pieces.



**Figure 2.2: One-part hermetic housing** (Bahlinger et al., 1975)

1 – Aluminium oxide housing wall; 2, 3 - metal cover plates (cathode and anode respectively); 4, 5 are metal plate of kovar material (iron, cobalt and nickel alloy); 6 - wafer; 7 - metal plate; 8 – recess; 9 - metal conductor; 10 – spring; 11 - insulating plate; 12 - insulating ring; 13 - slot; 14 - end of control line; 15 - socket



**Figure 2.3: Two-part hermetic housing (Cleford, 1970)**

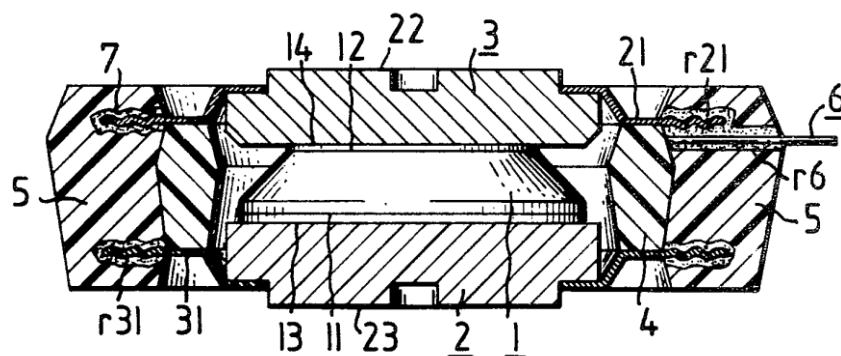
1 - wafer; 2, 3 - copper heat sinks; 4, 5 - the heat sinks circumferential periphery; 8, 9 - annular flange; 14 – housing; 12, 13 - two parts of the housing 14; 16, 17 - dished shaped flange; 19 - conduit from flange 16; 20 - ring, made of an electrically insulating material; 21 - ring made of desiccant material to maintain a dry interior; 22 - gate contact; 24 - external electrical connector; 23 - electrical tab to provide connection between contact 22 and external connector 24

## 2.2.2 Polymeric housing designs

Together with the hermetic package configuration, the patent review revealed that development of polymer-based high power thyristor housings have also been attempted in the past. For instance, devices developed by Brandt et al., 1980, Gerstenkoper et al., 1980, Merlin et al., 2003, Rohsler, 1982, and Podlesak et al., 1996 used polymers, such as epoxy resins and polyimide, for their housing.

One example of such a polymer housing for a press-pack thyristor, developed by Brandt et al., 1980, is shown in Figure 2.4. The device depicted here consists of a semiconductor wafer (1) sandwiched between a pair of solid-copper metal bodies (2, 3), mounted on its respective ends (11, 12). An insulating ring (4) made of either mineral or glass fibre reinforced epoxy resin is also provided to centre the metal bodies and semiconductor wafer. Annular copper sheets (21, 31) are hard-soldered to the periphery of the metal pieces. They protrude radially above the insulating ring and are provided with

corrugated edges embedded in the plastic jacket - manufactured by an injection pressing process and made of a thermosetting resin, e.g. epoxy. Although polymers are permeable to moisture, non-hermetic housings can also function reliably as hermetic ceramic packages through the inclusion of certain design features. For instance, for the polymer package developed by Brandt et al., 1980 (Figure 2.4), the moisture resistance property of the device is improved through the use of corrugated edges of the annular copper sheets that are embedded in the plastic jacket of the device. Examples of some other design configurations, that improve the reliability polymer housings and can thereby be extended to the polymer housing developed in the NEWTON project in the future, are described in section 2.3.



**Figure 2.4: Example of a non-hermetic polymer housing (Brandt et al., 1980)**

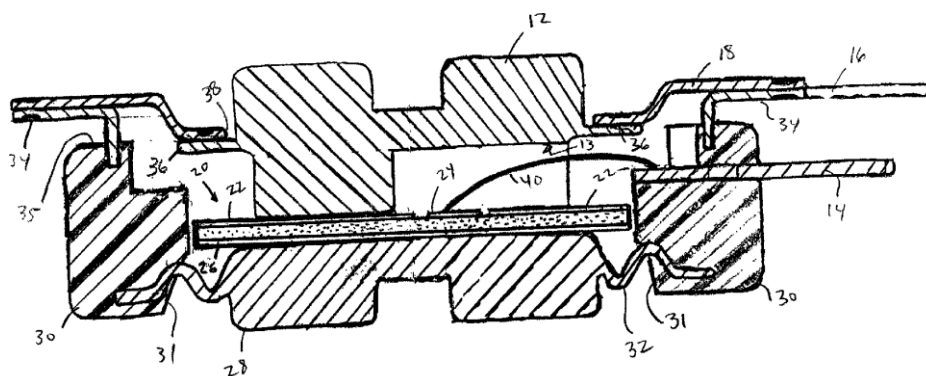
where 1 denotes the thyristor wafer (semiconductor); 2, 3 are metal bodies; 4 - insulating ring, made of mineral or glass fiber reinforced epoxy resin; 5 - plastic jacket of epoxy resins; 6 - tube through which control lead is passed; R6 - powder coating; 7 - powder coating of either epoxy resins, polyester resins, or polyurethane resins; 11, 12 - major surfaces of semiconductor element; 13, 14 - main electrodes; 21, 31 - annular metal strips; r21, r31 - corrugated edge regions

## 2.3 Key design features of thyristors

As highlighted in Chapter 1 and in section 2.1 of this chapter, thyristors require a high level of reliability throughout long service period. As a result, the integrity of different components, such as the semiconductor element, molybdenum discs, the housing, and also an appropriate connection of the



gate lead to the gate electrode of the semiconductor element, is required to ensure the proper functioning and performance of the thyristor device. From the patent literature review, thyristor devices were seen to contain gate leads of different designs. Examples of some common gate lead configurations include the spring-type gate terminal and the wire bond-type gate lead, as shown in Figures 2.2 and 2.5 respectively.



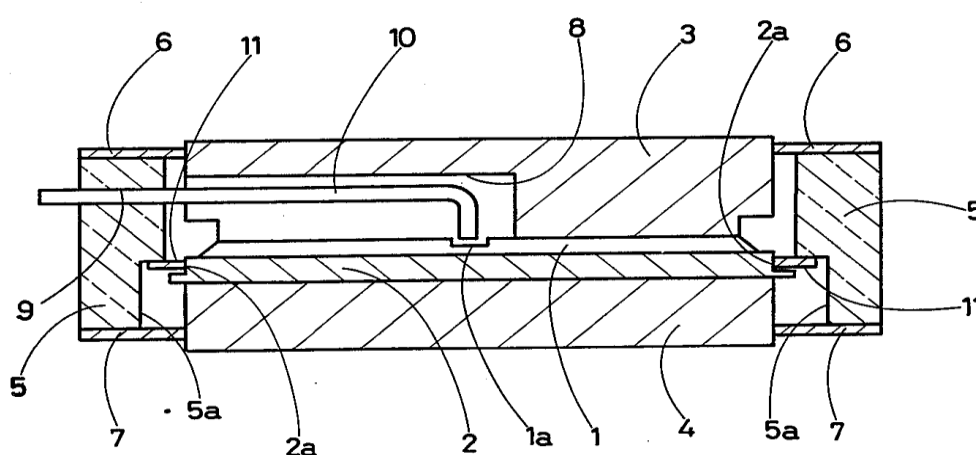
**Figure 2.5: Thyristor device having a wire bond connection gate lead (Merlin et al., 2003)**

where 10 - semiconductor package; 12, 28 - copper pole piece; 14 - Control lead; 16 - Connection terminal; 20 - semiconductor die; 22 - first major electrode; 24 - control electrode; 26 - second major electrode; 30 - insulating ring, made of insulating plastic; 32, 34 - annular flange; 36 - rib; 18 - connector; 40 - bond wire

For the thyristor to function properly, the gate lead and gate electrode of the semiconductor element are required to be in good contact by processes such as welding and pressure contact, and also properly aligned. Different design concepts have actually been proposed in the past to improve the alignment of the gate lead and the gate electrode of the silicon wafer in a thyristor. For example, in the case of a light-triggered thyristor (LTT) (which is also widely used in HVDC power systems and is triggered by high power laser impulse), the alignment of the light guide and the photosensitive portion of the element are essential. An example of such a LTT device whereby the alignment of the photosensitive portion of the LTT element and light guide is optimised is illustrated in Figure 2.6. In this device, an inner positioning ring (11) is attached to the inner wall of the housing (5a) and fixed on a reinforced metal disc (2) on which the LTT is mounted. The inner diameter of the disc is made

slightly larger than the outer diameter of the reinforced metal disc and the inner wall of the housing is machined to accommodate them.

Such a feature can actually also be included in the NEWTON thyristor to improve the alignment of the gate lead and gate electrode of the silicon wafer in the future. In such a device, an inner positioning ring similar to the LTT thyristor component (11) attached to the inner wall of the polymer housing can be used to improve the alignment between the gate electrode of the silicon wafer and the gate lead that is inserted inside a hollow gate tube (similar to the light guide (10)). The inner positioning ring is then fixed to the molybdenum disc of the NEWTON thyristor in a similar configuration as the position ring (11) is joined to the reinforced metal disc (2) in the LTT device. The inner edge of the polymer housing would also require machining to accommodate the positioning ring and molybdenum disc assembly for the improved gate lead and gate electrode alignment. Together with this, because the LTT device consists of a light guide (10) passing through the ceramic housing (5) similar to the gate lead that would pass in the polymer housing of the NEWTON thyristor, potential scopes also exist in the future to develop a novel LTT device that would also comprise of a housing made of polymeric material (instead of ceramic).

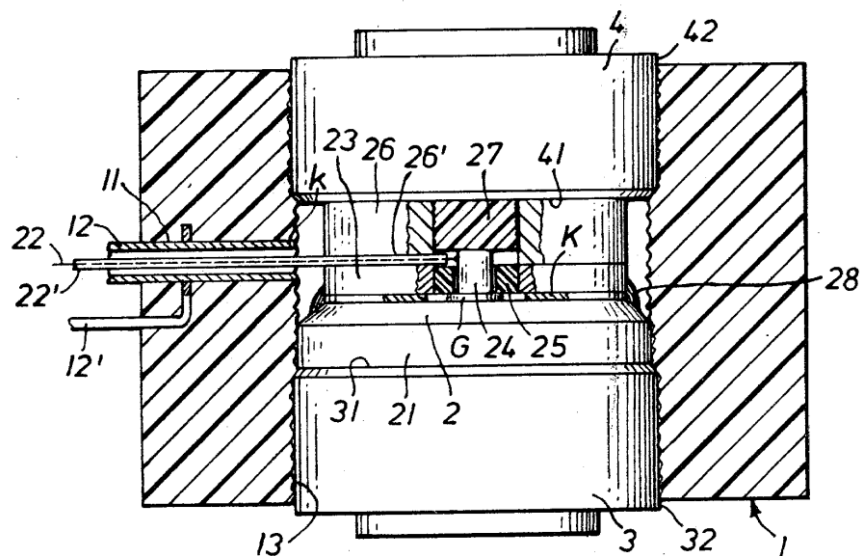


**Figure 2.6: Example of a LTT device where light guide and photosensitive element alignment is improved (Kiyohara, 1983)**

where 1 - light-triggered thyristor element; 1a - photosensitive part of the element; 2 - reinforced metal disc; 3, 4 - electrode members; 5 - insulated

housing of alumina ceramics; 6, 7 - annular flange; 8 - lateral groove to accommodate the light guide terminal 10; 9 - radial hole in insulated housing; 10 - light guide; 11 - positioning ring

Apart from having an appropriate gate lead and gate electrode alignment, the device is also required to resist environmental contamination (e.g. due to moisture and dust) to avoid potential failure during service. Together with using an ideal enclosure, different patented inventions have also revealed ensuring a close fit between the pole piece components and housing can result in a good barrier between the outside environment and basic unit of the thyristor. Examples of such a design feature, that can be extended to the NEWTON polymer housing, are shown in Figures 2.4 and 2.7. Figure 2.4 by Brandt et al., 1980 (introduced in section 2.2.2) describes a sealed housing achieved by the corrugated copper edges which are surface roughened and coated with powdered plastic to improve adhesion with the external resin housing. The powdered plastic is a powdered lacquer of epoxy resins, polyester resins or polyurethane resins. On the other hand, another such design by Gerstenkoper et al., 1980 depicts an interference fit package formed by a toothed profile along the inner side of the package and an external larger diameter of the contacting discs (Figure 2.7).



**Figure 2.7: Interference fit package (Gerstenkoper et al., 1980)**

where 1 - elastomer annular housing; 2 - semiconductor wafer, or thyristor disc; 3, 4 - contacting discs; 11 - radial channel for accommodating gate terminal; 12 - metal tube for accommodating gate terminal; 21 - support disc; 31 - major surface of contacting disc 3; 13 - inner peripheral surface of housing 1; 22 - gate terminal lead; 22' - Teflon sleeve; 41 - major surface of contact disc 4; 32, 42 - outer peripheral surface of contacting discs 3, 4; 24 - silver cylinder, used as control electrode contact; 25 - centering ring, made of electrical insulating material; 23 - silver annular ring; 26 - copper annular ring; 27 - cylindrical plug, made of elastomer material, e.g. viton; 28 - silicone lacquer to fix ring 23, 24, and 25 in relative position

## **2.4 Thyristor device failure modes**

Most thyristor failures occur due to exceeding the maximum operating ratings of the device - with overvoltage and overcurrent operations being more common failure causes. Other failure causes also tend to be due to mechanical damage in the form of excessive forces applied to the terminals during assembly of the thyristors (Littlefuse, 2008). This can lead to internal damage of the thyristor basic unit and crack formation. When the thyristor is electrically or physically abused in such a way, it can lead to either short-circuit or explosion failure. To mitigate potential failures due to these failure modes, various novel design concepts have also been patented over the years. Some housing designs identified from the patent review are described in the following sections.

### **2.4.1 Short circuit failure**

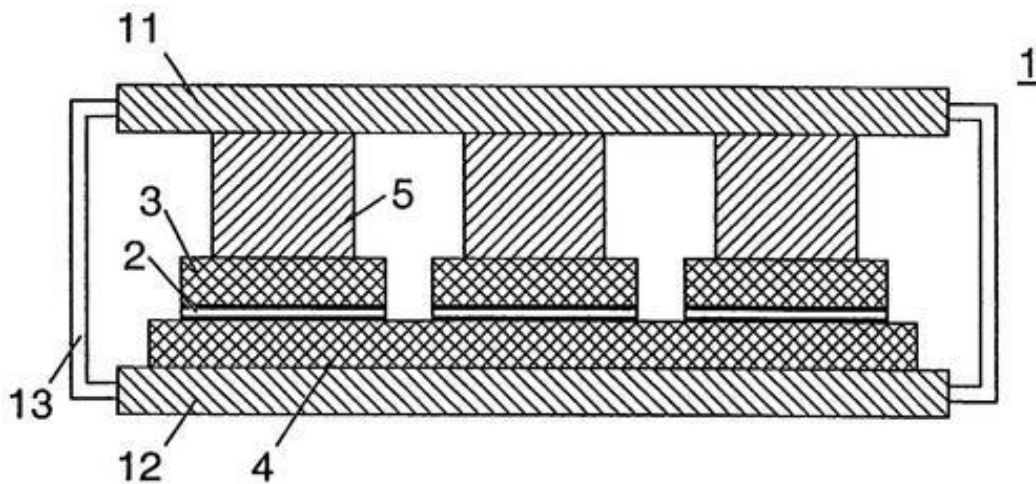
Short-circuit failure can be described as an unwanted low-resistance connection between two electrical circuit nodes, which are meant to be at different voltages. Unintentional short-circuits are usually caused either when there is insulation breakdown, or introduction of another conducting material – thereby allowing charge flow along the unwanted path. If a short-circuit leads

to an electrically overloaded connection or component, it can cause rapid overheating and lead to irreversible damage in other circuit components.

As described in Chapter 1, a number of thyristors are normally stacked in series to achieve the high total blocking voltage required in HVDC converters. In the event of a short-circuit, the silicon chip of the semiconductor device melts locally to form a hot spot over the entire thickness of the device as current flows. In this case, the faulty semiconductor device should ideally form a stable short-circuit and take the entire current to prevent an open circuit and failure of the entire stack (Gunturi et al., 2004). With the help of redundant thyristors that are included in the stacked thyristor assembly, such stable short-circuit failure should allow the non-faulty thyristors to continue operating normally and prevent unnecessary maintenance downtimes of the HVDC power station. The failed devices can then only be replaced during planned maintenance downtimes (typically 1 or 2 years). Different researchers have patented different power device designs aimed at improving their reliability, and also ensuring they continue operating normally due to short-circuit failure. Two such inventions that can also be extended to prevent short-circuit failure of the NEWTON thyristor are described next.

For instance, Gunturi et al., 2004 proposed a novel device design (Figure 2.8) whereby contacting either one or both electrodes of the semiconductor chip with a layer of metal matrix composite (MMC), both the thermo mechanical fatigue life and short circuit failure mode of the power semiconductor device takes longer to occur. This press-pack module design (Figure 2.8) consists of at least one semiconductor device (2) clamped between a conductive base plate (4), and at least one conductive top plate (3) enclosed in a housing (11, 12, 13). The package described here is also comprised of a novel metal matrix composite layer contacted to either one or both electrodes of the silicon semiconductor chip, and forms a eutectic mixture with the silicon material from the chip. The thermal coefficient of expansion of the layer is tailored to match that of the silicon chip to improve the thermo-mechanical property of the sandwich structure. To meet the electrical conductivity performance, the matrix of the layer is normally made of metals, such as silver, aluminium,

copper, or gold, while the reinforcement can be non-metallic, e.g. graphite or ceramic. Examples of such metal matrix composites are Al-graphite, Cu-graphite, Cu-Mo (Gunturi et al., 2004). In the event of a short circuit defect, when the entire sandwich structure consisting of the chip and MMC layer is heated, a conductive layer is formed between the contact layers once the melting point of the eutectic mixture is reached. This melting zone then extends across the entire silicon chip forming a stable conductive channel for the device to continue operating in the event of a short circuit. In this invention, because a MMC layer consisting of a high metallic content is used, a stable eutectic mixture with the Si from the chip is easily formed to ensure a longer operational time of the semiconductor module.

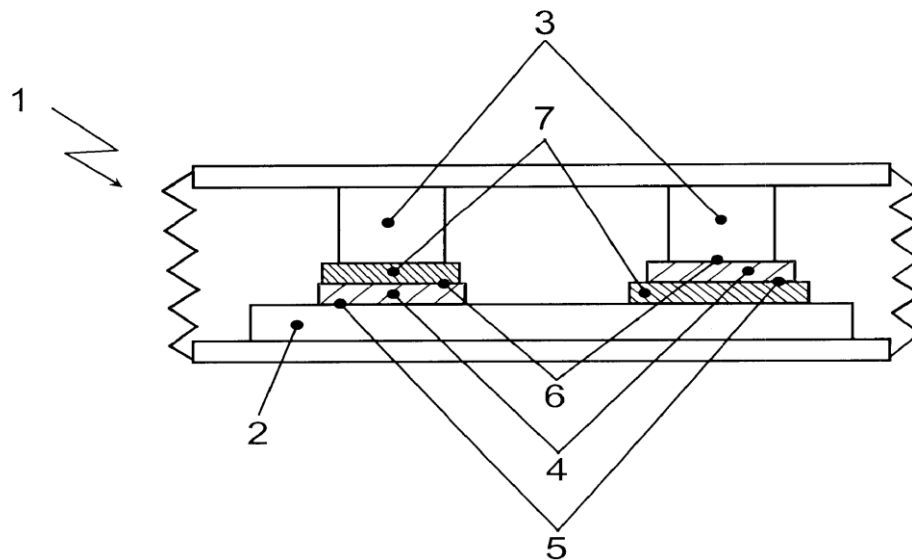


**Figure 2.8: Press-pack semiconductor module (Gunturi et al., 2004)**

where 1 - Press-pack module; 2 - Semiconductor device, chip; 3 - Composite top plate; 4 - Composite base plate; 5 - Contact piston; 6 - Bonding medium, solder; 11, 12 - Module housing power connections; 13 - Housing elements

Another example of a power device design where short circuit defect can be mitigated is illustrated in Figure 2.9 (Lang et al., 1999). In this invention, an additional layer, e.g. silver (which can be a paste, foil, or solder component) is brought into contact with the electrodes of the semiconductor chip. The silver and the semiconductor (e.g. silicon) chip forms a eutectic mixture whose melting point is also below that of two partner materials. In the event of a short circuit, the entire sandwich structure is heated, and once the melting point of

the eutectic mixture is reached, a metallic conductive channel is formed on the contact surface between the silver layer and the affected silicon semiconductor chip. The channel is limited to one part of the chip area, but is able to carry the entire rated current, and thus prevents further heating of the rest of the chip and allowing the device to continue operating normally.



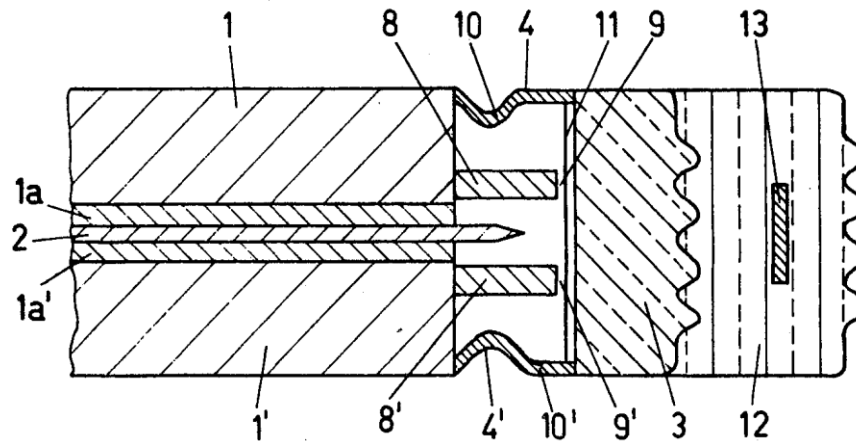
**Figure 2.9: Semiconductor device (Lang et al., 1999)**

where 1 - Housing; 2 - Substrate; 3 - Contact piston; 4 - semiconductor chip; 5, 6 - main electrodes; 7 - Layer (silver)

## 2.4.2 Explosion failure

Failure due to explosion in a semiconductor device normally originates when current initially flows at a defective point of the semiconductor power component to cause the silicon element to melt and evaporate. An arc is subsequently formed which spreads in a loop-shaped configuration to the connecting pieces of the housing that weld them together. This makes the pressure in the arrangement increase explosively causing the housing to be destroyed mechanically (De Bruyne et al., 1979).

Examples of some housing configurations proposed by De Bruyne et al., 1979 to reduce the pressure build-up in the housing (thereby mitigating failure due to explosion) are illustrated in Figures 2.10 to 2.12.



**Figure 2.10: Semiconductor device with reinforced housing** (De Bruyne et al., 1979)

Figure 2.10 shows a conceptual thyristor design aimed at reducing the severity of failure due to explosion. The device consists of a ceramic enclosure (3) enclosing a thyristor device (2) arranged between copper plates (1, 1'), and molybdenum plates (1a, 1a') contact pieces. To reduce the pressure build-up and explosion risk, the device also consists of different design features namely:

- current conductors (8, 8') made of copper surrounding the contact pieces - in the event of defect points that would cause arc formation and pressure build-up, the current conductors would retain the arc formed firmly on the conductors and prevent them from spreading to the contact pieces (1, 1', 1a, 1a') and the connecting pieces (4, 4')
- thermally and electrically insulating plastic coating (10, 10', 11) which is made of a slow vaporising plastics e.g. Sylgard (a silicone resin material), or Teflon (a tetrafluoroethylene fluorocarbon polymer)) – the plastic coating, which is found on the connecting pieces and interior of the housing, aims to retard the development and propagation of arc that would result in the explosion of the device



- a reinforcing element (12) made of plastics such as polyvinylchloride joined in the radial direction with the housing (3). This element that can optionally be included in the housing is comprised of a fibreglass or steel ring inlay aims at increasing the mechanical strength of the housing and reducing damage due to explosion.

Other housing embodiments also disclosed by De Bruyne et al., 1979 aimed at mitigating damage due to explosion, are also shown in Figures 2.11 and 2.12. The device in Figure 2.11, which consists of an explosion guard (14) made of cast resin or silicone rubber, reduces the risk of damage to other parts in an installation by intercepting any hot gases and fragments generated by an explosion. In this arrangement, the space in between the housing (5) and the guard, which is considerably larger than the space (16) enclosed by the housing (5), reduces damage due to explosion by keeping the pressure and temperature build-up to a minimum. The guard also has improved explosion resistant properties due to its improved mechanical strength properties. This is achieved by providing it with reinforcing rings (17) to absorb radial forces due to pressure build-up. Compared to the housing guard in Figure 2.11, the arrangement in Figure 2.12 also improves resistance due to explosion by using a housing design that acts as an overpressure valve. The outer housing here is composed of flow resistance (18', 19') and sealing lips (20) which function as an overpressure valve at the end faces of the device. In the event of an explosion, the sealing lip (20) deforms in the manner shown by the dash lines to permit the controlled release of explosion gases in the direction shown in the figure.

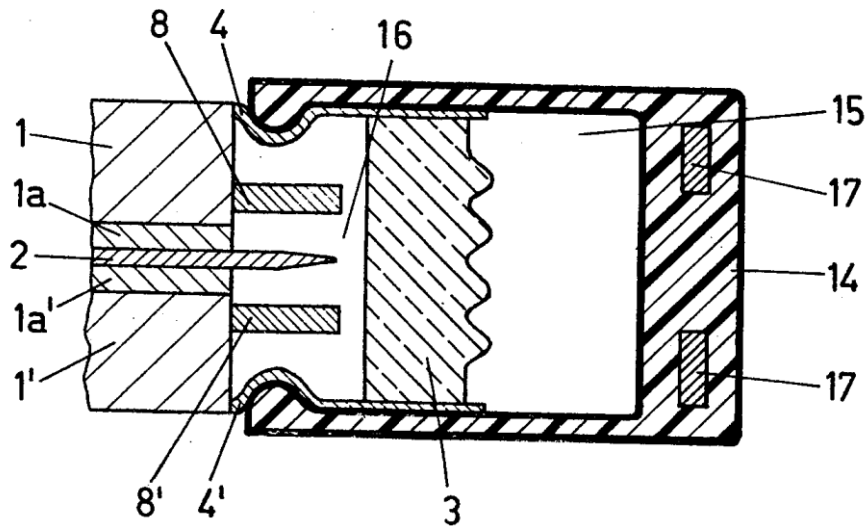


Figure 2.11: Explosion guard housing (De Bruyne et al., 1979)

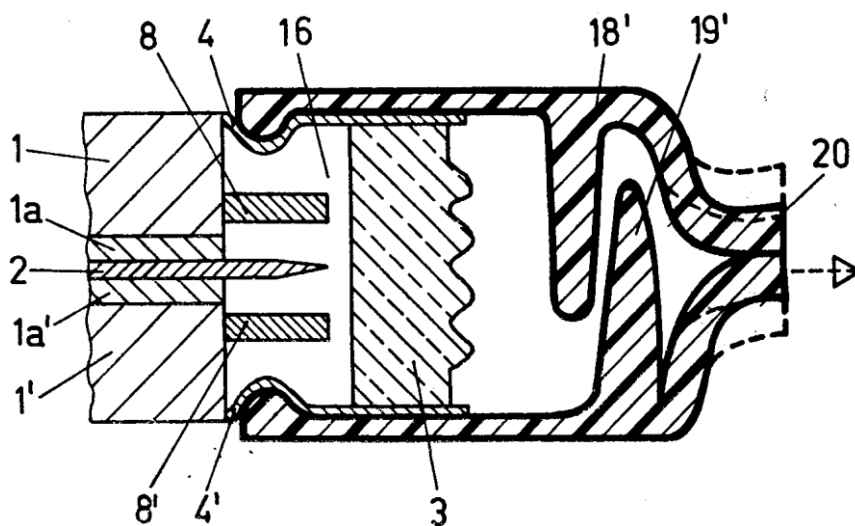


Figure 2.12: Overpressure valve like housing (De Bruyne et al., 1979)

## 2.5 Summary

In this chapter, an overview of different design concepts for press-pack thyristor packages has been described. The review summarises a study of different patents and published literatures, and also aims to avoid potential commercial and intellectual rights issues that may occur with respect to any thyristor package design that may be developed in the future. From the literature review, different thyristor design configurations have been observed

to have been developed in the past to meet requirements for improved performance. They have also helped identify different housings that contain key design features aimed at mitigating failure modes, such as short circuit and explosion, common to these devices. An overview of the different housing designs reviewed in this chapter is described next.

From the review of different published literatures, it was seen that attempts to develop hermetic and polymer-based non-hermetic thyristor housings have already been made in the past. Hermetic thyristor housings that were developed were based on either a one-part or two-part configurations. Materials that were used to build them were ceramics and aluminium oxide, whilst for non-hermetic housings polymers were used. Examples of polymeric materials used in the past include epoxies and polyimides.

On the other hand, to mitigate failures due to short-circuit in semiconductor devices, previous inventions have consisted of contacting the electrodes of the semiconductor element with either a layer or foil consisting of a material that can easily form an eutectic mixture with the semiconductor material in the event of a short circuit. When the sandwich structure of the semiconductor element and contacting material is heated during the short circuit, a stable conductive channel should then form between the contact layers once the melting point of the eutectic mixture is reached. This should ensure a longer operating time of the failed semiconductor module and avoid unplanned stoppage of the HVDC system. Examples of materials that have been used in previous inventions for the contacting layers have been silver, or metal matrix composites e.g. aluminium-graphite, copper-graphite, copper-molybdenum. Finally devices aimed at reducing failure due to explosion have consisted of adopting approaches, such as attaching a reinforcing element around the semiconductor housing to improve the strength. Examples of reinforcing materials that have been utilised in the past include plastic elements, such as polyvinylchloride or cast resin with optionally a fibreglass or steel ring inlay included in it to absorb radial forces due pressure increase more effectively.

## **3 Failure modes of thyristor devices**

### **3.1 Introduction**

In any product development and design effort, the goal is to produce a new product that is successful in the marketplace and results in maximum value to the manufacturer and user of the product. To achieve this goal, the product must be effectively designed and developed, and be of high reliability.

Reliability is defined as the probability that a device will perform its required function under stated conditions for a specific period of time. The longer the required lifetime, the greater is the demand on reliability to avoid potential failure (Di Giacomo, 1997). According to Bajenescu et al., 1999, one may distinguish failures as being of three types. First, there are failures that appear during the early period of life of a component, called early (or infantile) failures. They can be due to faulty manufacture or insufficient quality control during production, and can be reduced by a systematic screening test. The second type of failure is known as wear-out and is generally an indicator of the component ageing. Finally, accidental failures (the third category) are due to unexpected phenomena, such as sudden voltage increases, that can strongly influence the component quality and reliability. They appear randomly, and cannot be eliminated by screening (or burn-in) tests or preventive maintenance for example.

Most failures happen due to a complex set of interactions between the load acting on and within the system, and the materials and elements comprising the system. Dasgupta et al., 1991 categorised failure into four conceptual models, namely (1) stress-strength, (2) damage-endurance, (3) challenge-response, and (4) tolerance requirement. The stress-strength failure model identifies failures that are due to stresses exceeding the component strength (e.g. a steel bar in tension), while the damage-endurance model relates to

damage that accumulates irreversibly (e.g. corrosion, dielectric breakdown), and causes failure when the endurance limit of the device is reached. In the tolerance-requirement model, the system performance characteristic remains satisfactory only when the tolerance remains within requirement, whereas the challenge-response model relates to system failure due to an element that fails to respond when exposed to a stress. The development of a reliable product requires a thorough identification of potential failure mechanisms, i.e. the physical processes that may cause failure of the product by one or more of the conceptual models described above.

According to Dasgupta et al., 1991, different failure mechanisms, e.g. yield, dielectric breakdown, corrosion, etc., that are common in engineering systems can be broadly divided into two categories namely, overstress and wear-out. A description of the different overstress and wear-out failure mechanisms (identified by Dasgupta et al., 1991), is presented in the following sections. Section 3.2 describes the overstress failure mechanisms, while failures that commonly occur in the electronic systems due to wear-out are reviewed in section 3.3. Relevant failure mechanisms that are anticipated to be potential causes of failure in non-hermetic thyristors are then reviewed in section 3.4, before the concept of reliability and how it has been 'designed' in during the development of the polymeric thyristor package are defined in sections 3.5 and 3.6.

### **3.2 Overstress failure mechanisms**

Overstress failures are defined as sudden catastrophic failures that happen due to a single occurrence of a stress event exceeding the intrinsic strength of a component (Dasgupta et al., 1991). Different investigations in the past have identified various overstress failure mechanisms that happen for example due to mechanical and electrical stresses, and which can be responsible for failures in both hermetic and non-hermetic electronic packages when they exceed the safe limit. Some examples of failure mechanisms identified by

Dasgupta et al., 1991 that fall into this category include large elastic deformation, plastic deformation, fracture and yield.

From studies by Suhir, 2007, Xie et al., 1998, Yao et al., 2003, etc., failure due to large elastic deformation in electronic devices have been seen to occur most often in slender structures, such as leads, wirebonds, etc. Although the materials behave elastically when they are deformed and no permanent change occurs, such failure results from excessive deformation due to overstress. Examples of some external factors that can contribute to such an overstress are the applied mechanical and vibration loads (Dasgupta et al., 1992). Plastic deformation and fracture are also other examples of failure mechanisms that result from mechanical stresses. Plastic deformation occurs when a component is stressed past its yield strength during operation. This then leads to plastic strain and permanent deformation due to a permanent change in the material. This subsequently fails the electronic package. Plastic deformation may or may not constitute a failure depending on the application. In electronic devices, various investigations, e.g. Sun et al., 2008, Dresbach et al., 2007, have shown that plastic deformation is a common occurrence in metallic elements, such as bond wires, solder, copper plated vias and metallisation.

Failure due to fracture in electronic systems can occur in two forms: brittle and ductile fracture. Brittle fracture originates from high stress concentrations at local microscopic flaws in brittle materials under overstress. The excessive overstress then causes sudden propagation of the dominant micro-crack and results in rapid failure. Such failures are common occurrences in hermetic packages made of ceramic and glass (Mathieu et al., 1993), and can lead to failure of the actual device through ingress of moisture and other corrosive substances. In ductile fracture, failure occurs due to sudden propagation of a pre-existing crack in the material under external stress. Compared to brittle fracture, ductile crack propagation is preceded by yielding that occurs at the crack tip. In electronic systems, such failures can arise in materials such as solder, aluminium and gold wires (Dasgupta et al., 1991).

Apart from the previously described mechanical failure mechanisms, electronic package failure can also be driven by exposure to electrical stresses above the design level. As identified by authors, such as Wang et al., 2003 and Dasgupta et al., 1991, dielectric breakdown is one common example of an electrical failure mechanism that contributes to failure of polymer-based electrical and electronic devices. It occurs due to failure of the dielectric of an electrical component when the applied voltage across the device stresses the dielectric beyond its dielectric strength, resulting in a sudden transition from an insulating to a conductive state.

### **3.3 Wear-out failure mechanism**

In the wear-out failure mechanism, failure occurs when the accumulation of incremental damage exceeds the material endurance limit. Dasgupta et al., 1991 categorised failures, such as fatigue crack initiation and growth, creep, wear, interdiffusion, corrosion, and radiation induced damage, as common examples of wear-out failure mechanisms occurring in electronic packages. An overview of these failure mechanisms is described next.

Fatigue failure usually occurs at stresses much below the ultimate tensile strength, and results from accumulation of damage when a component is exposed to a cyclic stress. Such failure can comprise of two stages, namely crack initiation and crack propagation, or the crack may develop from an existing point or discontinuity, such as a defect in the material grain structure, because of a local stress concentration. Once initiated, the crack then propagates under cyclic stress until the structure is weakened it becomes unstable leading to overstress failure. Past studies, e.g. Omiya et al., 2005, and Regard et al., 2008, highlighted such problems are encountered at locations, such as bond wires, copper plated vias, solder, etc., in electronic devices.

Creep and wear are also other examples of mechanical wear-out failure mechanisms in electronic devices. Compared to plastic and elastic

deformation, creep is a time-dependent deformation. The deformation mechanism in polymers due to creep is different from those in metallic and ceramics structures because of their microstructure. In metals, it is due to grain boundary sliding, and intergranular or transgranular void migration, while in polymers the deformation is due to polymer chain reorientation. According to Dasgupta et al., 1991, failure due to creep is an issue at sites, such as solder joints and in printed circuit base materials at soldering temperatures.

On the other hand, wear refers to the erosion of material resulting from the sliding motion of two surfaces under the action of a contact force. It can be grouped into five categories namely: (1) abrasive (when a hard material is sliding against a soft material), (2) surface fatigue, (3) corrosive (chemical), (4) thermal (mainly in polymers), and (5) adhesive wear which is common in connector mating surfaces in electronic packages.

Examples of other failure mechanisms driven by chemical agents in electronic packages are interdiffusion and corrosion. Compared to diffusion which is a mass transport process at the atomic level, interdiffusion refers to a mutual mass transport process that occurs when two different materials are in intimate contact. Rather than being considered a primary failure mechanism, diffusion plays a role in other failure mechanisms, such as corrosion, creep and electromigration. In electronic devices, it can lead to device failure by degrading electrical, chemical, mechanical or thermomechanical properties of one or more components of the device if it is not properly controlled. On the other hand, corrosion refers to the process of chemical or electromechanical degradation of materials. It occurs in three forms: uniform, galvanic and pitting corrosion. Uniform corrosion happens due to chemical or electrochemical reactions occurring at the metal-electrolyte interface uniformly all over the surface. Its continuation depends on the nature of the corrosion product. If the corrosion product is soluble in water, it can be washed off to expose new surface for further corrosion. Otherwise, if it is an insoluble non-porous adherent layer, it then limits the rate of reaction and stops the process. Galvanic corrosion occurs when two different metals in contact act as the cathode and anode where reduction and oxidation reactions respectively take



place. Pitting corrosion occurs at localised areas and results in pit formation where corrosive conditions inside the pit accelerate the corrosion process. A number of factors influence the corrosion phenomena such as the metal conductor involved, the operating conditions and the environment. In electronic packages, the potential for corrosion is common in all metallic sites. One of the common corrosion failure modes observed on printed circuit boards (PCB) is electrolytic migration, which is an electrochemical phenomenon involving metal dissolution at the anode and deposition at the cathode controlled by an electric potential and the chemistry of the solution layer over the components (Ambat et al., 2008).

Damage due to radiation exposure is another example of the wear-out failure mechanism in electronic devices used in aerospace environments such as satellites, high altitude aircraft, and also in terrestrial environments such as nuclear-power. Damage due to radiation can take two forms: mechanical failure and electrical damage. The mechanical failure mechanism is embrittlement, while the electrical phenomenon is more of an unpredictable overstress and soft errors due to passage of radiation particles. Radiation damage is responsible for various types of aging in materials. In metals and ceramics, radiation causes point defects, such as pairwise combinations of vacancies and interstitial atoms by knocking atoms out of their lattice structures. These point defects then cause embrittlement, and alter the thermal, optical and electrical properties of active devices and materials in electronic packaging applications (Dasgupta et al., 1991). In polymeric materials, irradiation is responsible for reduction in strength by breaking of the polymer chain, oxidation, gas formation, or changing the degree of polymerisation due to chain branching (Al-sheikhly et al., 1994).

### **3.4 Thyristor failures**

In relation to the research presented here, there are a number of failure mechanisms identified above that could potentially cause the failure of the NEWTON thyristor during its service life. These physical and chemical

processes will actually be driven by the different stresses the device will be exposed during its operation, and also defects that relate to its design features and fabrication process. For example, mechanical and structural defects in the NEWTON thyristor can occur from weak parts (e.g. the metal flanges or the housing), inappropriate mechanical design, and issues relating to the soldering or cold welding process of the flanges that join the copper pole pieces to the housing. These can contribute to ingress of harmful contaminants inside the package and lead to functional degradation of thyristor over time. Surface and bulk defects are also other types of flaws that can contribute to the failure of thyristor. Examples of surface defects include external contaminants that can collect in the housing or penetrating through it, while bulk defect examples include defects in the crystalline structure of the semiconductor or other metallic components, undesirable impurities and diffusion defects. Such flaws can either lead to a sudden failure of the semiconductor element, or also contribute to the gradual functional failure of the thyristor over its service life.

Examples of some major stresses the thyristor device will encounter during its lifetime include (1) mechanical, (2) voltage and current, (3) temperature stresses, and (4) moisture. During its normal service, the NEWTON thyristor device will experience static mechanical stresses when it is assembled together with heat sinks to form the clamped thyristor assembly, together with shock and vibration stresses during transportation. On the other hand, electrical and thermal stresses will be encountered during the AC/DC conversion process due to the resulting power dissipation; whilst humidity and moisture will be experienced if the environment in which the thyristor is stored, transported or operated is uncontrolled. Numerous studies have actually shown occurrence of such stresses is an important issue to the reliability performance of electronic devices, such as the high power thyristors.

In the past, different studies have discussed the damaging effect caused when electronic devices are exposed to an uncontrolled humidity (or moisture) environment. For example, Li et al., 2008 studied the moisture induced failure of a stacked die package tested according to J-STD-20 MSL standard, and

Fan et al., 2008 presented different methods to characterise the degradation of interfaces in electronic packages in the presence of moisture. Both these authors identified that the major failure mechanisms that arise when an electronic package is exposed to a humidity environment, are popcorn failure, corrosion and cracking. Popcorn failure occurs when the moisture absorbed in plastic packages vaporises at high temperatures creating an overpressure condition. Under severe conditions, the induced vapour pressure coupled with the thermal stress then result in creation of localised stress regions and crack formations that may propagate outwards. If the crack reaches the package exterior, the high pressure may be released producing an audible popping sound, characteristic of the popcorn failure mechanism (Galloway et al., 1997). Crack formation is another failure mechanism that results when a package is subjected to moisture induced stresses. Upon moisture absorption, polymer materials in packages swell, leading to dimensional changes. Interfacial adhesion can also be affected by moisture. With long periods exposure to humidity, aging effects can occur leading to delamination failure along weaker interfaces and eventually package failure. The third type of moisture assisted failure occurs when the presence of a crack provides a path for corrosive material to enter the package. This can lead to the uniform, galvanic or pitting corrosion highlighted earlier in section 3.3.

Together with the studies of humidity effects, different researchers have also investigated the effect of the thermal and electrical stresses on the reliability of electronic devices. For instance, Nied, 2003 identified interfacial fracture (or delamination) as a common cause of failure when an electronic device that is comprised of dissimilar materials having different thermal coefficient of expansion is subjected to temperature changes. On the other hand, Janssen et al., 1999 in his review of different types of composite insulating materials for high outdoor insulation technology stated that occurrence of an electrical overstress can cause electronic device failure through initiating partial discharges in its insulation material. Other studies, e.g. Barreau et al., 2008, have also identified mechanical stresses resulting from shock and drop can also cause electronic device failure when they are transported or mishandled. In plastic packages, mechanical shock has been reported to generate chipout

in the moulding compound, and in brittle components, e.g. silicon dies, it can cause failure through fracture.

To control and monitor the highlighted defects that can be responsible for the thyristor failure, various in-process tests can be performed on the device. Examples of such tests include measurement of forward voltage drop at high current density levels and thermal resistance measurement (Bajenescu et al., 1999). However, in order to mitigate the stress driven failure mechanisms highlighted above, a physics-of-failure approach was adopted in this project to develop a reliable thyristor. This is discussed next.

### **3.5 Reliability complexities**

As mentioned earlier, reliability is today a critical issue in any industrial and consumer product development because of determinant factors such as time-to-market and cost issues of a product which are decisive in the global market place. No matter how sophisticated a product is designed and manufactured, it becomes useless if it fails to deliver the designed performance during its expected lifetime.

From a reliability point of view, engineering products are classified in three classes. Class I devices are made as reliable as possible as their potential failure is viewed as catastrophic. Examples of such products include military aircraft, battleships, space devices among others, and are usually made for a single customer, e.g. the military or the space agencies. Devices intended for the industrial market where a low number of failures is required with relatively high production volumes for demanding applications are categorised in Class II, e.g. aircraft, automobile, ships, whereas products focussed towards the consumer market are categorised in Class III (Suhir, 2007).

Attaining an adequate, though less than perfect, level of reliability for these products demands an integrated and total engineering approach through a clear definition of different activities, e.g. material selection, design and

manufacturing processes, etc., and concurrent effort between design, manufacturing, management and marketing efforts. It starts from the early stages of design with the definition of the product requirements and life cycle environment; implemented in manufacturing related tasks, such as material and manufacturing characterisation, parts selection, process capability design, etc.; and evaluated using electrical, environmental and mechanical testing to identify potential failure sites and mechanisms. During production, manufactured products are then thoroughly checked, and if necessary they are maintained during subsequent field operation.

A reliable and cost-effective product can be designed through an effective physics-of-failure and root-cause analysis approach. Such tools exhibit an array of capabilities, such as reliability prediction under a range of environmental conditions, time-to-failure prediction for fundamental failure mechanisms, and analysis of the effects of different manufacturing processes on product reliability, using virtual qualification and accelerated testing tools. Design guidelines based on physics-of-failure models can also be used to develop tests, screens, and derating factors, and measure specific quantities for detection of unexpected flaws, manufacturing, and maintenance issues.

Manufacturing and assembly processes have a tendency to strongly influence the quality and reliability of devices through the introduction of defects, flaws and residual stresses that act as potential failure sites later in the product life. Auditing a manufacturing process can be done in two categories. First, qualification procedures are used to ensure the manufacturing specifications do not compromise the long-term reliability of the hardware. Secondly, batch screening and accelerated testing (described next) ensure that variability of the manufacturing processes is within specified tolerances.

#### **3.5.1.1 Accelerated testing**

Accelerated testing involves measuring the performance of the test examples of a product under loads more severe than would normally be encountered in

the field condition to enhance the damage accumulation rate within a reduced time period. The key criteria for the success of such a test relies on the assumption that the failure mechanism and modes in the accelerated environment will be the same as those observed under actual usage conditions without introducing non-representative failure mechanisms. Accelerated life testing is not a new concept because it has been widely used to investigate different system's reliability in the past. Example of a study where the accelerated life test concept has been successfully applied to study a hermetic device is Schnable et al., 1976, who investigated the reliability of hermetically sealed complementary MOS integrated circuits that are typically used for military and aerospace equipment. In this study, the failure mechanisms of these devices were investigated using accelerated life tests, and their reliability compared against existing CMOS components. On the other hand, examples of studies, where accelerated life tests have been successfully used to study non-hermetic devices, include Theis et al., 2000 and Schlegel et al., 2001 who analysed the integrity of non-hermetic laser and Insulated Gate Bipolar Transistor (IGBT) modules respectively. Theis et al., 2000 investigated novel non-hermetic diode devices using a series of 85 °C and 85% (commonly referred as 85/85) relative humidity accelerated life test, which were shown to be sufficiently reliable for future use in telecom applications. On the other hand, Schlegel et al., 2001 assessed the performance of a newly developed non-hermetic high power IGBT module up to industry standards after evaluating its resistance to humidity using the 85/85 temperature and humidity test, and also its life expectancy using the temperature cycling experiments.

Accelerated testing begins with the identification of any anticipated overstress and wear-out failure mechanisms. Once the failure mechanisms are identified, the normal steps are: to select the appropriate acceleration load; determine the test procedures and stress levels; determine the test method, such as stress acceleration or step-stress acceleration; perform the tests; and interpret the test data, which includes extrapolating the accelerated test results to normal operations (Suhir, 2007). The failure results should also provide information for improving the component through design or process changes.

Examples of some accelerated loads include (1) thermal loads, e.g. storage temperature, temperature cycling, (2) chemical loads, e.g. humidity, corrosives, (3) electrical loads, such as voltage, or power, (4) mechanical loads, like vibration, mechanical load cycles, (5) or a combination of the above. The main objective of an accelerated life test is to reveal the physics-of-failure of the device – to establish the modes and mechanisms of failure and to identify the parametric degradation of the materials and structures under test.

Highly accelerated life test (HALT) is another alternative to accelerated life tests (ALT), which aims to generate failures as fast as possible. However, the main difference between the two is that HALTs are carried out with a smaller number of samples to obtain data as soon as possible (typically less than two or three months) to provide preliminary information about reliability of the product and the principal physics of their failures. On the other hand, ALTs enable more realistic information about the product failure to be obtained. Unlike HALTs, ALTs are conducted with a larger number of samples and for considerably longer times. It is on the basis of such tests that reliability engineers accumulate failure statistics to establish the probability of failure under field conditions for a given operation time.

### **3.6 ‘Designing’ reliability into the NEWTON device**

Various documents have been produced in the past to streamline the process of understanding the reliability needs of both the suppliers and customers. For instance, the IEEE standard 1332 (IEEE-SA Standards Board, 1998) guides suppliers in planning a reliability program to suit their design philosophy, the resources at their disposal, and the product concept, and also provides guidelines for a contractual relationship between the customer and the supplier. The IEEE 1332 standard identifies three reliability objectives to ensure the customer requirement and product needs are met, namely (1) the supplier and customer should work together to identify the requirements and

product needs, (2) the supplier should develop and follow a series of engineering activities to meet the requirements and needs, and (3) the supplier should include activities that assure the customer that the requirements and product needs have been satisfied. The benefits of such a program depend on the accuracy and completeness of the information and methods used to conduct these predictions.

The methods used for reliability evaluation are often a matter of contention, and application of the three major types of tests (product verification, qualification and accelerated life tests (ALTs)) is highly dependent on the aims and objectives of the test program. For instance, the product verification test is used to obtain technical feedback about the viability of a design approach, qualification test to demonstrate a product is qualified to serve in the given category, and ALTs to understand the physics of failure of the product (Suhir, 2007).

The polymer-based high voltage thyristor housing developed in the NEWTON project can be classified as a Class II type product intended for large HVDC commercial scheme applications where a low failure rate is expected, i.e. out of the 5280 thyristors required in a  $\pm 800$  kV scheme, only 5 thyristor failures are allowed per year (Woodhouse, 2007b). However, the definition of their reliability requirements and test program by demanding government standards, such as MIL-STD-750C: 'Test methods for standard semiconductor devices', is economically unviable due to the stringent and expensive reliability test programs required by such standards. Also, due to the novelty of the packaging technology and application environment the product will be used in, choosing product verification tests is inappropriate because the test plans are inefficient and may not 'torture' the part sufficiently for an effective reliability prediction. Instead the usage of accelerated life tests has been proposed to investigate the housing reliability and reveal potential failure modes and mechanisms as in the actual field condition. Attempts to investigate the reliability of thyristor devices using such an accelerated life test concept have been made in the past. Sampei et al., 1997 used temperature and voltage acceleration tests to study the changes in the characteristics of



power thyristors that were implemented in different phases in Hokkaido-Honshu HVDC link. From the results of the investigation, the thyristors that were in operation for several years in the converter station were found to still have characteristics and service life equivalent to new ones. On the other hand, Tanaka et al., 1999 also studied the long-term performance of 8 kV, 3500 A light triggered thyristors developed for a 500 kV, 2800 MW HVDC system using accelerated life tests at  $\pm 625$  kV DC. The insulation capabilities of the tested thyristors were concluded to be satisfactory for their intended long period. However, these studies determined the reliability and life expectancy of thyristor housings by focussing on their current and voltage characteristics, rather than their physics-of-failure.

Ceramic materials used to build hermetic housings have traditionally demonstrated good reliability, and have been widely used in electrical insulation applications because of their excellent properties. For instance, they tend to be chemically stable and they are generally neither degraded by nor permeable to environmental stresses, e.g. humidity. Because ceramics are rigid, they also impart significant mechanical strength to any component they are used in. However, some disadvantages ceramic materials introduce are: (1) they can experience brittle fracture and mechanical damage in service, during handling and transportation; (2) because they are generally heavy materials, the handling, transportation and installation of ceramics-based components tends to be expensive and time-consuming; (3) due to their high surface free energy, the surfaces of ceramic components tend to easily wet, which can then lead to flashover in contaminated locations. A shift to a polymer-based thyristor housing will help eliminate the cost, weight and flashover limitations inherent to ceramic packages. However, coupled with the failure mechanisms that can occur due to defects and stresses as highlighted earlier, additional limitations a polymer material housing brings to the NEWTON thyristor are: (1) their mechanical strengths are lower than ceramic materials; (2) they can age and deteriorate under environmental stresses (e.g. moisture, operation temperature) it encounters in service (Mackevich et al., 1997).

As elaborated in section 3.4, the stresses the thyristor will encounter during its operation lifetime are: current, voltage, temperature, mechanical stresses, and moisture. If these stresses exceed the tolerance level of the packages, they are likely to result in damage to the thyristor by short-circuit and explosion failure modes. To avoid such failure, a careful electrical, mechanical and thermal design of the different components of the thyristor is required. Electrical overstress can lead to dielectric breakdown of the polymeric housing. The stability of the thermal characteristics of the thyristor components is important because any deterioration of the thermal pathway can lead to a localised temperature increase and finally its destruction. Because the device will be exposed to a range of temperature loadings during service, thermal fatigue might also occur. Careful selection of the interfacing material would thus be required to ensure compatibility of the thermal coefficient and reduce the thermal stress to mitigate the likelihood of delamination (or interface fracture) between the different materials. On the other hand, to improve the mechanical design of the thyristor, rigid parts with reduced mass and small inertial moments would be required and mechanical resonances from vibrations (e.g. due to transportation) would have to be eliminated to prevent potential failure due to fracture for example.

To overcome the disadvantages of a switch to a polymer-based housing and reduce the likelihood of short-circuit and explosion failure modes occurring, various accelerated life tests were conducted as part of an extensive reliability test programme to study the physics-of-failure of the polymeric package which could be used to take corrective design measures. Examples of some acceleration parameters used for these tests included high/low temperature, high humidity, temperature cycling, power cycling, etc. These are described in Chapter 4.

## 4 Research Methodology

### 4.1 Introduction

This chapter discusses the research approach used to determine whether a switch from the current ceramic housing to a polymer-based material for high voltage thyristors is appropriate.

As described earlier, the hockey-puck thyristor that is commonly used in HVDC transmission schemes is comprised of a silicon wafer sandwiched between molybdenum discs and copper pole pieces that act as heat transfer mediums to carry heat away from the device and as anode and cathode terminals for electrical connection (Figure 1.6). The device also includes a gate terminal that connects to the gate electrode of the silicon wafer and enables triggering of the thyristor. The whole assembly is enclosed in a hermetically sealed ceramic enclosure to prevent environmental attack and provide mechanical robustness. Since their introduction, such housings have demonstrated excellent reliability and performance because of their hermeticity, and excellent electrical resistant properties to tracking and breakdown. However, because future long distance HVDC transmission will be implemented at higher ratings where larger diameter thyristors are required to avoid increasing their number, the main disadvantages of the current hockey-puck configuration, which are its processing cost and weight, need to be considered. To overcome these issues, replacing the current ceramic housing with a polymeric material was investigated in this project. Although such a change provides several advantages in terms of low cost and light weight, some of the challenges involved when using a polymeric housing are: (1) they are permeable to moisture and can lead to the functional degradation of the thyristor over time, (2) the manufacturing routes can be complex, (3) they have properties that vary with temperature, (4) because the material properties of ceramic and polymers are different, the electrical, thermal and

mechanical performance of the polymer package will also be different from the current ceramic housing of the thyristor. In this project, these challenges are addressed by developing and testing a polymeric housing for the thyristor device that will ideally provide reliability and performance comparable, if not better than current ceramic packages.

## **4.2 Housing prototype design selection**

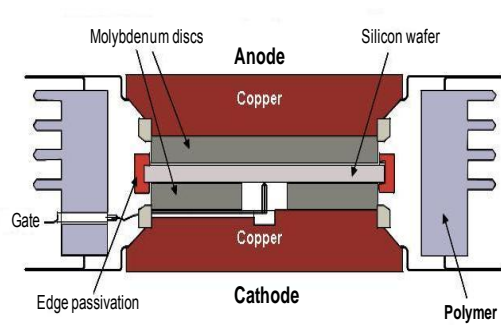
In the NEWTON project, the different research activities were based on a 50 mm diameter prototype. The benefit this size provided was that it would allow benchmarking the performance of a polymer-based housing against a similar size ceramic housing currently available commercially using readily available silicon wafers. Once sufficient confidence will be gained from the various studies, the development of a 125 mm and 150 mm polymer housing will then be initiated using the experience gained from the 50 mm housing. For the NEWTON project, the technical specifications these larger thyristor devices were required to meet are as follows (Woodhouse, 2007a):

- Operating lifetime : > 40 years
- Number of permissible failures per year : 5 out of the 5280 thyristors intended for exploitation in the project (equivalent to 100 Failure In Time (FIT))
- Voltage rating of thyristor : 8.5 - 10 kV
- Power transmission schemes the device is intended for exploitation within : 4000 A at  $\pm 800$  kV
- Valve hall environment in which the thyristors will be located during service:

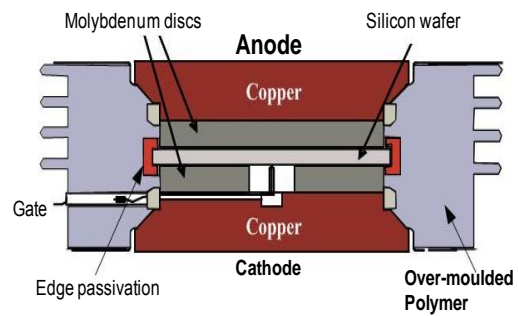
Altitude:	< 2000 m
Temperature:	10 °C – 60 °C
Humidity:	40% - 80%

- **Recyclability:** The constituent materials of the device will need to be recoverable for recycling in a cost effective and environmentally friendly manner.

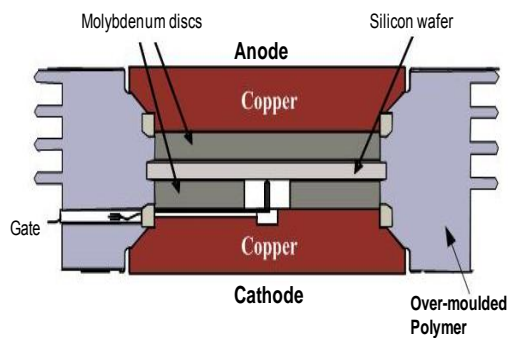
Following detailed studies by Ahmad, 2009, the 50 mm prototype was based on a 'replacement' design configuration after comparison with other housing design concepts, such as 'overmoulded non-integrated' and 'overmoulded integrated' configurations. An illustration of the 'replacement', 'overmoulded non-integrated' and 'overmoulded integrated' design concepts is shown in Figure 4.1. As shown in Figure 4.1(a), in a 'replacement' concept the ceramic housing of the thyristor is directly substituted with a polymer material. In an 'overmoulded non-integrated' configuration (Figure 4.1(b)), no housing cavity exists between the polymer material and the stacked assembly of copper pole pieces, molybdenum discs and silicon wafer (with rubber edge passivation around) – the stacked assembly is here in direct contact with the polymer moulded around it. Compared to the 'overmoulded non-integrated' configuration, no rubber edge passivation exists around the silicon wafer circumference, and the polymer material is moulded directly around the stacked assembly of the device in an 'overmoulded integrated' design (Figure 4.1(c)). To identify the appropriate design concept for the 50 mm prototype, Ahmad, 2009 ranked each housing configuration against various criteria, such as ease of final assembly, thermal/electrical benefits, installation, etc., and found the 'replacement' design technology to be the most appropriate for the polymer thyristor housings. On the other hand, Ahmad, 2009 also concluded that the most appropriate polymers for the thyristor housing are polyimide (PI), liquid crystal polymer (LCP), polyetherimides (PEI), polyphenylene sulfide (PPS), epoxy, polyetheretherketone (PEEK), and polybutylene terephthalate (PBT).



**(a) Replacement design**



**(b) Overmoulded non-integrated design**

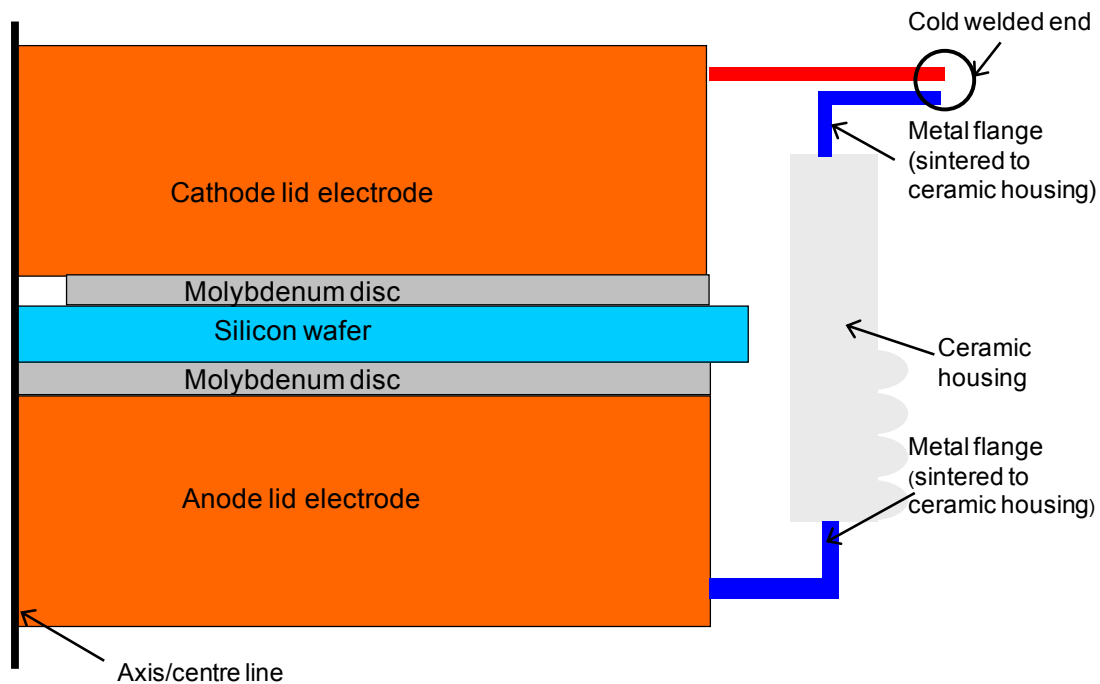


**(c) Overmoulded integrated design**

**Figure 4.1: Overview of different housing design options**

### 4.3 Design considerations

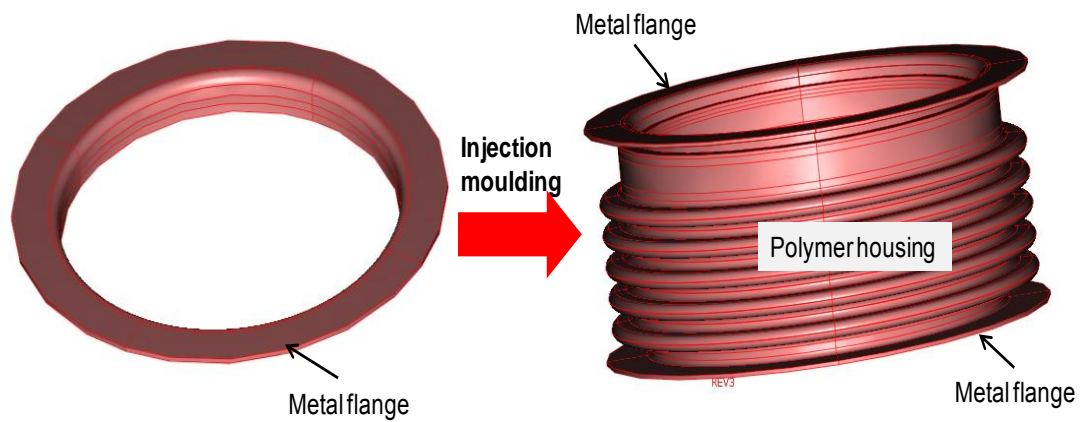
A commercial hockey-puck ceramic thyristor package is typically based on a 2-part design comprising of a separate cathode pole piece and a ceramic housing which is joined to the anode pole piece, as shown in Figure 4.2. The assembled package is then sealed by welding the cathode flange of the ceramic housing to the separate cathode pole piece.



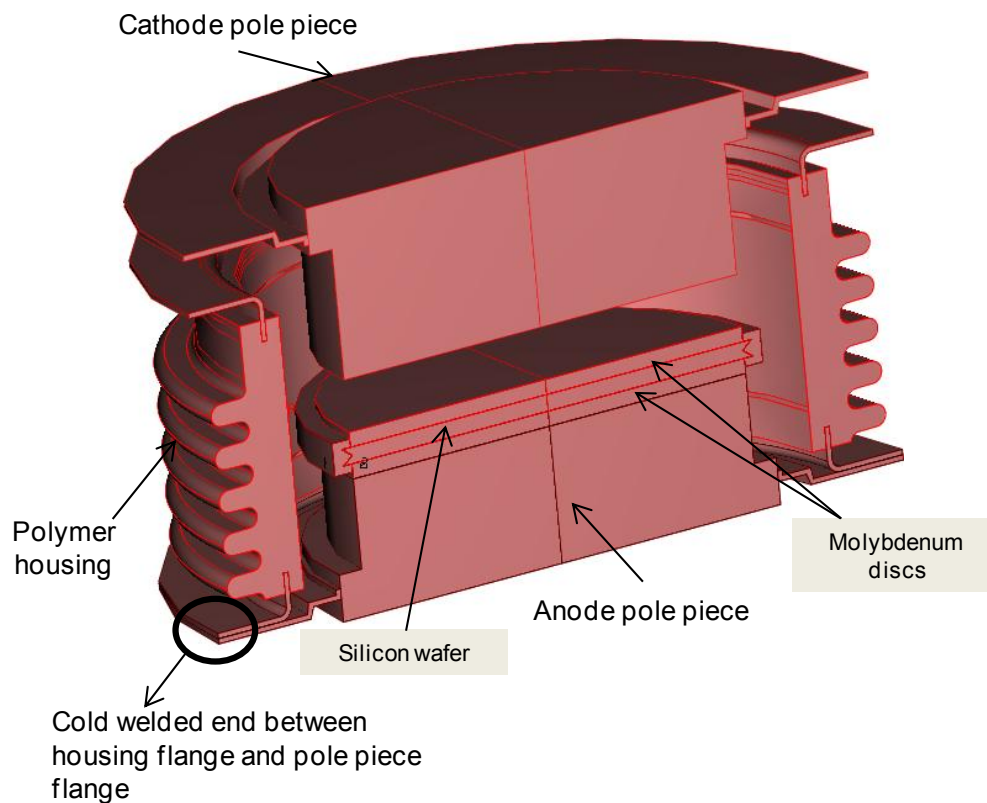
**Figure 4.2: Common configuration of a ceramic-based thyristor (Courtesy - Dynex Semiconductors Ltd)**

Unlike such commercial ceramic package, the 50 mm prototype developed in the project was based on a 3-part design, namely the housing comprised of metal flanges overmoulded into polymer at both the cathode and anode ends, with separate cathode and anode pole pieces which are both welded to the housing flanges to form the assembled thyristor device. A typical metal flange that is used in the polymer housing is shown in Figure 4.3. To manufacture the polymer housing, two such flanges are normally used. During the injection moulding process, the flanges are placed inside the mould tool, and are then overmoulded with the polymer material to manufacture the polymer housing. The moulded housing is then assembled in a 2-stage process. First, one flange at the end of the housing is cold-welded with a pole piece (either anode or cathode), and then the stack of the molybdenum discs and silicon wafer are placed into it, as shown in Figure 4.4. It is then welded with the second pole piece to form the assembled thyristor device (Figure 4.5). The reason this approach was taken was because (1) this design configuration was more feasible to weld using the in-house welding tool at Dynex Semiconductor, and (2) developing the mould tool to manufacture the polymer housing that was

only comprised of the metal flanges (no pole pieces inserted in the mould tool) was found to be less complex.

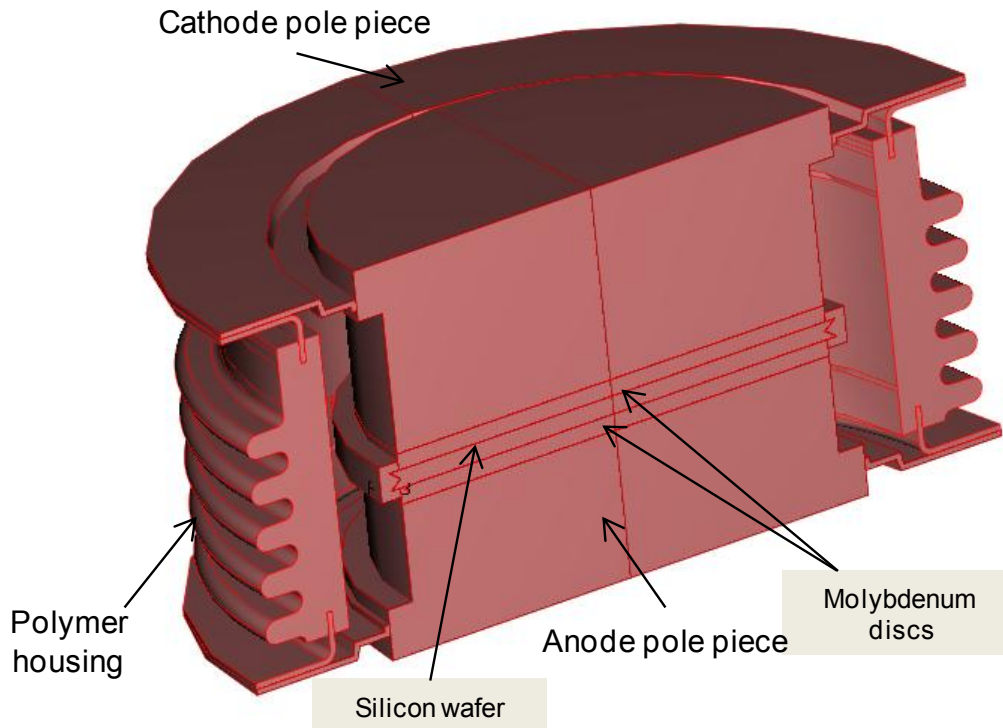


**Figure 4.3: Drawing illustrating the metal flange used to manufacture the polymer housing**



**Figure 4.4: Diagram illustrating a half section of the polymer housing that has been cold-welded at its anode and stacked with molybdenum discs and silicon wafer, before it is cold-welded again with the cathode pole piece**





**Figure 4.5: Drawing illustrating the half section of an assembled thyristor device cold-welded at both ends**

To develop the 50 mm prototype based on the ‘replacement’ configuration, different studies were required to ensure the housing had the appropriate performance and properties. For instance, having appropriate electrical properties would prevent housing failure due to dielectric breakdown and partial discharge mechanisms; whilst good mechanical properties would help prevent mechanical failure of the housing due to explosion, and when it is clamped to other thyristors and heat sinks. On the other hand, degradation of the polymer due to excessive temperature changes, and delamination at interface regions caused by components having different coefficients of thermal expansion could also be avoided if the housing material has good thermal properties. Several investigations were thus needed within the NEWTON project to allow for the design modifications being made. An overview of these is described next.

- **Housing material selection and moulding parameters identification:**

Selecting the appropriate polymer for the housing was important for electrical and moulding performance. For example, should an

inappropriate plastic be selected, partial discharge and dielectric breakdown due to high electrical stresses could result. In case the polymer is also not resistant to moisture and contains harmful contaminants within it, undesired corrosion and interfacial delamination would occur. On the other hand, using an inappropriate moulding parameters can result in moulding defects, such as void occurrence and shrinkage, which also lead to partial discharge failure.

- **Understanding the electrical and thermo-mechanical behaviour of the polymeric housing:**

This study was necessary so that the housing could be developed in terms of electrical and thermo-mechanical performance. To reduce the likelihood of dielectric breakdown and partial discharge failures, identifying the magnitude of the electric field strength and the maximum electric field region were required. On the other hand, the thermo-mechanical behaviour study aimed to study the internal stress distribution and identify potential delamination sites in the housing when exposed to a range of temperatures.

- **Housing flange study:**

Having an appropriate design of the flange was also another critical area of investigation because it could influence the injection moulding process of the housing. For instance, if the flange has either a complex design or inappropriate geometry, inappropriate polymer flow around the contact region of the insert and housing can result in partial discharge failure of the package through formation of defects such as void, warpage.

Together with this, the flange design was also critical so that the housing had the appropriate mechanical and electrical performance. If the flange also has any sharp corners, or voids are present around the contact region between the flange and polymer housing, partial discharge failure of the housing can result when exposed to electrical stresses. On the other hand, when the polymer thyristor is clamped to heat sinks and

other thyristor devices, an appropriate flange design and dimension will help impart appropriate mechanical properties and prevent excessive deformations that will lead to failures, such as plasticity or delamination at the flange and housing interfaces.

- **Design parameters study:**

Together with the housing flange design, materials selection and moulding parameter investigations, identifying the correct dimensions of the different design parameters of the housing was also necessary to improve the housing performance and ensure manufacturability. For instance, determining the appropriate dimensional tolerances of critical dimensions, such as the depth the flange protrudes inside the housing, the thickness of the housing, etc., can help mitigate the risk of dielectric breakdown due to high electric fields, together with void and shrinkage defects during moulding. On the other hand, filling the housing cavity (formed by thyristor and stacked assembly of silicon wafer, molybdenum discs and copper pole pieces) with the appropriate content, and determining the correct polymer housing shape by varying the convolute design are also other important design parameters to study so that the housing does not fail due to breakdown and tracking along the housing exterior respectively.

- **Protection of silicon wafer edge:**

As the polymer material of the prototype housing is non-hermetic and moisture can diffuse through during its service life, corrosion of the thyristor can occur if it is not protected by an appropriate protection barrier. Currently silicone rubber passivation is used around the circumference of silicon wafers used in ceramic hockey-puck housing to prevent its corrosion due to moisture ingress. For wafers that will be used in the NEWTON polymer housing, the development of novel protective barrier will be required, as the polymer material of the housing will not be fully hermetic, i.e. it is likely to be permeable to moisture.

- **Gate design:**

As highlighted in Chapter 3, an appropriate design of the gate lead and its alignment with the gate electrode of the silicon wafer are also important to ensure the thyristor functions normally. In case the gate lead design is unsuitable and does not contact and align with the wafer gate electrode, the thyristor would then not trigger during service. On the other hand, in the event of a poor adhesion between the polymer material of the package and the gate lead that passes through it, ingress of moisture and ionic contaminants through the package can lead to corrosion of the silicon wafer, thereby causing failure of the housing.

- **Reliability and hermeticity assessment:**

The reliability assessment of the prototype housing using a series of experiments was also regarded to be important to assess whether a switch from the current ceramic housing to the polymeric option was appropriate. Also, because the polymer housing is non-hermetic and will allow diffusion of moisture over time, assessment of the device moisture permeability was considered critical. Through the study of these areas, identifying the physics-of-failure of the polymer housing would be possible, and would benefit the future development of larger size housings.

#### **4.4 50 mm prototype development**

Following initial work by Ahmad, 2009 to identify appropriate polymers for the prototype housing and after different technical and economic feedbacks, a high performance glass-reinforced polyimide polymer grade was selected for the prototype. Different development activities of the 50 mm prototype in the NEWTON project were then accomplished within a parallel collaboration with DuPont™, a leading polymer manufacturing company, who also supplied the selected polyimide grade.

The different research activities were initiated following the generation of a preliminary prototype design by Dynex Semiconductors. Loughborough University and DuPont™ then performed different development studies to assess and improve the prototype design and performance. For instance, identification of the appropriate moulding parameters for the glass-filled polyimide housing was studied by DuPont™. For this study, based on their previous moulding experience and knowledge, Moldflow simulation software was used to simulate the moulding process of the housing, as detailed publications focussed on the processing of the selected glass-filled polyimide polymer grade were not available on the public domain. This study also aimed to identify the likely locations of any moulding defects and improve the housing design.

Together with these, electrical and thermo-mechanical studies were also undertaken by Loughborough University to develop the housing. It is these studies that are discussed in this thesis.

An overview of the Finite element analysis (FEA) method used to perform the electrical and thermo-mechanical simulations is presented in Chapter 5. The electrical behaviour of the polymer housing was modelled, when AC and DC voltages were applied. The AC voltage study aimed to identify the occurrence of any dielectric losses that could lead to temperature rise within the package and thereby its potential degradation. The DC study aimed at investigating whether the electric field due to the applied voltage would be likely to result in housing failure as a result of dielectric breakdown. It also aimed at identifying any localised electric field concentrations which might present a risk of partial discharge failure if coincident with voids. These results are presented in Chapter 6.

To further improve the electrical performance of the housing, other simulation studies were also carried out (described in Chapters 7 and 8). Different flange end shape designs were studied to improve the electrical performance of the housing and the influence of critical geometrical parameters, such as the flange depth, wall thickness, etc., on the electrical performance of the housing

were also assessed. The electrical simulation results from these studies were compared with the moulding modelling work from DuPont™ to finalise the prototype design before its manufacture.

Following their development and manufacture, the prototypes were exposed to a series of accelerated life tests as a technique to study their reliability and reveal their physics-of-failure to assist the future development of larger size housings, e.g. 125 mm and 150 mm diameters. Only the moulded housings were available for exposure to the different aging conditions and therefore it was not possible to test the moisture permeability of the prototype at this stage. Further investigation, including moisture diffusion measurements, will be appropriate in the future when the moulded housing is assembled with the silicon wafer present within. An assembled housing will also allow the study of novel passivation technologies around the silicon wafer to prevent any undesired moisture ingress. As highlighted in Chapter 3, because the thyristor will be subjected to electrical, mechanical, environmental and temperature stresses during its lifetime, a series of accelerated life tests (ALTs) were required to be performed, including temperature cycling and temperature-humidity ALTs. In this thesis, the results of the different ALT experiments are not completely discussed because of commercial confidentiality requirements in the project. However, results from the temperature cycling test between -40 °C and 125 °C are presented in Chapter 9. This study is also complemented with a thermo-mechanical simulation study performed on the housing between the same temperature range to study the internal stress distribution and identify any potential delamination regions.

The extension of the models used for the 50 mm housing to the development of a larger size 125 mm thyristor housing using the Taguchi method of experimental design (TMED) was also carried out and is described in Chapter 10 of the thesis. For this work, the influence of different design parameters, e.g. the convolute shape, the flange depth, wall thickness of the housing, copper pole piece thicknesses and diameters, etc., on the electrical field strength within the housing was studied, so that a 125 mm thyristor having an optimum combination of the different parameters could be developed in the

future. Based on the outcomes of the research, a number of design recommendations for larger size thyristor housings were identified and these are outlined with other conclusions and further work in Chapter 11.

## **5 An overview of the Finite Element Analysis method**

### **5.1 Introduction**

This chapter discusses the main research method of Finite Element Analysis (FEA) used in design studies for the polymeric housing in high voltage operation. The preliminary part of the chapter provides an overview of the finite element analysis technique and the principals the selected finite element solver uses to perform the selected simulation studies. The latter part highlights the strategy used to validate the methods the selected FEA solver uses.

### **5.2 Finite Element Analysis**

In many branches of engineering and the physical sciences, complex systems tend to be analysed by studying the variation of different variables characterising the system as a function of time, space, or with respect to other variables of the system. Although classical analytical methods or mathematical statements of the governing laws in the form of differential equations can be used to analyse simple problems, obtaining an exact solution tends to be difficult and often requires the use of a high level of approximation when applied to real-life problems, due to their typically complex geometry and boundary conditions. To overcome this limitation, computational methods such as the use of boundary elements, finite differences, finite volumes and finite elements, etc. are often used (Seshu, 2003, Doshi, 1998).

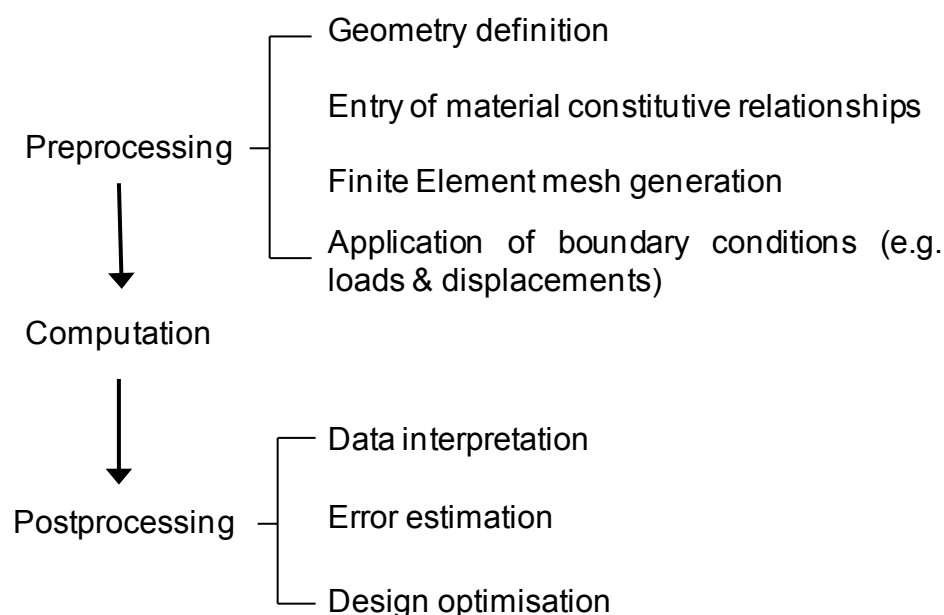
The term 'finite element method' was first coined by Clough, 1960 in a paper on plane elasticity problems. However, the idea behind the finite element analysis technique can be traced back much further to 1943 from the works of



Richard Courant where he studied the St. Venant torsion problem using an assembly of triangular elements and the principle of minimum potential energy (Huebner et al., 2001). From its original application to stress studies of complex airframes in the late 1950s, the finite element method has since received widespread interest and acceptance in engineering with innumerable papers, conferences and books having appeared on the subject. In fact, a recent web search on the phrase “finite element” on the Google search engine yielded over 6 million pages of results. It is today also an integral part of Computer Aided Engineering (CAE) and is extensively used in the analysis and design of many complex real-life systems in various technical areas, such as mechanical, civil, aerospace, heat transfer, biomechanics, geomechanics, acoustics, etc.

The basic essence of the method is that a continuum volume, whether solid or fluid, is considered to be built up of numerous tiny connected parts each having a simple geometry and called an element. These elements can be arranged in virtually any fashion to model complex shapes and algebraic equations for the behaviour of the individual elements are then used to model the required problem. The availability of high end computing tools has allowed FEA to become a commonplace tool in research and development. It is also used in combination with other computer-aided design (CAD) software to create and validate virtual prototype of new product designs before physical prototypes are developed in the product development process. FEA is nowadays the basis of a multibillion dollar per year industry (Roylance, 2001) and has proved to be cheaper compared to the conventional development approach involving iterative physical prototype development and testing. For instance using a computational simulation approach to the design of the bottom dome of an aluminium can would cost about \$2000 and less than 2 weeks to complete, compared to a typical development approach which would cost around \$100,000 and 6 months to a year to complete (Dieter, 2000). Although FEA offers several benefits to the study of complex engineering problems, it can nevertheless lead to wrong answers if common sense and sound engineering judgment are not used in its application.

The introduction of the first commercial finite element software was by Control Data Corporation in 1964. Engineers are now also able to choose from a wide range of FEA packages, and run them in a cost effective manner with the availability of powerful PCs today. Some popular packages used today include Abaqus from Simulia (a Dassault Systèmes brand), Ansys from Ansys Inc., Comsol Multiphysics from the Comsol Group, MSC/Nastran from MSC Software Group, etc. As highlighted earlier, since its early application during the 1950s to solve structural problems in the aerospace and civil engineering areas, FEA has today grown and is widely used for the numerical modelling of physical systems in a wide variety of engineering fields, e.g. electromagnetism, fluid dynamics, heat transfer, vibration, etc. The basic steps involved in FEA computation are quite generic and are common to different problem – be it from structural mechanics or heat transfer, or fluid flow. In fact, the common FEA steps that are involved in solving a typical structural problems are as depicted in Figure 5.1.



**Figure 5.1: Steps involved in solving FEA problems (Dieter, 2000)**

It consists of three distinct steps, namely the preprocessing, computation and postprocessing stages. The preprocessing stage starts with the setting up of the geometry by either importing it from a separate CAD software, or creating

it using drafting tools in the package. Material properties, such as elasticity and plasticity, of different domains of the geometry are then defined before it is meshed by dividing it into elements. Selecting the appropriate element type to use and building the mesh are also key to achieving a solution with the required accuracy and efficiency. The last step involved in the preprocessing stage is the definition of the boundary conditions and loads relative to the geometry before it is submitted to the FE solver for computation.

During computation, the FE solver generates a stiffness matrix for each element, calculates the displacements due to the applied loads, and then assembles each element's contribution to form a response matrix for the whole model. Once an equilibrium condition has been achieved, the results can then be imported into a post-processor for interpretation of the field values from the FEA solution in the final stage. Typically the output data can be plotted as deformed shapes, as animation to bring the model to life, or as a colour contour representing the stress and strain levels in any of the x, y or z directions on the model. Depending on the analysis, information, such as strain energy, plastic strain, creep strain can also be obtained.

### **5.3 Research Methodology**

To minimise the risk of package failure due to the expected electrical stresses (outlined in Chapter 3) during field operation, FEA using Comsol Multiphysics (formerly known as FEMLAB) has been used to study the housing performance and design. Initially developed by graduate students of Germund Dahlquist (a Swedish mathematician) in 1986, Comsol Multiphysics is now a full-featured commercial finite element analysis and solver software package suitable for various physics and engineering applications, and is particularly suited to multiphysics studies, i.e. where more than 1 physics are coupled and simultaneously solved. It comprises of different application modes that consist of predefined templates and user interfaces with equations and variables for specific areas of physics, and different application add-on modules used for specialised studies for the specific areas, e.g. the AC/DC module is used to

simulate electrical components and devices that depend on electrostatics, magnetostatics and electromagnetic quasi-static fields, the Acoustics module to model acoustic propagation in solids and stationary fluids, and the Heat Transfer module to analyse heat transfer by conduction, convection and radiation (COMSOL AB, 2010).

As part of the computer modelling carried out in this project, electrical and thermo-mechanical simulations were performed to study the package behaviour and identify the factors affecting the risk of electrical and thermal stress failures. For the electrical modelling work, the device was simulated under both direct current (DC) and alternating current (AC) conditions. The DC simulations aimed to study the electrical field distribution in the package under a static voltage and identify localised electrical stress regions to improve the housing design, whilst the AC mode studies sought to investigate the influence of alternating fields on electrical losses and therefore heating and resulting temperature changes within the housing. On the other hand, the thermo-mechanical simulations aimed to identify high thermal stress regions within the package that might occur due to the various thyristor components having different thermal coefficients of expansion. An overview of the fundamental theories that Comsol Multiphysics uses for electrical and thermo-mechanical simulations is discussed next.

### **5.3.1 Comsol Multiphysics Background**

Electromagnetic field simulations are usually done using one of four application modes in Comsol, namely *Electrostatics*, *Conductive Media DC*, *Magnetostatics* and *AC Power Electromagnetics*, and also using the additional *AC/DC* add-on module for specialised and complex electromagnetic problems. The Electromagnetics-based application modes are tailored for both static and time-varying electromagnetic-based simulations, with the *Conductive Media DC* application mode being more appropriate for DC simulation studies.

Maxwell's equations (Equations 5.1 – 5.4) together with the equation of continuity expressing charge conservation (Equation 5.5) are used to solve electromagnetic problems in Comsol (COMSOL AB., 2007a):

$$\nabla \times H = J + \frac{\partial D}{\partial t} \quad \text{Equation 5.1}$$

$$\nabla \times E = -\frac{\partial B}{\partial t} \quad \text{Equation 5.2}$$

$$\nabla \cdot D = \rho \quad \text{Equation 5.3}$$

$$\nabla \cdot B = 0 \quad \text{Equation 5.4}$$

$$\nabla \cdot J = -\frac{\partial \rho}{\partial t} \quad \text{Equation 5.5}$$

where  $\nabla$  is the curl of a vector field,  $H$  is the magnetic flux intensity,  $J$  is the current density,  $D$  refers to the electric flux density,  $E$  the electric field intensity,  $B$  the magnetic flux density, and  $\rho$  the electric charge density. The first two equations (Equations 5.1 and 5.2) are known as Maxwell-Ampere's law and Faraday's law respectively, and imply that magnetic fields can be generated by electrical current and changing electric fields, and a changing magnetic field can induce an electric field. Gauss' law in electric and magnetic form are described in equations 5.3 and 5.4 respectively and describe how an electric field is generated by electric charges, while the magnetic field is generated by a dipole configuration. The constitutive relationships relating the different physical properties of the mediums under study are related according to equations 5.6 – 5.8 (COMSOL AB., 2007a):

$$D = \varepsilon_0 E + P \quad \text{Equation 5.6}$$

$$B = \mu_0 (H + M) \quad \text{Equation 5.7}$$

$$J = \sigma E \quad \text{Equation 5.8}$$

where  $\varepsilon_0$  is the permittivity of a vacuum,  $P$  is the electric polarisation vector describing how a material is polarised under the influence of an electric field

$E$ ,  $\mu_0$  is the permeability of a vacuum,  $M$  is the magnetisation vector which describes how a material is magnetised when within a magnetic field  $H$ , and  $\sigma$  is the electrical conductivity.

To investigate the influence of AC voltages on the polymeric housing, a sequential electrical-thermal finite element simulation approach was used to study the temperature rise within the polymer housing as a result of electrical losses at a range of frequencies. For this study, the *Meridional Induction Currents, Magnetic Field* application mode in the AC/DC module and the *Heat Transfer by Conduction* application environment was utilised. The *Meridional Induction Currents, Magnetic Field* application mode is based on Maxwell's equations for electromagnetism explained previously, whilst the *Heat Transfer by Conduction* application mode is modelled using the heat diffusion equation 5.9 (COMSOL AB., 2007b):

$$\rho C \frac{\partial T}{\partial t} - \nabla \cdot (k \nabla T) = Q \quad \text{Equation 5.9}$$

where  $\rho$  is the density,  $C$  is the heat capacity,  $T$  is the temperature,  $k$  the thermal conductivity and  $Q$  is the heat source or heat sink.

For the thermomechanical modelling studies, the *Stress-Strain* application mode in the Structural Mechanics module was used to study the thermal stress due to temperature changes in the housing. For the analysis of such physics, the fundamental stress-strain relationship for solving linear conditions problems is given by equation 5.10 (COMSOL AB., 2007b):

$$\sigma = D \varepsilon_{el} + \sigma_0 = D(\varepsilon - \varepsilon_{th} - \varepsilon_0) + \sigma_0 \quad \text{Equation 5.10}$$

where  $\sigma$  is the stress,  $D$  is an elasticity matrix,  $\sigma_0$  is the initial stress,  $\varepsilon_{el}$  and  $\varepsilon_0$  are the elastic and initial strains respectively, and  $\varepsilon_{th}$  is the thermal strain, which is computed using equation 5.11:

$$\varepsilon_{th} = \alpha(T - T_{ref})$$

Equation 5.11

where  $T$  is the present temperature,  $T_{ref}$  is the stress-free reference temperature, and  $\alpha$  represents the thermal expansion.

## 5.4 Validation of Finite Element Methodology

The assessment of the capabilities and accuracy of different commercial finite element systems available today are an important stage of the finite element analysis process (Wood, 1994). To aid such activities, the National Agency for Finite Element Methods and Standards (NAFEMS) in the UK has in the past published reports describing various benchmark simulations covering different engineering analysis areas, such as Dynamics & Vibration, Fracture Mechanics, Linear Analysis, etc., which can be used to validate finite element tools.

For the studies described in the coming chapters, the Comsol FEA tool has not been validated in this way since it is a widely used commercial package for the study of various physics in different engineering applications in industry and academia. Instead simple problems that can be solved using exact analytical solutions have been used to verify whether the use of the *Electromagnetics* and *Stress-Strain* application modes were appropriate for the intended electromagnetics and thermo-mechanical simulation studies respectively. The analyses performed for these studies are next described in sections 5.4.1, 5.4.2 and 5.4.3.

### 5.4.1 DC Simulation

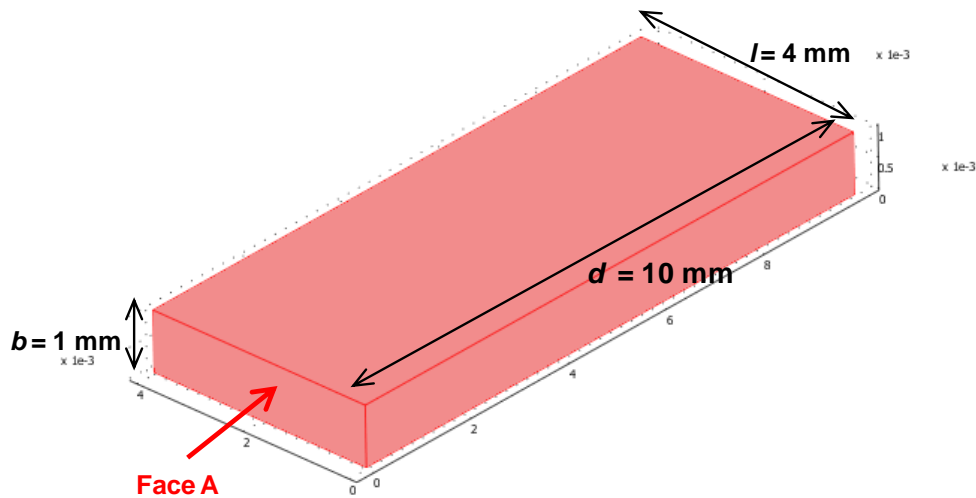
To confirm that the *Conductive Media DC* application mode was appropriate for the DC simulations in Comsol, a conductive rectangular block (Figure 5.2 (a)) having dimensions length,  $l$ , 4 mm, breadth,  $b$ , 1 mm and depth,  $d$ , 10

mm, and electrical conductivity of  $5.92 \times 10^7$  S/m was chosen for study. The block was subjected to a 20 V DC voltage, and its resulting electrical field was compared used with an analytical solution. In this case, because the electric field strength would be constant along the depth,  $d$ , of the block, a 2D planar model (Figure 5.2 (b)) of face A was used. As shown in the figure, a 20 V DC was applied across the boundary AB and 0 V across CD, while edges BC and AD were defined as insulator boundaries to compute the electrical field magnitude. Its solution was then compared against the analytical solution of the electrical field,  $E$ , calculated using equation 5.12 (McComb et al., 2005):

$$E = V/b$$

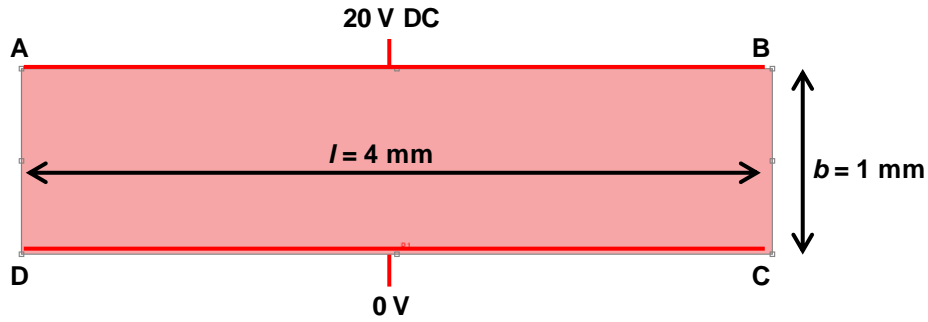
**Equation 5.12**

where  $b$  is the width of the rectangular model (1 mm in this case) and  $V$  is the applied DC voltage (20 V).



**(a): 3D geometry of rectangular block**





(b): 2D rectangular planar model

Figure 5.2: Illustration of 2D and 3D models of rectangular block used for DC studies

The computed electric field is shown in Figure 5.3, and can be observed to have a constant magnitude of 20 kV/m throughout. Because the electrical field calculated from the equation 5.12 also resulted in an electrical field magnitude of 20 kV/m, the *Conductive Media DC* application mode was concluded to be a valid tool for the DC modelling studies.

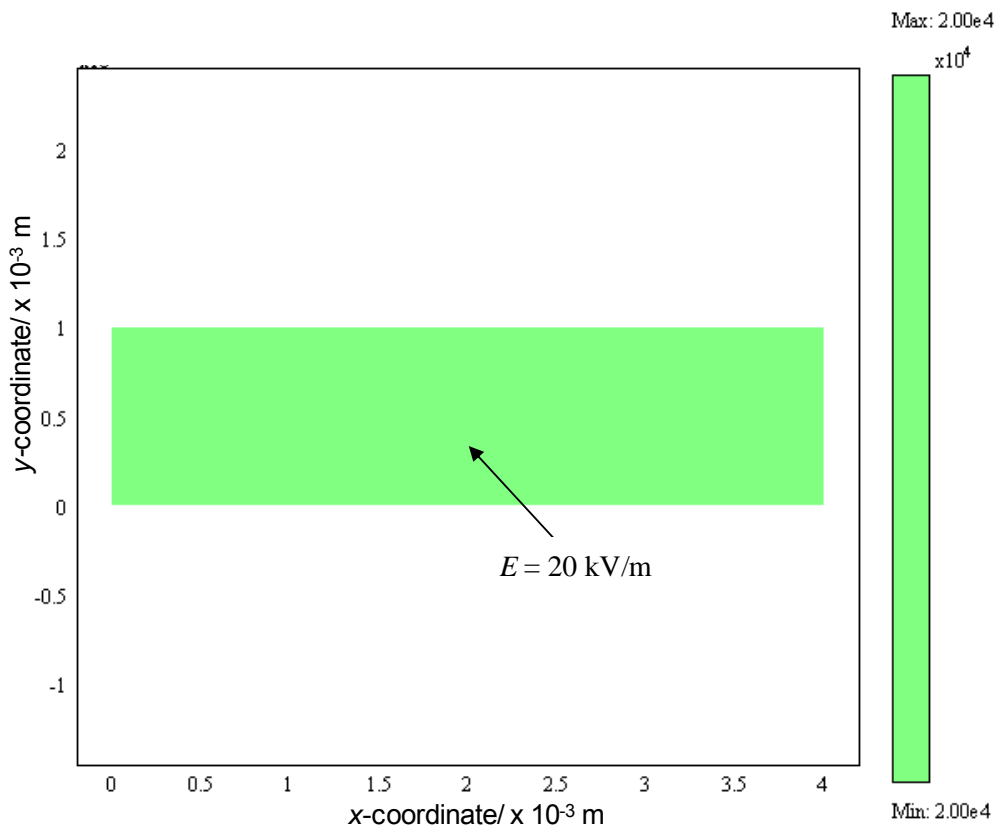


Figure 5.3: Surface plot of electric field ( $\text{V.m}^{-1}$ ) computed using Comsol

### 5.4.2 AC Simulation

For this study, a planar 2D rectangular region representing a rectangular polymer block under the influence of an AC voltage was used to benchmark the method for AC simulation in Comsol, as illustrated in Figure 5.4. The polymer material was given a dissipation factor (DF) of 0.0012 and dielectric constant,  $\epsilon_r$ , of 3.8, and was subjected to a 10 V AC potential at frequencies between 10 Hz and 0.1 MHz to study the resulting dielectric losses and consequent resistive heating.

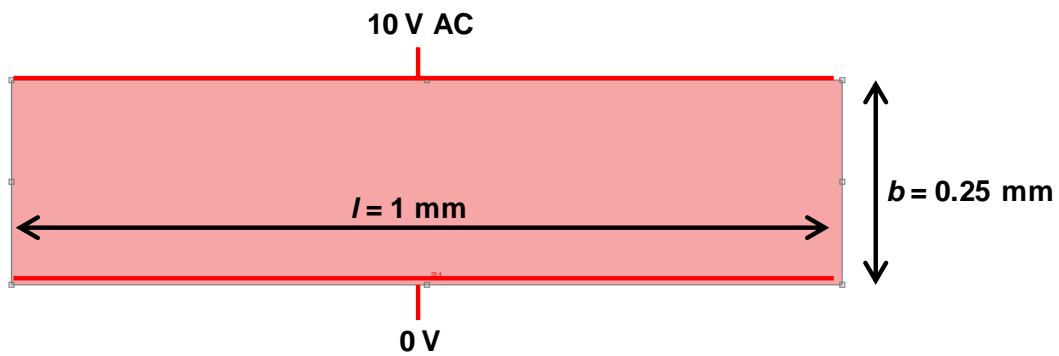


Figure 5.4: 2D model of a polymer block

The heat dissipated due to direct or low alternating frequency alternating current flow through a material (also known as resistive or ohmic heating) is normally determined by the material resistance, the magnitude of the potential difference and the current flowing across the material. The analytical solution used to determine the resistive heating  $P$  is as shown in equation 5.13 where  $V$  represents the applied voltage (r.m.s for AC), and  $R$  is the dielectric resistance (Avison, 1989):

$$P = V^2 / R \quad \text{Equation 5.13}$$

where resistance,  $R$ , of a component with a uniform cross-sectional area,  $A$ , and length,  $l$ , is:

$$R = \rho \frac{l}{A} \quad \text{Equation 5.14}$$

where  $\rho$  is the electrical resistivity.

The resistive heating,  $P$ , as a function of the component cross-sectional area,  $A$ , its length,  $l$ , and its electrical resistivity,  $\rho$ , can therefore also be calculated according to equation 5.15:

$$P = \frac{V^2 A}{\rho l} \quad \text{Equation 5.15}$$

The behaviour of lossy dielectrics such as the polymers being considered under AC conditions is reviewed in detail in Chapter 6, however the constitutive equations governing this behaviour, and that have been used to benchmark the AC simulation methodology in Comsol, are summarised in equations 5.16 – 5.18 (Pecht et al., 1999):

$$\rho = \frac{l}{\sigma} \quad \text{Equation 5.16}$$

$$\sigma = \omega \times DF \times \varepsilon \quad \text{Equation 5.17}$$

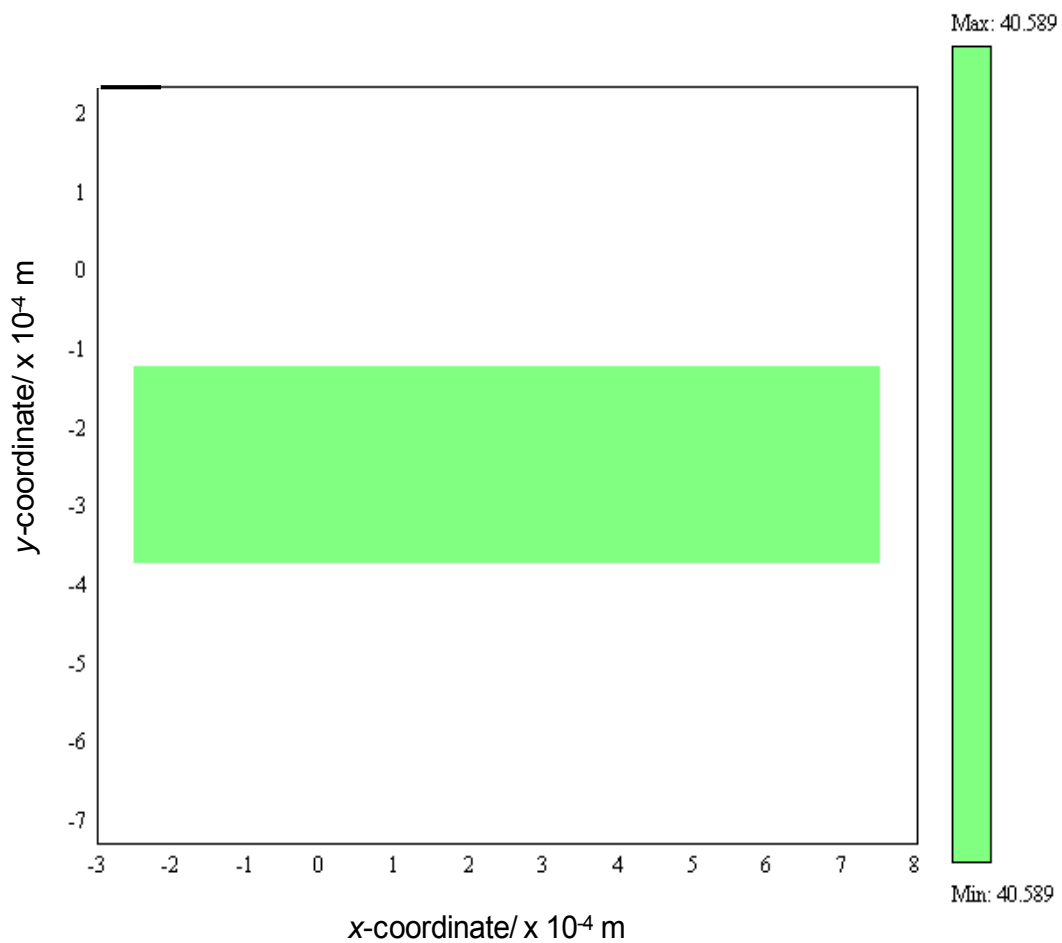
$$\varepsilon = \varepsilon_r \varepsilon_o \quad \text{Equation 5.18}$$

$$\omega = 2\pi f \quad \text{Equation 5.19}$$

where  $\sigma$  is the dielectric conductivity,  $\omega$  is the angular frequency (related to frequency  $f$  according to equation 5.19),  $\varepsilon$  is the dielectric permittivity and  $\varepsilon_o$  is the permittivity of a vacuum ( $8.854 \times 10^{-12}$  F/m).

A surface plot of the resistive heating is shown in Figure 5.5 for a frequency,  $f$ , of 0.1 MHz, while its corresponding variation when the frequency,  $f$ , varies between 10 Hz and 0.1 MHz is illustrated in Figure 5.6. From the latter, it can be seen the magnitude of the losses increases linearly as the frequency is

raised. Also, the calculated resistive heating values (using Equations 5.13 - 5.19) are also observed to complement those obtained from Comsol simulation. For instance, when the frequency  $f$  is 0.1 MHz, the loss predicted using Comsol is observed to be  $40.6 \text{ Wm}^{-3}$ , as indicated from the contour plot in Figure 5.5. A similar value is also obtained when the relevant equations (Equations 5.13 - 5.18) are used as depicted in Figure 5.6 – thereby validating the selection and use of the AC simulation tools from Comsol.



**Figure 5.5: Surface plot for 0.1MHz frequency ( $\text{W.m}^{-3}$ )**

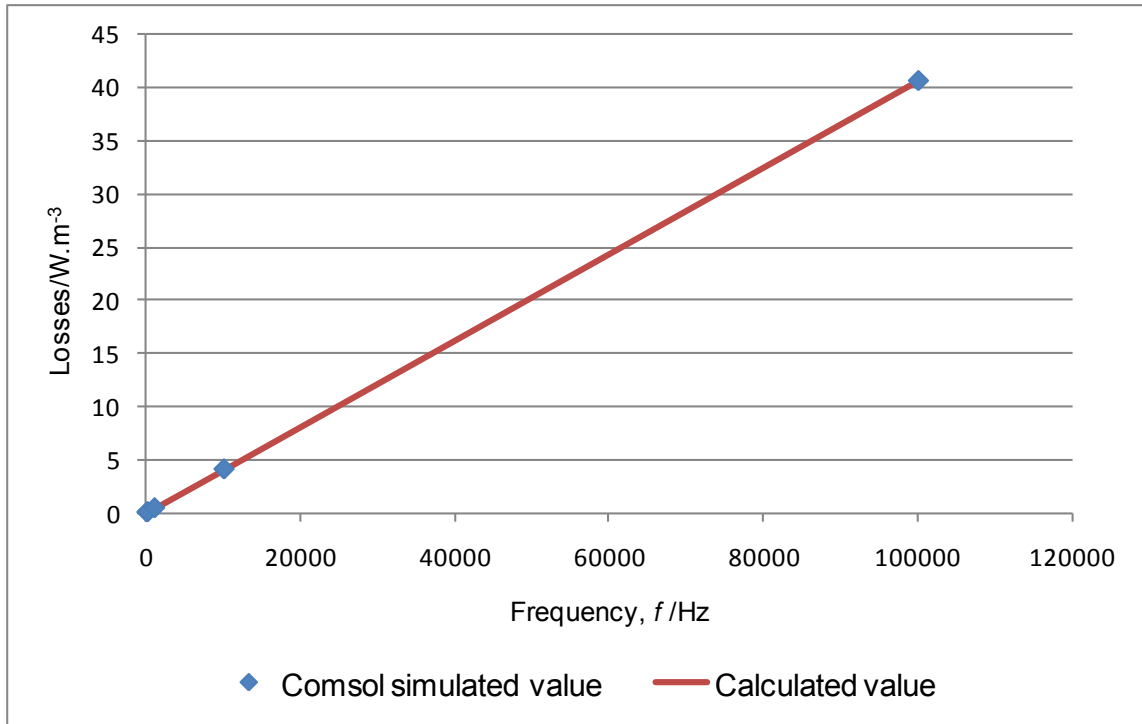


Figure 5.6: Variation of dielectric losses with frequency

### 5.4.3 Thermo-mechanical Simulation

A model of a bimetallic strip (Figure 5.7) consisting of two metal strips (copper and molybdenum) joined together perfectly was used to validate the use of the *stress-strain* application mode in Comsol for thermo-mechanical analysis. The materials properties used for the computational modelling studies are shown in Table 5.1. The model was subjected to a temperature change,  $\Delta T$ , from 273.15 K to 373.15 K ( $\Delta T = 100$  K), and the resulting thermal stresses compared with an analytical solution (Equations 5.19 – 5.21) (Young et al., 2000).  $\sigma_A$  is the thermal stress along the top surface of the copper strip (Material A in this case), while  $\sigma_B$  is the stress along the bottom surface of the molybdenum strip (Material B).

$$\sigma_A = \frac{-(\alpha_A - \alpha_B) \cdot \Delta T \cdot E_A}{K_1} \left[ 3 \left( \frac{t_A}{t_B} \right) + 2 \left( \frac{t_A}{t_B} \right) - \frac{E_B t_B}{E_A t_A} \right] \quad \text{Equation 5.20}$$

$$\sigma_B = \frac{(\alpha_B - \alpha_A) \cdot \Delta T \cdot E_B}{K_1} \left[ 3 \left( \frac{t_A}{t_B} \right) + 2 - \frac{E_A}{E_B} \left( \frac{t_A}{t_B} \right)^3 \right] \quad \text{Equation 5.21}$$

where

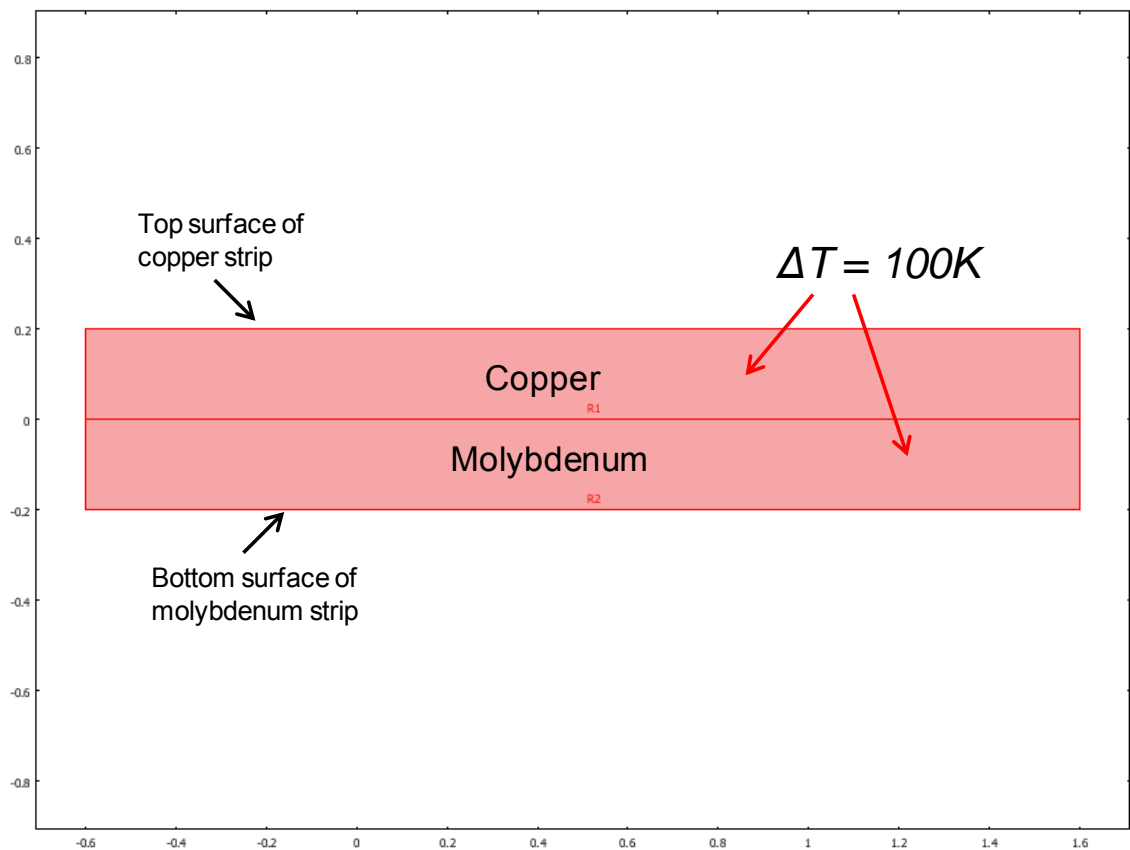
$$K_1 = 4 + 6 \frac{t_A}{t_B} + 4 \left( \frac{t_A}{t_B} \right)^2 + \frac{E_A}{E_B} \left( \frac{t_A}{t_B} \right)^3 + \frac{E_B t_B}{E_A t_A} \quad \text{Equation 5.22}$$

The definitions of the variables in each equation are as follows:

$\alpha_A, \alpha_B$  - Thermal coefficient of expansion in materials A and B

$t_A, t_B$  - Thickness of materials A and B

$E_A, E_B$  - Young's modulus of materials A and B

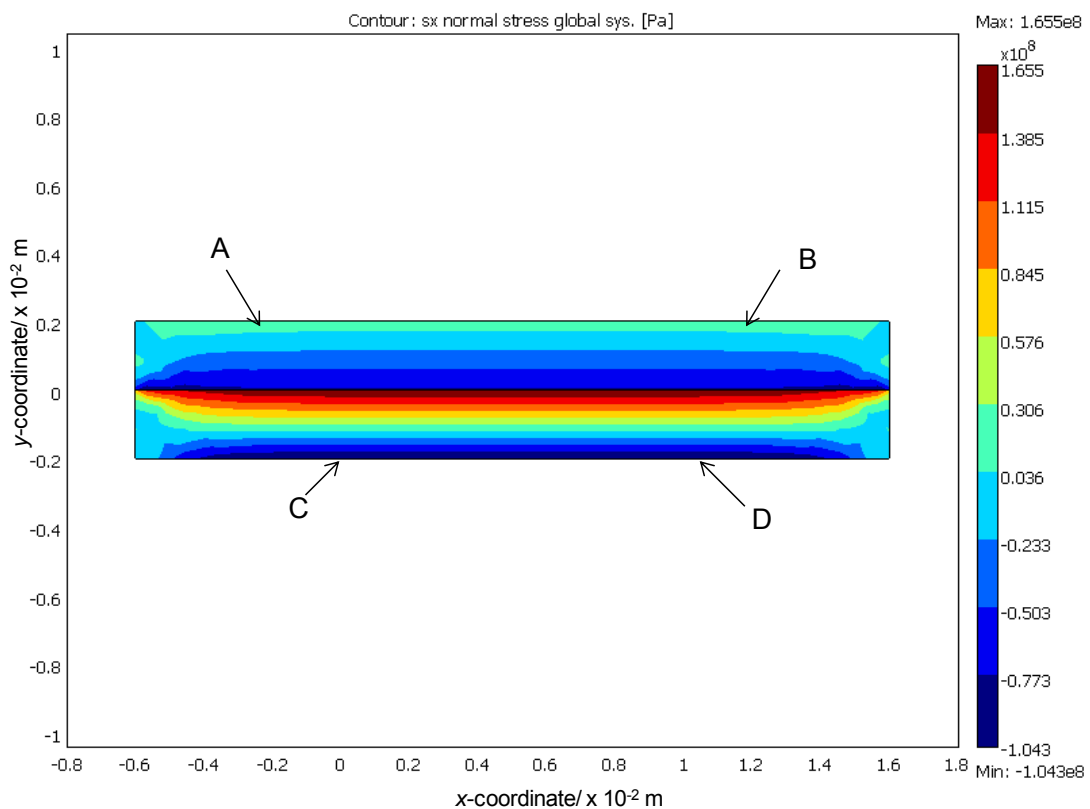


**Figure 5.7: Plane strain 2D model of bimetallic strip**

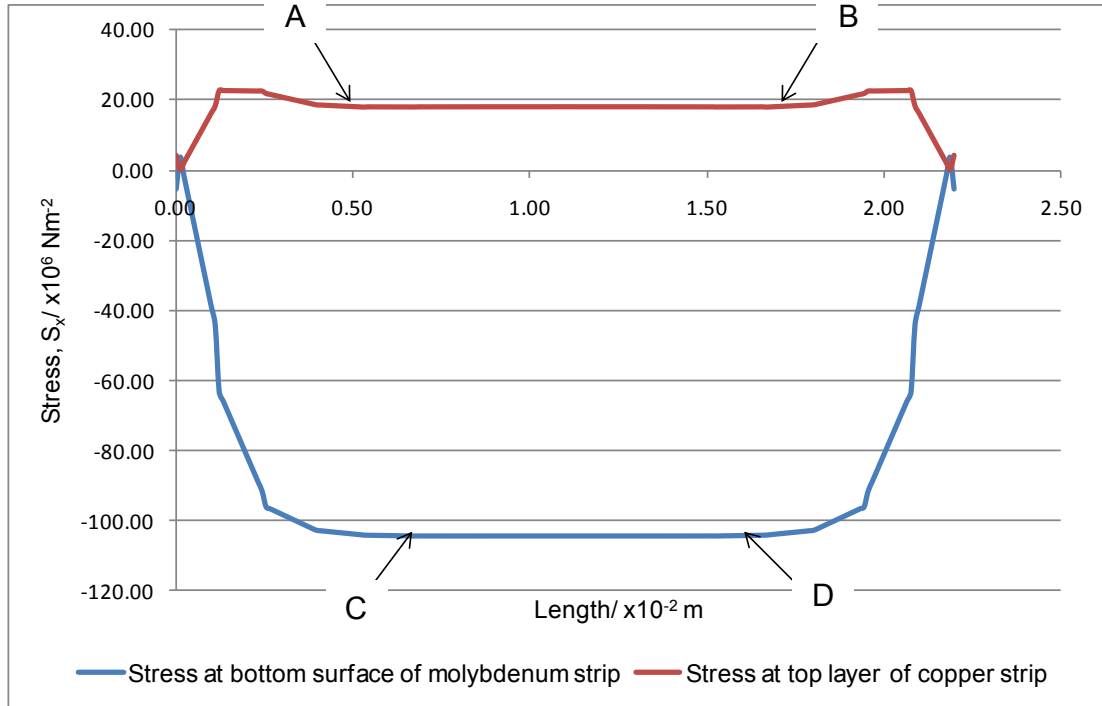
Property	Copper (Mat. A)	Molybdenum (Mat. B)
Thermal coefficient of expansion, $\alpha/\times 10^{-6} \text{ K}^{-1}$	16.5	4.8
Young's modulus, $E/\text{GPa}$	119	329

**Table 5.1: Properties for materials in thermomechanical simulation**

Figure 5.8 illustrates the predicted x-direction thermal stress distribution in the bimetallic strip as a result of the temperature change, while the stress variation along the top copper layer surface and bottom layer of the molybdenum strip are shown in Figure 5.9.



**Figure 5.8: Stress distribution ( $S_x$ ) across bimetallic strip arising due to temperature increase**



**Figure 5.9: Variation of stress  $S_x$  along the top and bottom layer of bimetallic strip**

As can be seen in Figures 5.8 and 5.9, the thermal stress along the top surface of the copper strip was observed to vary predominantly between 18  $\text{MN/m}^2$  and 23  $\text{MN/m}^2$ , and between -100  $\text{MN/m}^2$  and -104  $\text{MN/m}^2$  along the bottom surface of the molybdenum metal. In fact, because the stress variation between points AB along the top and CD along the bottom surface of the bimetallic strip were noticed to be in exact agreement with the calculated values (using equations (using equations 5.20 – 5.22), i.e. 18.2  $\text{MN/m}^2$  along the top of the copper layer and -104  $\text{MN/m}^2$  along the bottom of the molybdenum strip, the selected *Stress-Strain* application mode in the Structural module of Comsol was concluded to be valid for the thermomechanical simulations.

## 5.5 Summary

This chapter has outlined the benefits of using Finite Element Analysis (FEA) as opposed to conventional complex analytical solutions in the design of the thyristor device housing. An overview of the finite element analysis steps,



together with the background theory the selected FEA solver (Comsol Multiphysics) uses to solve electrical and thermomechanical problems have also been presented. Finally the tools Comsol Multiphysics provides for electrical and thermomechanical studies have been validated by modelling geometrically simple problems (whose solutions can be found analytically) and comparing the simulated and calculated values. In this case, analytical published solutions for the various problems were found to match closely the Comsol simulations. It is therefore concluded that use of the Comsol FEA solver is appropriate for the electrical and thermomechanical studies described in the following chapters.

## **6 Electrical performance studies for polymeric thyristor housings**

### **6.1 Introduction**

High voltages are today used in a wide variety of applications such as cathode ray tubes, generation of X-rays, electrical power distribution, and various industrial and scientific uses. For all these uses, the high voltage equipment being used requires careful design of its insulation to sustain the various conditions it is exposed to, since insulation failure can cause serious safety, technical and economic issues (Naidu et al., 2009). In fact, with the demand for high voltage technology in areas such as power distribution and transmission, reliable high voltage systems with insulation that is less likely to fail during service is becoming increasingly important.

In this chapter, the electrical performance of the polymer-based housing for the high voltage thyristor device is studied. The first part of the chapter discusses the electrical behaviour of polymers and reviews key dielectric properties that need to be considered when designing such a polymeric package. The influence of a static (or DC) potential on the housing performance is then discussed to identify any localised electrical stress regions in the package and whether the polymer may degrade during service. Finally the effect of a varying (i.e. AC) potential on the electrical field distribution and any temperature gradients resulting from dielectric losses within the package, has been investigated.

### **6.2 Electrical Properties of Polymers**

Investigating the performance and failure mechanisms of insulation systems is an active area of research for which numerous studies have been undertaken

in the past. For example, James et al., 2009 conducted partial discharge tests on high voltage cables used as transmission lines to study the location and voltage at which a discharge appeared, and the magnitude of these discharges in order to mitigate insulation failures and improve the service life of such components, while Fabian et al., 2005 identified different insulation failure modes in Insulated Gate Bipolar Transistor (IGBT) power modules and described an optical inspection based experimental analysis method to identify critical regions of high electric fields. Example of some other works also include Vakser et al., 1994 who proposed various novel recommendations to minimise the stresses that occur due to mechanical, electrical and thermal conditions in the insulation of coils for high voltage rotating electrical machines, and among others Brütsch et al., 2008 who studied insulation failures in power generators arising due to operating conditions. The latter work identified that insulation failures could be classified into four main types namely (1) design, (2) material, (3) manufacturing, and (4) maintenance failures, and also found aging and internal discharges to be the dominant root causes of insulation failures for power generation systems. Among other findings, they also showed that the aging phenomenon in such systems is a combination of mechanical and thermal stresses rather than due to electrical stresses only.

During service, the voltage across the device will normally be complex, comprising of 50/60 Hz fundamental frequency components, harmonics, repetitive fast transient voltages and a DC component. In these cases, the polymer housing can potentially experience dielectric losses due to the high frequency content of the applied voltage. Also, the DC voltage component, which will lead to polarisation of the material (i.e. a redistribution of charges in the material where the positive charges are attracted towards the negative electrode and vice versa). Such DC components will be applied for prolonged periods (weeks or even months) followed by rapid reversal to the opposite polarity, which can lead to abnormally high local voltage gradients (Woodhouse, 2007a). In these circumstances, the integrity of the housing is critical for the reliable operation of the power thyristor along with other components. The required electrical properties of polymers used in such high

voltage applications include a suitable dielectric constant, loss tangent, and dielectric strength among others. The other important electrical properties that polymeric package materials should have are overviewed in section 6.2.1. These discussions are summarised from Goosey, 1999, Pecht et al., 1999 and Hoffman, 1957, before the electrical modelling studies are overviewed.

### **6.2.1 Electrical Behaviour of Polymers**

In order to be of use in electrical and electronic applications, a polymer should have appropriate properties over a broad range of temperatures, frequency and humidities. Most polymer materials are considered good dielectrics or insulators, where they resist the flow of current upon application of a potential difference. Compared to metals whereby the atomic nuclei are surrounded by a sea of electrons, polymers and their atoms that make them up have their electrons tightly bound to a central long chain and side groups through covalent bonding. Typical resistivity values for polymers are of the order  $10^{12}$   $\Omega\text{cm}$  compared to  $10^2 - 10^4$   $\Omega\text{cm}$  for semiconductors, and  $10^{-5}$   $\Omega\text{cm}$  for metals (Shashoua, 2008).

Depending on their molecular structure, polymers can be classed as polar or non-polar dielectrics. In polar dielectrics, dipoles are present due to an imbalance in the electron distribution, whereas the molecular bonds in a non-polar polymer are fully covalent and generally have symmetrical molecules. No polar molecules are present in such polymers, and application of an electric field does not cause dipole realignment. However it does cause electron polarisation in the material when the electrons are shifted in the direction of the applied electric field. These types of dielectrics tend to have dielectric constants less than 3, whereas polar dielectrics have higher dielectric constants, e.g. at low frequencies (60 Hz), polar plastics have dielectric constants between 3 and 9, and at high frequencies ( $10^6$  Hz) dielectric constants between 3 and 5 (Zeus Inc, 2010).

For polar dielectrics, dipolar polarisation tends to take place, and application of an external electric field causes a reorientation of the dipoles in the direction of the applied field. When an AC potential is applied across the dielectric, it is alternately charged and discharged each half cycle. During the change of polarity, the charges of the dipole are displaced through the dielectric first in one direction and then in the other, and overcoming the opposition they encounter leads to heat production through dielectric loss. As a result, the dissipation factor ( $\tan \delta$ ), which is indicative of the level of dielectric loss by representing the ratio of power loss in a dielectric material to the power transmitted through it, tends to be one of the more important electrical properties when polymers are used in electrical applications. A review of other important dielectric properties (e.g. permittivity, dielectric strength, arc resistance and comparative tracking index) that need to be considered when using polymers in high voltage applications, such as for the thyristor housing, is described next.

#### 6.2.1.1 Permittivity

To account for the charge storage in a dielectric due to a time-varying potential, the permittivity (which is a complex number) is used. The permittivity,  $\epsilon$ , which is a measure of how much resistance is encountered when forming an electric field in the dielectric, is related to the electric susceptibility,  $\chi_e$ , i.e. how easily a dielectric polarises under an applied field, according to equation 6.1 where  $\epsilon_0$  is the permittivity of free space (equal to  $8.85418782 \times 10^{-12}$  F/m).

$$\epsilon = (1 + \chi_e)\epsilon_0$$

Equation 6.1

### 6.2.1.2 Relative Permittivity

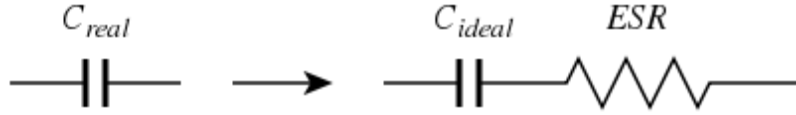
The relative permittivity (or dielectric constant) of an insulation material reflects the extent to which it can concentrate the electrostatic lines of flux. Numerically, it is the ratio of the capacitance of a capacitor using the material as dielectric between its electrodes, to the capacitance of the same capacitor with vacuum or free space between the electrodes. Most materials possess a dielectric constant,  $\epsilon_r$ , that depends to some extent on the frequency of the applied electromagnetic field. The dependence on the electrical frequency is due to the reorientation of inherent dipoles in the material, electronic polarisation of the atoms of the material, and also the displacement of any ions within its molecules. The relative permittivity can vary from one to several thousands for some inorganic materials (Goosey, 1999), and is related to electric susceptibility,  $\chi_e$ , according to equation 6.2, and to the permittivity,  $\epsilon$ , according to equation 6.3.

$$\epsilon_r = 1 + \chi_e \quad \text{Equation 6.2}$$

$$\epsilon_r = \frac{\epsilon}{\epsilon_0} \quad \text{Equation 6.3}$$

### 6.2.1.3 Loss tangent or Dissipation factor, $\tan \delta$

The loss tangent or dissipation factor ( $\tan \delta$ ) is a measure of the energy dissipation due to a varying electric field applied across a dielectric. Any dielectric between two conductors will form a capacitor, which in equivalent circuits is typically represented as a lossless capacitor in series with a resistor termed as the equivalent series resistance (ESR) responsible for the energy dissipated as heat, as shown in Figure 6.1.



**Figure 6.1: Model of a dielectric placed between conductors**

A good dielectric is often characterised as having a low ESR, while a poor insulator has a large ESR value. The ESR value is normally governed by the mobility of dielectric conduction electrons and the dipole relaxation phenomena. In a dielectric either the conduction electrons or dipole relaxation typically dominates loss (Ramo et al., 1994). For instance, when the conduction electrons are responsible for the dominant loss, the ESR is calculated using equation 6.4,

$$ESR = \frac{\sigma}{\epsilon \omega^2 C} \quad \text{Equation 6.4}$$

where  $\sigma$  is the bulk conductivity of the dielectric,  $\omega$  is the angular frequency of the applied alternating current,  $\epsilon$  is the lossless permittivity of the dielectric, and  $C$  is the lossless capacitance. When an AC potential is applied to the dielectric, the dissipation factor (DF) due to the non-ideal dielectric is expressed as the ratio of the resistive power loss in the ESR to the reactive power oscillating across the dielectric (equation 6.5), and is related to the resistivity and permittivity of the polymer according to equation 6.6.

$$DF = \frac{i^2 ESR}{i^2 |X_c|} \quad \text{Equation 6.5}$$

$$DF = \frac{\sigma}{\epsilon \omega} \quad \text{Equation 6.6}$$

#### **6.2.1.4 Dielectric Strength**

The dielectric strength of a dielectric is a measure of its ability to withstand voltage without breakdown or passage of considerable amounts of current, before an arc forms and eventually leads to partial discharge and breakdown failure of the material. It is defined as the minimum voltage at or below which no breakdown occurs, and in practice depends on properties such as molecular structure, level of impurities, voids present in the specimen, and the relative humidity and temperature to which the sample has been exposed (Goosey, 1999).

#### **6.2.1.5 Arc Resistance**

The arc resistance of a dielectric is defined as the time that its surface can be exposed to an arc before dielectric breakdown occurs. The arc resistance of a dielectric is dependent upon its molecular structure and the presence and amount of certain additives, such as alumina and silica, in their formulation can give considerable improvements. Arc resistance is also dependent on the condition of the surface and is easily reduced by moisture, salts, or grease, e.g. from skin contact (Goosey, 1999).

#### **6.2.1.6 Comparative Tracking Index (CTI)**

The tracking index is the relative resistance of dielectrics to tracking when the surface is exposed under electrical stress to water containing ionic contaminants. During service, insulating materials exposed to high voltage gradients combined with ionic contamination need to be resistant to tracking, and need to have as high a CTI as possible. CTI values of dielectrics are influenced by the presence of additives used in their formulation. For instance, they can be lowered by pigments, e.g. carbon black, and by flame retardants



and glass fibres, and can be raised by addition of minerals such as titania (Goosey, 1999)

### **6.3 Research Scope**

Because polymer materials behave differently under different electrical stresses, understanding the influence of both static and time-varying potential differences was considered important when polymers are used instead of ceramic for the thyristor housings.

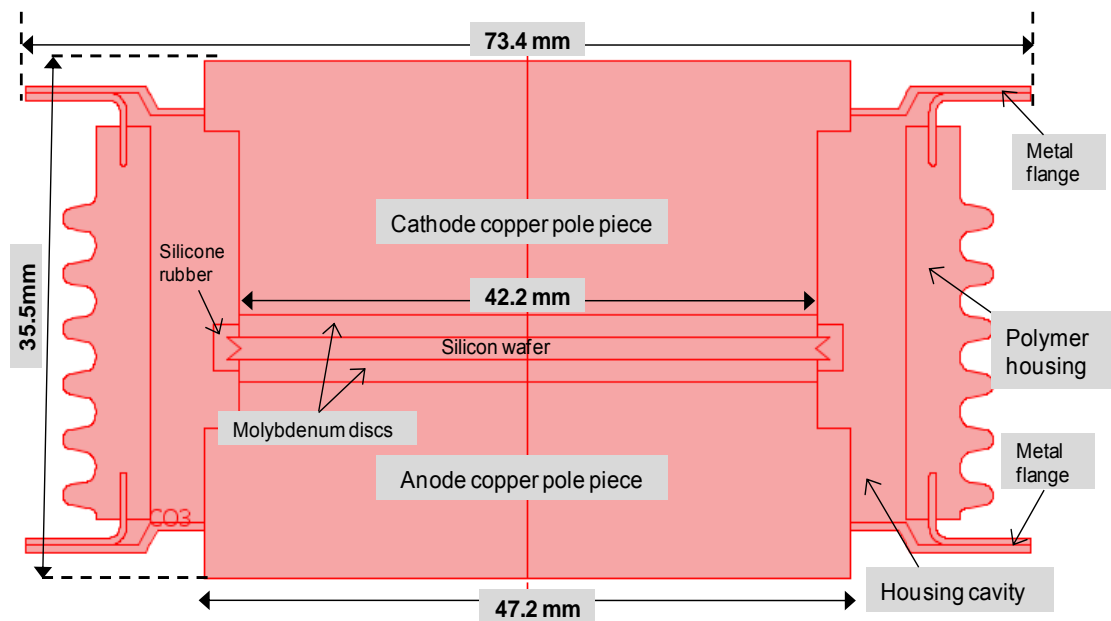
In section 6.4, the performance of the polymer package when a static voltage (direct current (DC)) is applied between the copper pole pieces of the thyristor is investigated. It aims to identify the existence of any localised electrical stress regions and design options that will reduce these stresses within the housing. Such a study is important as different investigations, e.g. Phillips et al., 2008, have shown that the occurrence of such localised high electric field regions plays a dominant role in polymer materials degradation in high voltage applications.

Section 6.5 then discusses the effect of a time-varying potential (i.e. at a 50 Hz frequency and harmonics thereof). Here, the influence of the AC voltage on the electric field strength and the energy loss density has been analysed. The resulting temperature changes that occur within the package due to such energy losses are also investigated to assess the risk of them contributing to the deterioration of the polymer material of the housing.

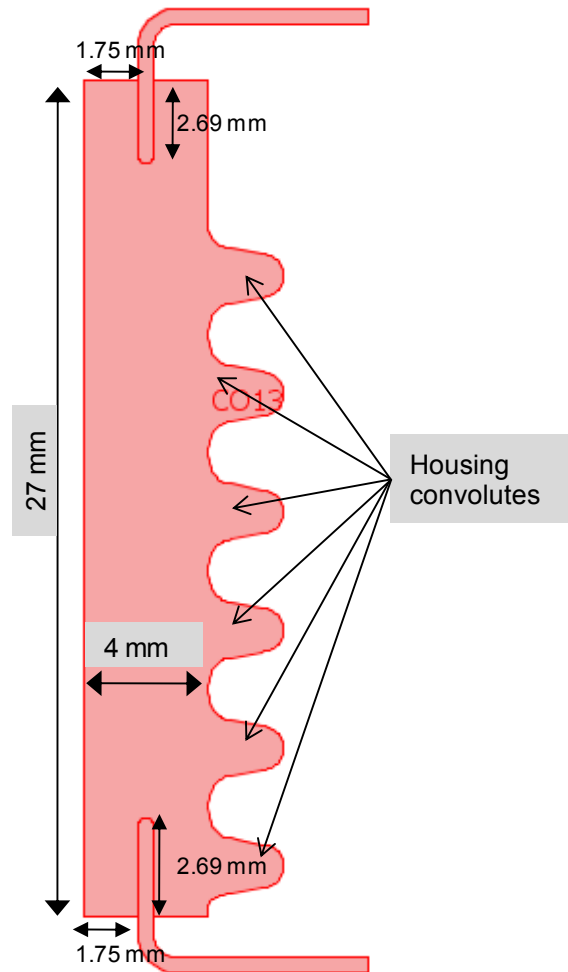
For the electrical simulation studies described in this chapter, a preliminary housing design based on a 50 mm hockey-puck ceramic housing was selected, as shown in Figure 6.2. As described in Chapter 4, this initial concept was based on a 'replacement' design configuration, where the ceramic housing was directly replaced by a polymer. However, compared to the commercial 50 mm hockey-puck ceramic thyristor, the polymer prototype was based on a 3-part configuration consisting of the polymer housing with

the metal flanges overmoulded within at both the cathode and anode ends, and separate anode and cathode pole pieces.

As shown in Figure 6.2, in the preliminary design the diameter of the silicon wafer and copper pole pieces were respectively 42.2 mm and 47.2 mm, while the external diameter and vertical height of the thyristor package were each 73.4 mm and 35.5 mm. A detailed overview of the housing dimensions and metal flange arrangement is also illustrated in Figure 6.3. As shown in Figure 6.3, the housing was based on a design having 6 convolutes and with a wall thickness and package height of 4 mm and 27 mm respectively. The metal flanges were based on a straight insert design whose ends were rounded. Their thickness was selected to be 0.5 mm, while the depth it protrudes inside the housing and its location from the inner housing edge were respectively 2.69 mm and 1.75 mm.



**Figure 6.2: Cross-section of the preliminary 50 mm prototype design**



**Figure 6.3: Overview of the polymer package dimensions**

For the simulation studies, because the thyristor device is axially symmetric apart from the gate connection, the device was modelled as a 2D axisymmetric structure to reduce use of computational resources and analysis time. An illustration of the 2D axisymmetric model is shown in Figure 6.4. As described in previous chapters, the finite element model of the thyristor device was comprised of a silicon wafer sandwiched between molybdenum discs and cathode and anode copper pole pieces. This stacked assembly was then enclosed with the polymer housing. For the purpose of the simulation studies, the device was considered to be surrounded by air as the latter is an excellent dielectric. This model geometry was generated in Comsol, then assigned the appropriate material and boundary properties, before it was also meshed and solved in Comsol.

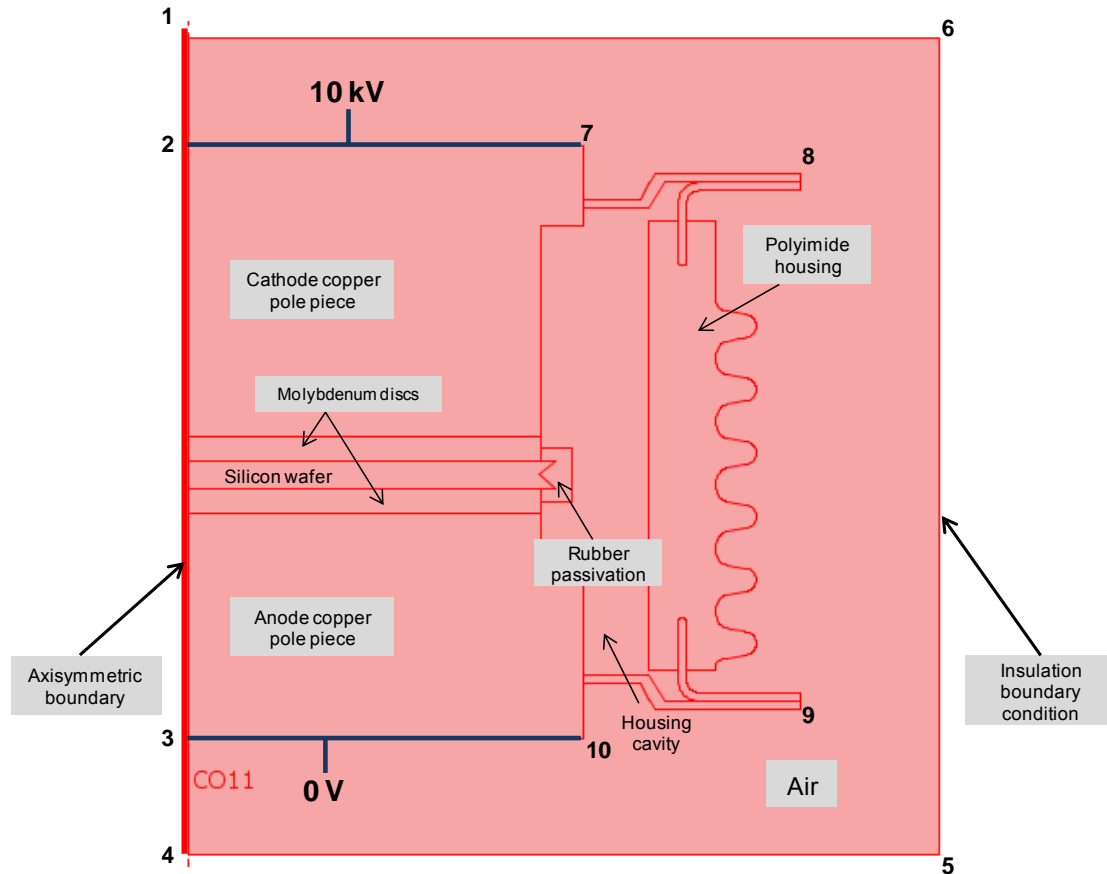


Figure 6.4: 2D axisymmetric model of the preliminary 50 mm prototype

For the DC simulation studies described in section 6.4, instead of the 8.5 kV rating required to achieve the goals of the NEWTON project, a higher 10 kV DC voltage was applied between the cathode and anode pole pieces to investigate the electrical behaviour of the 50 mm housing. The 10 kV voltage was applied across the ‘top’ surface (between points 2-7 in Figure 6.4) of the cathode pole piece, while the ‘bottom’ surface of the anode pole piece was maintained at 0 V (along edge 3-10). For the device to be modelled as a 2D axisymmetric model, edges 1-2, 2-3 and 3-4 of the device were defined as *axial symmetry* boundaries. On the other hand, exterior edges 1-6, 6-5 and 5-4 were taken as *insulation* boundaries so that no electric current flows across them; whilst the rest of the edges inside the device and along its exterior surface 7-8, 8-9 and 9-10 were defined as *continuity* to ensure any electric current is continuous across them.

The electrical conductivity values used to define the different components (or subdomains) of the FE model are listed in Table 6.1. The conductivity of the polymer housing material was based on a glass-reinforced polyimide polymer grade from DuPont™, while the surrounding air boundary was selected to have a lower electrical conductivity for the different studies since it is a better dielectric than polymers. On the other hand, the content of the housing cavity formed by the thyristor package and the stacked assembly of molybdenum discs, copper pole pieces and silicon wafer was also varied for the different electrical simulations described in later sections. Instead of the dry nitrogen that is commonly used in hockey-puck thyristors, conduction values representative of other materials were used. In cases where dry nitrogen was considered to be present in the housing cavity, an electrical conductivity similar to the surrounding air boundary was used. This is because an exact conductivity for dry nitrogen has been difficult to identify from the literature.

<b>Subdomain material</b>	<b>Electrical conductivity/Sm<sup>-1</sup></b>
Copper	$5.92 \times 10^7$
Molybdenum	$1.87 \times 10^7$
Polyimide	$3.03 \times 10^{-15}$
Rubber Passivation	$2 \times 10^{-15}$
Silicon wafer (Depletion region)	$1 \times 10^{-16}$
Air	$1 \times 10^{-18}$

**Table 6.1: Electrical conductivities of FE model subdomains**

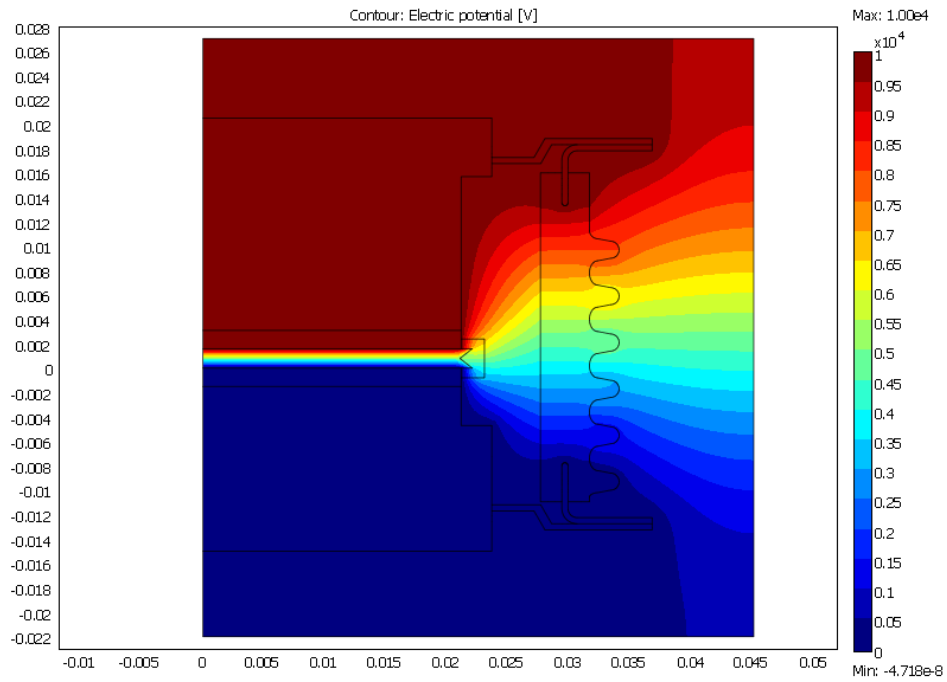
After the materials properties and boundary conditions were defined, the FE models were then automatically meshed in Comsol, before they were submitted to be solved as a static problem. For the computation, a direct solver was used, whilst the default Lagrange elements was used to mesh the FE model. Compared to cubic or linear Lagrange elements, order 2 (i.e. quadratic) elements were here used. This was because they were found to provide better trade-off between the accuracy of the computed results and the computational time and the simulation results were mesh independent.

## 6.4 DC Modelling Studies

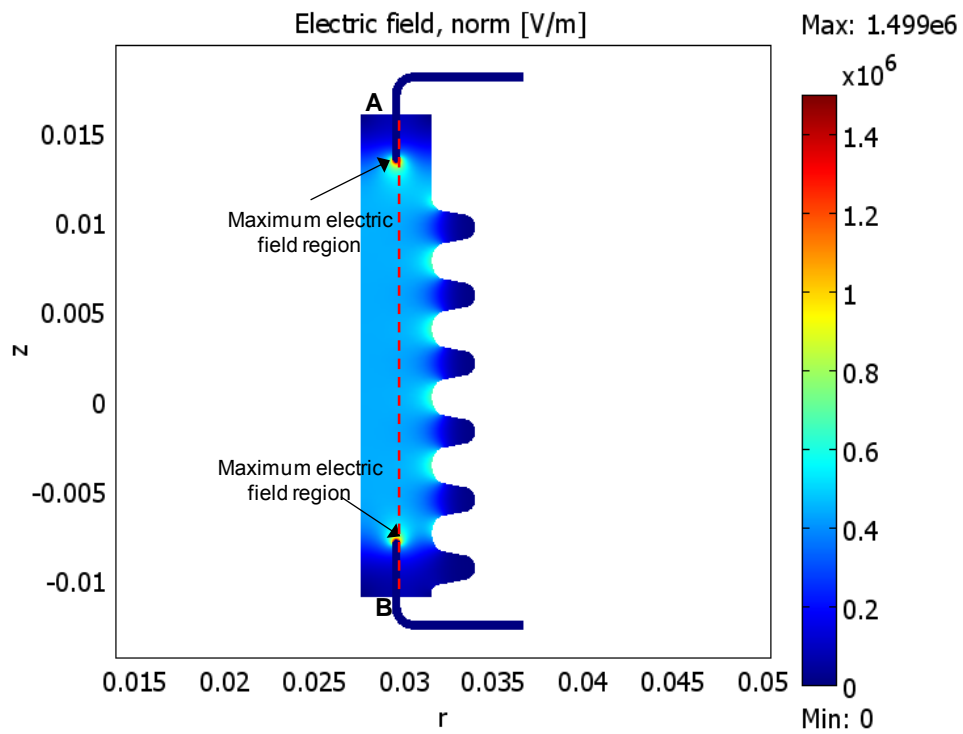
A typical contour plot of the electric potential distribution resulting from the 10 kV DC voltage applied between the pole pieces of the device (whose cavity is comprised of dry nitrogen) is shown in Figure 6.5. As can be seen, the electric potential spreads out from the silicon component, and results in different potential levels across the package.

Figure 6.6 also shows the corresponding electrical field strength plot within the package, while its variation along path AB can be seen in Figure 6.7. From this graph, the electric field magnitude can be seen to vary by around  $4.5 \times 10^5$  V/m order, and is significantly less than the dielectric strength of the selected polyimide grade ( $30.3 \times 10^6$  V/m in this case). As discussed earlier, because the electric field strength is lower than the dielectric strength of the selected polyimide polymer, this shows the risk of dielectric breakdown in such a package, provided no air voids are present, is low.

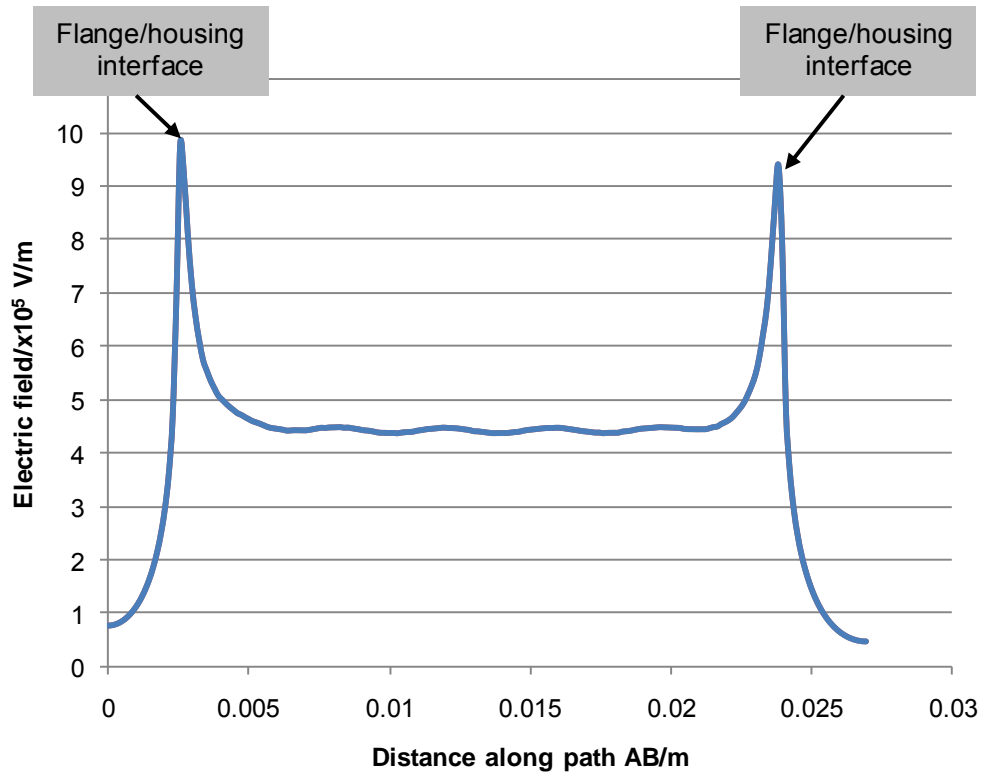
However localised high electric field strength magnitudes, corresponding to the sharp spikes in Figure 6.7 plot, were observed to occur at the interface regions at both the cathode and anode ends where the flange contacts the polyimide housing. Their magnitudes, which are also lower than the dielectric strength of the polymer, are seen to be equal at both ends and higher than other regions within the package. As highlighted earlier, because these localised occurrences are potential causes of failure for the device during service particularly if they coincide with voids or delamination, they are undesired.



**Figure 6.5: Electric potential contour plot for the whole device**



**Figure 6.6: Electric field contour plot within polyimide housing**



**Figure 6.7: Variation of electric field along path AB in housing**

The electric field distribution within an equivalent hermetic ceramic housing, whose electrical conductivity was taken to be  $1 \times 10^{-12}$  S/m and with dry nitrogen present within the internal housing cavity, is plotted in Figure 6.8, while a comparison of the electric field strength in the ceramic housing and the polyimide package, along identical paths CD and AB respectively, is shown in Figure 6.9. As can be seen from the graph, the variation of the electric field strength in the ceramic housing is seen to be identical to that for the polyimide package. As for the polyimide housing, the electric field is observed to be highest at the flange/housing interface regions. Their magnitudes are also seen to be equal at the cathode and anode end interface regions (Figure 6.9). Because the ceramic and polyimide materials have different electrical conductivities, this initial comparison suggests changing the electrical conductivity of the housing does not significantly influence the magnitude of the resulting electric field strength within it.



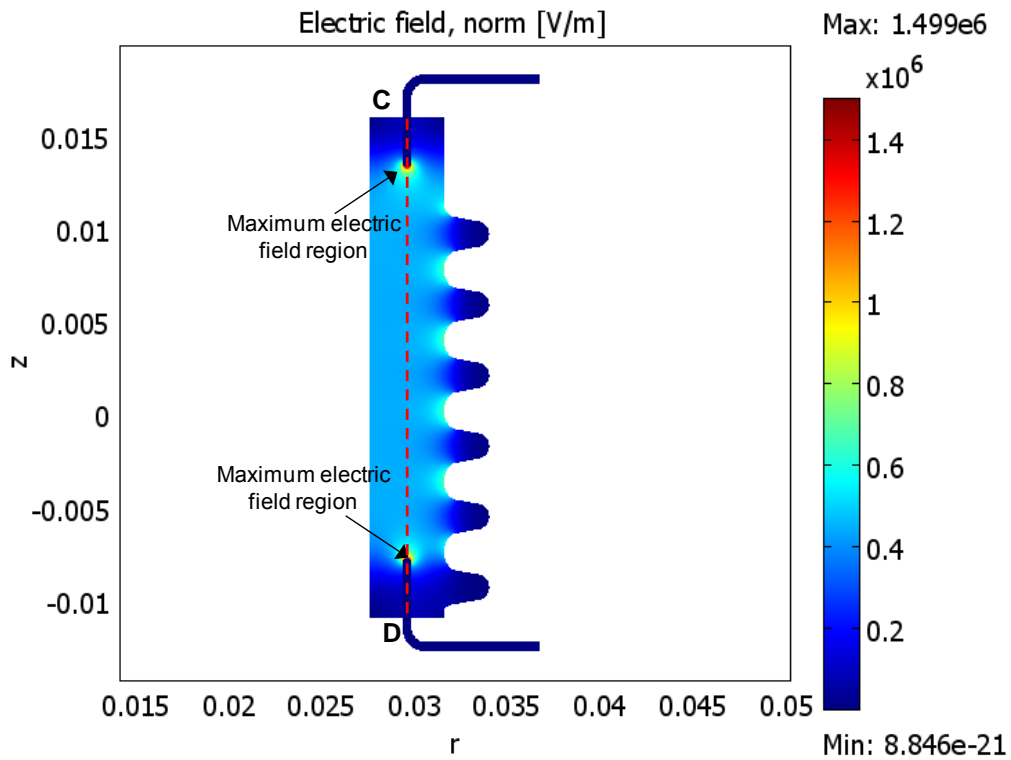


Figure 6.8: Electric field strength plot for ceramic housing

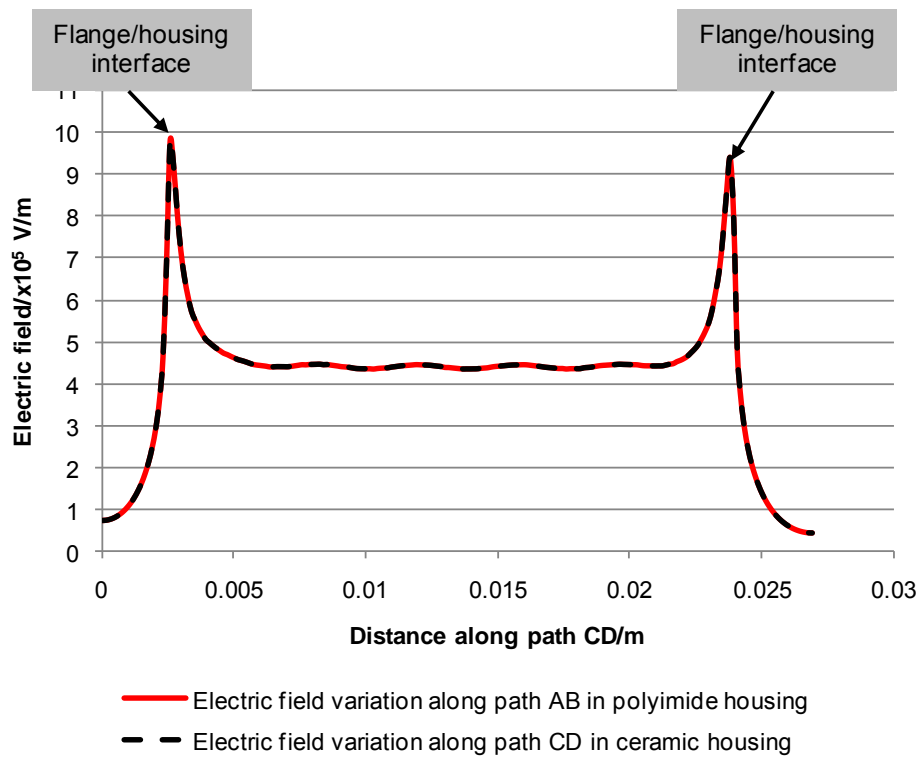


Figure 6.9: Comparison of electric field strength variation in ceramic and polyimide housings

Because intense localised electric fields were observed at the contact regions between the metal inserts and the polyimide housing at both the cathode and anode ends, attempts to reduce this electrical stress concentration and therefore the likelihood of insulation failure during normal service are described next. For these studies, the potential to reduce the localised electric field are investigated by varying the electrical conductivity of both the polymer housing material and that filling the housing cavity.

Studies, such as Wong et al., 1989, have shown that silicone gels improve the reliability of different electronic packages by acting as an excellent barrier to moisture. Because polymers are permeable to moisture, the electrical performance of the package, when the housing cavity is comprised of silicone gel instead of dry nitrogen, has been compared in section 6.4.1 to investigate effect of changing the electrical conductivity of the housing cavity. For this study, the electrical conductivity of the silicone gel was taken to be  $1 \times 10^{-13} \text{ Sm}^{-1}$ , i.e. 5 orders of magnitude higher than air. The influence of the electrical conductivity of the package is also studied in section 6.4.2. The electrical conductivity of the housing was varied over the range of the different polymer candidates identified by Ahmad, 2009.

#### **6.4.1 A comparison of silicone gel and dry nitrogen as cavity fillers**

The predicted electric field within the polyimide housing, when the housing cavity is filled with silicone gel, is shown in Figure 6.10, and the comparative plot of the electric field variation between points E and F across the package for both the silicone gel and dry nitrogen cases is seen in Figure 6.11.

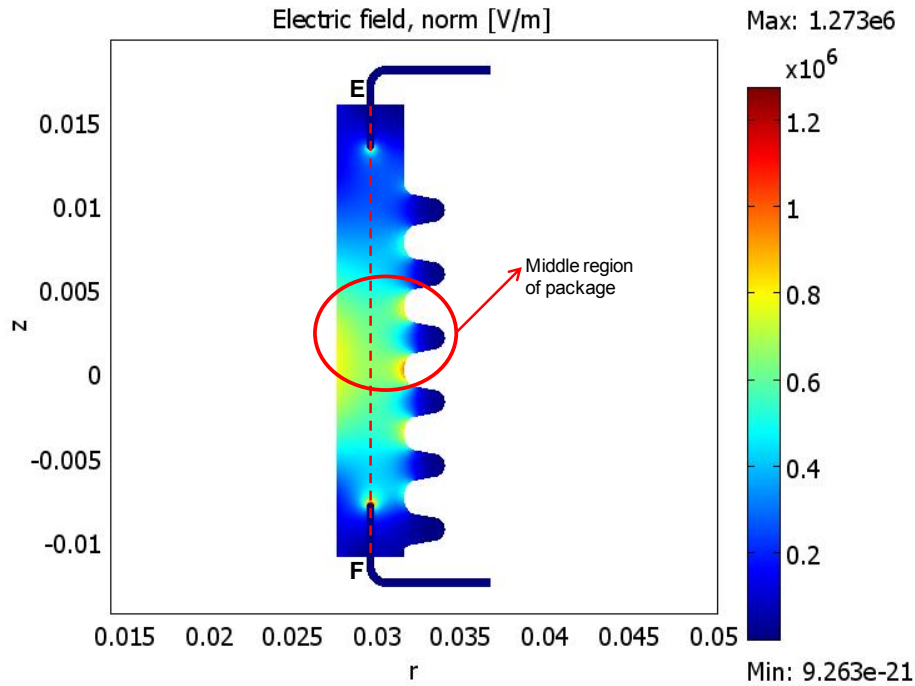


Figure 6.10: Electric field contour plot within polyimide housing when the housing cavity is filled with silicone gel

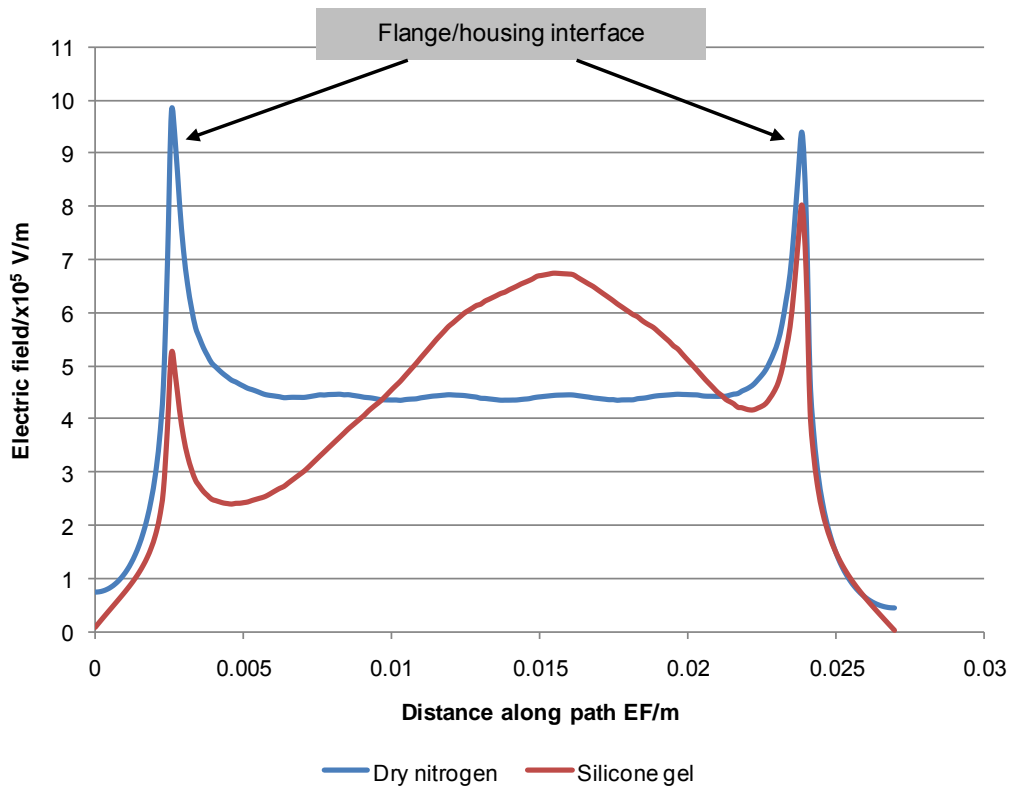


Figure 6.11: Comparative plot of electric field variation inside polyimide housing when either silicone gel or dry nitrogen is present

When silicone gel is present inside the housing cavity instead of dry nitrogen, localised regions of high electric field strength were again observed to occur at the flange and housing interface at both the cathode and anode ends (Figure 6.11). The average variation of the electric field magnitude within the housing was around  $5 \times 10^5$  V/m, and as observed in the dry nitrogen case it was less than the dielectric strength of the selected glass-filled polyimide polymer – thus suggesting risk of breakdown of a ‘void free’ polyimide housing is again low. From the plot, the localised electric field is also seen to be higher at the anode than at the cathode end. This is due to the unequal thickness of the copper pole pieces for the 50 mm housing studied. A comparison of the highest electric field strength at the anode interface region also showed the difference between their magnitude to be low. This again highlighted that changing the electrical conductivity of the housing cavity does not have substantial influence on the highest electrical field strength occurring in the interface region (anode end in this case) in the package.

From this study, the electric field variation along path EF was also observed to be different when the housing cavity consisted of either dry nitrogen or silicone gel. As can be seen in Figures 6.10 and 6.11, a high electric field was also noticed in the middle region of the housing comprised of silicone gel. Such varying electric field change was considered to result due to the different current paths inside the device when the DC potential was applied. When the dry nitrogen is filled inside the housing cavity, the electrical conductivity of the cavity content is orders of magnitude lower than of the polyimide housing. Consequently the current path between the cathode and anode flange ends are confined to the package wall causing the electrical field magnitude in the housing to be low and constant. This situation is also similar for the ceramic/dry nitrogen device configuration (Figures 6.6 & 6.7). On the other hand, when silicone gel is filled inside the housing cavity, the electrical conductivity of the housing cavity content is higher than of the polyimide material. Consequently the current paths can cross the housing cavity and affect the electrical field distribution in the package.

### 6.4.2 Comparison of Alternate Polymer Housing Materials

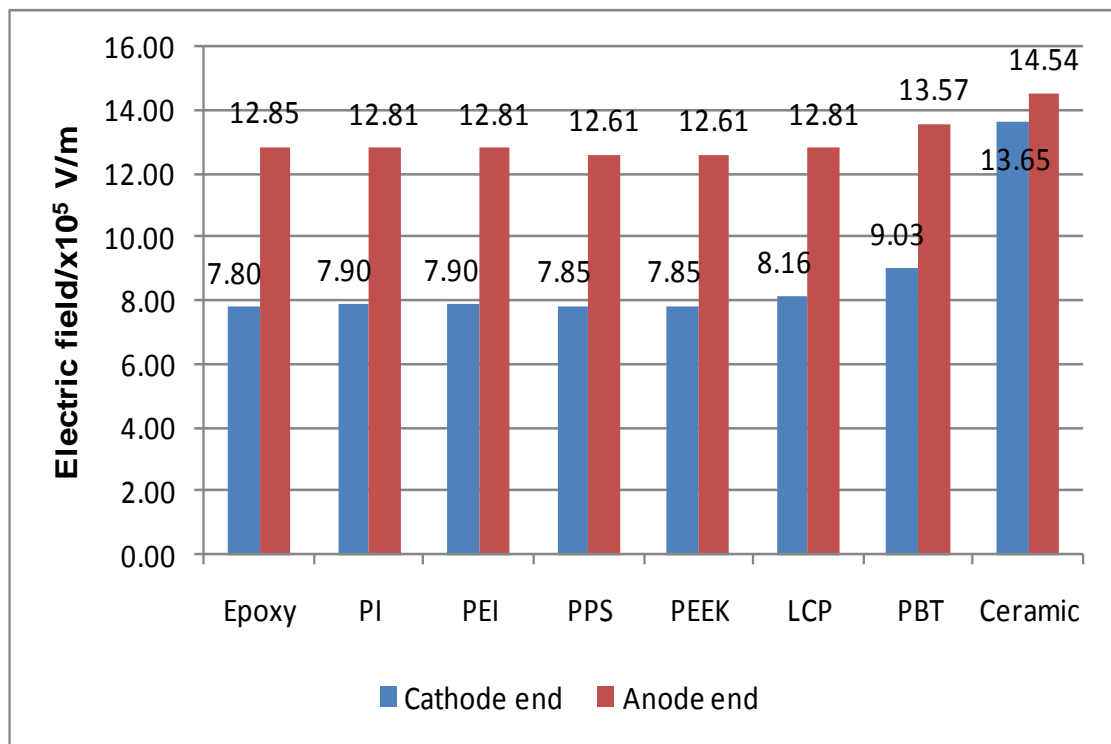
As highlighted in Chapter 4, studies by Ahmad, 2009 to select the appropriate polymers for thyristor housings identified polymers such as polyimide (PI), liquid crystal polymer (LCP), polyetherimides (PEI), polyphenylene sulfide (PPS), epoxy, polyetheretherketone (PEEK), and polybutylene terephthalate (PBT) to be suitable candidates. By comparing the shortlisted polymer candidates and the ceramic housing performance, the present study aims to investigate in greater detail the influence of changing the housing electrical conductivity on the electrical field strength magnitude in the anode and cathode flange/housing contact regions. The electrical conductivity values used for each polymer in the simulation studies (which are in equilibrium with the environment) are tabulated in Table 6.2.

Materials	Electrical Conductivity/ $\text{Sm}^{-1}$
Epoxy	$1 \times 10^{-16}$
PEI	$3.03 \times 10^{-15}$
PI	$3.03 \times 10^{-15}$
PEEK	$3.3 \times 10^{-15}$
PPS	$3.3 \times 10^{-15}$
LCP	$1 \times 10^{-14}$
PBT	$3.3 \times 10^{-14}$

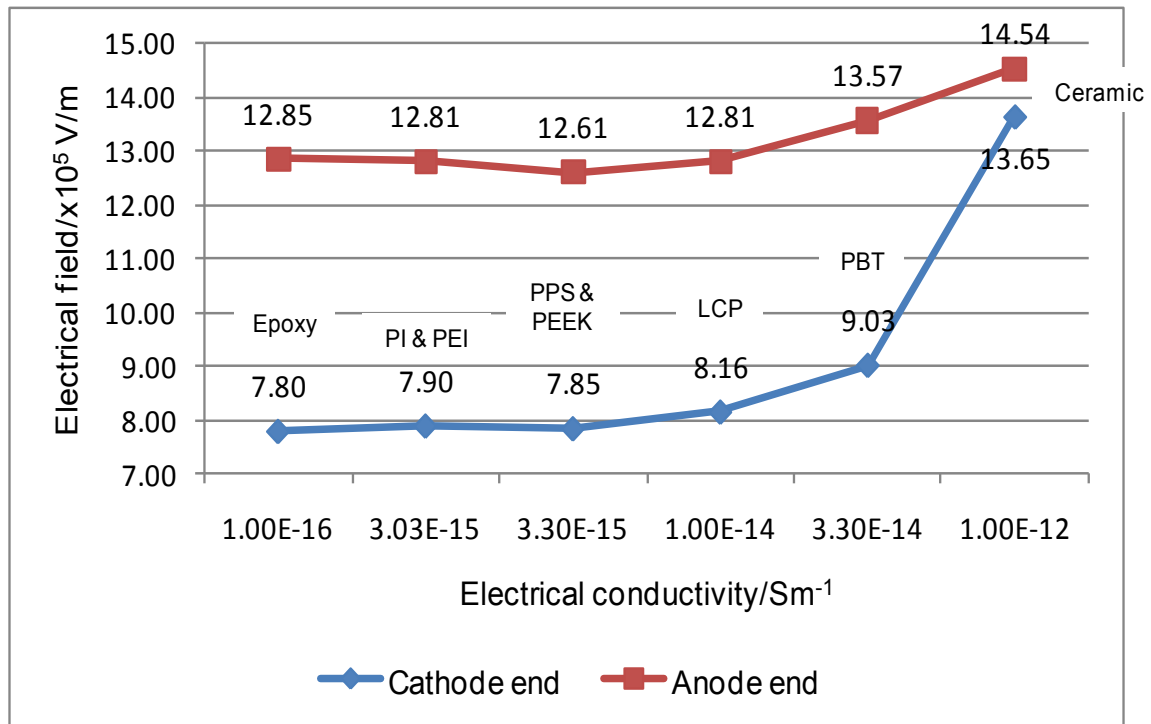
**Table 6.2: Electrical conductivities of candidate polymers for the housing**

A comparison of the electrical field magnitude at the cathode and anode contact regions when the different polymer candidates and ceramic material are studied and the housing cavity is comprised of silicone gel, is illustrated in Figure 6.12; whilst Figure 6.13 also illustrates the variation of the electrical field strength at the interface region as a result of change in the electrical conductivity of the housing material. From the plot, the electrical fields in the interface regions are seen to remain predominantly constant when the electrical conductivity of the polymer housing is varied - with only PBT and

epoxy yielding slightly higher than values than the rest. Compared to the polymer housings, higher electric fields magnitudes were actually observed at the cathode and anode ends of the ceramic housing. Together with this, the difference in the cathode and anode ends electric field magnitude were also noticed to lower in the ceramic housing than that in the polymeric packages. This comparatively higher electrical field magnitude was due to the electrical conductivity values of the housing cavity content (silicone gel in this case) and that of the package material. In the case of the polymer housings whose electrical conductivities are lower than that of the silicone gel ( $\sigma_{\text{silicone gel}} = 1 \times 10^{-13} \text{ S/m}$ ), the difference in the electric field magnitudes at the cathode and anode ends were seen to be significantly larger than in the ceramic housing. For the ceramic housing whose electrical conductivity ( $\sigma_{\text{ceramic}} = 1 \times 10^{-12} \text{ S/m}$ ) is higher than that of the silicone gel, the difference between the cathode and anode end electric field magnitudes was observed to be lower.

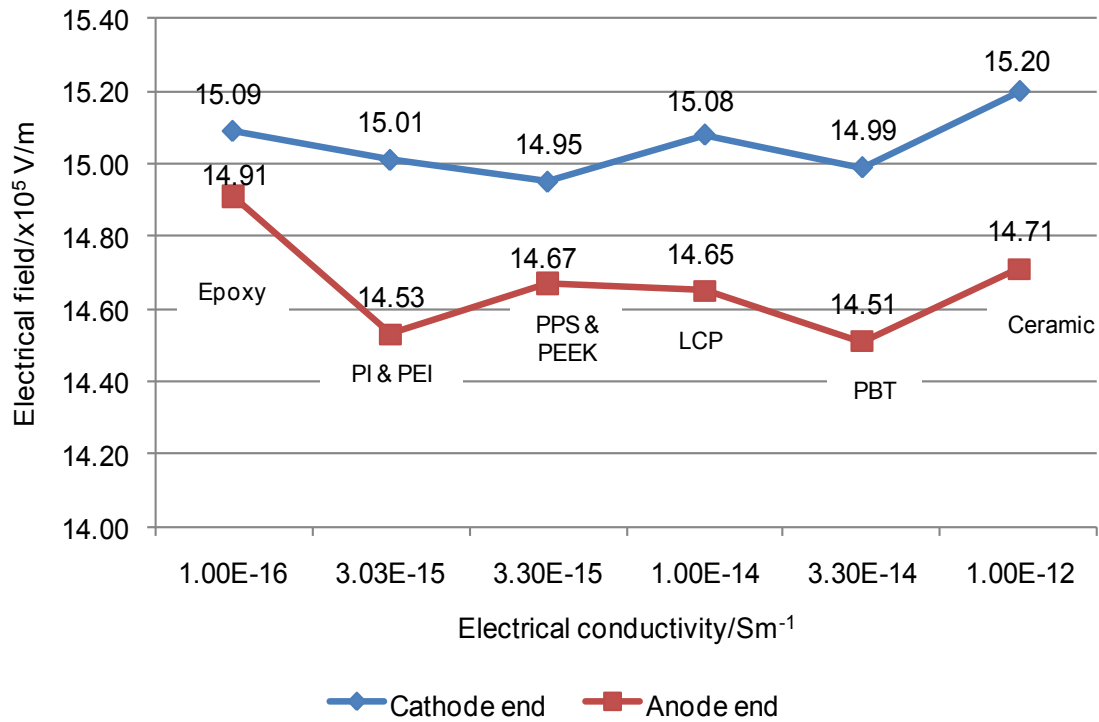


**Figure 6.12: Comparison of electric field magnitude at cathode and anode ends as a result**



**Figure 6.13: Study of the electric field variation trend as a result of change in the electrical conductivity of the housing (silicone gel present in housing cavity)**

The electric field variation when dry nitrogen (instead of silicone gel) is present inside the housing cavity is also shown in Figure 6.14. As can be seen in the graph, when the different polymer candidates were studied, the variation of the field magnitude were also observed to be predominantly constant. This suggests changing the electrical conductivity of the housing material does not have a significant influence on the magnitude of the electric field strength within. As observed in the case when the housing cavity is comprised of silicone gel and the package made of ceramic material (Figures 6.12 and 6.13), because the electrical conductivities of the housing materials studied herein were also higher than that dry nitrogen present in the housing cavity, the difference between the electrical field magnitude at the cathode and anode ends was also not observed to be significant.



**Figure 6.14: Variation of electric field at cathode and anode interface end when housing electric conductivity is changed (dry nitrogen present in housing cavity)**

## 6.5 AC simulations

During service, the polymer housing is likely to experience temperature changes due to heat that is dissipated from different sources, e.g. the silicon wafer, and as highlighted earlier in the chapter due to dielectric losses when an AC voltage is applied across the thyristor device. Most of the heat generated within the device will then be extracted by liquid-cooled aluminium heat sinks mounted on both the anode and cathode ends pole pieces, whereby the coolant inlet temperature is maintained between 20 °C and 50 °C with occasional rises to 60 °C (Woodhouse, 2007a). Some convective heat losses from the package to the surrounding air may also occur. The occurrence of significant temperature gradients within the housing can be anticipated to lead to the delamination between the flange and housing, deterioration of the polymer material of the housing, and to subsequently cause failure of the thyristor during operation. Thus, a study of temperature changes that the polymer package is likely to experience in operation from the



different heat sources is important. In this project, prediction of the heat dissipated from the silicon wafer has not been achieved. It can be investigated when the polymer-based thyristor is fitted with an appropriate silicon wafer and then experimentally tested. However, prediction of the temperature changes within the housing due to dielectric losses arising from AC voltages and its harmonics together with the effect of different boundary conditions influencing the convective losses, has been investigated using FEA, and are discussed next.

To predict the temperature changes due to dielectric losses in the polymer package, a time-varying 8.5 kV voltage was applied between the cathode and anode pole pieces of the same device used for the DC simulation and having silicone gel within its cavity. The electrical properties used for the subdomain components of the FE model are as listed in Table 6.3. The molybdenum discs and copper parts (pole pieces and flanges) were here taken to be purely conductive components and only their electrical conductivity was defined, while the other subdomains of the FE model were treated as lossy dielectrics having a lossless ideal capacitor connected in series with a resistive component. Their electrical conductivity and relative permittivity properties were hence defined for the AC modelling studies, and were kept constant irrespective of any variation in the frequency. For instance the silicone gel was taken to have an electric conductivity of  $1 \times 10^{-13}$  S/m and a dielectric constant of 3.2. For the selected glass-filled polyimide polymer grade for the housing, the relative permittivity values were based on technical data obtained from the polymer supplier, DuPont™. According to DuPont™, the relative permittivity for the glass-filled polyimide is 3.8 for frequencies below 1 MHz, and for 1 MHz and above the relative permittivity is 3.7, while its dissipation factor was 0.0012 for frequencies less than 1 kHz. The polyimide conductivity at different frequencies was calculated using equation 6.6. The resulting temperature gradient due to the AC losses was calculated using the thermal conductivity values also listed in the table.

FE model subdomains	Electrical conductivity/ $\text{Sm}^{-1}$	Relative permittivity	Thermal conductivity/ $\text{Wm}^{-1}\text{K}^{-1}$
Copper flange and pole pieces	$5.92 \times 10^7$		400
Molybdenum discs	$1.87 \times 10^7$		138
Silicon wafer (Depletion region)	$1 \times 10^{-16}$	12	148
Glass-filled polyimide	<i>Calculated using equation 6.6</i>	3.8 ( $f < 1 \text{ MHz}$ ) 3.7 ( $f > 1 \text{ MHz}$ )	0.34
Silicone rubber	$2 \times 10^{-15}$	3.2	0.22
Silicone Gel	$1 \times 10^{-13}$	2.86	2.45

**Table 6.3: Electrical properties of subdomains used for AC modelling studies**

In practice, the temperature gradients within the package due to the convective heat loss are likely to be influenced by three key boundary condition parameters namely: (1) the temperature of the ambient air around the device ( $T_{\text{surrounding}}$ ), (2) the heat transfer coefficient,  $h$ , and (3) the temperature of the cooling fluids flowing in the heat sink ( $T_{\text{pole piece}}$ ), as illustrated in Figure 6.15. Because exact values of the different parameters the thyristor is likely to encounter in normal service are unknown at this stage, different heat loss scenarios have been investigated to predict the likely temperature gradient within the package, and study the influence of the individual boundary parameters.

In operation, when the AC voltage will be applied across the device, the periodic waveform will be complex comprising of a fundamental 50/60 Hz frequency (Woodhouse, 2007a), and also multiple harmonics frequency components. In case the applied voltage contains substantial harmonic frequency elements, it can lead to unsatisfactory operation and failure of the device. To account for the effect of harmonics, the housing performance was investigated when a 50 Hz, 8.5 kV half-cycle sine wave voltage was applied between the copper pole pieces. Together with the fundamental 50 Hz frequency element of the applied voltage, the influence of its harmonic

components on the power loss and resulting temperature gradients across the housing was also studied. For this study, the FE model used was assumed to be surrounded by ambient air at 298 K (25 °C) so that the temperature change due to the dielectric heat losses could be studied. These are discussed in section 6.5.1.1. On the other hand, the influence of the heat transfer coefficient,  $h$ , and the copper pole piece temperature,  $T_{pole\ piece}$ , are reviewed in section 6.5.1.2.

As highlighted earlier, because the convective heat loss process is influenced by the pole piece temperature, its effect on the temperature distribution in the housing was also studied through three case studies namely CS1, CS2 and CS3. In CS1, the temperature change across the package was studied while assuming the device was surrounded by 298 K ambient temperature and the heat due to the dielectric loss of the polymer was dissipated due to the natural convection process. In CS2 and CS3, the pole piece temperature,  $T_{pole\ piece}$ , were taken to be 308 K (35 °C) and 298 K (25 °C) respectively, while keeping the ambient air temperature,  $T_{surrounding}$ , and the heat transfer coefficient,  $h$ , respectively constant at 298 K (25 °C) and 10 W/m<sup>2</sup>K.

Together with these, the influence of the heat transfer coefficient,  $h$ , was also studied while keeping the temperature values  $T_{surrounding}$  and  $T_{pole\ piece}$  constant at 298 K and 308 K respectively. The heat transfer coefficient,  $h$ , depends on different variables, e.g. surface geometry, nature of fluid motion, properties of fluid and bulk fluid velocity, and typical values vary between 2 W/m<sup>2</sup>K and 25 W/m<sup>2</sup>K under ambient atmospheric conditions (Cengel, 2003). For this study, because an exact heat transfer coefficient value that the thyristor will encounter in practice could not be quantified,  $h$  was varied between 2 W/m<sup>2</sup>K and 25 W/m<sup>2</sup>K to simulate the range of potential heat loss scenarios.

For the different AC simulation-based studies, the FE model depicted in Figure 6.15 was used. As highlighted in section 5.3.1, because a sequential electrical-thermal finite element simulation approach was used to investigate the AC voltage influence on the dielectric heat loss in the housing, both electrical and convective heat loss boundary conditions were required to be

defined before computation. For the AC electrical simulation, the different boundaries were as defined for the DC study (Section 6.3). For the device to be modelled as a 2D axisymmetric model, edges 1-2, 2-3 and 3-4 were defined as axial symmetry boundary. Exterior edges 1-6, 6-5 and 5-4 were taken as insulation boundaries so that no current flows across them; whilst the rest of the edges inside the device and along its exterior surface 7-8, 8-9 and 9-10 were defined as continuity to ensure the current flowing across them is continuous. On the other hand, an 8.5 kV AC voltage was applied across the 'top' edge 2-7 of the cathode pole piece, whilst the 'bottom' edge 3-10 of the anode pole piece was maintained at 0 V. For the convective heat loss study, the pole piece temperature,  $T_{pole\ piece}$ , were defined on edges 2-7 and 3-10 of the cathode and anode pole pieces respectively. Edges 1-2, 2-3 and 3-4 were again defined as axial symmetry boundary; whilst  $h$ , the heat transfer coefficient, was taken to be along edges 7-8, 8-9 and 9-10. Edges 1-6, 6-5 and 5-4 were defined as thermal insulation boundary conditions.

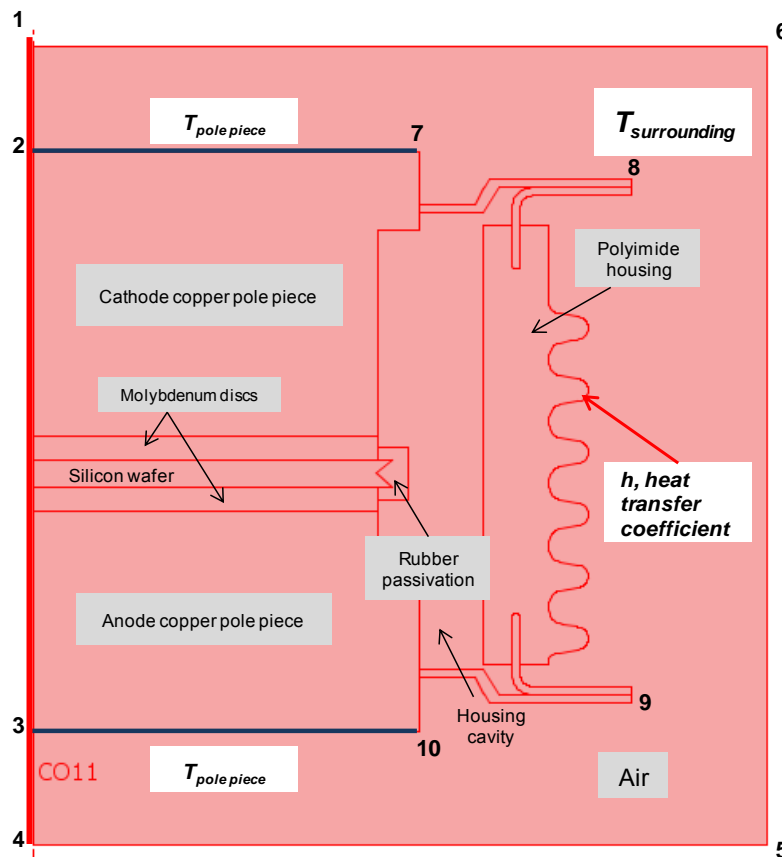
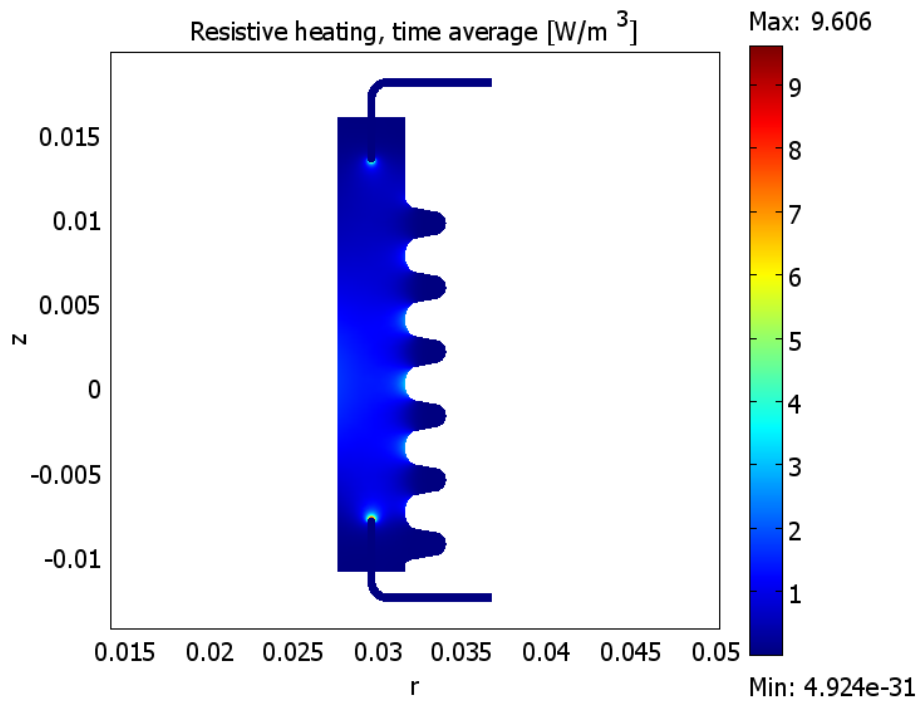


Figure 6.15: FE model boundaries used to study the AC voltage influence

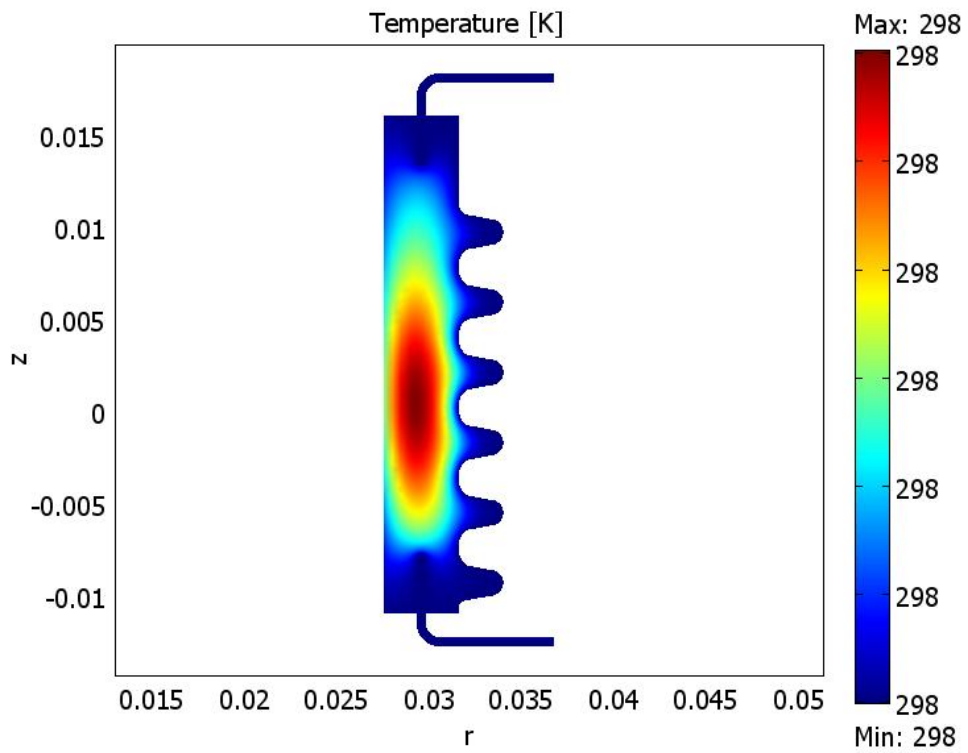
## **6.5.1 AC simulation results**

### **6.5.1.1 Influence of AC voltage and its harmonics**

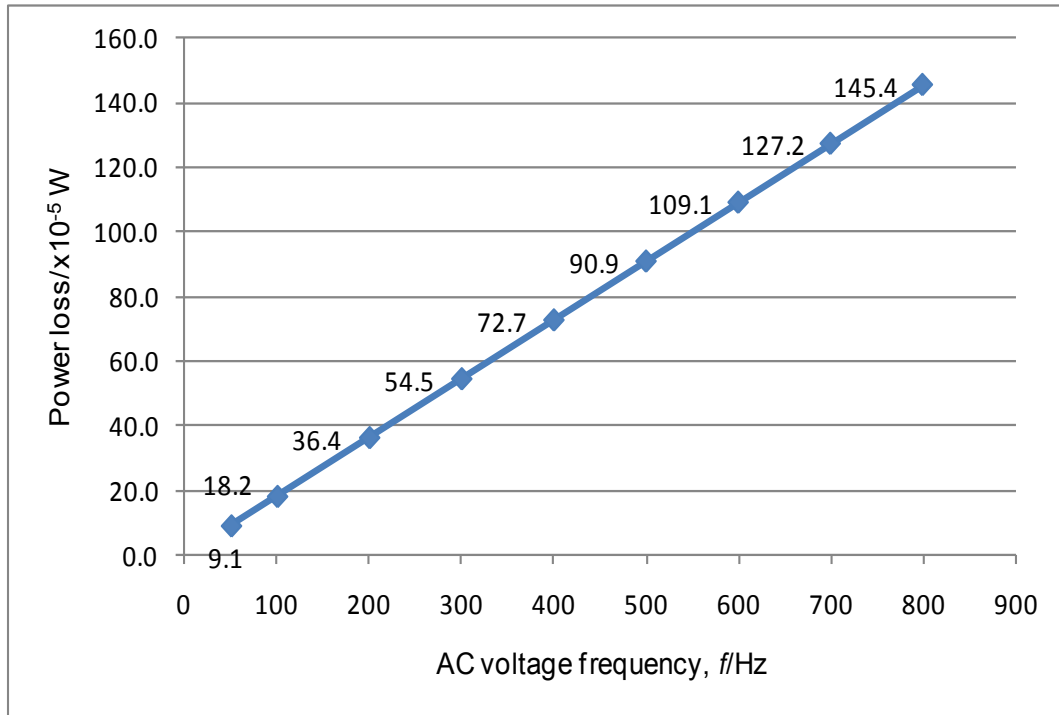
When a 50 Hz, 8.5 kV sinusoidal AC voltage was initially applied across the device, the electric field distribution in the package was found to be identical as in the case of an applied DC potential (Figure 6.10). An illustration of the contour plots depicting the power density and the resulting temperature gradient, as a result of the AC voltage, are shown in Figures 6.16 and 6.17 respectively. As shown, both the power density and resulting temperature gradient that occurred in the package was observed to be very low. The total dielectric loss within the package was calculated to be  $9.088 \times 10^{-5}$  W. The power dissipation in the package was however observed to increase as the frequency of the applied voltage was raised. The variation of the power loss as a result of the frequency change can be seen in Figure 6.18 whereby the total dielectric loss in the housing can be observed to increase linearly as the frequency increases from 50 Hz to 800 Hz whilst maintaining a fixed voltage. However in operation the magnitude of the higher frequency components of the voltage waveform are likely to be small in relation to the operating voltage and an evaluation of the total power loss in the dielectric requires knowledge of both the frequencies and magnitudes of these components.



**Figure 6.16: Power density contour plot at a 50 Hz applied frequency**



**Figure 6.17: Contour plot of temperature distribution within package (Applied frequency,  $f = 50$  Hz)**



**Figure 6.18: Variation of the power loss with applied AC voltage frequency**

In normal operation the thyristors will conduct for half the cycle, during which the voltage will be small, and block for the other half cycle so the overall voltage waveform will approximate a half-sinusoid. Fourier analysis provides a method to resolve such a waveform into its different harmonic components. When the harmonic components of the half-sinusoid AC voltage (given by equation 6.1, where  $T$  is the time period) were considered, their contribution on the total power loss across the polymer housing was also found to be negligible as described next.

$$f(t) = \begin{cases} 8.5 \sin(2\pi t/T), & 0 \leq t < T/2 \\ 0, & T/2 \leq t < T \end{cases} \quad \text{Equation 6.7}$$

The Fourier series of a periodic function  $f(t)$  can be represented by an infinite sum of sine and/or cosine functions as shown in equation 6.8:

$$f(t) = a_0 + \sum_{k=1}^{\infty} [a_k \cos(k\omega_0 t) + b_k \sin(k\omega_0 t)] \quad \text{Equation 6.8}$$

where  $k$  is the integer sequence 1, 2, 3, ...,  $\omega_0 = 2\pi/T$  is the fundamental frequency of the periodic function  $f(t)$ , and  $k\omega_0$  is known as the  $k$ -th harmonic of  $f(t)$ . The  $a_0$ ,  $a_k$ , and  $b_k$ , which are the Fourier coefficients, are calculated using equations 6.9 to 6.11:

$$a_0 = \frac{1}{T} \int_{t_0}^{t_0+T} f(t) dt \quad \text{Equation 6.9}$$

$$a_k = \frac{2}{T} \int_{t_0}^{t_0+T} f(t) \cos(k\omega_0 t) dt \quad \text{Equation 6.10}$$

$$b_k = \frac{2}{T} \int_{t_0}^{t_0+T} f(t) \sin(k\omega_0 t) dt \quad \text{Equation 6.11}$$

The Fourier series for a half-cycle sine wave has been widely reported, e.g. in Smith, 1998, Suresh Kumar, 2009, and is given by equation 6.12, while its  $a_k$  and  $b_k$  coefficients can be calculated using equations 6.13 and 6.14 where  $A$  is the amplitude of the applied waveform (8.5 kV in this case).

$$f(t) = \frac{A}{\pi} + \frac{A}{2} \sin(\omega_0 t) - \frac{2A}{\pi} \sum_{k=2,4,6,\dots}^{\infty} \frac{\cos(n\omega_0 t)}{(k^2-1)} \quad \text{Equation 6.12}$$

$$a_k = \begin{cases} -\left(\frac{2A}{\pi}\right) \frac{1}{k^2-1}, & k = 2, 4, 6, \dots \\ 0, & k \text{ is odd} \end{cases} \quad \text{Equation 6.13}$$

$$b_k = \begin{cases} \frac{A}{2}, & k = 1 \\ 0, & k \geq 2 \end{cases} \quad \text{Equation 6.14}$$

The amplitude,  $c_k$ , of the  $k$ -th harmonic of such a periodic waveform is given by the square root of the sum of the squares of the Fourier coefficients,  $a_k$  and  $b_k$  (Equation 6.15), while the contribution to the dielectric heating power,  $P$ , from each frequency component in the waveform is calculated by summing the power in each frequency component (Equation 6.16), which is given by



the product of a scale factor,  $X_k$ , and square of the amplitude,  $c_k$ . In the case of the fundamental 50 Hz frequency, the scale factor,  $X_o$ , would then equal to dielectric loss across the housing at the fundamental frequency,  $P_{50Hz}$ , divided by the square of the waveform amplitude (Equation 6.17).

$$c_k = \sqrt{a^2 + b^2} \quad \text{Equation 6.15}$$

$$P = \sum_{k=-\infty}^{\infty} X_k \cdot |c_k|^2 \quad \text{Equation 6.16}$$

$$X_o = P_o / |c_o|^2 \quad \text{Equation 6.17}$$

For the half-cycle sine wave applied to the thyristor, because the voltage would be comprised of the 50 Hz fundamental frequency together with 2<sup>nd</sup>, 4<sup>th</sup>, 6<sup>th</sup> and other even number harmonics, the contribution of different harmonics in the waveform to the dielectric power loss in the housing,  $P_v$ , would then be:

$$P_v = P_{50Hz} + P_{100Hz} + P_{200Hz} + P_{300Hz} + \dots \quad \text{Equation 6.18}$$

where  $P_{50Hz}$  represents the power at the 50 Hz fundamental frequency, i.e. for a full sinusoidal wave having a 50 Hz frequency, whilst  $P_{100Hz}$ ,  $P_{200Hz}$  and  $P_{400Hz}$  are the power at the 2<sup>nd</sup> (100 Hz), 4<sup>th</sup> (200 Hz) and 6<sup>th</sup> (300 Hz) component. As depicted in equation 6.19, the power in the half-cycle sine waveform was determined by summing the power in each harmonic component. From Figure 6.18, because the power loss within the package was observed to increase linearly with the applied frequency, the power loss should the 2<sup>nd</sup>, 4<sup>th</sup> and 6<sup>th</sup> harmonics have a magnitude of 8.5 kV would be  $18.2 \times 10^{-5}$  W,  $36.4 \times 10^{-5}$  W and  $54.5 \times 10^{-5}$  W, a total of 12 times that of the fundamental frequency. However when these values are substituted in equation 6.18 to give equation 6.19, the increase in the power loss in the package due to the 2<sup>nd</sup>, 4<sup>th</sup> and 6<sup>th</sup> frequency components can be seen to be low (respectively represented by the 2<sup>nd</sup>, 3<sup>rd</sup> and 4<sup>th</sup> term in the equation). This

showed that the contribution of the different harmonics in a half-sinusoidal voltage waveform was low towards the total power loss in the package.

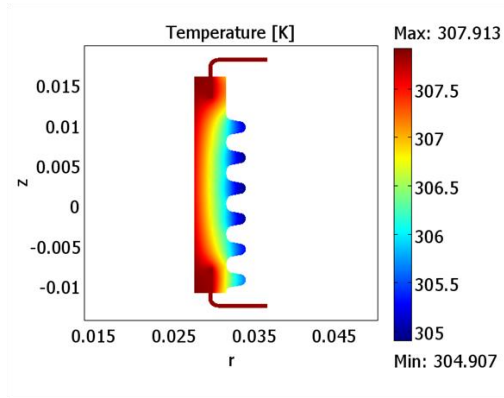
$$P_v = \left[ \left( \frac{A}{2} \right)^2 \right]_{50Hz} + \left[ \left( \frac{2A}{\pi} \times \sin(2\pi \times 100t) \right)^2 \right]_{100Hz} + \left[ \left( \frac{2A}{15\pi} \times \sin(2\pi \times 200t) \right)^2 \right]_{200Hz} + \left[ \left( \frac{2A}{35\pi} \times \sin(4\pi \times 300t) \right)^2 \right]_{300Hz} + \dots$$

**Equation 6.19**

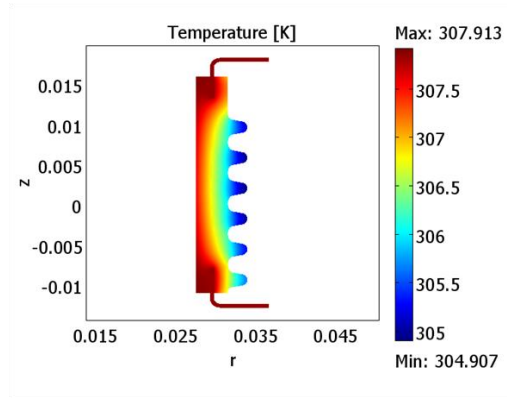
Areva have not provided details of the other transient voltage conditions the devices may see in service, but the above analysis suggests any dielectric losses associated with them are not likely to be significant. However the above approach could be applied if it was thought necessary to provide a quantative analysis in the future.

#### **6.5.1.2 Influence of copper pole piece temperature and heat transfer coefficient boundary conditions**

The temperature distribution within the package, when the copper pole piece temperature was varied, is shown in Figures 6.19 (a) and (b). The contour plot of the temperature gradient in the housing when the pole piece temperature is fixed at 35 °C (CS2) and 25 °C (CS3) are respectively depicted in Figures 6.19 (a) and (b) , while the temperature distribution in the housing when the heat loss across the device is due to the natural convection process is illustrated in Figure 6.17 (CS1). As seen from the different contour plots, because the temperature change across the various housings were observed to be low from the simulation studies, changes in the pole piece temperature were thus deduced to have negligible effect on the convective heat loss process from the package.



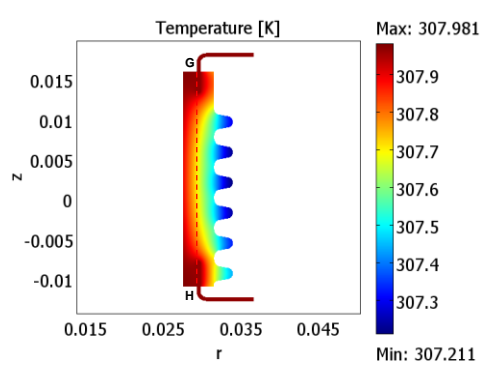
(a):  $T_{pole\ piece} = 35\ ^\circ\text{C}$  (CS2)



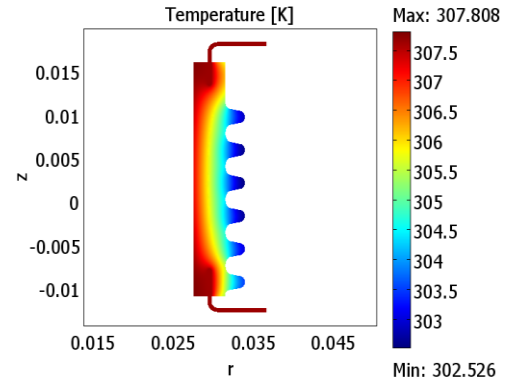
(b):  $T_{pole\ piece} = 25\ ^\circ\text{C}$  (CS3)

Figure 6.19: Temperature plot due to pole piece temperature variation

On the other hand, the temperature distribution within the package, when the heat transfer coefficient,  $h$ , was varied between  $2\ \text{W/m}^2\text{K}$  and  $25\ \text{W/m}^2\text{K}$ , are also shown in Figures 6.20 (a) and (b) respectively, while their variation between points G and H across the package is illustrated in Figure 6.21.

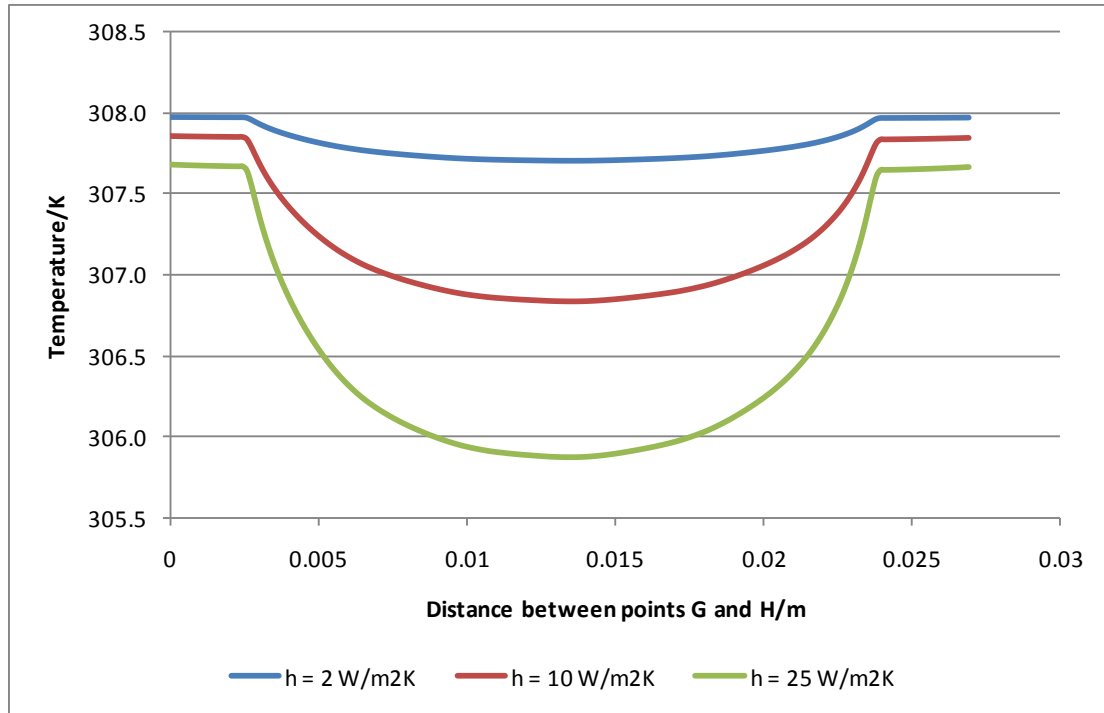


(a):  $h = 2\ \text{W/m}^2\text{K}$



(b)  $h = 25\ \text{W/m}^2\text{K}$

Figure 6.20: Temperature distribution within the housing when  $h$  is equal to (a)  $2\ \text{W/m}^2\text{K}$ , (b)  $25\ \text{W/m}^2\text{K}$  (applied frequency =  $50\ \text{Hz}$ )



**Figure 6.21: Comparison of temperature variation along path EF across package when heat transfer coefficient  $h$  is changed at an applied frequency of 50Hz**

As can be seen in Figure 6.21, the loss of electrically generated heat from the package was observed to increase, as the magnitude of the heat transfer coefficient value,  $h$ , was increased. However, because the temperature change within the package and the resulting risk of degradation were low, the influence of the heat transfer coefficient,  $h$ , on the convective heat loss from the package was also concluded to be negligible.

## 6.6 Discussion

In this chapter, an initial study focussed on the electrical behaviour of the polymer-based thyristor housing is discussed. The electrical performance of the package when DC and AC voltages are applied to the package has been studied to assist the 50 mm prototype development.

As seen in section 6.4, when a 10 kV DC voltage was applied across a preliminary design for a 50 mm housing device, the electrical field strength magnitude in the housing was observed to be less than the dielectric strength of the selected glass-filled polyimide polymer by a factor of  $10 \text{ Vm}^{-1}$ . This

suggested the risk of dielectric breakdown of a void-free polyimide housing was low even when a 10 kV DC voltage was applied between the pole pieces of the device. However localised regions of high electrical field strength magnitude were also noticed at the cathode and anode ends interface regions formed by the flange and polymer housing. Because such localised regions of high electrical stress can lead to partial discharge failure of the polymer housing (especially when there are delamination between flange and housing, or air void around the interface region), initial approaches were investigated to reduce the field magnitude and develop a reliable prototype. These initial studies focussed on varying the electrical conductivity of the housing material and the cavity formed between the housing and the stacked assembly of silicon wafer, molybdenum discs and copper pole pieces. The electrical conductivity of the polymer material of the housing was varied by considering the suitable polymer candidates identified by Ahmad, 2009 for the NEWTON device, while the influence of the internal housing cavity was studied by comparing the electrical performance of the package when either dry nitrogen or silicone gel is present inside it.

From the electrical simulation studies that were performed, different electrical field distributions were observed inside the housing when either dry nitrogen or silicone gel is present inside its cavity. Dry nitrogen in the housing cavity was observed to result in equal electric field strength magnitude at both the cathode and anode end flange/housing interface regions. The field values at these locations were actually higher than other areas in the package, but lower than the dielectric strength of the selected glass-filled polyimide polymer. On the other hand, when silicone gel is present, the electrical field strength magnitude at the cathode and anode ends interface regions were actually observed to be unequal. One reason this occurred was because the FE model used for this study was based on unequal anode and cathode copper pole piece thicknesses. The electric field magnitude, which was higher than other locations in the package, actually occurred at the anode end interface region, and was thus regarded as the most likely location where partial discharge failure could result. However although the distribution changed significantly, because the difference between the maximum electric

field values was considered to be insignificant when either dry nitrogen or silicone gel is present inside the housing cavity, changing the electrical conductivity of the housing cavity was regarded to have no major influence on the maximum electric field value the housing can experience when exposed to a DC potential.

On the other hand, when the housing electrical conductivity was varied (by comparing the performance of the different shortlisted polymer housing, together with that of a ceramic package), a similar observation was noticed. Irrespective of the housing cavity content, no significant change in the electric field strength magnitude was also observed when the polymer-based housings were studied. However, when the electrical behaviour of the polymer-based housings were compared again a ceramic housing that consisted of silicone gel inside its cavity, a higher electric field magnitude was observed at the cathode and anode interface region in the ceramic package. The difference between the interface field magnitudes was also seen to be lower than in the polymer housing whereby the electric field magnitude at the cathode contact region was significantly lower than at the anode end. Such an occurrence was due to the electrical conductivity values of the housing material and the fillers in the device cavity. When the housing was comprised of the different polymer materials whose electrical conductivities are lower than that of the silicone gel present in the internal cavity, the electric field magnitude at the anode interface tends to be higher than at the cathode. On the other hand, when ceramic material is instead used for the housing and silicone gel present in the device cavity, because the electrical conductivity of the ceramic material is higher than that of the silicone gel, the field magnitudes at the cathode and anode interfaces were observed to be more or less equal. As highlighted earlier in this section, a similar observation was also noticed when dry nitrogen, instead of silicone gel, was used as cavity fillers inside polymer-based housings (Figure 6.14). Because the electrical conductivities of the polymer materials were higher than that of the dry nitrogen filler, the difference between the electric field magnitude at the anode and cathode was not observed to be significant.

Because the DC simulation studies identified the occurrence of localised electric field regions at the flange/housing interfaces, and subsequent attempts to reduce their magnitude by varying the polymer housing material and its cavity conductivity were found to be insignificant, additional studies were thus planned to reduce the field magnitude and ensure a reliable prototype is developed. A review of the identified studies is described later in the section.

Together with the DC simulation studies, the action of a time-varying potential between the thyristor was also studied. Compared to the DC studies which aimed to see whether electric field strength magnitudes result in dielectric breakdown and partial discharge failures, since the AC voltages cause dielectric losses in polymer, the AC simulation experiments focussed on identifying changes in the electrical field intensity, power density, and the occurrence of any significant temperature gradient in the package. It should be noted the exact temperature changes the housing will experience in normal service could not be predicted through the different simulation studies. This is because the temperature changes the package would experience in normal service also depend on the heat loss from the silicon wafer. As the appropriate silicon wafer that can be used in the polymer-based prototype has not been identified at this stage of the project, quantification of the temperature change due to the heat loss from the wafer was not possible in this project. An electrical performance study when the package is exposed to a 50 Hz half sine wave AC voltage was thus carried. The resulting power loss due to the fundamental frequency and harmonic components of the AC waveform were also studied, together with the temperature changes due to the convective heat losses.

From the AC voltage study, when the 8.5 kV, 50 Hz voltage rating was applied, the electric field distribution and magnitude were noticed to be similar as when the housing was exposed to the static DC voltage. The field magnitude was less than the dielectric strength of the polyimide polymer, and localised regions of high electric stress were noticed at the flange/housing interfaces. When the AC voltage was applied, the power loss across the

package due to the fundamental and harmonic frequency components of the applied voltage waveform was seen to be low together with the resulting temperature gradient in the housing.

Additional studies about the convective heat losses and the influence of different parameters, such as the copper pole piece temperature and the heat transfer coefficient, were also performed to predict potential temperature gradient in the housing. From the different studies, when the copper pole piece temperature and the heat transfer coefficient were changed, the temperature rise in the housing was observed to be low. However, because the heat loss from the silicon wafer could not be predicted, the temperature rise the polymer housing may encounter in practice can be higher. Additional works will be needed in the future to determine the temperature changes more accurately. Nevertheless, these preliminary AC simulation studies also show that the resulting temperature gradients due to the AC voltage are unlikely to be influenced by boundary parameters, such as the heat transfer coefficient, temperature of the ambient air, that influence the convective heat loss.

As highlighted earlier from the DC simulation studies, because changing the electrical conductivity of the housing cavity and housing materials did not influence the electric field strength magnitude in the package, additional studies were thus carried to reduce the localised electric stresses at the flange and housing interfaces to develop the prototype housing. These are discussed next in Chapters 7 and 8. In Chapter 7, finite element modelling based studies are described to reduce the high electric field magnitude at the flange/housing interfaces by varying the design of the flange ends, while the influence of different geometrical design parameters, e.g. the wall thickness of the housing, the flange depth, etc, are described in Chapter 8 and compared with moulding simulation studies results from DuPont™ to determine the final 50 mm prototype housing design.



## **7 50 mm prototype development I: Flange end design**

### **7.1 Introduction**

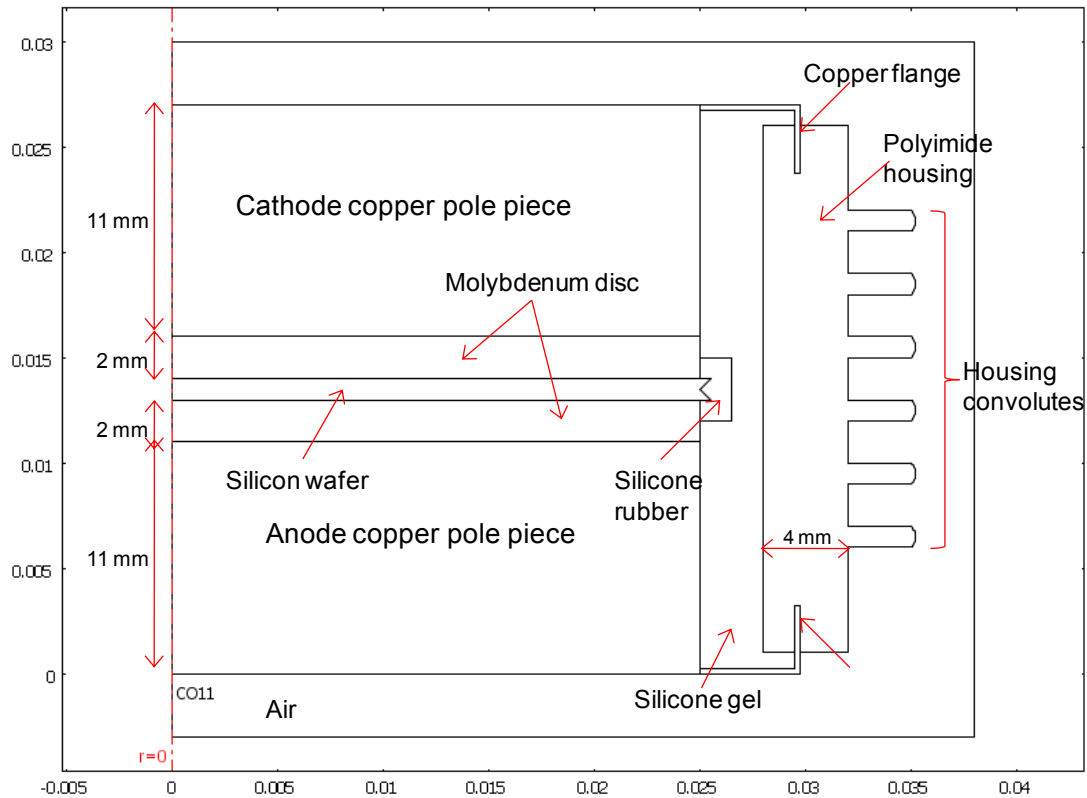
Based on the electrical studies of the polymer package described in Chapter 6, localised regions of high electric field strength were observed at the flange and housing interface regions at both the cathode and anode ends. Because such high electrical field regions are undesirable in high voltage applications and can result in the housing failure during normal service, attempts to reduce the electric field intensity at the contact regions were carried out and are described in this chapter.

From different studies, the shapes of electrodes that are in contact with insulators have been observed to influence the electric field occurring within. For example, Pillai et al., 1984 who calculated the electrical field distribution using the charge simulation technique at electrode-insulator interfaces having different designs in high voltage systems, and Guoqiang et al., 1999 who investigated the optimal design of high voltage bushing electrode in transformers, both found the electrical field magnitude at the electrode-insulator junction to vary as a result of change in the electrode shapes. To reduce the electric field strength magnitude at the contact regions in the polymer housing, the scope of modifying the shape of the flange end and investigating the resulting effect on the electrical behaviour of the polymer package was studied using the FEA technique. For this study, a range of different flange designs were initially investigated. Examples of some preliminary flange designs that were studied included a straight insert with a curved end, and inserts having circular and elliptical-shaped wire-edged geometries. Based on their electrical performance, a shortlist of some appropriate design concepts was then proposed for further studies. In these subsequent modelling studies, the flange dimensions were varied to investigate and compare the electric field magnitude around the interface region (described from section 7.2 onwards). The appropriate flange end

geometry was then identified from the electrical performance and ease of fabrication so that it could be used in the 50 mm prototype.

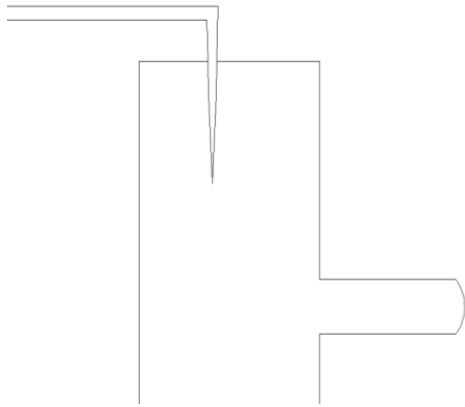
## **7.2 Electrical field variation around metal insert ends**

In this section, the results of a preliminary study to investigate the influence of different flange end designs on the electric field strength magnitude at the flange/housing contact regions are presented. This study was performed on a 2D axisymmetric model of a 50 mm diameter thyristor device shown in Figure 7.1. Compared to the 50 mm prototype configuration used in Chapter 6, in the device used for this study the copper flanges protruding inside the polyimide housing were welded directly to the outer circumference of the anode and cathode copper pole pieces. The housing was chosen to be comprised of the selected glass-filled polyimide polymer and consisted of 6 convolutes. As in Chapter 6, a 10 kV DC voltage was again applied between the copper pole pieces, and the electrical conductivities of the different components of the FE model were based on the values outlined in Table 6.1 of Chapter 6. Silicone gel was selected to be present inside the housing cavity, and the depth the flange protrudes inside the housing at both ends, and its position along the package were respectively kept constant at 2.3 mm and 1.5 mm for the different simulation studies to compare the performance of the different flange end designs.

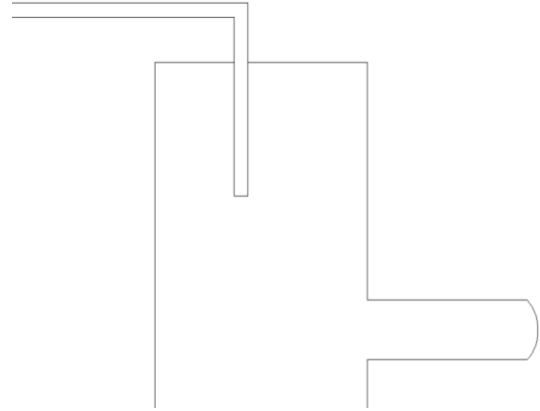


**Figure 7.1: 2D axisymmetric model of 50 mm diameter thyristor (6-convolutes configuration)**

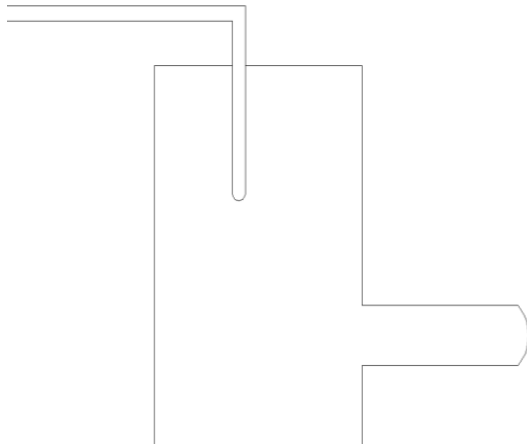
The flange ends that were investigated in this initial study are shown in Figure 7.2. Concept 1 (Figure 7.2 (a)) illustrates a straight point end flange, while concepts 2 and 3 in Figures 7.2 (b) and (c) respectively show other straight insert design variations. In concept 3, the straight flange end is curved (or rounded), compared to the 'flat' end of concept 2. To improve the mechanical strength of the flange/housing joint, flanges having a circular (concept 4) and an elliptical-shaped wire edged end (concept 5), shown respectively in Figures 7.2 (d) and (e), were also studied, together with a curved end flange profile. Two such designs are shown in Figures 7.2 (f) and (g), namely concepts 6 and 7 where the flanges are respectively bent outwards and inwards.



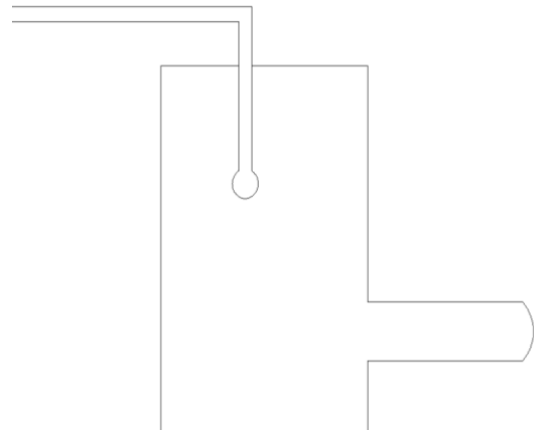
**(a): Concept 1 - Point end insert**



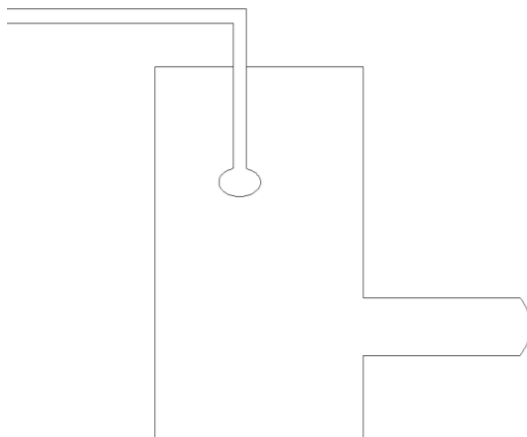
**(b): Concept 2 - Straight insert with a 'flat' end**



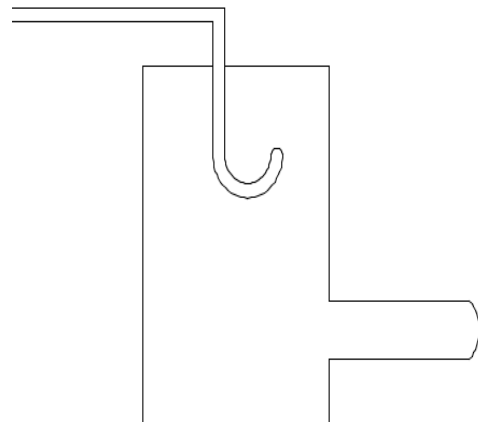
**(c): Concept 3 -Straight insert with a round end**



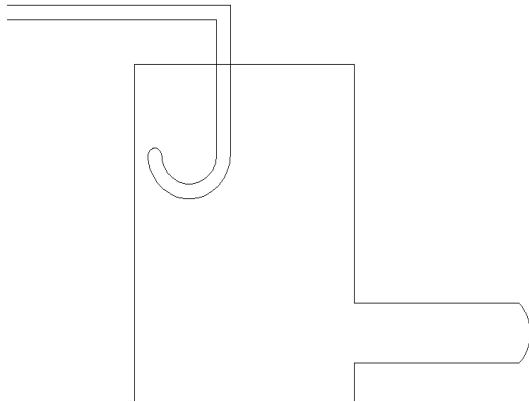
**(d): Concept 4 - Circular wire edged flange end**



**(e): Concept 5 - Elliptical wire edged flange end**



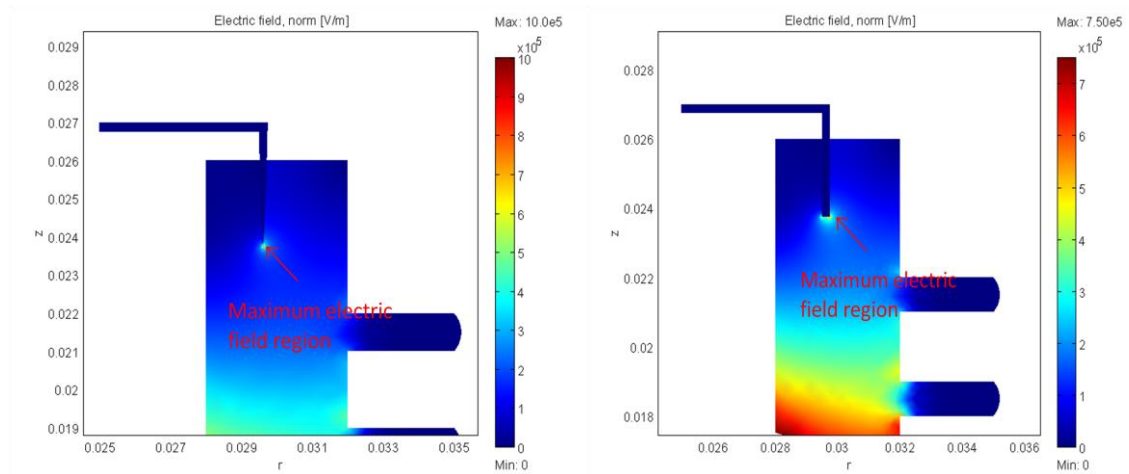
**(f): Concept 6 - Curved flange end (bent outwards)**



**(g): Concept 7 - Curved flange end (curved inwards)**

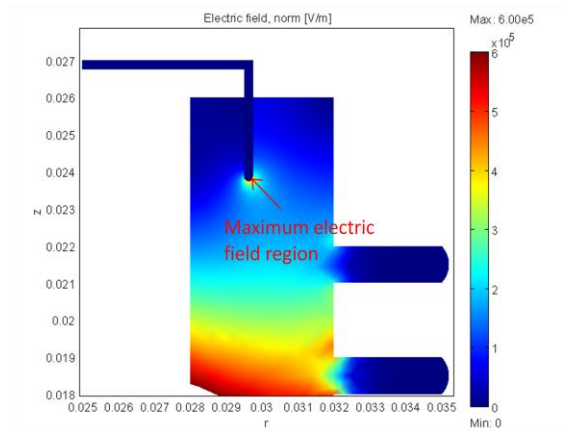
**Figure 7.2: Overview of preliminary flange end designs**

The electrical field contour plots depicting the electrical field distribution around the cathode end flange/housing interface region are illustrated in Figure 7.3, while a comparison of the maximum electrical field strength magnitude around the different flange designs is shown in Figure 7.4.

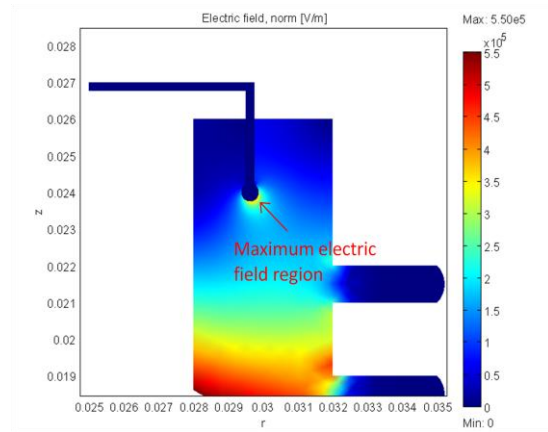


**(a): Point end insert**

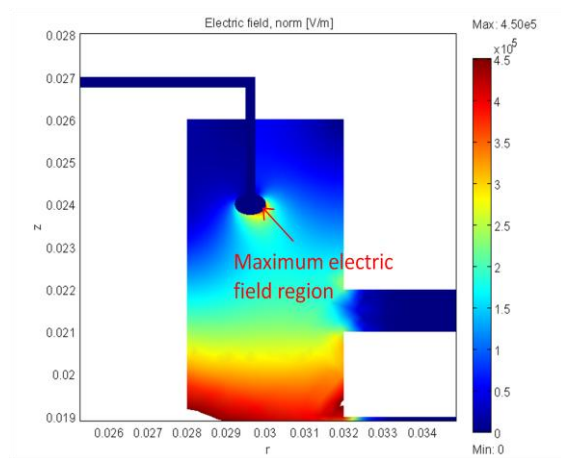
**(b): 'Flat' end straight flange**



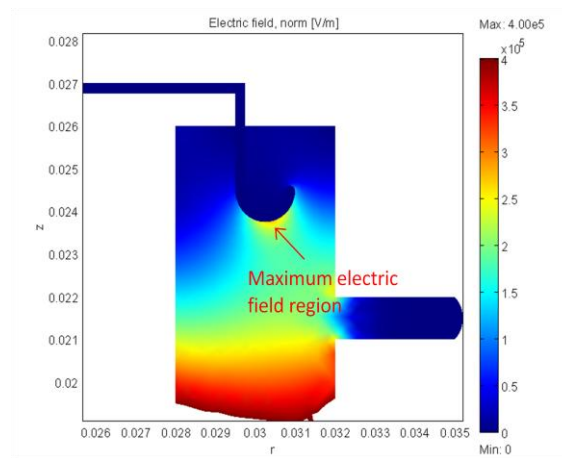
**(c): Round end straight flange**



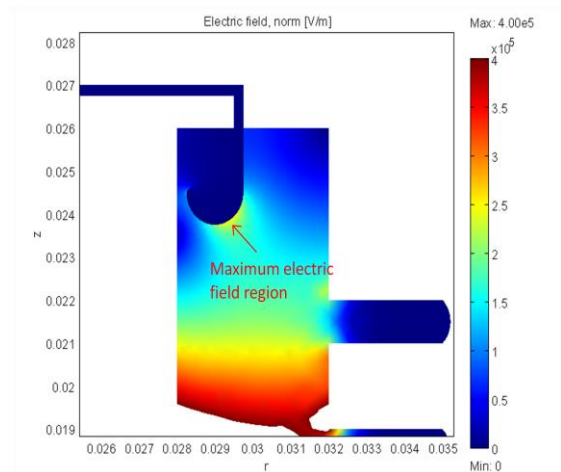
**(d): Circular wire-edged flange end**



**(e): Elliptical wire-edged flange**

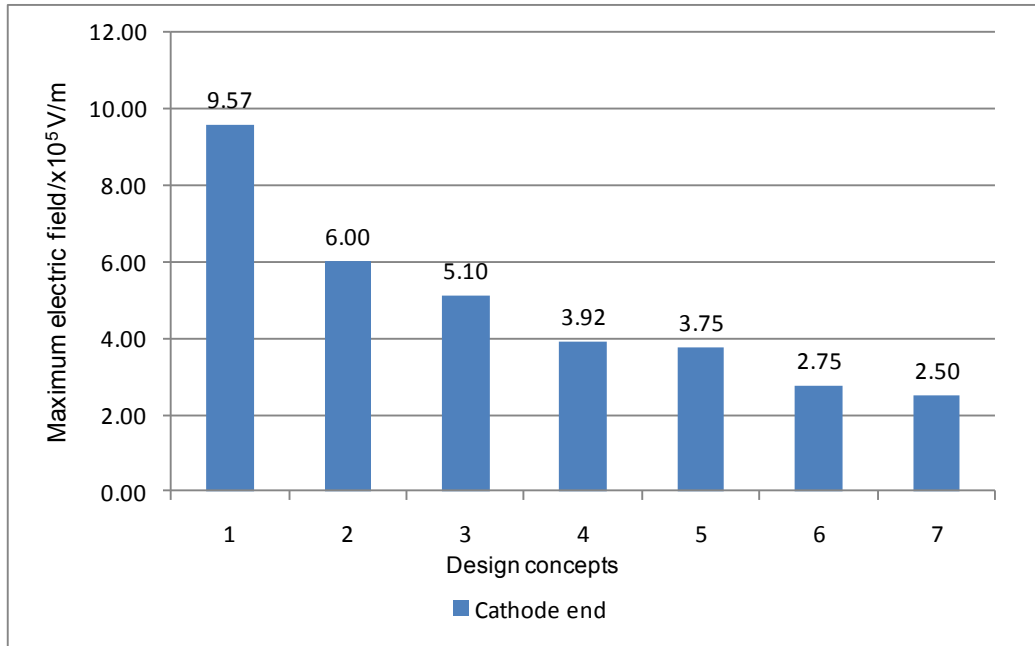


**(f): Curved flange end (bent outwards)**



**(g): Curved insert (bent inwards)**

**Figure 7.3: Electric field contour plots around the preliminary studied flange end designs**



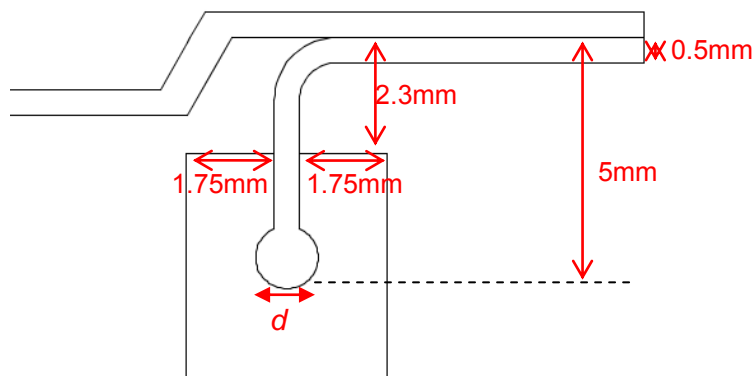
**Figure 7.4: Comparison of the maximum electric field magnitude at the contact regions of the different flange insert designs initially studied (Cathode end)**

As seen from the graph in Figure 7.4, because the surface charge density near sharp points are high (Gauthier, 1990), the highest electric field value was observed, as expected, to occur around the pointed end flange design (concept 1), whilst compared to the straight flange designs (concepts 3 & 4), lower electric field magnitudes were observed to occur around the circular, elliptical and curved flange end geometries (concepts 4 to 7).

Because these flange designs resulted in a lower electric field, additional simulation-based studies were performed to select the appropriate flange design for the 50 mm prototype. For these studies, the effect of the different flange end designs on the electric field magnitude at the cathode and anode end contact regions were again investigated and are described in sections 7.3 to 7.7. The electrical simulations were based on the 50 mm replacement prototype illustrated in Figure 6.2 (Chapter 6), where only the flange end designs were varied. A 10 kV DC voltage was again applied between the copper pole pieces, and the electrical conductivity values used to define the thyristor device component material properties were also according to values listed in Table 6.1.

### 7.3 Circular flange

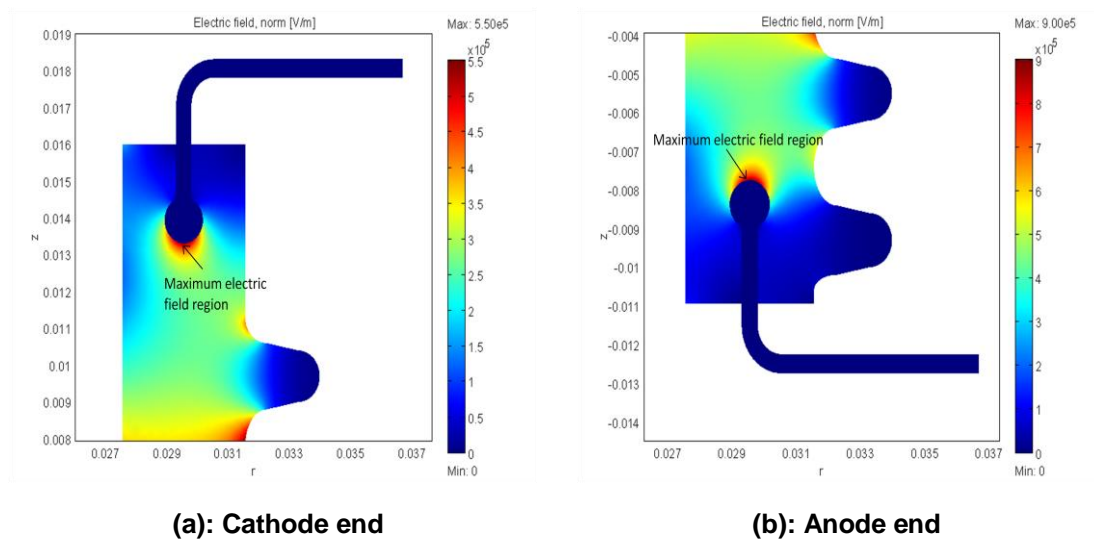
The electrical field variation at the cathode and anode end contact regions, as a function of the size of the circular wire edged flange end, is presented in this section, for which the layout of the circular flange inside the polyimide housing adopted is shown in Figure 7.5. As in the previous study, the flange thickness and depth inside the housing were taken to be 0.5 mm and 2.7 mm respectively, whilst its location along the housing was 1.75 mm from the inner and outer edges of the housing, i.e. it was located in the middle of the enclosure. The change in the electric field inside the housing was studied as the diameter,  $d$ , of the circular flange end was varied between 1.0 mm and 2.0 mm.



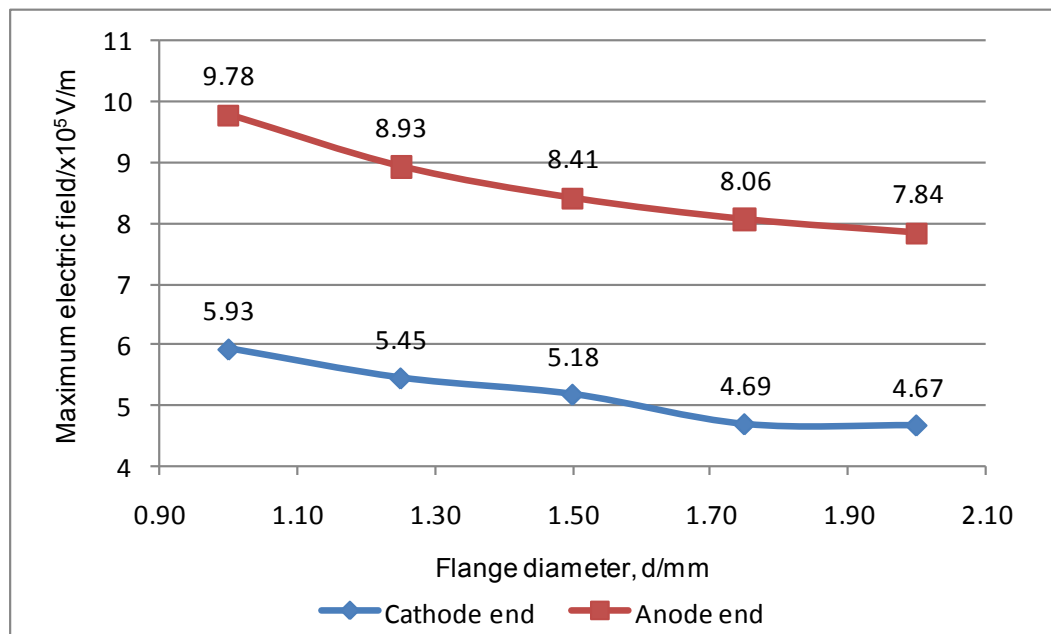
**Figure 7.5: Typical layout of the flange inside the polymer package**

Example of some typical electrical field contour plots at both the cathode and anode ends of a 1.25 mm diameter circular flange end are illustrated in Figures 7.6 (a) and (b) respectively, while the variation of the maximum electrical field strength at the interface region as a result of the diameter change,  $d$ , is shown in Figure 7.7.





**Figure 7.6: Contour plot of the electric field strength around a circular flange end of diameter,  $d$ , 1.25 mm**



**Figure 7.7: Variation of the maximum electrical field at the anode and cathode interface regions when the diameter,  $d$ , of the circular flange is changed**

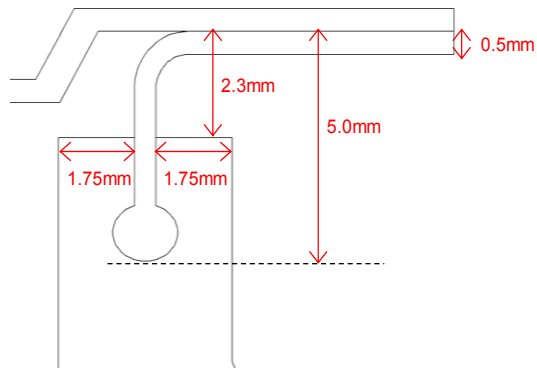
As seen in the electrical field plots when the flange end diameter is 1.25 mm, the maximum electrical field regions at both the cathode and anode ends were respectively observed to occur along the 'bottom' and 'top' surfaces of the curved regions. This location of the maximum electric field regions was also observed for other circular flange sizes. The maximum electrical field magnitude at the cathode end was actually seen to be lower than its

magnitude at the anode end. This was accounted to be due to the anode and cathode copper pole pieces having unequal thickness and the silicon wafer not located at an equal distance from the cathode and anode ends of the thyristor (i.e. not in the middle of the housing). When the circular flange diameter was also increased, as has been highlighted in different literatures, such as Dai, 2006, the maximum electrical field was herein also seen to decrease at both the cathode and anode ends (Figure 7.7). However, this electrical field variation with diameter was observed to be low at both ends of the package. For instance, for a 1 mm increase in the flange diameter the decrease in electrical field at the cathode end was around 126 V/mm for a 1 mm increase in flange diameter, while at the anode end the field decrease was 214 V/mm.

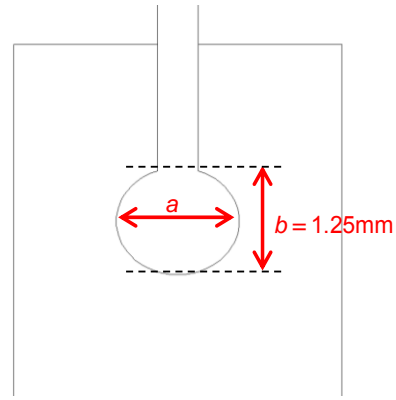
## **7.4 Elliptical flange**

Together with the circular flange variation, the effect of changing the size of the elliptical wire edged flange end on the electrical field strength at the contact regions was also investigated based on the initial 50 mm polyimide replacement thyristor device depicted in Chapter 6. The flange layout chosen for this study is as illustrated in Figure 7.8.

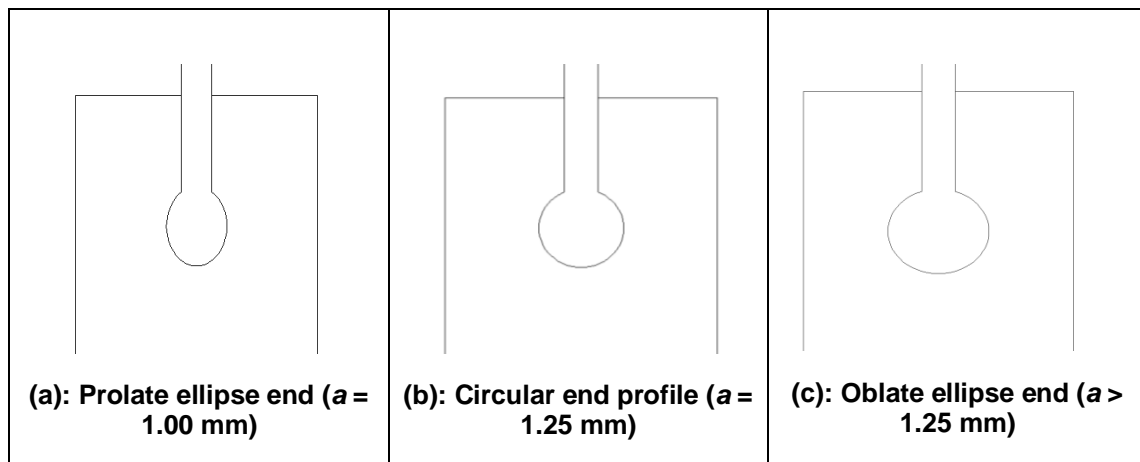
In this study, the vertical minor axis,  $b$ , of the ellipse profile was kept constant at 1.25 mm, while the dimension of the horizontal major axis,  $a$ , was varied between 1 mm and 2 mm (Figure 7.9). It should be noted when the dimension,  $a$ , of the flange changes, the shape of the ellipse geometry is also modified. The shape changes from a prolate ellipse to a circular end, and finally an oblate ellipse end, as the length of the major axis increases from 1 mm to 1.25 mm and then 1.50 mm onwards (as shown in Figures 7.10 (a) to (c)).



**Figure 7.8: Layout of the elliptical flange inside the polymer package**

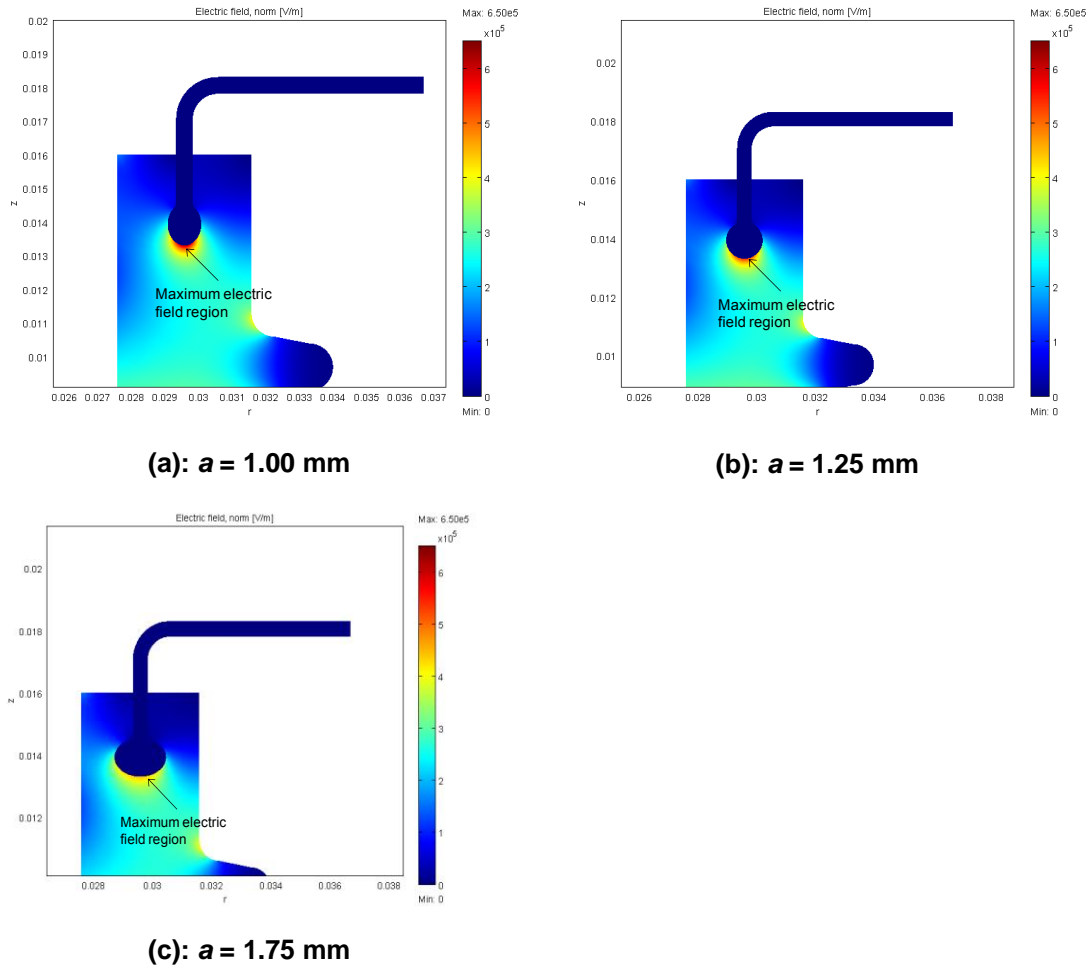


**Figure 7.9: Major and minor axis dimensions of the elliptical flange end**

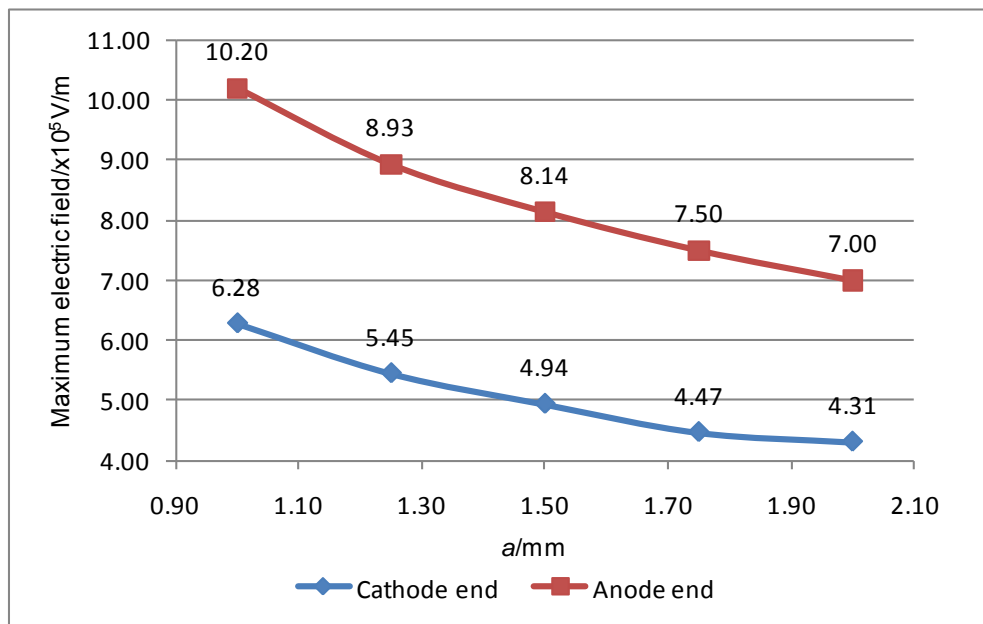


**Figure 7.10: Variation of the elliptical flange shape as a result of change in the major axis dimension**

The electric field distributions at the cathode end when the flange major axis,  $a$ , was respectively at 1 mm, 1.25 mm and 1.75 mm dimensions are shown in contour plots (a) to (c) in Figure 7.11, while the variation in the maximum electrical field at the cathode and anode ends due to the change in the horizontal major axis,  $a$ , dimension is illustrated in Figure 7.12.



**Figure 7.11: Contour plot of the electric field distribution around the cathode contact region when the major axis dimension,  $a$ , of the elliptical flange end is varied**

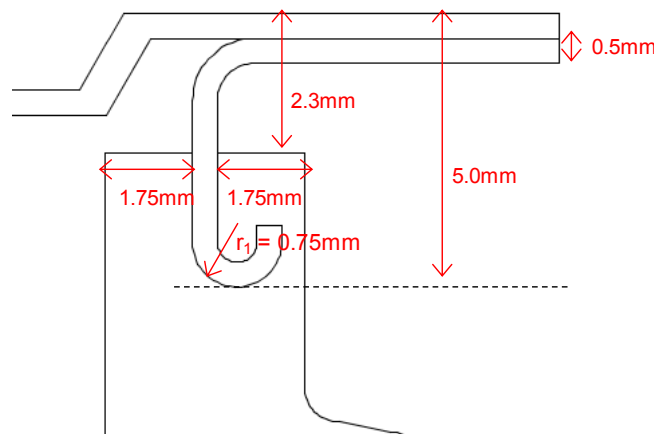


**Figure 7.12: Variation of the maximum electric field at the interface region due to change in the dimension of the elliptical flange major axis,  $a$**

When the elliptical flange sizes were varied, the maximum electric field region at the cathode end was observed to be predominantly located at the bottom region of the insert curvature (Figure 7.11), whilst at the anode end the maximum field region was at the top region of the elliptical flange curvature. As illustrated in Figure 7.12, the maximum electrical field was also seen to decrease at both the cathode and anode ends, when the length of the major axis,  $a$ , was increased with the minor axis dimension kept constant. As part of this study, the electric field around an oblate ellipse flange end design was also noticed to be lower than around a circular and a prolate ellipse end configuration - as shown by the electrical field contour plot in Figure 7.11 (c) which depicts an oblate ellipse flange and  $a$  is greater than 1.25 mm.

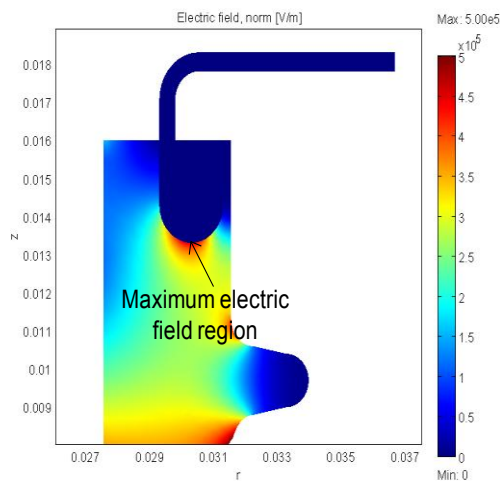
## 7.5 Curved flange

The change in the electric field magnitude around the curved flange end was also modelled using the 50 mm prototype (Figure 6.2). As shown in Figure 7.13, a 0.5 mm thick flange that was located in the middle of the 4.0 mm thick housing, and protruded to a 2.7 mm depth inside the housing was used for this study. The radius of curvature,  $r_1$ , of the flange was here modified between 0.7 mm and 1.1 mm to investigate the change in the electrical field magnitude at both the cathode and anode end contact regions.



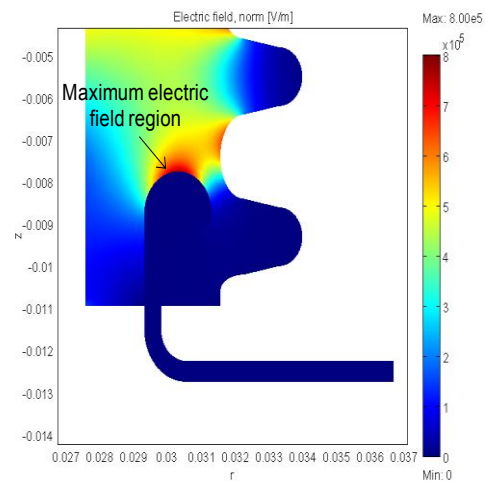
**Figure 7.13: Layout of the curved flange end inside the housing**

Examples of contour plots depicting the electrical field distribution around the cathode and anode ends of a 1 mm curved flange radius are illustrated in Figures 7.14 (a) and (b). As seen in both plots, the maximum electrical field regions were observed to occur along the curvature of the curved insert end, rather than the flange tip. When the radius of curvature was varied, this maximum field region was also seen to move at different points along the curvature.



Maximum electric field magnitude at  
cathode end =  $4.53 \times 10^5$  V/m

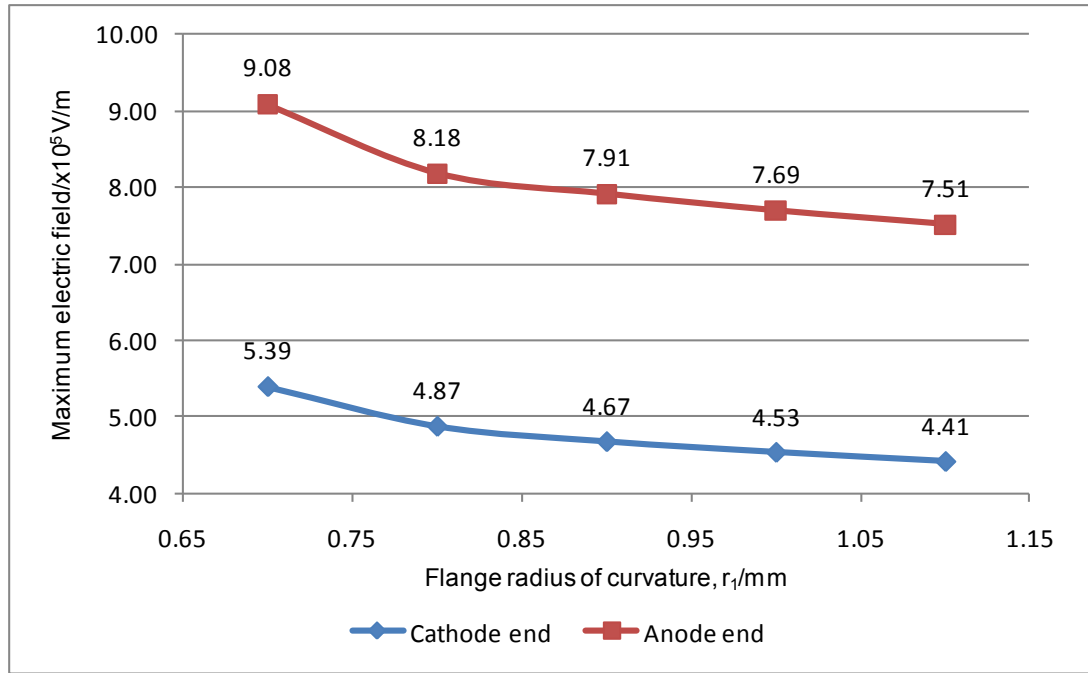
**(a): Cathode end electric field plot**



Maximum electric field magnitude  
(anode end) =  $7.69 \times 10^5$  V/m

**(b): Anode end electric field plot**

**Figure 7.14: Electric field plots around the cathode and anode ends of a 1 mm radius curved flange end**



**Figure 7.15: Variation of the maximum interfacial electric field magnitude when the flange bend radius,  $r_1$ , is changed**

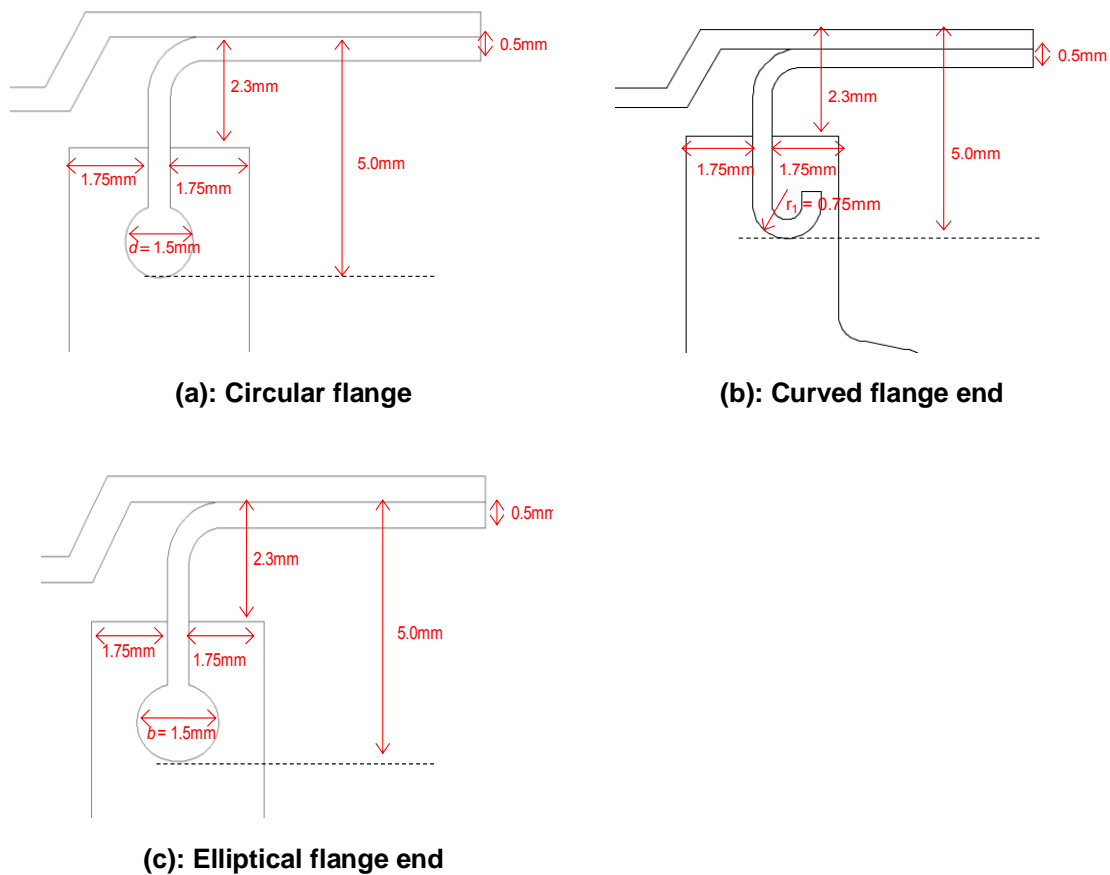
The variation of the maximum electrical field strength as a result of changes in the flange radius of curvature,  $r_1$ , is illustrated in Figure 7.15, where it can be seen the electric field magnitude decreases as the radius of curvature (or flange radius) increases. As in the case of the circular and elliptical shape flange ends, the change in electrical field values was here also observed to be low at both ends. For example, when the flange radius was varied between 0.80 mm and 1.10 mm, the decrease in electrical field magnitude was seen to be around 46 V/mm and 67 V/mm at the cathode and anode ends respectively.

## **7.6 Electric field comparison around circular, elliptical and curved flange end geometries**

Because the electric field magnitude variation was noticed to be low due to the dimensional changes of the circular, elliptical and curved flange ends, a comparative study based on the field magnitude was carried out to select the appropriate flange design for the 50 mm prototype. In this study, since the

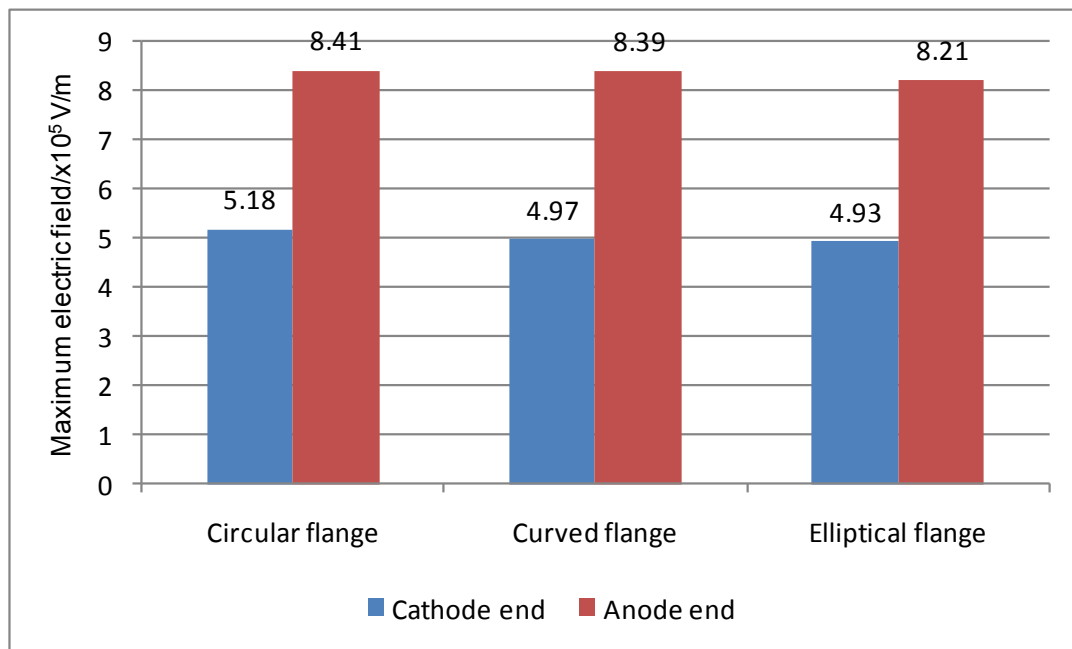
maximum electrical field region at the cathode and anode end of the different flange designs was respectively observed to occur along the ‘top’ and ‘bottom’ contour regions of the insert, flange ends, whose ‘horizontal’ axis dimension are equal and have the similar radius of curvatures (1.5 mm in this case), were selected and their performance studied using the 50 mm replacement housing.

As shown in Figure 7.16, the circular, elliptical and curved flanges chosen for the electrical performance study were each located at a 1.75 mm distance along the housing and at 2.7 mm depth inside the package. The circular flange end was chosen to have a diameter,  $d$ , of 1.5 mm; the radius of curvature,  $r_1$ , of the curved flange end was taken to be 0.75 mm; while the dimensions of the elliptical flange end was taken to be 1.5 mm and 1.25 mm along the horizontal major and vertical minor axes respectively. As illustrated, the ‘horizontal’ dimension in all three flange designs was 1.5 mm.



**Figure 7.16: Layout of the selected flange end designs inside the housing**





**Figure 7.17: Comparative plot of the maximum electric field magnitude at the interface region of the selected flange end designs**

The comparative plot depicting the maximum electrical field strength around the different flange profiles at the cathode and anode ends is illustrated in Figure 7.17. As shown in the plot, a lower electrical field was observed to occur around the elliptical-shaped flange end compared to that around the curved and circular wire-edged flange ends. However, the differences were relatively small and it was found that to manufacture either the elliptical or the circular wire-edged flange ends would be difficult and costly during the NEWTON project. As a result, the curved insert flange design that could be relatively easily manufactured was chosen to be developed for the 50 mm prototype.

## 7.7 Optimisation of the flange end design

Although using the curved flange design would provide electrical performance and manufacturing benefits, a major disadvantage of such an end geometry was the potential for voids to be formed around the inner curvature region of the insert during the moulding process, (Figure 7.18). As highlighted in

Chapter 3, presence of such air voids can lead to partial discharge failure of the polymer housing.

Occurrence of such voids in the package was considered to be likely due to two factors, namely the moulding parameters and the curved flange dimensions. In case of an inappropriate moulding condition and incorrect curved flange dimension, an inappropriate polymer flow would occur around the inner region of the insert (Figure 7.18) during the injection moulding process and lead to the unwanted void formation. To prevent this occurrence in the housing, different studies aiming to improve the design and dimension of the curved flange were performed and are described in this section. Two geometrical parameters of the flange, that were varied to improve the flange design and 'reduce' the curved profile of the insert end, were namely the vertical height,  $h$ , of the curved profile, and the curved length of the flange contour. Their influence on the electrical performance of the 50 mm package used in previous sections is discussed next.

### **7.7.1 Variation of vertical height, $h$ , of the curved flange**

The influence of varying the vertical height,  $h$ , of the flange on the electrical field magnitude at the flange/housing interface is here studied. To ensure the polymer flows properly around the curved end profile and void formation is prevented as a result of the moulding process, an insert with a reduced vertical height,  $h$ , is ideally preferred (Figure 7.18). For this study, the flange height,  $h$ , was varied between 1 mm and 2 mm, and its influence on the electrical field magnitude at the contact regions studied to determine the appropriate dimension of the vertical height. As shown in Figure 7.18, a flange layout, similar to those described in previous sections, was used for the present study, i.e. a 0.5 mm thick flange located in the middle of the housing and at a depth of 2.7 mm was considered.

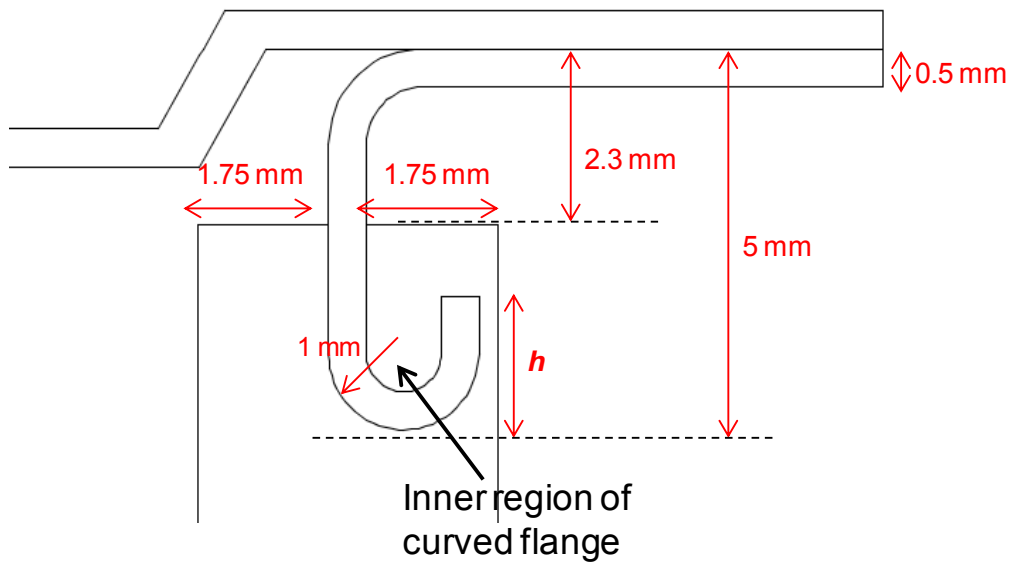


Figure 7.18: Illustration of the vertical height,  $h$ , parameter for the curved flange end

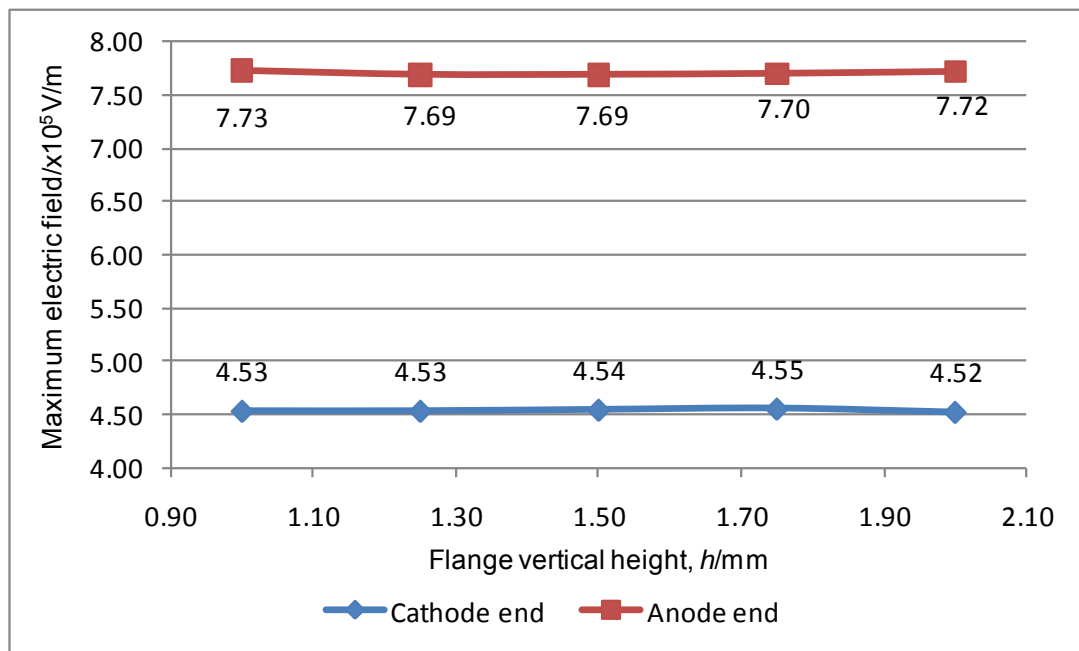


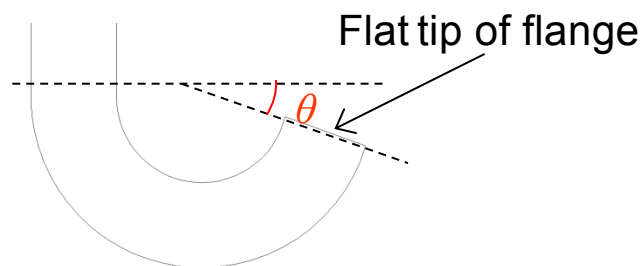
Figure 7.19: Variation of the maximum electrical field strength at the cathode and anode end contact as a result of change in the flange vertical height,  $h$

The variation of the electric field strength as a result of the change in the flange vertical height,  $h$ , at both the cathode and anode ends is illustrated in Figure 7.19. Because the radius of curvature of the flange was kept constant, the electrical field magnitude at the contact regions of both ends was seen to

remain almost constant as a result of the change in the flange vertical height. Because a reduced vertical height is desired so that the polymer can flow around the inner curve region of the flange and reduce the probability of void formation during moulding process, a vertical height of 1 mm was considered appropriate for the flange.

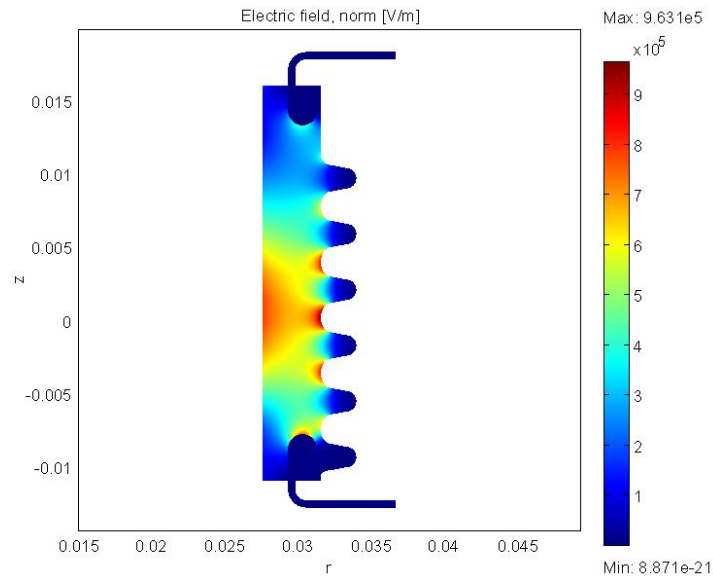
### 7.7.2 Contour length variation

To further improve the curved flange design and lower the electrical field magnitude in the housing, the influence of changing the contour length of the curved flange end was also studied. The angle  $\theta$ , shown in Figure 7.20, was varied between  $0^\circ$  and  $90^\circ$  to change the flange contour length. For instance, when  $\theta$  was  $0^\circ$ , the flange would have a fully curved profile with a vertical flange height of 1 mm (based on electrical simulation results in section 7.7.1), whilst the flange end would have a semi-curved profile when  $\theta$  would be equal to  $90^\circ$ .



**Figure 7.20: The ' $\theta$ ' parameter used to vary the flange contour length**

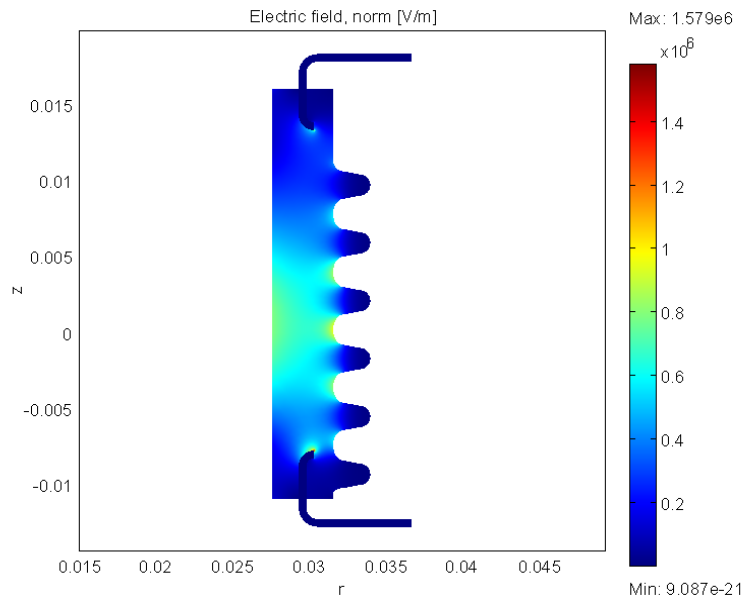
Figures 7.21 and 7.22 respectively show examples of contour plots of the electric field around the contact regions of  $20^\circ$  and  $90^\circ$  flange end profiles; while the variation of the electrical field strength magnitude at the cathode and anode end contact regions as a result of change in  $\theta$  angle parameter is depicted in Figure 7.23.



Maximum electric field magnitude at the anode end contact region =  $4.52 \times 10^5$  V/m

Magnitude of the maximum electric field at the cathode end contact region =  $7.70 \times 10^5$  V/m

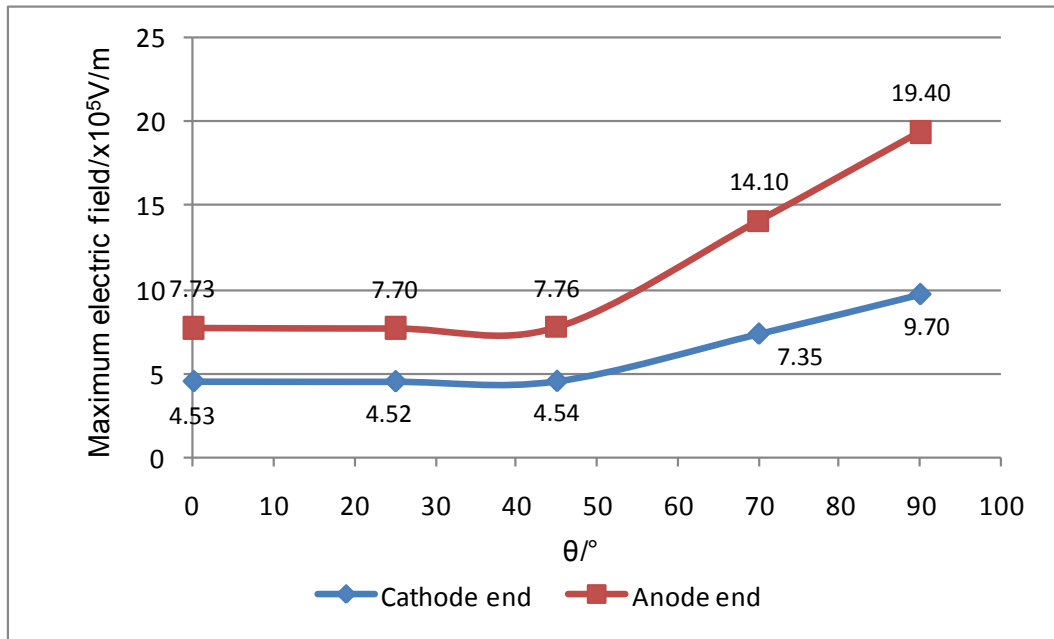
**Figure 7.21: Electric field distribution across the housing when the flange end profile,  $\theta$ , is  $20^\circ$**



Maximum electric field magnitude at the anode end contact region =  $9.70 \times 10^5$  V/m

Magnitude of the maximum electric field at the cathode end contact =  $19.40 \times 10^5$  V/m

**Figure 7.22: Electric field distribution across the package when  $\theta = 90^\circ$**



**Figure 7.23: Variation of the maximum electric field as a result of the flange contour angle  $\theta$**

As shown in Figure 7.23, the electrical field was seen to remain predominantly constant when  $\theta$  was less than or equal to  $45^\circ$ , whilst for  $\theta$  greater than  $45^\circ$  the field magnitude was observed to increase at both the cathode and anode ends. The higher electric field magnitude, when  $\theta$  was greater than  $45^\circ$ , was due to the maximum electric field region being located at the tip of the curved flange end rather than along the curved surface which was the case for angles less than  $45^\circ$ . Examples of some electric field contour plots at the interface region of flanges having  $45^\circ$  and  $70^\circ$  profiles are shown in Figures 7.24 (a) and (b) respectively. As can be seen, when  $\theta$  is equal to  $45^\circ$ , the maximum electrical field region was observed to occur along the curvature of the curved end, while for  $\theta$  greater than  $45^\circ$ , the maximum field region was located at the tip of the curved flange end. As highlighted earlier, because location of the maximum electric field region at a sharp end (as found at the curved profile tip) would act as an electrical stress raiser and lead to partial discharge failure of the housing, a flange end with a  $45^\circ$  profile was considered appropriate for the 50 mm prototype, and was thus fabricated. Together with the improved electrical performance benefit such a flange profile would provide is it would enable the appropriate polymer flow around

the inner curve region of the flange and reduce the likelihood of any void formation during the moulding process compared to a fully-curved flange end.

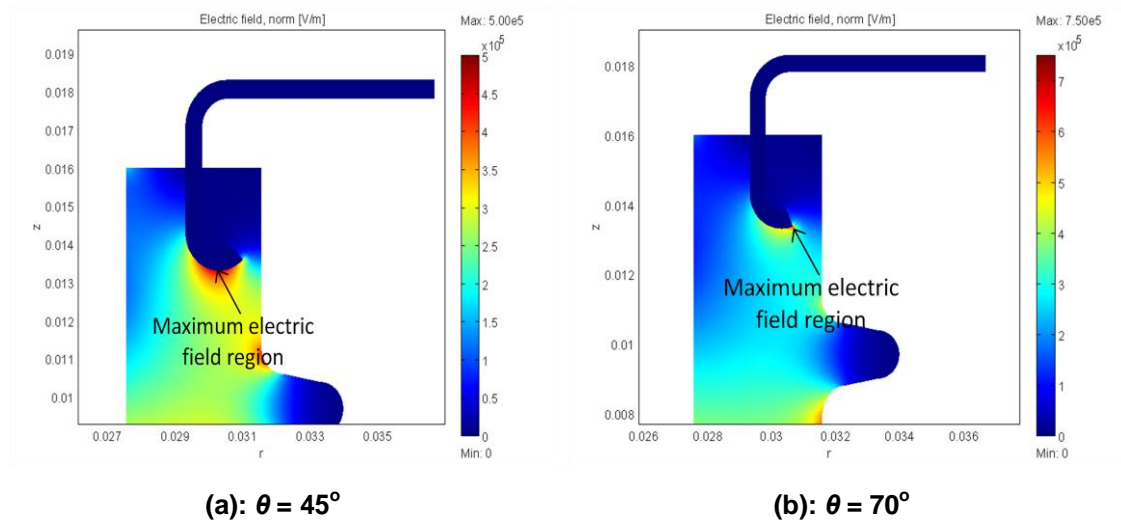


Figure 7.24: Electric field plot around flanges having 45° and 70° profiles

### 7.7.3 Flange tip design

To further reduce the electric field at the flange/housing interface region, the effect of rounding the tip of the curved flange was also investigated (as shown in Figure 7.25). To investigate any potential benefit this may bring, the electrical field magnitude at the interface region of 45° and 90° flange end profiles were compared under an applied 10 kV DC voltage.

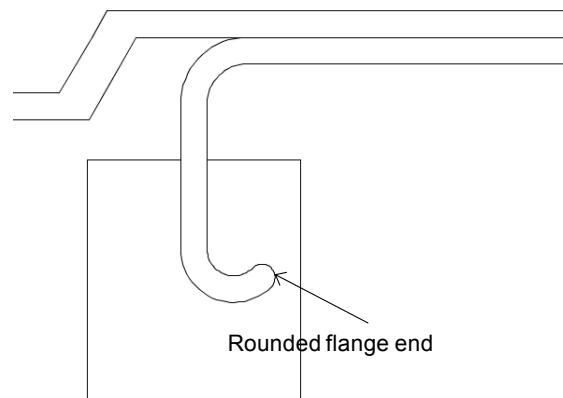
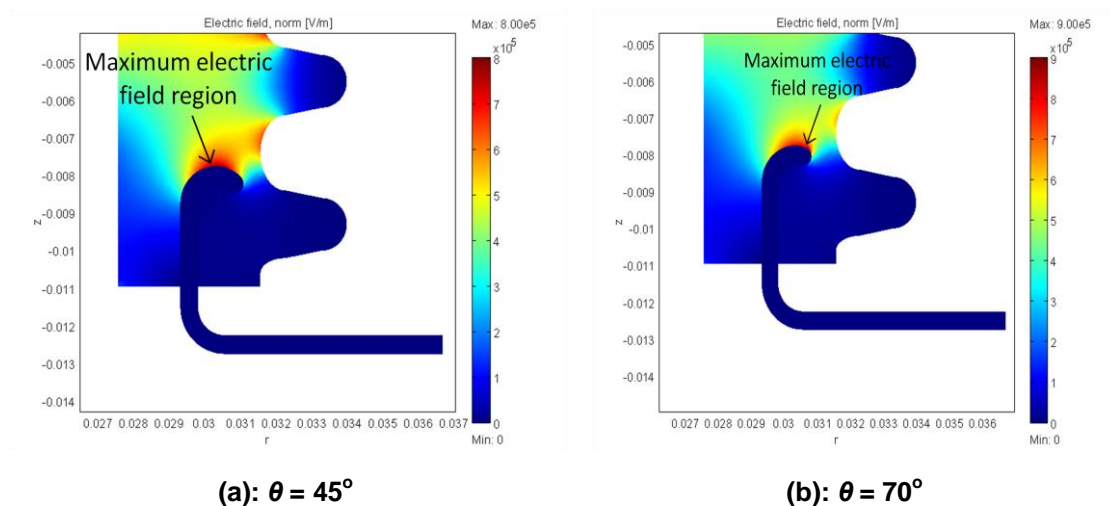
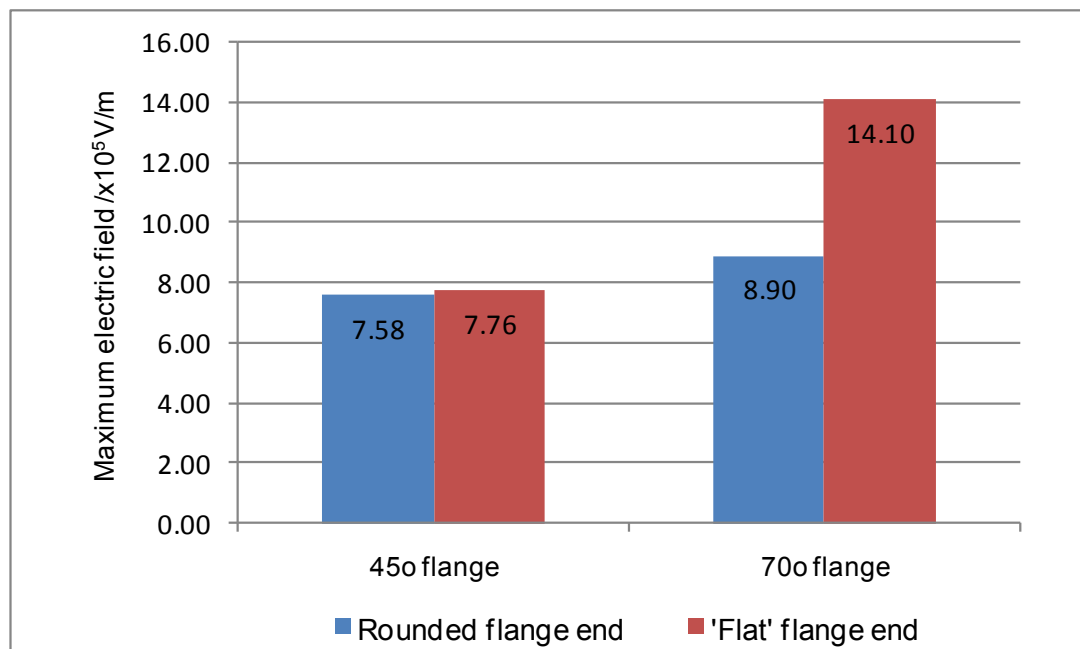


Figure 7.25: Example of a curved flange whose end (or tip) has been rounded

Contour plots illustrating the electrical field strength distribution around the anode end contact regions of 45° and 70° rounded end flange end profiles are shown in Figures 7.26 (a) and (b); while a comparison of the maximum electrical field values at the anode end contact regions of flanges, whose ends were either kept 'flat' (as shown in Figure 7.20) or rounded, is illustrated in Figure 7.27.



**Figure 7.26: Contour plots of electric fields around rounded end curved flanges**



**Figure 7.27: Comparison of the maximum electrical field strength magnitude at the anode end contact region of a curved flange having a 'flat' and a round end respectively**

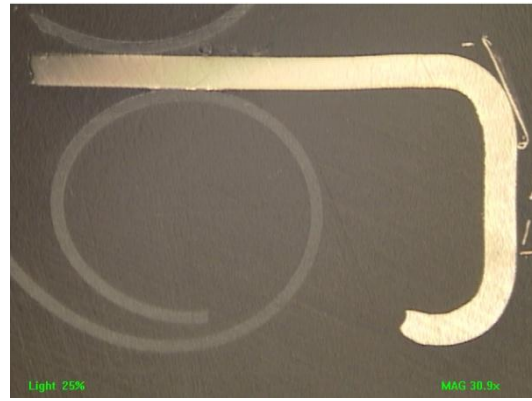


As seen from the electrical field contour plots, the maximum electrical field regions were respectively observed to be located along the curvature and near the tip of the 45° and 90° curved flange profiles. However, compared to the 'flat' end design, a lower maximum electric field magnitude was observed around a rounded end flange end. In fact, from the comparative plot in Figure 7.27, the electric field magnitude was observed to reduce from 1.41 MV/m to 0.89 MV/m for the 70° flange profile, and from 0.78 MV/m to 0.76 MV/m when the insert has a 45° contour end.

Because rounding the end of the curved flange was observed to reduce the magnitude of the electric field strength at the interface region, the 45° curved flange whose end is rounded was considered appropriate for the 50 mm prototype. The flange was then fabricated under another parallel collaboration involving Loughborough University and Advanced Chemical Etching (ACE) Ltd (<http://www.ace-uk.net>). To develop the flanges, since the maximum electrical field strength region was required to be located along the curvature and away from the flange tip, various development iterations were necessary before the appropriate rounded end 45° curved profile was successfully manufactured. To prevent oxidation of the copper flange during the cold-welding process when the thyristor device was assembled, the insert was also required to be plated with a 5.0 µm thick nickel coating. A photo of the curved copper flange that was successfully manufactured in the NEWTON project is shown in Figure 7.28; while Figure 7.29 illustrates a close-up of the 45° rounded end curved profile of the manufactured flange. A photograph of the flange after the nickel coating process is also shown in Figure 7.30.



**Figure 7.28: Photo of a fabricated copper flange**



**Figure 7.29: Photo depicting the fabricated curved profile having a rounded end also**



**Figure 7.30: Photo of a nickel-plated flange used in the development of the 50 mm prototype**

## 7.8 Discussion

In this chapter, different studies have been presented to reduce the high electric field around the flange/housing interface region and prevent housing failure during the operation of the thyristor due to partial discharge and dielectric breakdown. Because different research work has found that the shapes of electrodes attached to insulators influence the electric field magnitude within them, the design of the copper metal flanges protruding inside the polymer housing at the cathode and anode ends and joining the copper pole pieces to the housing was varied to reduce the electric field magnitude at the flange/housing interface regions. The research activities also aimed to identify the appropriate design and dimension of the metal flanges

so that they could be used in the 50 mm prototype. To simulate and compare the electrical performance of different flange end designs, the finite element analysis technique was used, with a 10 kV DC voltage applied between the copper pole pieces.

The initial studies involved a preliminary comparison of the electrical performance of different design concepts. Examples of some initial flange end designs studied involved straight flange inserts having pointed and rounded ends, circular and elliptical shaped wire-edged end geometries, and also insert ends having a curved end profile. By comparing the electric field magnitude around these initial geometries, the circular, elliptical and curved insert designs were observed to have lower electric field magnitude around them as opposed to the straight flange. Additional studies were thus done on these flange designs, whereby the influence of varying their sizes on the electric field magnitude at the contact regions were investigated to determine the appropriate flange shape and dimension for the 50 mm prototype. As have been widely reported in different literatures, when the radius of curvature of the shortlisted flanges was increased, the electric field magnitudes at the cathode and anode ends contact regions were also observed to decrease in these studies. However, the change in the electric field values around each flange designs was observed to be low.

To determine the appropriate flange design, an additional study to compare the electric field magnitude around the circular, elliptical and curved flanges, where each had similar curvatures, was thus necessary. From this study, the electric field was seen to be slightly lower around the elliptical flange end, compared to the circular and curved inserts. However, because attempts to manufacture the elliptical and circular flange proved difficult in the project compared to the curved profile which could be fabricated, the curved flange was hence selected to be used for the 50 mm prototype.

Although the curved flange design provided benefits in terms of their electrical performance and manufacturing feasibility, the added disadvantage such an insert profile provided was void could be formed inside the curved region of

the insert during the moulding process of the housing. To reduce the probability of occurrence of such a defect, two geometrical parameters were varied and the electrical performance of the housing studied. These included the vertical height and the contour length of the flange. When the flange height was varied, the electrical field at the cathode and anode ends contact regions were seen to remain predominantly constant because the radius of curvature of the curved flange was unchanged in this study. Because the bend radius of the curved flange studied was 1 mm, a flange having a reduced vertical height of 1 mm was thus initially selected. Such a flange end would correspond to a fully-curved design. To further improve the curved flange design and enable an appropriate flow of the polymer around the inner curve region to reduce likelihood of void formation, the length of the curved flange contour length was reduced by changing an angle parameter  $\theta$  between  $0^\circ$  and  $90^\circ$  (Figure 7.20). When the flange contour length was changed by varying  $\theta$ , a lower electric field was observed for flanges having profile angle less than  $45^\circ$ . This corresponded to the maximum electrical field being located along the desired curvature of the flange. However, for larger electrical field values observed for flanges having profile angles greater than  $45^\circ$ , the maximum electrical field region was observed to occur at the tip of the flange end, which is undesired and will cause partial discharge failure of the polymer housing. Coupled with these simulation studies to improve the curved flange design, attempt to round the insert ends and investigate their influence on the electrical field was also studied. From this study, further reduction of the electrical field magnitude was observed at flange/housing contact regions.

Based on the electrical simulation studies described in this chapter to lower the localised electrical field magnitude at the contact regions, a  $45^\circ$  insert having a curved profile and a rounded end was concluded to be appropriate for the 50 mm prototype. This would ensure the electric field magnitude around the flange/housing contact region would be lower during the thyristor operation, and failure of its polymer housing due to partial discharge would be prevented. In collaboration with ACE Ltd, different development trials were

performed in the NEWTON project before the appropriate rounded end 45° curved flange profile was successfully developed.

## **8 50 mm prototype development II: Influence of thyristor housing geometry**

### **8.1 Introduction**

Following the electrical performance study of the polymer housing and identification of the metal flange design in Chapters 6 and 7 respectively, additional studies, focussed on the geometrical parameters of the thyristor housing, were also performed to assist the 50 mm prototype development. These are discussed in this chapter. As highlighted in Chapter 4, inappropriate dimensions of certain geometrical parameters can result in the housing failure. For instance, having an incorrect dimension of the flange depth, the position it is located within the housing, and the package thickness can result in moulding defects, together with partial discharge and dielectric breakdown failures when exposed to electrical stresses. On the other hand, inappropriate design and dimensions of the housing convolutes located along the package exterior can also lead to failure due to tracking.

To reduce the likelihood of any moulding defect formation and electrical failure of the housing, the influence of the critical geometrical parameters highlighted above were studied in a 2-stage process to develop a 50 mm prototype having improved performance properties. In stage 1, the influence of varying the flange depth, its position within the housing, and the convolute shapes on the electrical performance of the polymer package were studied. These were done using a series of electrical simulations to further reduce the localised electric fields at the flange/housing interface regions at the cathode and anode ends. A modified 50 mm housing design, having either 4 or 5 convolutes respectively shown in Figures 8.1 and 8.2, was used for these studies. The design was constrained so that the 50 mm prototype being developed could fit in an in-house assembly jig that was used for cold-welding the pole pieces and housing flanges at Dynex.

As illustrated in both Figures 8.1 and 8.2, the cathode and anode copper pole piece diameters of the modified thyristor device design were taken to be around 47 mm and their thicknesses to be 20.3 mm and 16.6 mm respectively, while the package thickness was 4.2 mm and its height around 26.5 mm. The design of the insert end was based on the partially curved 45° flange with a radius of 1 mm, identified in Chapter 7, and with its end having the flat tip design (instead of the desired round shape). The outer diameter of the device was chosen to be 70.8 mm so that it could fit in the cold-weld assembly jig. The different housing geometries, namely the depth,  $d$ , the flange protrudes inside the housing, and the position,  $f$ , across the package, studied in the stage 1 phase are also shown in Figure 8.3. It should be noted when these geometries were changed, the overall size, i.e. its overall height, external diameter, was kept constant.

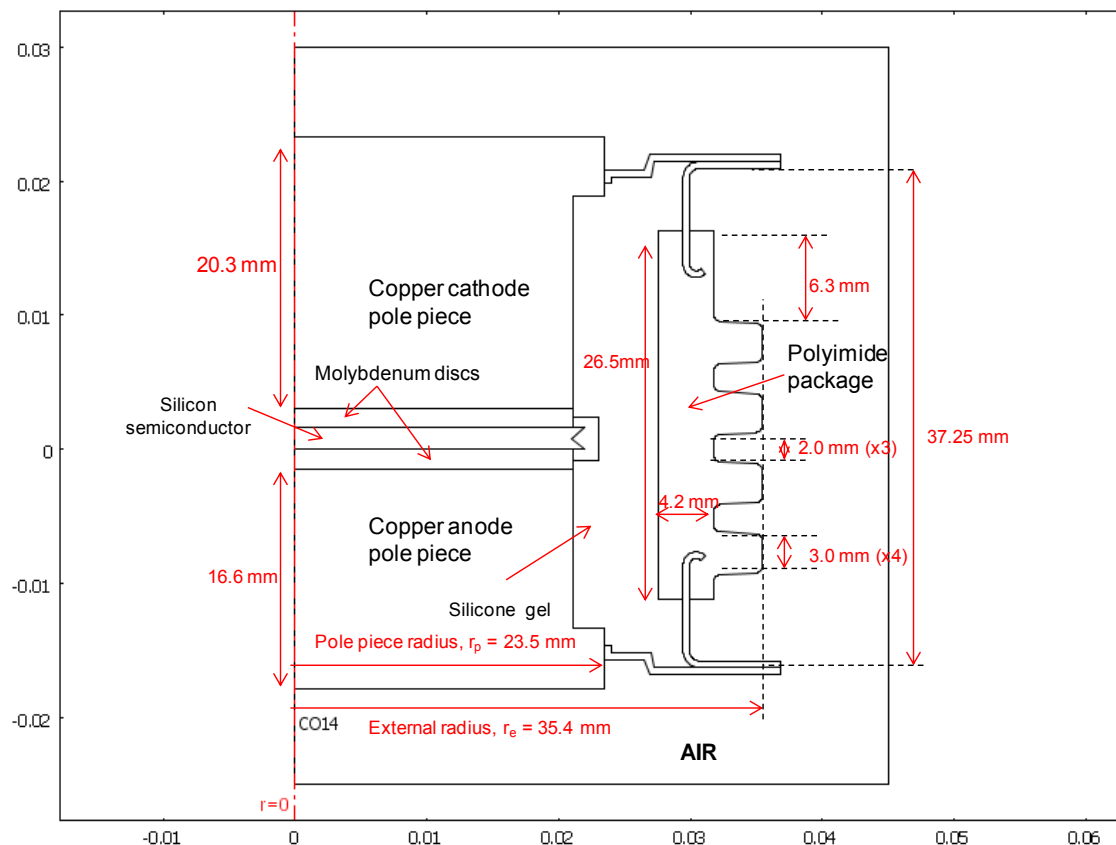
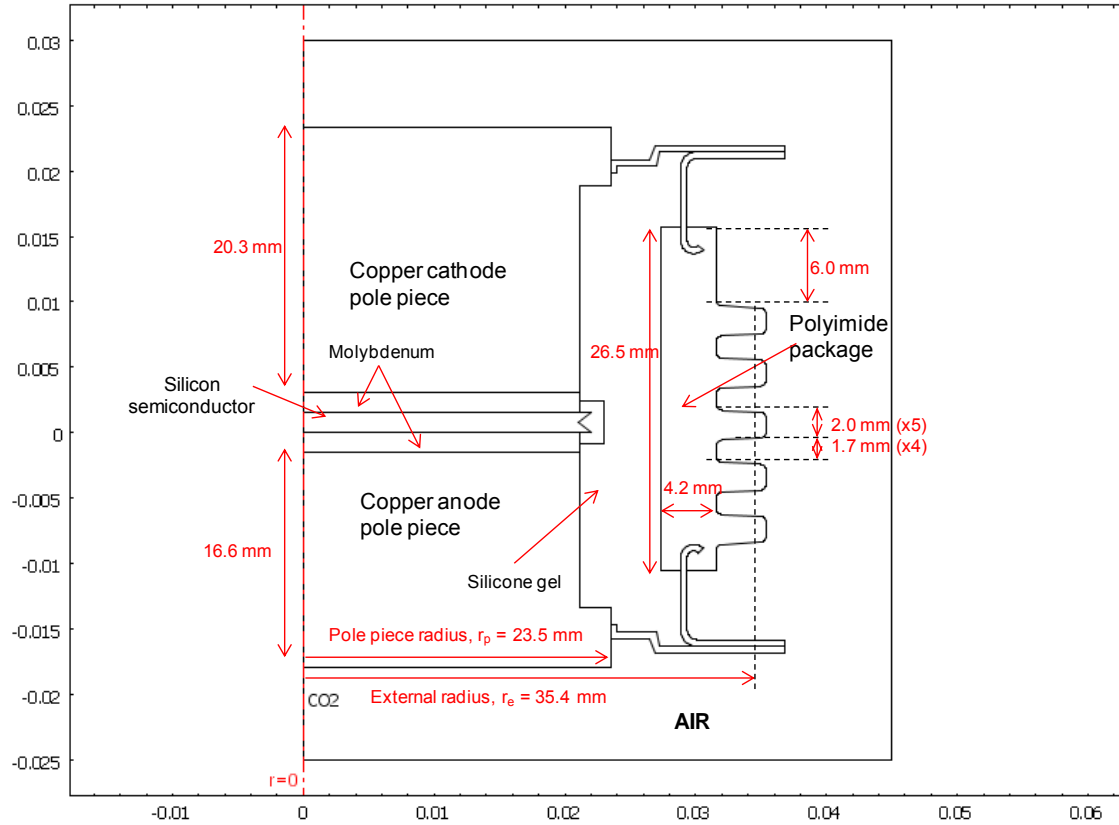
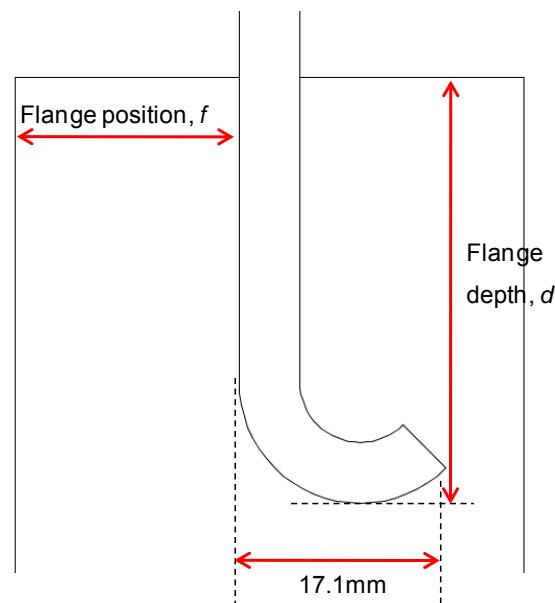


Figure 8.1: Axisymmetric model of the modified 4 convolute housing design



**Figure 8.2: Axisymmetric model of the 5 convolute housing design**



**Figure 8.3: Illustration of the housing parameters studied in stage 1**

In the second phase (stage 2), the package design benchmarked from stage 1 was further refined from both an electrical and moulding performance



perspective. In a typical injection moulding process, common moulding defects that can occur include sinks, voids and among others warpage if moulding process parameters, such as fill time and packing time, are not properly determined. Together with this, having an appropriate wall thickness for the housing (that is ideally thinner) was also considered important to reduce the probability of occurrence of these defects. Different injection moulding studies were performed by DuPont™ using Moldflow FE software. This was also complemented with various electrical simulation studies performed in parallel by Loughborough University. The moulding and electrical simulation results were then compared before an optimum wall thickness and design for the 50 mm prototype housing was finalised.

The different investigations performed in stage 1 and 2 phases to develop the 50 mm prototype are discussed in the following sections of the chapter. Section 8.2 overviews the stage 1 simulation studies, whereby the electrical performance of the housing was studied to identify the appropriate dimensions of the flange position, the depth it protrudes inside, together with the housing convolute design. The stage 2 simulation studies which focussed on determining the effect of housing thickness are discussed in section 8.3. Section 8.4 finally presents the final 50 mm prototype design determined following stage 1 and 2 simulation studies. It should be noted that for the different electrical simulation studies described in this chapter, silicone gel was selected to be present inside the cavity of the polymer thyristor.

## **8.2 Stage 1: Housing geometry study**

In this section, the influence of the flange position, its depth inside the housing, together with the convolute shape influence on the electrical performance of the modified 50 mm housing design is discussed. As highlighted earlier, to improve the electrical performance of the package, the aim was to reduce the localised electric field magnitude at the flange/housing contact region.

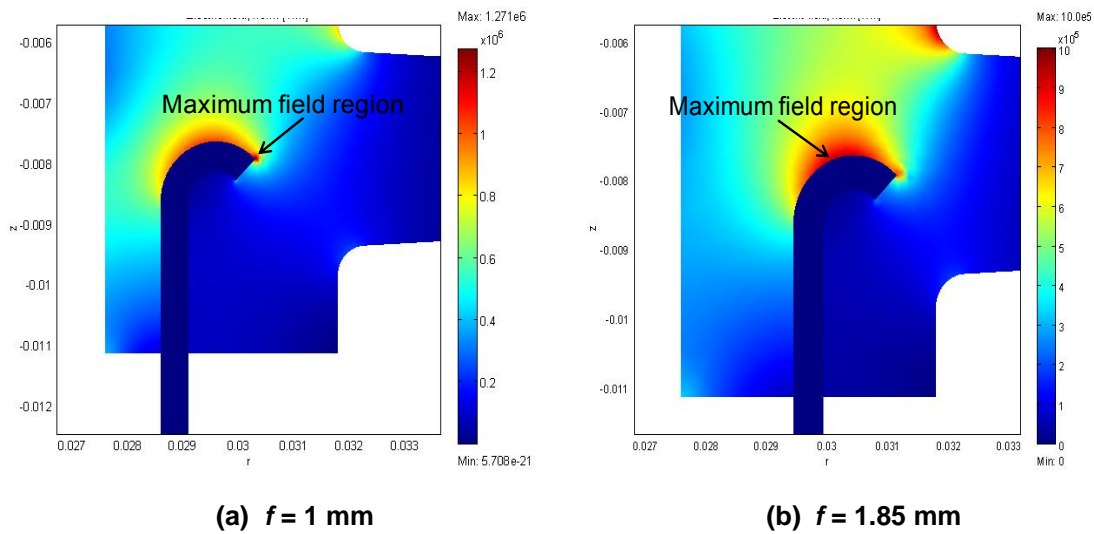
### 8.2.1 Flange position, $f$ , and insert depth, $d$ , geometries

The flange position parameter and its depth in both the 4 and 5 convolute housings were investigated first, before changes in the electrical performance due to the housing convolute design were considered. The electrical behaviour of the housing due to the flange position,  $f$ , was studied by varying the insert position between 0.75 mm and 2.40 mm distance from the inner edge of the housing, while the flange depth,  $d$ , was kept constant at 3.5 mm (Figure 8.3). On the other hand, the influence of the flange depth,  $d$ , was investigated by changing the depth between 1.5 mm and 5.5 mm distance while keeping its position,  $f$ , constant at an appropriate distance mentioned later in this section.

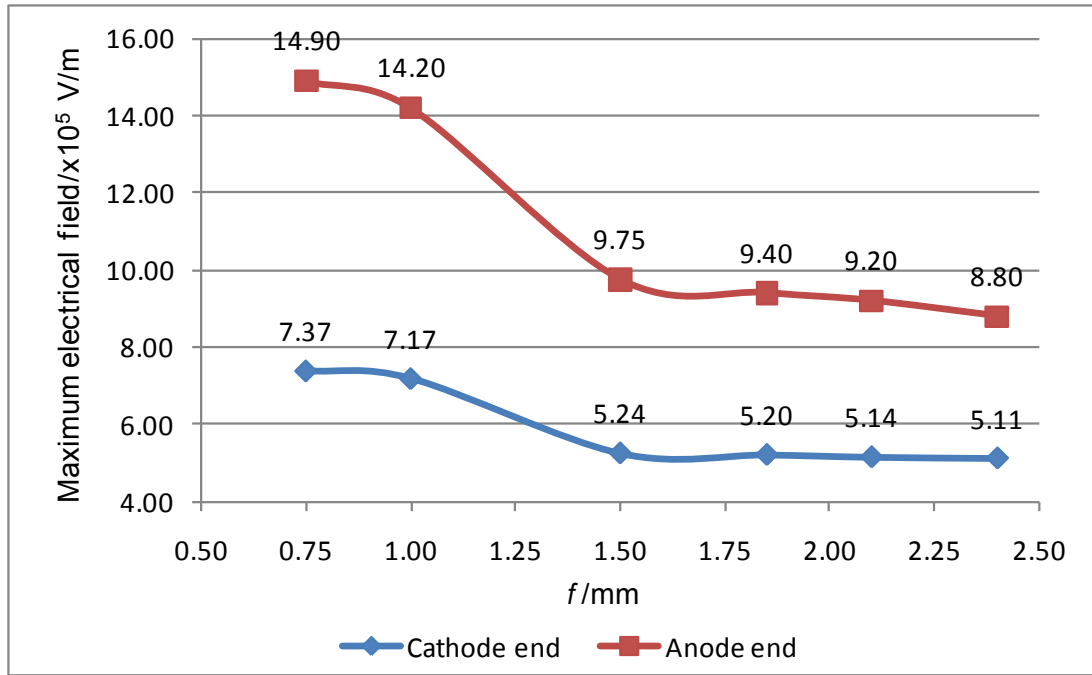
Electric field strength contour plots, when the flange protruded 3.5 mm inside the housing and was located at a distance,  $f$ , 1 mm and 1.85 mm distance from the inside edge of the 4 convolute housing, are respectively shown in Figures 8.4 (a) and (b). As shown in Figure 8.4 (a), the maximum electric field region at the flange/housing interface was seen to be located at the tip of the curved flange when the insert was located at 1 mm from the inner edge of the housing; whilst when located at a 1.85 mm distance, the maximum was seen to be along the desired flange curvature.

The electric field variation at the cathode and anode end contact regions, when the flange position,  $f$ , was varied between the 0.75 mm and 2.40 mm distance inside the 4 convolute housing, is illustrated in Figure 8.5. As shown in Figure 8.5, the maximum electric field magnitudes at the interface region of the cathode and anode ends were seen to remain predominantly constant when the flange was located more than 1.50 mm from the inner edge of the housing. However, when the insert was at less than 1.50 mm distance, a comparatively higher electric field strength magnitude was observed at both the cathode and anode end interfaces. These high field values were found to be due to the maximum electric field region being located at the tip of the curved end of the flange; whilst for flange positions greater than 1.50 mm the maximum field region was located along the curvature of the curved insert

(desired region). As highlighted in Chapter 7, location of the maximum electrical field at such a location is undesired, as it can lead to partial discharge failure of the polymer housing. From this study, the location of the maximum electric field region at the interface was actually observed to be influenced by the inner edge of the housing and the flange distance along the package. When the insert was located close to the inside periphery of the 4 convolute housing, e.g.  $f = 0.75$  mm and 1 mm, the maximum electric field region was found to be at the undesired flange tip region. When the location of the flange was increased, e.g.  $f > 1$  mm, the maximum field region was seen to move from the flange tip to occur along the curved flange curvature. As a result of this study, it was thus deduced a flange that is located at an appropriate distance away from the inner housing edge, e.g. in the middle of the package, would be appropriate to ensure the maximum electric region occur along the flange curvature, whereas a location near the inside housing edge would be undesired.



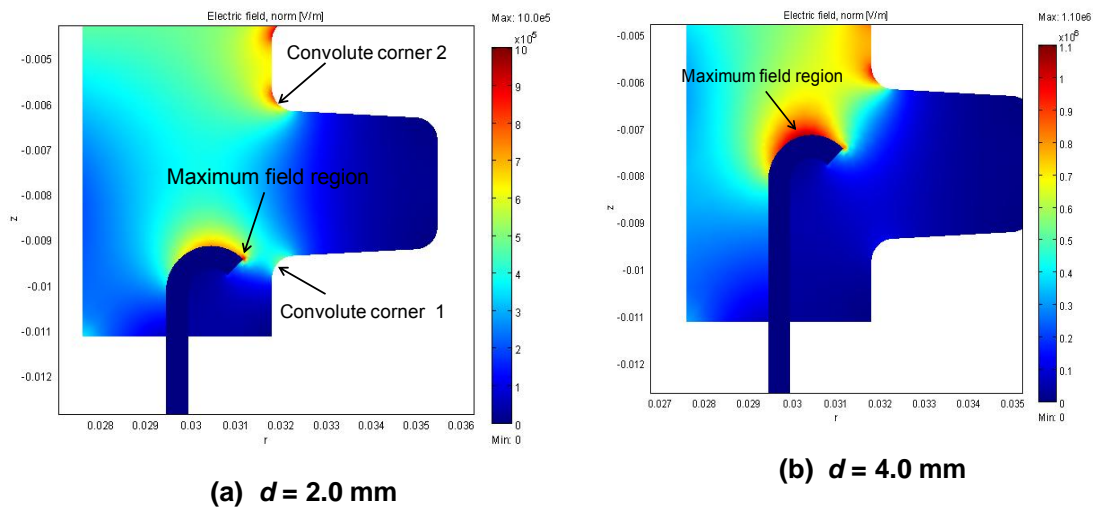
**Figure 8.4: Contour plot illustrating the electric field distribution around the anode end interface region when the flange position,  $f$ , is varied**



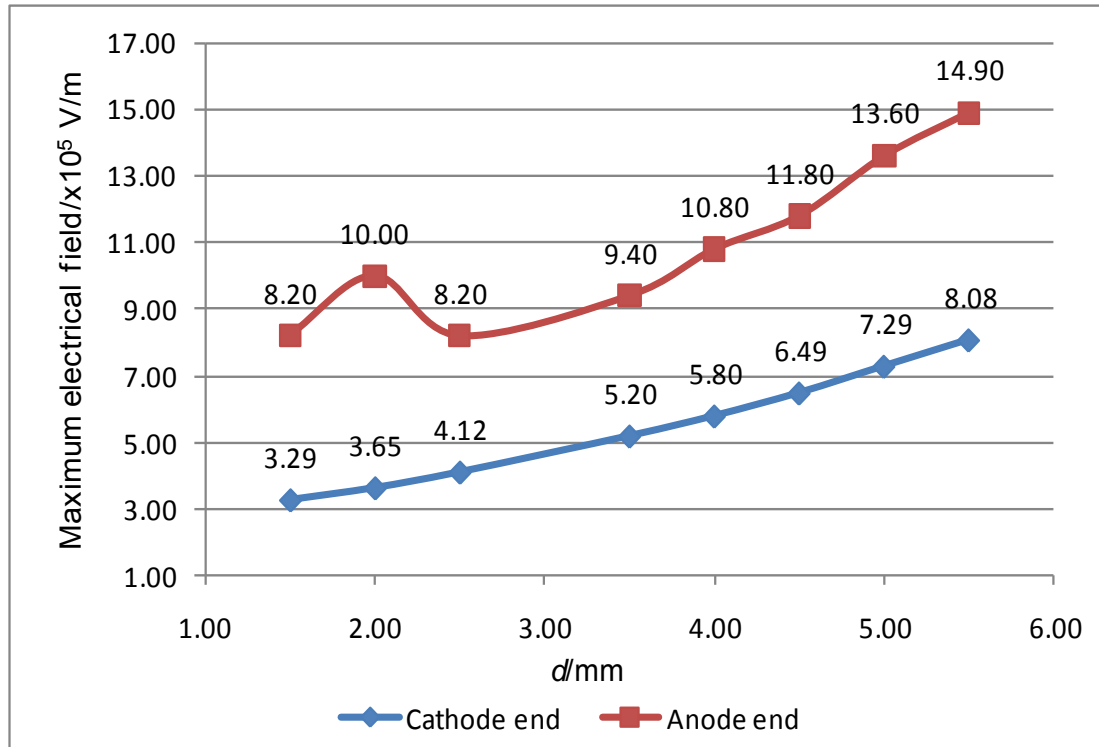
**Figure 8.5: Electric field variation as a result of change of flange position,  $f$ , for the 4 convolute housing**

The electric field distribution at the anode end interface region, when the flange protruded 2 mm and 4 mm inside the 4 convolute housing, are respectively illustrated in Figures 8.6 (a) and (b), while the maximum electric field variation at the cathode and anode end interface regions, as the flange depth was varied, is also shown in Figure 8.7. From the flange position variation study in Figure 8.5, because the maximum electric field region was observed to be located along the flange curvature when the insert is positioned at distance,  $f$ , greater than 1 mm, a flange position of 1.85 mm was selected for this investigation. As can be seen from the graph, the electric field magnitude was observed to increase at both the cathode and anode ends when the distance between the flange tips was reduced (i.e. the flange depth at both ends increased). However, higher electric field values, corresponding to the small peak in the electric field variation, were also observed when the flange was located at 1.5 mm and 2.0 mm depth at the anode end. Such high electric field magnitudes were again attributed to the maximum electric field regions being located at the tip of the curved flange (as shown in Figure 8.6 (a)), and were also observed to occur due to the flange location with regards to the housing convolute corners and outer periphery of the housing. From the

different simulation studies, the location of the maximum electric field region at the flange tip was observed to occur when insert end was near the outer housing edge ( $d = 1.5$  mm), and also when the insert tip was close (or at same height) to the convolute corners. As seen in Figure 8.6 (a) when  $d = 2.0$  mm and the maximum field region was located at the flange tip, the insert tip was at the same height as corner 1 of the bottom housing convolute in this case. When the flange depth was increased and was located away from the convolute corners, e.g.  $d = 4.0$  mm in Figure 8.6 (b), the maximum electric field region was observed to move away from the flange tip to its curvature. As a result of this study, it was thus deduced that locating the flange that is between the flange corners and at an appropriate distance from the outer edge of the housing, would ensure the maximum electric field regions are not located at the flange tips. Because the maximum electric field region was also observed to be located at the undesired flange tip region at a flange depth less than 2 mm, these preliminary electrical studies suggest an insert, located at more than 2 mm depth, would be appropriate for a 4 convolute 50 mm housing.



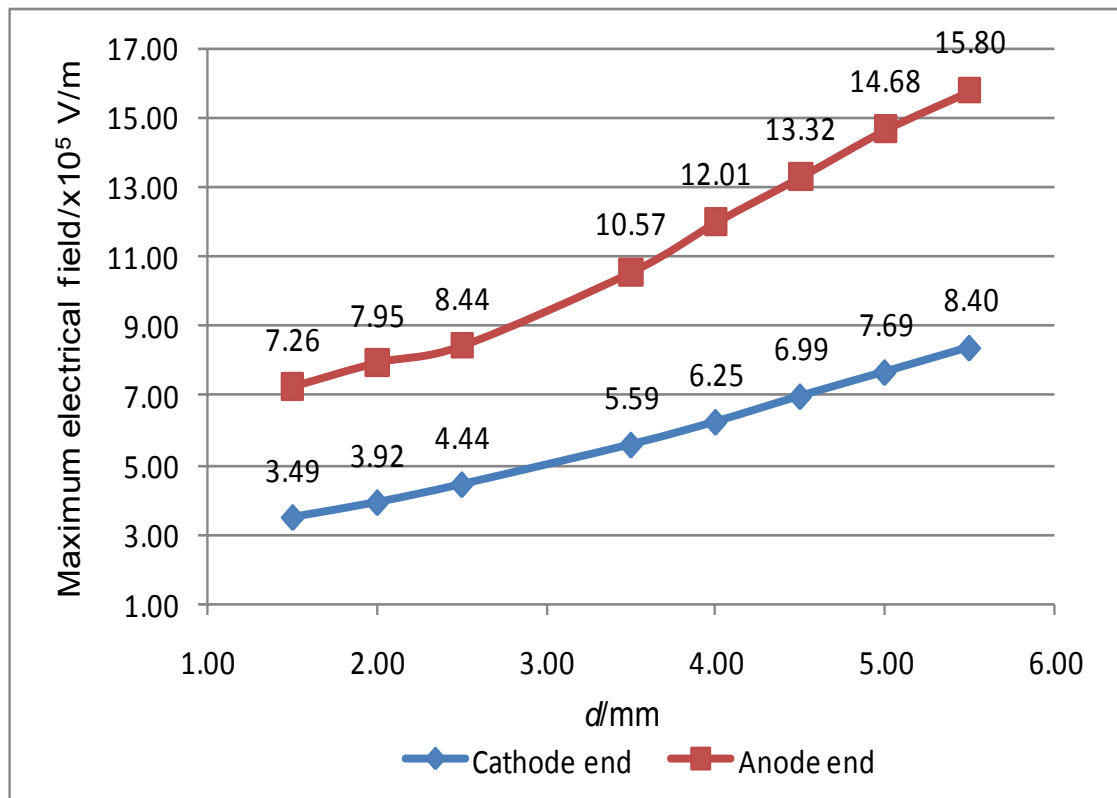
**Figure 8.6: Electric field distribution around the anode end interface region when the flange depth is varied**



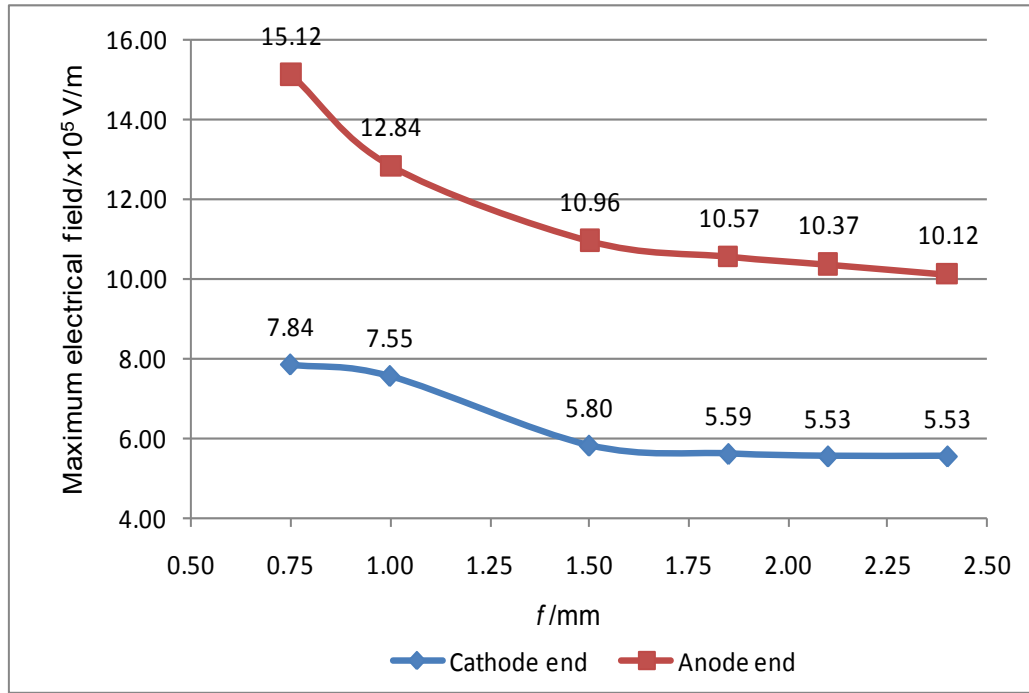
**Figure 8.7: Maximum electric field variation at anode and cathode contact regions when the flange depth,  $d$ , is changed inside the 4 convolute housing**

The variation of the interface region electric field, as a result of the flange depth,  $d$ , and the position,  $f$ , variation in the 5 convolute housing (Figure 8.2), are also shown in Figures 8.8 and 8.9. Compared to the 4 convolute housing, the electric field magnitudes inside the 5 convolute housing were observed to be slightly higher when the flange depth,  $d$ , and its position,  $f$ , were varied. Together with this, as in the case of the 4 convolute housing, the electric field was also observed to rise when the flange depth,  $d$ , inside the housing was increased (Figure 8.8); while they were observed to decrease when the flange position,  $f$ , from the inner edge of the housing was increased. Compared to the 4 convolute housing, the maximum electric field regions in the 5 convolute package were observed to remain along the flange curvature, when the flange depth was varied. This was because for the different flange depth locations in the 5 convolute housing the flange tip was not located at the same height and near the convolute corners. When the depth was fixed at 3.5 mm and the inserts were located at distances more than 1.50 mm from the inside edge of the housing (Figure 8.9), the maximum electric field region was observed to remain predominantly constant at both cathode and anode ends, However,

when located at distances less than 1.50 mm, a comparatively higher electric field values was obtained which was due to the maximum electrical field regions being located at the tip of the curved flange end similar to the case for the 4 convolute housing. As observed in the 4 convolute housing, the higher electric field and maximum electric field location at the flange tip was again due to the influence of the housing inner edge. As the flange location,  $f$ , was increased, the maximum electric field region at the interface was seen to move from the flange tip to occur along the insert curvature.



**Figure 8.8: Maximum electric field variation when the flange depth,  $d$ , is varied in the 5 convolute housing ( $f = 1.85$  mm)**



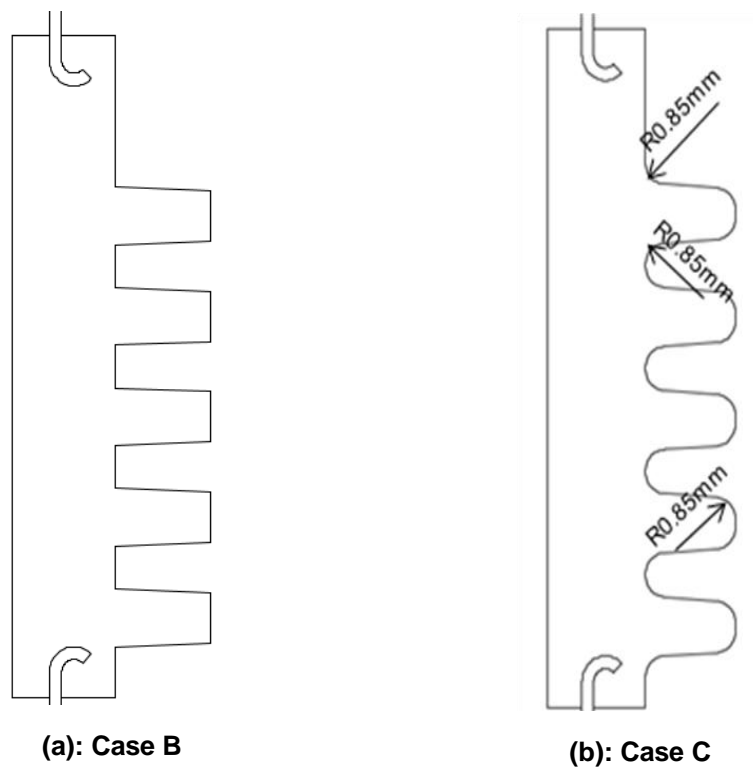
**Figure 8.9: Maximum electric field variation due to change in the flange position,  $f$ , in the 5 convolute housing ( $d = 3.5$  mm)**

### 8.2.2 Housing convolute design

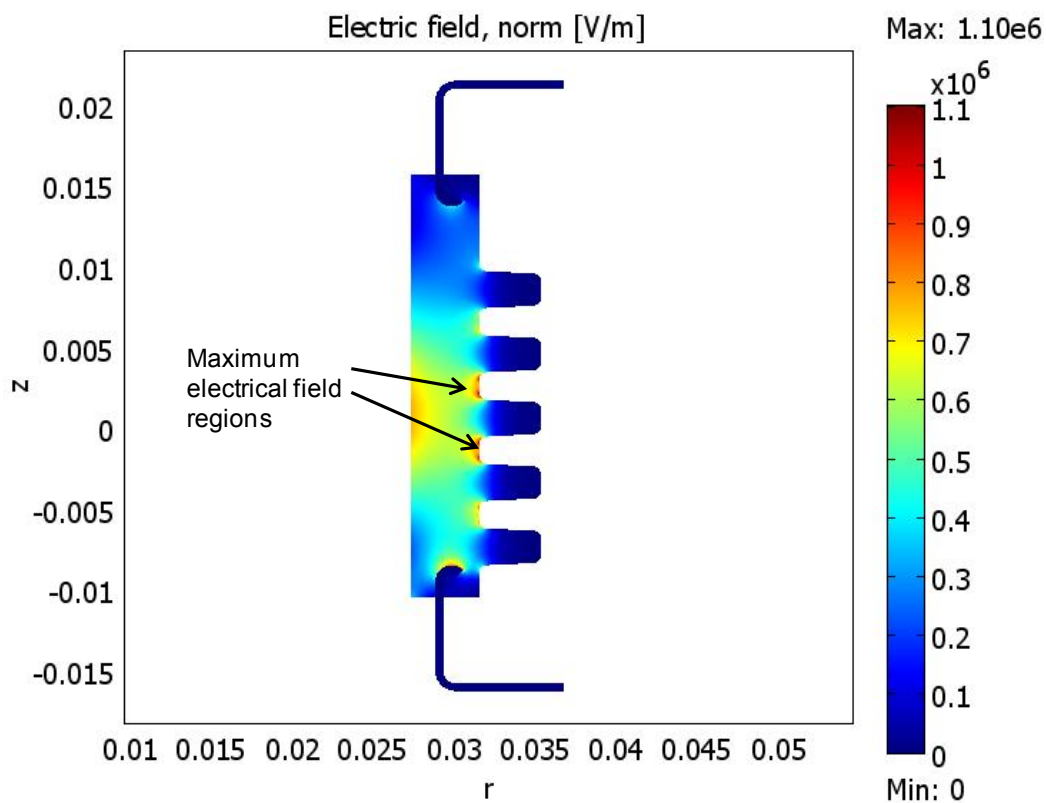
Together with the flange depth and position parameter studies, the influence of different housing convolute designs on the electrical performance of the housing was also studied to assist the 50 mm prototype development. To vary housing convolute design, the radius of curvature of the convolute profile was changed for these studies. It should be noted, instead of the 4 convolute housing (Figure 8.1), the 5 convolute configuration design was here used. This was because across this housing the maximum electrical field regions were seen to remain predominantly along the curvature of the curved flange rather than the flange tip when the flange depth parameter was varied. Also, because the comparative tracking distance of the selected glass-filled polyimide polymer for the polymer housing could not also be quantified in the project, selecting a 5 convolute housing would enable the tracking distance along the exterior surface between the anode and cathode ends of the thyristor to be higher than a 4 convolute configuration housing (thereby also reducing the probability of failure due to tracking along the housing exterior).



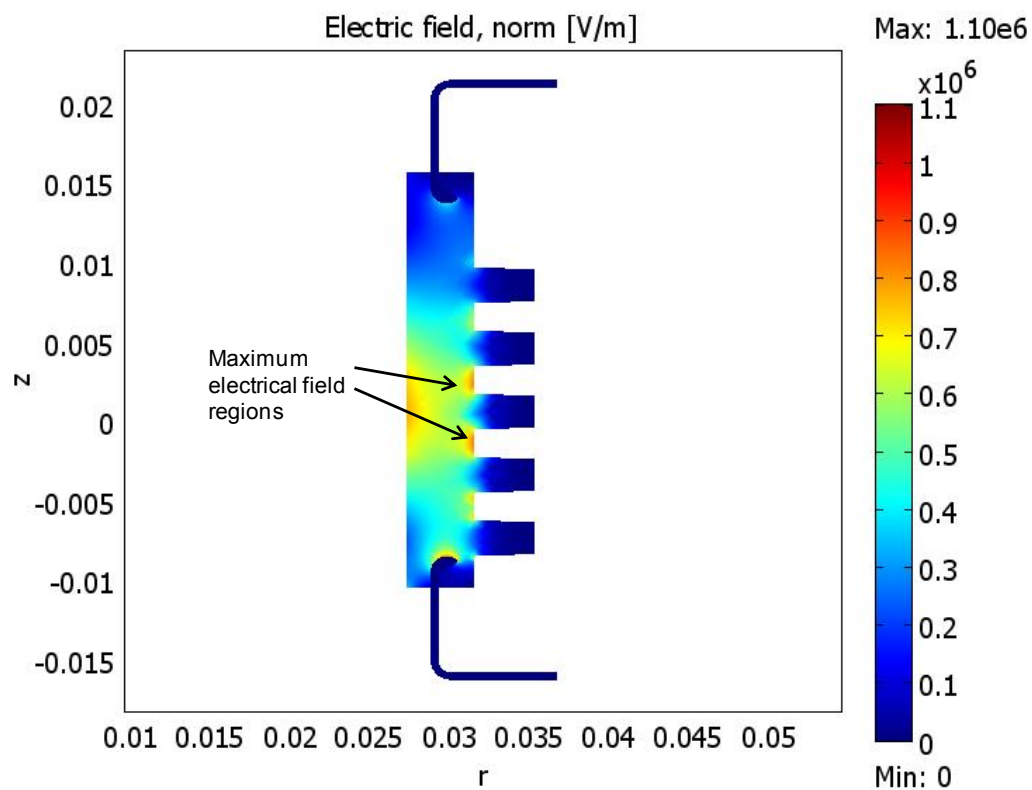
For this study, the 5 convolute housing, which had 0.5 mm radius of curvature at the top and bottom of the housing convolutes (case A), was compared with two different convolute profiles (cases B & C). In case B (Figure 8.10 (a)), no rounded corners were present at the top and bottom corners of the convolute, while in case C the convolute radius was taken to be 0.85 mm (Figure 8.10 (b)). The electrical field distribution within the different housing designs is described next. It should be noted that for these studies the flange depth,  $d$ , was taken to be 2 mm, while the distance it was located within the housing was selected to be  $f = 1.5$  mm because the maximum electric field region at the interface was observed to be located along the curvature of the flanges for these flange depth and position dimensions (as highlighted in Figures 8.8 and 8.9).



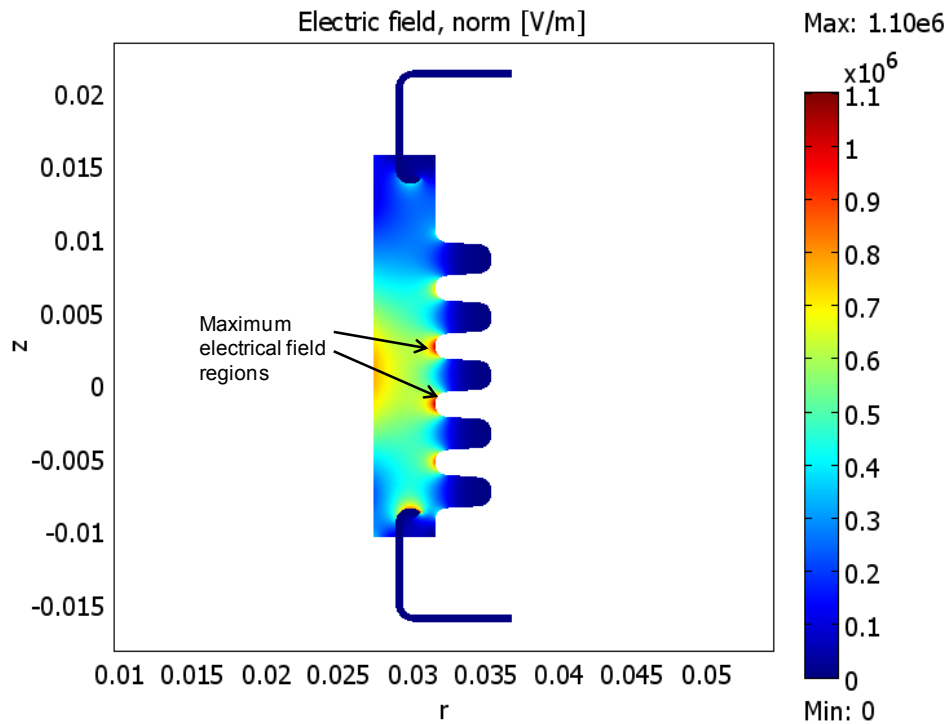
**Figure 8.10: Housing convolute design**



(a): Radius of curvature = 0.5 mm (Case A)



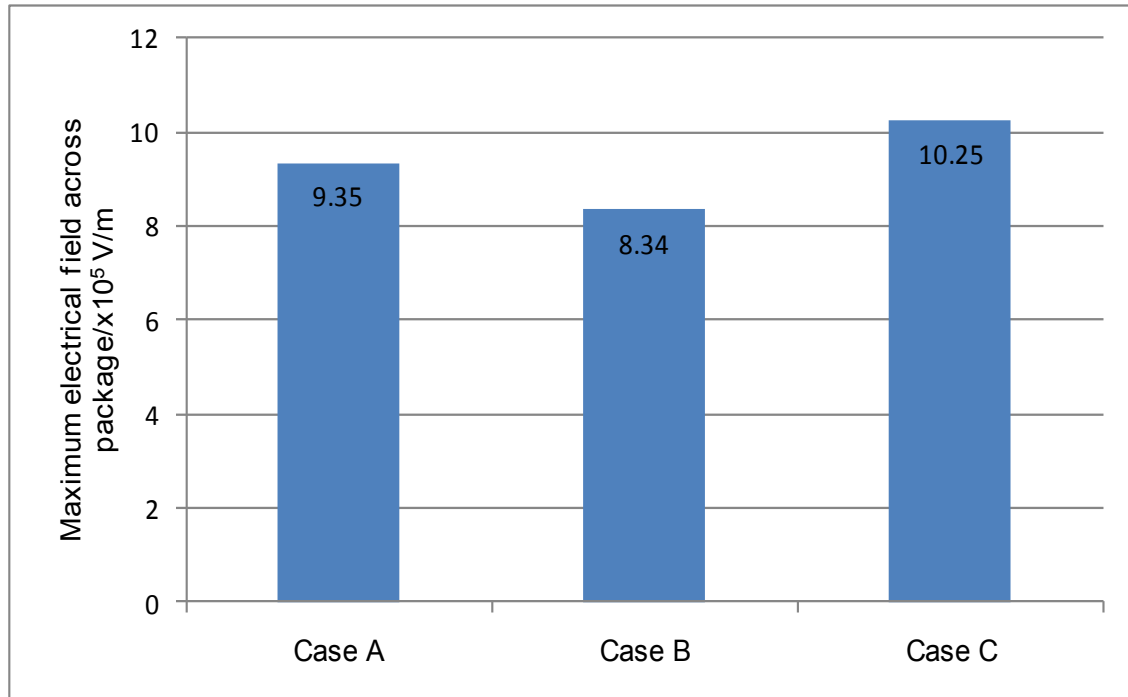
(b): No rounded corners present along the convolutes (Case B)



**(c): Radius of curvature = 0.85 mm (Case C)**

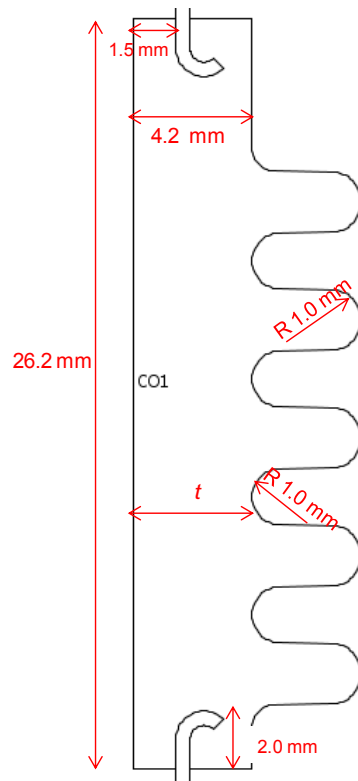
**Figure 8.11: Electric field contour plots when the housing convolute designs are varied**

The electric field contour plots across the different housing convolute designs are illustrated in Figures 8.11(a) to (c). For the different convolute profiles, the maximum electrical field regions that occur at the cathode and anode end flange/housing interfaces, were observed to occur along the curvature of the curved flange. Together with this, high electric field regions were also observed within the package between the 2nd and 4th convolutes also. A comparison of the maximum electrical field magnitude at these regions, when the radius around the convolute was varied, is illustrated in Figure 8.12. From Figure 8.12, it can be seen the lowest electric field magnitude was observed to occur in case B, which had no rounded corners around the housing convolutes, whilst the highest field magnitude was noticed to occur when the radius of curvature around the housing convolute was highest, i.e. case C.



**Figure 8.12: Comparison of maximum electric field magnitude across the package as a result of change in the convolute profile**

As a result of the different housing design parameter studies, an initial benchmark design for the 50 mm prototype based on a 5 convolute configuration package, was selected as shown in Figure 8.13. Although the electric field magnitude within the housing having no rounded convolutes was found to be low, a package whereby the radius of the housing convolute corners were of 1 mm dimension was chosen as the mould tool that would used to mould such housing was regarded to be easier to fabricate. From the electrical performance studies described earlier, the flange depth,  $d$ , and its position,  $f$ , along the housing were also taken to be 2.0 mm and 1.5 mm respectively. For electrical performance reasons, the flange was also positioned at 1.5 mm distance, so that at least a 1 mm separation was maintained between the outer surface of the housing and the flange tip. According to experts familiar with the selected glass-filled polyimide polymer processing, such spacing would also ensure the polymer flowed properly around the inner curved region of the flange, thereby reducing the likely formation of any moulding defects, such as voids, in the housing.



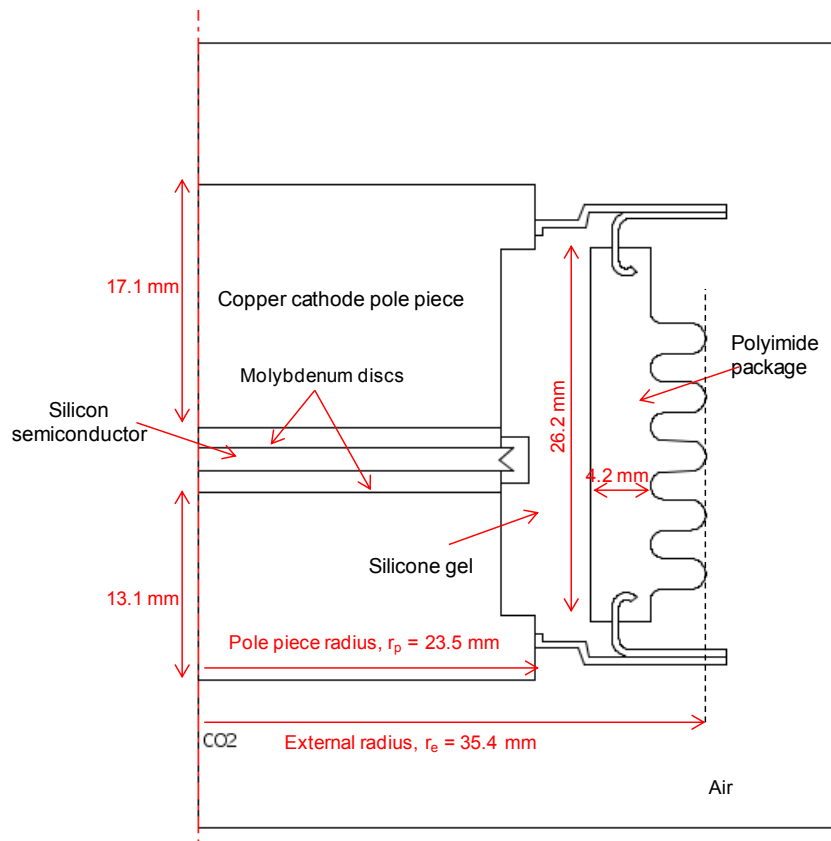
**Figure 8.13: Initial benchmark design of 50 mm prototype housing determined from stage 1 studies**

### 8.3 Stage 2: Variation of package thickness

Together with the electrical performance studies to prevent potential partial discharge and breakdown failures of the polymer housing, additional studies were also required to reduce the probability of any moulding defects due to inappropriate dimensions. The housing dimension, that was considered to be critical to reduce the likelihood of any moulding defects, was the housing wall thickness. To determine the appropriate housing thickness, the electrical and moulding performance of package designs having 2.0 mm, 2.5 mm, 3.0 mm, 3.5 mm and 4.2 mm wall thicknesses ( $t$  in Figure 8.13) were compared. It should be noted rather than varying the wall thickness of the whole package, only the wall thickness,  $t$ , around the convolute area was modified for this study. Comsol FE package was again used for the electrical performance study, while a series of moulding simulations were performed in parallel by DuPont™ using the Moldflow package to highlight potential moulding issues.

The results from both the electrical and moulding simulation studies were then compared, before the optimum housing thickness and design for the 50 mm prototype were finalised.

The electrical simulation studies performed to determine the polymer housing thickness are first discussed in sections 8.3.1, while the different injection moulding studies performed by DuPont™ are summarised in section 8.3.2. It should be noted, compared to the stage 1 FE models, a different anode and cathode copper pole piece dimension was here used, so that the housing could fit in a cold-weld tool whose design and dimensions were updated during the project. For the electrical simulation studies in this stage, the thickness of the anode and cathode pole pieces were here respectively reduced to 17.1 mm and 13.1 mm dimensions, as shown in Figure 8.14.



**Figure 8.14: Axisymmetric model of the housing design used for stage 2 electrical simulation studies**

### 8.3.1 Electrical performance studies

Typical contour plots of the electrical field distribution within 2.0 mm and 4.2 mm thick housings can be seen in Figures 8.15 (a) and (b); while a comparison of the maximum electrical field magnitude around the housing convolutes, when the housing thickness,  $t$ , is changed, is illustrated in Figure 8.16.

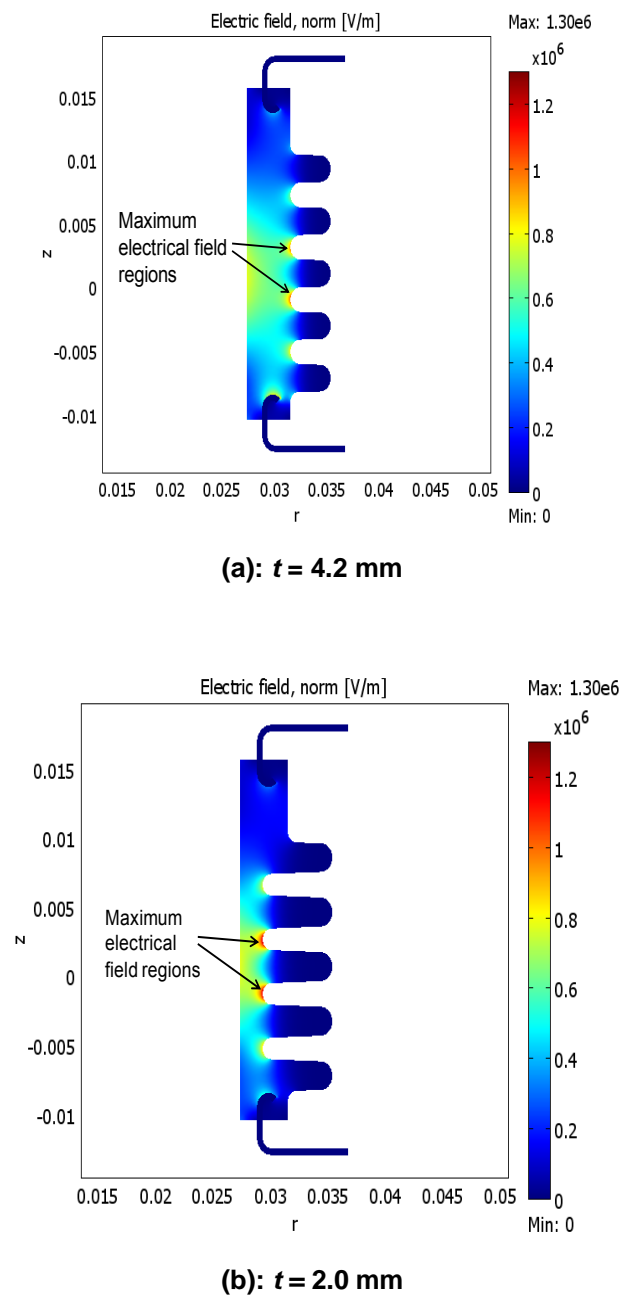
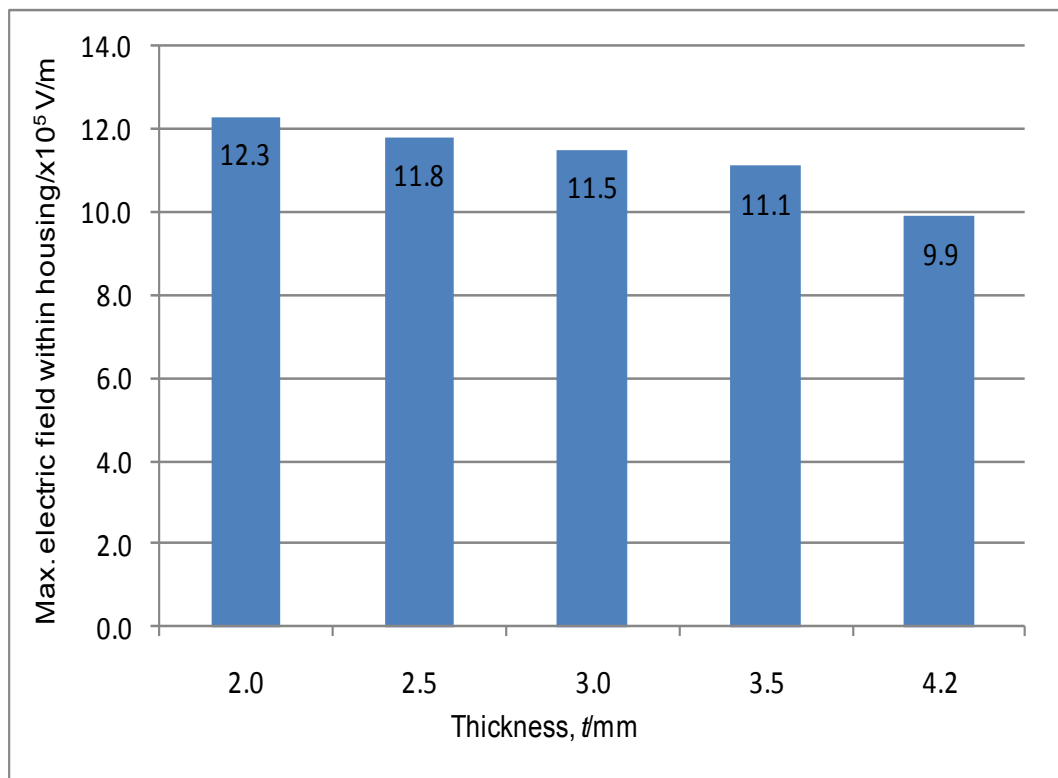


Figure 8.15: Electric field distribution across 2 mm and 4.2 mm thick housings



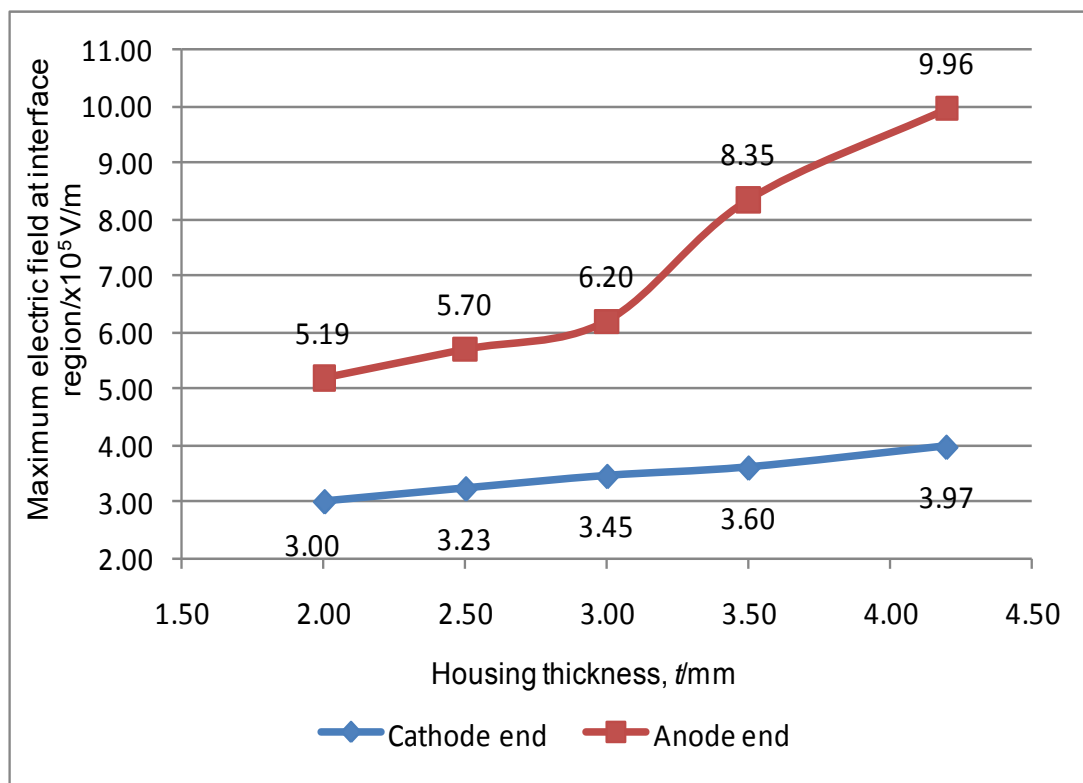
**Figure 8.16: Comparative plot of the maximum electric field magnitudes within the polymer when the thickness of the housing is varied**

Similar to the case of the housing convolute design studies in section 8.2.2, together with the maximum electrical field regions at the cathode and anode flange/housing contact areas, high electric fields were also observed around the 2nd and 4th convolutes of the housing when the package thicknesses were varied (Figure 8.15). When the package thickness,  $t$ , was increased, the magnitude of the electric field around the housing convolute was observed to decrease, as illustrated in the comparative plot in Figure 8.16.

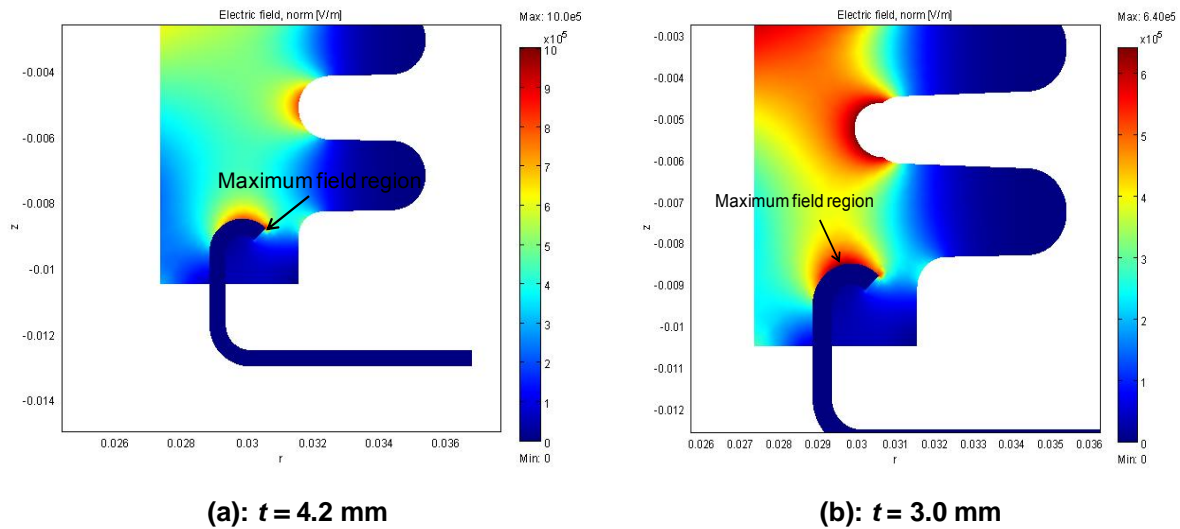
The variation of the maximum electrical field at the anode and cathode end flange/housing contact region is also highlighted in Figure 8.17. As can be seen from the graph, the electric field magnitude at the interface regions were observed to increase, when the wall thickness of the package also increased. In particular, a higher electric field magnitude was noticed when the package had a thickness greater than 3 mm. This was actually due to the housing convolute design which caused the maximum electric field region to be



located at the flange tip. As shown in Figure 8.18 (a), when the wall thickness was 4.2 mm, the maximum electric field region at the contact region was located at the flange tip; while when the housing was reduced to thicknesses less than 3.5 mm, the maximum electrical region at the cathode interface was observed to move away from the flange tip to be located along the curvature of the flange insert, as shown in Figure 8.18 (b) which illustrates the electric field plot at the anode end contact region of a 3.0 mm thick housing. As discussed in earlier sections, because location of the maximum electric field at the curved flange tip can lead to partial discharge failure of the package during service, a housing, with a thickness less than 3.0 mm, was thus concluded to be appropriate for the prototype based on the electrical simulation results.



**Figure 8.17: Variation of the maximum electrical field at the interface region as a result of change in the housing thickness**



**Figure 8.18: Electric field distribution at the anode ends of 3 mm and 4.2 mm thick housings**

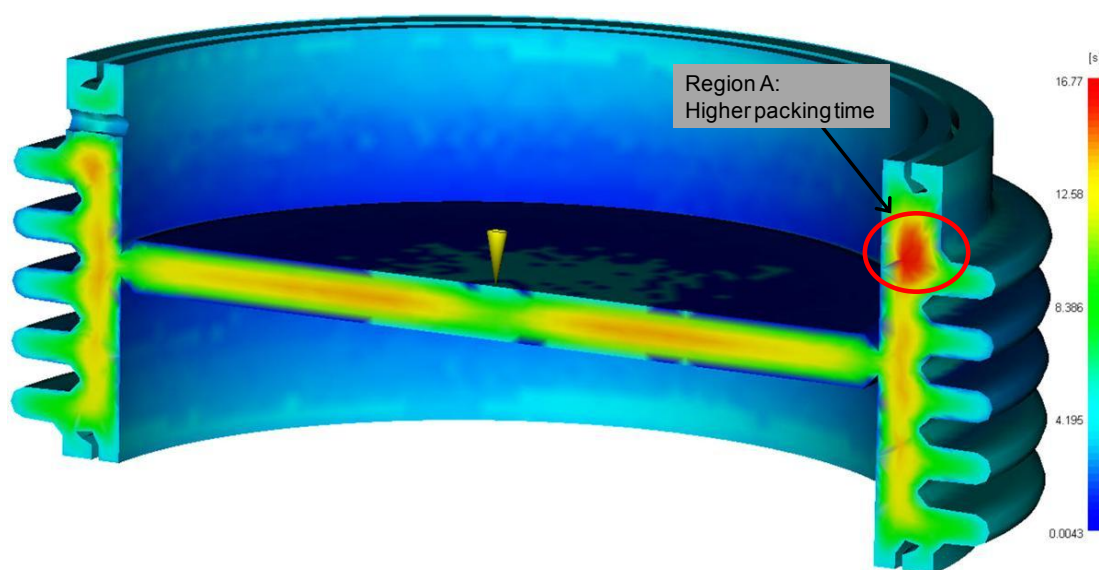
### 8.3.2 Injection moulding simulation studies

In parallel to the electrical simulation studies described in section 8.3.1, different injection moulding simulation studies were also performed by DuPont™ to identify potential moulding defects and determine the appropriate thickness of the housing. A summary of the works performed is described next.

From initial modelling studies, a longer packing time (which is the duration it would take to fill the mould cavity as full as possible to manufacture the finished part without any undue stress during the moulding process) was observed around a region located above the 1<sup>st</sup> convolute at the cathode end – illustrated by region A in Figure 8.19. This represented a likely location where voids and warpage defects could be formed as a result of the moulding process. Because the time required for the polymer to pack fully around region A was also observed to become longer than other housing locations as the housing thickness was reduced around the convolute regions, DuPont™ investigated other ways to reduce the packing time differential across the housing, thereby minimising the likelihood of any moulding defect formation.

Based on their knowledge and expertise, one approach DuPont™ chose was to ‘core’ the housing around region A, so that the package thickness was reduced and it corresponded to the wall thickness dimension around the convolutes, as shown in Figure 8.20. From additional simulation studies that were done to assess the benefit of coring the housing, the difference in the packing time in region A, with regards to other locations in the housing when the housing was cored, was observed to have been reduced. A plot illustrating the different packing duration at different locations across a 3 mm cored housing is illustrated in Figure 8.21. As can be seen from the plot, the packing time differential between region A and other housing locations was observed to be have been significantly reduced, compared to the 3 mm uncored housing, depicted in Figure 8.19.

As determined from the electrical simulation studies in section 8.3.1, because a housing thickness less than 3 mm was seen to be appropriate to prevent the maximum electrical field at the flange/housing interfaces being located at the flange tip, a housing design, that has been cored for moulding benefits and has a 3 mm thickness, was regarded to be appropriate for the 50 mm prototype. The final design of the 50 mm prototype is next presented in section 8.4.



**Figure 8.19: Packing time when  $t = 3$  mm**

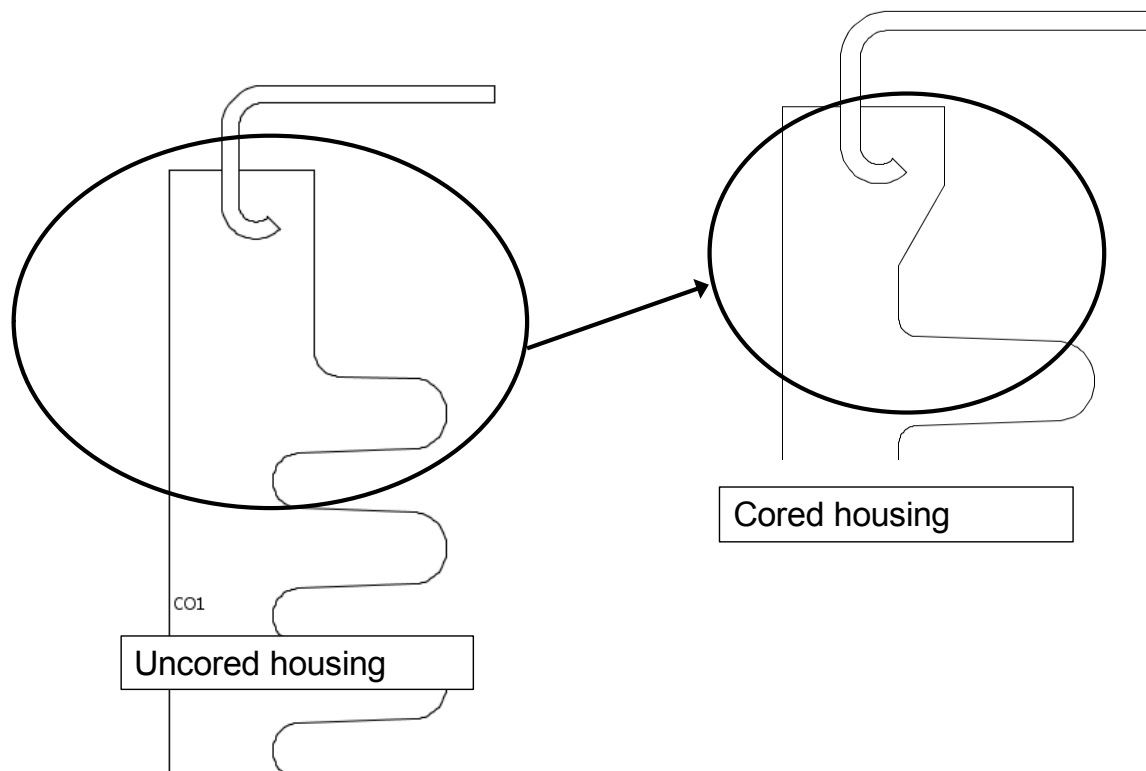


Figure 8.20: Illustration of a cored and uncored housing design

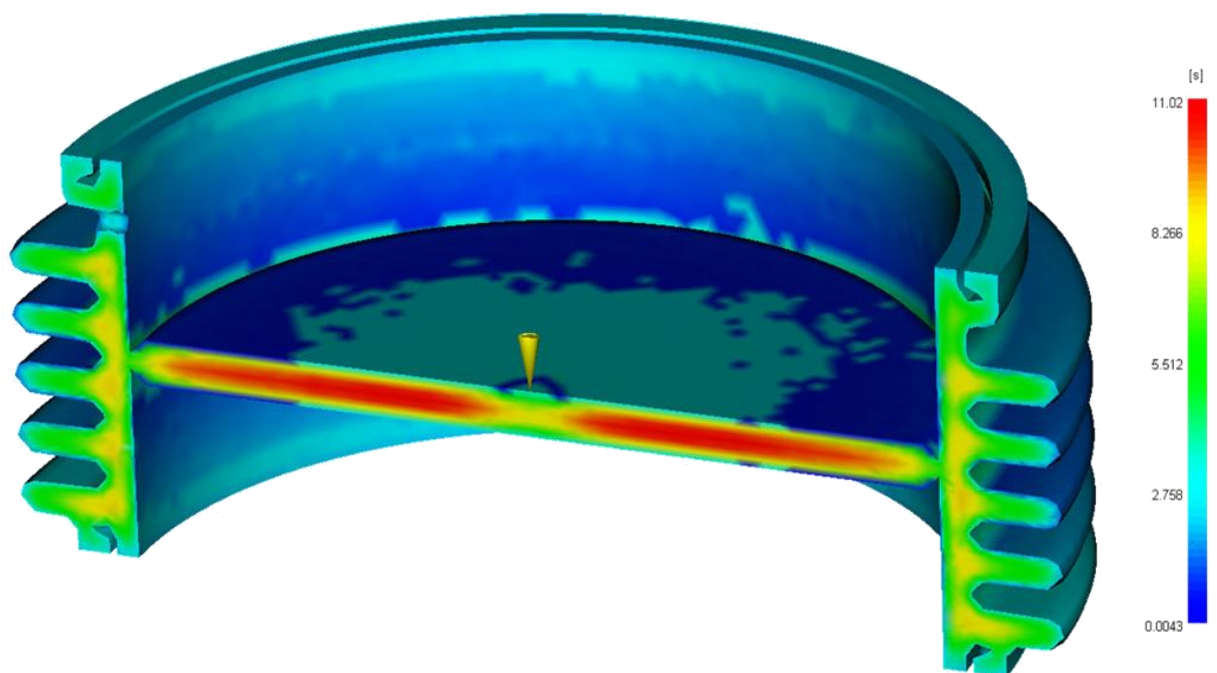


Figure 8.21: Packing time when the housing is cored ( $t = 3$  mm)

## 8.4 Final design of 50 mm prototype housing

From the electrical and moulding analysis results discussed in the previous sections, a final package design was subsequently chosen for the 50 mm prototype, and is illustrated in Figure 8.22. As highlighted in section 8.3.2, a housing, whose wall thickness was cored and had a 3 mm dimension, was considered to be the most appropriate for the 50 mm prototype. The position of the flange within the housing was chosen to be 1.5 mm from the inside edge, while the depth it protruded inside was taken to be 2.0 mm based on the electrical simulation studies described in section 8.2. In order to fit the assembly in the cold-welding assembly jig at Dynex, the lower (i.e. 5th) convolute located near the anode end of the housing was also required to be modified, so that its outer radius was reduced from 35.4 mm to 33.3 mm.

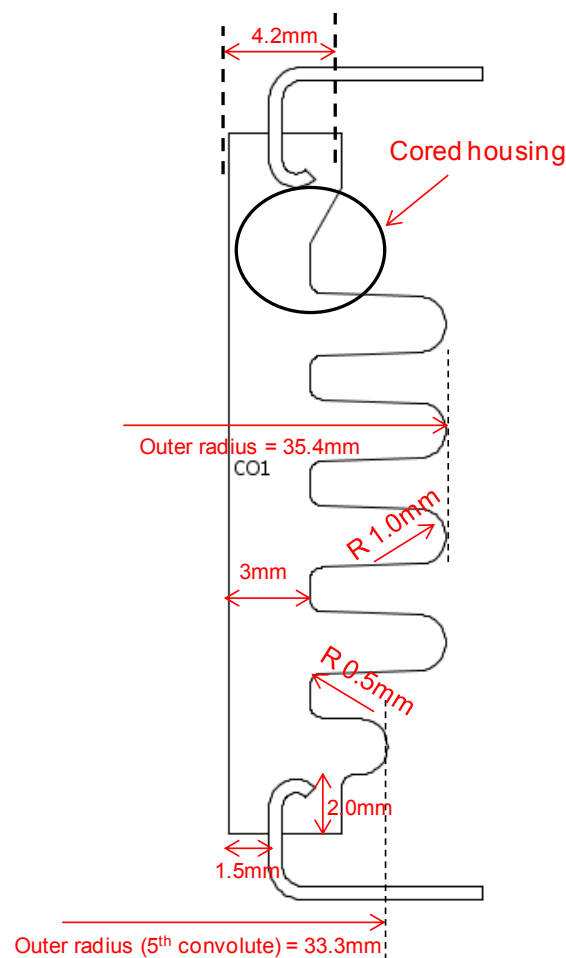
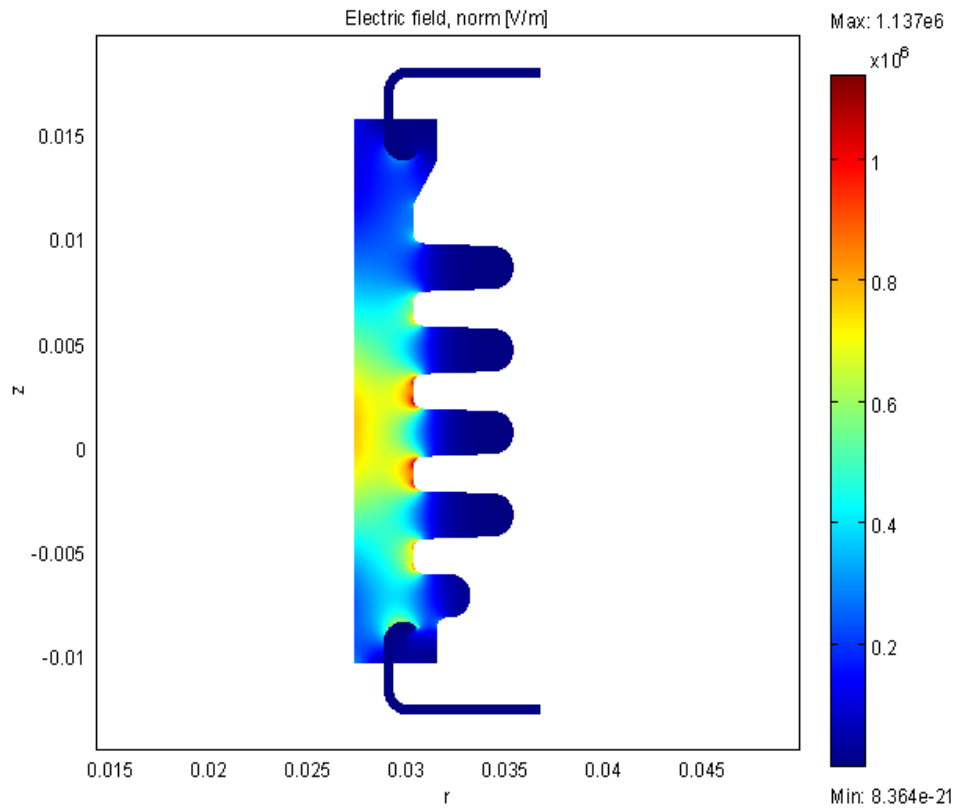


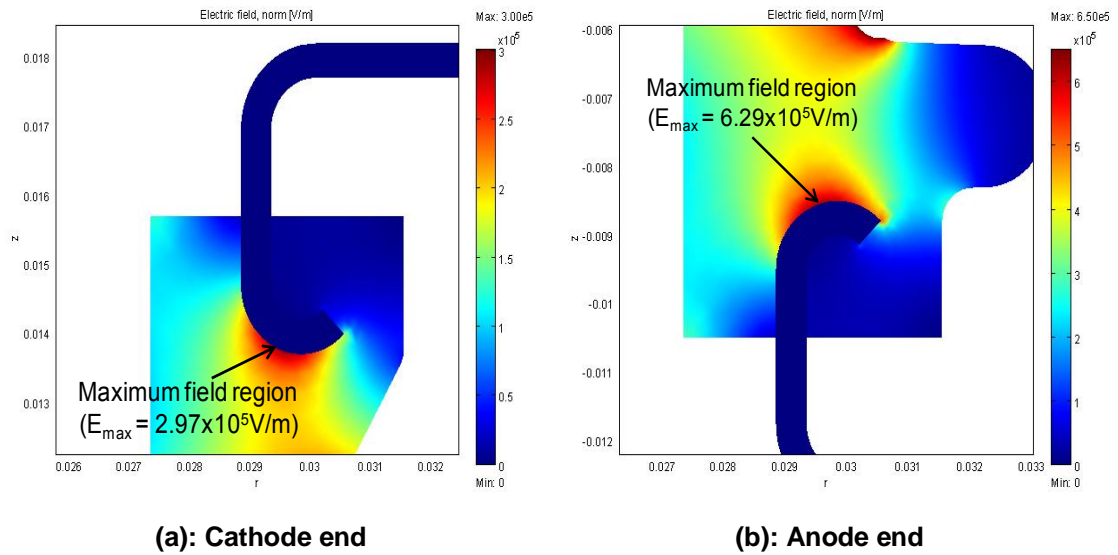
Figure 8.22: Finalised housing design of 50mm prototype

Additional moulding and electrical simulation studies performed by DuPont™ and Loughborough University respectively, found the proposed design for the 50 mm prototype to be appropriate from both the moulding and electrical criteria. For instance, because no pronounced packing time differentials were observed from the moulding simulations across the package, the component was considered to be able to pack fully, and occurrence of any moulding defects was regarded to be unlikely. On the other hand, as the maximum electric field regions at both the anode and cathode end contact regions were observed to be located along the flange curvature, the likelihood of the prototype housing failing due to partial discharge was also concluded to be low. Contour plots showing the electrical field distribution across the package, and around the flange/housing contact regions are respectively shown in Figures 8.23 and 8.24.

Further to determining the final 50 mm prototype design, the mould tool used to manufacture the polymer housing was then developed by DuPont™, before a number of prototypes were successfully manufactured for use in subsequent accelerated life tests to study the prototype reliability. A photo depicting an example of the 50 mm prototype that was successfully manufactured and delivered by DuPont™ in the NEWTON project is shown in Figure 8.25.



**Figure 8.23: Electrical field distribution across the finalised 50 mm prototype design**



**Figure 8.24: Electrical field distribution around the cathode and anode end flange/housing contact regions in the final prototype housing**



**Figure 8.25: Photo of the manufactured 50 mm prototype**

## **8.5 Conclusion**

The simulation studies described in this chapter has focussed on the different geometrical parameters of the thyristor housing to assist the 50 mm prototype development. The housing parameters that were here studied included the housing convolute design, the flange depth and its position within the housing, and also the housing wall thickness. These parameters were identified because if incorrect, they could result in electrical-stress driven failures and occurrence of moulding defects, such as voids, warpage, in the package. To reduce the likelihood of formation of such defects, a 2-stage study (stage 1 & 2) was performed to investigate the different critical parameters influence.

In stage 1, the influence of varying the flange depth, its position within the housing, and the convolute shapes on the electrical performance of the polymer housing was studied to benchmark an initial housing design. These studies were based on a 4 and 5 convolute housing configuration. In stage 2, the package design benchmarked from stage 1 was further refined from both an electrical and moulding performance perspective. Injection moulding simulation studies were here performed by DuPont™ using the Moldflow FE software in parallel with the electrical simulation studies carried by



Loughborough University to determine the appropriate wall thickness dimension, before the design of the 50 mm prototype housing was finalised.

From the electrical simulation studies in stage 1, the maximum electric field magnitude at the cathode and anode contact region was seen to decrease, when the flange position (i.e. its location from the housing inner edge) was increased in both the 4 and 5 convolute housings. However, for certain flange locations in the 4 and 5 convolute housing, a comparatively higher electric field that corresponded to the maximum electric field region being located at the flange tip was observed. This occurred when the flange was located near the inner edge of the housing. When the flange position was increased to be further from the inside housing edge, the maximum electric field region was seen to move away from the flange tip to occur along the curvature of the curved flange, causing the electric field magnitude to decrease. As a result of this study, it was deduced for the maximum electric field region at the interface region to be located along the flange curvature, the insert should be located at an appropriate distance away from the inner edge of the housing, e.g. in the middle of the package. To ensure the appropriate flow of the polymer around the inner region of the curved flange during the moulding process, at least a 1 mm spacing between the flange tip and outer edge of the housing should also be maintained when selecting the flange location.

When the flange depth was varied in the 4 and 5 convolute housings, the electrical field variation was also observed to be similar in both packages. The field magnitude at the contact region was observed to increase at both the cathode and anode ends, when the depth the flange protruded inside the package was increased. As in the case of the flange position variation, higher electric fields corresponding to the maximum field region at the flange tip was also observed in the 4 convolute housing. These higher field magnitudes were actually observed to be influenced by the relative position of the flange tip and housing convolute corners. The high electric field magnitude was noticed when the flange tip was located at a depth that was either lower or equal to the height of the bottom convolute corner. When the insert depth was increased beyond the height (from the housing ends) of the convolute

corners, the maximum electric field region was seen to be along the flange curvature. As a result of this study, an insert located ideally at a height greater than the convolute corners was also concluded to be an appropriate depth location of the flange so as to ensure the maximum electric field location along the flange curvature.

Together with these, the influence of the convolute design on the electric field in the housing was also studied in stage 1. The convolute configuration was here modified by varying the radius of curvature around their corners and the electrical performance of the housing studied. For this study, three housings (A, B and C) having different radius of curvatures were studied, namely (1) package A had 0.5 mm radius of curvature around its corners, (2) the convolute corners in package B had no rounded corners, (3) housing C had a 0.85 mm radius around its corners. When the electric field magnitude within the three housings was compared, the field magnitude around the convolutes in package B (no rounded convolute corners) was observed to be lowest, while the highest field magnitude was observed around the 0.85 mm dimension convolute corner.

From the stage 1 simulation studies, a preliminary housing that comprised of 5 convolutes having a 1 mm radius of curvature around its corners and its flanges located at a 2.0 mm depth and 1.5 mm position was selected for further studies in stage 2. Although the electric field magnitude within the housing with no rounded corners was seen to be lowest, the benefit a 1 mm convolute radius offered was the mould tool to manufacture the polymer housing was regarded to be comparatively easier to fabricate. Another advantage the 5 convolute housing also provided compared to the 4 convolute configuration was the tracking distance along its exterior package surface between the anode and cathode ends was higher than a 4 convolute housing. Such a feature would reduce the probability of the housing failure due to tracking along its exterior.

In stage 2, the influence of varying the wall thickness of the package was studied from a moulding and electrical performance criteria. When the wall

thickness of the benchmarked housing design was reduced across the convolute area between 2.0 mm and 4.2 mm dimensions, the electric field magnitude at the cathode and anode contact region was observed to decrease. The maximum electric field region was observed to be located at the tip region of the flange for the housing having thicknesses greater than 3.5 mm. On the other hand, as the wall thickness was reduced below 3.5 mm, the maximum electric field region location was observed to move from the flange tip to the insert curvature and cause the field magnitude to decrease. Because such change was again observed to be due to the position of the housing convolute corners, a housing having a wall thickness less than 3.0 mm was concluded to be appropriate. On the other hand, from the injection moulding simulation studies performed by DuPont™, a higher packing time was also observed around a region that was below the cathode end flange/housing interface region and above the first convolute from the cathode end. Because such occurrence can lead to moulding defects formations, such as voids and shrinkage, the housing was 'cored' so that occurrence of these flaws could be minimised. In the 'cored' housing design, the wall thickness above the first housing convolute at the cathode end was reduced so that it corresponded to the wall thickness dimension around the housing convolutes.

Following subsequent electrical and moulding simulation studies, the design and dimensions of the 50 mm prototype were finalised before it was successfully manufactured. The wall thickness of the prototype housing was 'cored' and had a 3 mm dimension. The position of the flange along the housing was chosen to be 1.5 mm, while its depth it protruded inside was taken to be 2.0 mm based on the electrical studies that were performed.

## **9 Thermo-mechanical study of the 50mm prototype housing**

### **9.1 Introduction**

As highlighted in previous chapters, the reliability of the thyristor housing, along with the integrity of the electrical connections between its different components, e.g. the molybdenum discs and copper pole pieces, are critical to prevent device failure during operation. In previous chapters, the simulation studies presented were performed in order to study the electrical performance of the polymer-based thyristor housing and to assist in the development of a 50 mm prototype for the NEWTON project. These studies, which should also be applicable to the development of polymer housings for other device sizes in the future, also aimed at preventing failure of the package due to electrical stress driven failures, such as partial discharge and dielectric breakdown. In this chapter, thermo-mechanical based studies are described so as to study the reliability of the 50 mm prototype developed in the NEWTON project.

Thermo-mechanical stresses normally occur due to a mismatch in the thermal expansion when the temperature is changed across materials of either a component or an assembly having different thermal coefficient of expansion (CTE). They have been observed to be a major cause of failure for different electronic packages, e.g. Tounsi et al., 2004 who presented a coupled electrical and mechanical simulation method to predict the thermo-mechanical stresses that are responsible for the MOS power modules failure, and Radivojevic et al., 2006 who performed accelerated thermal cycling tests to locate the most vulnerable parts in Thin & Fine Ball Grid Array (TFBGA) packages and predict their failure rates. In the case of the thyristor housing which consists of the polymer material and the nickel-plated copper inserts, because these components have different CTE values, thermo-mechanical stresses are likely to be encountered as a result of temperature changes. As

observed from studies by Xue et al., 2008 and Lin et al., 2003, these can lead to defects such as delamination and crack formation. For the NEWTON thyristor housing, events where temperature changes are likely to be encountered are: (1) at the end of the moulding process where thermal stresses will develop when the housing is cooled back to ambient temperature, (2) service conditions when the thyristor device is periodically turn on and off, and (3) during environmental changes the device will experience during transportation and storage. These can lead to either failure of the housing over time when it is exposed to the different temperature cycles during its operation lifetime, or sudden failure when it is exposed to above normal temperature levels.

To understand the thermo-mechanical performance of the electronic device and reveal appropriate information about its mechanical integrity (thus its reliability also), cycling between different temperatures is performed (de Lambilly et al., 1993). The two main types of tests used to accelerate thermal aging include temperature and power cycling. In temperature cycling, the device is cycled between two preset temperatures in a temperature chamber. In power cycling, the temperature change is obtained by generating varying energy losses inside the module.

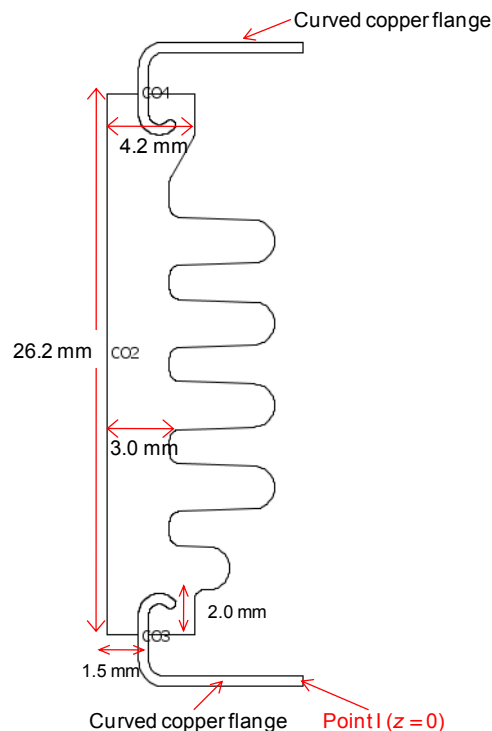
The thermo-mechanical reliability of the 50 mm prototype was assessed by both simulating and experimentally cycling the housing between two temperatures. FEA technique was initially used to study the internal stress distribution over a range of temperatures and identify likely areas of failure (discussed in section 9.2). This was also complemented by a series of experiments whereby samples of the manufactured 50 mm prototype housing was exposed to a number of temperature cycles between -40 °C and 125 °C to investigate its quality (reviewed in section 9.3).

## 9.2 Thermo-mechanical simulation

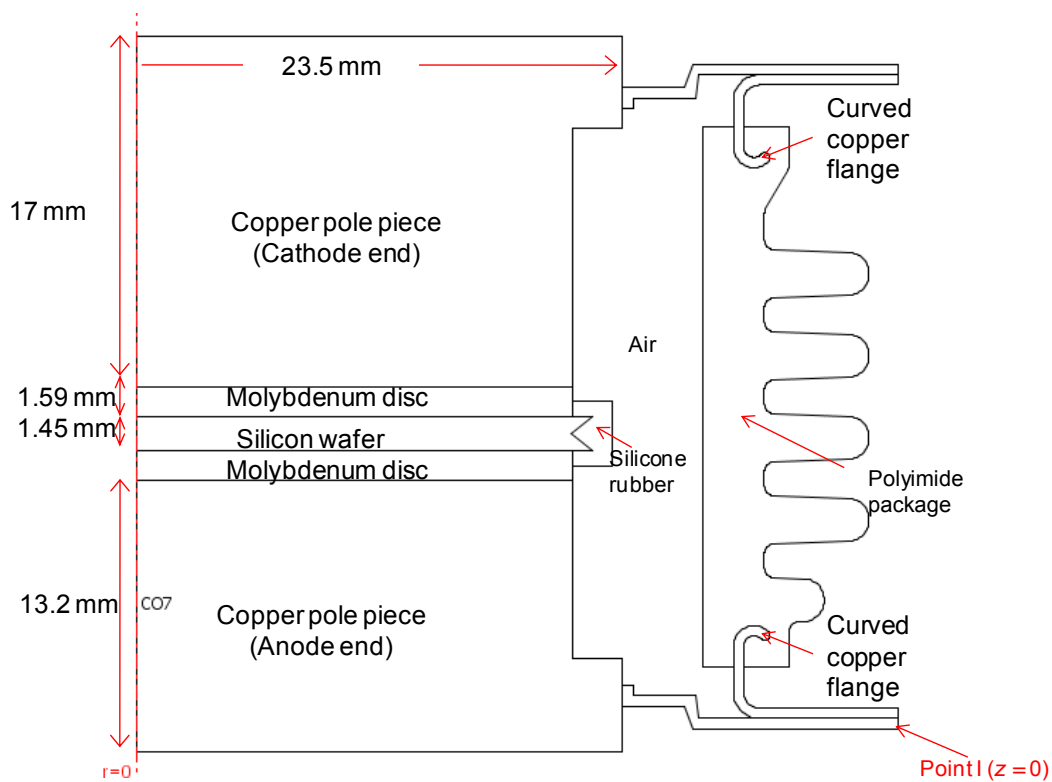
Together with temperature cycling experiments, widespread studies have also been done in the past using FEA to analyse electronic package failure due to temperature changes and to study the stress distribution within. The main objective of the thermo-mechanical investigation performed on the 50 mm prototype and described in this section was to identify potential failure sites inside the housing due to temperature changes. Together with this, an attempt to predict the onset of plasticity of the polyimide housing material was also investigated. As in the case of the electrical simulation studies, because the thyristor housing is axially symmetrical, a 2D axisymmetric finite element (FE) model was built for the thermo-mechanical simulation studies to again take advantage of the geometrical symmetry. Comsol Multiphysics was used to compute the thermal stresses. The FE model geometries used for this study are shown in Figures 9.1 and 9.2. Figure 9.1 represents the manufactured prototype packages (FE model A) consisting of the moulded polyimide package body and the copper flanges. This model was selected for study so that the thermal stress that occurs only due to expansion of the metal flanges and polymer material can be studied when the temperature is varied. On the other hand, to investigate potential stress transfer across the housing due to other components of the assembled thyristor and compare the thermal stress level due to temperature variation, an assembled thyristor device with the copper pole pieces welded to the polyimide housing flanges was also studied – FE model B (Figure 9.2). It should be noted instead of the silicone gel that was used for the electrical studies and is considered the appropriate filler material for the polymer housing, air was selected to be present inside the housing cavity of the assembled device. This was because an appropriate method to dispense the silicone gel inside the housing cavity was not identified in this project. By considering the housing cavity of the FE model and that of the assembled prototype to be comprised of air, an appropriate comparison of the thermo-mechanical performance of the prototype housing would be possible through both simulation and experimental studies. As highlighted by Moore et al., 2001, because high tensile or shear stress

regions initiate delamination and provide a site for crack growth, identification of the occurrence of such areas inside the package was an aim of this simulation study.

In the temperature cycling test, the entire package are exposed to sudden temperature changes at very rapid rate. This can potentially cause extreme temperature gradients to occur within the device and result in high thermo-mechanical stresses which are undesired and can precipitate the failure of the device. In the temperature cycling test, because the occurrence of such temperature gradient resulting from the rapid temperature cycle was not studied in depth, for the FEA studies a uniform spatial temperature distribution was assumed across the whole FE model when the temperature was changed. Together with this, a mechanical constraint was also applied at point I in FE models A and B (Figures 9.1 & 9.2) to prevent displacement along the vertical axis, i.e.  $z = 0$ . For this study, because the simulation results were also found to be mesh independent, both FE models were meshed using the default second order Lagrange elements to simulate the effect of temperature change in the package.



**Figure 9.1: Model A – polymer housing & copper flange only**



**Figure 9.2: Model B – assembled device**

To investigate the thermal stresses induced in the package and identify potential failure locations, a purely elastic FEA study was first performed at the  $-40\text{ }^{\circ}\text{C}$  and  $125\text{ }^{\circ}\text{C}$  temperature extremes required by the device specifications. The tensile modulus and CTE used for the different subdomains of the two FE models are as shown in Table 9.1. As the visco-elastic properties of the selected polyimide grade for the housing were not available, temperature-dependent linear elastic material property values supplied by DuPont™ were instead used for the modelling. A constant coefficient thermal of expansion value for the polyimide was also used for the simulation, although its value could probably change with temperature in practice. This was because no data was available at this stage of the project to be included in the simulation.

Following the moulding process, as the polymer housing will cool from its moulding temperature, residual stresses will normally develop inside the polymer housing. A ‘stress-free’ state, where no residual stresses are present



in the polymer package, was thus necessary to be identified for the thermo-mechanical simulations. For this study, this state was considered to occur at 210 °C, which was the moulding temperature for the 50 mm prototypes. As suggested in earlier section of this chapter, to identify the regions where delamination is likely occur within the housing, the normal and shear stress parameters were studied, whilst to predict the onset of plasticity of the housing, the von Mises stress was analysed - the von Mises stress being a scalar function of stress tensor which allows the onset and amount of plastic deformation under multiaxial loading conditions to be predicted from the yield strength value measured in a simple uniaxial tensile test (Abdullah et al., 2009).

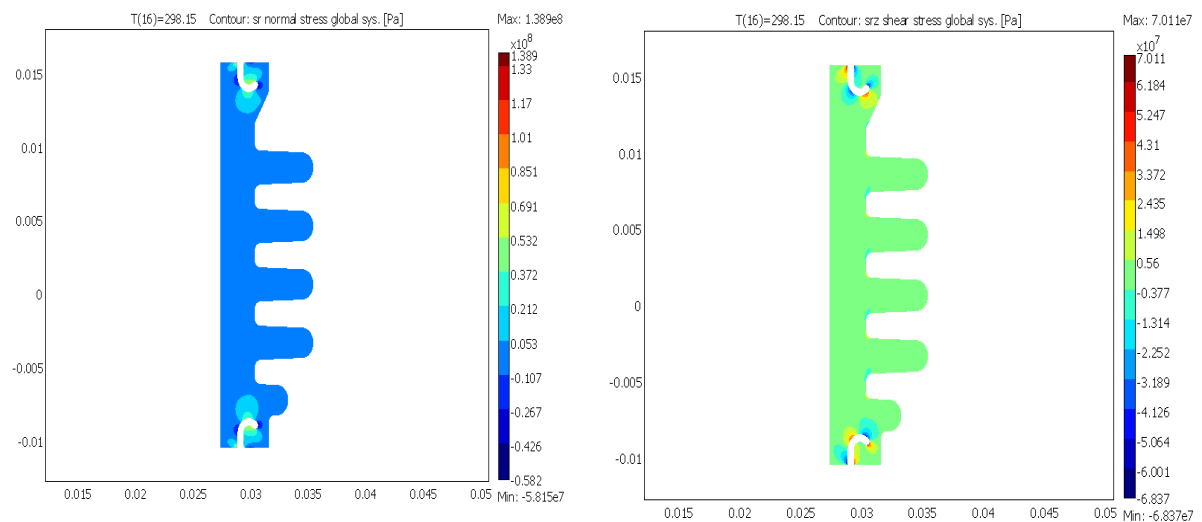
	<b>Young's modulus/MPa</b>	<b>Coefficient of thermal expansion (CTE)/K<sup>-1</sup></b>
Polyimide polymer	10200 (-40 °C) 10200 (23 °C) 6500 (100 °C) 6000 (150 °C)	52x10 <sup>-6</sup>
Copper flange/pole piece	117000	16.9x10 <sup>-6</sup>
Molybdenum disc	329000	4.8x10 <sup>-6</sup>
Silicon wafer	185000	2.6x10 <sup>-6</sup>
Silicone rubber		8.1x10 <sup>-6</sup>

**Table 9.1: FE models A and B subdomain properties**

### 9.2.1 Simulation results & discussion

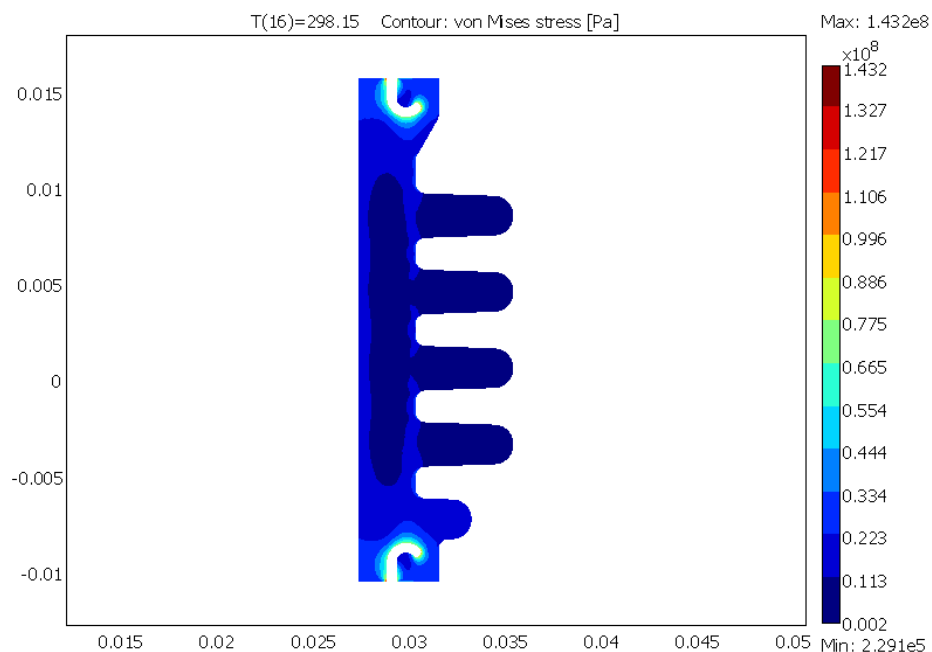
Contour plots of the normal stress along the horizontal *r*-axis (which also represent tensile and compressive stresses), the shear and the von Mises stress, when the temperature is reduced from the stress-free state (210 °C) to 25 °C (298.15 K) for the housing model, are shown in Figures 9.3 (a) to (c). As can be seen in these plots, localised regions of high normal and shear stress were observed to occur at both the cathode and anode ends flange/housing interface regions - a close-up view of the normal and shear stress distributions around the cathode end contact region can actually be

observed in Figures 9.4 (a) and (b). Because delamination and crack growth defects are likely to originate from these localised normal and shear stress regions, the flange/housing interface regions at both the cathode and anode ends were thus regarded to be likely failure sites in the package when the temperature is varied.



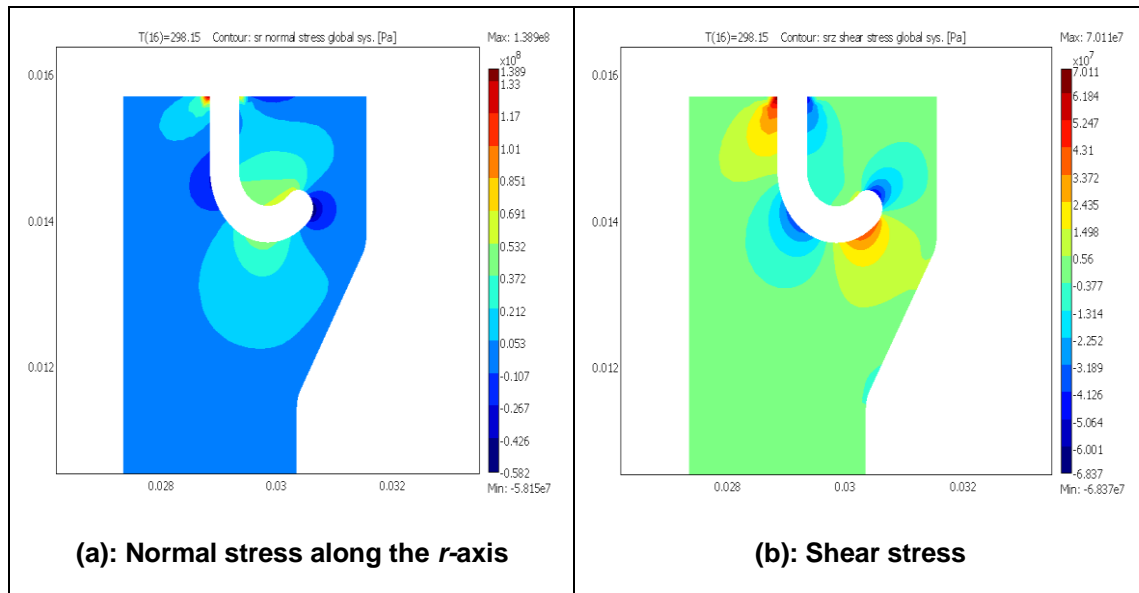
(a): Normal stress across the housing  
(horizontal  $r$ -axis direction)

(b): Shear stress

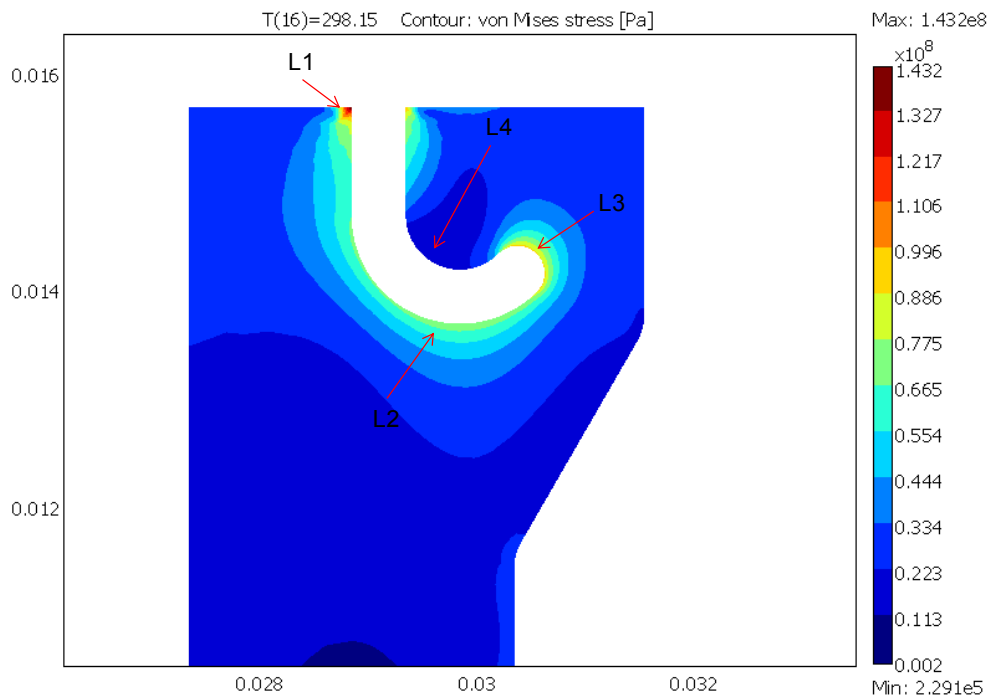


(c): Von Mises stress

Figure 9.3: Contour plots of stresses across the polymer housing when the thermal load is reduced from 210 °C to 25 °C



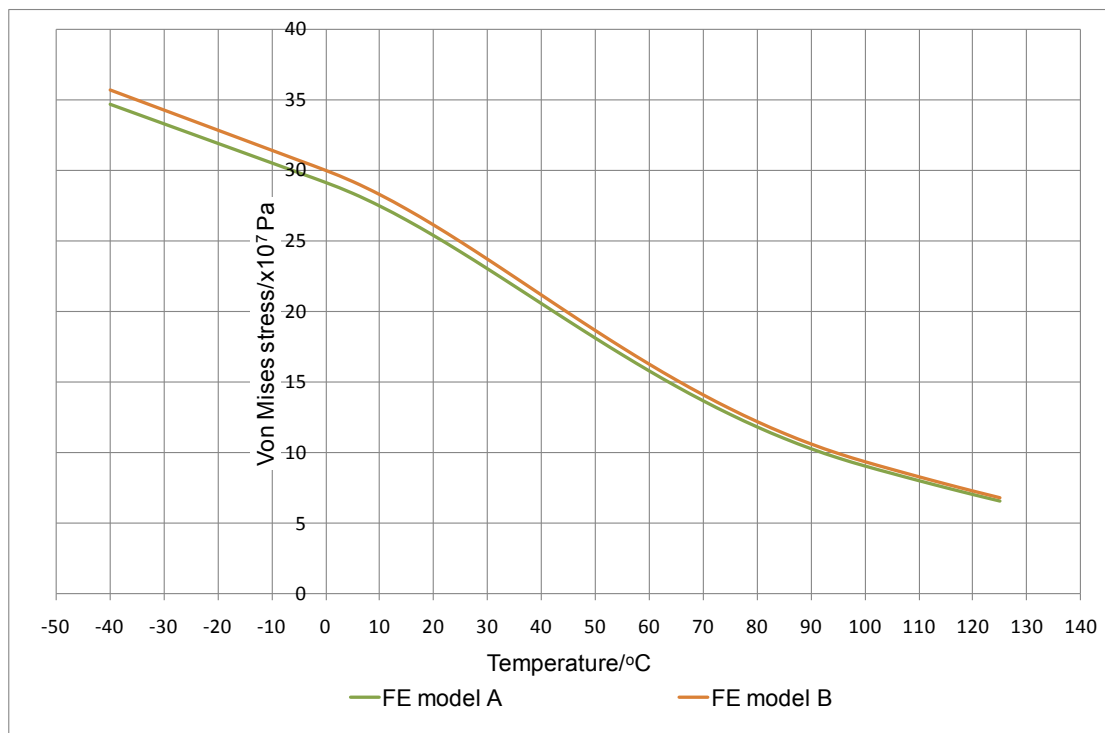
**Figure 9.4: Zoom-in contour plots of the normal and shear stress around the flange/housing interface**



**Figure 9.5: Von Mises stress contour plot across the flange/housing interface region**

The von Mises stress distribution around the cathode end flange/housing contact region is also depicted in Figure 9.5. In this case, the highest von Mises stress magnitude was observed to occur at location L1. The magnitude

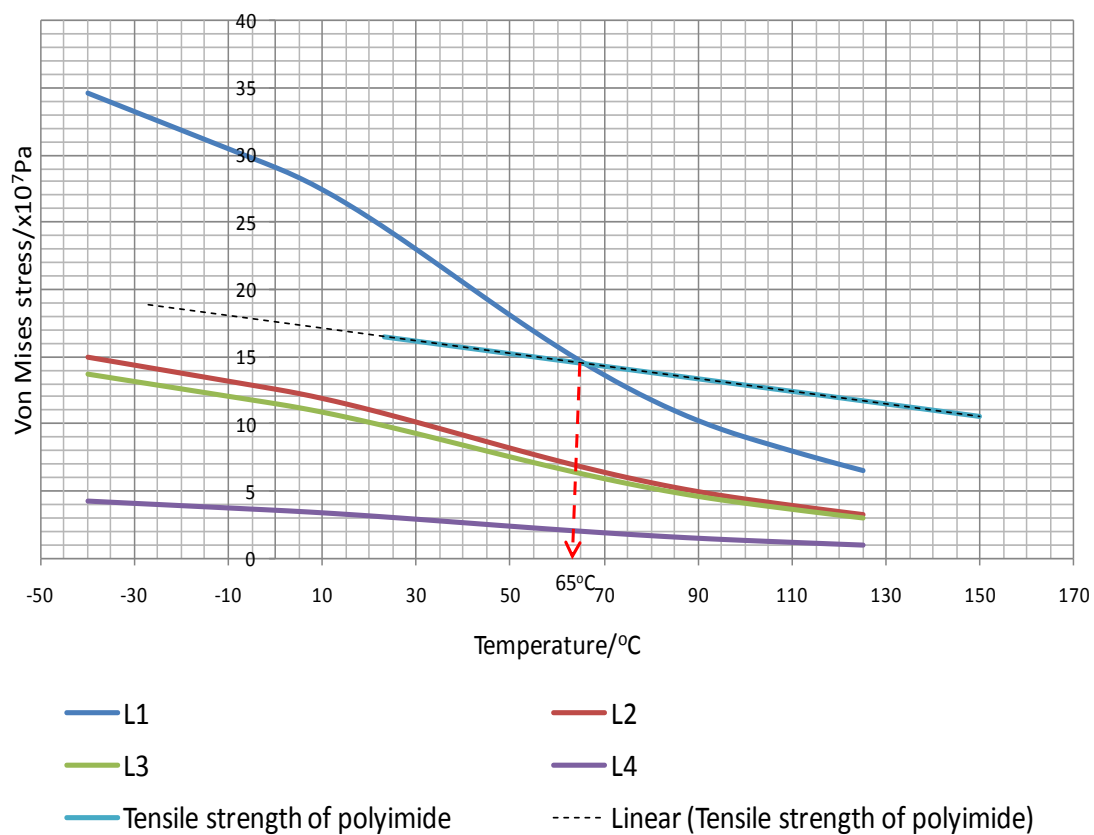
of the von Mises stress in the housing of both FE models A and B was observed to increase when the thermal load was reduced from the 'stress-free' state to 125 °C and then to -40 °C. The variation of the von Mises stress at location L1 in the housing is illustrated in Figure 9.6. As can be seen from the graph, the highest von Mises stress magnitude was observed to occur at a temperature of -40 °C. The graph also illustrate a comparative variation of the von Mises stress at the same location in the housing of FE model B. From the graph, no significant change in the von Mises stress magnitude was observed when the housing is assembled with the other components, thus suggesting expansion of the different components of the assembled device does not contribute any significant additional stresses to those that occur in the housing as a result of the temperature change.



**Figure 9.6: Variation of the von Mises stress at housing location L1 when the temperature is changed across FE models A and B**

To predict the onset of the plasticity in the polymer housing, the von Mises stress were also studied at locations L2, L3 and L4 across the housing interface region in model A (Figure 9.5) and then compared with the tensile strength of the selected polyimide polymer used for the housing. Because the

yield criterion of the selected glass-filled polyimide polymer is also unknown at this stage of the project, the von Mises yield criterion was here chosen to predict the onset of plasticity. According to the von Mises yield criterion, yielding starts to occur when the von Mises stress exceeds the material yield strength calculated from the results of a simple tensile test. For this study, the tensile strength of the polyimide material was taken to be 165 MPa at 23 °C and 106 MPa at 150 °C (as provided by DuPont™), and a linear variation of the tensile strength with temperature between these values was assumed.



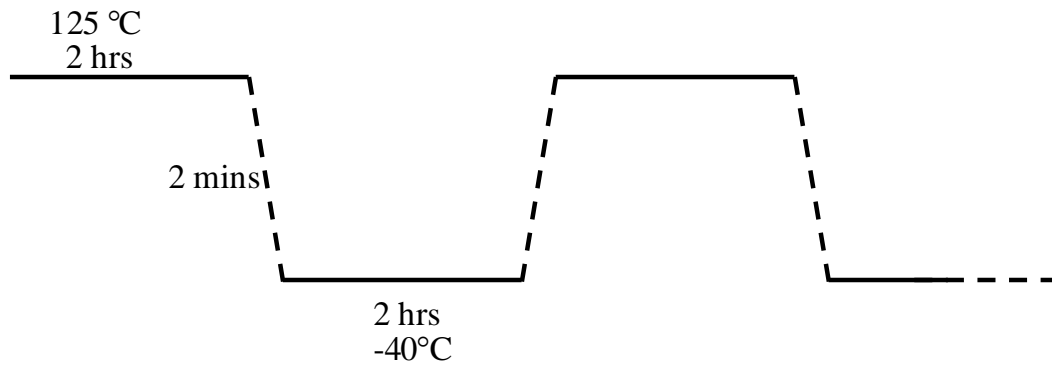
**Figure 9.7: Von-Mises stress change due to temperature change across housing locations L1, L2, L3 and L4**

Figure 9.7 illustrates the von Mises stress variation against the tensile strength of polyimide material at housing locations L1 - L4, when the package temperature is varied. As can be seen from the plot, when a linear elastic behaviour was assumed for the polyimide material, the limiting temperature, where plastic flow starts within the housing, was 65 °C at location L1 only. Because the von Mises stress was observed to be lower than the yield

strength of the polymer across the -40 °C and 125 °C temperature ranges, plastic yielding of housing was considered to unlikely occur at regions L2, L3 and L4. However, it should be noted the levels of stress predicted in this study could be either lower or higher than what actually occurs in practice. This would then change the limiting temperature for plasticity at the various housing locations. The present limitation in the predicted value is because the physical properties of the polymer have not been accurately measured at this stage of research. The linear elastic model assumed for this study is likely to deviate as a result of the shrinkage and the orientation of the glass fibres in the polyimide polymer, due to the moulding process, which are unknown at this point of the project. Further investigations will be required in this area in the future to predict more accurately the temperature limit for plasticity onset. By predicting this temperature, the likelihood of degradation of the polymer material and delamination at the housing interfaces could be minimised to prevent early failure of the package in the future.

### **9.3 Temperature cycling experiment**

As highlighted in earlier section of this chapter, the temperature cycling (TC) test performed on the 50 mm prototype was conducted according to the IEC 60068-2-14 standard temperature profile, shown in Figure 9.8, where the high and low temperatures phases were maintained at a constant 125 °C and -40 °C respectively. The transition time between these two temperatures and the dwell (or exposure) time for this cycle were specified as 2 minutes and 2 hours respectively, while the test duration was 5 cycles. To achieve the required rapid temperature changes for this experiment, two separate environmental chambers were used, maintained at the two temperature levels. During the experiment, the housings under test were manually transferred between the chambers to complete the test cycles.



**Figure 9.8: Temperature profile for thermal cycling test**

To inspect the integrity of the housings, additional tests, namely partial discharge (PD) and dye penetrant, were also performed before and after temperature cycling. The partial discharge tests performed before the TC aimed to identify defects (e.g. voids or delamination) that may be already present in the housings following the moulding process, while the test repeated after cycling sought to investigate whether the electrical performance of the housings had degraded as a result of the different thermal exertions. The dye penetrant tests were performed to detect any other defects in the housing which although not giving rise to PD activity may lead to failure. This was initially performed on a batch of manufactured housings before the TC experiment so that any damage (such as delamination, surface crack) that might be present due to the moulding process could be identified. The test was again performed on the samples used in the cycling experiment to detect any visual degradation that resulted from cycling. The experimental procedures for the partial discharge and dye penetrant tests are described in sections 9.3.1 and 9.3.2 respectively, while the results of the thermal cycling test are outlined in section 9.3.3.

### **9.3.1 Partial discharge test approach**

Since the introduction of high voltage technology for the generation and transmission of electrical power, different studies have recognised partial discharge to be a harmful ageing process and failure cause for electrical

insulation, e.g. Mitic et al., 1999 who identified the metallisation edges and interfaces in silicone gel to be locations where partial discharge originates in IGBT modules, and among others Ahmed et al., 2001 who highlighted partial discharge to be a leading cause of cable system failure. IEC 60270 'High-voltage test techniques – Partial discharge measurements' actually defines partial discharge (PD) as a localised electrical discharge that only partially bridges the insulation between conductors and which may or may not occur adjacent to a conductor (CENELEC, 2001). It is in general a consequence of local electrical stress in the insulation or on the surface of the insulation which exceeds the limit of the insulating material. The partial discharge test is typically a non-destructive test and is used as a quality assessment tool to give information on the strength of the insulating material. Because the stress the insulation is exposed to during the PD test is likely to have an influence on the life expectancy of the material, a reasonable compromise between the applied stress to get reliable results and the lifetime reduction due to the test is normally sought during these tests (Gockenbach, 2001).

To measure the partial discharge activity of the 50 mm prototype housings prior to and after the temperature cycling experiment, the IEC 60270 test method was used. The PD activity was measured using a 'Biddle Series 27000' partial discharge detection system from Biddle Instruments at Dynex Semiconductor. In this test, as the amount of charge involved locally at the discharge site cannot be measured directly, IEC 60270 recommends the use of the apparent charge as the quantity to be measured (usually expressed in pC). The IEC 60270 refers to the apparent charge of a PD event being that charge which, if injected over a very short time between the terminals of the test object in a specified test circuit, would give the same reading on the measuring instrument as the current pulse from the PD activity.

Based on the operational stress levels and lifetime that the NEWTON thyristor is required to endure, the IEC 60270 standard recommends a partial discharge limit of 5 pC at 6 kV rms (8.5 kV peak) to assess the quality of the moulded housing. In order to study the polymer housing in greater depth, a higher partial discharge limit level of 5 pC at 8.5 kV rms (12 kV peak) was



opted. The PD test regime applied to each housing consisted of initially increasing the applied voltage up to 12 kV. As the voltage was gradually increased, the partial discharge inception voltage was noted when a discharge activity was observed at the minimum discharge level, i.e. 5 pC. The voltage was then further increased to the maximum specified voltage level and thereafter gradually decreased back to zero. As the voltage was reduced, the partial discharge extinction voltage, i.e. the voltage at which the discharge activity became less than the specified limit (5 pC), was also noted. According to the IEC 60270 standard, the partial discharge inception voltage is defined as the applied voltage at which repetitive partial discharges are first observed in the test object when the applied voltage to the object is gradually increased from a lower value at which no PD is observed. On the other hand, the partial discharge extinction voltage is the applied voltage at which the repetitive partial discharge activity ceases to occur in the test object when the applied voltage is gradually reduced from a higher value at which the PD activity has been observed.

### **9.3.2 Dye penetrant test procedure**

Dye penetrant testing (or liquid penetration test) is a widely applied inspection method used to locate surface-breaking defects, such as cracks or delamination, in metals, ceramics or plastics. The process operates on the principle that penetrant dyes are absorbed into the surface-breaking defects by capillary action to make the defects more visible. The first step of the penetrant inspection procedure typically consists of carefully cleaning the test object to remove all surface oil and contaminants. The dye is then applied to the surface and allowed to soak into the defects wherever they may be present. After soaking the dye is then removed from the surface, leaving only the dye that is trapped in the surface cracks. Finally, a powder-like developer is applied to the test object to draw the residual dye out of the cracks and make their presence visible (National Materials Advisory Board, 1983).

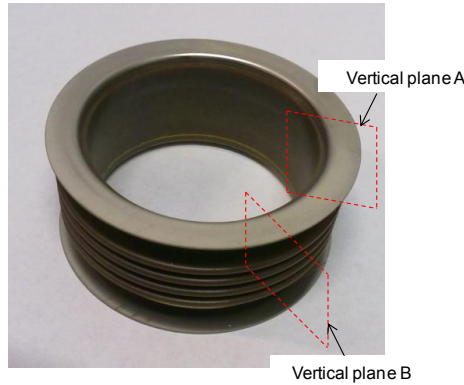
To identify the occurrence of any surface defects on the surface of the polymer housing, the conventional dye penetrant test procedure mentioned

above was not used. This is because the pre-cleaning step which involves using solvents to remove any dirt, oil or contaminant out of a defect could potentially degrade the polymer material when the housing surface is cleaned. Also, because the housing surface was complex (i.e. not flat), the probability for the dye to soak into any defect on the package surface was regarded to be low, thereby resulting in a test that has a decreased sensitivity. To detect any surface defect on the housing, a modified dye penetrant test procedure was thus used.

For the dye penetrant tests of the prototypes, a coloured dye, namely Epo-Color™ from Buehler®, which consists of an enhanced resin and hardener system, was thus used to mount the housing samples using vacuum impregnation process to identify the occurrence of cracks or delamination defects across its surface. Because the epoxy also appears bright red under darkfield or polarised light illumination, the Epo-Color™ offered the benefit of being able to clearly differentiate between the epoxy and materials of similar reflectance such as polymers and coatings.

The dye penetrant tests performed involved five key steps namely:

- in the initial 'sample preparation' phase, the housings were either sectioned vertically (e.g. along two vertical planes A and B as shown in Figure 9.9) before they were mounted, or studied as a complete part whereby they were mounted at both the cathode and anode ends to avoid 'secondary' stresses occurring at the flange/housing interfaces as a result of the sectioning process



**Figure 9.9: Illustration of the vertical planes along which the housing is sectioned for the test**

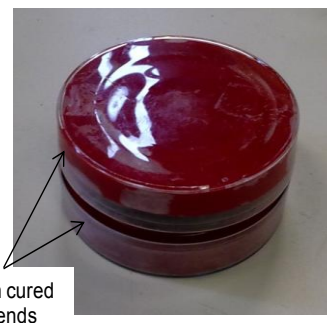
- the prepared samples under study were then vacuum impregnated with the coloured epoxy resin so that cracks or delamination cavities opened to the housing surface were filled with the resin. During this process, air that is entrapped in the specimen under study is first evacuated to enable the mounting compound to fill any pores or separation present in the sample
- after filling with the mounting compound, the vacuum was removed and the curing process of the test sample was initiated for 6 to 8 hours at room temperature
- after curing, housings that were potted at each end during the 'sample preparation' phase were sectioned
- the sectioned samples were then polished before they were inspected in detail under microscope

### **9.3.3 Results & Discussion**

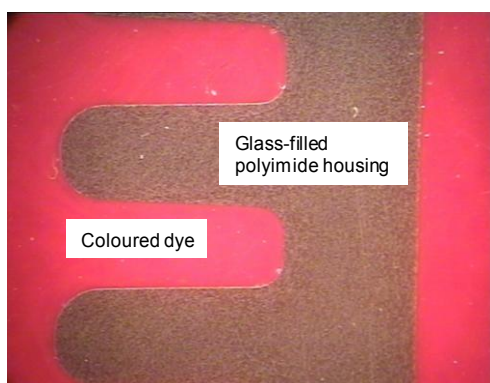
Figures 9.10 (a) and (b) illustrate examples of some mounted housing samples after curing. An example of a housing that was sectioned along the vertical planes shown in Figure 9.9 and then cured is shown in Figure 9.10 (a), while a prototype that was mounted at both the cathode and anode ends is depicted in Figure 9.10 (b).



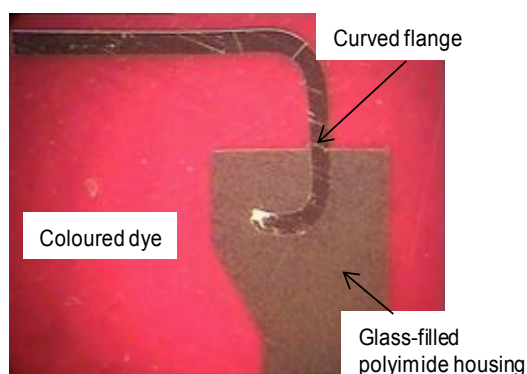
**(a): Photo of a sectioned housing after it has been mounted using Epo-Color resin**



**(b): Photo of a housing after it has been potted with the Epo-Color resin at both ends**



**(c): Illustration of the potted resin around the convolutes of the sectioned polyimide housing**

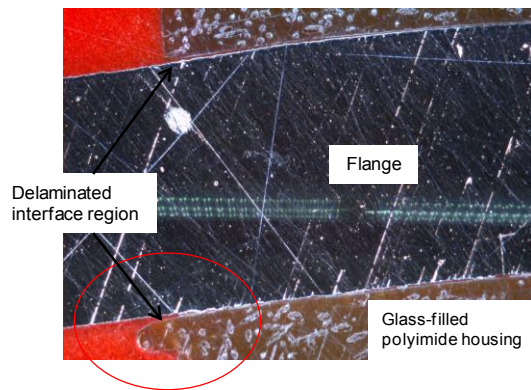


**(d): Photo of the potted resin around the flange/housing contact region of the sectioned housing**

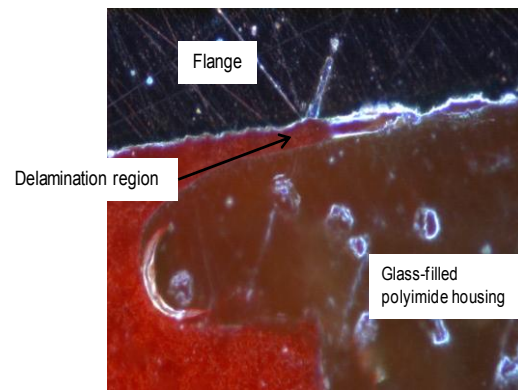
**Figure 9.10: Photos of mounted housing samples**

Photos highlighting the distribution of the cured coloured resin around the housing convolutes of the mounted sample in Figure 9.10 (a), and at the flange/housing interface region relating to the potted housing in Figure 9.10 (b) are also shown in Figures 9.10 (c) and (d). From detailed optical microscopic inspections that were performed on the manufactured housings after they were mounted with the epoxy resin, no cracks or defects were observed to be present along the housing surface area. However, delamination was seen to be present at the flange/housing interface regions at both the cathode and anode ends. In this case, the bright red epoxy resin was observed between the insert and polyimide housing. A photo highlighting the delamination region where the insert enters the housing is shown in Figure 9.11 (a), while Figure 9.11 (b) shows a close-up view of the circled delamination region in Figure 9.11 (a). Further studies around the contact

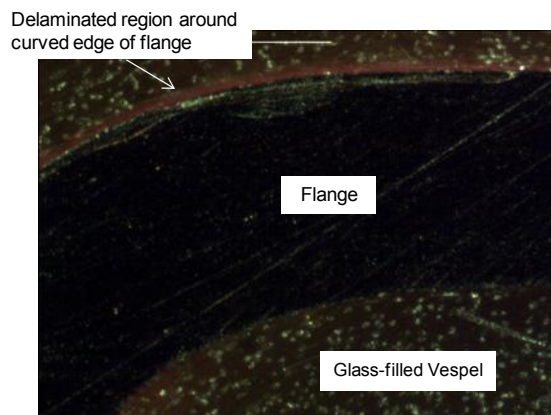
region also revealed the flange/housing separation to extend along the curved contour profile of the insert, as shown in Figure 9.11 (c). However, no such delamination was identified at the end of the curved flange (Figure 9.11 (d)). The causes for the occurrence of the observed delamination around the contact region have not been identified at this stage of the project. This may be due to a number of complicated issues related to the current injection moulding process parameters used for the housing moulding for example, or may be due to the surface finish of the flange also. To eliminate this defect, further investigations will be required in the future to identify the root causes before development of larger size housings is initiated.



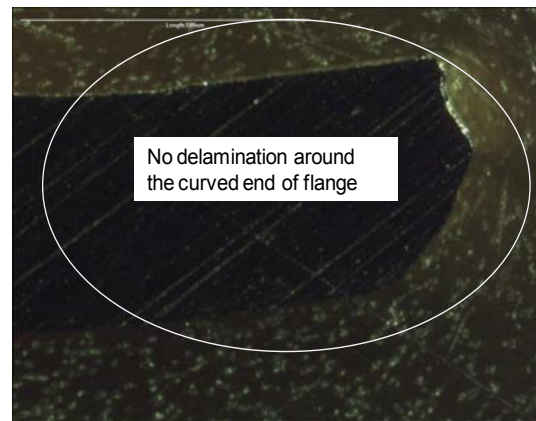
**(a): Delamination around the contact region where the insert enters the polyimide housing**



**(b): Zoom-in view of the circled delamination region in Figure 9.11(a)**



**(c): Delamination around the curved contour of flange**



**(d): Photo illustrating occurrence of no delamination around the end of curved flange**

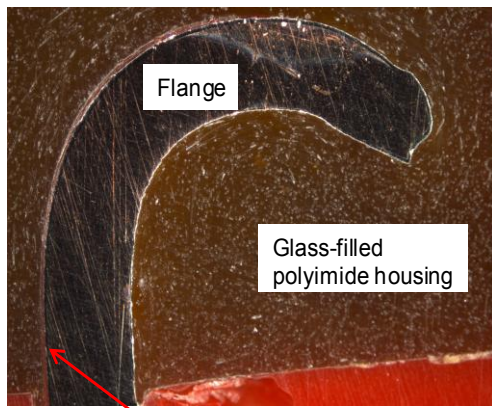
**Figure 9.11: Photos depicting the delaminated regions between the flange/housing interface before the TC experiment**

In the partial discharge test that was also performed before the TC experiment to assess the quality of the 148 prototypes manufactured in the project, a partial discharge activity of less than 5 pC was measured on all but one housing when the applied voltage was increased up to 12 kV. This suggested apart from one, the remaining 147 moulded prototypes did not contain any air voids that could potentially cause their failure when exposed to electrical stresses. These non-defect housings used were thus used for the different accelerated tests performed in the project, including the TC experiment described in this chapter.

For the TC experiment, 3 prototypes were used and exposed to the 5 temperature cycles between 125 °C and -25 °C, as illustrated in Figure 9.8. To identify any electrical degradation as a result of this test, the PD test was again repeated on three tested prototypes. When the voltage was increased up to 12 kV, a partial discharge activity of less than 5 pC was again measured in all three samples, thereby suggesting the polyimide housing had not degraded as a result of the cycling experiment.

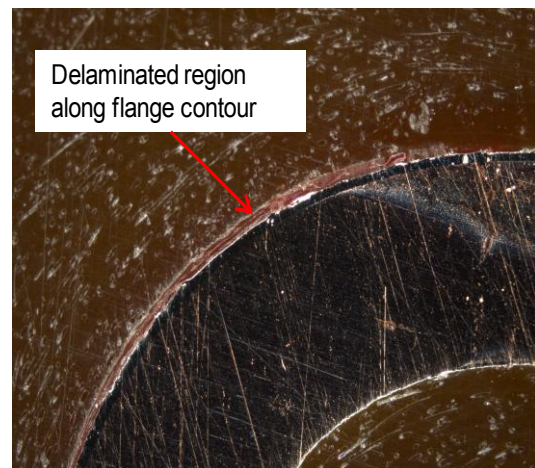
From the dye penetrant tests that were performed on the three tested prototypes after cycling and PD experiments, delamination patterns identical to those observed before cycling (Figures 9.11 (a) - (d)) were observed, i.e. no surface cracks or damage were observed along the housing convolute surface area and as observed for the as-manufactured samples, separation between the flange and polyimide polymer was again observed in the anode and cathode contact regions. Examples of some photos depicting the insert/housing separation in the tested housing can be seen in Figures 9.12 (a) - (c). Figure 9.12 (a) illustrates the delamination across the whole area of contact region, while Figures 9.12 (b) and (c) respectively depict close-up views of the interface region along the curved profile of the insert and at its end. As seen in Figure 9.12 (b), occurrence of delamination was observed to continue along the curvature of the insert, while no such separation was observed at the end of the flange (Figure 9.12 (d)). This suggests the tested polymer housings did not further delaminate (or physically degrade) as a result of the TC experiments.



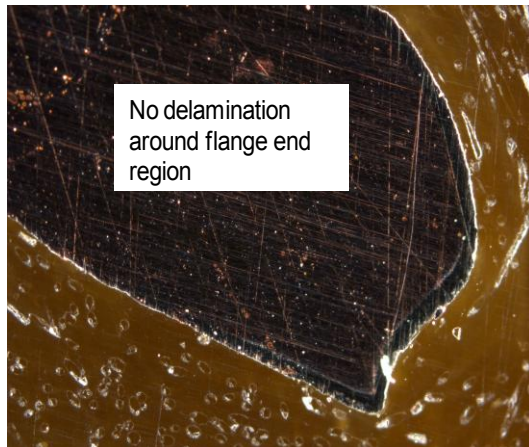


Delaminated flange/housing interface region

**(a): Photo depicting delamination across the contact region of the housing and insert**



**(b): Illustration of the insert and housing separation that has extended along the contour profile of the flange**



**(c): Photo depicting the contact region around the curved flange end**

**Figure 9.12: Photographs illustrating delamination regions at the flange/housing interfaces across tested housings**

## 9.4 Discussion

To investigate the quality of the manufactured 50 mm prototypes, preliminary studies designed to assess the thermo-mechanical performance of the housing have been described in this chapter. The manufactured prototypes were exposed to a temperature cycling test of 5 cycles between  $-40\text{ }^{\circ}\text{C}$  and  $125\text{ }^{\circ}\text{C}$ , and with dwell and transfer times of 2 hrs and 2 mins respectively.

This was also assisted by a computer modelling study using FEA to identify the likely failure locations across the package at the temperature extremes.

From the FEA studies, localised regions of high shear and normal stresses were observed to occur around the flange/housing contact regions at both the cathode and anode ends. Because different studies have shown cracks and delamination typically originate from such high stress locations, the contact regions at both the cathode and anode ends were regarded to be the most likely failure sites in the package when the temperature is varied. On the other hand, when the thermal load was changed from the 'stress-free' temperature (here assumed to be equal to the moulding temperature of the prototype, i.e. 210 °C) to 125 °C and then -40 °C, the different stress components, i.e. normal, shear, and von Mises, were all seen to increase with the highest stress magnitudes occurring at -40 °C.

In order to prevent early failure of the package during its service life, additional simulation studies were also performed to identify the limiting temperature for onset of plasticity of the polymer as a result of temperature changes that arises from the different manufacturing, storage, transportation and service conditions to which the housings are exposed. Based on studies whereby the polyimide housing was assumed to have linear elastic properties, the limiting temperature for onset of plasticity of the polymer was found to be 65 °C. It occurred only at the region where the flange contacts the polymer housing. Because the physical properties of the polyimide are influenced by the polymer material shrinkage and glass fibre orientation during the moulding process, and these have not been quantified, the computed 65 °C temperature for the plasticity onset is likely to deviate in practice. In-depth studies would be required in the future to more accurately predict the temperature for onset of plasticity in the polymer housing.

As part of a temperature cycling (TC) test programme, dye penetrant and partial discharge tests were performed before and after the experiments. The dye penetrant test that was performed before the TC experiment aimed to identify the presence of any delamination or surface cracks across the



moulded prototypes, while the partial discharge test assessed the quality of the moulded housings by identifying the presence of defects, such as voids or delamination, that may be present following the moulding process. In the initial PD test where the 148 prototypes manufactured by DuPont™ during the project were tested, only one housing was observed to have a PD activity greater than the 5 pC limit when it was exposed to the 12 kV peak voltage. This suggested the housing contained air voids that would lead to its failure when exposed to electric stresses. On the other hand, because a PD activity less than 5 pC was measured in the remaining 147 prototypes, air voids that could potentially cause catastrophic failure of the housing during service were considered to be absent. The prototypes used for the TC experiment were thus selected from this 'non-faulty' category. As a result of the dye penetrant test carried on a batch of the manufactured prototypes, occurrence of surface cracks or delamination was not observed around the surface area of the housing convolutes. However, occurrence of delamination at both the cathode and anode flange/housing interface regions was observed. This suggests limitations, that may be due to either the surface finish of the flange or the moulding process parameters and procedures used to manufacture the prototypes, currently exist. Additional studies would thus also be required in this area in the future to identify the root cause.

Following these tests, 3 prototypes, that were concluded to be free from potentially damaging air voids as a result of the PD test mentioned above, were used for the TC experiment. After the experiment, the PD and dye penetrant tests were again repeated on the tested housing. PD test were first performed to assess whether their electrical performance had degraded as a result of the different thermal exertions in the test, before the dye penetrant experiment was carried to detect any visual degradation resulting from the TC experiment.

The PD and dye penetrant tests indicated that the manufactured prototypes were free from significant deterioration, and they can be concluded to be reliable at this development stage. For instance, from the PD test, the electrical performance of the tested housings was not observed to have

degraded as a result of the temperature cycling experiments. Together with this, no further delamination or formation of any other defects within the housing bulk was also observed when the dye penetrant test was performed.

## **10 Design of a 125 mm thyristor package using the Taguchi Method of Experiment Design (TMED)**

### **10.1 Introduction**

From the electrical simulation studies described in Chapter 8, different geometric parameters of the housing were observed to have varying influence on the magnitude of the electric field. For instance, when the flange depth,  $d$ , was changed inside a 5 convolute housing between 3.5 mm and 4.0 mm, the increase in the magnitude of the maximum electric field located along the curvature of the flange was found to be greater than 0.1 MV/m at the anode end. On the other hand, when the anode end electric field magnitude was studied as a result of change in the flange position,  $f$ , between 1.50 mm and 2.00 mm in a 5 convolute housing, the decrease in the field strength was found to be less than 0.06 MV/m at the anode end.

Because different design parameters of the thyristor housing were observed to have varying degrees of effect on the electrical field magnitude within, their combined influences needed to be investigated through a series of FEA simulations. For this study, the Taguchi method of experimental design (TMED) approach was first used to understand the influence of the different housing parameters. As highlighted in Chapter 1, because fewer numbers and larger size thyristor devices are intended to be exploited in future high voltage schemes, the conclusion from this initial study was then applied to the design of a larger 125 mm diameter polymer package. The Analysis of Variance (ANOVA) statistical technique has also been used in the analysis of the experiment results to establish the optimum design factor combination for the electric field within the package to be low, and also estimate the contribution of individual design factors towards the electric field variation in the housing. These are discussed in the following sections, together with a review of the Taguchi method.

## 10.2 Taguchi Method of Experimental Design (TMED)

According to Roy, 1990, the origin of the Taguchi method (developed by Dr Genichi Taguchi in the 1950s) can be traced to the work of Sir R. A. Fisher in agricultural experimentation where he introduced the concept of factorial design of experiments in the 1920s. The factorial design of experiments is a technique of defining and investigating all possible conditions in an experiment involving multiple factors. In it, the total number of possible experiments,  $N$ , is equal to  $L^m$  where  $L$  is the number of levels for each factor and  $m$  is the number of factors involved in the experiment. A full factorial experiment design is normally manageable when a particular study involves a small number of factors and levels. However, they can easily become costly and time-consuming to perform when large numbers of factors and levels are considered. For example, an experiment involving 15 factors at 2 levels each will provide 32768 ( $2^{15}$ ) possible combinations to investigate. In these cases, a partial factorial experiment is helpful to simplify the experiment, since it considers only a fraction of all the possible combinations. However, different sets of partial factorial experiments are also possible when this concept is used to perform a study involving a large number of combinations.

In order to provide a simplified and standardised approach to the design of partial factorial experiments, the Taguchi method is used. It enables different investigators working on the same problem to use the same experiment design and obtain similar results. Since its early application to improve engineering experimentation at the Electrical Communication Laboratories (ECL) in Japan after the second world war, the Taguchi method has made successful inroads and been adopted by a number of major industrial organisations, e.g. Ford Motor Company, Xerox, etc. (Baker, 1990), and different areas of applications. In fact, various publications and textbooks are today available whereby the successful application of the Taguchi method in different fields is highlighted. Examples of some studies where the Taguchi method has been successfully applied include Palanikumar et al., 2009 who

assessed different factors influencing tool wear when glass fibre-reinforced plastics are machined, Anawa et al., 2008 who evaluated key parameters influencing the weld quality when dissimilar AISI 316 stainless steel and AISI 1008 low carbon steel plates are joined together using a laser beam welding process, and among others Bing et al., 2006 who used the Taguchi method and finite element method virtual experiments to analyse the effects of different forming parameters on the quality of parts manufactured by a tube hydroforming process.

According to Roy, 1990, although different views exist on the actual contribution of the Taguchi method to the field of statistical design of experiments (one view holds that the Taguchi method is a revolution, while others perceive the ideas proposed as not new), the key strength of the method lies within the philosophy proposed by Dr. Taguchi regarding quality and the procedure of carrying out experiments. His philosophy is based on three fundamental concepts which are as follows: (1) quality should be designed into the product and not inspected into it, i.e. quality improvement does not start during the production phase, but rather during the design phase of a product/process, (2) quality is best achieved by specifying a target value for a critical factor and developing processes such that it is immune to environmental factors and can meet the target value with little deviation, (3) the cost of quality should be measured as a function of deviation from the standard in terms of the overall life cycle costs (Roy, 1990).

The Taguchi method also differentiates online and offline quality control methods within the quality engineering systems, compared to the conventional quality control approach where all activities are focussed during the production stage only when it is used for a study. The offline quality control consists of activities that take place during the product planning, design and development stages and include system design, parameter design and tolerance design phases, as opposed to online quality control which include activities taking place during the production stage. The application of the Taguchi method normally involves four steps which are as follows (Peace, 1992):

- brainstorm the quality characteristics and design parameters important to the product/process;
- design and conduct the experiments. A standard set of orthogonal arrays (OA) are used here to accommodate different experiment situations. The steps involve selecting the appropriate OA, assigning the factors to the appropriate columns and determining the conditions for the individual experiments;
- analyse the results to determine the optimum conditions. This is normally done in a standard series of phases. First the main effects are evaluated to determine the influence of the factors. The optimum condition and the performance at the optimum condition are also determined from this stage. In the next phase, analysis of variance (ANOVA) is performed on the result to determine the relative influence of each factor;
- run a confirmatory test using the optimum conditions. This is done to confirm that the performance is the best and matches the performance predicted by the analysis.

### **10.3 Research methodology**

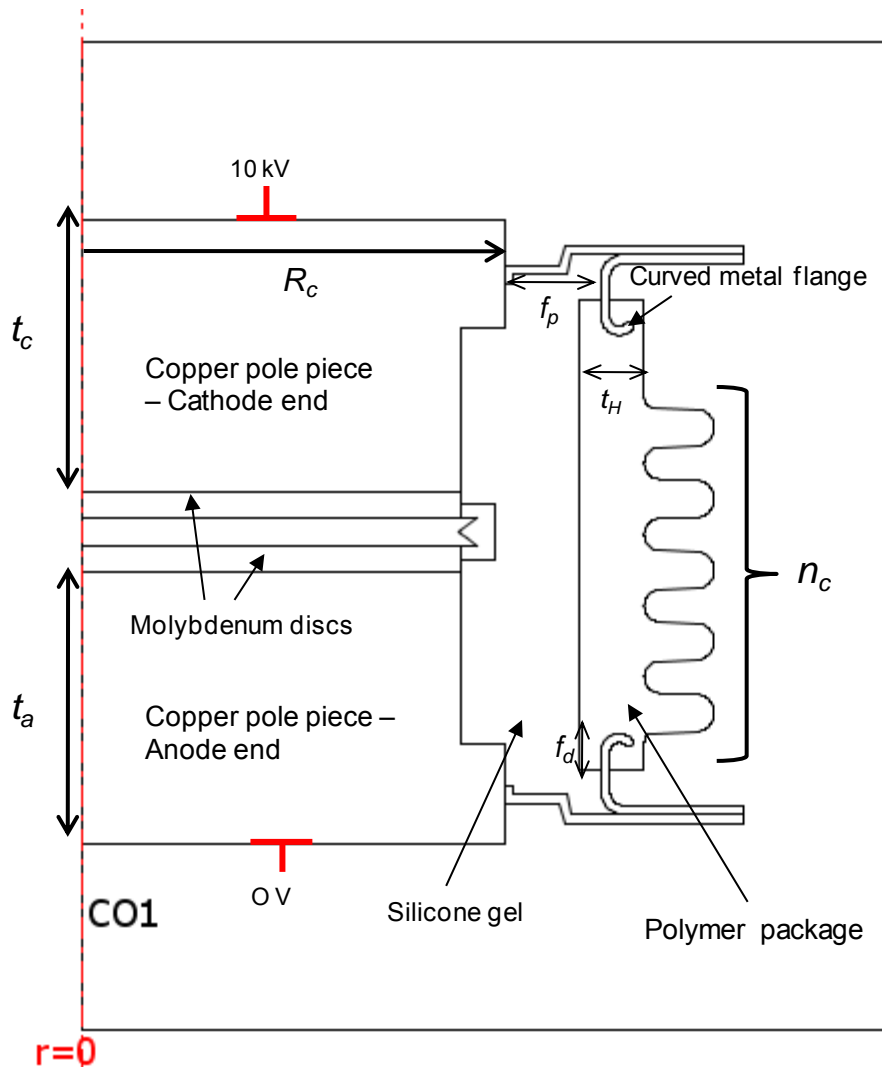
To investigate the influence of the different design parameters on the electrical performance of the polymer housing, the electric field strength was here selected as the appropriate quality criterion. Also, because a low electric stress is desired within the housing to prevent failure, the electric field strength was here classed as a ‘the smaller the better’ quality characteristic.

For the experiments outlined in this chapter, a two stage approach (stage A and B) was used to investigate the design parameters influence in order to develop the 125 mm housing. In stage A, the relevant relationships (or interactions) between the chosen design factors were to be identified, i.e. which particular design parameter’s influence is likely to be influenced by the

level (or magnitude) of another factor. The relevant design interactions determined from stage A were then used to determine the optimum design settings for a 125 mm size device and investigate the relative contribution of each design parameter towards the electric field variation using the Analysis of Variance (ANOVA) technique in stage B. For both stages, the appropriate OA was first chosen, and then the different design parameters and interactions were assigned to the appropriate columns of the OA according to Taguchi's Table of Interaction. Finally the experiments were conducted according to the appropriate design matrix using finite element analysis. It should be noted that the procedures involved in assigning the relevant design parameters and interactions to the relevant OA columns are not discussed here, but can rather be reviewed from different published sources, e.g. Roy, 1990.

### **10.3.1 FEA Model**

The 'hockey-puck' thyristor device configuration was again used for the studies described in this chapter, with the silicon wafer sandwiched between molybdenum discs and copper pole pieces and enclosed in a polyimide-based polymer package with silicone gel present in the housing cavity. The flange was based on the 45° curved profile where the tip was rounded to keep the electric field at the interface region as low as possible (as outlined in section 7.7.3 in Chapter 7).



**Figure 10.1: Axisymmetric model of 'hockey-puck' device used for Taguchi method-based studies**

To study the electrical performance of the polyimide housing, a 10 kV DC voltage was again applied between the two pole pieces (as illustrated in the finite element axisymmetric model in Figure 10.1), while the electrical conductivity values defined for the different subdomains in the model were as listed in Table 6.1 in Chapter 6. The electrical field magnitude at the flange/housing interface region at only the anode end was studied here because the localised field magnitude at this region was found to be higher than that at the cathode end from previous simulation experiments.



## 10.4 Design factor interactions – Stage A

### 10.4.1 Methodology

As observed in Chapter 8, design parameters, such as the flange depth,  $f_d$ , flange position,  $f_p$ , and number of convolutes,  $n_c$ , were seen to have varying influence on the electric field strength within the housing. To fully understand the influence of different design factors on the electrical performance of the polymeric housing, other geometrical parameters, such as the cathode and anode pole piece diameters ( $R_c$ ), the cathode and anode pole thickness ( $t_c$  and  $t_a$  respectively), and the package thickness ( $t_H$ ) were also investigated in this study (Figure 10.1). Because these parameters could be economically controlled to optimise the electrical performance of the housing, they were all categorised as control factors and studied at two levels, while their interactions were studied between two factors. The individual levels and notations of the design parameters used for this experiment are shown in Table 10.1, where the different parameter levels can be seen to have been coded as 1 and 2 for ease of processing. It should be noted the levels of the different design parameters, e.g. the flange position along the housing, package thickness, etc., were selected on the basis of knowledge gathered from different simulation studies performed in the initial stages of the NEWTON project for the 50 mm package, and also based on moulding related feedback from DuPont™. For example, the flange position dimension levels were chosen so as to maintain at least 1 mm distance between the rounded flange tip and the outer edge of the housing for most simulation studies. This was required to enable a proper polymer flow around the curved profile of the flange during moulding and thereby reduce the probability of any void formation. As part of these studies, other dimensions that were also kept constant included the overall height of the device (34.7 mm), the silicon wafer and molybdenum disc thicknesses (1.45 and 1.59 mm respectively), and the tracking distance along the exterior contour of the housing convolutes (around 55 mm). An illustration of the typical designs of the housing when the number

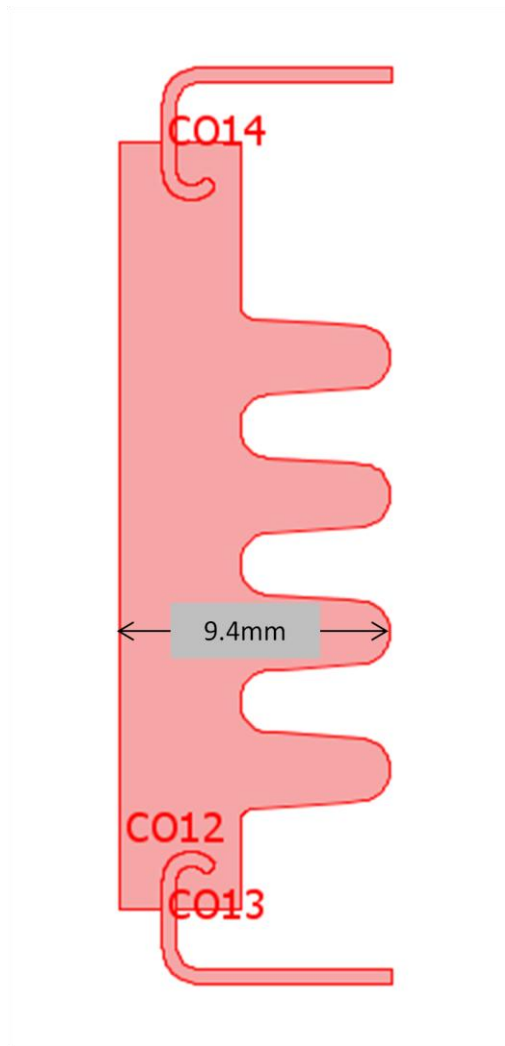
of convolutes were changed while keeping the tracking distance constant are shown in Figures 10.2 (a) and (b). In Figure 10.2 (a), the resulting span between the inner periphery of the housing and exterior edge of the 4 convolute housing was equal to 9.4 mm; while for the 5 convolute housing, the distance was around 8.1 mm (Figure 10.2 (b)).

This experiment was comprised of 6 design parameters and 15 possible interactions, namely A x B, A x C, A x D, A x E, A x F, B x C and so on. Because each design parameters were studied at two levels and the degree of freedom (DOF) is computed by subtracting the number of levels by 1, the DOF of each design factors were in this case equal to 1. Likewise, because the DOF of each interaction is computed by multiplying the DOF of each interacting design parameters, the DOF of each interactions in this experiment were also equal to 1. Thus, the total DOF required to study the 6 design factors and 15 interactions involved in this study was calculated to be 21.

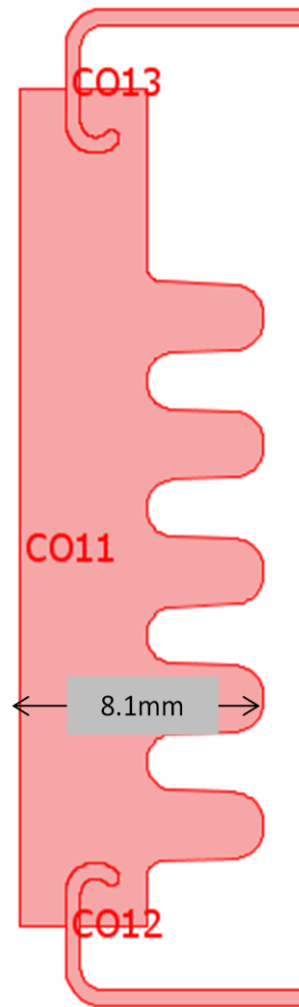
When a Taguchi-based OA is selected to design and conduct an experiment, the selected OA cannot have a DOF that is less than the total DOF of the experiment. For this study, an L32 OA was considered to be appropriate among the different set of OAs used in Taguchi, e.g. L16, L27, L64, etc. The benefits this OS provided was: (1) it could easily accommodate the 21 DOF; (2) it also limited the total number of experiments for this study to only 32 runs, as opposed to 64 experiments ( $2^6 = 64$ ) that would have been required for a full factorial experiment design in this case.

DESIGN FACTORS		LEVEL 1 (1)	LEVEL 2 (2)
A	Pole piece radius, $R_c$	25 mm	37.5 mm
B	Pole piece thickness, $t_o/t_a$	17.0 mm/13.2 mm	15.1 mm/15.1 mm
C	Flange position, $f_p$	5.4 mm	4.9 mm
D	Flange depth, $f_d$	2.0 mm	3.0 mm
E	Package Thickness, $t_H$	4.2 mm	3.5 mm
F	No. of convolutes, $n_c$	5	4

Table 10.1: Factors for the design parameter interaction investigation



(a): 4 convolutes housing



(b) 5 convolutes housing

Figure 10.2: Illustration of the 4 and 5 housing convolute designs

## 10.4.2 Results & Discussion

Figure 10.3 depicts a typical contour plot of the electrical field distribution across a 5 convolute housing when a 10 kV DC voltage is applied, while Figure 10.4 illustrates a close-up view of the electrical field distribution around the flange and polymer interface region at the anode end where the maximum electric field can be seen to occur along the curved surface of the flange.

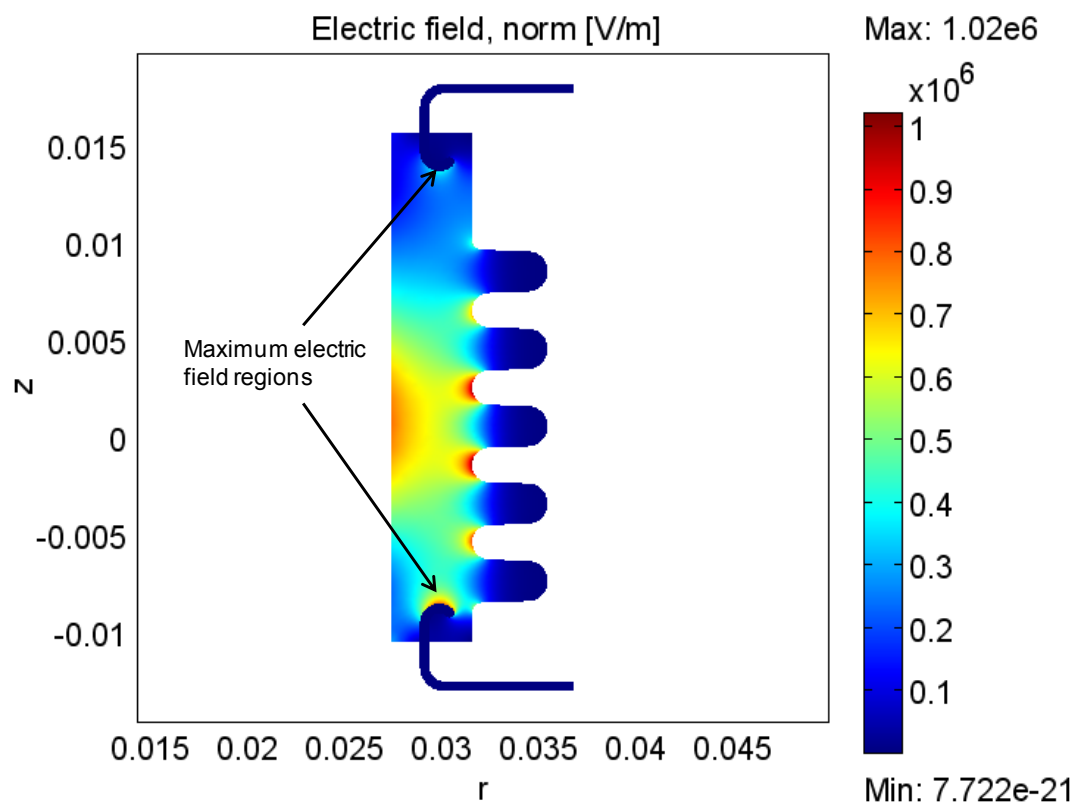


Figure 10.3: Typical electric field contour plot across a 5 convolutes housing

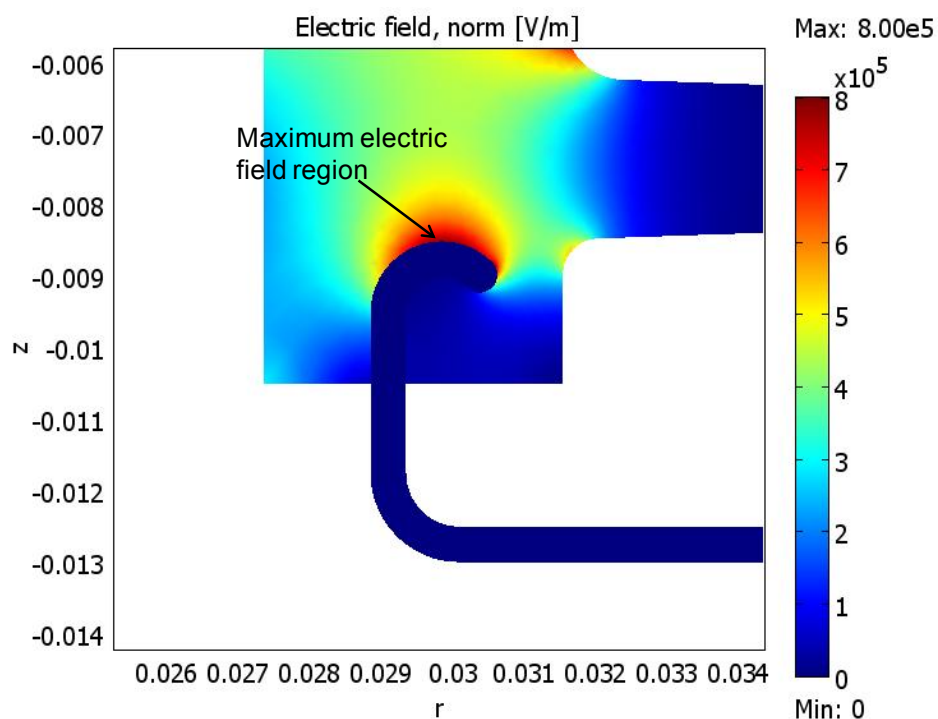
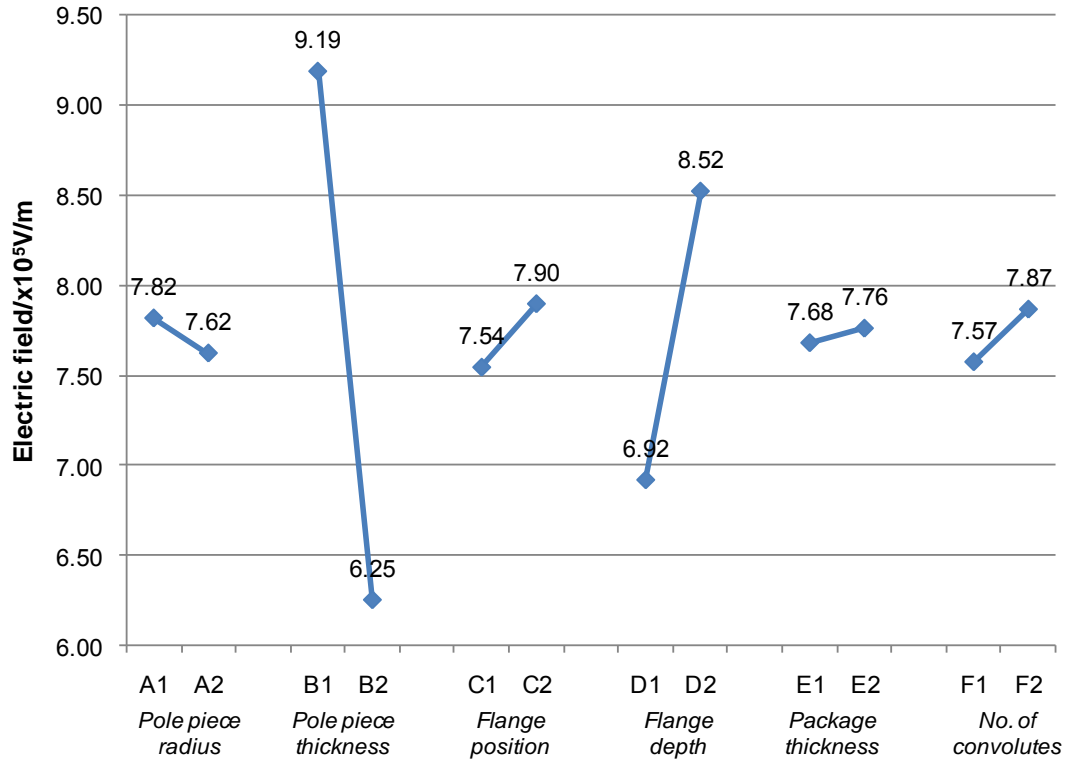


Figure 10.4: Magnified view of electric field plot across the housing/flange interface region



and cathode pole piece thicknesses were 17.0 mm and 13.2 mm. The different design parameters and 15 interactions were then assigned to the different columns according to the standard Taguchi method procedures described in Roy, 1990, before the simulations of each parameter combinations were performed and their results analysed.

The main effect plot of the different design parameters is shown in Figure 10.5. The electric field values of each design factor represent the average electric field response computed at each level. For instance, the standard method to calculate the average electric field response for a design parameter, e.g. pole piece radius (factor A) at level 1, involved taking the mean of the field responses from experiments 1 to 16, while the average at level 2 was computed by averaging the response from experiments 17 to 32. Such an approach was also used to compute the average effect of the other design parameters at levels 1 and 2. As highlighted in Chapter 8, different design parameters were seen from the plot to have varying influences on the electric field response in the package. For example, the pole piece thickness (factor B) and the flange depth (factor D) were here observed to influence the electric field magnitude more than other parameters, such as the pole piece diameter (A), or the number of convolutes (F). This electric field variation actually correlates well with the studies in Chapter 8. As observed in Figures 8.5 to 8.9, when the flange depth was varied, the electrical field magnitude at the cathode and anode contact regions was seen to vary more than when the flange position and number of convolutes along the housing were changed.

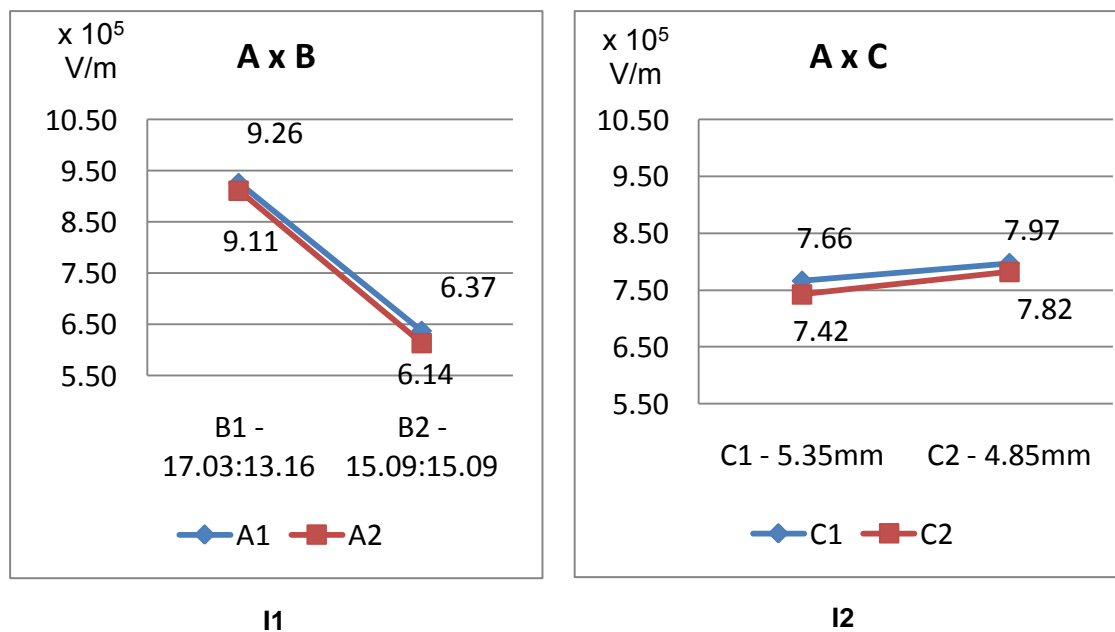


**Figure 10.5: Main effects of design parameters (Design interaction study)**

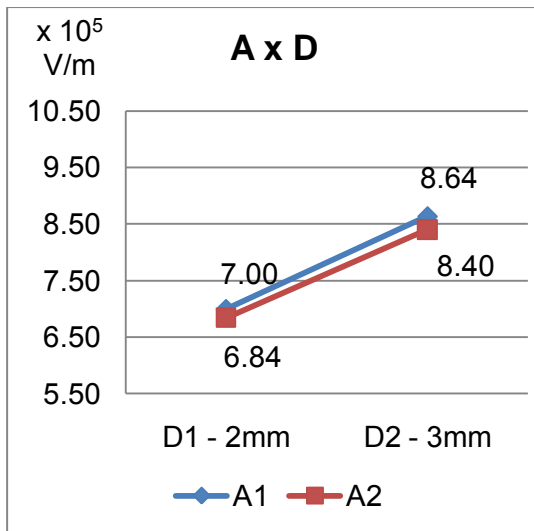
The interaction plots depicting the relationships between the design parameters are illustrated in graphs I1 to I15 in Figure 10.6. In these plots, if the lines are parallel, no interaction is said to occur between the two variables (or parameters), whereas the greater the lines depart from parallel, the greater their interaction, i.e. if the lines cross each other, strong interactions are said to occur between the parameters. To illustrate how the data in these graphs was derived, consider I1 the interaction between A and B. The ( $A_1B_1$ ) interaction is calculated from results that contain both  $A_1$  and  $B_1$  levels. It should be noted here the interaction ( $A \times B$ ) assigned to column 3 in Table 10.2 is not used here to calculate ( $A_1B_1$ ) interaction. Instead columns 1 and 2 which represent the individual factors A and B are used. From Table 10.2, it can be seen  $A_1$  is contained in rows (experiment number) 1 to 16, and  $B_1$  from rows 1 to 8 and 17 to 24. Comparing the two, the rows that contain both  $A_1$  and  $B_1$  can be seen to be 1 to 8. The average effect of  $A_1B_1$  was thus calculated from the electric field results in rows 1 to 8, and was computed to be  $9.26 \times 10^5$  V/m. Other interactions, e.g.  $A_1B_2$ ,  $A_2B_1$ ,  $A_2B_2$ , etc., were also

calculated using the same procedure to find the average field influence, and are shown in the remaining interaction plots in Figure 10.6.

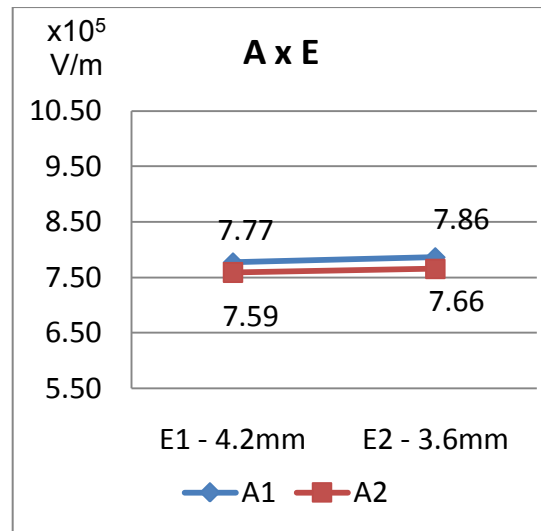
From the simulation experiments, strong interactions were seen to occur only between the pole piece thickness (B) and the number of convolutes (F) (Plot I9), and between package thickness (E) and the number of convolutes (F) (Plot I15). On the other hand, as can be seen from other interaction plots, interactions between other parameters were seen to be either a 'non-occurrence' or 'not obvious' because the lines are almost parallel (Tsai et al., 1996). A summary of the identified parameter relationship is depicted in Table 10.3, where the shaded cells reveal the existence of a relationship between the corresponding design parameters. These identified design relationships were subsequently used in stage B to design the 125 mm diameter device.



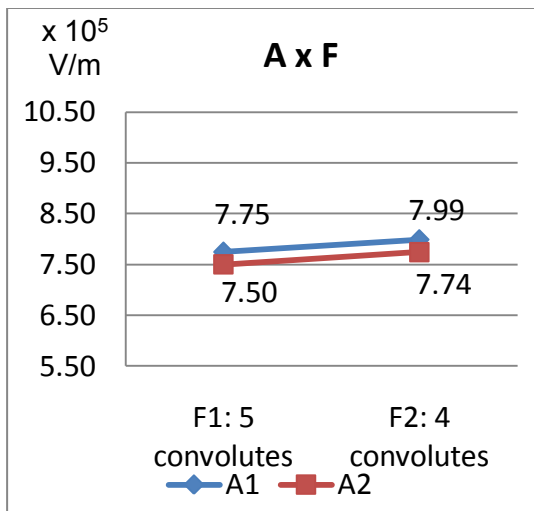




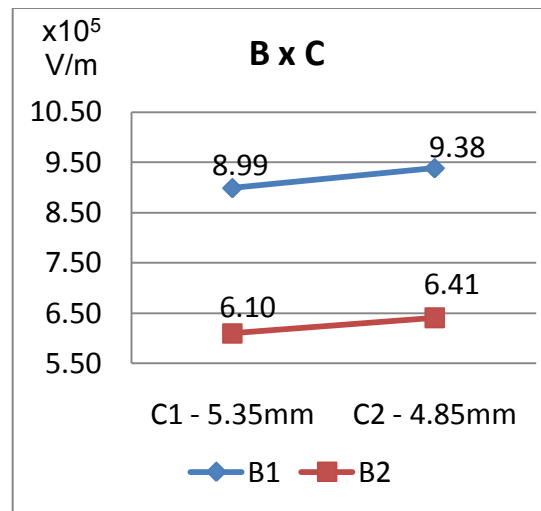
I3



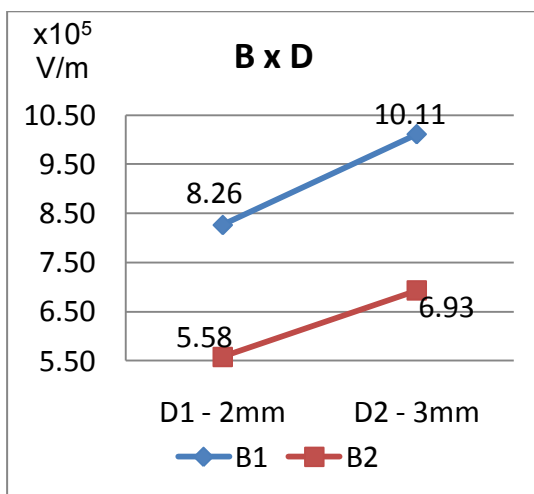
I4



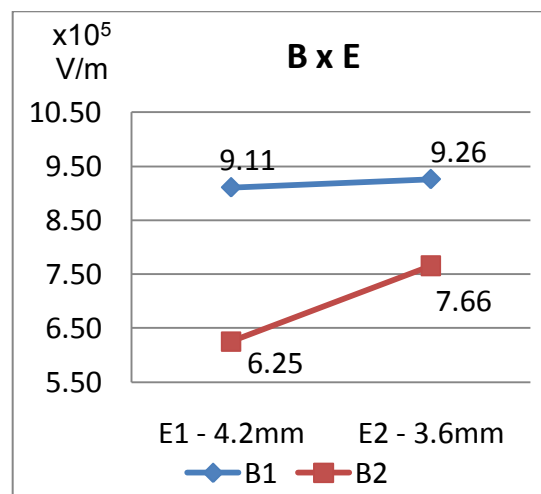
I5



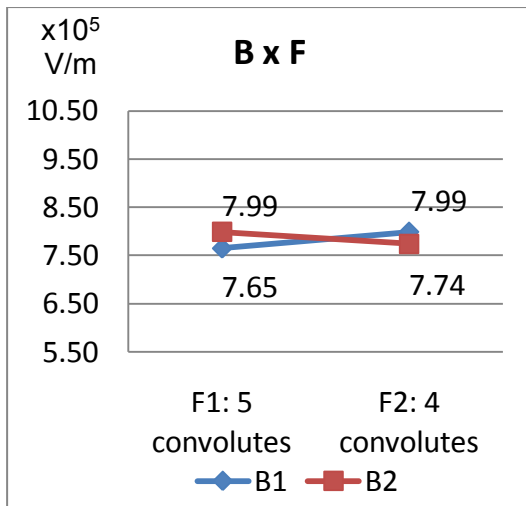
I6



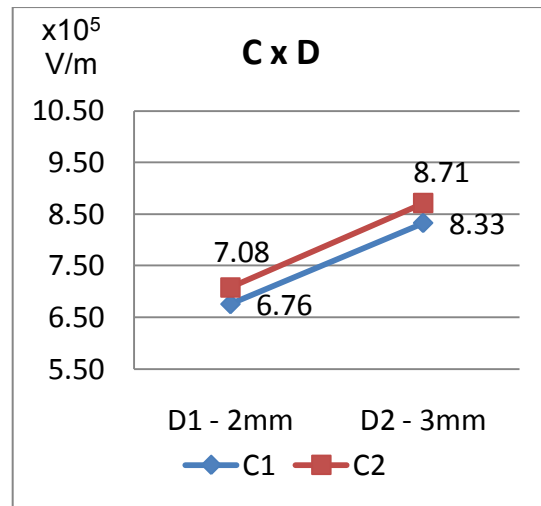
I7



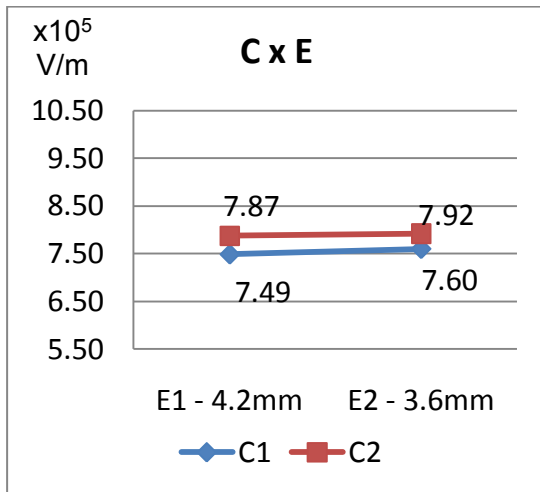
I8



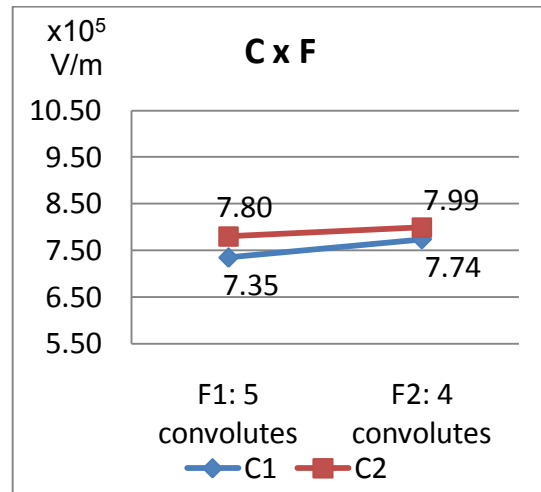
I9



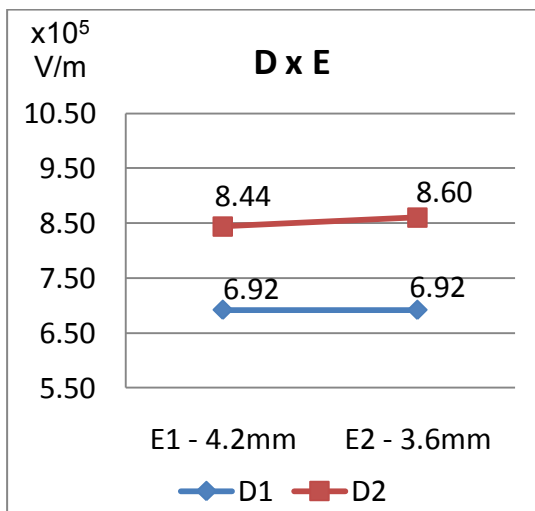
I10



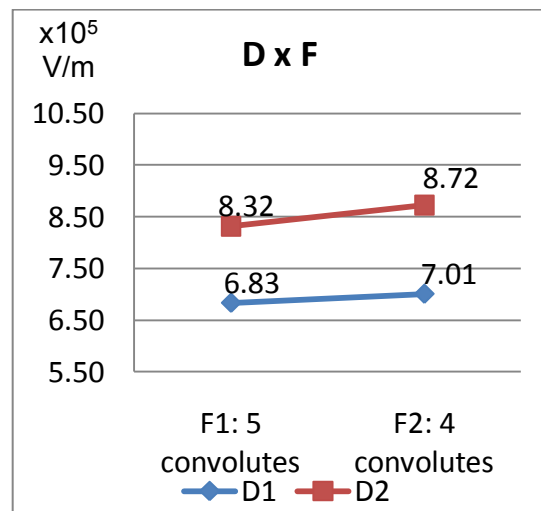
I11



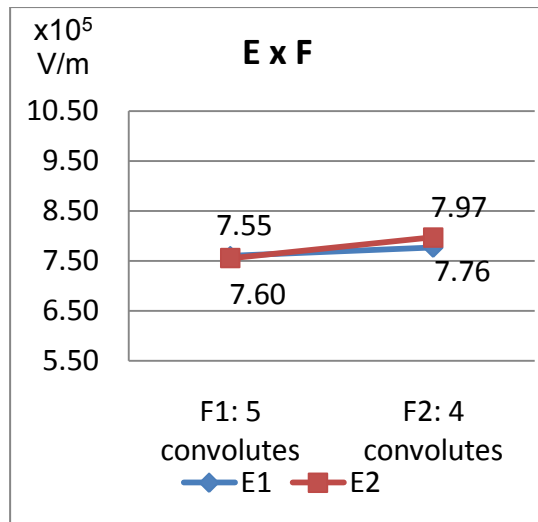
I12



I13



I14



I15

Figure 10.6: Interaction plots between design parameters

A, Pole piece diameter	B, Pole piece thickness	C, Flange position	D, Flange depth	E, Package thickness	F, No. of convolutes	
	A x B	A x C	A x D	A x E	A x F	A, Pole piece diameter
		B x C	B x D	B x E	B x F	B, Pole piece thickness
			C x D	C x E	C x F	C, Flange position
				D x E	D x F	D, Flange depth
					E x F	E, Package thickness
						F, No. of convolutes

Table 10.3: Summary of interactions between all design parameters

## 10.5 Stage B - 125 mm housing design

### 10.5.1 Methodology

The Taguchi method of experimental design was again used to assist the design of a 125 mm size thyristor device. In this experiment, the aim was to

determine the optimum design settings for the 125 mm size device. In addition, the contributions of the different design parameters towards the electric field variation were studied using the ANOVA statistical technique. A review of the terms and computations involved in ANOVA technique (sourced from Roy, 1990) is summarised in section 10.5.1.1.

As opposed to the experiments in stage A, the diameter and thickness of the copper pole pieces were here kept constant to maintain the device diameter around 125 mm together with the overall device height, and the thickness and diameter of the molybdenum discs and silicon wafer. An example of the axisymmetric FE model of the 125 mm thyristor used for this case study is shown in Figure 10.7. As illustrated in the figure, the thicknesses of the molybdenum discs and silicon wafer were taken to be respectively 1.45 mm and 1.59 mm, and the anode and cathode copper pole pieces were each considered to be 13 mm and 16 mm. On the other hand, the design parameters changed included the flange position,  $f_p$ , along the housing periphery, its depth inside the housing,  $f_d$ , the package thickness,  $t_H$ , and the number of convolutes,  $n_c$ . The design factors were again chosen as two-level control factors, and were treated at the same ranges used in stage A (Table 10.4). Together with the main design parameters, the interaction between the package thickness (E) and the number of convolutes (F) identified from stage A was also included in the experiment matrix. In this case, since the total degree of freedom was 5 (i.e. the four main design parameters 4 and 1 for the considered interaction), an L8 OA was considered appropriate to design the experiment trials. As in stage A, a lesser number of simulations, i.e. 8 experiments in this case, was performed compared to a full factorial experiment design that would require 16 experiments ( $2^4 = 16$ ).

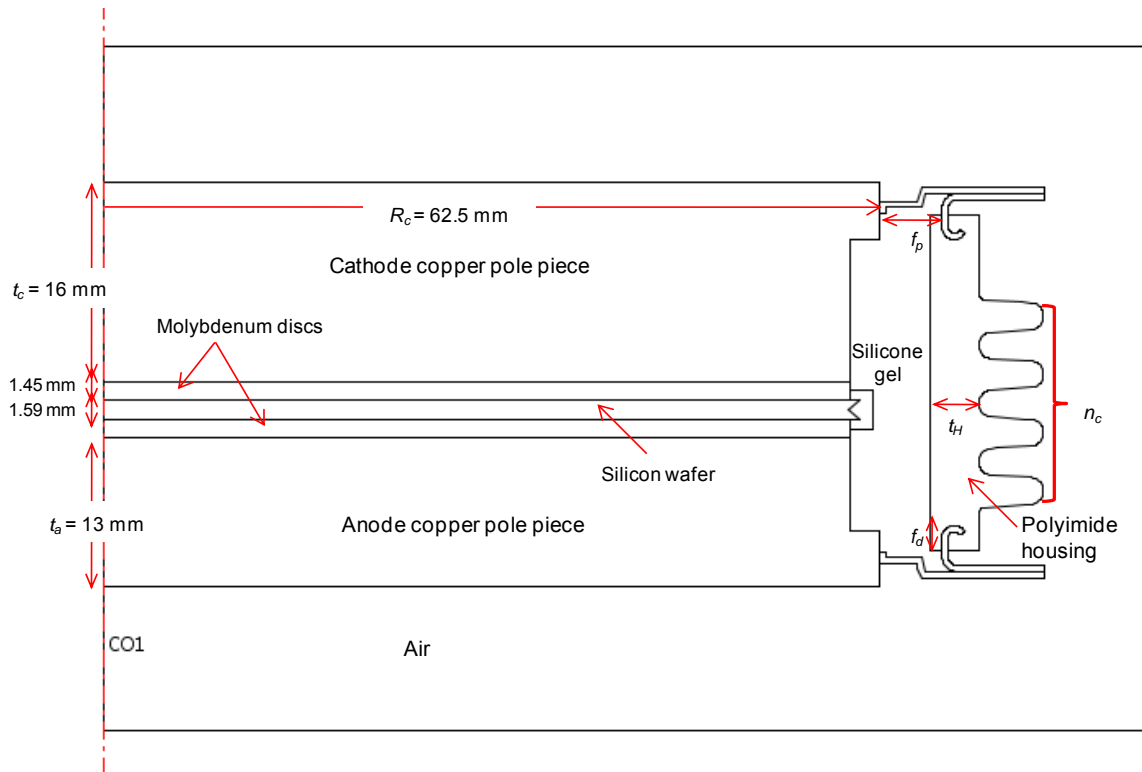


Figure 10.7: Axisymmetric model of 125 mm size thyristor device

DESIGN FACTORS		LEVEL 1 (1)	LEVEL 2 (2)
C	Flange position/radius	5.4 mm	4.9 mm
D	Flange depth	2.0 mm	3.0 mm
E	Package Thickness	4.2 mm	3.5 mm
F	No of convolutes	5	4

Table 10.4: Selected design factors and level

### 10.5.1.1 ANOVA

The Analysis of variance (ANOVA) statistical technique is widely used to determine the relative contributions of different factors by comparing their variances. As part of this analysis, different quantities, such as degrees of freedom, sum of squares, mean squares, etc., are required to be computed and are organised in a standard tabular format for analysis purposes. An example of such a table consisting of factors A and B, and an interaction A x

B is illustrated in Table 10.5, while the definition of the different quantities required for computation are overviewed in sections 10.5.1.1.1 to 10.5.1.1.6.

FACTORS	DEGREES OF FREEDOM, $f$	SUM OF SQUARES, $S$	VARIANCE (MEAN SQUARES), $V$	VARIANCE RATIO, $F$	PURE SUM OF SQUARES, $S'$	% CONTRIBUTION, $P$
A	$f_A$	$S_A$	$V_A$	$F_A$	$S'_A$	$P_A$
B	$f_B$	$S_B$	$V_B$	$F_B$	$S'_B$	$P_B$
A x B	$f_{A \times B}$	$S_{A \times B}$	$V_{A \times B}$	$F_{A \times B}$	$S'_{A \times B}$	$P_{A \times B}$
Error, $e$	$f_e$	$S_e$	$V_e$	$F_e$	$S'_e$	$P_e$
Total, $n$	$f_T$	$S_T$	$V_T$	$F_T$	$S'_T$	$P_T$

Table 10.5: ANOVA table

#### 10.5.1.1.1 Degrees of freedom (DOF), $f$

The DOF is a measure of the amount of information that can be determined from a given set of data. DOF for the data concerning a factor is equal to one less than the number of levels. For example if a factor A has 4 levels, then the DOF will be 3 in this case, i.e.  $A_1$  can be compared with  $A_2$ ,  $A_3$  and  $A_4$  data, but not with itself.

An L8 OA with seven columns representing 2 level factors has 7 DOF. On the other hand, for an experiment with  $n$  trials and  $r$  repetitions of each trial having  $n \times r$  trial runs, the total DOF,  $f_T$ , is then given by equation 10.1.

$$f_T = n \times r - 1 \quad \text{Equation 10.1}$$

Similarly, the DOF for a sum of squares term,  $f_T$ , is equal to the number of terms used to compute the sum of squares and the DOF of the error term,  $f_e$ , is expressed using Equation 10.2.

$$f_e = f_T - f_A - f_B \quad \text{Equation 10.2}$$

#### **10.5.1.1.2 Sum of squares, S**

The sum of squares is a measure of the deviation of experimental data from the mean value of the data. Thus the total deviation,  $S_T$ , is expressed as a summation of each squared deviation, as shown in equation 10.3, where  $Y_i$  is the experiment result,  $\bar{Y}$  is the average value of  $Y_i$ .

$$S_T = \sum_{i=1}^n (Y_i - \bar{Y})^2 \quad \text{Equation 10.3}$$

#### **10.5.1.1.3 Variance, V**

The variance of each factor is determined by the sum of the square of each trial involving the factor divided by the degrees of freedom. For example, the variance of factor A, B, A x B and the error term are given by equations 10.4 to 10.7.

$$V_A = S_A / f_A \quad \text{Equation 10.4}$$

$$V_B = S_B / f_B \quad \text{Equation 10.5}$$

$$V_{A \times B} = S_{A \times B} / f_{A \times B} \quad \text{Equation 10.6}$$

$$V_e = S_e / f_e \quad \text{Equation 10.7}$$

#### **10.5.1.1.4 Variance ratio, F**

The variance ratio is defined as the variance of the factor divided by the error variance. For example, the variance ratio for factor A is typically calculated using equation 10.8.

$$F_A = V_A / V_e \quad \text{Equation 10.8}$$

#### **10.5.1.1.5 Pure sum of squares, $S'$**

The pure sum of squares is the sum minus the degrees of freedom times the error variance, as shown by equations 10.9 and 10.10 commonly used to compute the pure sum of square for factor A and error, e.

$$S'_A = S_A - f_A \times V_e \quad \text{Equation 10.9}$$

$$S'_e = S_e + (f_A + f_B + f_C) \times V_e \quad \text{Equation 10.10}$$

#### **10.5.1.1.6 Percentage contribution, $P$**

The percent contribution of each factor is defined as the ratio of the factor sum to the total, expressed as a percentage. For instance, the percentage contributions of factor B and error, e are expressed using equations 10.11 and 10.12.

$$P_B = S_B \times 100/S_T \quad \text{Equation 10.11}$$

$$P_e = S_e \times 100/S_T \quad \text{Equation 10.12}$$

### **10.5.2 Results & Discussions**

The L8 OA showing all 8 sets of experimental trial conditions and their electrical field responses at the anode end flange/housing contact region computed using FEA is illustrated in Table 10.6, while the influence of the different design factors is shown in Figure 10.8.

From the plot, an improvement in the quality characteristic (i.e. low electric field within the package) was seen to be achieved when all design parameters C, D, E and F were all at level 1 ( $C_1D_1E_1F_1$ ). That is, the optimum design settings for the electric field to be lower in the 125 mm device is observed when (a) the flange separation between the cathode and anode ends is



increased, i.e. the flange depth (D) is reduced, (b) the number of convolutes (F), the package thickness (E) and the distance between the pole piece and the flange location along the housing (C) is increased. These results were again seen to be in agreement with the simulation studies when the flange depth and its radial position were varied in Chapter 8. As can be seen in Figures 8.5 to 8.9, the electric field at the cathode and anode contact regions was observed to increase when the flange depth and its radial position were increased in the 4 and 5 convolute housings. However, the electric field magnitude in the 4 convolute housing (Chapter 8) was observed to be lower than in the 5 convolute package configuration, and was not in agreement with the Taguchi results highlighted earlier in this section. At this stage of the project, a detailed correlation between the housing convolute number and the magnitude of the electric field is not fully understood. Further works will be required in this area in the future.

The result of the ANOVA analysis is illustrated in Table 10.7. From the analysis, the percentage contribution of the flange depth (D) parameter towards the electric field variation was seen to be around 90%, and higher than other design parameters. This result correlated with other simulation studies observation whereby varying the flange depth was also seen to have a more significant influence on the electric field magnitude than other parameters, such as the flange position or the number of the housing convolutes. Based on the ANOVA results, because the interaction between the package thickness (E) and the number of convolutes (F) was found to be very low (0.24%), the suspected interaction between the factors E and F was concluded to be non-existent.

Experiment Number /Columns	L8 Array							Max. Electric Field Mag. at Anode End/ $\times 10^5 \text{ Vm}^{-1}$
	E: Package Thickness	F: No of Convolutes	E x F	C: Flange Position	D: Flange Depth	Unused Column	Unused Column	
	1	2	3	4	5	6	7	
1	1	1	1	1	1	1	1	7.76
2	1	1	1	2	2	2	2	9.89
3	1	2	2	1	1	2	2	8.06
4	1	2	2	2	2	1	1	10.27
5	2	1	2	1	2	1	2	9.61
6	2	1	2	2	1	2	1	8.11
7	2	2	1	1	2	2	1	10.28
8	2	2	1	2	1	1	2	8.34

Table 10.6: L8 OA used for the 125 mm housing design

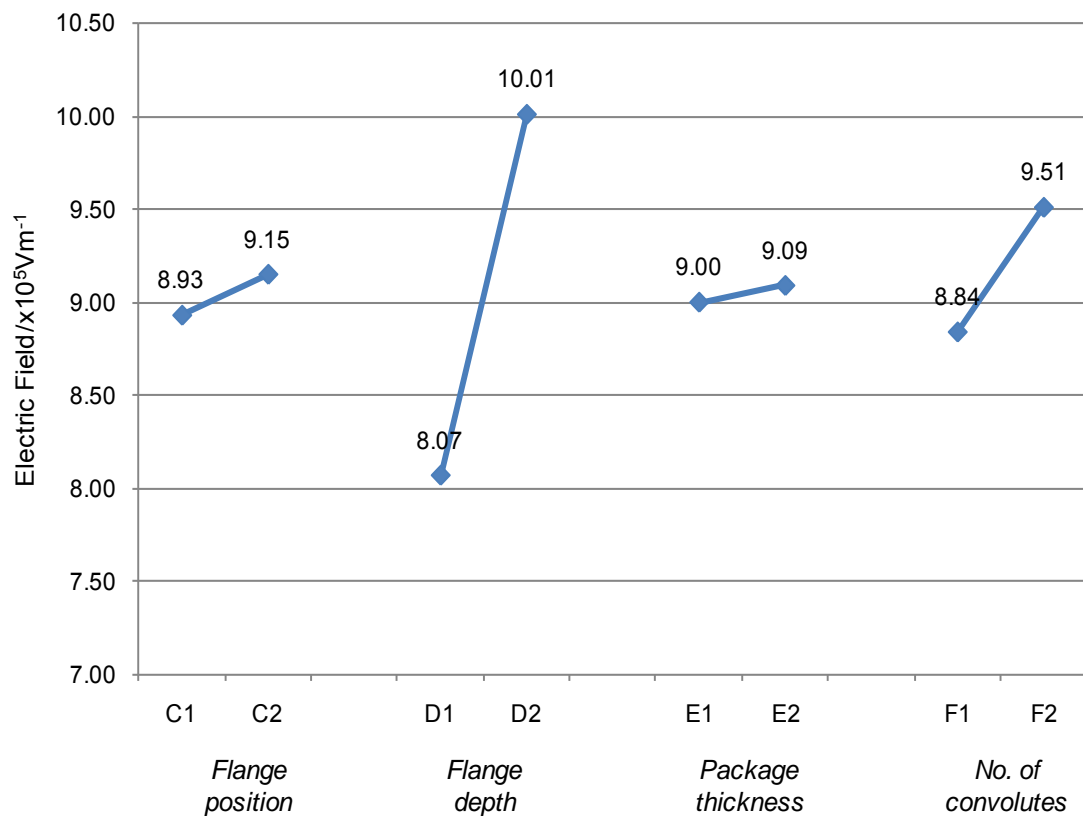


Figure 10.8: Main effects of design parameters (125 mm device design)

Source of Variation	f	SUM OF SQUARES	VARIANCE (MEAN SQUARES), V	VARIANCE RATIO, F	PURE SUM OF SQUARES, S'	PERCENT CONTRIBUTION, P
C	1	<b>0.96</b>	0.96	58.98	0.94	5.33
D	1	<b>15.93</b>	15.93	979.74	15.92	90.03
E	1	<b>0.42</b>	0.42	25.74	0.40	2.28
F	1	<b>0.28</b>	0.28	17.06	0.26	1.48
E x F	1	<b>0.06</b>	0.06	3.66	0.04	0.24
Error, e	2	<b>0.03</b>	0.02	1.00	0.11	0.64
Total, n	7	<b>17.68</b>				100.00

**Table 10.7: ANOVA table for 125 mm device design**

## 10.6 Conclusion

From electrical simulations that were performed to develop the 50 mm prototype, different geometrical design parameters of the polymer thyristor housing were observed to have varying influence on the electrical field within the package. In order to fully understand the interaction and influence of the different geometrical parameters, an in-depth study was thus carried out and applied to a 125 mm dimension housing. The aim was to identify an optimum combination of different geometrical parameters for the electrical field at the flange/polymer interface to be low. To achieve these objectives, a two stage approach (stage A & B) consisting of various electrical simulations using finite element analysis were done and organised as an array of experiments using the Taguchi method of experimental design.

In stage A, the relevant relationships between different parameters were identified. The appropriate interactions and design parameters were then used in stage B to design the 125 mm size device.

From the simulation trials in stage A, strong interactions were seen to exist between the copper pole thickness and the number of convolutes, and between the package thickness and the number of convolutes design

parameters. Together with these interactions, housing parameters, such as the flange position and radius, package thickness and the number of convolutes, were then used to develop the 125 mm housing in stage B. Following the application of the Taguchi method where the different housing parameters and interactions were organised in an L8 OA, a lower electric field in the 125 mm housing was achieved when the housing parameters were as follows: (1) the depth the metal flange protrudes inside the housing at both the cathode and anode ends is kept as low as possible, i.e. the flange separation between the cathode and anode ends is increased, (2) the number of convolutes, the package thickness, and the distance between the pole piece and the flange location along the housing at both the cathode and anode ends are increased. Similarly, using the ANOVA statistical technique, any variation in the flange depth parameter was observed to influence the electric field within the housing more than other design parameters.

# **11 Conclusions and future work**

## **11.1 Introduction**

This chapter summarises the work completed and then draws together the conclusions from the research presented in this thesis in the form of a set of design and design-for manufacture recommendations. It then proposes potential directions for future investigations.

## **11.2 Research summary**

Commercial thyristor devices used in long distance high voltage transmission are today only commercially available in a hermetic configuration comprised of a ceramic housing enclosing a silicon wafer sandwiched between molybdenum discs and anode and cathode copper pole pieces. In this project, the scope for developing a novel polymer-based enclosure has been investigated so that a cheaper, lighter and higher performance 8.5 kV thyristor can be available to long distance HVDC transmission schemes in the future. As reviewed in Chapter 2, although polymer-based housings for power semiconductor devices have been developed in the past, the polymer package developed in this project is novel because it will be designed to a higher power rating and is expected to have better properties, e.g. low failure rate, long service life, etc., for future commercial exploitation. In order to identify whether a shift towards polymer-based packaging was appropriate for high voltage thyristor devices, a 50 mm wafer diameter prototype was chosen as a case study for this project. Through this development exercise, design and performance related challenges were identified, which must be addressed before the development of larger housings, e.g. for 125 mm and 150 mm diameter wafers, could be initiated in the future. It is the development and

reliability performance of the 50 mm prototype that has been primarily discussed in this thesis.

As elaborated in Chapter 3, the different failure mechanisms that are likely to contribute to the thyristor device failure when it is exposed to a variety of electrical, mechanical and thermal stresses include: dielectric breakdown and partial discharge if the polymer housing encounters an electrical overstress; fracture due to applied mechanical loads and resonances from transportation; and interfacial delamination when the package is exposed to varying temperature.

The different studies that were performed in this project were split between computer modelling studies applied to design of the 50 mm prototype, and physical performance and reliability testing of the manufactured prototypes. The simulation studies were undertaken using the Comsol multiphysics finite element (FE) package. They focussed on assisting and improving the design of the polymer package when it is exposed to electrical and thermal stresses, whilst the reliability studies, which comprised of a series of accelerated life tests, aimed at investigating the physics-of-failure of the prototype. Following work by Ahmad, 2009 to shortlist appropriate polymers and a basic design configuration for the housing (as discussed in Chapter 4), a glass-reinforced polyimide polymer grade supplied by DuPont™ was selected for the package, while its design was based on a 'replacement' type concept where the ceramic housing of the device was directly replaced with the polymer material. The different simulation and reliability test results relating to the 50 mm prototype development that were described in Chapters 6 to 10 are summarised next.

- **Chapter 6: Electrical performance of polymer housing**

Through the computer simulation studies performed in this chapter to investigate the electrical behaviour of the polymer-based housing, when the required static DC operating voltage was applied between the two pole pieces, the peak electric field magnitude within the housing was seen to be only 5% of the dielectric strength of the selected

polyimide polymer. This suggested a void-free polymer housing was unlikely to fail due to dielectric breakdown when the thyristor is in service. However localised regions of high electrical field strength were observed at the cathode and anode interface regions between the flange and polymer housing. Because such localised high electric stress regions can lead to partial discharge failure of the package if it has any voids or other defects, different design studies were performed to establish design rules that reduce the peak field magnitude and therefore reduce the risk of in-service failure.

The preliminary simulations that were performed included studying the effect of changing the electrical conductivity of the polymer housing, and of the material filling the internal cavity formed between the housing and the stacked assembly of silicon wafer, molybdenum discs and copper pole pieces. To vary the housing cavity electrical conductivity, the cavity was considered to be filled with either dry nitrogen or silicone gel; whilst to investigate the housing electrical conductivity influence, the performance of housings that were comprised of the different polymer candidates shortlisted by Ahmad, 2009 was compared with that of the typical ceramic used in traditional hermetic packages. The shortlisted polymer candidates were polyimide, liquid crystal polymer, polyetherimides, polyphenylene sulfide, epoxy, polyetheretherketone and polybutylene terephthalate and cover a range of conductivities of 2 orders of magnitude.

When the housing cavity was filled with dry nitrogen, the peak electric field magnitude at the cathode and anode contact regions were observed to be equal and to be higher than other regions within the package. Since the localised electric field magnitude around the interface regions was observed to be significantly lower than the dielectric strength of the selected polyimide polymer grade (around 5%), the probability of dielectric breakdown of the polymer housing was again considered to be low in this case. When silicone gel was used as the housing cavity filler, a localised electric field that was higher at the

anode interface region was observed. However, a comparison of the highest field magnitude that occurred at the anode interface showed the difference between the magnitudes to be low when the housing cavity was comprised of either dry nitrogen or silicone gel. From this observation, it was deduced that changing the electric conductivity of the housing cavity does not have a substantial influence on the peak electric field magnitude in the package.

Varying the electrical conductivity of the housing was also concluded to have no significant influence on the high electric fields around the contact regions. This variation was similar when either dry nitrogen or silicone gel was used as the cavity filler. However, when the electrical performance of the polymer housing (e.g. polyimide) and an equivalent ceramic package that had silicone gel as the cavity filler was compared, the electric field within the ceramic housing was observed to be higher. Together with this, the difference between the cathode and anode field magnitude was also seen to be lower in the ceramic housing than in the polymer package. Such electric field variation was actually considered to be due to the electric conductivity of the housing material and its internal cavity. In the case of the ceramic housing that had silicone gel inside its cavity, the higher electrical conductivity of the ceramic than that of the silicone gel resulted in the small difference in the field magnitude at the cathode and anode interfaces.

Based on these initial DC simulation studies, because the changes in the peak electrical field in the housing were observed to be insignificant as a result of changes in the cavity filler and housing electric conductivity, the choice of appropriate material for the cavity filler and the housing should not be based on their electrical conductivity. Instead, their selection should be determined from other critical properties, such as moisture permeability and thermal stability.

When a time-varying 50 Hz AC electric potential was also applied across the thyristor, the electric field distribution was observed to be



identical to the case of an applied DC potential. The power density due to dielectric losses and therefore the resulting temperature rise in the package was found to be very low. When the harmonic components of a half-sinusoid AC voltage were also considered, the total power loss within the polymeric housing was still found to be negligible.

- **Chapter 7: Flange shape influence**

Because varying the electrical conductivity of the polymer housing and the internal cavity did not have significant influence on the localised electric field magnitude at the interface regions, further studies were undertaken in this chapter to reduce the field magnitude by investigating the influence of the flange geometry. The flange end designs that were studied were a straight flange end, a circular and elliptical-shaped wire-edged profile shape, together with a curved end flange shape. Because a preliminary study showed the interface electric field magnitude around the circular, elliptical and curved flange end shapes to be lower than the straight insert design, they were selected for further studies. In summary these studies showed: (1) when the radius of curvature of the different flanges was increased, as anticipated from the results of different published studies the electrical field magnitude at the interfaces was seen to decrease; (2) a comparison of the predicted field magnitudes also showed the electrical field around the elliptical flange end to be lower than around the circular and curved flange ends.

Based on these studies and also because the manufacture of the elliptical and circular flange end designs was identified as being difficult, and therefore expensive, compared to the curved shaped flange, the latter was chosen for use in the 50 mm prototype. Because voids could form around the inside curved region of such flanges during the moulding of the polymer housing, further studies were performed to refine the curved flange end design by varying its contour length. The electric field around the interface region varied as a result of changes in the contour length of the curved flange end. From the

modelling studies that were performed, because the maximum electric field region was observed to be located along the curvature of the curved insert (rather than the undesired location at the flange tip), a curved flange having a contour length corresponding to a 45° angle and with a rounded end was determined to be appropriate for use in the polymer housing for this application.

- **Chapter 8: Thyristor geometry influence**

To further assist the development of the 50 mm prototype, studies focussed on the geometrical parameters of the thyristor housing were also performed in this chapter. Because the flange depth, its radial position, the housing wall thickness, and the housing convolute design were regarded as critical parameters which, if incorrect, could lead to the failure of the package, a 2-stage investigation was herein performed. In stage 1, the influence of the flange depth, its position and the convolute shape on the electrical performance of a 4 and 5 convolute housing was studied to benchmark a preliminary prototype design. In stage 2, the housing benchmarked in stage 1 was further refined and the influence of changing the wall thickness of the package was studied from an electrical performance and moulding perspective, before the final 50 mm prototype design was determined.

From the stage 1 studies, the electrical field magnitude at cathode and anode interface was seen to decrease when the flange distance from the inside wall was increased; whilst it increased when the depth the insert protruded inside the package was increased. In these studies, a comparatively higher electric field magnitude was also observed when the insert was positioned at a depth equal to or less than the height of the housing convolute corners, and also when it was located near the inner wall of the housing.

Based on these studies and investigation of the housing convolute design, a preliminary housing design was chosen. From the housing convolute study, although the electric field around convolutes which

had no radius of curvature at its corners were noticed to be lower, a 1 mm radius for the convolute corners was instead chosen for the preliminary 50 mm prototype housing. The benefit it provided was its mould tool was easier to fabricate as compared to a tool for a housing which had no curvature around its convolute corners.

In stage 2, during which the housing thickness was reduced only around the convolute areas, the field magnitude across the cathode and anode interface regions was observed to decrease. A higher electric field that is due to its location at the flange tip was here also noticed when the wall thickness was greater than 3.5 mm. From the injection moulding simulations performed by DuPont™, a higher packing time was also observed at a region that was below the cathode end flange/housing interface region and above the first convolute from the cathode end. Because high packing times could lead to moulding defects, such as voids and shrinkage, the housing was 'cored' so that the wall thickness above the first housing convolute at the cathode end was reduced to correspond with the wall thickness around the housing convolutes. Following additional electrical simulation studies, the design and dimensions of the 50 mm prototype were finalised before it was successfully manufactured. The wall thickness of the prototype housing was 3 mm and 'cored'. The flange position from the inside housing wall was chosen to be 1.5 mm, while the depth it protruded inside was 2.0 mm based on the electrical studies.

- **Chapter 9: Thermo-mechanical performance study**

Following manufacture of the 50 mm prototypes, a preliminary study was here performed to study its reliability by investigating its thermo-mechanical performance as a result of temperature changes. Finite element analysis was here used to identify likely failure areas due to temperature changes, together with a temperature cycling (TC) test of 5 cycles between -40 °C and 125 °C to complement the simulation studies. The temperature cycling test programme also comprised of two additional tests carried out before and after the cycling experiment,

namely a dye penetrant test to identify delamination and surface cracks across the housing, and a partial discharge test to inspect the electrical performance of the manufactured prototype. From the FE simulation study, the region where delamination in the housing was considered likely to occur was at the cathode and anode flange/housing interface regions. On the other hand, the dye penetrant test performed before the TC experiment to inspect the quality of the manufactured housing also revealed no crack or damage along the housing surface. However, as observed in the thermo-mechanical simulation studies, delamination at the cathode and anode interface regions was observed. Partial discharge measurements on the manufactured prototypes before the TC experiment also showed the housings did not contain any air voids that would likely to result in failure during service. Out of the 148 prototypes that were manufactured in the project, only one housing failed the partial discharge test and was concluded to contain air voids that could contribute to its failure when it is in operation. Following the TC experiment, the dye penetrant test performed on the tested prototypes did not reveal any additional delamination or defects. As observed in the as-manufactured housings, only localised flange/housing delamination was seen. Also from the partial discharge test carried out after the TC experiment the electrical performance of the polymer showed no degradation as a result of the cycling experiment. This indicated that the manufactured 50 mm prototypes were free from any significant deterioration. However, because of the occurrence of the delamination around the cathode and anode interface regions which may be due to either the surface finish of the flange influencing its adhesion with the polymer or the moulding process parameters and procedures, additional studies are required in the future to improve the flange and housing adhesion.

- **Chapter 10: 125 mm housing design using Taguchi method**

The influence of the different geometrical parameters of the thyristor housing was also investigated using the Taguchi method of experimental design (TMED) to assist with the design of a larger

package for 125 mm diameter devices in this chapter. In this study, the relationships between electrical stress and different geometric values were studied along with identifying the optimum design values to minimise the electrical field in the 125 mm housing. As a result of this investigation, strong interactions were observed between the copper pole thickness and the number of convolutes, and also between the package wall thickness and the convolute number. As observed from studies in Chapter 8, the different geometrical parameters were also seen to have varying influences on the electrical stress in the housing. For example, when the diameter of the copper pole piece was changed, the change in the electric field was seen to be less significant than compared to the variation in the pole piece thickness and the flange separation between cathode and anode ends. From the TMED studies, a lower electric field was also observed to occur in the 125 mm housing when the dimensions of the flange separation between the cathode and anode ends, package thickness, distance between the pole piece and insert location along the housing and the number of convolutes were maximised.

### **11.2.1 Design & Design-for-manufacture recommendations**

Based on the different studies that were performed during this project, a number of design recommendations were identified to assist the development of future larger diameter polymer thyristor housings, and ensure the electric magnitude within them is low (most specifically at the flange/housing interface). They are grouped in the following categories:

- **Flange design**

- *Flange shape:*

- To ensure the electrical field magnitude is low at the interface region, a 45° curved flange whose end is also rounded should ideally be used in polymeric housings for thyristor devices. This design will ensure the maximum electric field region is located along the flange curvature,

rather than at the flange tip, to prevent partial discharge failure of the package. Increasing its radius of curvature will also ensure the electric field at the interface is kept low. However, determining the appropriate radius of curvature dimension should be according to the manufacturing feasibility of the flange and the housing thickness.

- *Flange location:*

In the housing, the flange should ideally be positioned so that the high electric field region at the flange/housing interface is not influenced by either the inside housing wall or the housing convolute corners. For the maximum field region to be located along its curvature, the curved flange should ideally be located in the middle of the housing and at a depth that is more than the convolute height corner. For injection moulding reasons, a spacing of at least 1 mm should be maintained between the flange tip and housing outside wall when identifying the radial position of the flange.

- *Housing convolute design:*

The dimension of the radius of curvature around the housing convolute corners should be selected based on the ease to manufacture the mould tool for the polymer housing moulding. Together with this, identifying the appropriate number of convolutes and its shape should also be associated with the comparative tracking index property of the polymer material to avoid failure due to tracking along the housing exterior.

- **Materials selection**

- *Polymer material:*

Varying the electrical conductivity of the polymer housing does not cause significant changes in the electrical field magnitude in the housing. Although the glass-filled polyimide polymer was used for the 50 mm prototype, other plastics (ideally cheaper) can also be considered in the future to develop larger size housings. Instead of

electrical conductivity property, the housing material choice should be rather based on other critical properties, such as moisture permeability.

- *Housing cavity fillers:*

Changing the electrical conductivity of the internal cavity of the housing also does not result in significant variation in the electrical field magnitude in the housing. Although the electrical performance of silicone gel and dry nitrogen fillers were studied in this project, in case other appropriate fillers are identified in the future, their choice should ideally be based on other properties, e.g. moisture permeability, thermal stability, rather than their electrical conductivity.

- **Other design features**

- *Copper pole piece size:*

The diameter of copper pole piece does not also have a significant influence on the electrical field in the housing. For future development works, choice of the copper pole piece diameter can be based on factors, such as manufacturability and availability, instead of the electrical properties of the copper material.

### **11.3 Future work**

The research activities discussed in this thesis have successfully helped develop a prototype polymer-based housing for a 50 mm diameter thyristor, and through doing so have enabled identification of different challenges that can be applied to the development of a larger size polymer package. These are outlined next.

- **Delamination defect elimination:**

The first area where further work is required regards the defects that were observed in the moulded 50 mm prototypes. From the dye penetrant test that were performed on these housings, delamination

between the flange insert and the polymer housing were seen at the cathode and anode ends interface regions. These highlight that either poor adhesion exists between the flange and polymer material, or the defect is due to the moulding procedures and process used to mould the 50 mm prototype. Additional work will thus be required in the future to improve the flange and polymer material adhesion to avoid moisture ingress in the housing through the separation. Example of some investigations that would potentially resolve this issue include a re-evaluation of the procedures and parameters used in the moulding process for the 50 mm prototypes moulding, study of the influence of the surface finish of the insert on the adhesion property between the polymer material and flange, and also potentially consider the use of adhesion promoters.

- **Identifying plasticity limit of polymer housing:**

Although other accelerated life test experiments (not been discussed in this thesis) were also conducted in the NEWTON project to understand the physics-of-failure of the polymer housing for the purpose of larger housing development, additional simulation studies in the future would also help broaden the knowledge in the area. One such study lies in a more accurate study of the thermo-mechanical behaviour of the housing when it is exposed to a range of temperature changes. As highlighted in Chapter 9, an accurate thermo-mechanical simulation study of the housing was not possible in this project due to lack of published data on the physical properties of the selected polymer. Through additional works to characterise the physical properties of the polymer, parameters, such as the temperature limit where onset of plasticity starts to occur in the polymer, can be accurately determined and help protect the housing from premature failure through either design changes or by controlling the temperatures in which the housing is stored, or to which it will be exposed to during service.



- **Moisture diffusion:**

As highlighted in Chapter 3, failure of an electronic package due to corrosion and among others cracking will normally occur when it is exposed to a humidity environment. Because polymers are permeable to moisture allowing them to diffuse through, characterisation of the permeability property of the selected polyimide polymer (not performed at this stage of the project) is also required in the future. This will help assess the polymer reliability and suitability for the thyristor device.

- **Comparative Tracking Index (CTI) characterisation:**

Together with the moisture permeability property, the CTI of the selected polymer material has also not been characterised in this project. Because polymer package will be exposed to high voltage gradients during service, in case the polymer material has a low CTI value, failure of the housing due to tracking can occur. To ensure the housing is reliable, future characterisation of the CTI value of the selected polymer material is thus important. In case the concerned value is found to be low, scopes to coat the housing with materials, such as PTFE, can then also be investigated in the future.

- **Explosion resistance:**

As discussed in Chapter 2, together with short-circuit failure, failure due to explosion is also another reliability issue that can lead to the housing being destroyed mechanically. Because an explosion failure will lead to unplanned maintenance issues during the normal service of the device, determining the housing resistance to explosion failure is another critical area of study for the future.

- **Housing cost:**

Another area where additional work is required concerns determining the actual cost of the larger size 125 mm and 150 mm polymeric housings. To ensure they are successfully commercialised and widely exploited in the future, their cost would be required to be cheaper than

current commercial ceramic packages. Although preliminary cost figures quoted for the 50 mm size polymer housing appear promising compared to a similar size ceramic housing, additional work is still required to determine whether the additional significant investment (based on a revised moulding process for example) needed for the polymeric based thyristor to be successfully applied in the high voltage industry in the future is commercially viable. Because the electrical field in the housing were not observed to have a significant variation when the electrical conductivity is changed, the scope to use a cheaper plastic that will not degrade and ensure the reliable operation of the thyristor can also be exploited in the future. Using a cheaper polymer will also enhance the commercial value of the thyristor housing.

## Reference

- ABDULLAH, S., ABDULLAH, M.F., ARIFFIN, A.K. and JALAR, A., 2009. Thermal-mechanical analysis of a different leadframe thickness of semiconductor package under the reflow process. *American Journal of Applied Sciences*, **6**(4), 616-625.
- AHMAD, K.K., 2009. *Novel polymer-based packaging technologies for high power semiconductors*. M. Phil edn., Department of Materials, Loughborough University. Loughborough, UK.
- AHMED, N. and SRINIVAS, N., 2001. Partial discharge severity assessment in cable system, *Transmission and Distribution Conference and Exposition IEEE/PES 2001, October 28, 2001 - November 2, Atlanta, GA, United states* 2001 2001, Institute of Electrical and Electronics Engineers Inc pp849-852.
- AL-SHEIKHLY, M. and CHRISTOU, A., 1994. How radiation affects polymeric materials. *IEEE Transactions on Reliability*, **43**(4), 551-556.
- AMBAT, R., JENSEN, S.G. and MAILER, P., 2008. Corrosion reliability of electronic systems, *Corrosion General Session - 211th ECS Meeting, May 6, 2007 - May 11, Chicago, IL, United states* 2007 2008, Electrochemical Society Inc pp17-28.
- ANAWA, E.M., OLABI, A.G. and HASHMI, M.S.J., 2008. Application of Taguchi method to optimise dissimilar laser welded components. *International Journal of Manufacturing Technology and Management*, **15**(2), 219-227.
- ARDEBILI, H. and PECHT, M.G., 2009. *Encapsulation technologies for electronic applications*. 1st edn. Burlington, USA: Elsevier.
- ARRILLAGA, J., 1998. Chapter 1: Introduction. *High Voltage Direct Current Transmission*. 2nd edn. London, UK: The Institution of Electrical Engineers, pp. 1-9.
- ASPLUND, G., CARLSSON, L. and TOLLERZ, O., 4, 2003a-last update, 50 YEARS HVDC PART 1: ABB - FROM PIONEER TO WORLD LEADER [Homepage of The ABB Group], [Online]. Available: <http://search.abb.com/library/ABBLibrary.asp?DocumentID=03MC0127&LanguageCode=en&DocumentPartID=1/2&Action=Launch> [11/02, 2007].
- ASPLUND, G., CARLSSON, L. and TOLLERZ, O., 04, 2003b-last update, 50 YEARS HVDC PART II: THE SEMICONDUCTOR TAKEOVER [Homepage of The ABB Group], [Online]. Available:

<http://search.abb.com/library/ABBLibrary.asp?DocumentID=03MC0128&LanguageCode=en&DocumentPartID=2/2&Action=Launch> [11/02, 2007].

AVISON, J., 1989. Chapter 12: Electric currents. *The World of Physics*. 2nd edn. Cheltenham UK: Thomas Nelson and Sons Ltd, pp. 251.

Bahlinger W., Egerbacher W. and Martin H., 1975, *Thyristor housing assembly*, US 3886586, United States.

BAJENESCU, T.I. and BAZU, M.I., 1999. *Reliability of electronic components: a practical guide to electronic systems manufacturing*. Berlin; New York: Springer.

BAKER, T.B., 1990. *Engineering quality by design: interpreting the Taguchi approach*. New York; Milwaukee: Marcel Dekker.

BARLOW III, F.D., 1999. *Electronic packaging strategies for high current DC to DC converters*, Virginia Polytechnic Institute and State University.

BARREAU, L., PRUNET, P. and SERRE, C., 2008. Shock test evaluation for electronic packages, *2008 2nd Electronics Systemintegration Technology Conference, ESTC, September 1, 2008 - September 4*, Greenwich, United kingdom 2008 2008, Inst. of Elec. and Elec. Eng. Computer Society pp1209-1212.

BING, L., NYE, T.J. and METZGER, D.R., 2006. Multi-objective optimization of forming parameters for tube hydroforming process based on the Taguchi method. *The International Journal of Advanced Manufacturing Technology*, **28**(1-2), 23-30.

Brandt J., Herold L., Pikorz W. and Sonntag A., 1980, *Semiconductor device plastic jacket having first and second annular sheet metal strips with corrugated outer edges embedded in said plastic jacket*, 4240099, United States.

BRÜTSCH, R., TARI, M., FRÖHLICH, K., WEIERS, T. and VOGELSANG, R., 2008. Insulation Failure Mechanisms of Power Generators. *IEEE Electrical Insulation Magazine*, **24**(4), pp. 17-25.

CENELEC, 2001. *High-voltage test techniques - Partial discharge measurements*. IEC 60270:2000. UK: British Standard.

CENGEL, Y.A., 2003. Chapter1: Basics of heat transfer. *Heat transfer: a practical approach*. 2nd Ed. edn. New York; London: Mc Graw-Hill, pp. 26.

Cleford A. P. , 1970, *Encapsulated semiconductor elements*, 1188452, United Kingdom.

CLOUGH, R.W., 1960. The finite element in plane stress analysis, *2nd ASCE Conference on Electronic Computation*, September 1960, .

COMSOL AB, 2010-last update. Available: [www.comsol.com](http://www.comsol.com) [08/01, 2010].

COMSOL AB., 2007a. *Comsol Multiphysics Modelling Guide*. COMSOL 3.4 edn.

COMSOL AB., 2007b. *Structural Mechanics Module User's Guide*. COMSOL 3.4 edn.

DAI, L., ed, 2006. *Carbon Nanotechnology: Recent Developments in Chemistry, Physics, Materials Science and Device Applications*. 1st edn. Oxford, UK: Elsevier Science.

DASGUPTA, A. and PECHT, M., 1991. Material failure mechanisms and damage models. *IEEE Transactions on Reliability*, **40**(5), 531-536.

DASGUPTA, A. and HU, J.M., 1992. Failure-mechanism models for excessive elastic deformation. *IEEE Transactions on Reliability*, **41**(1), 149-154.

De Bruyne P. and Niemeyer L., 1979, *Arrangement for semiconductor power components*, 4162514, United States.

DE LAMBILLY, H. and KESER, H.O., 1993. Failure analysis of power modules: A look at the packaging and reliability of large IGBT's. *IEEE transactions on components, hybrids, and manufacturing technology*, **16**(4), 412-417.

DI GIACOMO, G., 1997. *Reliability of electronic packages and semiconductor devices*. New York; London: McGraw-Hill.

DIETER, G.E., 2000. *Engineering design: a materials and processing approach*. 3 edn. Boston: Mc Graw-Hill.

DOSHI, J.P., 1998. Chapter 1: Preliminary Concepts. *Analytical Methods in Engineering*. New Delhi: Narosa Publishing House, pp. 1 - 12.

DRESBACH, C., KNOLL, H., SCHISCHKA, J., PETZOLD, M., HOSSEINI, K. and SCHRAPLER, L., 2007. Test methods for characterizing the local plastic deformability of bonding wires, *ESTC 2006 - 1st Electronics Systemintegration Technology Conference, September 5, 2006 - September 7, Dresden, Saxony, Germany* 2006 2007, Institute of Electrical and Electronics Engineers Inc pp732-740.

FABIAN, J.H., HARTMANN, S. and HAMIDI, A., 2005. Analysis of Insulation Failure Modes in High Power IGBT Modules, *Industry Applications Conference, 2005. 40th IAS Annual Meeting. Conference Record of the 2005*, Oct. 2-6 2005, pp799-805.

FAN, X., ZHOU, J. and CHANDRA, A., 2008. Package structural integrity analysis considering moisture, *2008 58th Electronic Components and Technology Conference, ECTC, May 27, 2008 - May 30, Lake Buena Vista*,

FL, United states 2008 2008, Institute of Electrical and Electronics Engineers Inc pp1054-1066.

GALLOWAY, J.E. and MILES, B.M., 1997. Moisture absorption and desorption predictions for plastic ball grid array packages. *IEEE transactions on components, packaging, and manufacturing technology. Part A*, **20**(3), 274-279.

GAUTHIER, N., 1990. *Radius of curvature and charge accumulation near points*.

Gerstenkoper H. and Juchmann H., 1980, *Disc-shaped semiconductor device having an annular housing of elastomer material*, 4188637, United States.

GOCKENBACH, E., 2001. Chapter 17 - Partial discharge measuring technique. In: H.M. RYAN, ed, *High voltage engineering and testing*. 2nd edn. London: The Institution of Electrical Engineers, pp. 533-548.

GOOSEY, M., 1999. Chapter 1: Introduction to polymers and their important properties for electronic applications. *Plastics for electronics*. Netherlands: Kluwer Academic Publishers, pp. 1-24.

Gunturi S. and Schnelder D., 2004, *Press pack power semiconductor module*, EP1403923, EU.

GUOQIANG, Z., YUANLU, Z. and XIANG, C., 1999. Optimal design of high voltage bushing electrode in transformer with evolution strategy. *IEEE Transactions on Magnetics*, **35**(3), 1690-1693.

HOFFMAN, J.D., 1957. The mechanical and electrical properties of polymers: an elementary molecular approach. *IRE transactions on component parts*, **4**(2), 42-69.

HUEBNER, K.H., DEWHIRST, D.L., SMITH, D.E. and BYROM, T.G., 2001. Meet the Finite Element Method. *The finite element method for engineers*. 4th edn. United States of America: John Wiley & Sons Inc., pp. 3 -15.

IEEE-SA STANDARDS BOARD, 1998. *IEEE standard reliability program for the development and production of electronic systems and equipment - IEEE Std 1332-1998*. The IEEE Inc. New York, USA.

JAMES, J., KULKARNI, S.V. and PAREKH, B.R., 2009. Partial Discharge in High Voltage Equipments-HV Cable, *Proceedings of the 9th International Conference on Properties and Applications of Dielectric Materials*, July 19-23 2009, pp445-449.

JANSSEN, H., SEIFERT, J.M. and KARNER, H.C., 1999. Interfacial phenomena in composite high voltage insulation. *IEEE Transactions on Dielectrics and Electrical Insulation*, **6**(5), 651-659.

Kiyohara T. , 1983, *Thyristor with self-centering housing means*, US 4677454, United States.

Lang T. and Zeller H. R., 1999, *Short-circuit resistant IGBT module*, US 6426561, United States.

LESCALE, V.F., ASTROM, U., NUNES, J., WEIMERS, L. and WU, D., 2010. *Power transmission with HVDC at 800kV*.  
[http://www05.abb.com/global/scot/scot221.nsf/veritydisplay/8e4000a3468ecd9c12571d90031659e/\\$File/B4\\_106.pdf](http://www05.abb.com/global/scot/scot221.nsf/veritydisplay/8e4000a3468ecd9c12571d90031659e/$File/B4_106.pdf) edn., The ABB Group.

LI, C.Y., HUA, Z.K., LUO, Y.X., CAO, L.Q. and ZHANG, J.H., 2008. Investigation of the moisture impact on the stacked die package, *2008 2nd Electronics Systemintegration Technology Conference, ESTC, September 1, 2008 - September 4*, Greenwich, United kingdom2008 2008, Inst. of Elec. and Elec. Eng. Computer Society pp1175-1178.

LIN, T.Y., XIONG, Z.P., YAO, Y.F., TOK, L., YU, Z.Y., NJOMAN, B., CHUA, K.H. and MA, Y.Y., 2003. Failure analysis of full delamination on the stacked die leaded packages. *Journal of Electronic Packaging, Transactions of the ASME*, **125**(3), 392-399.

LINDER, S., 2010a. *Power Semiconductors - Part One: Basics and applications*(ABB review /2006).  
<http://www02.abb.com/global/abbzh/abbzh251.nsf!OpenDatabase&db=/global/gad/gad02077.nsf&v=19EA6&e=us&c=720055C14D533EAEC125722E0033E120&m=6d56> edn., The ABB Group.

LINDER, S., 2010b. *Power Semiconductors - Part Two: Housing Technology and Future Developments* (ABB review 1/2007).  
<http://www.abb.com/cawp/abbzh252/AA869EF2772FCA0DC1257284002AA5CB.aspx#> edn., The ABB Group.

LIPS, H.P., 1998. Technology trends for HVDC thyristor valves, *Power System Technology, 1998. Proceedings. POWERCON '98. 1998 International Conference on*, 1998, pp451-455 vol.1.

LITTLEFUSE, I., 2008-last update, Teccor brand Thyristors. Available: [http://www.littelfuse.com/data/en/Application\\_Notes/an1009.pdf](http://www.littelfuse.com/data/en/Application_Notes/an1009.pdf) [02/25, 2011].

MACKEVICH, J. and SHAH, M., 1997. Polymer outdoor insulating materials. Part I: Comparison of porcelain and polymer electrical insulation. *Electrical Insulation Magazine, IEEE*, **13**(3), 5-12.

MADDURI, S., SAMMAKIA, B.G., INFANTOLINO, B. and CHAPARALA, S., 2008. A review of non-hermetic optoelectronic packaging, *2008 11th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, I-THERM, May 28, 2008 - May 31*, Orlando, FL, United states2008 2008, Inst. of Elec. and Elec. Eng. Computer Society pp913-919.

MATHIEU, B. and DASGUPTA, A., 1993. Stress analysis of glass-to-metal lead seals, *Proceedings of the ASME Winter Conference, November 28, 1993 - December 3, New Orleans, LA, USA* 1993 1993, Publ by ASME pp1-7.

MCCOMB, G. and BOYSEN, E., 2005. Obeying Ohm's Law. *Electronics For Dummies*. 2nd edn. Indianapolis, United States of America: Wiley Publishing Inc., pp. 54.

Merlin M., Torti A. and Santi S., 2003, *Compression assembled electronic package having a plastic molded insulation ring*, 0141517, United States.

MITIC, G. and LEFRANC, G., 1999. Localisation of electrical-insulation- and partial-discharge failures of IGBT modules, *Proceedings of the 1999 IEEE Industry Applications Conference - 34th IAS Annual Meeting, October 3, 1999 - October 7, Phoenix, AZ, USA* 1999 1999, IEEE pp1453-1458.

MITLEHNER, H. and SCHULZE, H., 1988. *Thyristors for HVDC transmission*.

MOORE, T.D. and JARVIS, J.L., 2001. Improved reliability in small multichip ball grid arrays. *Microelectronics Reliability*, **41**(3), 461-469.

N. MONSUR, V.K. SOOD and L. LOPES, 2006. Modeling a Hybrid Diode-Thyristor HVDC Rectifier in EMTP-RV, *Electrical and Computer Engineering, 2006. CCECE '06. Canadian Conference on*, 2006, pp1258-1262.

NAIDU, M.S. and KAMARAJU, V., 2009. Chapter 1: Introduction. *High Voltage Engineering*. 4th edn. New Delhi, India: Tata McGraw-Hill Publishing Company Ltd, pp. 1-24.

NATIONAL MATERIALS ADVISORY BOARD, 1983. *Non-destructive evaluation of metal matrix composites*. NMAB-413. Washington, D.C.: National Academy Press.

NEI, L. and PECHT, M., 2007. Regulations and market trends in lead-free and halogen-free electronics. *Circuit World*, **33**(2), 4-9.

NIED, H.F., 2003. Mechanics of interface fracture with applications in electronic packaging. *IEEE Transactions on Device and Materials Reliability*, **3**(4), 129-143.

OMIYA, M., KISHIMOTO, K. and AMAGAI, M., 2005. Fatigue crack growth in lead-free solder joints, *EMAP 2005: 2005 International Symposium on Electronics Materials and Packaging, December 11, 2005 - December 14, Tokyo, Japan* 2005 2005, Inst. of Elec. and Elec. Eng. Computer Society pp232-237.

PALANIKUMAR, K. and DAVIM, J.P., 2009. Assessment of some factors influencing tool wear on the machining of glass fibre-reinforced plastics by coated cemented carbide tools. *Journal of Materials Processing Technology*, **209**(1), 511-519.



PARLIAMENTARY OFFICE OF SCIENCE AND TECHNOLOGY, 2001. *UK Electricity Networks*. <http://www.parliament.uk/documents/post/pn163.pdf> edn., The Parliamentary Office of Science and Technology. London UK.

PEACE, G.S., 1992. Chapter 1: Conceptual Background. *Taguchi methods: a hands-on approach*. Reading, Massachusetts: Addison-Wesley, pp. 1-10.

PECHT, M.G., AGARWAL, R., MCCLUSKEY, P., DISHONGH, T., JAVADPOUR, S. and MAHAJAN, R., 1999. Chapter 1: Properties of Electronic Packaging Materials. United States of America: CRC Press, pp. 3-20.

PHILLIPS, A.G., KUFFEL, J., BAKER, A., BURNHAM, J., CARREIRA, A., CHERNEY, E., CHISHLOM, W., FARZANEH, M., GEMIGNANI, R., GILLESPIE, A., GRISHAM, R., HILL, R., SAHA, T., VANCIA, B. and YU, J., 2008. Electric Fields on AC Composite Transmission Line Insulators. *IEEE Transactions on Power Delivery*, **23**(2), 823.

PILLAI, A.S. and HACKAM, R., 1984. ELECTRIC FIELD DISTRIBUTION AT SOLID INSULATOR-VACUUM (OR GASEOUS) INTERFACE OF DIFFERENT ELECTRODE-INSULATOR GEOMETRIES. *IEEE Conference Record of 1983 Interfacial Phenomena in Practical Insulating Systems*. Gaithersburg, MD, USA1984, IEEE pp5-11.

PODLESK, T.F., SINGH, H., BEHR, S. and SCHNEIDER, S., 1996. A compact lightweight 125mm thyristor for pulse power applications, *Twenty-second International Power Modulator Symposium*, 25-27 June 1996, pp43-46.

RADIOJEVIC, Z., ABDUL-QUADIR, Y., MYLLYKOSKI, P. and RANTALA, J., 2006. Reliability prediction for TFBGA assemblies. *IEEE Transactions on Components and Packaging Technologies*, **29**(2), 379-384.

RAMO, S., WHINNERY, J.R. and VAN DUZER, T., 1994. *Fields and waves in communication electronics*. 3rd edn. 1994: Wiley.

RASHID, M.H., 2007. Chapter 6: Thyristors. *Power electronics handbook: devices, circuits, and applications*. 2nd edn. Burlington, USA: Elsevier Academic Press, pp. 89.

REGARD, C., GAUTIER, C., FREMONT, H., VAL, A., ROULLIER, F., SCHWINDENHAMMER, P. and POIRIER, P., 2008. Solder fatigue of Wafer Level Package assemblies. comparison with flip Chip BGA'S, *EuroSimE 2008 - International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Micro-Systems*, April 20, 2008 - April 23, Freiburg im Breisgau, Germany2008 2008, Inst. of Elec. and Elec. Eng. Computer Society.

Rohsler I. C. , 1982, *A semiconductor package*, 0064383, EU.

ROY, R.K., 1990. *A primer on the Taguchi method*. New York: Van Nostrand Reinhold.

ROYLANCE, D., 02/28, 2001-last update, Finite Element Analysis [Homepage of Department of Materials Science and Engineering, Massachusetts Institute of Technology], [Online]. Available: <http://ocw.mit.edu/courses/materials-science-and-engineering/3-11-mechanics-of-materials-fall-1999/modules/fea.pdf> [11/10, 2010].

RUDERVALL, R., CHARPENTIER, J.P. and SHARMA, R., 2010. *High Voltage Direct Current (HVDC) transmission systems technology review paper*.  
[http://www05.abb.com/global/scot/scot221.nsf/veritydisplay/9e64dab39f71129bc1256fda004f7783/\\$File/Energyweek00.pdf](http://www05.abb.com/global/scot/scot221.nsf/veritydisplay/9e64dab39f71129bc1256fda004f7783/$File/Energyweek00.pdf) edn., The ABB Group.

SAMPEI, M., YAMADA, T., TANABE, S., TAKEDA, H. and KOBAYASHI, S., 1997. Secular change in characteristics of thyristors used in HVDC valve. *IEEE Transactions on Power Delivery*, **12**(3), 1159-1167.

SCHLEGEL, R., HERR, E. and RICHTER, F., 2001. Reliability of non-hermetic pressure contact IGBT modules. *Microelectronics Reliability*, **41**(9-10), 1689-1694.

SCHNABLE, G.I., REISS, E.M. and VINCOFF, M., 1976. RELIABILITY OF HERMETICALLY-SEALED CMOS INTEGRATED CIRCUITS. *IEEE Electron and Aerosp Syst Conv (EASCON '76), Rec.*

SESHU, P., 2003. Chapter 1: Introduction. *Textbook of finite element analysis*. New Delhi: Prentice-Hall of India Private Limited, pp. 1-15.

SHASHOUA, Y., 2008. *Conservation of plastics: materials science, degradation and preservation*. 1st edn. Oxford, UK: Butterworth-Heinemann.

SMITH, E.H., 1998. *Mechanical Engineers Reference Book*. Elsevier Butterworth-Heinemann.

STOMBERG, H., ABRAHAMSSON, B. and SAKSVIK, O., 2010. *Modern HVDC Thyristor Valves*.  
[http://www05.abb.com/global/scot/scot221.nsf/veritydisplay/1402c60973f47e72c1256fda004aead8/\\$File/thyrvalv.pdf](http://www05.abb.com/global/scot/scot221.nsf/veritydisplay/1402c60973f47e72c1256fda004aead8/$File/thyrvalv.pdf) edn., The ABB Group.

SUHIR, E., 2007. *Accelerated life testing (ALT) in microelectronics and photonics: Role, Attributes, Challenges, Pitfalls and Interaction with Qualification Testing*. IEEE sponsored course edn., Greenwich, UK.

SUN, P., LEUNG, V.C., XIE, B., MA, V.W. and SHI, D.X., 2008. Warpage reduction of package-on-package (PoP) module by material selection process optimization, *2008 International Conference on Electronic Packaging Technology and High Density Packaging, ICEPT-HDP 2008, July 28, 2008 - July 31, Pudong, Shanghai, China* 2008, Inst. of Elec. and Elec. Eng.

Computer Society ppChina Electronics Packaging Society CEPS, China Inst. Electronics; Fudan University; The Component, Packaging, Manuf. Technol. Soc. IEEE (IEEE-CPMT); The International Microelectronics and Packaging Society (IMAPS).

SURESH KUMAR, K.S., 2009. Waveform Symmetry and Fourier Series Coefficients. *Electric Circuits and Networks*. 1st edn. Delhi, India: Dorling Kindersley, pp. 536 - 539.

TADROS, T. and BAINS, G., 1989. Design considerations for semiconductor packaging (effects of semiconductor package reliability and life expectancy), *Main Line Railway Electrification, 1989., International Conference on*, 1989, pp265-269.

TANAKA, Y., ONO, T., SAMPEI, M., OBATA, T., TANABE, S., TSUCHIE, E. and MURAOKA, T., 1999. Long-term test of the equipment for &plusmn;500 kV DC converter station, *Power Engineering Society Summer Meeting, 1999. IEEE*, 1999, pp1152-1157 vol.2.

TEST, H., 1988. Trends in semiconductor packaging, a merchant house view, *Customs Integrated Circuits Conference, 1988., Proceedings of the IEEE* 1998, 05/16 - 05/19 1988, IEEE pp23.2/1-23.2/3.

THEIS, C.D., SICONOLFI, D.J., COMIZZOLI, R.B., KIELY, P.A., WU, P., CHAKRABARTI, U.K. and OSENBACH, J.W., 2000. Highly accelerated life testing for non-hermetic laser modules, *50th Electronic Components and Technology Conference*, Las Vegas, NV, USA2000, IEEE pp955-961.

TOUNSI, P., CHAUFFLEUR, X., DORKEL, J.-., FRADIN, J.-., DUPUY, P., MARTY, A. and DERAM, A., 2004. Thermo-mechanical stress modelling of MOS device with electro- Thermal considerations, *Proceedings of the 5th International Conference on Thermal and Mechanical Simulation and Experiments in Microelectronics and Microsystems, EuroSimE 2004, May 10, 2004 - May 12, Brussels, Belgium2004* 2004, Institute of Electrical and Electronics Engineers Inc pp41-46.

TSAI, C.S. and MORT, N., 1996. Simulation and optimisation in manufacturing systems using Taguchi methods, *Part 1 (of 2), September 2, 1996 - September 5, Exeter, UK1996* 1996, IEE pp467-472.

TUMMALA R R, 2005. Packaging: Past, Present and Future, *6th International Conference on Electronic Packaging Technology*, 30/08 - 02/09 2005, IEEE pp3-7.

VAKSER, B.D. and NINDRA, B.S., 1994. Insulation problems in high voltage machines. *IEEE Transactions on Energy Conversion*, **9**(1), 143-151.

VETTRAINO, L.G. and RISBUD, S.H., 1999. Current trends in military microelectronic component packaging. *Components and Packaging Technologies, IEEE Transactions on*, **22**(2); addressed. A recent U.S. Air

Force (reliability without hermeticity [RWOH]) study and follow on work, conducted by the joint military/industry plastic package availability (PPA) program, investigated the use of two ceramic layers ( $\text{SiO}_2$ /(TRUNCATED)), 270-281.

WANG, K., POMMERENKE, D., CHUNDRU, R., VAN DOREN, T., DREWNIAK, J.L. and SHASHINDRANATH, A., 2003. Numerical modeling of electrostatic discharge generators. *IEEE Transactions on Electromagnetic Compatibility*, **45**(2), 258-271.

WELLEMAN, A. and FLEISCHMANN, W., 2003. High current, high di/dt semiconductor devices for single- and repetitive pulse applications, *Pulsed Power Conference, 2003. Digest of Technical Papers. PPC-2003. 14th IEEE International*, 2003, pp1213-1216 Vol.2.

WONG, C.P., SEGELKEN, J.M. and BALDE, J.W., 1989. Understanding the use of silicone gels for non-hermetic plastic packaging, *Electronic Components Conference, 1989. Proceedings., 39th*, 1989, pp769-776.

WOOD, J., 1994. Finite element analysis of composite structures. *Composite Structures*, **29**, 219-230.

WOODHOUSE, M., 2007a. *NEWTON project work package 1: Requirements Specification*. Areva T&D. Stafford, UK.

WOODHOUSE, M., 2007b. *NEWTON Project: An introduction to HVDC thyristor valves*. NEWTON project presentation edn., Stafford, UK.

XIE, D.J. and WANG, Z.P., 1998. Process capability study and thermal fatigue life prediction of ceramic BGA solder joints. *Finite Elements in Analysis and Design*, **30**(1), 31-45.

XUE, K., WU, J., CHEN, H., SUN, Y., KWAN, K., YUEN, J. and LAM, A., 2008. Numerical analysis of interfacial delamination in thin array plastic package, *2008 International Conference on Electronic Packaging Technology and High Density Packaging, ICEPT-HDP 2008, July 28, 2008 - July 31*, Pudong, Shanghai, China 2008, Inst. of Elec. and Elec. Eng. Computer Society ppChina Electronics Packaging Society CEPS, China Inst. Electronics; Fudan University; The Component, Packaging, Manuf. Technol. Soc. IEEE (IEEE-CPMT); The International Microelectronics and Packaging Society (IMAPS).

YAO, Y.F., LIN, T.Y. and CHUA, K.H., 2003. Improving the deflection of wire bonds in stacked chip scale package (CSP), *53rd Electronic Components and Technology Conference 2003, May 27, 2003 - May 30*, New Orleans LA, United states 2003, Institute of Electrical and Electronics Engineers Inc pp1359-1363.

YOUNG, W.C. and BUDYNAS, R.G., 2000. Chapter 8: Beams; Flexure of straight bars. In: R.J. ROARK and R.G. BUDYNAS, eds, *Roark's formulas for stress and strain*. 7th edn. New York: Mc Graw-Hill, pp. 125.

ZEUS INC, 10/09, 2010-last update, Dielectric properties of polymers.

Available:

[http://www.zeusinc.com/UserFiles/zeusinc/Documents/Zeus\\_Dielectric.pdf](http://www.zeusinc.com/UserFiles/zeusinc/Documents/Zeus_Dielectric.pdf)

[10/09, 2010].

# Appendix 1

In this appendix, a summary of the various patents identified from the literature review is provided. The patents describe different thyristor housing designs that have been developed over the years.

TITLE	Author	Type of device	Housing Type	Housing material	Comments	Additional remarks
SEMICONDUCTOR DEVICE PLASTIC JACKET HAVING FIRST AND SECOND ANNULAR SHEET METAL STRIPS WITH CORRUGATED OUTER EDGES EMBEDDED IN SAID PLASTIC JACKET	Brandt et al. (1980)	Thyristor	Press-pack	Epoxy resins	Refers to the manufacture methods of thyristors	
DISC-SHAPED SEMICONDUCTOR DEVICE HAVING AN ANNULAR HOUSING OF ELASTOMER MATERIAL	Gerstenkoper et al. (1980)	Thyristor/Rectifier Diode	Press-pack	Elastomer	Relates to the development of a semiconductor package of elastomer material.	A tight fit assembly is enhanced by a toothed profile of the inner wall of the housing
COMPRESSION ASSEMBLED ELECTRONIC PACKAGE HAVING A PLASTIC MOLDED INSULATION RING	Merlin et al. (2003)	Thyristor/MOSFET/IGBT	Press-pack	Plastic	Refers to designs of gate leads connecting the gate electrode to an external circuit	
A SEMI-CONDUCTOR PACKAGE	Rohsler (1982)	Thyristor	Press-pack	Synthetic resin	Relates to the semiconductor package used as a thyristor chopper circuit	
ENCAPSULATED SEMICONDUCTOR ELEMENTS	Cleford (1970)	Thyristor	Press-pack	Ceramic	Describes the design of 2-part semiconductor housing	It consists of a 2-part housing
IMPROVEMENTS IN OR RELATING TO SEMICONDUCTORS COMPONENTS	Siemens Aktiengesellschaft (1974)	Thyristor	Press-pack	Ceramic ( <i>possibly</i> )	Refers to the manufacture methods of thyristors	It consists of a 2-part housing
SEMICONDUCTORS DEVICES AND THEIR MANUFACTURE	Collier et al. (1970)	Thyristor	Press-pack	Ceramic ( <i>possibly</i> )	Refers to the manufacture methods of thyristors	
SEMICONDUCTOR DEVICES	Lord et al. (1972)	Control rectifiers	Press-pack	Ceramic	Refers to an assembly of semiconductor control rectifiers	
THYRISTOR HOUSING ASSEMBLY	Bahlinger et al. (1975)	Thyristor	Press-pack	Alumium oxide	Refers to the manufacture methods of thyristors	Spring gate terminal
THYRISTOR HAVING AN IMROVED COOLING AND IMPROVED HIGH FREQUENCY OPERATION WITH ADJACENT TERMINALS	Lehmann et al. (1979)	Thyristors	Press-pack	Ceramic ( <i>possibly</i> )	Relates to semiconductor devices having a plurality of control lines	Semiconductor device with at least 1 control line
THYRISTOR WITH SELF-CENTERING HOUSING MEANS	Kiyohara (1983)	LTT	Press-pack	Ceramic	Refers to an LTT device wherein the alignment of the light guide and photosensitive portion of the LTT element is improved.	
PACKAGE FOR LIGHT-TRIGGERED SEMICONDUCTOR DEVICE	Electric Power Research Institute Inc (1977)	LTT	Press-pack	Alumina ceramic	Refers to a hermetically sealed LTT device	
SEMICONDUCTOR ARRANGEMENTS	Siemens Schurkertwerke Aktiengesellschaft (1968)	Rectifier & Thyristor	Press-pack	Ceramic	Describes novel constructions of rectifiers and thyristor	
THYRISTOR	Weismann et al. (1980)	Thyristor		Ceramic ( <i>possibly</i> )	Describes a thyristor assembly	

METHOD OF MANUFACTURING A THYRISTOR HOUSING	Erkan et al. (1983)	Thyristor	Press-pack	Ceramic	Refers to a gate tube assembly which is hermetically sealed to prevent ingress of contaminants as a result of assembly processes	
ARRANGEMENT FOR POWER SEMICONDUCTOR COMPONENTS	De Bruyne et al. (1979)	Thyristor	Press-pack	Ceramic	Refers to explosion proof housing designs	
PRESS PACK POWER SEMICONDUCTOR MODULE	Gunturi et al. (2004)	IGBT/Thyristor	Press-pack		Describes a semiconductor device that provides enhanced short-circuit failure mode properties	
SHORT-CIRCUIT RESISTANT IGBT MODULE	Lang et al. (1999)	IGBT	Press-pack		Describes a semiconductor device that provides enhanced short-circuit failure mode properties	
A COMPACT LIGHTWEIGHT 125mm THYRISTOR FOR PULSE POWER APPLICATIONS	Podlesak et al. (1996)	Thyristor			Refers to thyristors used for high current milliseconds pulse power applications	
POLYMERIC COMPOSITION FOR PACKAGING A SEMICONDUCTOR ELECTRONIC DEVICE AND PACKAGING OBTAINED THEREFROM	Zafaranna et al. (2002)	Semiconductor device		Polymer	Relates to polymeric composition for electronic package materials	
HIGH VOLTAGE THYRISTOR EQUIPMENT	Eccles et al. (1971)	Thyristor			Refers to a thyristor equipment whereby a better cooling efficiency is achieved	
SEMICONDUCTOR DEVICE	Siemens Schurkertwerke Aktiengesellschaft (1965)	Silicon thyristors, silicon rectifiers	Press-pack	Ceramic	Refers to a silicon rectifier or silicon thyristor semiconductor construction	
HOUSING FOR A GATE TURN-OFF POWER THYRISTOR (GTO)	Almenrader et al. (1990)	GTO	Press-pack	Ceramic	Refers to a GTO having an auxiliary cathode connection	
SEMICONDUCTOR	Kyoto Ceramic Kabushiki Kaisha (1972)	High-frequency power transistor		Ceramic	Refers to the heat dissipative mounting of a high-frequency power transistor	
THYRISTOR TRIGGERING DEVICE	Debus et al. (1989)	LTT			Refers to an LTT device where a single flash lamp is used to trigger multiple thyristors	



Almenrader P. and Diouhy J., 1990, *Housing for a gate turn-off power thyristor (GTO)*, US 4953004, United States.

Bahlinger W., Egerbacher W. and Martin H., 1975, *Thyristor housing assembly*, US 3886586, United States.

Brandt J., Herold L., Pikorz W. and Sonntag A., 1980, *Semiconductor device plastic jacket having first and second annular sheet metal strips with corrugated outer edges embedded in said plastic jacket*, 4240099, United States.

Cleford A. P. , 1970, *Encapsulated semiconductor elements*, 1188452, United Kingdom.

Collier H. A. and Wadsworth R. M., 1970, *Semiconductors devices and their manufacture*, 1191232, United Kingdom.

De Bruyne P. and Niemeyer L., 1979, *Arrangement for semiconductor power components*, 4162514, United States.

Debus G. and Bartscher B., 1989, *Thyristor triggering device*, US 4868461, United States.

Eccles E. M. and Weaver J. J. L., 1971, *High Voltage Thyristor Equipment*, 1218852, England.

Electric Power Research Institute Inc , 1977, *Package for light-triggered semiconductor device*, 1529145, United Kingdom.

Erkan G. and Scott G., 1983, *Method of manufacturing a thyristor housing*, 4420869, United States.

Gerstenkoper H. and Juchmann H., 1980, *Disc-shaped semiconductor device having an annular housing of elastomer material*, 4188637, United States.

Gunturi S. and Schnelder D., 2004, *Press pack power semiconductor module*, EP1403923, EU.

Kiyohara T. , 1983, *Thyristor with self-centering housing means*, US 4677454, United States.

Kyoto Ceramic Kabushiki Kaisha , 1972, *Semiconductor*, 1327352, United Kingdom.

Lang T. and Zeller H. R., 1999, *Short-circuit resistant IGBT module*, US 6426561, United States.

Lehmann E., Martin H. and Voss P., 1979, *Thyristor having improved cooling and improved high frequency operation with adjacent control terminals*, US 4158850, United States.

Lord D. E. and Lootens W. F., 1972, *Semiconductor Devices*, 1299514, United Kingdom.

Merlin M., Torti A. and Santi S., 2003, *Compression assembled electronic package having a plastic molded insulation ring*, 0141517, United States.

PODLESK, T.F., SINGH, H., BEHR, S. and SCHNEIDER, S., 1996. A compact lightweight 125mm thyristor for pulse power applications, *Twenty-second International Power Modulator Symposium*, 25-27 June 1996, pp43-46.

Rohsler I. C. , 1982, *A semiconductor package*, 0064383, EU.

Siemens Aktiengesellschaft , 1974, *Improvements in or relating to semiconductor components*, 1362942, United Kingdom.

Siemens Schurkertwerke Aktiengesellschaft , 1968, *Semiconductor arrangement*, 1113822, United Kingdom.

Siemens Schurkertwerke Aktiengesellschaft , 1965, *Semiconductor device*, 1070484, United Kingdom.

Weismann K. and Kommissari K., 1980, *Thyristor*, GB 2038554, United Kingdom.

Zafaranna R., Scandurra A., Pignataro S., Tenya Y. and Yoshizumi A., 2002, *Polymeric composition for packaging a semiconductor electronic device and packaging obtained therefrom*, US 2002/0022679, United States.

# Appendix 2

In this appendix, a publication that has resulted from the research activities in this project is enclosed.

- *'NOBEEN, N.S., WHALLEY, D.C., HUTT, D.A. and HAWORTH, B., 2010. Computational modelling of electrical field intensity for high voltage semiconductor package design, 2010 International Symposium on Advanced Packaging Materials: Microtech, APM '10, February 28, 2010 - March 2, Cambridge, United kingdom 2010 2010, IEEE Computer Society pp54-59.'*

# Computational Modelling of Electrical Field Intensity for High Voltage Semiconductor Package Design

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## Abstract

Although plastic packaging has successfully replaced ceramic and metal packages for many high reliability electronic packaging applications (e.g. military and aerospace), hermetically sealed ceramic packages are still the dominant technology for large power devices, such as the thyristors and diodes used in high voltage DC (HVDC) power transmission. With increasing energy requirements of growing economies, the demand for higher operating currents is driving suppliers to use larger diameter silicon devices, therefore requiring bigger and more expensive packages. A switch to polymer packaging in such applications has the potential to provide robust and light weight components at a lower cost.

A Finite Element Analysis (FEA) based study aimed at optimising the electrical performance of a polymeric package for such power semiconductors is described in this paper. From the FEA simulations carried out, it was observed that one critical region where the electrical stresses tend to be high, and long-term failure may therefore occur, is in the contact region between the polymer housing and the metal inserts (flanges) which attach the housing to the copper pole pieces of the device. Different design features for the insert edge were studied in order to investigate their influence and to reduce the peak electrical field (E-field) in the critical region. The results showed that the E-field around the contact region decreased as the radii of curvature of the insert ends was increased. A comparison of the E-field magnitude for different insert designs also showed it to be lower around an elliptical insert end compared to circular and straight flange designs. Changes in the depth to which the flange protrudes inside the housing also had a significant effect in the electrical field magnitude in the contact region, whilst variation of other housing design parameters, such as the package thickness and the location of the insert relative to the housing periphery, did not cause the electric field to change significantly.

## 1. Introduction

With the rapid economic growth of large countries such as China, India, Brazil, etc., HVDC transmission is expected to play a major role in meeting their expanding energy demands. Studies have shown that these needs will be best met with an increased transmission voltage of up to  $\pm 800\text{kV}$  DC at currents up of  $4000\text{A}$  [1-2].

Meeting these challenges will require thyristors with higher current ratings for use in the AC to DC and DC to AC converters used in HVDC schemes.

A common 'hockey-puck' thyristor (Fig. 1) for such applications typically comprises of a silicon wafer sandwiched between pairs of molybdenum discs and copper pole pieces acting both as anode and cathode terminals and serving as the heat transfer path to cool the device. These are enclosed in a hermetic ceramic housing (Fig. 2) by joining together flanges that are attached to both the pole pieces and the ceramic housing. For thyristors, a gate lead is also provided to connect the gate electrode of the wafer to an external triggering circuit.



Fig. 1: Photo of a hockey-puck thyristor

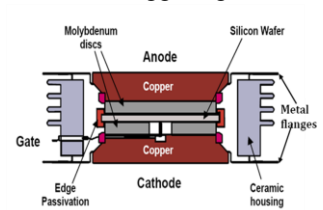


Fig. 2: Cross-sectional view of a hockey-puck thyristor

With silicon-based semiconductors being a mature technology [3], the demand for higher operating currents is today driving suppliers to adopt increased wafer diameters (hence larger devices) and also focus more on the design and performance of the housing to develop economic thyristors for the future. It is also thought that a switch from the present hermetic ceramic housings to a non-hermetic polymeric package can also help achieve a robust, low-cost, light-weight and complex-shaped device with potentially lower environmental impacts. However, such a shift is challenging due to the severe demands placed on packaging materials in these applications. Two factors of particular importance due to the high operating voltage are that the polymer must be void-free in high electrical stress areas to prevent partial discharge failures, and have low electrical stresses to reduce the risk of dielectric breakdown.

This paper will describe a simulation-based study aimed at optimising the performance of polymeric packages for HV semiconductor devices by minimising the electrical stresses. The package being considered herein is one where the conventional 'hockey puck' ceramic housing is directly substituted by a polymer (Fig. 3). In this work, the electrical field (E-field) distribution is predicted using finite element analysis (FEA) for such

a polymer-based device. In order to illustrate the problem to be addressed here, Fig. 4 plots the E-field obtained along path A in the housing of Fig. 3: the E-field is seen to be higher in the contact areas between the polymer housing and the metal inserts which attach the housing to the copper pole pieces. Different studies have shown that the occurrence of such high E-field regions plays a dominant role in the degradation of polymer materials in high voltage applications [4-5]. Although it can be argued that the E-field magnitude in the contact region can be changed by varying the conductivity of the polymer housing, the influence of the insert end shapes on the electrical stresses around the contact region is the main focus of discussion in this paper. A range of design options for the insert ends having varying degrees of curvature was thus selected for study based on factors such as the potential electrical performance benefits and their fabrication feasibility. The designs considered included (1) a wire-edged (circular) end (Fig. 5a), (2) an elliptical wire-edged flange end (Fig. 5b), and (3) a curved or “hook shaped” end (Fig. 5c). The resulting E-field magnitudes in the contact regions were studied and compared with a straight flange (Fig. 5d). Another study discussed in this paper considers the influence of other design parameters on the electrical stresses in the contact region.

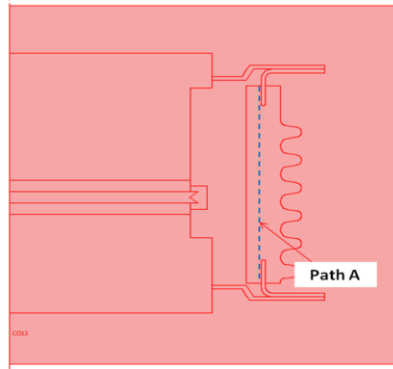


Fig. 3: Cross sectional view of proposed polymer-based hockey-puck package

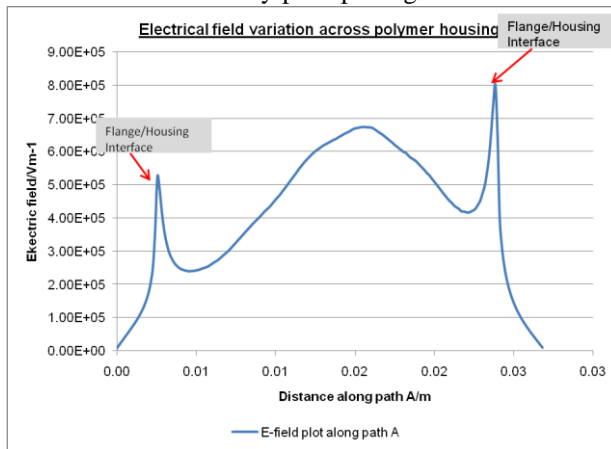


Fig. 4: Variation of E-field magnitude along path A shown in Fig. 3. The ‘0’ distance position corresponds to the cathode pole piece

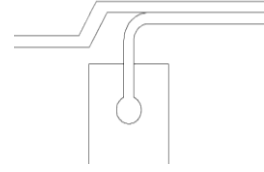


Fig. 5a: Circular wire-edged flange end

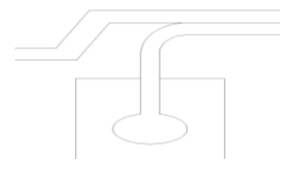


Fig. 5b: Elliptical wire-edged flange end

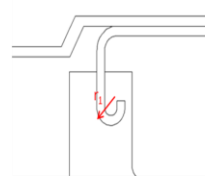


Fig. 5c: Curved/hook shaped flange end



Fig. 5d: Straight flange end

## 2. Methodology

For this work, FEA using the commercial package COMSOL Multiphysics was used to study the electrical behaviour of the polymer-based thyristor package described earlier. A 50mm diameter ‘hockey-puck’ thyristor package, but without the gate lead, was selected as the baseline test device for this study, and its arrangement comprised of a silicon wafer sandwiched between molybdenum discs and copper pole pieces, enclosed in a polymer-based housing and with silicone gel used to fill the cavity in the package. A 10kV DC voltage was applied between the pole pieces and the electrical field distribution simulated. To save computational resources and time, the device was modelled as a 2D axi-symmetric structure, as shown in Fig. 6. Details of the device dimensions are listed in Table 1, whilst the material conductivities used are listed in Table 2. Some assumptions made for the study were: (a) all materials were considered homogeneous and linear; (b) there is perfect contact at all material interfaces with no voids or delamination.

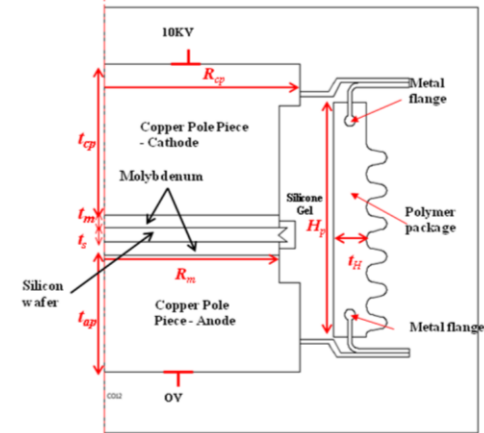


Fig. 6: 2D axi-symmetric model of 50mm device

Component	Dimensions (mm)
Molybdenum Discs	Disc radius, $R_m = 21.1\text{mm}$ Disc Thickness, $t_m = 1.5\text{mm}$
Silicon Wafer	Wafer Thickness, $t_s = 1.6\text{mm}$ Wafer radius = $21.9\text{mm}$
Copper Pole Piece	Cathode pole piece thickness, $t_{cp} = 17.4\text{mm}$ Anode pole piece thickness, $t_{ap} = 13.5\text{mm}$ Pole Piece radius, $R_{cp} = 23.6\text{mm}$
Polymer Housing	Housing Thickness, $t_H = 4.2\text{mm}$ Housing Height, $H_p = 27\text{mm}$

Table 1: Dimensions of package components

Materials	Electrical conductivity/ $\text{Sm}^{-1}$
Copper Pole Pieces & Flanges	$5.92 \times 10^7$
Molybdenum Discs	$1.87 \times 10^7$
Silicone Gel	$1 \times 10^{-13}$
Silicone rubber	$2 \times 10^{-15}$
Polymer housing	$3.03 \times 10^{-15}$
Silicon semiconductor	$1 \times 10^{-16}$
Air	$1 \times 10^{-18}$

Table 2: Material Properties of components

### 3. Results & Discussion

#### 3.1 Influence of insert shape and size on the electric field in the contact region

The maximum electrical field regions for the flange concepts under consideration were observed to occur at their ends where they are embedded in the polymer housing. Examples of such E-field distributions are illustrated in Figs. 7a & 7b which respectively depict the electric field distribution for the circular wire-edged and for the elliptical-shaped insert ends at the cathode side of the package. The E-field variation as a result of changes in the size of insert ends is illustrated in Figs. 8-10.

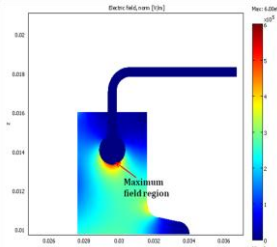


Fig. 7a: E-field distribution around a circular wire-edged insert end

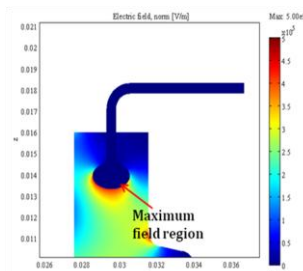


Fig. 7b: E-field distribution around an elliptical-shaped flange end

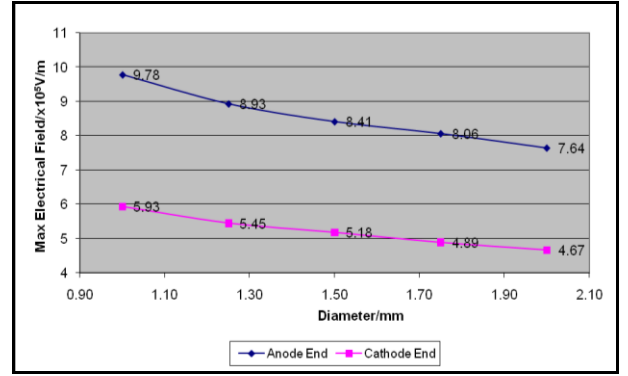


Fig. 8: Variation of maximum E-field magnitude as a result of diameter change of circular insert end

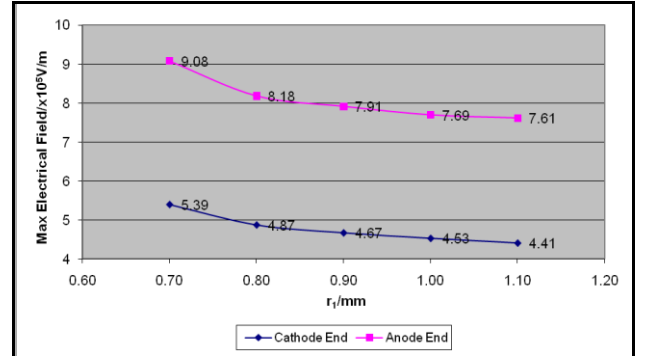


Fig. 9: Electrical field variation as a result of change in the bend radius,  $r_1$  of the curved flange end

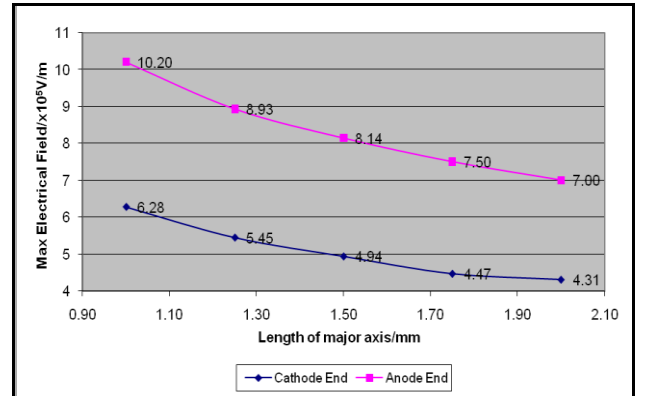


Fig. 10: E-field variation with respect to elliptical flange end dimensional change

From Figs. 8-10, it was observed, as expected, that as the radii of curvature of the flanges were increased, the electrical field at both the cathode and anode sides of the package was seen to decrease. For instance, in the case of the circular wire-edged insert end in Fig. 8, when the wire diameter was increased from 1mm to 2mm, E-field reductions of around 0.21MV/m and 0.13MV/m respectively were observed at the anode and cathode ends; whilst a similar variation is depicted in Fig 9 for the curved flange as its radius of curvature,  $r_1$ , was increased. A similar change also occurred for the elliptical flange edge when its length along the major (or horizontal) axis was increased, while the minor axis length was kept constant at 1.25mm. The shape of the ellipse flange end thus changed from a prolate ellipse to a circular end, and finally an oblate ellipse end, as the

length of the major axis increased from 1mm to 1.25mm and then 1.50mm onwards. Since the maximum E-field magnitudes at both cathode and anode ends were also seen to be significantly less than the dielectric strength of the polymer housing under study (around 22MV/m in this case), dielectric breakdown of a ‘void-free’ package was also regarded as unlikely.

On the other hand, a comparison of the maximum E-field values for the four geometries at both the cathode and anode also revealed the elliptical flange to have the lowest E-field magnitude, as shown in Fig. 11. The flanges studied were placed at equal depth inside the housing and had similar curvature, i.e. the diameter of the circular wire-edged flange and the length of the major axis of the elliptical flange were both 1.25mm, and the radius of curvature of the curved (hook) flange was 0.63mm in this case.

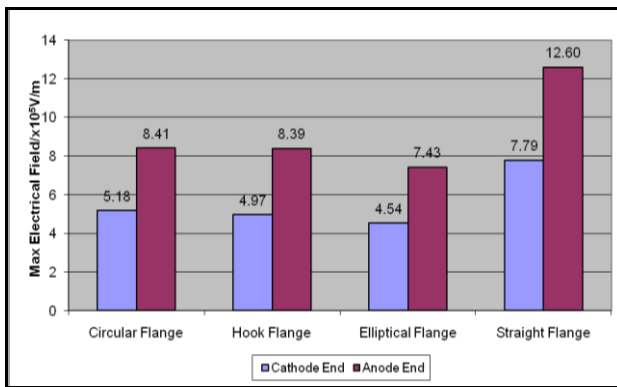


Fig.11: Comparison of maximum electric field around different flange end designs

### 3.2 Flange Design Optimisation

As opposed to a circular wire edge or an elliptical end insert, one major disadvantage of using a curved insert inside the polymeric package is that air voids may be more likely to be formed inside the curved profile during the process of moulding the housing. This could arise due to inadequate flow of the polymer around the curved profile and could lead to partial discharge failure of the housing during service. In this case, a ‘reduced’ curved profile of the flanges is preferred to allow appropriate polymer flow during processing. This aspect has been analysed through the use of polymer flow simulation software and will be reported in a separate paper. The geometry of such profiles can be described in terms of the angle  $\theta$  less than a full 180° hook geometry (Fig. 12).

From the simulation studies performed on a 1mm radius of curvature insert, the magnitude and location of the maximum electrical field region was seen to change as a result of changes in  $\theta$ . For instance, the maximum E-field region was seen to occur along the curvature of the curved insert when  $\theta=45^\circ$  and at the tip of the curved end when  $\theta=70^\circ$ , as shown in Figs. 13 and 14 respectively.

The location of the maximum E-field region at the curved profile tip (Fig.14) is likely to be detrimental to the service life of the package since the corner will act as

both an electrical stress raiser and a mechanical stress raiser and any delamination initiating at the corner could



Fig. 12: ‘Reduced’ curved profile

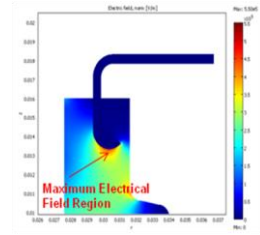


Fig. 13: E-field distribution when  $\theta=45^\circ$

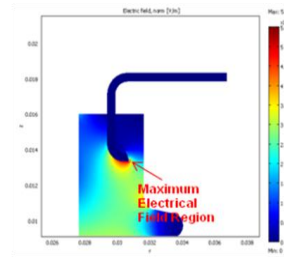


Fig. 14: E-field distribution when  $\theta=70^\circ$

then rapidly lead to a partial discharge failure developing. The study of the influence of  $\theta$  on the electric field magnitude suggested an insert profile with  $\theta=45^\circ$  to be the most appropriate since the maximum electrical field at both the cathode and anode ends was seen to be predominantly constant between  $\theta=0^\circ$  and  $45^\circ$  and the maximum E-field region remained located along the curved surface of the flange insert. However, the E-field increased significantly for  $\theta$  values greater than  $45^\circ$  (Fig. 15) and the location of the maximum region moved from the curved surface to the tip of the curved profile tip.

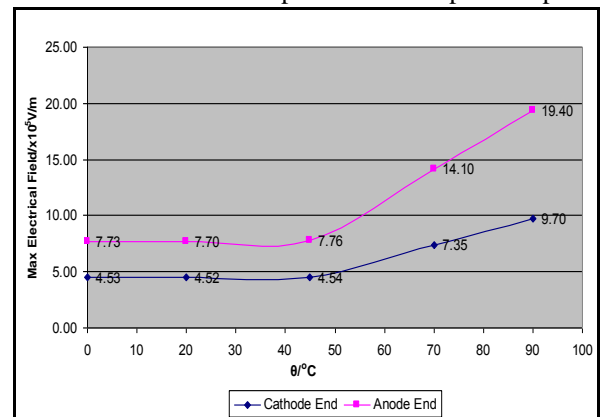


Fig. 15: E-field magnitude versus flange curve angle  $\theta$

### 3.3 Influence of Design Parameters

For this study, the influence of (1) the depth  $d$  the flange protrudes inside the housing, (2) the package thickness  $t$  and (3) the flange position  $f$  with respect to the copper pole piece outer surface, on the electric field in the contact region was investigated (Fig. 16). The experiment was based on the hockey puck device in Fig. 6 where the insert end was a 1.25mm diameter circular



wire-edged flange end. The package height  $H_p$  was kept constant while flange depth  $d$  was varied. An increase in the flange depth caused a reduction in the distance between flange tips at each end in this case. On the other hand, for the variation in the package thickness  $t$ , the outer and inner package diameters each changed and the flange position  $f$  was constant, whilst the housing parameters remained the same when the flange position  $f$  changed.

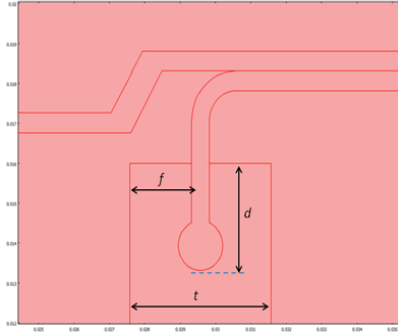


Fig. 16: Housing design parameters studied

The variation in the flange depth,  $d$ , was seen to have a more significant influence on the maximum electrical field magnitude in both the cathode and anode contact regions, compared to changes in the package thickness,  $t$ , and flange position,  $f$ , with respect to the housing interior surface. Their influences on the electrical field magnitude in the contact region are shown in figures 17-19. For example, the maximum E-field magnitude was seen to increase by 0.27MV/m and 0.47MV/m at the cathode and anode ends respectively for a 2mm increase in flange depth (Fig. 17), whilst the E-field value remained almost constant when the different package thicknesses were compared (Fig. 18). Likewise, no major change was observed in the field magnitude when the flange position,  $f$  was varied with respect to the housing surface (Fig. 19).

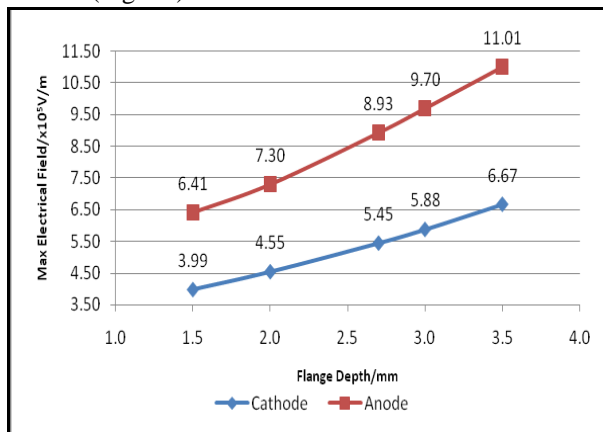


Fig. 17: Maximum electrical field variation with respect to change in the flange depth  $d$

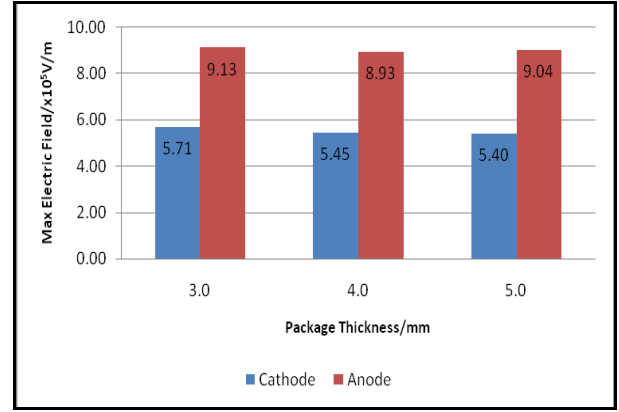


Fig. 18: Comparison of the maximum electrical field magnitude at the anode and cathode ends as a function of package thickness

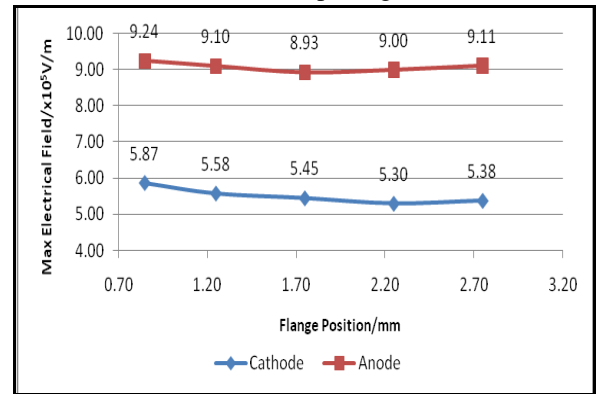


Fig. 19: Maximum electrical field changes as a result of changes in the flange position across the package

## Conclusions

Finite Element Analysis (FEA) was used to study the high voltage behaviour of a polymeric-based hockey-puck style power semiconductor package. The simulations confirmed that the contact region between the polymer housing and inserts (flanges) which join the housing to the copper pole pieces of the device tend to be areas of high electric stresses and may cause the polymer to degrade during its service life. Different insert edge designs were therefore studied to reduce the electric field magnitude around the contact region. The analysis revealed the electric field magnitude to be lowest around an elliptical-shaped insert end. However the benefits of this geometry were small compared to the circular and curved geometries studied and both of these were significantly better than the straight flange end. However in terms of both manufacturability of the flange inserts and their over-mouldability it was concluded that the curved geometry inserts were superior. The studies also showed that (1) the electric field at both the cathode and anode ends of the devices decreased as the radii of the different insert ends were increased, (2) a curved flange end with a '45° reduced contour profile', which is more appropriate from the moulding perspective for use in such devices compared to a fully curved profile, will not be significantly worse from an electrical perspective.



The influence of other housing dimensions, i.e. housing thickness, flange depth inside the housing and its position along the housing periphery, on the electric field was also studied. In this case, the variation in the flange depth was found to influence the field magnitude more significantly compared to changes in the housing thickness and flange position.

### **Acknowledgments**

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### **References**

1. S. Linder, "Power semiconductors - Part two: housing technology and future developments", ABB Review, no. 1, 2007
2. V.F Lescale, U. Alstrom, J. Nunes, L. Weimers and D. Wu, Power Transmission with HVDC AT 800 kV [Homepage of CIGRE - International Council On Large Electric Systems], [Online]. Available: <http://search.abb.com/library/ABBLibrary.asp?DocumentID=1JNL100112-051&LanguageCode=en&DocumentPartID=&Action=Launch> [2007, 12/5], 2007.
3. W. Breuer, D. Povh, D. Retzmann and E. Teltsch, "Trends for future HVDC Applications", Proceedings of the 16<sup>th</sup> CEPSI Conference of the Electric Power Supply Industry, India 2006.
4. A. J. Phillips, J. Kuffel, A. Baker, J. Burnham, A. Carreira, E. Cherney, W. Chishlom, M. Farzaneh, R. Gemignani, A. Gillespie, T. Grisham, R. Hill, T. Saha, B. Vancia and J. Yu, "Electric Fields on AC Composite Transmission Line Insulators", IEEE Transactions on Power Delivery, vol. 23, no. 2 (2008), pp. 823-830
5. A. J. Phillips, D. J. Childs & H. M Schneider, "Aging of non-ceramic insulators due to corona from water drops", IEEE Transaction on Power Delivery, vol. 14, no. 3, (1999), pp. 1081-1086.