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# SOLID STATE HIGH FREQUENCY ELECTRIC PROCESS HEATING POWER SUPPLIES 

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A DOCTORAL THESIS<br>Submitted in part fulfilment of the requirements for the award of Ph.D. of Loughborough University of Technology 1989<br>Supervisor: Dr. L. Hobson<br>Department of Electronic and Electrical Engineering

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(i)


#### Abstract

A detailed critical review has been made of both solid state power devices and circuit topologies with emphasis on their application to high frequency electric process heating power supplies operating between 3 and 30 MHz .

A number of prototype units have been designed and constructed and their suitability for high frequency induction heating and dielectric heating applications investigated. Desirable qualities being robustness, tolerance to load mismatch, ease of design, simplicity and cost of constituent components as compared with present day valve equipment.

The experience gained in these investigations has resulted in the choice of the power MOSFET as the most appropriate device and Class E amplifier as being the most applicable circuit topology for the generation of RF power for high frequency electric process heating applications.

A practical and theoretical study has been made of the limitations of the power MOSFET as a high frequency switching device. The effect of source feedback on the switching speed of TO3 packaged devices has been investigated by the addition of a second source terminal in a specially modified TO3 package.

Novel drive circuits have been developed enabling high frequency switching of both power and RF MOSFETs. These have been employed in inverters operating at 3.3 MHz at power levels up to 600 W and at frequencies between 7 and 27 MHz at power levels over 100 W , with conversion efficiencies of up to $95 \%$.


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## TABLE OF SYMBOLS

| SYMBOL | DESCRIPTION | UNIT |
| :---: | :---: | :---: |
| A | The side of the square in a square sectioned toroidal inductor. | m |
| $A_{\nu}$ | The voltage gain of a MOSFET switching stage. | - |
| $B$ | The susceptance of the shunt capacitor in a Class E circuit. | S |
| $B V_{c b o}$ | The open circuit collector to base breakdown voltage of a BJT. | V |
| $B V_{\text {cro }}$ | The open circuit collector to emitter breakdown voltage of a BJT. | V |
| $B V_{d s}$ | The drain to source breakdown voltage of a MOSFET. | V |
| $B V_{80}$ | The open circuit gate to source breakdown voltage. | V |
| C | An unspecified capacitance. | F |
| $C_{1}$ | The shunt capacitor in the Class E circuit. | F |
| $C_{2}$ | The output capacitor in the Class E circuit. | F |
| $C_{b c}$ | The base to source capacitance of the MOSFET parasitic BJT. | F |
| $C_{d b}$ | The drain to base capacitance of the MOSFET parasitic BJT. | F |
| $C_{d q}$ | The drain to gate capacitance of a MOSFET. | F |
| $C_{\text {d }}{ }^{\circ}$ | The increased drain to gate capacitance of the MOSFET when reverse biased. | F |
| $C_{\text {dso }}$ | The gate-drain overlap capacitance of a MOSFET. | F |
| $C_{\text {dt }}$ | The drain to source capacitance of a MOSFET. | F |
| $C_{8}$ | The gate to source capacitance of a MOSFET. | F |
| $C_{80}$ | The gate-source overlap capacitance of a MOSFET. | F |
| $C_{\text {is }}$ | The input capacitance of a transistor. | F |
| $C_{\text {ass }}$ | The output capacitance of a transistor. | F |
| $C_{p}$ | The parallel impedance matching capacitor. | F |
| $C_{r}$ | A resonating capacitor. | F |
| $C_{r a}$ | The reverse transfer capacitance of a transistor. | F |
| C, | The series impedance matching capacitor. | F |
| $C_{3}^{\prime}\left(C_{31}\right)$ | The effective series matching capacitor. | F |
| $C_{\text {stras }}$ | The stray circuit capacitance. | F |


| $c$ | The Brooks coil dimension. | m |
| :---: | :---: | :---: |
| d | The diameter of a wire. | m |
| $E_{2}$ | The energy band gap of a semiconductor. | eV |
| $E$, | The d.c. input voltage to a circuit. | V |
| $E_{\text {rumber }}$ | The energy dissipated in the snubber. | J |
| $f$ | Frequency. | Hz |
| $f$ | The frequency of switching of a MOSFET. | Hz |
| $f_{T}$ | The unity gain cut off frequency of a transistor. | Hz |
| $8 f$ | The transconductance of a MOSFET. | $\mathrm{AV}^{-1}$ |
| $I^{1}$ | An unspecified current. | A |
| $I_{b}$ | The base current of a BJT. | A |
| $I_{C 1}$ | The current through the shunt capacitance in a Class E circuit. | A |
| $I_{C d s}$ | The current through the MOSFET drain to gate capacitor. | A |
| $I_{\text {c }}$ | The collector current of a BJT. | A |
| $I_{\text {cc }}$ | The collector supply current of a bipolar transistor circuit. | A |
| $I_{d}$ | The drain current of a MOSFET. | A |
| $I_{\text {d¢ }}$ | The peak drain current of a MOSFET. | A |
| $I_{\text {abive }}$ | The MOSFET gate drive current. | A |
| $I_{F L}$ | The full load supply current. | A |
| $I_{s}$ | The MOSFET gate current. | A |
| $I_{8 c}$ | The MOSFET gate charging current. | A |
| $I_{8 d}$ | The MOSFET gate discharge current. | A |
| $I_{s z}$ | The gate to source leakage current of an SIT. | A |
| $I_{L}$ | The current flowing through a load. | A |
| $I_{\text {max }}$ | The maximum current through a conductor. | A |
| $I_{\text {asjec }}$ | The mismatched load supply current. | A |
| $J_{\text {max }}$ | The maximum allowable current density through a conductor. | $\mathrm{Am}^{-2}$ |

[^0]| $K$ | The transformer coupling factor. | - |
| :---: | :---: | :---: |
| $k$ | The ratio of wire length to diameter in an inductor. | - |
| $L_{1}$ | The RF supply inductor in the Class E circuit. | H |
| $L_{2}$ | The output inductor in the Class E circuit. | H |
| $L_{B}$ | The inductance of a Brooks coil. | H |
| $L_{\text {chate }}$ | The d.c. supply inductance. | H |
| $L_{d}$ | The drain lead inductance of a MOSFET. | H |
| $L_{t}$ | The gate lead inductance of a MOSFET. | H |
| $L_{m}$ | The magnetising inductance of a transformer. | H |
| $L_{\text {o }}$ | The scale inductance term used to calculate the parameters of the square sectioned toroidal inductor. | H |
| $L_{p}$ | The transformer primary inductance. | H |
| $L_{r}$ | A resonating inductance. | H |
| $L_{s}$ | The transformer secondary inductance. | H |
| $L_{\text {s }}$ | The inductance of a square sectioned toroid. | H |
| $L_{\text {s }}$ | The source lead inductance of a MOSFET. | H |
| $L_{\text {stray }}$ | The stray circuit inductance. | H |
| $N$ | The number of turns on an inductor. | - |
| $N_{1}$ | The number of primary turns of a transformer. | - |
| $\mathrm{N}_{2}$ | The number of secondary turns of a transformer. | - |
| $P_{d}$ | The power dissipated in the MOSFET. | W |
| $P_{\text {dinu }}$ | The power dissipated in the gate drive transistors. | W |
| $P_{8}$ | The power dissipated in a MOSFET gate. | W |
| $P_{0}$ | The output power of a transistor stage. | w |
| $Q$ | The quality factor of a circuit or component. | - |
| $Q_{8}$ | The gate charge of a MOSFET. | C |
| $Q_{8}$ | The total charge delivered to the MOSFET gate during switching. | C |
| $Q_{\text {spabami) }}$ | The charge delivered to the MOSFET gate during the switching transition. | C |
| $Q_{L}$ | The loaded $Q$ of the Class E circuit. | - |


| $R$ | An unspecified resistor. | $\Omega$ |
| :---: | :---: | :---: |
| $R_{a}$ | The anode resistance. | $\boldsymbol{\Omega}$ |
| $R_{\text {derive }}$ | The source resistance of a MOSFET drive circuit. | $\Omega$ |
| $R_{\text {datas }}$ | The drain to source of resistance of an SIT. | V |
| $R_{\text {drom) }}$ | The drain to source resistance of a MOSFET when it is in the Ohmic region. | $\Omega$ |
| $R_{z}$ | The gate resistance. | $\Omega$ |
| $R_{L}$ | The load resistance. | $\Omega$ |
| $R_{0}$ | The drain to drain output resistance. | $\Omega$ |
| $R_{p}$ | The parallel matched load impedance. | $\Omega$ |
| $R$ s | The bulk source resistance of a MOSFET. | $\Omega$ |
| $S$ | The minor radius of a toroid. | m |
| $t$ | Time. | S |
| $t_{f}$ | Fall time. | S |
| $t_{\text {off }}$ | The turn off time of a semiconductor. | S |
| $t_{\text {ar }}$ | The turn on time of a semiconductor. | S |
| $t_{\text {platay }}$ | The time taken for the MOSFET gate voltage to traverse the plateau region. | s |
| $t$ | Rise time. | S |
| $t_{r}$ | The reverse recovery time of a silicon diode. | s |
| $t_{\text {muichive }}$ | The time taken for the MOSFET to turn on and off. | S |
| $V$ | Voltage at an unspecified point. | V |
| $V_{a}$ | The anode voltage. | V |
| $V_{b o r(a d)}$ | The base to emitter saturation voltage of a bipolar transistor. | V |
| $V_{c}$ | The collector voltage of a BJT. | V |
| $V_{c c}$ | The collector supply voltage of a bipolar transistor circuit. | V |
| $V_{c o p a t}$ | The collector to emitter saturation voltage of a bipolar transistor. | V |
| $V_{d}$ | The MOSFET drain voltage (w.r.t. 0 V ). | V |
| $V_{\text {da }}$ | The drain supply voltage to an FET circuit. | V |


| $V_{\text {dive }}$ | The gate drive voltage to a MOSFET. | V |
| :---: | :---: | :---: |
| $V_{d s}$ | The drain to source voltage of a MOSFET. | V |
| $V_{\text {arame }}$ | The drain to source conduction drop of a MOSFET in the ohmic region. | V |
| $V_{\text {drppack }}$ | The MOSFET peak drain to source voltage. | V |
| $V_{s}$ | The MOSFET gate voltage (w.r.t. 0 V ). | V |
| $V_{s}$ | The gate to source voltage of a MOSFET. | V |
| $V_{\text {axa }}$ | The gate to source cut off voltage of an SIT. | V |
| $V_{L S}$ | The voltage developed across the source inductance. | V |
| $V_{\alpha \text { (max) }}$ | The maximum output voltage of a Class E circuit. | V |
| $V_{\text {on }}$ | The 'on' gate voltage of the MOSFET. | V |
| $V_{p}$ | The plateau voltage at the MOSFET gate. | V |
| $V_{p e}$ | The externally measured MOSFET plateau voltage at turn on. | V |
| $V_{p d}$ | The externally measured MOSFET plateau voltage at turn off. | V |
| $V_{\text {placauk }}$ | The MOSFET plateau region voltage. | V |
| $V$ s | The MOSFET source voltage (w.r.t. 0 V ). | V |
| $V_{x(\text { max })}$ | The maximum voltage impressed across a switch. | V |
| $V_{\text {samber }}$ | The voltage across the snubber. | V |
| $V_{t}$ | The threshold voltage of a MOSFET. | V |
| $w$ | The length of the wire forming an inductor. | m |
| $Z_{\text {drive }}$ | The source impedance of a drive circuit. | $\Omega L^{\circ}$ |
| $Z_{s \prime}$ | The gate to source impedance of a MOSFET. | $\Omega L^{\circ}$ |
| $\mathrm{Z}_{\text {in }}$ | The input impedance of a transistor or transmission line. | $\Omega$ |
| $Z_{L}$ | The impedance of a load circuit. | $\Omega L^{\circ}$ |
| $Z_{\text {lise }}$ | The characteristic impedance of a transmission line. | $\Omega L^{\circ}$ |
| $Z_{\text {d }}$ | The output load impedance of a transistor. | $\Omega L^{\circ}$ |
| $Z_{\text {owe }}$ | The output impedance of a circuit. | $\Omega L^{*}$ |

## GREEK SYMBOLS

| $\omega_{r}$ | The radiancy of resonance of a circuit. | radians ${ }^{1}$ |
| :---: | :---: | :---: |
| $\eta$ | Efficiency. | - |
| B | The transistor current gain. | - |
| $\mu$ | The electron mobility in a semiconductor. | $\mathrm{m}^{2} \mathrm{~V}^{-1} \mathrm{~s}^{-1}$ |
| $\mu_{0}$ | The permeability of free space. | $\mathrm{Hm}^{-1}$ |
| $\tau$ | Time constant. | s |
| $\tau_{1}$ | The time constant of the MOSFET gate below threshold. | s |
| $\tau_{2}$ | The time constant of a MOSFET gate during the plateau region. | s |
| $\tau_{3}$ | The time constant of the MOSFET gate during the over drive region. | s |
| $\tau$ | The time constant of the load and output capacitance of a MOSFET when the reverse transfer capacitance is reverse biased. | s |
| $\tau_{s}$ | The time constant of the load and output capacitance of a MOSFET when the reverse transfer capacitance is forward biased. | s |
| $\theta_{f}$ | The electrical angle of transistor fall time. | radians |
| $\theta_{J}$ | The junction temperature of a semiconductor. | ${ }^{\circ} \mathrm{C}$ |
| $\delta$ | The magnetic skin depth of a conductor. | m |

## Chapter 1

## INTRODUCTION

A brief theory of induction and dielectric heating principles is presented. The high frequency generators presently used in RF heating applications are described and the reasons for undertaking the work reported in this thesis mentioned.

## 1 INTRODUCTION

When an electrically conducting substance is placed within an alternating magnetic field, current is induced into the conductor. The resulting current causes resistive heating within the conductor. This process is known as induction heating.

The magnetic field diffuses into the conductor as a strongly damped propagating wave with characteristic penetration depth $\delta$, known as the skin depth. The induced current within the conductor is confined near to the surface to a depth of the order of $\delta$ (Zahn 1979) ${ }^{1}$. This skin depth reduces as a function of the square root of the reciprocal of the frequency of the alternating magnetic field. This phenomena is utilised in high frequency induction heating applications when only the surface of the conductor is required to be heated, for example in surface hardening applications.

Conversely, when an electrically non-conducting material is placed between two electrodes to form a dielectric, the application of an alternating electric field can cause heating, i.e. dielectric heating. The energy dissipated within the dielectric either by ohmic or polarisation losses (Metaxas et al. 1983) is related to the operating frequency, the loss factor of the material and the square of the electric field strength applied across the material. The loss factor is an inherent property of the material although it can vary with temperature, operating frequency and moisture content. The electric field is limited to avoid voltage breakdown effects and thus to achieve appreciable heating rates, high operating frequencies are required. Table 1.1 shows the frequencies commonly used in dielectric heating applications within the frequency bands allocated for industrial, scientific and medical (I.S.M.) uses. For plastic welding applications in particular, the frequency band of 27.12 MHz is the most common because of its greater allowable tolerance on frequency stability.

| Table 1.1 <br> Dielectric Heating Frequencies |  |
| :---: | :---: |
| Frequency <br> $\mathbf{M H z}$ | Tolerance <br> $( \pm \%)$ |
| 13.56 | 0.05 |
| 27.12 | 0.60 |
| 40.68 | 0.05 |

Induction heating is performed at a number of frequencies and power levels. Applications range from $50 \mathrm{~Hz}, 100 \mathrm{MW}$ billet heating systems; through surface hardening, zone refining, fibre optic production performed at frequencies ranging from 3 kHz to 3 MHz ; to induction coupled plasma and metal spluttering applications at 7 MHz .

1 The reader is referred to the references.

The size of the dielectric heater is dependent mainly upon the application. Those used for drying of textiles, backing products, wood glues etc. have power outputs from several tens of kW to 200 kW . Those used for plastic welding application range from 800 W to 30 kW .


Figure 1.1 Block Diagram of Valve RF Generator.
The main power element used in RF generators for both high frequency induction heating and dielectric heating applications is the triode valve which is operated in Class $C$ mode and used in tuned anode, modified Colpitts or Hartley oscillators. A simplified block diagram of an RF generator is shown in Figure 1.1. The three phase mains input is transformed to a high voltage, typically $5 \mathrm{kV}-15 \mathrm{kV}$, rectified to produce a d.c. voltage which is then applied to the valve; the valve is resonated by means of a tuned circuit (often called a tank circuit). In RF induction heating supplies the tank circuit is formed from discrete components, at the higher dielectric heating frequencies the circuit is formed from a lumped capacitor-inductor in the form of a resonant cavity. The high frequency output from the valve is fed to an applicator containing the workpiece via a section of the resonant tank circuit or by a load matching circuit. A typical load matching circuit used in dielectric heating supplies is shown in Figure 1.2.


Figure 1.2 Typical Dielectric Heating Load Matching Circuit.

The efficiency of conversion of mains input to RF power within the generator is generally less than $60 \%$. Modern trends are towards solid state technology and power transistors have size and weight advantages over their valve counterparts. Other advantages include:
(a) the absence of a valve filament power supply;
(b) operation at lower d.c. voltage levels which are much more applicable to portable hand-held units; and
(c) the relative freedom from maintenance and longer device life-span of solid state devices imply long term economic advantages.

Recent progress in the development of solid state inverters for medium frequency ( 50 to 400 kHz ) induction heating applications coupled with the continuing advancement in solid state devices has suggested that it may be possible to produce solid state supplies suitable for high frequency ( 3 to 30 MHz ) induction heating and dielectric heating applications.

The ensuing chapters report the achievements and conclusions of a three year investigation into the above suggestion.

## Chapter 2

## DEVELOPMENTS IN POWER SEMICONDUCTOR DEVICES

In this chapter, recent advances in semiconductor devices are critically reviewed.

Predictions are made upon likely future developments.
Comment is given upon their suitability for use in high frequency, ( $3-30 \mathrm{MHz}$ ) electric process heating equipment, with particular reference to plastic welding applications at 27.12 MHz .

As with most areas of the electronics industry, a great deal of development has taken place over the last decade in power electronic devices. The most notable being the advent of the power MOSFET, the Static Induction Transistor (SIT), the Gate Tum Off Thyristor (GTO), and the combination of bipolar-FET technologies, for example the so called BIPMOS, COMFET devices (Hinchliffe ${ }^{2}$ et al. 1986a, 1986c). A comparison of frequency and power handling capabilities of different power semiconductor types is shown in Figure 2.1.


Figure 2.1 Controlled Power Versus Operating Frequency of Power Semiconductors.

[^1]The consequence of these advances has been greater switching speeds and subsequent increase in operating frequencies. This has enabled a reduction in size of switch mode power supplies (SMPS's) and power inverters (due to smaller smoothing, transformer and resonating components), and an improvement in efficiency (through a reduction in switching losses).

### 2.1 The Gate Turn Off Thyristor (GTO)

The GTO is a four layer device of similar construction to the thyristor or Silicon Controlled Rectifier (SCR) except that the regenerative loop gain is carefully controlled.

Although interest in the gate turn off thyristor has existed for many years, large scale devices have only been made possible with recent advances in semiconductor device fabrication technology (Matsuzaki et al. 1983).

The equivalent circuit of a GTO is shown in Figure 2.2. The anode resistor, $R_{a}$, represents short circuiting bars, fabricated between the anode $p^{-}$layer and the $n$ base, to reduce the gain of the pnp transistor and thus the total loop gain of the device. The gate resistor, $R_{g}$, represents residual gate series resistance, this limits the maximum current which can be drawn from the gate, determined by the gate-cathode reverse breakdown voltage (typically of the order of 12 to 20 volts).


Figure 2.2 Equivalent Circuit of a GTO.

As with conventional thyristors, the device is turned on by a pulse of gate current (Burgum et al. 1980), however, in order to achieve low conduction drop (typically 1.8 to 2 V ), a continuous gate current needs to be supplied, although of smaller amplitude than the initial firing pulse. The device is turned off by applying a negative gate current which reduces the internal gain ( $\beta \mathrm{npn} \times \beta \mathrm{pnp}$ ) to less than unity. As the device turns off and the cathode current extinguishes, a residual anode to cathode current flows, known as the 'tail' current (Burgum et al. 1982). This tail current becomes the dominant contributor to power loss at higher switching frequencies and is one of the main limiting factors on the GTO's performance.

A second limit to high frequency operation is the attainable $\mathrm{d} v / \mathrm{dt}$ (rate of change of anode voltage) at turn off. Because the turn off mechanism results in the anode current fragmenting into small filaments, high rates of increase of anode-cathode voltage can cause one of these conducting channels to overheat and destroy the device. However, the $\mathrm{d} v / \mathrm{dt}$ rating is superior to that of power bipolar transistors.

Inverters based upon GTO's have been operated at frequencies greater than 20 kHz (Wirth et al. 1987) and if techniques such as zero current switching or cathode turn off are employed then the frequency can be extended to 80 kHz (Goodfellow et al. 1988a 1988b, Leisten et al. 1989).

To summarise, the GTO combines inherently high blocking voltage (up to 4.5 kV ), high current and over current capability (up to 3 kA ) with gate control turn off (Hashimoto et al. 1988). Its two main disadvantages are its large gate drive consumption and low switching frequency, i.e. typically less than 20 kHz , although exceptionally 80 kHz .

### 2.2 The Field Controlled Thyristor (FCT)

This is another recent development of the thyristor family. Like the GTO, the FCT is a robust device, breakdown voltages of up to 2.5 kV and current handling capability of 500 A have been reported in experimental components.

Most FCTs or MOS-GTOs exhibit a 'normally on' characteristic (Grüning et al. 1986), i.e. current conduction ceases only when a negative gate drive is applied. However, very recent developments have resulted in the fabrication of 'normally off' devices (Stoisiek et al. 1986, Gruening et al. 1988).

One breed of the FCT is the Static Induction Thyristor (SITh) (Terasawa et al. 1982). Devices have been demonstrated with forward blocking voltage and average current rating of $2.5 \mathrm{kV}, 300$ A respectively and a turn off action within $6 \mu \mathrm{~s}$ at 500 A anode current (Nishizawa et al. 1986a). The SITh has been developed purely by Japanese technology and have been successfully used in commercial induction heating supplies operating at 60 kHz and 100 kW (Muraoka et al. 1986).

Like the GTO, its main applications are in variable speed motor control, medium frequency induction heating and chopper circuits.

### 2.3 The Bipolar Junction Transistor (B.JT)

Power transistors have been in existence for several decades, during which time improvements have continually been made.

In terms of current handling capability, breakdown voltage and conduction drop, bipolar transistors are superior to the more recent power MOSFET. Devices are readily manufactured with breakdown voltages up to 1400 V and current ratings of over 50 A . However, current gain is low, typically 3 to 7 for high power devices, necessitating the use of Darlington configurations.

Their main drawbacks are slower switching speed, resulting in higher switching losses at high frequencies, minimum stored charge recovery time, and reduced safe operating area. The principal limit on operating frequency being due to the fact that time is required to remove minority carriers out of the base region before the transistor can sustain a blocking voltage. That is to say they are minority carrier devices.

In terms of efficiency, the new generation of switched mode power transistors such as Motorola's SM111MJ16004, exhibit lower losses than all other devices in comparable applications at frequencies below 100 kHz . Above this, the switching losses of the bipolar transistor rapidly increase (Motorola 1982, Moore 1984).


Figure 2.3 RET Transistor.
The experience gained with power MOS development has been applied to the further development of power bipolar devices (Fruendal 1984, Morgan 1986). Figure 2.3 (above) shows a new type construction; the ring emitter structure (Hebenstreit 1987). The base and emitter are each in the form of fine structures, a large number of individual transistors are created and connected in parallel by the use of emitter series
resistors. The introduction of a second metal plate on the chip avoids the loss of active silicon area. Transistors fabricated in this way exhibit faster switching speeds and improved safe operating areas compared with conventional transistors (Miller 1986, Lorenz 1987).

Thus, although most of present day development is in new types of devices such as the GTO, the power MOSFET and so on, there is still much interest in the bipolar junction transistor (Aloise 1988).

### 2.3.1 RF Bipolar Junction Transistors

The construction technique used for the new power BJT is similar to the mesh emitter approach being developed for power RF bipolar transistors designed to operate in Class A, AB and Class C linear amplifiers.

A $900 \mathrm{MHz}, 120 \mathrm{~W}$ mesh emitter transistor has been reported in the literature (Ishu et al. 1983) which consists of 36 cells, has $55 \%$ collector efficiency and operates off a 50 V collector supply.

There are a number of bipolar transistors currently available designed specifically for use in HF amplifiers operating in the $3-30 \mathrm{MHz}$ region. Maximum rating for air cooled devices, operating from a 50 V collector supply, is typically 200 to 250 W PEP (Peak Envelope Power). These are available from several manufacturers (Motorola, Mullard, Thomson CSF etc.) and cost in the order of $£ 100$ per device which is approximately four times as expensive, watt for watt, as an air cooled valve.

There is at least one manufacturer (Thomson CSF) who market a 600 W PEP water cooled device, again operating off a 50 V supply. These cost in the region of $£ 250$ per device (at 1988 prices).

All of the devices mentioned typically require 10 W of drive power to achieve the rated output power. Thus amplifier stages have to be cascaded in order to provide the necessary signal gain.

### 2.4 The Static Induction Transistor (SIT)

This is a voltage controlled, majority carrier, field effect device. It employs a buried gate structure in the form of a grid of p type regions which are electrostatically coupled (Nishizawa 1980 and 1981). This grid type structure ensures that, unlike the power MOSFET, the power SIT does not exhibit a saturating $V_{d} I_{d}$ characteristic, unless the gate is heavily biased in the forward direction. In fact the SIT has a 'triode valve' type output voltage-current characteristic (Siegal 1982).

Figure 2.4 shows the device cross sectional structure along with its graphical symbol. The output characteristics of the SIT are shown in Figure 2.5. It can be seen that the SIT is a normally on device although it exhibits lower on resistance with a slightly positive ( $\approx 0.7 \mathrm{~V}$ ) gate-source bias. The conducting channel is restricted by an increasing negative gate-source voltage. More recent developments have resulted in the fabrication of normally off devices with $300 \mathrm{~V}, 200 \mathrm{~A}$ SIT modules being reported (Aoki 1988).


Figure 2.4 Static Induction Transistor (SIT).


Figure 2.5 SIT V-I Characteristics.
At low drain current levels the SIT exhibits a positive drain current temperature coefficient but at higher currents ( $>1 \mathrm{amp}$ ) this becomes negative, reflecting the temperature dependence of the series channel resistance. Thus, hot spots caused by current crowding do not occur. This offers a thermally stable operation for the high current region, excludes secondary breakdown and eases paralleling of devices.

Fabrication is technically very demanding and SITs tend to be more expensive than their power MOSFET counterparts, present commercial devices have gate to drain breakdown voltages of up to 1500 V , continuous drain current ratings up to 18 amperes and turn on - turn off times of the order of 200 ns . Table 2.1 gives electrical characteristics of three power SITs currently available.

| Table 2.1 Electrical Characteristics of Power SITs |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| Term | Symbol | Condition | Type designation |  |
|  |  |  | 2SK-182 | 2SK-183 |
| Gate to source break down voltage | $B V_{30}$ | $i_{z}=0.1 \mathrm{~mA}$ | 80 V |  |
| Gate leakage current | $I_{s e s}$ | $v_{u r}=-40 \mathrm{~V}$ |  |  |
| Drain current | $I_{4}$ | $\begin{aligned} & v_{s_{0}}=0 \mathrm{~V} \\ & v_{d \alpha}=10 \mathrm{~V} \end{aligned}$ | 18 A | 10 A |
| Gate-to-source cutoff voltage | $V_{\text {Pxaff }}$ | $\begin{aligned} v_{d} & =300 \mathrm{~V} \\ i_{d} & =1 \mathrm{~mA} \end{aligned}$ | 30 V |  |
| Gate-to-drain breakdown voltage | $B V_{\text {sto }}$ | $i_{d}=0.1 \mathrm{~mA}$ | 600 V | 800 V |
| Input capacitance | $C_{\text {itr }}$ | $\begin{aligned} & v_{v_{s}}=0 \mathrm{~V} \\ & v_{g z}=10 \mathrm{~V} \end{aligned}$ | 5000 pF | 8000 pF |
| Drain-to-source 'on' resistance |  | $\begin{aligned} y_{d} & =0 \mathrm{~V} \\ i_{d} & =2 \mathrm{~A} \end{aligned}$ | $1.05 \Omega$ | $0.5 \Omega$ |
| Drain-to-source 'off' resistance | $R_{\text {deand }}$ | $v_{\text {dt }}=300 \mathrm{~V}$ | $1 \mathrm{M} \Omega$ |  |
| Turn on time | $t_{\text {on }}$ | $\begin{aligned} & i_{d}=1.5 \mathrm{~A} \\ & \mathrm{~V}_{d}=50 \mathrm{~V} \end{aligned}$ | 250 ns | 100 ns |
| Turn off time | $t_{05}$ | $\begin{aligned} i_{d} & =1.5 \mathrm{~A} \\ v_{d d} & =50 \mathrm{~V} \end{aligned}$ | 300 ns | 100 ns |

The main limitation on frequency of the SIT is the gate source input capacitance and series source resistance. In theory the SIT should be capable of higher operating frequencies than the FET since the channel length is shorter for a given power rating, resulting in smaller input capacitance. However this is
not borme out in commercially available devices which have comparatively large input capacitances, of the order of 2.5 times greater than a comparably rated power MOSFET. Thus power SITs have application in the 50 kHz to 500 kHz range (Nakaoka 1984, Nishizawa 1986b, Ogiwara 1988).

There are a number of variations on the SIT and devices are being developed specifically for application in HF and UHF, linear amplifiers (Regan 1984, Chang 1983). These new SITs have demonstrated saturated, continuous wave, output power levels of 110 W at 275 MHz with a 6 db power gain (i.e. 27.6 watts input) and $68 \%$ drain efficiency with a d.c. supply voltage of 90 V .

### 2.5 The Vertical Double Diffused MOSEET (The Power MOSFET)

The power MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is a vertical, double diffused, self aligned, insulated gate device (DMOSFET for short but more commonly called simply the 'power MOSFET') developed in the late 1970's. It incorporates a closed cellular source structure enabling low on resistances to be achieved by paralleling many transistor elements on one die.

Being a voltage controlled, majority carrier device, it exhibits simple drive requirements, and fast switching speeds since, unlike the bipolar junction transistor, no time is required for minority carriers to recombine, i.e. there is no charge storage time. Further, because the device has a positive on resistance temperature coefficient ( $\mathrm{d} R_{d r o m} / d \theta_{J}>0$ ) no current crowding takes place, the device is free from secondary breakdown and thermal runaway (except in constant current situations) and can be easily paralleled.


Figure 2.6 Voltage-Current Characteristics of a Power MOSFET.

The voltage-current output characteristics are shown above in Figure 2.6. This comprises of two regions; region A (often called the linear region) where the device behaviour approximates to a voltage controlled resistor, and region $B$ (the active region) where the device acts as a voltage controlled current source. When operated as a switch, the MOSFET is normally driven into its fully enhanced, resistive region with a slightly higher gate voltage than necessary, to ensure minimum conduction losses and to improve noise immunity.

Most devices start to conduct at a gate source voltage $\left(\nu_{z}\right)$ of between 2 and 4 volts and require an increase in $v_{p}$, of about 4 volts to become fully enhanced. Gate source breakdown voltage ratings vary from manufacturer to manufacturer but are usually either $\pm 20 \mathrm{~V}$ or $\pm 40 \mathrm{~V}$.

Drain-source breakdown voltage, current carrying capability (and to a lesser extent parasitic capacitances) are directly related to the die size, whereas on resistance is dependent both on breakdown voltage and die size, and increases as a 2.6th. power law in relation to breakdown voltage:

$$
\begin{equation*}
R_{d r(0 n)} \propto B V_{d r}^{2.6} \tag{2.1}
\end{equation*}
$$

Where: $\quad B V_{d r}$ is the drain-source breakdown voltage.

Thus the higher the voltage rating required, the higher the on resistance, die size and parasitic capacitances. Hence maximum switching speed is slower for higher voltage devices. This is also true for low voltage high current devices except in this case, not only is the input capacitance increased, through larger chip size, but also the channel length is shorter, increasing output capacitance. To summarise, the higher the power rating, the larger the die size, the higher the parasitic components and the slower the maximum attainable switching speed.

As has been mentioned, the device has a positive $R_{\text {dron }}$ temperature coefficient, it is often said that paralleling of devices is a simple matter and that, because of the positive temperature coefficient, the devices will equalise the current shared between them. This is not strictly correct (Kassakian 1983, Gauen 1984, Forsythe 1981). It is true that current hogging (i.e. almost all the current tending to go through one device) does not occur. Current is shared (when in the on or conducting state) in relationship to the drain-source 'on' resistance of each device (as with paralleled resistors). The balancing effect of the positive $R_{\text {dson }}$ temperature coefficient is minimal, particularly if the devices are mounted on the same heat sink.

A further complication, when electrically paralleling devices, is that a high frequency parasitic oscillation can occur (Severns (ED.) 1984a). When power MOSFETs are paralleled, a resonant circuit is established between the gate lead inductance and parasitic capacitances. Since the unity gain cut-off frequency of a power MOSFET is high, self sustaining parasitic oscillations can occur which may result in a voltage
breakdown of the MOSFET gate-source oxide. Even if the gates are not directly paralleled and separate drive circuits are used, the reverse transfer capacitances provide the necessary energy feedback. At a certain frequency this feedback becomes positive, resulting in destructive oscillation. A practical solution to the problem is the introduction of differential mode ģate resistance, either as lumped components, or by the use of polysilicon overlays to damp parasitic oscillations.

Of the devices so far mentioned, the power MOSFET is perhaps the most applicable to high speed switching operation. It is therefore worthwhile spending a little extra time to discuss the effects which limit switching speed. Figure 2.7 depicts an ideal device with associated parasitic elements. The different elements are described in Table 2.2.


Figure 2.7 Power MOSFET With Associated Parasitic Components.


At moderate switching speeds, 50 to 200 ns (i.e. at switching frequencies of 100 to 500 kHz , say), the principal components affecting switching time (Gyma et al. 1980, Kor et al. 1983, Bullough et al. 1982, Clement et al. 1981) are:

1) At turn on: the input capacitance ' $C_{\text {iu }}$ ', consisting of the gate-to-source capacitance ' $C_{g}$ ', associated with the drain-to-gate or Miller capacitance ' $C_{d g}$ ', is in series with the gate drive impedance. This forms a low pass filter which slows down the rising edge of the drive waveform. This is aggravated by the Miller and varactor effects of $C_{d d}$ during switching.

At high drain-source currents, rapid change in the drain current (i.e. large $\mathrm{d} i d \mathrm{~d} t$ ) can cause source feed back effects, due to voltage developed across the finite source inductance. This reduces the effective gate drive voltage and further increases switching times.
2) Turn off is affected not only by the above but also by the drain-source (or output) capacitance in association with the load impedance. This capacitor takes a finite amount of time to charge (via the load) and can be the main limiting factor on turn off time.

Parasitic elements such as the gate and source lead inductance should not be ignored at higher frequencies. This inductance varies depending on the package used, the manufacturer and the number of silicon dice per package. For the ubiquitous TO3 single die package, gate and source inductances are typically of the order of 12 nH . In general, inductance is larger with metal can packages than plastic since the can is made of a ferrous material.

A final parasitic component is the internal gate series resistance ' $R_{z}$ '. This varies according to die size and the gate material, for a polysilicon gate structure (favoured by the major manufacturers) $R_{g}$ is typically 2 to $10 \Omega$. For an aluminium gate it is less than $0.5 \Omega$. One Japanese development (Ikeda et al. 1980a) is the self aligned molybdenum gate structure which offers a significant improvement, in terms of frequency response, over a polysilicon gate structure (Figure 2.8).


Figure 2.8 Comparison of Frequency Response for Polysilicon Gate and Molybdenum Gate.

Knowing the values of these parasitic components, an approximation of the theoretical minimum tum on and turn off times can be made. This is done in detail in Appendix I for a typical high power MOSFET (the $\operatorname{RF} 450$ ) switching a $12 \Omega$ load with a 14 V gate drive and a drain supply voltage of 300 V . The total time required to take the device from fully off to fully on and bask to fully off is of the order of 75 ns . This suggests an absolute maximum switching frequency of about 12 MHz where the switching time occupies $25 \%$ of the cycle. Here the switching losses alone approach the maximum power dissipation of the device.

In general, these switching times cannot be achieved (when switching high power levels) since, to avoid over voltage transients on the gate drive due to parasitic elements ringing in response to an applied step input, a small external gate resistance of the order of 3 to $10 \Omega$ is often required to damp out oscillations (Clement et al. 1981), although if the gate drive is of a low enough inductance (resulting from careful circuit layout), this resistor can be omitted (Severns et al. 1986). In addition, the simple model of Appendix I has neglected the effects of device lead inductance. The most dominant being drain and source inductance since these experience the greatest rate of change of current.

The effect of the drain inductance is to reduce the rate of rise of drain current whilst allowing the drain voltage to collapse. The source inductance introduces source feedback which opposes the applied gate voltage and thus reduces switching speeds. This source feedback must not be confused with that caused by the source bulk resistance which is dominant when the device enters saturation.

The effect of the source inductance can be quantified by considering that the MOSFET switches 7 amperes in 10 ns . The rate of rise of current $\mathrm{di} d \mathrm{dt}$ is $700 \mathrm{~A} / \mu \mathrm{s}$. For an IRF450 the stray source inductance is 12 nH . Thus the feedback voltage developed during switching is 8.4 V , reducing the applied drive voltage to 1.6 V . In fact the rate of rise of current is limited to the level which the remaining drive voltage can produce.

One parasitic component which so far has not been mentioned, and which must be considered even at moderate switching frequencies, is the anti-parallel diode and its recovery time. In most commercially available power MOSFETs this device has reverse recovery times $\left(t_{7}\right)$ of $1 \mu \mathrm{~s}$. If a voltage fed, single or double ended bridge is used, design considerations must ensure that current commutates from the conducting diode to its associated transistor in order to avoid a crowbar action. This is to say, in a resonant voltage fed converter the frequency of operation must be slightly above resonance (Frank et al. 1982).

To overcome this problem MOSFETs are now being marketed with fast recovery epitaxial anti-parallel diodes, the so called FREDFETs; e.g. Siemens BUZ211. These have recovery times of the order of 200 to 300 ns which greatly reduce diode recovery losses. However, if operating in the MHz region care still needs to be taken to ensure commutation takes place as described above.

A final limiting factor on the high frequency operation of power MOSFETs is their $\mathrm{d} v_{d} / \mathrm{d} t$ rating (maximum allowable rate of rise of drain voltage). There are four types of $d v_{d} / d t$ spurious tum on modes identified in power MOSFETs (Severns 1981, Sevems 1984b).

The four modes can be explained by reference to Figure 2.7.

Mode 1) This first mode of spurious dv$v_{d} / d t$ turn on is caused by charge coupled through $C_{d q}$ and $C_{\operatorname{stry}}$ into $C_{p r}$. If the impedance of the gate drive circuit is sufficiently high then $C_{p}$ will charge to a voltage above the threshold level of the MOSFET and the MOSFET will start to conduct. This turm on mode is not usually destructive but it does increase device dissipation. This is the simplest mode of turn on to avoid, all that is required is appropriate design of the gate drive circuit.

Mode 2) This turn on mode is caused by charge injected into the base of the parasitic BJT by $C_{d .}$. If the voltage across $R_{b}$ exceeds 0.6 V then the BJT will start to conduct. This reduces the breakdown voltage of the BJT resulting in avalanche breakdown. If $i_{d}$ is not limited, secondary breakdown of the BJT can occur destroying the device. This turn on effect occurs at rise times of the order of 3 to 4 ns and the maximum rate of rise of drain-source voltage, although not specific in data sheets, is generally understood to be in the 10 to $20 \mathrm{~V} / \mathrm{ns}$ range (Lottet al. 1984, Kuo et al. 1983).

Mode 3) This occurs when the device reverse rectifier is used as a freewheeling or catch diode with inductive loads. The current path is shown in Figure 2.9. Since, even in the inverted mode, the parasitic BJT will have finite gain, some current flows emitter to collector, saturating the base region with charge.

$I_{1}=$ MAIN CURRENT FLOW.
$I_{2}=$ BJT CURRENT
FLOW DUE TO INVERSE GAIN

Figure 2.9 Body-Drain Diode Current Path.

Mode 3 breakdown occurs when the base collector diode recovers from a reverse current flow due to an applied reverse voltage causing large $L \mathrm{di} / \mathrm{dt}$ effects (dependant on the 'snappiness' of the diode's recovery) which cause the BJT to turn on as in Mores 2.

Mode 4) As with mode 3 this occurs when the device reverse rectifier is used as a freewheeling or catch diode. The device goes into avalanche breakdown caused by the large voltage spike on diode recovery before the BJT turns on. Both of these turn on modes are destructive.

It can be concluded that the realistic maximum switching frequency of higher power MOSFETs (i.e. above 2 kW power handling capability) is of the order of 1 to 5 MHz . This upper frequency limit is imposed mainly by device and external parasitic elements (Baliga 1987).

At higher switching frequencies, other factors must be considered. The input impedance of a power MOSFET is dominated at low frequencies by the input capacitance. In the off state this is mainly the gate-source capacitance, whilst in the active region it is principally the drain-gate capacitance amplified by the Miller effect, whereas in the on state, the input capacitance is determined by the gate-source capacitance in parallel with the drain-gate capacitance. Thus as the switching frequency increases, the input impedance of the FET decreases.

Although $C_{d g}$ is voltage dependent (since it is a depletion layer capacitor; the lower the applied voltage the higher the capacitance) its affect upon $C_{i s}$ is minimal above 5 volts drain-to-source and, as an approximation when calculating input impedance, the input capacitance can be taken as being equal to $C_{g}$.


Figure 2.10 Simplified Gate Circuit.
A simplified gate-source circuit can thus be drawn as in Figure 2.10. The impedance of this circuit, with components typical of an IRF450 (500 V 12A device) to the fundamental component of a 5 MHz gate drive square wave is:

$$
\begin{equation*}
Z_{\mu}=15.3 \angle-82.5 \Omega \tag{2.2}
\end{equation*}
$$

and at 10 MHz this drops to:

$$
\begin{equation*}
Z_{x y}=6.75 \angle-72.77 \Omega \tag{2.3}
\end{equation*}
$$

In fact the circuit is self resonant at 23 MHz . These impedance figures are very much removed from the quoted d.c. input impedance of $200 \mathrm{M} \Omega$.

As the switching frequency increases, the power loss in the MOSFET gate can no longer be ignored. For a switching frequency of ' $f$ ' Hz , power dissipated in the gate (assuming no drive circuit impedance) is given by Equation 2.4, derived in Appendix II.

$$
\begin{equation*}
P_{z}=C_{\text {is }} V_{\text {diva }}^{2} f_{z}=Q_{z} V_{\text {dind }} f_{z} \tag{2.4}
\end{equation*}
$$

Where: $\quad Q_{s} \quad$| is the charge given to and extracted from |
| :--- |
| the gate during each cycle; |
| is the applied drive voltage. |

For an IRF450 with a 10 V gate drive, $Q_{z}$ is approximately 80 nC . If the gate drive circuit contains source impedance $R_{\text {dime }}$ then the power dissipation in the gate is now given by:

$$
\begin{equation*}
P_{s}=Q_{z} V_{\text {dinin }} f\left\{\frac{R_{z}}{R_{d \text { dive }}+R_{z}}\right] \tag{2.5}
\end{equation*}
$$

For a 5 MHz switching frequency, the power dissipated in the gate of an IRF450 is approximately 4 W . It is not clear from the literature how much power can be dissipated in the gate and there is some dispute among the manufacturers on this point. However, one can make intuitive assumptions that, since the gate structure covers most of the surface of the die, it should be able to dissipate greater than 4 watts.

### 2.5.1 The Self Aligned Terraced Gate MOSFET

This is one of the later developments of the double diffused vertical power MOSFET (Ueda et al. 1984). It utilises a new type of self aligned gate structure by forming a thick oxide layer on the gate drain overlap region, Figure 2.11. This gate oxide structure reduces $C_{z}, C_{d q}$ and $C_{d s}$ by 20,80 and $10 \%$ respectively per unit gate width.


Figure 2.11 Self Aligned Terraced Gate MOSFET.
A $500 \mathrm{~V}, 2.3 \Omega$ experimental STG MOSFET developed by Ueda exhibited rise and fall times of 5 and 20 ns respectively.

### 2.5.2 The Interdigitated Gate Structure

It has been suggested that the cellular structure of commercially available MOSFETs is not optimum for high frequency operation (Fuoss 1982). Although the cellular vertical DMOS structure (Figure 2.12a) makes efficient use of silicon area, it leads to an increased parasitic gate to source capacitance, limiting switching performance.

An interdigitated gate structure (Figure 2.12b) requires more active area, resulting in larger drain-to-source output capacitance but the gate-source input capacitance is significantly reduced. This, coupled with a low resistivity gate material, significantly improves tum on time.

The experimental device fabricated achieved a 110 V breakdown voltage, 'on' resistance of $5-6 \Omega$ (cf. a 100 V IRF150 which has a $\left.0.055 \Omega R_{d d(m)}\right)$, and showed rise times of 500 ps . However, it must be stressed that since output capacitance is the major contributor to fall times, this device, with its increased $C_{d}$, would not show a marked improvement in tum off times.
(a)


Figure 2.12 Design Comparison for Vertical DMOS FETs.
(a) Layout and cross-sectional views of:

1. Interdigitated gate structure; and
2. Conventional cellular structure.
(b) Total device-area ratio and input capacitance ratio for structures 1 . and 2. as a function of gate width.

### 2.5.3 The Low Reverse Transfer Capacitance VDMOS

A further new VDMOS transistor structure has been proposed (Sakai et al. 1988) which reduces the reverse transfer capacitance of the power MOSFET. Essentially the structure contains an additional pregion (Figure 2.13) formed at the surface of the nepitaxial layer. This extra pregion reduces the voltage dependant capacitor $C_{r a}$.


Figure 2.13 Low $C_{r e}$ VDMOS Structure.
Tests on the new structure have shown that the reverse transfer capacitance is reduced by $50 \%$ without affecting source breakdown characteristics, although the on resistance is increased by $15 \%$. Improvement in switching speed being of the order of $35 \%$.

One potential problem with this structure is that the second parasitic, npn BJT created by the added $p^{\circ}$ region could reduce $\mathrm{d} v / \mathrm{d} t$ immunity.

### 2.5.4 Third, Fourth and Fifth Generation Devices

Since the advent of the power MOSFET in the late 1970's, improvements have continually been made, particularly with respect to reduced 'on' resistance and greater power handling capability, both through the use of greater die size (Hollinger 1986) and the use of multi-die packages (Colley 1986 and Bresch 1986). More recently, improvements have also been made in terms of greater ruggedness, larger safe operating area (SOA) and greater over voltage capability (Hollinger 1986, Zommer 1986).

### 2.5.4.1 Avalanche Rated MOSFETs

Improvements in device characteristics, especially SOA, have arisen from improvement in device symmetry and a lower $\mathrm{p}^{+}$region parasitic BJT base-emitter shorting resistance. This results in power

MOSFETs having a limited, over voltage break down, recovery capability (early devices could dissipate no energy when in avalanche breakdown). These improvements have further increased the $\mathrm{d} v / \mathrm{d} t$ rating of the body-drain diode upon reverse recovery (Grant 1987, International Rectifier 1988).

When a power MOSFET initiates avalanche breakdown, current flows through the drain body diode and partly through the base region of the parasitic BJT. Sufficient base current to cause turn on of the BJT causes second breakdown and thus device failure.

Although 1985 devices always went into second breakdown as soon as the drain voltage rating was exceeded, more modem devices can sustain an unclamped inductor turn-off voltage. Providing avalanche current is below a specific level, stored inductor energy can be safely dissipated (Carison 1986).

Since 1987, data sheets for power MOSFETs have carried an avalanche current rating. This specifies the maximum, unclamped, inductive current which can be switched with the MOSFET entering into a recoverable avalanche break down mode. The avalanche current capability is die temperature dependant (Blackburn 1988). That is the energy which can safely be dissipated during avalanche breakdown decreases as the turn off current increases or as the case temperature increases.

### 2.5.4.2 'Smart' MOS Devices

Whilst improvements have been taking place in device ruggedness and power handling capability, work has been proceeding on the integration of the power MOSFET device with its control and protection circuitry. Since fabrication of the power MOSFET is by processes similar to that of low voltage MOS integrated circuit manufacture, it is relatively easy to fabricate both the high power MOSFET structure and low power, low voltage control, drive and protection circuits on the same piece of silicon.

The majority of applications for such devices are in the auto-mobile industry, where a reliable, easily controlled, self protecting switch is required to replace the relay (Siemens 1987), and in low power, single chip, d.c.-d.c. voltage converters (Dewsbury et al. 1987).

There is no reported commercial effort at present, though, to use such technology to improve the switching speed of power MOSFET devices.

### 2.5.4.3 Current Sensing MOSFETs

Several manufacturers have developed a power MOSFET specifically for use in current mode control, switched mode power supplies (Cordonnier 1987, Young 1987). This device obviates the need for a separate current sensing resistor which is normally placed in the source connection of the power MOSFET.

The current sensing n-MOS symbol and circuit schematic is shown in Figure 2.14 and has two source (one being the sense, or mirror), drain, gate and kelvin connections. The drain, source and gate are identical to a standard MOSFET, as is operation. In current sensing devices, however, a small number of the individual MOSFET cells are isolated from the rest. These 'sense' cells mirror the operation of the source by taking a fraction of the total drain current to provide a constant ratio of the drain current. A typical sense ratio is 1:1800 (Frank 1986).


Figure 2.14 Current Sense MOSFET Equivalent Circuit.
The kelvin connection is used to minimise millivolt errors that result from high current, inductive switching transients. The kelvin contact is bonded to the source metalisation close to the sense cell area of the die. It has been suggested that this extra source contact could be used as the gate drive return, there-by avoiding source feedback effects, and increasing switching speeds (International Rectifier 1988).

### 2.5.5 RF Power MOSFETs

There are a number of power MOSFETs designed specifically for use in RF applications in the HF $(3-30 \mathrm{MHz})$, VHF $(30-300 \mathrm{MHz})$ and UHF ( $300-3000 \mathrm{MHz}$ ) bands, and have similar ratings to long standing, bipolar RF transistors (Motorola 1984, Hejhall 1982, Appel et al. 1982, Ikeda et al. 1982).

These transistors are designed to be used in linear Class A, AB, B or exceptionally Class C wideband amplifiers (Granberg 1981 and 1983a), working with a $6,12.5,24,50$, or exceptionally, a 100 V drain supply voltage. Also, experimental Class D amplifiers employing these devices and operating at frequencies up to 10 MHz have been reported in the literature (Granberg 1981).

Highest power devices available are: Motorola's MRF154 which can produce 600 W of ouput power at 30 MHz with a typical gain of 16 dB (i.e. 15 W input power) when operating off a 50 V drain supply; and MA/COM-PHI's DVD150T which can produce 180 W at 100 MHz with a typical gain of 16 dB (i.e. 5 W input) when operating off a 120 V drain supply.

Unlike the choice between power bipolar transistors and power MOSFETs when operating at switching frequencies in excess of 50 kHz , the advantages of RF MOSFETs over RF bipolar transistors for use in linear amplifiers are less clear cut (Hejhall 1982).

The main advantages of RF MOSFETs are:
higher d.c. bias impedance and therefore less complex bias circuits;
greater tolerance to VSWR mismatch;
exclusion of thermal runaway; and
slightly higher gain.
Their main disadvantage is cost. A power FET requires 50 to $100 \%$ more die area than a bipolar transistor for equal power rating. This is mainly due to the higher saturation voltage, but the geometry also gives some $30 \%$ less gate periphery than the available base area in bipolar devices. Since the price of a solid state device is a function of die size, FETs are more expensive, watt for watt, than bipolar transistors. For example a pair of matched, $150 \mathrm{~W}, \mathrm{RF}$ BJTs can be obtained for the same price as a single, $150 \mathrm{~W}, \mathrm{RF}$ FET. Comparisons between RF MOSFETs and RF bipolar transistors are made in Table 2.3.

Table 2.3 Comparison of RF Power MOSFETs with RF Power BJTs

|  | RF Bipolar | RF FET |
| :---: | :---: | :---: |
| $\mathrm{Z}_{\text {is }}, \mathrm{RS} / \mathrm{XS}$ ( 30 MHz ) | 0.65-j0.36 $\Omega$ | 2.2-j2.8 $\Omega$ |
| $Z_{o l}$ (load impedance) | Almost equal in each, depending on power level and supply |  |
| Biasing | High current voltage source necessary. <br> Fails usually under current conditions. <br> Thermal runaway and secondary breakdown possible. | Low current voltage source required. <br> Failure modes: gate punch through; exceeding gate break down voltage; over dissipation. |
| Advantages | Wafer processing easier. Low collector-emmiter saturation voltage. | Input impedance more constant under varying drive level. Lower high order IMD. Devices or Dice can be paralleled. Lower d.c. bias requirements. More tolerant to load mismatch. High voltage devices easier to implement. |
| Disadvantages | Low input impedance with high reactive component. Internal matching required to lower Q. <br> Input impedance varies with drive level. <br> Devices or dice cannot be easily paralleled. | Larger die required for comparable power level. <br> Non-recoverable gate breakdown. High drain-source saturation voltage. <br> About $50 \%$ more expensive Watt for Watt |

Japanese manufacturers favour geometries with horizontal channels (lateral MOS devices as opposed to vertical). Required power levels are achieved by paralleling several elements on one die. This technique represents a more wasteful use of the die surface than for vertical MOS structures but results in smaller parasitic capacitances.

It is possible, by using the combined power of several power amplifier modules (Granberg 1982, Gottlieb 1982), to achieve powers in the kW level into $50 \Omega$, but the circuits are complex and expensive. Because devices have a low voltage rating compared with valves, power is achieved by low voltage; high current circuits which, although ideal for transmitter applications, is less than ideal for dielectric heating.

There are a number of reasons why solid state RF transistors are low voltage devices, one is principally related to market demand. The major application is in transmitter amplifiers designed for mobile communication equipment. Hence devices are designed to operate off low voltage, battery supplies. The second reason, as previously stated, is that it is easier to fabricate low voltage high current components due to $\mathrm{d} \nu / \mathrm{d}$ limitations, parasitic elements etc. than it is to fabricate high voltage low current devices.

### 2.5.5.1 The RF Packaged Power MOSFET

One very recent development is the packaging of standard power MOSFET die in an RF case. Directed Energy, an American company involved with pulsed power applications, have incorporated two, standard, IRF840 MOSFET dice into an RF strip line package with a second source terminal attached for gate drive purposes. Use of the second source terminal reduces source lead inductance feedback effects when switching large currents at high speed. The device was developed for pulsed power systems where a 1 ns driver was required to drive the grid of triode valves (Krausse 1987).

Switching speed capability of a typical power MOSFET cell is of the order of 200 ps , the polysilicon gate structure resistance (as opposed to Aluminium) reduces this to 500 ps but the largest inhibitors to fast switching are source lead inductance and packaging.

The RF packaged switch is capable of switching $500 \mathrm{~V}, 10 \mathrm{~A}$ in 1.3 ns. Krausse reported that standard packaged IRF 840 's driven by the same drive circuit were capable of $10-90 \%$ fall times of only 10.8 ns .

The drive circuit used consists of modified RF bipolar devices, driven in their linear region, i.e. outside saturation, and only low duty ratios of operation are possible. The company is now marketing a commercial range of such devices, prices being approximately $\$ 300$ each at 1988 prices.

### 2.5.6 The MESFET (GaAs FET)

The Gallium Arsenide Field Effect Transitor (GaAs FET) has been slowly established over the last decade for low to medium power (up to a few tens of watts) amplification in the microwave region. Although power levels are small and operating frequencies rather higher than required in dielectric heating (e.g. devices are generally designed for use between 100 MHz and 10 GHz ), they are worthy of a mention as potential, high speed, high power components. The use of GaAs as an improved semiconductor material for power devices in the HF range has, in the main, been overlooked.

The major advantage of GaAs over silicon is that, for a per unit area of semiconductor material, group III-V semiconductors, such as GaAs, can carry up to eight times the current than their silicon counterpart. This superior power handling capability results from their higher electron mobility, as well as a larger energy band gap (Baliga 1982). Indeed it has been shown that for devices with the same breakdown voltage and device structure, the on resistance is inversely proportional to the third power of the energy band gap and inversely proportional to the mobility (Baliga et al. 1981a).

In addition, the frequency response of these devices (neglecting parasitic components) increases in proportion to the mobility and the energy band gap.

$$
\begin{equation*}
f_{T} \propto \mu E_{z} \tag{2.6}
\end{equation*}
$$

Where: $\quad$| $f_{\tau}$ is the cut off frequency; |
| :--- |
| $\mu$ is the electron mobility; |
| $E_{z}$ is the energy bandgap of the |
| semiconductor. |

Thus for devices with equal power handling capability, GaAs components can be significantly smaller, resulting in smaller parasitic elements. This, coupled with increased mobility, raises the operating frequency. Recent investigation of alloy semiconductors, such as GaAlAs and GaAsP, have shown them to be superior, in terms of current handling capability, even to GaAs devices (Baliga 1982).

However, the successful development of high voltage power FETs using group III - V materials is limited by a number of technical considerations. Very high purity $n$ type epitaxial layers with low doping concentrations and good electron mobilities are required. Also, the ability to fabricate high voltage pn junctions (unnecessary in microwave GaAs devices) and to invert the surface of the $p$ type GaAs to obtain $n$ channel MOSFETs is required.

Recent developments have shown that high purity GaAs can be grown to obtain high breakdown voltage Schottky diodes (Sears et al. 1981, Baliga et al. 1981b). Unfortunately the normal development of enhancement mode devices (favoured by circuit design considerations) using MIS (Metal Insulated Semiconductor) structures on GaAs, which allows inversion of its surface, is a problem that remains unsolved.

The alternative to the MOSFET is the junction FET. High voltage, vertical, GaAs junction FETs have been experimentally fabricated using buried gate regions to yield breakdown voltages of 150 V , blocking gains of over 10 and gate turn on and off speeds of less than 5 ns (Campbell et al. 1982). Thus, despite technological difficulties, the significant advantages of replacing silicon with GaAs should encourage further development of this technology although it is unlikely that commercial devices will be available this decade.

### 2.5.7 The ISOFET

This is a variation on a V-groove MOSFET (Figure 2.15), while the V-groove MOSFET features a recessed channel (this is difficult to manufacture, hence $V$-grooved devices have fallen out of favour with most FET manufacturers) the ISOFET uses an inverted V-groove MOS pattern to place the channel closer to the surface of the device where electron mobility is higher. As a result, the power gain of the improved structure is 6 to 10 dB higher than comparable MOSFET designs, the frequency coverage being typically four times as high (Moss 1983).


Fig. (b)

Figure 2.15 V -groove MOSFET.
The ISOFET (lower) represents a modified VMOS transistor (upper).

The gate to drain capacitance is approximately one fourth that of comparable RF MOSFETs. This low capacitance results from the device construction: since the channel is parallel to the surface, the gate length is shorter than with conventional MOSFETs. A metal gate structure, as opposed to polysilicon, also enhances high frecuency operation due to is lower resistance.

The ISOFET is a relatively simple device to fabricate, unlike GaAs FETs. It is constructed with a triple self aligned process, whereas a typical GaAs FET uses interdigitated fingers which are difficult to align. The ISOFET can be constructed using only five steps, or mask operations, whereas V-grooved MOS devices require eight or nine masks.

A further advantage of the short channel lengths is that the parasitic bipolar junction transistor, associated with the npn diffusion process, is less likely to spuriously tum on and thus destroy the device (Leighton 1983). Since the ISOFET has been developed with a greater SOA, for improved reliability, it is claimed in the literature that the ISOFET can withstand almost infinite VSWR without risk of damage from load mismatch.

Currently, ISOFETs are available at power levels of 120 W , designed to operate in the VHF and UHF bands. Devices for 100 to 300 MHz operation rated at 300 W are under development. The main area of application of the ISOFET is in medium power VHF amplifiers ( 100 W to 300 W ), this area is dominated by RF bipolar devices. Since, like the RF MOSFET, the ISOFET is inherently more stable than the BJT, circuit design will be easier with the ISOFET than with BJTs.

### 2.6 Bipolar-MOSEET Combinations

For low to medium power ratings, i.e. devices below 10 kVA capability, the power MOSFET is the closest device, currently available, to the 'ideal switch'. At higher powers, the chip size, and therefore the cost, become prohibitive (Fruendal 1984, Cogan et al. 1985). This has led to the development of a number of FET-bipolar combinations which aim to combine the advantages of the MOSFET (high speed, low drive requirements, increased safe operating area) with those of the bipolar transistor (low conduction loss, high current and voltage capability) (Chen et al. 1983, Rishmüller 1983, Bowler et al. 1986).

This approach, by necessity, cannot avoid compromises in performance, particularly in terms of switching speed. Thus, whilst FET-bipolar combinations cannot be considered 'ideal'; depending on the application, they can prove superior to either power MOSFETs or bipolar transistors used in isolation.

There are five main FET/bipolar combinations, namely: the cascade (or Darlington); parallel; cascode (or emitter turn-off); reverse emitter coupled (REC); and FET gated transistors (FGT). Each will be reviewed in turn.

### 2.6.1 The Darlington or Cascade Connection

This is the same configuration as a conventional bipolar Darlington pair (Figure 2.16). The FET provides the necessary base drive for the BJT and the BJT conducts the majority of the load current. Thus a high current capability switch, having low drive requirements, is formed.


Figure 2.16 Bipolar-MOS Cascade Connection.
At turn on, the FET conducts the whole of the collector current $\left(i_{c}\right)$ providing a large turn on current pulse to the base of the BJT (in fact an ideal turn on waveform), when the BJT starts to conduct the current taken by the FET reduces $i_{d} \beta$ where $B$ is the current gain of the bipolar transistor. Since MOSFETs have a good surge current capability, the FET need only have a current rating of $i / \beta$, it does, however, require the same voltage rating as the BJT.

The principal advantages of this circuit are: high current capability; low drive requirements; fast tum on; and inexpensive.

There are, however, a number of disadvantages. The BJT can only be used up to its collector-emitter breakdown voltage ( $B V_{c o o}$ ) and not to the higher rated collector-base breakdown voltage ( $B V_{c b a}$ ). Since, at turn off, the BJT is not reverse biased, turn off is through a process of minority carrier recombination in the base region and is therefore slow (typically $>1 \mu \mathrm{~s}$ ). Also, unless adequate snubber protection is provided, there is a risk of secondary breakdown. The safe operating area of the BJT is not enhanced by the MOSFET, further, the combination has a poor dv/dt capability, that is the FET in the configuration is subject to high rates of rise of drain voltage and any false turn on of the FET is amplified by the BJT. Finally, as with all Darlington combinations, the conduction drop is high.

The turn off time can be improved by incorporating a turn off diode as shown in Figure 2.17. Here the BJT is reverse biassed at turn off, greatly reducing storage and turn off time. Now, of course, the drive circuit must be capable of sinking the reverse base current of the BJT. A second disadvantage is that the BJT becomes prone to reverse bias secondary breakdown (RBSB).


Figure 2.17 Improved Bipolar-MOS Cascade Connection.

### 2.6.2 The Parallel Configuration

This configuration, shown in Figure 2.18, requires two, precisely timed, drive signals. The purpose of the FET is not to provide easy driving requirements but rather to act as an active snubber for the BJT during switching. At turn on, the FET conducts before the BJT and at turn off the BJT ceases to conduct before the FET. Thus the BJT is not subject to simultaneous stress of voltage and current. That is the FET performs the switching and the BJT carries the current. Because the BJT and FET are switched consecutively, turn off delay times are greater than for a BJT in isolation.


Figure 2.18 Bipolar-MOS Parallel Configuration.

As with the Darlington configuration, the breakdown rating is only $B V_{\text {cos }}$ and the FET is subject to the full voltage. stress but need only have a low current rating since the BJT caries the majority of the current. Again the $\mathrm{d} v / \mathrm{d} t$ rating is poor.

Its principal advantage over the Darlington connection is its low conduction drop, which is the lowest of all the bipolar/FET combinations (Lorenz 1986).

### 2.6.3 The Cascode (Emitter Turn Off) Configuration

The emitter open (or common base) technique of using a low power BJT to interrupt the emitter current in a large power transistor, overcoming problems of reverse bias secondary breakdown and improving the turn off times has been employed for a number of years (Chen 1981).

With the advent of power MOSFETs, this low power BJT has been replaced with a fast switching, low voltage MOSFET. In fact the MOSFET needs only to withstand 20 voits or so although it must have the same current handling capability as the power BJT. Nevertheless, low voitage, high current FETs are easy to manufacture and are therefore inexpensive.


Figure 2.19 Bipolar-MOS Cascode Connection.
As can be seen above in Figure 2.19, the basic configuration requires two drive signals. To turn on the switch and keep it conducting, base current must be provided to the BJT and a positive gate voltage maintained on the FET. The FET is turned off by a zero or negative gate voltage, this interrupts the emitter current of the BJT, diverting the collector current out of the base through the zener diode. This ensures that all the stored charge is 'swept' out of the base, resulting in short storage and fall times for the BJT. Storage times of $0.9 \mu \mathrm{~s}$ and fall times of 10 to 15 ns when switching 600 V and 10 A have been
reported (Rishmüller 1983) and more recently, cascode circuits have operated in $720 \mathrm{~V}, 300 \mathrm{~A}$ systems with tum-off current rates of $1000 \mathrm{~A} / \mathrm{us}$ (Goodfellow et al. 1988a) and in $300 \mathrm{kHz}, 30 \mathrm{~kW}$ supplies (Lafore et al. 1987).

The cascode configuration has several distinct advantages. One is the ease of turn off of a high voltage transistor without fear of RBSB, another is that the main transistor can be operated up to its $B V_{c b o}$ rating (which is usually twice the $B V_{\text {ces }}$ rating). In order to overcome the problem of having to provide a separate base drive for the BJT a drive can be tapped from the load current via a current transformer as shown in Figure 2.20 (Clement 1983).

Although there are commercially available MOSFETs with $1000 \mathrm{~V}, 10 \mathrm{~A}\left(@ 25^{\circ} \mathrm{C}\right.$ ) capability, their conduction drop and cost make the cascode arrangement an atractive alternative for switching frequencies below 400 kHz .


Figure 2.20 Bipolar-MOS Cascode Connection with Base Drive Transformer.

### 2.6.4 The Reverse Emitter Current (REC) Configuration

This connection, shown in Figure 2.21, reduces storage and fall times by reverse biasing the base emitter junction. This causes a negative base current, -ib, to flow which is higher than the collector current resulting in a reverse current to flow through the emitter-base junction. This reverse current rapidly discharges the base emitter junction capacitance.

With the cascode connection, emitter current at turn off is zero and the base-emitter capacitance is discharged through recombination, resulting in slightly longer storage times than for the REC.


Figure 2.21 Reverse Emitter Configuration (REC).
To obtain high negative base currents the MOSFET $\mathrm{Q}_{2}$ must be supplied with a voltage close to the base-emitter breakdown voltage of the power BJT (about 20 to 30 V ). This high negative voltage can drive the base-emitter junction into avalanche. To avoid subsequent overheating of the BJT the reverse drive must be removed after the BJT has turned off. Unfortunately this reduces the immunity of the switch to false $\mathrm{d} v / \mathrm{d} t$ turn on.

A second disadvantage of the REC over the cascode configuration is that the main transistor can only be operated up to $B V_{\text {coe. }}$. On the other hand, the voltage drop across the switch is the same as for a quasi saturated transistor (i.e. about 1 V ) and the MOSFET need only be a low voltage, low current device (since it need only take brief surge currents). This, in turn, results in shorter delay times, introduced by MOSFET tum on and tum off, than for the other combinations.

For collector-emitter voltages of 1000 V and collector current of 10 A , storage times in the region of 200 to 900 ns and collector current fall times of 15 ns have been reported (Rishmüller 1983). Turn on time for this configuration is similar to that for a quasi saurated transistor, typically about $1 \mu \mathrm{~S}$, putting maximum frequency of operation between 70 to 150 kHz .

### 2.6.5 The FET Gated Transistor

This is a combination of both the cascode and cascade connections, Figure 2.22. Referring to Figure 2.22, when the gate voltage is high both $\mathrm{Q}_{1}$ and $\mathrm{Q}_{3}$ turn on, $\mathrm{Q}_{1}$ provides a base current for $\mathrm{Q}_{2}$ and the whole
switch conducts. As with the cascade connection, $\mathrm{Q}_{1}$ provides an initial high base current 'kick' equal to the load current and, as $Q_{2}$ starts to conduct, $T_{1}$ reduces the base drive to $i d$. When the gate drive is removed (or taken negative) $Q_{1}$ and $Q_{3}$ tum off, interrupting the emitter current of $Q_{2}$ whose collector current is transferred out of the base and through the zener diode, rapidly turning off $Q_{2}$.


Figure 2.22 FET Gated Transistor.
This is an ideal BJT base drive current waveform which is accomplished with negligible gate currents and both turn on and turn off speeds are fast (Intemational Rectifier 1985). Even though two MOSFET input capacitances need to be charged and discharged, the combined capacitance is less than that for a FET with comparable rating to the entire configuration.

As with the cascode connection, the BJT can be operated up to $B V_{\text {cbo }}$ it does not suffer from RBSB and is largely immune to false turn on through high rates of rise of collector voltage ( $\mathrm{d} v / \mathrm{d} t)$.

The main disadvantage of the FGT is its large conduction drop which is typically greater than 6 to 7 volts.
For all these combinations, it must be appreciated that the switching time, including delay time; storage time; rise and fall times cannot be shorter than with a comparable MOSFET, for example the FGT has a turn off time typically 300 ns longer than a comparable MOSFET. Hence the advantages of these combinations are in improvement of the power handling capability and SOA of power MOSFETs rather than in increasing the switching speed.

As an aside, it is worthwhile pointing out that very fast switching speeds, although allowing higher frequency of operation, are not always desirable nor practically acceptable. For example, the cascode, FGT and REC combinations are capable of switching $3 \mathrm{kA} / \mu \mathrm{s}$, thus for every 10 nH of lead inductance, equivalent to the source lead inductance of a TO3 packaged MOSFET, 30 V is developed at turn on and turn off.

### 2.6.6 Monolithic Bipolar/FET Combinations

Of the above combinations both the parallel and cascade have been fabricated on a single chip. However, although the cascade device (Figure 2.23) exhibits low on resistance and low drive requirements, switching speed is relatively slow, limiting applications to those below 50 kHz .


Figure 2.23 Monolithic cascode Bipolar-MOS Combination.
More recent developments have focused attention on a MOS-gated-SCR variously called, by the different manufacturers: Insulated Gate Transistor (IGT or MOSIGT) by General Electric; Conductivity Modulated FET (COMFET) by RCA (Becke et al. 1982); Gain Enhanced MOSFET (GEMFET) by Motorola. All these devices are similar in structure, processing and specifications and can be grouped under the generic term: Injector FET (Chang et al. 1983, Goodman et al. 1983).

The cross sectional structure of an injector FET cell is compared with a MOSFET cell in Figure 2.24. In its simplest form, the injector FET is identical to the MOSFET except that the $\mathrm{n}^{+}$substrate has been replaced by a $p^{+}$'injector' layer. Figure 2.25 gives its equivalent circuit. The injector FET comprises of a MOS transistor driving a non latching, bipolar, silicon controlled rectifier. The result is a high input impedance, voltage controlled gate combined with the low on state losses of a bipolar transistor. The conduction losses are about one tenth of a comparably rated MOSFET, and, unlike conventional MOSFETs (for devices above 200 V drain breakdown rating), the 'on' resistance does not increase as rapidly with voltage rating. Thus the injector FET is of use in high voltage applications of 400 V and upwards.


Figure 2.24 Cross Section of Injector FET.


Figure 2.25 Injector FET Equivalent Circuit.

Low on state conduction losses result because the $\mathrm{p}^{+}$region injects the nepitaxial layer with a high concentration of carriers which increase, or modulate, the conductivity of the high-resistivity, epitaxial layer.

The main drawbacks of these devices are their slow switching speed and tendency, above certain collector current levels (and/or rates of change of collector current), for the parasitic SCR to latch, thereby removing gate control.

The different manufacturers have used varying techniques in an attempt to increase latching current and improve switching speeds. For example, RCA have improved turn off time, in experimental devices, from $10 \mu$ s to under 100 ns by generating recombination centres through high energy radiation and heavy metal doping. There is, however, a trade-off between speed and on resistance and it has been suggested that this may lead to families of injector FETs having various combinations of switching times and on resistance.

Latching current is increased by an emitter short which limits the current gain of the npn element. RCA achieve this with the combination of a heavily doped $\mathrm{p}^{+}$region in the centre of each cell and Al metalisation to short the $\mathrm{n}^{+}$and $\mathrm{p}^{+}$regions. In GE's IGT there is no $\mathrm{p}^{+}$region, instead, latching current is increased by keeping the $\mathrm{n}^{+}$cathode region narrow and the sheet resistance of the p base low.

However, this modified structure, which comprises a thin $\mathrm{n}^{+}$epitaxial layer between the $\mathrm{p}^{+}$substrate and nregion, is unable to withstand high reverse voltages.

These different approaches to avoid latching have resulted in a wide spread of switching speeds and conduction drops quoted by the different manufacturers. For example, present commercially available devices with a $600 \mathrm{~V}, 30 \mathrm{~A}$ rating have turn on times in the region of 200 ns to $0.5 \mu \mathrm{~s}$, tum off delay times between 300 ns and $1 \mu \mathrm{~s}$ and fall times between $2.0 \mu \mathrm{~s}$ and $4 \mu \mathrm{~s}$.

Because of the relatively slow switching speeds of these devices, they are only suitable for operating frequencies below 50 kHz and are aimed at high voltage, high current applications where their conduction losses are superior to those of power MOSFETs (below 200 V , MOSFETs exhibit lower conduction losses because of the, unavoidable, forward biased diode, conduction drop of injector FETs).

Although at low current levels (below 25 to $50 \%$ of rated current) the devices have a negative temperature coefficient of on resistance, at higher currents this becomes positive, allowing paralleling. The devices are also free from secondary breakdown and, unlike conventional MOSFETs, they will not conduct current in the reverse direction (because of their four layer pnpn structure).

Development and improvement of these devices is taking place rapidly. $100 \mathrm{~A}, 1800 \mathrm{~V}$ devices have been reported in the literature (Nakagawa 1986) having a conduction drop of 3 V (@ 30 A ) and fall times reduced from $10 \mu \mathrm{~s}$ to 500 ns . Also, complementary IGTs have been fabricated, with blocking voltages of 400 V and current ratings of 20 A (Ruble et al. 1985, Shulz 1986). These devices have a much lower conduction drop than equivalent pchannel MOSFETs.

In summary, this new generation of MOS structures have potential application in low, to medium frequency, switching circuits where high power devices with low conduction drop are required. In fact the main trend of research and development in the field of power electronic devices is towards higher power ratings at the expense of switching speed.

### 2.7 Conclusions

To summarize, it is apparent that the power semiconductor switch most suitable to high frequency operation is the power MOSFET. This device is capable of switching frequencies up into the low MHz region (albeit at reduced power levels). It is difficult to establish an absolute maximum operating frequency since this is dependent on circuit configuration as well as device type and construction.

Developments in high speed ( 5 ns switching), high voltage ( 150 V breakdown) GaAs FETs are encouraging. However, it is clear that the main development drive of power semiconductor manufacturers is towards higher power levels at lower switching frequencies, e.g. Bipolar/MOSFET combinations such as the IGT or COMFET, and at least one of the major manufacturers has abandoned further development work on high voltage GaAs devices (Baliga 1985).

High frequency bipolar transistors suited to linear power amplifiers have been available for several years and more recently (since about 1980) power RF MOSFETs have emerged. The advantages of RF MOSFETs over bipolar transistors in linear amplifiers are less clear cut than for devices developed for switching applications and it is questionable whether the advantages of RF MOSFETs outweigh their extra cost. This apart, in terms of dielectric heating supplies there is no overall advantage in using either solid state device in preference to the thermionic valve, particularly in terms of cost, where solid state devices are about four times as expensive watt for watt.

However, RF power MOSFET devices could be incorporated into low power solid state dielectric heaing supplies where the advantages of high efficiency, compactness, and battery powered capability could outweigh the increased expense of solid state devices over the thermionic valve.

Also, the potential high frequency capability of standard power MOSFETs suggests that they are suitable for use in high frequency induction heating supplies operating between 1 MHz and 7 MHz .

Chapter 3

## REVIEW OF SOLID STATE HIGH FREQUENCY POWER SOURCES

In this chapter, recent advances in high frequency converters and inverters are reviewed and predictions made upon likely future developments.

Comment is given upon their suitability for adaptation to high frequency ( $3-30 \mathrm{MHz}$ ) power sources for electric process heating applications.

## 3 REVIEW OF SOLID STATE HIGH EREOUENCY POWER SOURCES

With the advent of computers and their use in aerospace equipment, much research has been undertaken in the field of power conditioning. Because of the need to increase efficiency and reduce size, switching frequencies have steadily increased. This has brought about a number of new converter/inverter topologies which are more suited to high frequency applications than standard switched mode circuits (Hinchliffe et al. 1986b).

In this chapter standard switch mode supplies are reviewed, recent developments in resonant power convertors are discussed and the use of solid state linear amplifiers as high power, high frequency sources to replace the valve oscillator is considered.

In each case, the usefulness of the configuration to dielectric heating and high frequency induction heating applications is discussed and comments made upon realistic upper limits on frequency and power rating.

### 3.1 Switched Mode Supplies

### 3.1.1 Switching Regulators

The transistorised switching regulator, the most common type of power convertor, can be described as a d.c. - to - d.c. transformer. A number of configurations have been developed over the years, each with their own particular advantages and disadvantages (General Electric 1984).

The main use of the switching regulator is in low power ( $<1 \mathrm{~kW}$ ), low to medium frequency (generally operating up to a few tens of kHz , exceptionally a few hundred kHz (Matsumoto 1983, O'Brian 1988)) supplies where stabilised d.c. voltages are derived from a common d.c. rail. Several different switching regulator types are described briefly in Table 3.1.

### 3.1.2 Rectangular Wave Inverters

These were the first generation of high power transistorised inverters and are still widely used in low to medium frequency applications such as motor drivers, etc. As with the switching regulators mentioned above, many configurations have evolved to suit varying circuit requirements, cost criteria and so on.

Some of the more common inverter switching stages are given in Table 3.2. With all the stages shown, load line shaping has to be employed by the use of snubber circuits to avoid simultaneous high voltage across, and high current through the switching device (McMurray et al. 1977, Nair et al. 1984, Domb et al. 1985).


| TYPE OF CONVERTER | BUCK (STEP DOWN) | BOOST (STEP UP) | BUCK - BOOST | FLY BACK |
| :---: | :---: | :---: | :---: | :---: |
| IDEAL TRANSFER FUNCTION | $\frac{V_{o}}{V_{\text {in }}}=\frac{\tau}{T}=D$ | $\frac{V_{o}}{V_{\text {in }}}=\frac{T}{T-\tau}$ | $\frac{V_{o}}{V_{\text {in }}}=\frac{\tau}{T-\tau}(-1)$ | $\frac{V_{0}}{V_{\text {in }}}=\frac{N_{2}}{N_{1}}\left(\frac{\tau}{T-\tau}\right)$ |
| ADVANTAGES | High efficiency, simple, no transformer, high frequency operation easy to stabilise regulator loop | High efficiency, simple no transformer, high frequency operation. | Voltage inversion without using a transformer, simple, high frequency operation. | Simple, multiple outputs are possible. Collector current reduced by turns ratio of transformer. Low parts count, isolation. |
| DISADVANTAGES | No isolation between input and output. Requires a crowbar if $Q_{1}$ shorts. $C_{1}$ has high ripple current. Current limit difficult. Only one output possible. | No isolation between input and output. High peak collector current, only one output is possible. Regulator loop hard to stabilize. | No isolation between input and output. High peak collector current. Only one output is possible, poor transient response. | Poor transformer utilisation, transformer design critical, high output ripple. |



| TYPE OF CONVERTER | FORWARD | PUSH-PULL | Cúk (WITH TRANSFORMER |
| :---: | :---: | :---: | :---: |
| IDEAL TRANSFER FUNCTION | $\frac{V_{o}}{V_{\text {in }}}=\frac{N_{2}}{N_{1}}\left(\frac{\tau}{T}\right)$ | $\frac{V_{0}}{V_{\text {in }}}=2 \frac{N_{2}}{N_{1}}\left(\frac{\tau}{T}\right)$ | $\frac{V_{o}}{V_{\text {in }}}=\frac{\tau}{T-\tau}$ |
| ADVANTAGES | Simple, multiple outputs are possible, collector current reduced by ration of $\mathrm{N}_{2} / \mathrm{N}_{1}$. Low output ripple. | Simple, good transformer utilisation. Collector current reduced as a function of $\mathrm{N}_{2} / \mathrm{N}_{1}$. Good at low values of $V_{i n}$. | Continuous input and output current, highest efficiency, very low ripple, smallest number of switching components, switching losses low, drive current referenced to ground. Highest operating frequency. |
| DISADVANTAGES | Poor transformer utilisation, poor transient response, parts count high, transformer design critical. | Cross conduction of $\mathrm{Q}_{1}$ and $\mathrm{Q}_{2}$ possible, high parts count. Transformer design critical. Poor dynamic range. Poor transient response. | $C_{1}$ and $C_{2}$ have high ripple current requirements. Transformer design critical. Power output is limited. |

Table 3.16 Power Converter Circuits.

## Table 3.2 Inverter Switching Stages



## Single Quadrant Stage

Advantages: Only one switching element required.
Disadvantages: Power input to load (motor etc.) in first quadrant only. Diodes must be fast recovery to minimise reverse recovery in switch.


QUASI FULL BRIOGE OUIPUT STAGE

## Quasi Full Bridge Stage

Advantages: Power input to load can be achieved in two quadrants using a single d.c. supply. Disadvantages: Capacitors have a high ripple current, possibility of conduction overlap, isolated drives required.

## T(Push-Pull) Output Stage

Advantages: Power input to load in both quadrants (1 and 3).
Disadvantages: Bipolar d.c. supplies required, anti-parallel diodes must be fast recovery. Possibility of conduction overlap, hence 'dead band' must be employed.


## H(or Full) Bridge Output Stage

Advantages: Single d.c. supply. Power input to load in two quadrants. Potential divider capacitors not required.
Disadvantages: Four switching elements required, conduction overlap possible, isolated drives required.

There are a number of factors which limit the operating frequency of both switching regulators and rectangular wave inverters:
a) As was discussed in Chapter 2, the switching elements themselves pose a limit to the maximum operating frequency. The principal limit being the switching speed. For a 1 kW supply, say, devices currently available limit maximum operating frequency to below 1 MHz .
b) Since the waveforms are non-sinusoidal, high $\mathrm{d} / \mathrm{dt}$, $\mathrm{d} v / \mathrm{dt}$ of the switching edges in association with stray parasitic components can cause over voltage breakdown or false turn on of the devices.

Because it is impossible to eliminate completely, stray parasitic elements, they represent a major limitation to the upper frequency operation of switched mode supplies.

As a brief example, consider a 1 kW switched mode supply, operating from a 300 V d.c. rail, using switching elements with a 400 V rating operating at a switching frequency of 500 kHz :

For high efficiency the switching times should be less than two percent of the time period $1 / f_{s}$, where $f_{s}$ is the switching frequency.

Thus for $f_{s}=500 \mathrm{kHz}$, the rise and fall times are approximately:

$$
t_{\mathrm{r}}=40 \mathrm{~ns}
$$

Hence the rate of change of load current at each switching edge is:

$$
\begin{equation*}
\frac{\mathrm{d} i_{L}}{\mathrm{~d} t}=\frac{1 \times 10^{3}}{300} \times \frac{1}{40 \times 10^{-9}}=83 \mathrm{~A} / \mu \mathrm{s} \tag{3.1}
\end{equation*}
$$

Generating 83 V for every $1 \mu \mathrm{H}$ of stray wiring inductance.
c) During the switching transition the switching element is subject to both high voltage and high current simultaneously. Thus at higher frequencies, switching losses become predominant and limit the efficiency of the stage.
d) The harmonic content of the current drawn from the a.c. line is often high with these types of converters, as is the radiated Radio Frequency Interference (RFI). RFI problems in particular become more severe as the switching frequency is increased.

The main advantage of these supplies, apart from their simplicity, size and weight is that power control is readily achieved by pulse width modulation (Wilson 1978, O'Brian 1988).

One recent variation on the square-wave converter is the Milberger converter (Jones et al. 1987). This utilises two d.c. chopping H -bridges linked by a common transformer secondary which is wound, in series, onto separate transformer cores. The voltage produced on the secondary winding is the algebraic sum of the voltages which would be produced by each primary independently. Figure 3.1 shows the basic configuration and associated waveforms. Each H-bridge is driven at the same frequency, derived from a single oscillator. Output voltage control is achieved by varying the phase of one H -bridge with respect to the other (when the bridges are in phase the oupput is twice the primary voltage, for unity turns ratio, and when the bridges are $180^{\circ}$ out of phase the output is zero). Thus output voltage (puise width) can be controlled uniformly down to zero.


Figure 3.1 Milberger Converter.

This configuration has been operated at power levels of 3 kW at 150 kHz and 500 W at 1 MHz . High frequency operation is achieved by the use of a 'quasi' resistive load, that is to say the leakage inductance of the output transformers is utilized to give a slightly lagging load power factor resulting in zero voltage turn on of the power devices.

This type of converter retains many of the problems inherent in high frequency operation of rectangular wave converters described above. Its main advantage is that it overcomes the problems associated with pulse width modulation control such as poor utilisation of the output transformer at low pulse duration and finite minimum pulse width.

In short, rectangular wave converters/inverters are mainly used in low to medium frequency applications. Regardless of the speed of operation of the switching element, the actual circuit topology limits the maximum operating frequency to a few hundred kHz for medium power circuits ( $<1 \mathrm{~kW}$ ) and to a few tens of kHz for higher power circuits.

### 3.1.3 Resonant Converters-Inverters

In an attempt to overcome the problems associated with switching loss at high frequencies and the high harmonic content of rectangular wave converters/inverters, resonant converters/inverters were developed (Steigerwald 1984). There are two basic families of resonant inverters: voltage fed, employing a series resonant load circuit; and current fed employing a parallel resonant load circuit. Both have the advantage of reduced switching loss since switching takes place at or near a zero current or zero voltage crossing point respectively.

| Type | Conventional Rec- | Resona | nt Wave |
| :---: | :---: | :---: | :---: |
| Item |  | Voltage Resonance | Current Resonance |
| Efficiency | Good | Excellent | Excellent |
| Transistor and diode stress | Bad SOA, Good voltage, large recovery stress | Good SOA, Higher voltage stress and rating | Good SOA, Higher current stress and rating |
| Load open circuit tolerance | Average | Good | Poor |
| Load short circuit tolerance | Average | Poor | Good |
| Size, weight | Good | Fair | Fair |
| EMI, noise | Bad | Good | Good |
| Reliability | Good | Good | Good |
| Regulation | Good (by PWM control) | Good <br> (by MAG Amp control) | $\begin{gathered} \text { Fair } \\ \text { (by PPM Control) } \end{gathered}$ |

Both types of inverters have been used for many years, employing thyristors or bipolar junction transistors as the active elements (Okeke 1978, Matthes 1978). More recently, power MOSFETs have been utilised and the operating frequency of such inverter types increased to 100 kHz and above (Frank et al. 1982, Hinchliffe 1983, Tebb et al. 1984). Rectangular wave and resonant wave inverters are briefly compared in Table 3.3 above.

### 3.1.3.1 Series Resonant Inverters

A series resonant H -bridge configuration is shown on Figure 3.2. Ideal operation is as follows: switches 1 and 4 are turned on, applying a voltage across the series resonant circuit, the current in which builds and falls as a half sinusoid. As the load current resonates back towards zero, switches 1 and 4 are turned off, after a brief period (known as the 'dead time'), switches 2 and 3 are turned on, reversing the voltage across the load as the current in the load naturally reverses. When the load current has resonated to a peak in the opposite direction and then back towards zero, switch 2 and 3 are turned off and, again after the 'dead time' has elapsed, switches 1 and 4 are turned back on and the cycle repeated.


Figure 3.2 Series Resonant H-bridge Configuration.
Thus, under ideal conditions, the switching frequency of the power devices is matched to the natural resonant frequency of the load and switching takes place at a zero current crossing point, minimising switching loss.

The capacitor, RFBC, is purely a radio frequency by-pass capacitor used to supply the RF pulsed currents to the bridge, the inductor $L_{\text {chock }}$ decouples the RFBC from the supply ensuring that a clean current waveform is drawn from the mains supply. This inductor is also used to limit the current drawn by the bridge under fault conditions, allowing time for protection circuits to act.

The anti-paraliel diodes are used to take any lagging or leading current should the load be run off resonance. Generally, when employing power MOSFETs, the load is run slightly inductive, that is at a lagging power factor, this ensures that current commutates from the integral anti-parallel diode to its associated MOSFET, overcoming problems associated with the low recovery time of the power MOSFET's integral anti-parallel diode and mode 3 and 4 break down mechanisms as discussed in the previous chapter. Some designers incorporate a series Schotky diode with the power MOSFET to stop the integral diode conducting, an external fast recovery anti-parallel diode is used to carry any lagging or leading load currents. This has the added advantage of decoupling the output capacitance of the power MOSFET from stray circuit inductance, thus reducing 'ringing' at the switching transients (Frank et al. 1982, Hinchliffe 1983, Hinchliffe et al. 1987a, 1987b)

In order to ensure the correct phase relationship between the drive to the power MOSFETs and the load, a frequency feedback mechanism is often employed. Two main types have been proposed. In both cases the phase and frequency of the load current is detected by means of a current transformer (which can also be used for closed loop power control and overload detection). In one technique a proportion of the output current is fed back and its phase compared with that of the switching frequency, a phase comparator circuit is used to ensure that the switching frequency is slightly above the resonant frequency of the load, resulting in a lagging load current (Frank et al. 1982, Mauch 1986, Savary et al. 1987).

The alternative technique (Hinchliffe 1983, Hinchliffe et al. 1987a, 1987b, Lafore et al. 1987) uses a zero crossing detector on the secondary of the current transformer to detect the zero crossing transitions of the load current. The resulting pulses are used to frequency lock a PWM control IC to the load frequency. The required loading drive frequency being obtained by time advarving the zero crossing pulses applied to the control IC. A complete voltage fed, series resonant inverter control circuit employing the frequency lock technique is shown in Figure 3.3 (Hinchliffe 1983).

There are number of disadvantages with the series resonant circuit which will be briefly described below:
(i) The mode of operation of the voltage fed inverter, requiring a minimum dead time, is often described as "a short circuit waiting to happen." In that, should both devices in one leg be turned on simultaneously the supply is shorted through the switching devices.

The affects of such a malfunction can be minimised by ensuring that the radio frequency by-pass capacitor is of a minimum value and that the series choke in the supply limits the fault current until the protection circuits can react.

Similarly, under load short circuit conditions, the current in the switching devices can build rapidly. However, as mentioned, suitable design of the input filter ensures that protection circuits have time to react before damage to the active devices occurs.


Figure 3.3 Series Resonant Induction Heater Control Circuit.
(ii) At resonance, the impedance of the load falls to the effective RF resistance of the work coil and load. Thus an output transformer is often required to match the load to the inverter. This can be an expensive item for which there is no real solution other than using a pre-converter before the bridge to step down the voltage supplied to the bridge.
(iii) As the switching frequency increases, the time taken to switch becomes a greater part of the resonant time period of the load circuit. Since switching occurs close to the zero crossing point of a sinusoid, the rate of change of current is at a maximum. For any increasing, relative delay in turn on, the current through the load, and thus through the switch, increases rapidly, thereby raising switching loss.

Hence the realistic, maximum operating frequency limit of the series resonant circuit, at appreciable power levels, is approximately 1 MHz (Tatsuta et al. 1988).

The advantages of the voltage fed circuit are that it is inherently immune to open circuit load conditions, also the voltage across the H -bridge is clamped by the RFBC. This is important when voltage sensitive components such as the power MOSFET or SIT are used (Divan 1986). As is mentioned in Chapter 2, the power MOSFET is able to withstand quite high surge currents but has very little over voltage capability.

### 3.1.3.2 Parallel Resonant Inverters

A parallel resonant H -bridge configuration is shown in Figure 3.4. Ideal operation is as follows: the supply inductor $L_{\text {choke }}$ is assumed to carry a constant RF current, switches 1 and 4 are turned on, delivering the RF choke current to the parallel load which resonates, producing a half sinusoid of voltage at the output of the bridge. As the output voltage approaches zero, before current in the load reverses, devices 2 and 3 are turned on, shorting out the load and ensuring that the current in the RF choke is maintained. After the load current and voltage have reversed, due to the resonant nature of the load circuit, devices 1 and 4 are turned off and devices 2 and 3 are held on. As the load resonates back towards the positive half cycle, devices 1 and 4 are switched back on, devices 2 and 3 being switched off after the load has commutated and the cycle is repeated.

Thus, under ideal conditions, the switching frequency of the power devices is matched to the natural resonant frequency of the load and switching takes place at a zero crossing point of voltage, thereby reducing switching loss.

The inductor $L_{\text {choke }}$ is purely a radio frequency choke used to ensure a constant RF current and does not, normally, smooth the mains frequency ripple. This inductor inherently limits current drawn by the bridge under fault conditions (Tebb et al. 1984, Bottari 1985, Tebb et al. 1986b, 1986c, Pudney et al. 1986).


Figure 3.4 Parallel Resonant Inverter.
Generally, the current fed inverter is run at a slightly leading power factor, that is to say, the load current is always in advance of phase with the load circuit. This ensures that each MOSFET is naturally commutated off by the load, reducing the need for snubber components (Casella et al. 1987). The majority of authors propose a frequency phase lock loop circuit, similar to the control circuit used for the voltage fed inverter (except that the output voltage phase is detected rather than the output current), to ensure inverter operation is close to the resonant frequency of the load (Bottari et al. 1985, Casella et al. 1987). An altemative method proposed by Tebb (Tebb et al. 1986b, Leisten 1986, Leisten et al. 1988) is to use a microprocessor to detect minimum d.c. link current at resonance and to produce the required dive signals at calculated resonant frequency. The main problem with this approach is the speed of response of the microprocessor which is unable to follow rapid load transients.

The principal disadvantages of the parallel resonant circuit are outlined briefly below:
(i) The circuit is intolerant to load open circuit conditions or sudden falls in the load impedance. Under open circuit conditions the voltage across the inverting bridge rises rapidly (mainly under the influence of the RF choke) which results in over voltage breakdown of voltage sensitive components such as the power MOSFET.

This can be avoided by means of a fly back diode across the choke, but this results in a non continuous current being delivered to the bridge (Bottari et al. 1985, Hartman 1987, Casella et al. 1987).
(ii) The device voltage stress encountered under normal operation can be substantially higher than the supply voltage due to the resonant nature of the load voltage (Divan 1986).
(iii) Parasitic oscillations between the device output capacitance and stray inductance can result in large 'ringing' transients on the switch voltage waveform. This is exasperated by the fact that a path is established via the load tuning capacitance for these high order harmonic oscillations to be propagated in a loop within the bridge.

Several solutions have been proposed to deal with this problem. Most authors favour placing a blocking diode in series with the switching devices, preventing reverse conduction and isolating the device output capacitance from stray inductance (Bottari 1985, Mauch 1986, Casella 1987), this also reduces the peakresonant voltage seen by the switches. An alternative approach, proposed by Tebb, modifies the resonant circuit by placing an inductor in series with the resonating capacitance and large capacitor snubbers across the active devices to filter out the 'ringing' frequencies (Tebb et al. 1986a). This latter solution generates two further problems:
(a) The capacitors placed across the active devices form part of the tank circuit, increasing the current in the links between the bridge and parallel resonant load.
(b) Should the inverter be run off resonance, then the energy stored in the filter capacitors $\left(1 / 2 \mathrm{CV}^{2}\right)$ is dissipated in the active devices at the turn on transitions.
(iv) As the switching frequency increases, the time taken to switch becomes a greater part of the resonant time period of the load circuit. Since switching occurs close to the zero crossing point of a sinusoid, the rate of change of voltage is at a maximum. When operated at higher switching frequencies the increased, relative delay in turn on, results in a non zero voltage condition at the switching instant, thereby raising switching loss.

The major advantages of the current fed or parallel resonant inverter are:
(i) The inverter is inherently immune to short circuit load conditions.
(ii) It is generally easier to match the inverter to the resonant load. The impedance of the load, given as:

$$
\begin{equation*}
Z_{L}=\frac{L_{r}}{R_{L} c_{r}} \tag{3.2}
\end{equation*}
$$

Where: $C_{r}$ is thecapacitome of the tank circuit.
$L_{r}$ is the tank circuit inductance.
$R_{\mathrm{L}}$ is the RF resistance of the load circuit.
Can be such that a matching transformer is not required.
(iii) Over current caused by simultaneous conduction of devices in the same leg of the bridge is not destructive.

One variation on the parallel resonant inverter described above has been proposed by Kassakian (Kassakian 1982). This places the resonating capacitors directly across the switching devices which are configured in a half bridge arrangement as shown in Figure 3.5. One distinct advantage of this circuit is that a high voltage isolated drive is not required and the drive to both switching devices can be referenced to ground. A further advantage is that the device output capacitance can be incorporated into the resonant circuit allowing higher frequency operation. It does, however, suffer from many of the disadvantages associated with the parallel resonant circuit described above.


Figure 3.5 Kassakian Inverter.

### 3.1.3.3 Hybrid Series - Parallel Inverter

This circuit is similar to the quasi full bridge series resonant converter, except that the resonating inductor capacitor network is replaced by a series inductor and parallel resonant circuit. A configuration which can be used for induction heating applications is shown in Figure 3.6 along with associated waveforns (Carsten 1987a, Magalhaes et al. 1988).


Figure 3.6 Hybrid Series-Parallel Converter.

It operates with virtually zero switching loss since the active devices turn off into capacitive loads and on at zero voltage. Turning off into capacitive loads has the effect of clamping the device voltage until the current through the switch has reduced to virtually zero (depending on the size of the capacitive load). The circuit is frequency tolerant due to a zero $\mathrm{d} v / \mathrm{d} t$ region at switch on. With reference to Figure 3.6, for maximum power transfer the series inductance should be approximately $Q_{L}$ times the parallel resonant inductor (where $Q_{L}$ is the loaded $Q$ of the tank circuit being $=5$ ). The load circuit is run slightly inductive to aid commutation.

Advantages of the circuit are:

## Zero switching loss;

No step change in current or voltage;
Tolerant to open or short circuits;
Easily controlled and protected by combined:
(a) Maximum current limited by "toggling" the drive;
(b) Maximum on time (variable power control).

The voltage stress across the switches does not exceed the supply.
Disadvantages of the circuit are:

$$
\begin{equation*}
\text { Resonant } V A=K \times P_{\text {oun }} \tag{3.3}
\end{equation*}
$$

Where: $1<K<10, K=$ loaded Q ;

> Resonant $V A$ is a constant with respect to load;
> Non linear control over a large range;
> Simultaneous low voltage and low current operation requires a large frequency increase;
> The spread of delay in turn on and off times of components means that it is not possible to ensure correct timing of drive waveforms for upper and lower devices when operating in the MHz region.

Thus the circuit is useful for induction heating applications at frequencies below 1 MHz , but the possibility of simultaneous conduction of both upper and lower switches limits higher frequency operation.

### 3.1.4 Quasi Resonant Converters

In this new breed of d.c. to d.c. resonant converter circuits the resonant components are devolved from the load and placed around the active device to form a quasi resonant switch. The quasi resonant switch consists of a switching device and an additional inductor and capacitor to shape current and voltage waveforms. The resulting element can be used to replace a simple semiconductor switch in many standard
converter configurations. Resonant switch techniques can eliminate switching stress and losses, thus boosting the switching frequency into the low MHz region. The technique avoids the need for snubber networks required in standard PWM supplies to ensure operation in the SOA.
The actual implementation of the resonant switch can be either in 'hałf wave' configuration, where current can only flow in the forward direction, or in a 'full wave' configuration, where current can flow bidirectionally. Full wave quasi resonant switches reduce the sensitivity of the d.c. voltage conversion ratio to load changes.

There are two main types of resonant switch giving rise to two types of quasi resonant converter configurations (Liu et al. 1985).

### 3.1.4.1 Zero Current Switch Quasi Resonant Converters (ZCSQRC)

Quasi resonant converters combine sine and square waves, in zero current quasi resonance, current is sinusoidal and voltage square. A number of zero current quasi resonant switch configurations are shown in Figure 3.7. Operation of the zero current quasi resonant switch requires an inductive load and is analysed on the assumption of a constant current through the output inductor, for example buck, Cúk converter topologies etc.

(a)


(b)


(c)



Figure 3.7 Zero Current Quasi Resonant Switch Configurations and Ideal Waveforms.
(a) General topologies
(b) Half-wave
(c) Full-wave

Theory of operation of the zero current quasi resonant switch can be described by applying it to a flyback converter configuration. An equivalent circuit of a flyback converter incorporating a quasi resonant switch is shown in Figure 3.8. It is assumed that the resonating inductor $L_{r} « L_{m}$ and that the switch is turned on before the current in $\mathrm{L}_{\mathbf{m}}$ has fallen to zero.


Figure 3.8 Resonant Switch Flyback Converter Equivalent Circuit
After the switch (SW) is turned on the current $i_{r}$ will increase, at a rate determined by $L_{r}$ until it equals $i_{m}$. Diode D will now turn off. The rate of rise of the current in SW is much lower than in the equivalent conventional switch circuit and so the turn on losses are much reduced.
$L_{n} L_{m}$ and $C_{r}$ now form a resonant circuit which charges up $C_{r}$ and causes $i_{r}$ to rise sinusoidally to a peak and fall back to zero. The switch can now be turned off with very low losses. The voltage on $C$, is greater than the input voltage, therefore $S W$ will be reverse biased and will need a reverse blocking capability. This means, in practice, that $S W$ will be the series combination of a controllable switch, e.g. a transistor, MOSFET, GTO etc., and a fast diode.

With the switch is turned off, the resonant circuit $L_{m} / C_{r}$ causes $i_{m}$ to increase and the voltage $v_{c}$ to fall until it equals $V_{\sigma}$. Diode D will now turn on and the current which was flowing into $C_{r}$ will now flow into the output smoothing capacitor and the load. The current $i_{m}$ decreases until the control circuit turns switch SW on once more.

Thus the reduced switching losses arise from:
$L_{r}$ acting as a di/dt limit at switch on;
The resonant circuit $L_{r} L_{m}$ and $C_{r}$ ensuring that the current is zero at turn off.

For a half wave switch, i.e. one which conducts in only one direction, constant output voltage for varying load conditions is maintained by varying the operating frequency. As the load impedance increases, the frequency lowers. Theoretically at zero loading, frequency of operation is zero.

The full wave switch, i.e. conduction forward and reverse, is not load sensitive. The quasi resonant converter can utilize the leakage inductance of the ouput transformer by moving the resonating capacitor into the secondary circuit. In a full wave quasi resonant switch a Schottky barrier diode is used to prevent the internal body diode of the FET conducting and a 'wrap round' reverse diode is incorporated. The half wave quasi resonant switch exhibits less ringing at the expense of a longer off time.

There are a number of basic problems associated with the zero current quasi resonant switch:
At turn on, energy stored in the diode junction capacitance is transferred into the switch. Thus at high frequencies of operation a substantial amount of energy can be dissipated in the switch.

High d $v / d t$ across the switch couples energy through the Miller capacitor into the gate drive circuit causing ringing, thus the drive circuit needs to be designed. with a low impedance to reduce ringing.

The zero current quasi resonant switch is not suitable for frequencies of operation greater than a few MHz (depending on the device) since parasitic elements (such as $C_{0 u 1}$ ) of the switching device are not incorporated into the resonating components, producing losses at higher frequencies. This limits the operating frequency to about 2 MHz (Tabisz et al. 1988).

In its mode of operation it is primarily designed to work into a constant current carrying inductor and is not specifically designed to give the high frequency a.c. outputs required in electro-process heating applications.

The diodes chosen to provide reverse blocking or reverse conducting capability must have both fast forward and reverse recovery. This again limits high power, high frequency operation due to the availability of suitable high voltage, fast recovery diodes. GaAs and Schotky diodes are limited, at present, to a 200 V breakdown capability.

Circuit design is not entirely empirical and there are no general equations giving the required inductive and capacitive elements directly (Liu et al. 1985, Jovanovic et al. 1987).

### 3.1.4.2 Zero Voltage Switch Quasi Resonant Converters (ZVSQRV)

The zero voltage quasi resonant switch (ZVQRS) minimises high $\mathrm{d} v / \mathrm{d} t$ by ensuring that the transistor switches at zero voltage. Applying the principles of duality, the current is a square wave and voltage a half sinusoid as shown in Figure 3.9 (Lee 1987).


Figure 3.9 Zero Voltage Quasi Resonant Switch and Waveforms.
(a) General topology
(b) Half-wave
(c) Full-wave

Considering the half wave ZVQRS, the diode and capacitor are in built, thus neither $\mathrm{d} v / \mathrm{d} t$ nor $\mathrm{d} / \mathrm{d} t$ are present. In this configuration the body diode is allowed time to recover since current is commutated from the diode to the switch. Also the parasitic components of the switch are incorporated into the resonant elements. Thus high frequency operation incorporating the body diode is possible (Tabisz et al. 1988).

With the ZVQRS, the allowable range of load variation is from no load to full load. Beyond full designed load, quasi resonant switch operation is lost. Thus unlimited open circuit loading can be tolerated, duality applies such that the zero current switch can handle unlimited load short circuit.

The ZVQRS can be applied to any PWM converter (given the proviso that it switches into a capacitor carrying constant voltage) but the zero current switch is generally more attractive since there is lower voltage stress with ZCQR over ZVQR. Finally, the zero voltage switch generally has cleaner waveforms than the zero current switch.

The principal disadvantages of the ZVQRS for high frequency electric process heating supplies are similar to those of the zero current quasi resonant switch:

In its mode of operation it is primarily designed to work into a constant voltage capacitor and is not specifically designed to.give the high frequency a.c. outputs required in electric process heating applications.

The diodes chosen to provide reverse blocking or reverse conducting capability must have both fast forward and reverse recovery.

Circuit design is not entirely empirical and there are no general equations giving the required inductive and capacitive elements directly (Liu et al. 1985, Jovanovic et al. 1987).

The ZVQRS produces voltage amplification and the voltage impressed across the switch can be many times the supply voltage.

### 3.2 Class E Amplifiers

The Class E amplifier was developed by the Sokals in the mid 1970's for use in light weight, low power, high efficiency power converters and RF amplifiers (Sokal et al. 1975a, Sokal et al. 1975b).

By the method of operation, the Class E amplifier eliminates the simultaneous high voltage and current stress on the active device during switching transitions by shaping the device current and voltage waveform. This waveform shaping is achieved by a series inductor-capacitor network whose resonant frequency is slightly lower than the operating frequency of the inverter.

The major cause of inefficiency in power converters, inverters and amplifiers is the power loss in the active output device(s). To reduce this dissipation it is necessary to minimise:

1) the voltage across the device when current flows through it (i.e. its saturation voltage);
2) the current through the device when the voltage exists across it (i.e. its leakage current); and
3) the unavoidable duration when appreciable current and voltage exists simultaneously (i.e. during the switching transition).

Most switching converters achieve 1) and 2) by suitable selection of devices with low saturation voltage and low leakage current. The switching loss (type 3 loss) is usually minimised by ensuring that the switching interval is only a small fraction of the switching period. Thus as switching frequency increases, type 3 losses become dominant.


Figure 3.10 Basic Class E Amplifier Circuit and Ideal Waveforms.
The Class E amplifier attempts to overcome this. The basic circuit is shown above in figure 3.10 along with ideal and actual waveforms. As can be seen, the following conditions are met by the Class E waveforms:

1) \& 2) Conditions 1) and 2): described above, are met by the choice of switch and drive circuit and are substantially independent of the load network.
2) The switching time of the switch is minimised: this again is fulfilled by correct choice of active device and proper design of driver. This condition is partially dependent on the load network, particularly in terms of turn off time (since the charging current for the active device's output capacitance is obtained through
the load). The load network of the Class E amplifier is said to aid switching speed (Sokal et al. 1979). The load network is arranged to have an input step response as described below:
3) Voltage delay at switch turn off: in the interval during which the switch makes its transition from the on to the off state, the voltage across the switch remains low for a time period long enough such that the current through the switch reduces to zero, the switch voltage then increases, ensuring that high voltage does not exist across the switch while the current through it is non-zero.
4) Voltage return to zero at switch turn on: during the 'off' state, the load network input-port transient response carries the voltage across the switch first upwards and then down back towards zero; thus the switch voltage reaches zero just prior to the start of the switch 'on' state, i.e. just before current starts to flow.
5) Zero voltage slope at switch turn on: when the 'off' state transient response reaches zero voltage across the switch, i.e. just before the beginning of the 'on' state, it does so with approximately zero slope. This allows some tolerance in the operating point (frequency, duty ratio) of the amplifier. Also, in view of limited di/dt capabilities of switching devices, this zero starting current is desirable because it helps to minimise switch turn on time.

Thus, in short, the Class E amplifier eliminates simultaneous voltage and current stress (since the voltage across the switch only rises after the current through it has fallen to zero, and the current through the switch only rises after the voltage across it has fallen to zero) and, unlike conventional sinewave resonant converters, has a tailored response which allows deviation from the optimum operating frequency without impinging efficiency.

Hence the main advantages are high efficiency, high frequency capability and therefore small size. The main use of the Class E amplifier has been in low power (i.e. a few tens of watts) d.c.-d.c. converters and in high efficiency HF amplifiers. The Class E amplifier has further advantages over traditional linear amplifiers (Class B, Class C) in that it is largely insensitive to component tolerances, particulariy the active switching element characteristics (Sokal et al. 1979 Raab et al. 1978), also the circuit operation is well defined and predictable (Kazimierczuk 1983a, 1983b, Redl et al. 1983, 1984, Kazimierczuk 1984). Thus reliable circuits can easily be designed and built without having to resort to the empirical, heuristic techniques often associated with Class A, B or Class C amplifiers.

There are, however, a number of fundamental disadvantages associated with the ClassE amplifier. Although the switching element is not subject to simultaneous high current and high voltage stress, it is subjected to current and voltage stresses considerably higher than those which occur in conventional switch-mode resonant inverters.

The maximum voltage ( $v_{\text {s(max }}$ ) impressed across the switch in relation to the supply voltage can be extremely high in Class E circuits. In the case of optimum operation it has been shown (Kazimierczuk 1983b, Kazimierczuk 1984, Redl 1983) that:

$$
\begin{equation*}
v_{t(\max )}=3.56 \mathrm{~V}_{d d} \tag{3.4}
\end{equation*}
$$

Where: $\quad$\begin{tabular}{ll}

$V_{d d}$ \& | is the drain supply voltage; and |
| :--- |
| $\left.v_{\alpha \text { max }}\right)$ | <br>

\& | is the maximum voltage impressed |
| :--- |
| across the switch. |

\end{tabular}.

However $v_{\text {smax) }}$ can easily reach values greater than $4.5 V_{d d}$ when operation is sub optimal (either unintentional due to circuit load mismatch, or intentionally for voltage/power control purposes). Further, when conducting, the current through the switch can be as high as three times the supply current $I_{d d r}$. Thus, assuming $90 \%$ efficiency, a Class E amplifier capable of delivering 500 W must use a switch capable of handling 11 kVA .

However, according to Raab (Raab 1977), if the operating point is slightly outside the region of ideal operation then the voltage and current stresses at full load are slightly below those which occur when operating optimally. Also, if the switching device has good peak current (or voltage) to continuous current (or voltage) capabilities then the ratio of delivered power to VA capability can be improved.

A further disadvantage is that the Class E amplifier has little tolerance to excessive load mismatch and or reactance. If off nominal loads must be accommodated, a load resistance lower than nominal is safe (although efficiency becomes poor) but a load resistance much higher than nominal is potentially dangerous. The reason being that the higher than normal load resistance results in a loaded $Q$ lower than the design value. The switching element will then dissipate power of $1 / 2 C_{1} V^{2} f_{s}$ where $V$ is the voltage across the switch and the shunt capacitor, $C_{1}$, at the turn on instant (Sokal 1985).

The upper limit on operating frequency is not only that imposed by the switching speed of the active device but also that imposed by its output capacitance since this, in the limit and in association with the parasitic capacitance of the RF choke, sets the minimum value for $C_{1}$. With high power devices, this minimum value could exceed the optimum required in the load network.

Thus the class E amplifier is capable of high frequency operation but until recently this has only been shown at low power levels.

There are several circuit configurations which employ Class E operation other than the one originally devised by the Sokals (Raab 1977). Two of these are described briefly below:

## a) Push-Pull Class E

The push-pull configuration (Figure 3.11) allows the combination of two Class E amplifiers, working in anti-phase, to increase the output power. As with any push pull amplifier, the two devices are driven alternately, each side operating as though it was a single transistor Class E amplifier.


Figure 3.11 Push-Puil Class E Amplifier Circuit.

When a given transistor is driven on, it provides a ground connection to the primary of the output transformer, causing the d.c. input current and the transformed sinusoidal output current to charge the capacitor shunting the output transistor.

The voltage appearing on the secondary winding of the output transformer contains both a positive and a negative Class E shape.

## b) Parallel-Tuned Amplifier With Series Inductor

A parallel-tuned Class E amplifier employing a series inductor as storage element is shown in Figure 3.12. As with the series tuned amplifier, the series inductor could be discrete, or could be incorporated as the leakage inductance of the transformer.


Figure 3.12 Parallel Tuned Class E Amplifier Circuit.
This configuration is the dual of the series-tuned amplifier (Figure 3.10) in that the current and voltage roles are reversed. As a consequence of the duality, the net effect of the parallel-tuned circuit on the fundamental frequency must be a capacitive susceptance for optimum operation, as opposed to inductive for the series tuned circuit.

The power and frequencies achieved by other authors to date using the class E amplifier configuration are given below:
a class E amplifier has been reported capable of running off 240 V mains employing a bipolar MOSFET combination cascode switch delivering 21 W with an operating frequency of 500 kHz (Latteke et al. 1985);
a 14 MHz 100 W Class E d.c.d.c. converter using a standard power MOSFET and giving 20 V at 5 A has been reported (Redl et al. 1986);
a resonant d.c.-d.c. converter producing 50 W operating at 22 MHz using surface mount technology and Class E principles has been reported (Bowman et al. 1988).

Higher operating frequencies have been reported but at much reduced power levels. None of the above are of sufficient power capability to be useful as electric process heating power sources, but clearly the Class E amplifier has potential for use in such applications.

### 3.3 RF Power_Amplifiers

It has been stated previously that conventional switched mode power supplies are only capable of high power operation (i.e. greater than a few hundred watts) at frequency levels up to the low MHz region both due to device and circuit topology limitations.

An alternative to the switched mode supply is the linear amplifier operating in Class $\mathrm{A}, \mathrm{AB}, \mathrm{B}$ or C modes. These circuit configurations are well known and documented, particularly in the communications field (Gottlieb 1982). However it is worth while reviewing the technology, particularly in the light of advances in solid state RF devices.

The traditional active component in linear amplifiers has, until the mid 1970's, been the thermionic valve (commonly called simply a tube, or valve). And, certainly, in most high power amplifiers (of 500 W or more) it is still predominantly used, particularly in non portable equipment, for a number of reasons (M-O Valve Co. 1981).

1) It generates a lower proportion of harmonic output. This is particularly true with respect to a bipolar transistor, less so with a field effect device.
2) Intermodulation distortion (IMD) products are less.
3) Although valves deteriorate more rapidly with use than transistors and thus can be expected to have a shorter working life, a valve will usually survive harsher maltreatment such as load short or open circuits.
4) Glass envelope valves have a particular advantage concerned with cooling. Transistors need to be conduction cooled and, often, the heat sinks required can be bulkier than an equivalently rated valve.
5) In the event of failure, a valve is often easier to replace.
6) Generally more simple circuit construction.
7) Finally, thermionic valves are less expensive, watt for watt, than solid state RF devices, particularly in the HF band ( $3-30 \mathrm{MHz}$ ).

The main disadvantages of the valve over the transistor are:

1) It is a more bulky component;
2) it is less able to withstand mechanical shock;
3) it requires the use of an HT supply and separate cathode heater supplies.

Hence, for portable equipment, solid state devices are preferable.
Supplies for dielectric heating applications predominantly use valves as the active device, operating in Class C mode as part of a Colpitt's oscillator. In plastic welders operating at 27.12 MHz the resonant network is often in the form of a distributed tank circuit or cavity resonance chamber, this has the advantage of providing a very high $Q$. Further, since the operating voltage is high, current flowing in the tuned circuit is relatively low, thus the cavity undergos little thermal expansion due to $I^{2} R$ losses and hence exhibits a stable resonant frequency.

Because solid state RF devices have low operating voltages (a maximum of 50 V for BJTs and exceptionally 100 V for FETs), currents have to be higher in order to achieve appreciable power levels. This results in a number of limitations when trying to apply the same technology employed with valve electric process heating supplies to solid state supplies.

1) Because of large current levels, $L \mathrm{~d} / / \mathrm{dt}$ effects are more dominant thus layout becomes more critical.
2) High currents cause increased $I^{2} R$ losses in resonant components of the oscillator, thus even if the oscillator circuit has a high $Q$, frequency stability will be poor due to thermal expansion and contraction of resonating components.
3) Variations in load parameters have a greater affect on the resonant frequency of a low $Q$ circuit and hence are of greater concern in transistorised oscillators.

Thus when employing solid state devices, it is more reasonable to utilise the classical, communications approach of a stable low power oscillator feeding into a power amplifier, either constructed as a single unit, for power levels up to 300 W, (Goutlieb 1982, Granberg 1976, Granberg 1975) or multiple units combined to achieve the required power levels. Amplifiers capable of delivering up to 2 kW of RF power have been constructed using this technique (Granberg 1983, Granberg 1976).


Figure 3.13 300 W 3-30 MHz FET Amplifier.
The circuit of a basic FET 300 W amplifier module is shown above in Figure 3.13, there are a number of advantages of field effect devices over bipolar which have been detailed in the previous chapter, however a brief summary is given below:

1) More tolerant to load mismatch;
2) simplified circuit design and biasing;
3) easier to broad band due to higher input impedance;
4) gain can be easily controlled by adjusting bias voltage;
5) slightly higher power gain. The difference in gain at 30 MHz is between 3-6 dB.

The second most important feature is item 4). In a common source circuit configuration the power gain can be controlled by 20 dB or more. This control helps to ease protection of the devices in the case of excessive load mismatch. The control signal for overload 'shut down' can easily be derived from a reflectometer in the amplifier output.

A block diagram of a basic 1 kW amplifier is shown in Figure 3.14. Here, two main modules, each consisting of four push pull amplifiers (Figure 3.13), are combined to produce the full ouput power of 1600 W using 16 MRF 150 's (the total cost of the active devices being around $£ 2200$ at 1988 prices).


Figure 3.14 Block Diagram of $\mathbf{1} \mathbf{~ k W}$ HF Amplifier.
Because the combined power dissipation of the devices is of the order of 600 to 800 W in a confined area, heat dissipation is a problem. Copper heat spreaders along with forced air cooling are required to enhance utilisation of the heat sinks.

Bias regulation is required because, although the $R_{\text {ddoce })}$ resistance of RF MOSFETs has a positive temperature coefficient (above a certain quiescent current level) which enhances thermal stability, at low to medium quiescent current levels the gate voltage required to maintain a set idling current falls with
temperature (Figure 3.15). Temperature compensation can be provided by a thermistor, thermally connected to the heat sink, which forms part of the resistor divider network associated with the voltage regulator. Thus idle current in the FETs is thermally stabilised by closed loop control of the gate bias voltage. With bipolar devices this is normally done with forward biased diodes where the diode voltage drop with respect to temperature closely follows that of the base emitter junction.


Figure 3.15 Gate-source Voltage Versus Case Temperature of Typical Power RF MOSFET.
With reference to Figure 3.13, $\mathrm{Q}_{1}$ and $\mathrm{Q}_{2}$ are operated in common source configuration (cf. common emitter for the BJT and common cathode for thermionic valves). Since the gate is almost purely capacitive with respect to the source, the input $Q$ is high and must be lowered to achieve stability. This is done with $R_{1}, R_{2}$ and $C_{10}$ in conjunction with the negative feedback derived from $\mathrm{T}_{2} . \mathrm{T}_{3}$ is required to match the output impedance of the transistors to the input impedance of the power combiner (Figure 3.16) and is calculated as:

$$
\begin{equation*}
R=2 \frac{\left[V_{d u}-V_{d t(a)}\right]^{2}}{P_{0}} \tag{3.5}
\end{equation*}
$$

Where:

$$
p_{\text {Pum }}
$$

is the expected output power is the device on voltage and is calculated from:

$$
\begin{equation*}
V_{d(m)}=R_{d d(m)} \times I_{d(m a)} \tag{3.6}
\end{equation*}
$$



FIG. (a) FOUR PORT POWER DIVIDER


FIG. (b) FOUR PORT OUTPUT COMBINER

Figure 3.16 RF Amplifier Power Combiner/Divider.
The power combiner is constructed in a similar manner to the input power splitter and consists of straight pieces of coaxial cable loaded by a sleeve of ferrite. The purpose of the balancing resistors $(R)$ is to dissipate any power if the VSWR increases (i.e. should one of the power modules fail).

It is possible to generate upwards of 600 W without the use of power combiners by directly paralleling power RF MOSFETs in Class AB amplifiers (Granberg 1983). A circuit designed by H.O. Granberg of Motorola uses two paralleled pairs of power MOSFETs. In the circuit, drain and source connections are paralleled, each gate is biased by a separate supply, the bias voltage being set by trimmer resistors to compensate for differences in gate thresholds. However, the devices still have to be matched for near equivalent transconductance. The technique used is considered impractical for bipolar devices because of their low input impedance; in a common source configuration, an RF power MOSFET has between 5 and 10 times higher input impedance than a comparable bipolar transistor, operated in a common emitter circuit.

The limitation on the number of FETs that can be paralleled is dictated by physical rather than electrical considerations, although the mutual inductance between drain connections is the most critical aspect and limits the upper frequency range of operation. These problems could be partially overcome by use of multiple die packages. Alternatively, for higher frequency narrow band circuits, mutual inductance could be incorporated into the output matching network.

A further problem associated with paralleling devices is that, if the unity gain frequency of the device is sufficiently high, potentially damaging oscillation can occur between paralleling inductances and gate and drain capacitances. However, the problem can be overcome by the use of low value ( $a 1.0 \Omega$ ) non inductive resistors to isolate paralleling inductances from the gate. The stability of the amplifier is claimed to be good even when tested with a $30: 1$ load impedance mismatch at all phase angles.

All the amplifiers mentioned previously are operated in Class AB or Class B mode, maximum efficiency being less than $65 \%$. A better approach for dielectric heating applications would be to operate the transistors in a Class C mode.

Further, there is a distinct advantage in using push-pull circuits with isolating input baluns, apart from the obvious advantage of greater power output, the circuit avoids RF current loops being set up through the ground potential. A typical 60 W push-pull broad band Class C amplifier circuit is shown in Figure 3.17. Here conversion efficiency is claimed to be about $73 \%$ (DeMaw 1982a). The transistors are biased slightly beyond their threshold level, to aid amplifier gain.


Figure 3.1760 W Push-pull Broad Band Amplifier.
All the circuits mentioned above are intended for broad band operation in the HF range, typically 3 to 30 MHz . Broadband capability is not a requirement of a dielectric heating power source. Thus narrow band amplifiers would be a better choice. Since impedance matching networks can be used at the output rather than broad band transformers, efficiency is substantially improved (Becciolini 1978, DeMaw 1982b, Zarrel 1983).

At higher frequencies, for example in the upper VHF band ( $100-300 \mathrm{MHz}$ ), transmission line matching techniques can be used. Indeed for the high power VHF transistor such as the DVD150T, capable of 150 W output and operating from a 100 V rail, the full performance potential can only be realised by use of such techniques. The efficiency of an output matching transformer and balun is only about $80 \%$, whereas the efficiency of a transmission line matching network is limited only by the insertion loss of the
coaxial cable used. Similarly, toroidal baluns are limited to matching impedance ratios of specific integer values such as $1: 1$ and 4:1, the coaxial balun, however, can be used to match any two impedance values if the characteristic coaxial impedance is chosen correctly.

The characteristic impedance of a quarter-wave transmission line transformer is given by the formula:

$$
\begin{equation*}
Z_{\text {line }}=\sqrt{Z_{m o w t} Z_{o w t}} \tag{3.7}
\end{equation*}
$$

Where: $\quad Z_{i s} \quad$ is the impedance seen by the input of the balun and
$Z_{\text {ous }} \quad$ is the impedance seen by the output.

Figure 3.18 shows a practical circuit using a pair of DVD 150T's, designed to operate in Class B or C mode (depending on the bias voltage) capable of delivering 300 W at 175 MHz .


Figure 3.18 Output Stage of 146 MHz 300 W Amplifier Employing Transmission Line Output Matching.

## $3.4 \quad$ Conclusions

There are no switched-mode topologies capable of delivering appreciable power levels greater than 1 kW at switching frequencies above a few MHz . Of the circuits employing switched mode operation, the most suitable for high frequency switching is the Class E amplifier which offers slightly higher efficiency and, since switching losses are low, slightly higher operating frequency than the Class D amplifier.

One of the major drawbacks of the Class E amplifier is that it is not a very efficient user of device switching power capability in that the device must be able to withstand up to 4-5 times the supply voltage and approximately 3 times the supply current.

An alternative method for obtaining high power levels using solid state devices at dielectric heating frequencies is to use linear amplifiers. In terms of efficiency, Class B or Class C would be the best choice. Since dielectric heaters operated at a specified frequency, narrow band amplifiers would be most applicable.

To conclude, there is no viable, solid state alternative to the thermionic valve at present for high power (greater than 1 kW ) HF electric process heating applications. Solid state devices could be used on smaller scale plastic welders where ease of carriage is an advantage. However, when using resonant topologies such as the Class E amplifier, the switching frequency of standard power MOSFETs can be increased to the low MHz region at power levels useful to high frequency induction heating applications.

## Chapter 4

## PRELIMINARY PRACTICAL INVESTIGATIONS

Investigations into the suitability of RF linear amplifiers and Class E inverters for the generation of high frequency $(3-30 \mathrm{MHz})$ power for electric process heating applications are reported.

## PRELIMINARYPRACTICAL INVESTIGATIONS

The conclusions of a detailed review of relevant literature (Hinchliffe et al. 1986a-c) reported in the previous chapters, and earlier work which had been undertaken at Loughborough University on conventional, voltage and current fed, solid state medium frequency ( $100-400 \mathrm{kHz}$ ) induction heating supplies (Hinchliffe 1983, Tebb 1986, Hinchliffe et al. 1987a-b,1988a) has suggested that standard resonant power sources have an upper frequency limit of about 1 MHz . The main limitation being increased switching loss at higher frequencies.

Thus the conclusions of the review and of previous work are that the most suitable active devices for operation in the MHz region are the power MOSFET and the RF power MOSFET. The most applicable circuits for generation of RF power are the Class C amplifier and the Class E inverter.

The following details practical investigations into the suitability of the Class C amplifier and the Class E inverter for the generation of RF power for use in high frequency electric process heating applications.

### 4.1 The Class C Amplifier

With the recent commercial availability of high power ( 600 W ) RF power MOSFETs, it was considered that large scale, solid state, linear amplifiers could be applied to dielectric heating applications. To investigate the techniques involved in linear amplifier design and to assess their suitability as dielectric heating power sources, a $300 \mathrm{~W}, 27.12 \mathrm{MHz}$ Class C power amplifier was designed and constructed. A block diagram of the generator, which consists of two power amplifiers connected in cascade, is shown in Figure 4.1.


Figure 4.1 Block Diagram of Linear Amplifier.

The RF signal input is generated by a crystal oscillator which, after a power boost by a buffer amplifier, is used to drive a Class AB push-pull amplifier. The output of this pre-amplifier is then coupled to a Class C amplifier, also in push-pull configuration, which converts the 50 volt d.c. supply into a $300 \mathrm{~W}, 27.12 \mathrm{MHz}$ RF power output suitable for dielectric heating applications ( Ng 1986, Hinchliffe et al. 1987c, 1987d).

### 4.1.1 Amplifier Circuit Description

The pre-amplifier and output power amplifier are Class AB and Class C push-pull amplifiers respectively. However, both amplifiers have a common circuit design and layout. The use of a common approach in design allows the mode of operation of a circuit module to be changed conveniently by varying, say, the bias voltage, power supply, active device and/or the output impedance matching transformer whilst maintaining other parameters constant. The circuit diagram of one of the two push-pull amplifiers, i.e. the building block of this system is shown in Figure 4.2.


Figure 4.2 Circuit Diagram of Linear Amplifier.
The signal source impedance of $50 \Omega$ is matched to the input impedance of the amplifier by a broad band input transformer $T_{1}$ which is coupled to the gates of transistors $Q_{1}$ and $Q_{2}$ by two d.c. blocking capacitors $C_{2}$ and $C_{3}$ as shown.

Power RF MOSFETs $Q_{1}$ and $Q_{2}$ form the basis of the amplifier module and are connected in common source configuration. Their individual, but equal, gate bias voltages are set by the biasing network resistors; $R_{5}, R_{8}, R_{9}, R_{10}$ and $R_{11}$ in association with the bias voltage regulator $\mathrm{IC}_{1}$. Diode $\mathrm{D}_{2}$ is present to protect the regulator against damage due to over-voltage in case of a drain-to-gate short in either $Q_{1}$ or $Q_{2}$. $C_{1}$ provides a bias adjustment of $0.5 \mathrm{~V}-9 \mathrm{~V}$ with the variable resistor $R_{3}$ and thermistor $R_{4}$. The thermistor, which has a negative temperature coefficient and is mounted on the transistor heat sink, is used for temperature compensation of the amplifier. Temperature compensation is required since, for a given gate bias voltage, quiescent drain current increases with temperature (the reader is referred to Figure 3.15 Section 3.3). The d.c. supply is fed to the drains of $Q_{1}$ and $Q_{2}$ via transformer $T_{2}$ and two separate $R F$ chokes $L_{1}$ and $L_{2}$. Under normal operation transformer $T_{2}$ provides a centre tap for the output transformer $\mathrm{T}_{3}$ and a degree of impedance transformation (Krauss et al. 1980). Capacitors $C_{5}$ and $C_{6}$ provide a d.c. block to the output transformer. The currents for each half cycle (with a conduction angle of less than $180^{\circ}$ in Class C mode) are in opposite phase in 'ac' and 'bd' of $\mathrm{T}_{2}$; and, depending upon the coupling factor between the windings, the even harmonics will see a much lower impedance than the useful fundamental component. The optimum line impedance for 'ac', 'bd' is equal to the drain-to-drain impedance of the transistors.

The output of the power amplifier is coupled to the load by broadband transformer $T_{3}$. This transformer is used to match the drain-to-drain output impedance with the load impedance. In the case of the Class $A B$ amplifier operating close to Class $A$, load line considerations yield the drain to source output resistance, $R$, to be given by (Krauss 1980, DeMaw 1982a, 1982b, Ng 1986):

$$
\begin{equation*}
R=\frac{V_{d u}^{2}}{P_{o}} \tag{4.1}
\end{equation*}
$$

The drain-to-drain resistance, $R_{o}$, is twice the value of $R$, therefore,

$$
\begin{equation*}
R_{o}=2 \frac{V_{d t}^{2}}{P_{0}} \tag{4.2}
\end{equation*}
$$

Taking into account the saturation voltage, $V_{\text {dros }}$, in the drain channel,

$$
\begin{equation*}
R_{0}=2 \frac{\left.\left(V_{d d}-V_{d(a n}\right)\right)^{2}}{P_{0}} \tag{4.3}
\end{equation*}
$$

Likewise, load line considerations for Class $C$ operation yields the resistance $R$ to be given by:

$$
\begin{equation*}
R=\frac{V_{d u}^{2}}{2 P_{0}} \tag{4.4}
\end{equation*}
$$

and:

$$
\begin{equation*}
R_{0}=\frac{V_{d d}^{2}}{P_{0}} \tag{4.5}
\end{equation*}
$$

Presence of drain saturation voltage gives:

$$
\begin{equation*}
R_{0}=\frac{\left.\left(V_{d u}-V_{d s(o n}\right)\right)^{2}}{P_{0}} \tag{4.6}
\end{equation*}
$$

Given that the load resistance is $R_{L}$, then the transformer required to match the output impedance of the transistor stage to the load impedance of $50 \Omega$ has a turns ratio, $\mathrm{N}_{2} / \mathrm{N}_{1}$, given by:

$$
\begin{equation*}
\frac{\mathrm{N}_{2}}{\mathrm{~N}_{1}}=\sqrt{\frac{R_{L}}{R_{o}}} \tag{4.7}
\end{equation*}
$$

The lower frequency -3 dB point (or lower bandwidth point) of the transformer is determined by the magnetising inductance of the transformer, the upper frequency -3 dB point being determined by the cut off frequency of the ferrite and inter-winding capacitance in association with leakage inductance. There is a trade-off between high efficiency at high frequency (lower for less primary turns) and low minimum operating frequency (lowest for more primary turns). Transformer $\mathrm{T}_{3}$ is a.c. coupled to the power transistors by d.c. blocking capacitors $C_{7}, C_{8}, C_{9}$ and $C_{10}$.

One of the main problems encountered with the construction of the RF amplifiers was the sourcing and procurement of suitable parts, many of the more expensive, specialised parts such as the power devices, ferrites and high voltage chip capacitors were obtained as engineering samples. Thus to aid any who may wish to repeat the work described here, a complete component listing is provided in Table 4.1.

Component values for the Class AB amplifier follow exactly that for the Class C power amplifier listed in Table 4.2 except for transistors $\mathrm{Q}_{1}, \mathrm{Q}_{2}$, the ouput transformer $\mathrm{T}_{3}$ and the output socket $\mathrm{SK}_{2}$ which are given in Table 4.2. The Class AB amplifier was designed to be capable of producing 30 W such that, ultimately, it could be used to drive several 300 W Class C modules operated in parallel as described in Chapter 3, Section 3.3.

| Component List For Class 4.1 C Power Amplifier. |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Description |  |  |  | Quantity | Comments |
| Voltage Regulator | MC1723CP |  |  | 1 | IC1 |
| Resistors: | 910R | 0.4W | metal film | 1 | R1 |
|  | 10R | 0.4W | metal film | 1 | R2 |
|  | 10k | preset p | potentiometer | 2 | R3, R5 |
|  | 10k | NTC th | hermistor | 1 | R4 |
|  | 2 k 0 | 0.4W | metal film | 3 | R6, R10, R11 |
|  | 10k | 0.4W | metal film | 1 | $R 7$ |
|  | 100R | 0.4W | metal film | 2 | R8, R9 |
| Capacitors: | 1000 pF | 200 V | ceramic disk | 1 | C1 |
|  | $0.1 \mu \mathrm{~F}$ | 200 V | ceramic chip (AVX) | 6 | C2-3,C7-10 |
|  | 470, F | 25 V | electrolytic | 1 | C4 |
|  | $0.33 \mu \mathrm{~F}$ | - | ceramic chip (AVX) | 2 | C5, C6 |
|  | $10 \mu \mathrm{~F}$ |  | electrolytic | 1 | C11 |
| Inductors: | $2 \mu \mathrm{H}$ Fair-Right 2673021801 |  |  | 2 | L1, L2 |
| Transistors: | MRF150 Motorola TMOS |  |  | 2 | Q1, Q2 |
| Transformers: | Stackpole Core 57-1845 <br> Primary: eturss 26 SWG <br> enamelled copper wire <br> Secondary:  <br> 1turn 3 mm copper  <br> braid  |  |  | 1 | T1 |
|  | Stackpole Core 57-9322 <br> 2 turns twisted-wire pair 22 <br> SWG enamelled copper wire |  |  | 1 | T2 |
|  | Stackpole Core $57-3228$  <br> (2 paralleled). 1 turn 6 mm copper <br> Primary: 1 braid <br> Secondary: <br> 2 <br>  turns 20 SWG <br> enamelled copper wire |  |  |  | T3 |
| Heat sink: | $0.4{ }^{\circ} \mathrm{C} / \mathrm{W}$ |  |  | 1 |  |
| Connectors: | $50 \Omega \mathrm{BNC}$ |  |  | 1 | SK1 |
|  | $50 \Omega \mathrm{~N}$ type |  |  | 1 | SK2 |


| Table 4.2Component List For Class AB Pre-amplifier. |  |  |  |
| :---: | :---: | :---: | :---: |
|  | Description | Quantity | Comments |
| As per Table 4.1 except: |  |  |  |
| Transistors: | MRF148 Motorola TMOS | 2 | Q1, Q2 |
| Transformers: | Stackpole Core $57-1845$Primary: $\quad$t turn 3 mm <br> copper braid <br> Secondary: <br> 1 tum 26 SWG <br> enamelled copper wire | 1 | T3 |
| Connectors: | $50 \Omega \mathrm{BNC}$ | 1 | SK2 |

### 4.1.2 Crystal Oscillator

A third overtone crystal oscillator was designed together with an RF buffer amplifier to provide the required, precise driving frequency of $27.12 \mathrm{MHz} \pm 0.6 \%$, and is shown in Figure 4.3. The crystal, $\mathrm{X}_{1}$, when operated at its third overtone of the fundamental and in parallel mode ${ }^{3}$, is equivalent to the combination of $L_{1}$ and $C_{2}$ in the resonant circuit shown at the drain output of transistor $Q_{1}$. The desired frequency generated by $\mathrm{X}_{1}$ is amplified by $\mathrm{Q}_{1}$. The tuned tank circuit comprising of $L_{1}, C_{2}$ serves as a feedback network and improves frequency stability. In theory, the frequency at the drain will be the third overtone of $\mathrm{X}_{1}$. In practice, however, to achieve the best stability for the crystal oscillator, the operation should be slightly above the resonant frequency (DeMaw 1982b).


Figure 4.3 Crystal Oscillator Used in Linear Amplifier.

3 Above 20 MHz it becomes expensive to fabricate fundamental mode crystals, so overtone modes are used. In practise, cost limitations restrict the designer to the use of third or fifth overtone crystals.

Resistor, $R_{4}$, in conjunction with decoupling capacitor, $C_{3}$, serves to prevent $R F$ energy from being fed back into the supply. $R_{1}, R_{2}$ and $R_{3}$ are d.c. biasing resistors for $\mathrm{Q}_{1}$ and $\mathrm{Q}_{2} . C_{1}$ acts to decouple RF and stabilize $Q_{2}$ 's gate d.c. voltage level. Capacitor $C_{4}$ couples the oscillator frequency to the input port of the buffer amplifier. The power developed at the output of the tuned circuit is small. Thus an RF buffer amplifier, consisting of transistor $Q_{2}$ operated in common-source configuration, is required to provide enough drive for the power pre-amplifier, this also serves to enhance the frequency stability of the oscillator. The amplified output is extracted from the drain of $Q_{2}$ by means of the un-tuned transformer $T_{1}$.

For minimum distortion of waveform, the amplifier gain is set at its minimum possible value. Minimum gain is dependant upon the transconductance of $Q_{2}$ and the impedances present at the gate of $Q_{1}$ and the drain ports. Transconductance is controlled by the bias voltage at the gate of $\mathrm{Q}_{2}$. By varying the potential at this point, a typical maximum gain of 25 to 30 dB might be obtained. The decoupling network of $R_{5}$ and $C_{7}$ heips to stabilise the d.c. potential at the drain of $\mathrm{Q}_{2}, R_{6}$ and $C_{8}$ fix and stabilise the source d.c. potential.

### 4.1.3 Construction and Testing

For the pre-amplifier and main power amplifier (Figure 4.2), careful construction of the input, ouput and interphase transformers is required to minimise non-linearities or distortions and to ensure adequate high frequency performance. The construction method for transformers $T_{1}$ and $T_{3}$ is shown in Figure 4.4. The ferrites used are of a 'balun' type (Granberg 1980). Transformer $\mathrm{T}_{1}\left(\mathrm{~T}_{3}\right)$ has a single turn secondary (primary) consisting of $3 \mathrm{~mm}(6 \mathrm{~mm})$ tinned copper braid formed into a tube. Through the middle of this winding runs the single (double) turn primary (secondary). This coaxial construction of primary and secondary windings ensures close coupling and minimises leakage inductance. The interphase transformer consists of a two turns of twisted pair ( 22 SWG) wound on a ferrite toroid. Before mounting the transformers, their HF performance and transformer ratio was checked by means of a Hewlett Packard Impedance Analyser, the -3 dB bandwidth for all the transformers being approximately 3 to 33 MHz .

The double sided PCB artwork used is based on a Motorola design for a Class AB amplifier module (Granberg 1972). A large RF ground plane is provided to discourage local fields. The heat sink is also solidly earthed. The final pre and power amplifier modules are shown in Figure 4.5.

Initially, each amplifier module was tested in isolation, with the crystal oscillator being replaced by a laboratory RF oscillator and RF amplifier. A high frequency oscilloscope was used to monitor waveforms at various parts of the circuit, input and output power and VSWR was measured by means of a Bird ${ }^{4}$ through-line RF wattmeter. When the units were cascaded, a certain degree of instability was noticed in the Class C amplifier. Thus feedback was introduced in the form of $R_{b 1}, R_{b 2}$ and $L_{3}$ as shown in Figure 4.6. This also had the benefit of improving the input VSWR of the power amplifier, thus minimising reflections and reducing harmonics.

[^2]

Figure 4.4 RF Transformer Construction.


Figure 4.5 Class AB and Class C Amplifiers Connected in Cascade.

All tests were carried out at a frequency of 27.12 MHz with a d.c. supply of 50 V , the output power was effectively controlled by adjusting the amplitude of the input signal to the amplifier.

An expression for VSWR is given in equation 4.8.


Figure 4.6 RF Amplifier Feedback Circuit.

### 4.1.3.1 Class AB Amplifier

The Class AB amplifier was tested with a transistor drain quiescent current $I_{d 4}$ of 1.5 A , the gate bias voltage being 4.5 V . VSWR measurements were carried out at both input and output port, with an output power of 30 W feeding a resistive load, for differing feedback resistance values. The effects of the feedback loop can be observed in Figure 4.7(a) and 4.7(b). Without feedback (Figure 4.7(a)), the input waveform is quite distorted compared with that with the feedback loop in place (Figure 4.7(b)). It should be added, though, that some of the distortion is introduced by the earth lead inductance of the oscilloscope probe (a better waveform monitoring technique would be to tap a fraction of the input or output power and
feed it via $50 \Omega$ cable to the $50 \Omega$ input of the oscilloscope, altematively, coaxial probe sockets could be used at the point of measurement). With the feedback in place the pre-amplifier had a measured power gain of approximately 12 dB .
(a)

## OUTPUT VOLTAGE 50V/DIV

15nS/DIV
infut voltage 20V/DIV


Figure 4.7 Class AB Amplifier Waveforms.

The input and output VSWR readings obtained for different feedback resistor values are summarised in Table 4.3. The optimum resistor values were discovered to be $18 \Omega$; giving an input and output VSWR of 1.16 and 1.06 respectively which is quite acceptable (a VSWR of 1.06 for an output power of 30 W represents a reflected power level of 0.025 W ), and $R_{b 1}, R_{b 2}$ were held at this value for all further tests. A small series inductance in the input and trimmer capacitance across the primary of $T_{1}$ reduced the VSWR at the input port still further to 1.12 (representing a reflected signal of $0.325 \%$ ).

| Table 4.3 <br> YSWR Measurements for Class AB Amplifiers |  |  |
| :---: | :---: | :---: |
| Feedback Resistance <br> $\Omega$ | Input VSWR <br> (unit less) | Output VSWR <br> (unit less) |
| 15 | 1.16 | 1.06 |
| 18 | 1.16 | 1.06 |
| 22 | 1.20 | 1.10 |
| 27 | 1.22 | 1.12 |
| 39 | 1.30 | 1.15 |
| 47 | 1.40 | 1.16 |
| $\infty$ | 1.80 | 1.21 |

### 4.1.3.2 Class C Amplifier Tests

All tests on the Class C amplifier were carried out with its drain supply voltage set to 50 V . Since, at high power output, the temperature of the ferrite cores used for transformers $T_{1}$ and $T_{3}$ can be high, measurements were taken for output power levels of 100 W , that is, below the 300 W design capability of the amplifier.

With the quiescent drain current set to 0.04 A , and the gate voltage at 3 V , the effects of the feedback loop on VSWR values were observed and are summarised in Table 4.4.

| VSWR Measurements for Class C Amplifier |  |  |
| :---: | :---: | :---: |
| Feedback Resistance <br> $\Omega$ | Input VSWR <br> (unit less) | Output VSWR <br> (unit less) |
| 15 | 1.20 | 1.06 |
| 18 | 1.20 | 1.06 |
| 22 | 1.20 | 1.06 |
| 27 | 1.45 | 1.09 |
| 39 | 1.50 | 1.10 |
| 47 | 1.7 | 1.10 |


(b)

OUTPUT VOLTAGE $50 \mathrm{~V} / \mathrm{DIV}$. 15nS/DIV.

INPUT VOLTAGE
20VIDIV.

(c)

OUTPUT VOLTAGE 50V/DIV.

15nS/DIV.
INPUT VOLTAGE 20V/DIV


Figure 4.8 Class C amplifier Waveforms.

Minimum input and output port VSWR was obtained for feedback resistance values of $22 \Omega$, thus resistors $R_{b 1}$ and $R_{b 2}$ were fixed at this value for subsequent measurement of circuit performance. The procedure used to determine input and output port impedance and VSWR showed that, again, the input port was capacitive. Again a small ferrite bead was inserted in series with the input transformer primary, reducing the input port VSWR to 1.16.

Figure 4.8(a) and 4.8(b) above shows the input and output waveforms of the amplifier for differing gate biasing potentials. When the amplifier is operated near to Class B (Figure 4.8(a)), the output power for a 4 W drive is 157 W , the power gain being 16 dB . With the amplifier biased deep into Class C mode, the input and output voltage waveforms are as shown in Figure $4.8(\mathrm{~b})$. Here a 9 W drive is required for a 175 W output, giving a power gain of 12.4 dB .

Finally, Figure 4.8(c) shows the input and output voltage waveforms of the Class C amplifier biased to the same condition as for Figure 4.8(b) but with the inclusion of a series inductance at the primary of transformer $\mathrm{T}_{1}$. The gain of the amplifier is about 12.9 dB with an input VSWR of 1.12 .

### 4.1.3.3 Cascade Connection of Amplifiers

To conclude this series of tests, both Class AB and Class C amplifiers were cascaded, with their biasing conditions set at those for Figure 4.7 (b) and 4.8 (c) respectively. The input power of the Class AB amplifier was increased until the output power of the Class C amplifier reached 160 W (the power being limited to avoid excessively high temperatures in the ferrite cores). The voltage waveforms at the output of both amplifiers is shown in Figure 4.9. The results are summarised in Table 4.5.
(a) OUTPUT VOLTAGE CLASS C
(b)

OUTPUT VOLTAGE CLASS AB

$50 \mathrm{~V} /$ DIV. 15 nS /DIV.
$20 \mathrm{~V} /$ DIV.

Figure 4.9 Output Waveforms of Cascaded Amplifiers.

| Table 4.5 <br> Results of Cascaded Operation of amplifiers. |  |
| :---: | :---: |
|  |  |
| Parameter | Value |
| Input power to Class AB amplifier | 280 mW |
| Input port VSWR of Class AB amplifier | 1.16 |
| Power into Class C amplifier | 4 W |
| Input port VSWR of Class C amplifier | 1.21 |
| Power output of Class C amplifier | 160 W |
| Output port VSWR of Class C amplifier | 1.12 |
| Power gain of the amplifier | 27.6 dB |
| Overall efficiency | $50 \%$ |

### 4.1.4 Conclusions of Linear Amplifier Results

Although continuous output powers of only 160 W were achieved, a pulsed power level of 300 W was obtained, the overall efficiency in this case being $60 \%$. These power levels are considered suitable for small scale plastic welding applications where a portable unit is desirable.

Higher powers could be achieved either by the paralleling of several amplifier modules and/or by the use of higher power RF MOSFETs such as the MRF154. However, circuit design and construction is ill defined and a certain degree of 'cut and try' was required with the prototype units in order to obtain satisfactory performance. Also, harmonic distortion of the ouput waveform is high and efficiency poor.

### 4.2 Class E Inverter

The Class E inverter (amplifier) was developed in the mid 1970's for use in lightweight, low power, high efficiency power converters/inverters and RF amplifiers (Sokal et al. 1975). By the method of operation, the Class E inverter eliminates the simultaneous high voltage and current stress on the active device and subsequent power loss during switching transitions by shaping the device current and voltage waveform.

This waveform shaping is achieved by means of a series inductor capacitor network whose resonant frequency is slightly lower than the operating frequency of the inverter. The circuit employed is shown in Figure 4.10.


Figure 4.10 4.5 MHz 75 W Class E Inverter Circuit and Ideal Waveforms.
With reference to Figure 4.10 and idealised Class E waveforms shown in Figure 3.10 (repeated here for convenience), circuit operation can be simply described as follows. The active device is operated as a switch, and ideally the only losses are conduction loss. The RF choke $L_{1}$ provides a d.c. current to the inverter. The shunt capacitor $C_{1}$ which incorporates the device output capacitance can be considered to act as a snubber element, limiting the rate of rise of drain voltage at turn off. The output network consisting of $L_{2}, C_{2}$ acts as a slightly lagging resonant network which carries the drain voltage up to a peak and back to zero in a damped oscillatory action before turn on occurs. Since the output network is lagging, current rises in the switch after the drain voltage is brought to zero (during a zero $\mathrm{d} v / \mathrm{d} t$ region). Thus switching loss - including the loss which is often incurred in discharging the device output capacitance at turn on ( $1 / 2 C V^{2} f$ loss) is negligible.

The Class E inverter has advantages over traditional linear amplifiers (Class B, Class C) in that it is largely insensitive to component tolerances particularly the active switching element characteristics (Raab 1978a, Kazimierczuk 1983a) also the circuit operation is well defined and predictable (Kazimierczuk 1984). Thus reliable circuits can easily be designed and built without having to resort to the empirical, heuristic techniques often associated with Class $\mathrm{A}, \mathrm{B}$ or Class C amplifiers.

### 4.2.1 Design and Construction of Prototype

The desired waveforms for Class E operation can be produced to any degree of accuracy by increasing the complexity of the load network. However, first-order approximations can be achieved using only three or four discrete components in the load network. The equations used in the design of the prototype are given in Appendix III. A simple BASIC program was written to give the required component values and ratings for a Class $E$ amplifier for either a required power output into a specified load at a specified frequency and operating $Q$, or maximum power delivered to a specified load for a given transistor ratings. The program calculates component values, current and voltage stress and power dissipated in the active device. The computer listing is given in Appendix IV.

The amplifier essentially consists of three parts:
(a) an active device;
(b) a gate drive circuit; and
(c) a matching network and load.

The active device chosen was an RF power MOSFET, the Motorola MRF150 which is a 150 W device designed for use in linear amplifiers operating at frequencies from 2 to 175 MHz . It has a maximum drain-source voltage of 125 V , continuous drain current of 16 A and input capacitance of 350 pF (reverse transfer capacitance being only 50 pF ).

The gate drive circuit is shown in Figure 4.11 and incorporates the DSO026 National Semiconductor MOS clock driver IC which has a rise time of 20 ns into 1000 pF . Figure 4.12 shows a typical MRF150 gate voltage waveform when operating at a frequency of 4.5 MHz with a drain supply voltage of 25 V and drain supply current of 3 A .


Figure 4.11 4.5 MHz Class E Inverter Drive Circuit.


Figure 4.12 MRF150 Gate Drive Waveform at 4.5 MHz . ( 10 V/Div. $50 \mathrm{~ns} /$ Div.)

The prototype was designed for an output power of $75 \mathrm{~W}(25 \mathrm{~V}$ at 3 A$)$ and a desired operating frequency of approximately 4.5 MHz . This gave an anticipated maximum drain current of 12 A and a peak drainsource voltage of 96 V (Hinchliffe et al. 1987e-f). From the design equations the required circuit components are as follows:

$$
C_{1}=1.2 \mathrm{nF}, C_{2}=1.8 \mathrm{nF}, L_{1}=7 \mu \mathrm{H}, L_{2}=0.8 \mu \mathrm{H}, R_{\mathrm{L}}=4.8 \Omega
$$

The initial load resistance of $4.8 \Omega$ was chosen for ease of component choice but in the later stages of the work a matching transformer was included so that power could be delivered to a $50 \Omega$ load, since it is often convenient, in high frequency electric process heating applications, to use a $50 \Omega$ power transmission system.

The inductors were of an air core type designed on the Brooks inductor principle (Murgatroyd 1986), which gives maximum inductance for minimum wire length, thereby maximising inductor $Q$ and hence minimising inductor conduction loss. The design equations for the Brooks coil are given in the above reference and in Appendix V. Again a computer program was written to calculate the required inductor dimensions, turns ratio and wire diameter for the required current and operating frequency, the listing is given in Appendix IV. The capacitors used were Unilator' high frequency power ceramics.

### 4.2.2 Class E Inverter Results

Figure 4.13 shows the drain-source and the load voltage waveforms and the source current waveform with a d.c. power input of 64 W , when supplying the $4.8 \Omega$ load. Conversion efficiency is approximately $90 \%$. The source current was measured by means of a low value, low inductance resistance placed in series with the source connection. The initial current pulse on the source current waveform before main device conduction is due to gate charging current.

Figure 4.14 shows the affect on the circuit of operating above the designed operating frequency. Drain-source and load voltage waveforms (Figure 4.14(a)) and drain-source voltage and source current waveforms (Figure $4.14(\mathrm{~b})$ ) are shown for operation at 6 MHz . The drain current is seen to rise before the drain voltage has been carried to zero, thus efficiency is reduced due to switching loss, further loss is incurred in discharging the shunt capacitance $C_{1}$. This is observed in the large current spike at turn on due to rapid discharge of the shunt capacitor which (at turn on) has a voltage above the saturation voltage of the device.

Similarly, when operated well below the designed operating frequency at 3.78 MHz (Figure 4.15(a) and (b)) the device is switched on after the zero $\mathrm{d} v / \mathrm{d} t$ region, and again efficiency is reduced. Again a large source current spike is seen at turn on due to the rapid discharge of the shunt capacitance. In both cases conversion efficiency dropped from above $90 \%$, when operated at designed frequency, to approximately $70 \%$ when operated at either 3.8 MHz or 6.0 MHz .

[^3]

Figure 4.13 (a) $\quad 75 \mathrm{~W}, 4.5 \mathrm{MHz}$ Class E Waveforms at Designed Frequency. Upper Trace - MOSFET Drain-source Voltage ( 50 V/Div. $50 \mathrm{~ns} /$ Div.); and
Lower Trace - Load Voltage ( $4.8 \Omega$ load) ( $20 \mathrm{~V} / \mathrm{Div} .50 \mathrm{~ns} / \mathrm{Div}$. )


Figure 4.13 (b) Upper Trace - MOSFET Drain-Source Voltage
( 50 V/Div. $50 \mathrm{~ns} /$ Div.); and
Source Current Waveforms ( $4.8 \Omega$ load).
( $2.5 \mathrm{~A} / \mathrm{Div} .50 \mathrm{~ns} / \mathrm{Div}$.)


Figure 4.14 (a) $\quad 75 \mathrm{~W}, 4.5 \mathrm{MHz}$ Class E Waveforms above Designed Frequency Upper Trace - Load Voltage
( $20 \mathrm{~V} / \mathrm{Div}$.$50 \mathrm{~ns} / Div.); and$
Lower Trace - Drain-source Voltage.
( $50 \mathrm{~V} / \mathrm{Div} .50 \mathrm{~ns} /$ Div.)

|  |  |  |  | $11 / \Delta{ }^{\text {l }}$ | 6.00 MHz |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | , | $\vdots$ |  | , |  |  |  |
|  |  |  |  | $\sim^{1}$ |  | - |  |
| $J$. | $\cdots$ |  | $n$ |  | m | $\checkmark$ |  |
|  |  | - | n | 1 | - | V | - |
|  | $L$ |  |  |  | $74$ |  | 1 |
|  |  | ; |  | 1 |  |  |  |
|  | 500 mV |  | 50 V |  | 50ns. |  |  |

Figure 4.14 (b) Upper Trace - Source Current
( 2.5 A/Div. $50 \mathrm{~ns} /$ Div.); and
Lower Trace - Drain-source Voltage.
( 50 V/Div. $50 \mathrm{~ns} /$ Div.)


Figure 4.15 (a) $\quad 75 \mathrm{~W}, 4.5 \mathrm{MHz}$ Class E Waveforms below Designed Frequency Upper Trace - Load Voltage
( $20 \mathrm{~V} / \mathrm{Div}$.$50 \mathrm{~ns} / Div.); and$
Lower Trace - Drain-source Voltage. ( 50 V/Div. $50 \mathrm{~ns} /$ Div.)


Figure 4.15 (b)
Upper Trace - Source Current
(2.5 A/Div. $50 \mathrm{~ns} /$ Div.); and

Lower Trace - Drain-source Voltage.
( 50 V/Div. $50 \mathrm{~ns} /$ Div.)

Figure 4.16 shows the drain-source and load voltage waveforms when the Class E amplifier was used to supply a $50 \Omega$ load. An approximately 9:1 impedance ratio transformer was used consisting of two ferrite core toroids with 0.9 mm diameter enamelled copper wire twisted pair windings. With a d.c. input of 30 V and 2.5 A (i.e. 75 W ) the power into the $50 \Omega$ load was 70 W at 5 MHz giving a conversion efficiency of $90 \%$.


Figure 4.16
75 W 4.5 MHz Class E Waveforms - $50 \Omega$ Load Upper Trace - Drain-source Voltage
( $50 \mathrm{~V} / \mathrm{Div} .50 \mathrm{~ns} /$ Div.); and
Lower Trace - Output Voltage.
( 50 V/Div. $50 \mathrm{~ns} /$ Div.)
Because of the high cost of the MRF150, the device was replaced with a standard power MOSFET, the IRF630 having a 200 V breakdown voltage, 8 A continuous current rating and input capacitance of 800 pF (reverse transfer capacitance of 150 pF ). Although operating efficiency dropped to $80 \%$ due to the higher switching times and the higher output capacitance of the IRF630 over the MRF150, resulting in non-ideal Class E operation, the device worked well, producing 100 W at 5 MHz . It was concluded that if the drive circuit was improved to allow rapid charge and discharge of the $\mathbb{R F} 630$ 's higher input capacitance, and the Class E inverter re-designed to accommodate the higher output capacitance of the IRF630 then standard power MOSFETs could be used in place of the more expensive RF power MOSFETs, at frequencies at least up to 5 MHz .

### 4.3 Conclusions

The RF power amplifier (in cascade) has the capability of delivering a pulsed output power of 300 W at 27 MHz which is suitable for plastics welding applications in the medical and veterinary fields such as sample sealing, e.g. blood, saline solutions etc. Because of the high operating temperature of the ferrite
cores during sustained high power tests, the circuit performance was tested below its maximum capability. Nonetheless, the cascade circuit showed an overall power gain of 27 dB when the power output was 160 W . Higher powers could be achieved by combining the outputs of a number of identical units operated in parallel.

However, circuit, component and PCB layout design is ill defined (often heuristic in nature) and critical. It proved difficult to obtain clean output waveforms with low harmonic distortion (even when operating in Class AB mode). Thus heavy filtering would be required in industrial units. Also operating efficiency is poor, with forced air cooling necessary for continuous operation.

Conversely, the Class E inverter is highly efficient, component values are not critical and the operation and design procedure is well defined allowing a-priori prediction of circuit performance. Although only 100 W at 5 MHz was achieved (the power levels exceeded the design values though) it was found that standard power devices could be used instead of the more expensive RF MOSFETs. Also the well behaved nature of the circuit, with its clean output waveforms, suggested that it is more suitable for use as an RF heating power source than linear amplifiers such as the Class C amplifier.

The circuit is simple yet has scope for much further development in terms of increased power (by the use of higher power MOSFETs) and/or increased frequency of operation (by the use of a superior drive circuit). Hence, subsequent work, detailed in the following chapters, concentrated on developing the Class E inverter for use as a high power, high frequency, electric process heating power source and on increasing the switching speed of standard power MOSFETs.

## Chapter 5

## HIGH SPEED SWITCHING OF POWER MOSFETS

An investigation is made into the limitations on switching speed of several power MOSFET types. A practical appraisal is made of maximum switching speeds and the main limiting factors.

## 5 HIGH SPEED SWITCHING OF POWER MOSFETS

Since the advent of the power MOSFET in the late 1970's and early 1980's, much attention has been focused on optimising its switching performance (Kom et al. 1983, Bullough et al. 1983, Severns et al. 1986). Recent developments in the use of distributed power conditioning for logic circuits, pulse power applications and high frequency power conversion has resulted in a requirement for an increase in switching frequencies.

At present, most switched mode converters operate at switching frequencies of between 10 kHz to 100 kHz . The latest generation of power converters operate in excess of 500 kHz , and it is predicted that in the near future, conversion frequencies in the MHz region will be used in production units (Carsten 1987b).


Figure 2.7 Ideal MOSFET and Associated Parasitic Components.
Figure 2.7, repeated here for convenience, depicts an ideal power MOSFET with associated parasitic elements. The terms shown have been defined in Table 2.2 and typical values for an RF450 given. At moderate switching speeds, say 50 to 100 ns , the principal components affecting switching time are: input capacitance ( $C_{i v e}$ ); reverse transfer capacitance ( $C_{r u}$ ); gate drive impedance $Z_{\text {dime }}$ and gate drive voltage $V_{\text {diviw }}$. Output capacitance ( $C_{\text {out }}$ ) mainly affects turn off only. To a large extent $Z_{\text {dime }}$ and $V_{\text {drive }}$ are under the control of the circuit designer and these can be chosen to achieve the required switching speeds. To a
lesser degree, stray capacitance can be controlled by suitable mounting methods. For example a TO3 package with a mica insulator has a case to heat sink capacitance of up to 400 pF , a 1.4 mm beryllia insulator adds a parasitic capacitance of only 27 pF .

At higher switching speeds, in particular below 10 ns , parasitic components such as the intrinsic resistance of the polysilicon gate network, lead inductance and lead resistance become more dominant. At switching frequencies above 1 MHz , skin and eddy current effects tend to increase lead resistance whereas lead inductance tends to fall due to reduced permeability. In metal packages, lead inductance and resistance effects are aggravated by eddy currents induced into the casing in the proximity of the device leads (Severns et al. 1986).

Of the components mentioned $C_{i u s}, C_{r u p}, C_{a u s}$ and the internal gate resistance are largely a function of the material, size and structure of the silicon die whereas drain lead inductance, $L_{d}$, source lead inductance, $L_{s}$, gate lead inductance, $L_{z}$, and gate and source lead resistance are a function of the package used. In standard devices, inductance in the source connection is common to both the drive circuit and the power or load circuit. This inductance introduces unwanted source feedback at turn on and turn off due to the high rate of change of drain current which creates a voltage across $L$, in opposition to the applied gate voltage.

In this chapter, investigations into the affect of source inductance on the switching speed of the TO3 packaged IRF450 are reported. The use of the kelvin contact to increase switching speed of TO220 packaged, current sensing MOSFETs is analysed and the failure mode of such devices, when used in a high frequency inverter, investigated. Finally, the results of high speed switching tests performed on RF packaged power MOSFETs are detailed.

### 5.1 The Effects of Source Inductance on an IRF450

One of the more commonly used power MOSFETs, and, until recently, one of the more powerful single die MOSFETs is the IRF450. This device has been used extensively in single phase, off line, medium frequency (up to 400 kHz ) induction heating supplies (Hinchliffe 1983, Tebb et al. 1985, Taylor 1986, Hinchliffe et al. 1988a). The following describes an investigation into the maximum, practical, attainable switching speed of an IRF450 and, in particular the affect of source feedback on the switching performance.

### 5.1.1 The Modified MOSFET and Test Circuit

In order to determine the affect of the source inductance, and to establish practical upper limits on the switching speed of the IRF450, a TO3 packaged device was modified by removing the top of the metal can, drilling a hole through the base between the existing gate and source terminals and installing a gold plated 'wire wrap' pin for use as a separate source lead. Several gold bonding wires were used to connect the pin to the source pad of the die to reduce inductance and provide sufficient current carrying capability. A PTFE bush was used to insulate the pin from the metal base or drain connection of the TO3 package. The resulting arrangement is shown in Figure 5.1.


Figure 5.1 Modified IRF450.
To investigate the effects of incorporating this separate source lead, a high speed drive circuit was developed based on the DS0026 MOS clock driver. This device has a high output current drive ( $\pm 1.5 \mathrm{~A}$ ), is capable of high repetition rates ( 5 to 10 MHz ) and has rise and fall times of 20 ns when driving a 1000 pF load. The output current drive is boosted by a pair of p and n channel MOSFETs in common source connection, this arrangement increases the DSO026 drive capability to $\pm 4 \mathrm{~A}$ peak. Four of these drive circuits were parallel giving a 16 A peak drive capability with a $0.5 \Omega$ drive source resistance. The complete circuit schematic is shown in Figure 5.2.
A great amount of care was taken over the PCB layout to obtain the full performance of the high speed drive circuit. When switching high currents at speeds in terms of nano seconds, parasitic circuit components can severely limit the potential of any circuit. For this reason a low inductance earth plane construction was used, the drive and signal side ground plane, $\mathrm{S}_{1}$, is held separate from the power or load side ground plane, $\mathrm{S}_{2}$. The only point where the power and drive side are electrically connected is at the actual source bonding pad of the MOSFET die. To minimise any delays between one driver circuit switching with respect to another, signal paths from input to the separate drive circuits were kept, as far as possible, to equal lengths.

The high current connection between the driver outputs and the gate of the IRF450 were made as short and wide as possible to reduce the stray inductance effects. Finally, the load resistance was placed above and in parallel with $\mathrm{S}_{2}$ to reduce the $L / R$ time constant of the load. Ideally a coaxial load construction should be used but it was found that load inductance could be held to a sufficiently low level by the method employed.


Figure 5.2 Switching Test Drive Circuit Schematic.

The complete test circuit, including the modified IRF450, is shown in Figure 5.3. The miniature coaxial sockets which can be seen above the gate and drain connection of the IRF450 provided a low inductance connection for the oscilloscope probe.


Figure 5.3 High Speed Switching Test Circuit.
Since a commercial pulse generator could not be used to drive the circuit (the earth connections of the measuring oscilloscope and oscillator would create a second electrical connection between $\mathrm{S}_{1}$ and $\mathrm{S}_{2}$, the timing pulses were generated by an isolated logic circuit designed to provide 60 ns pulses at a repetition rate of 20 kHz . This low duty cycle ensured that neither the load resistance nor MOSFET would over heat. A pre-trigger pulse, occurring some 10 ns before the drive pulse, was provided to synchronise the oscilloscope whilst observing switching waveforms (this had the advantage of placing the measured pulse centrally on the oscilloscope display), a high frequency pulse transformer being used to couple the pretrigger to the oscilloscope, ensuring isolation. To maintain clean signals without reflections, a $50 \Omega$, characteristic impedance, interconnection system was used. The pulse generator circuit diagram is given in Figure 5.4.


Figure 5.4 Pulse Generator used in High Speed Switching Tests.

### 5.1.2 Switching Test Results

Switching test were performed for three values of load resistor and thus drain current, drain supply voltage being 300 V . The resistance values are $47 \Omega$ (drain current, $I_{d}=6.4 \mathrm{~A}$ ), $27 \Omega$ (drain current being 12 A which is the device's maximum continuous drain current) and $12 \Omega$ (drain current being 25 A ). For each range of load resistance and drain current, comparison was made of the device switching performance with the extra source terminal isolated (as per a standard device) and when employing the extra source terminal as a drive connection. This was effected by modifying the test circuit PCB, using low inductance copper strip to either connect the second source lead to the drive ground or the original source lead to the drive ground. This method allows the same transistor and drive circuits to be used for both modified and unmodified tests. Thus the same MOSFET die is used when evaluating both standard and modified switching performances, ensuring a true comparison.

A comparison of switching times for standard and modified drive connection is given in Table 5.1 for the drain currents of $6.4 \mathrm{~A}, 12 \mathrm{~A}$ and 25 A . The improvement in turn on speed increases with drain current, that is source feedback effects are greater for higher drain currents (due to increased rates of change of current). At the rated continuous current of 12 A , the reduction in turn on time when employing the modified drive configuration is approximately $120 \%$. The turn off times, i.e. drain current fall times,
drain voltage rise times, are almost identical for standard and modified drive connections (that is whether employing the extra source connection or not) and are govemed by the $R C$ time constant of the load and MOSFET oupput capacitance.

| Table 5.1 <br> Results of switching tests on IRF450. |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Drain <br> Current <br> A | Load Resistance $\Omega$ | Drain Voltage Fall Time ns |  | Improvement <br> \% | Drain Voltage Rise Time ns |  |
| $V_{4}=300 \mathrm{~V}$ |  | Standard MOSFET | Modified MOSFET |  | Standard MOSFET | Modified MOSFET |
| 6.4 | 47 | 5.6 | 4.4 | 28 | 16.5 | 16.5 |
| 12 | 27 | 11 | 5 | 120 | 6.5 | 6.5 |
| 25 | 12 | 24.1 | 7.5 | 220 | 4 | 4 |

To demonstrate these results, oscillograms are given for both standard and modified switching tests of: drain voltage ( $v_{d}$ ); gate voltage ( $\nu_{s}$ ); and voltage developed across the source terminal ( $v_{L_{L}}$ ) (when not employing the extra source connection), measured with respect to the appropriate ground plane, for the 25 A drain current tests. Further tests and more detailed analysis can be obtained from the following references: Hinchliffe et al. 1988b; 1988c; 1989a.

Throughout the tests the gate drive pulse duration was held to 60 ns unless otherwise specified, the gate drive voltage being held to 14 V . The gate drive voltage was measured at the head of the kovar lead inside the TO3 case. Ideally this measurement should be made at the gate bonding pad itself, but this is difficult with conventional oscilloscope probes if device destruction is to be avoided. The inductance of the internal bonding wire will have some affect on the voltage waveform at the gate itself but this should be less than that due to the inductance of the kovar pin and PCB track extemal to the package.

Measurements of the voltage developed across the source lead inductance was performed with the extra source lead isolated from the circuit. The head of the second source lead (the gold wire wrap pin) was then used as a measurement point for the source voltage since, when isolated from the drive circuit, the second source lead is electrically at the same potential as the source bonding pad. Thus physical contact of the probe tip with the source pad is not made. Although this method of measurement is not ideal, the waveforms observed should be a realistic representation of the actual source pad voltage. Perraps a slight amount of ringing is caused by the reaction of the bonding wire inductance with the probe tip capacitance but this ringing will be less than that caused by the earth lead inductance of the probe - although a short ( 20 mm ) earthing spring was used to keep this to a minimum.


Figure 5.5 Gate Drive Waveform to IRF450, $V_{\mu}=0 \mathrm{~V}(5 \mathrm{~V} / \mathrm{Div} .20 \mathrm{~ns} /$ Div. $)$.
Figure 5.5 (above) shows the gate drive waveform used for the switching tests. The gate drive voltage being 14 V and pulse duration is 60 ns , no voltage was applied to the drain load. The gate drive falling edge is slightly faster than the rising edge, one factor affecting this being the lower on resistance and faster switching speed of the n channel gate drive transistors over the p channel drive transistors. The affect of the polysilicon intrinsic gate resistance can be observed by the fact that the plateau region at turn on is approximately 2 volts higher than at turn off. The gate voltage rings slightly after the turn off transition, the frequency of ringing being approximately 16 MHz which is the self resonant frequency of the gate network.

Figure 5.6 shows the voltage developed across the source bond wire and lead at the switching transients with no applied drain voltage. Comparison with Figure 5.5 will prove useful. The peak voltage developed across the source connection is roughly the same at turn on as at turn off, being 5 to 6 volts and of 6 ns duration. The voltage transients are developed in the source inductance by the high rates of change of gate charge and discharge current at the gate drive switching edges. These voltage transients coincide with those seen at the gate.


Figure 5.6 IRF450 Source Voltage $V_{\boldsymbol{\mu}}=\mathbf{0 V}$ (2 V/Div. $20 \mathrm{~ns} /$ Div. $)$.
Since voltage cannot change instantaneously across the gate capacitance, any sudden transient at the source will result in a transient at the gate of an equal amplitude. These transients serve to reduce the drive voltage available to charge the gate and thus reduce the rate of rise of gate voltage and therefore the switching speed. Ringing on the gate after tum on and turn off is observed by the ringing currents developing a voltage across the source connection.

Referring to Figure 5.5 again, the plateau region, at about $v_{t}=6 \mathrm{~V}$, is reached in 3 ns. The source switching transient causes the gate to rise to 9 V above ground. This reduces the available drive voltage and the rate of rise of gate current falls, causing the source and gate voltage to drop by 3 volts. The gate then charges by a series of ringing transients back to 9 volts. The end of the plateau region is reached in roughly 15 ns . At this point the gate current reduces (observe the negative transient on the source voltage waveform) and the gate is over driven at a slower rate to the full 14 V , overshooting slighty to 15 volts.

At turn off the gate is discharged rapidly to 8 volts at which point the negative transient, which is developed across the source lead, reduces the rate of rise of gate discharge current. This, in turn, causes the source lead voltage to collapse and, as the gate voltage rises, gate discharge is resumed at a slightly slower rate. The gate is fully discharged in roughly 22 ns but proceeds to ring slightly resulting in an undershoot of some 2 volts.

### 5.1.2.1 Switching Tests on the Unmodified IRF450

The following section details switching of a peak drain current of 25 amperes through a load resistance of $12 \Omega$ using a drain load supply voltage of 300 V with the original source lead used for both drive and power circuits.

Figure 5.7 depicts the falling drain voltage at turn on, 10 to $90 \%$ fall time is 24.1 ns. The effect of source feedback on the rate of rise of drain current and therefore fall of drain voltage is clearly visible when the drain voltage has collapsed to 150 V .

Figure 5.8 shows the rising drain voltage at turn off. Here turn off is completed in about 4 ns with a 60 V overshoot occurring, indicating that with a load resistance of $12 \Omega$ the load circuit is slightly under damped. The voltage at turn off is lower than at turn on due to charge being lost in the RF by-pass capacitors used to supply the high pulsed currents.

The turn off time is governed by the response of the under-damped load network; the load resistance, stray inductance and the IRF450's output capacitance, and appears to be unaffected by source feedback effects. For higher load resistance values, where this network is over damped, tum off times are determined by the $R C$ time constant of the load resistance and $C_{\text {our }}$.


Figure $5.7 \quad$ Falling Drain Voltage of Unmodified IRF450 Switching 300 V, 25 A ( 50 V/Div. $10 \mathrm{~ns} /$ Div.).


Figure $5.8 \quad$ Rising Drain Voltage of Unmodified IRF450 Switching 300 V, 25 A (50 V/Div. 2 ns/Div.).

Figure 5.9 shows the voltage developed across the source lead. It is useful to compare this figure with the gate drive and source voltages shown in Figures 5.5, and 5.6. The initial voltage puise due to the gate drive has a 5 V amplitude. As the device switches, a second pulse, resulting from the rapidly rising drain current, is seen. This second pulse reaches a peak of 12 V , the rate of rise of current then falls rapidly until the induced voltage across the source terminal has fallen to 6 V ; this is followed by a more sustained source voltage, caused by the, now reducing, rate of rise of drain current which has an almost constant slope from 6 volts to 0 volts. The device is fully switched on some 55 ns after conduction first began. It is apparent that this sustained voltage across the source lead is the main factor in the slowing of the rate of turn on of the MOSFET.

At turn off, a negative transient is developed corresponding to the falling edge of the gate drive waveform. The peak voltage being about -7 volts. Of more interest is the voltage transient developed across the source lead some 20 ns after the gate discharge transient. This corresponds to the falling drain current, which is delayed by some 15 ns after the gate voltage has fallen to zero. The induced voltage transient at turn off takes the source to 15 V below ground, the duration of the transient being 8 ns . It is important to note that the rate of fall of drain current is not reduced by this negative transient on the source. That is, turn off is not affected by the negative voltage developed across the source lead. This observation supports the measured results given in Table 5.1.


Figure 5.9 Induced Source Voltage of Unmodified IRF450 Switching 300 V, 25 A ( 5 V/Div. 20 ns/Div.).

Figure 5.10 shows the voltage across the source lead, superimposed on the drain voltage waveform. This confirms the description of the switching characteristics given above. The high source voltage pulse at turn on slows the rate of fall of drain voltage (and therefore rise of drain current). However, turn off is unaffected by the large negative transient on the source lead. During turn on, the source voltage transients due to gate charging current and rising drain current coincide and turn on is slowed. But during turn off there is a delay between the transient caused by the gate discharge current and that caused by the falling drain current. This delay goes some way to explaining why turn off is unaffected by source feedback.

Finally, Figure 5.11 shows the 14 V gate drive pulse superimposed on the drain voltage waveform. The 16 volt pulse just after the start of the plateau region coincides with the positive induced voltage pulse on the source lead. This is of sufficient amplitude to cause the reverse diodes in the $p$ channel drive transistors to become forward biased. It effectively reduces the drive voltage available to charge the input capacitance to complete turn on. Indeed if the integral anti-parallel diodes in the drive transistors start to conduct, the gate capacitance could begin to discharge. The gate voltage follows the same trends as the source voltage; that is the gate voltage drops back to the plateau level at $v_{g}=9 \mathrm{~V}$ as the drain current reaches its final value. Just before the end of the gate drive pulse, the gate voltage is seen to rise as the gate capacitance continues to be charged, over driving the transistor. Although, unlike the gate waveforms at lower currents, here the gate does not reach its full value before turn off is initiated.


Figure 5.10
Source Voltage Superimposed on Drain Voltage of Unmodified IRF450 Switching 300 V, 25 A ( 5 V/Div. 50 V/Div. 20 ns/Div.).


Figure 5.11
Gate Drive Waveform Superimposed on Drain Voltage of Unmodified IRF450 - Switching 300 V, 25 A ( 5 V/Div. 50 V/Div. 20 ns/Div.).

Considering now the turn off interval, the initial negative going transient, which occurs when $v_{z}$ has fallen to 6 volts, is in response to the voltage developed across the source lead inductance by the rapid rate of change of current flow out of the gate. This pulls the gate capacitance down by around 6 volts. As the gate current reduces, the negative source voltage transient reduces and the gate drive resumes removal of charge from the gate resulting in a second, smaller transient. At $v_{s}=2 \mathrm{~V}$ the device switches off, the rapidly falling drain current develops a large negative voltage transient across the source lead which is again reflected at the gate. By now the gate voltage has fallen to below the threshold level, and, although gate discharge is halted, the negative transient (which is some 16 V below the 0 V level) has little influence on the turn off speed of the MOSFET. After turn off is completed and the rate of fall of drain current has reduced to zero, the gate voltage resumes its original level and the drive circuit removes the remaining charge from the gate. Because there is a certain amount of gate circuit inductance, the gate rings slightly negative before assuming a 0 V 'off' level.

It is of interest that when the gate swings negative by 16 V , the reverse diode in the n channel drive transistors should be forward biased and start to recharge the gate capacitance, effectively turning the device back on. The fact that this does not occur can possibly be attributed to the gate lead inductance.

Overlap of the source and gate voltage on the drain voltage shows that the large voltage transients on the gate and source coincide with rapid rates of change of drain current. This indicates that stray load inductance is low enough such that it can be assumed that the drain voltage is the reciprocal of the drain current. The high frequency ringing seen on the gate voltage waveform is caused by the interaction between the two oscilloscope probe grounds which were, by necessity, located at different points in the circuit.

### 5.1.2.2 Switching Tests on the Modified IRF450

This section details oscillograms taken during switching tests on the modified IRF450 when switching 25 A with a drain supply voltage of 300 V and utilising the added source lead to connect the source to drive ground, isolating drive and power source connections.

Figure 5.12 shows the resulting drain voltage waveform falling edge, 10 to $90 \%$ fall time is achieved in 7.5 ns , roughly three times faster than when using the original source lead for both the drive and power returns. The rising edge of drain voltage at turn off is shown in Figure 5.13; 10 to $90 \%$ rise time is 4 ns , almost twice as fast as turn on and identical to the turn off times achieved with the unmodified source connection. Again overshoot occurs due to interaction of the load circuit stray inductance with the device output capacitance.

Knowing the value of the load resistance and the frequency of the settling transient at turn off, being approximately 100 MHz , a value for the stray load inductance can be calculated from:

$$
\begin{equation*}
L_{\mathrm{smay}}=\frac{1}{C_{o w} \omega^{2}} \tag{5.1}
\end{equation*}
$$

Where:
$\omega=2 \pi f_{r}$
$f r$ is the frequency of oscillation.


Figure $5.12 \quad$ Falling Drain Voltage of Modified IRF450 Switching 300 V, 25 A ( 50 V/Div. 5 ns/Div.).


Figure 5.13
Rising Drain Voltage of Modified IRF450 Switching 300 V, 25 A ( 50 V/Div. 2 ns/Div.).

Using a typical value for $C_{o u s}$ of 400 pF , the stray load inductance is calculated as being approximately 6 nH . Given that the inductance of the MOSFET drain connection is some $4-5 \mathrm{nH}$, a stray load inductance of 1 to 2 nH is quite acceptable.

Finally Figure 5.14 depicts both turn on and turn off with the gate drive voltage superimposed on the drain voltage waveform. Comparison with Figure 5.11 shows more clearly how incorporating the extra source lead has improved turn on time. Close comparison of the turn off intervals between the modified and unmodified MOSFETs reveals that, at these higher current levels, the large negative voltage transient at the source may have had some influence on the rate of fall at drain current in that drain voltage overshoot is higher for the modified MOSFET than for the unmodified MOSFET (particularly when monitoring the gate or source voltage as well as the drain voltage). This effect is not observed, though, for the lower pulsed current levels of 6.4 A and 12 A (Hinchliffe et al. 1988b-c). The voltage transient at the start of device conduction, 8 ns after the gate drive pulse has started to rise, is much reduced over that when switching without the extra source lead, and is thought to be made up of voltage developed across the source metalisation of the MOSFET die and source resistance feedback effects. In fact there is little difference between the gate drive waveform observed without power supplied to the load and the waveform seen when using the additional source connection with power supplied to the load.


Figure 5.14
Gate Drive Waveform Superimposed on Drain Voltage Waveform for Modified IRF450 Switching 300 V, 25 A. ( 5 V/Div. 50 V/Div. 20 ns/Div.)

The positive going resonance, observed at the gate after turn off, is sufficiently large to start the device conducting slightly. This conduction occurs at a much lower external gate voltage than when the device is tumed on at the start of the drive pulse. There are a number of possible explanations:

1) since the ringing transient results in lower rates of change of gate current than the switching pulse, less voltage is developed across source and gate inductances and the gate voltage external to the device at the switching threshold will appear lower;
2) there could be some remaining stored charge in the gate; but
3) the more plausible explanation is that since the gate circuit is oscillating at its resonant frequency, the voltage across the capacitor will be $Q$ times the driving voltage where $Q$ is the quality factor of the circuit.

The delay in the drain voltage waveform collapsing to its lowest level during conduction, from $v_{d}=40 \mathrm{~V}=$ $V_{\text {deom(inital) }}$ to $v_{d}=20 \mathrm{~V}=V_{\text {deon(finalj, }}$, for the first 10 ns of full conduction is due both to the reversal of the gate-drain depletion layer capacitance and to the delay line effects of the polysilicon gate network and distributed gate capacitance. That is to say, the MOSFET cells closest to the aluminium gate bus turn on before those further removed. Thus, device 'on' resistance and therefore conduction drop is higher at the start of conduction (Severns et al. 1986, Zommer 1986). This is an important factor when considering high frequency operation using the modified package.

Thus, to conclude, when employing the extra source connection to isolate drive and power returns, tum on times are greatly improved whereas turn off is largely unaffected by source feedback. The switching potential of the MOSFET die is now limited by the remaining second order parasitic components of the gate and drive source lead inductance which limit the rate of change of gate drive current.

### 5.1.3 PSpice Simulation Results of the Switching Tests

To back up the practical results, computer simulations of the modified IRF450 were performed for both single and double source lead configurations. The simulation software package used was the personal computer (PC) based, analogue simulator - PSpice ${ }^{6}$. One of the principal advantages of using such simulation packages for this type of work is that circuit parameters which are difficult to measure, such as MOSFET die gate-source voltages, gate and drain currents, can be viewed.

The simulation circuits used are shown in Figures 5.15 to 5.17. The simulation program listings are given in Appendix VI. During the initial simulation runs it quickly became apparent that the simulated switching speeds were very much below those measured practically. The reason was traced to the IRF450 MOSFET model used in PSpice.

[^4]

Figure 5.15 Simulation Circuit for the Unmodified IRF450.


Figure 5.16 Simulation Circuit for the Modified IRF450.


Figure 5.17 Simulation Driver Sub-circuit.
There are two main errors in the MOSFET model which, discovered by later work, appears to be true of all the power MOSFET models and are inherent in the way the MOSFET models are generated using the PSpice device model option (Parts).

One inaccuracy is in the values of the MOSFET parasitic capacitances. Two of the parasitic capacitances in the model, the gate-drain overlap capacitance ( $C_{\text {sto }}$ ) and the gate source overlap capacitance ( $C_{p_{\text {so }}}$ ) are multiplied by the channel width ( $w$ ) to yield their actual value. In the IRF450 model provided by Microsim, $C_{\text {sto }}=773.2 \mathrm{pF}, C_{p s o}=2.208 \mathrm{nF}$ and $\mathrm{w}=1.1$ giving $C_{d g}=850 \mathrm{pF}$ and $C_{g s}=2.43 \mathrm{nF}$. The actual IRF450 data sheet values for these capacitances are 100 pF and 1800 pF respectively. Thus the MOSFET model parameters were changed to $C_{810}=91 \mathrm{pF}$ and $C_{200}=1.636 \mathrm{nF}$. Similarly the zero bias bulk-drain capacitance ( $C_{50}$ ) which constitutes the majority of the output capacitance is given a value of $1.732 \mathrm{nF}^{7}$, the actual data sheet value is 400 pF , thus $C_{b d}$ in the MOSFET model was reduced accordingly.

A final anomaly was discovered to be the value of the intrinsic polysilicon gate resistance ( $R_{s}$ ). This is given a value of $1.927 \Omega$ and is determined by the Bowers and Neinhaus technique of using the fall time characteristics of the drain current when switching a resistive load (Bowers et al. 1985). This is not an accurate method since, at high switching speeds, current flow into the output capacitor, as it is charged when the MOSFET has switched off, will distort measured current fall times. A better method is to measure the gate current at low switching speeds and note the difference in gate plateau voltages for gate charging and discharging currents.

[^5]The intrinsic polysilicon gate resistance can then be calculated using:

$$
\begin{equation*}
R_{z}=\frac{V_{p c}-V_{t a}}{2 I_{z}} \tag{5.2}
\end{equation*}
$$

$\left.\begin{array}{ll}\text { Where: } \quad V_{p} & \text { is the externally measured turn on } \\ \text { plateau voltage; }\end{array}\right\}$

The intrinsic gate resistance of several IRF450's was measured using this technique, described more fully in Appendix VII, the average measured intrinsic gate resistance was $0.9 \Omega$, the spread being about $0.2 \Omega$. The following results were obtained using the amended IRF450 PSpice model.

### 5.1.3.1 Simulation Results for the Unmodified MOSFET

In this section the results of the simulation run when switching 300 V and 27 A using a common source connection for both drive and power retums are given.

Figure 5.18 shows the simulated drain and source voltage. When compared with Figure 5.10 the simulated source voltage agrees well with the practical waveform, the voltage transient at turn on ( $t=1.025 \mu \mathrm{~s}$ ) is about 13 V and the transient at turn off ( $t=1.095 \mu \mathrm{~s}$ ) is approximately -15 V (cf. 12 V and -15 V measured). Again there is an observed delay of some 25 ns between the negative going source voltage transient, at $t=1.07 \mu \mathrm{~s}$, caused by changing gate current and that caused by the falling drain current at $t=1.095 \mu \mathrm{~s}$.

Similarly, the $10-90 \%$ fall time of the drain voltage is approximately 25 ns. However, turn off is very different. The simulation shows that the large negative voltage transient on the source serves to slow down the rate of fall of drain current (and therefore rate of rise of drain voltage). The very much slower turn off induces a sustained voltage across the source connection in a similar manner to that at turn on.

Drain current is shown in Figure 5.19 and is essentially the reciprocal of the drain voltage. Thus stray load inductance has little affect on the drain current and the load can be taken as being effectively resistive. Hence the measured drain voltage in the practical results can be considered to be in anti-phase and proportional to the drain current.


Figure 5.18 Simulation of Drain and Source Voltage for Unmodified MOSFET.
Figure 5.20 shows the simulated gate voltage and drain voltage. The measurement point in the simulation circuit being between the gate bonding wire inductance and lead inductance, node 7 , and ground, node 0 (Figure 5.15 ) which is equivalent to the head of the kovar pin in the TO3 package. Again the voltage waveform bears close resemblance to that measured. A surprising feature is that the negative sustained source voltage at turn off, which occurs between $1.1 \mu \mathrm{~s}$ and $1.15 \mu \mathrm{~s}$, is not reflected in the gate voltage.

In Figure 5.21, the actual gate-source voltage (equivalent to that on the MOSFET die) is shown along with the drain voltage. This again is proof of the earlier assumption that the large transients seen on the gate are in fact the voltage transients developed across the source lead which carry the gate-source potential up or down accordingly, without actually changing the potential across $C_{z s}$ (i.e. altering the charge in $C_{z z}$ ). Here, also, the effects of the 'Miller' capacitance can be seen, which holds the gate-source voltage constant at the 'plateau' level during switching.

During turn off, the gate-source voltage is seen to rise for a.period coincident with the sustained source voltage transient and reduced rate of rise of drain voltage (between $t=1.1 \mu \mathrm{~s}$ and $t=1.15 \mu \mathrm{~s}$ ). This indicates that the gate has regained charge, resulting in the slow down of the rate of turn off. The gate-source voltage during this period is the exact inverse of the source voltage and hence the sustained source voltage transient is not observed on the gate voltage (Figure 5.20).

IRF 450 PULSE TEST INCLUDING DRIVE INDUCTANCE. 1 SOURCE LEAD. RL=12 OHMS


Figure 5.19 Simulation of Drain Current and Source Voltage for Unmodified MOSFET.


Figure 5.20 Simulation of Gate and Drain Voltage for Unmodified MOSFET.


Figure 5.21 Simulation of Gate-Source and Drain Voltage for Unmodified MOSFET.

The gate current during switching is shown in Figure 5.22 along with the source voltage. Referring to Figure 5.22 , gate current rises rapidly at the start of the gate drive pulse at $t=1 \mu \mathrm{~s}$, it is slowed momentarily by the first source transient (caused by the changing gate current) and rises to a peak of 4 A at $t=1.02 \mu \mathrm{~s}$. The second source transient, caused by the increasing drain current as the device turns on at $t=1.05 \mu \mathrm{~s}$, reduces the gate current to 1 A , slowing device tum on. The gate current only rises again after the device has completed turn on at $t=1.07 \mu \mathrm{~s}$. At the end of the 60 ns drive pulse, at $t=1.07 \mu \mathrm{~s}$, the gate current is reduced rapidly to zero, causing the first negative voltage transient on the source of approximately -10 V (cf. -7 V for the practical measurement). This limits the flow of current out of the gate to -0.25 A.

At $t=1.08 \mu \mathrm{~s}$, after the source pulse has subsided, current flow out of the gate increases to reach a maximum of -2.8 A (a second, much reduced negative transient is seen on the source). The device begins to turn off at $t=1.095 \mu$ s inducing the large negative transient on the source which reduces the discharging gate current to zero. Although no current flows into the gate, the gate drive circuit is unable to sink the current which flows through the reverse transfer capacitance at turn off (due to the fact that the gate voltage is taken negative by the source transient). It is this current which serves to increase the voltage across the gate-source capacitance of the MOSFET die, so slowing turn off (Figure 5.21).


Figure 5.22 Simulation of Gate Current and Source Voltage for Unmodified MOSFET.
Thus the main discrepancy between simulated and practical results is that, in the simulation, turn off is affected by source feedback. One reason being that, in the simulation, the gate seems to regain some charge as an indirect result of the large negative source transient at turn off. In practice this seems not to occur. One possible explanation being that the drive circuit inductance maintains a gate discharge current, even when the gate is taken below 0 V , forward biasing the anti-parallel diodes in the n channel drive transistors. Also the PSpice model of the power MOSFET does not incorporate a varactor effect for the reverse transfer capacitance. In the actual power MOSFET the reverse transfer capacitance, being a depletion layer capacitance, has a much higher value at low drain voltages, when the device is turned on, than at high drain voltages. Thus there will be a greater delay between the gate drive falling edge and the resulting initiation in the fall of drain current in the practical power MOSFET than in the PSpice model. This delay results in the gate being discharged to below threshold before a significant change in drain current occurs.

### 5.1.3.2 Simulation Results for the Modified MOSFET

Results of the simulation of the modified MOSFET when switching 300 V and 25 A are given here.

Figure 5.23 shows the simulated drain voltage and the voltage developed across the power source connection ( $L_{s b 1}$ in Figure 5.16). Drain voltage fall time ( $10-90 \%$ ) is 9 ns which compares favourably with the 7.5 ns measured in practice. Similarly, rise time is 5 ns , compared to 4 ns in practice. The very rapid turn off of current induces a large negative transition on the power source voltage waveform of some -45 V .


Figure 5.23 Simulation of Drain and Source Voltage for Modified MOSFET.
The drain current and voltage devcloped across the power source lead are shown in Figure 5.24. The power source voltage is seen to be proportional to the derivative of the drain current and has no influence on the switching speed.

Figure 5.25 shows the gate and drain voltage. The gate voltage is similar to that measured in practise for the modified MOSFET except that more high frequency ringing, which results from interaction between lead inductance and device capacitance, is observed. This difference between simulation and practice is probably due to the fact that the PCB track RF resistances have not been modelled into the circuit which would, in practice, damp the high frequency ringing.

Finally, the actual gate-source voltage, measured between nodes 5 and 4 of the simulation circuit (Figure 5.16), and the gate current are shown in Figure 5.26. The gate-source voltage and current are not influenced by the large voltage transients across the power source lead. This again confirms the substantial improvement which arises from the addition of the second source connection, even in a low frequency package such as the metal can TO3.

IRF 450 PULSE TEST INCLUDING ORIVE INDUCTANCE. 2 SOURCE LEADS, $R=12$ OHMS



Figure 5.24 Simulation of Drain Current and Source Voltage for Modified MOSFET.
iff 450 PULSE TEST INCLuding dRive inductance. 2 source leads, f=12 OHMS Date/Time run: 05/07/88 12:56:34 Temperature: 27.0



Figure 5.25 Simulation of Gate and Drain Voltage for Modified MOSFET.


Figure 5.26 Simulation of Gate-Source Voltage and Gate Current for Modified MOSFET.

### 5.2 Use of the Kelvin Contact in Current Sensing MOSEETs

A study was undertaken into the use of the kelvin contact as a separate source connection to increase switching speed in International Rectifier's current sensing MOSFETs. These devices are developed specifically for use in current mode control, switched mode power supplies. The current sensing n-MOS symbol and circuit schematic are shown in Figure 2.14 (repeated here for convenience). The kelvin connection is provided to minimise measurement errors when monitoring the sensed current. It is possible to use this extra source contact as a separate drive return, there-by avoiding source feedback effects and increasing switching speeds. This was investigated for a number of current sensing MOSFETs with a view to using them in high frequency inverters.

Comparison is made of switching performance for standard connection of the device where the same source connection is used for both the gate drive circuit and the power circuit, and for when the kelvin contact is used as a separate drive return terminal.

Three transistor types were evaluated - the $\operatorname{RRC830}$ (a 500 V device capable of carrying 4.4 amperes continuous and 18 amperes pulsed), the IRC630 (a 200 V device capable of 8 amperes continuous, 36 amperes pulsed) and the $\operatorname{RRC} 530$ (a 100 V device capable of carrying 14 amperes continuous and 56 amperes pulsed). All devices have an input capacitance of approximately 700 pF .


Figure 2.14 Current Sensing MOSFET Symbol and Circuit Schematic.
For the IRC830, tests were performed for a load of $18 \Omega\left(I_{d}=17 \mathrm{~A}\right)$ with $V_{d d}$ set to 300 V , for the IRC630 tests were performed for a load of $15 \Omega\left(I_{d}=10.7 \mathrm{~A}\right)$ with $V_{d t}$ set to 160 V and for the IRC530, switching tests are performed for a load of $7.3 \Omega\left(I_{d}=13.3 \mathrm{~A}\right)$ with $V_{d d}$ set to 100 V .

The drive circuits used were of similar design to that used in the modified RFF450 switching investigation as described in section 5.1.1. Throughout the tests the gate drive pulse duration was held to 60 ns as before. The gate drive voltage was measured at the entrance of the gate lead to the TO220 package. When the kelvin contact is not employed, i.e. when the normal source connection was used for both drive and power circuits, the kelvin contact lead was used as a test point to monitor the voltage dropped across the source bonding wire and lead inductance during switching since, when not carrying current, the kelvin contact is electrically at the same potential as the source of the device.

A summary of the switching times obtained for both drive connection configurations is given in Table 5.2. The increase in turn on speed when using the extra source connection is greater than $60 \%$ in all cases. For the IRC530 and IRC630, only turn on is affected by source feedback to any significant degree, as is the case with the modified $\mathbb{R F} 450$. However, for the $\mathbb{R C} 830$ both turn on and turn off are affected, that is, using the kelvin contact reduces both turn on and turn off times.

| Table 5.2 <br> Results of High Speed Switching Tests on Current Sensing MOSFETs |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Device | Operating Conditions |  | With Use <br> of Kelvin <br> Contact | Without Use <br> of Kelvin <br> Contact | Improvement |
| IRC830 | $\begin{aligned} & V_{d u}=300 \mathrm{~V} \\ & I_{d}=17 \mathrm{~A} \\ & R_{L}=18 \Omega \\ & V_{z z}=14 \mathrm{~V} \end{aligned}$ | Drain Volt- <br> age <br> Fall Time | 5.13 ns | 12.7 ns | $148 \%$ |
|  |  | Drain Voit- <br> age <br> Rise Time | 3.84 ns | 9.53 ns | $148 \%$ |
| IRC630 | $\begin{aligned} & V_{d u}=160 \mathrm{~V} \\ & I_{d}=11 \mathrm{~A} \\ & R_{\mathrm{L}}=15 \Omega \\ & V_{s,}=14 \mathrm{~V} \end{aligned}$ | Drain Volt- <br> age <br> Fall Time | 4.34 ns | 8.46 ns | 95 \% |
|  |  | Drain Volt- <br> age <br> Rise Time | 4 ns | 4 ns | 0\% |
| IRC530 | $\begin{aligned} & V_{d u}=100 \mathrm{~V} \\ & I_{d}=13 \mathrm{~A} \\ & R_{L}=7.5 \Omega \\ & V_{s z}=14 \mathrm{~V} \end{aligned}$ | Drain Volt- <br> age <br> Fall Time | 7.42 ns | 11.9 ns | 60 \% |
|  |  | Drain Volt- <br> age <br> Rise Time | 3.33 ns | 3.66 ns | $10 \%$ |

### 5.2.1 Oscillograms of Current Sense MOSFET Tests

A more detailed analysis of the switching characteristics of current sensing MOSFETs is given below.

### 5.2.1.1 IRC830 Switching Waveforms

Figure 5.27 shows the $\mathbb{R C} 830$ drain voltage rising and falling edge when not employing the kelvin contact. Fall time ( $10.90 \%$ ) is 12.7 ns , the rate of fall of drain voltage can be seen to appreciably slow down at $v_{d}=150 \mathrm{~V}$, in fact the trend is seen to reverse showing that the gate losses charge. This effect is almost entirely due to the voltage dropped across the source bonding wire and source lead inductance caused by the high $\mathrm{di} / \mathrm{d} d$. This raises the source and therefore gate potential, slowing the rate at which the gate is charged by the drive circuit. Because the pulse current is high, some of the source feed back will be due to pinch off effects, that is the bulk source resistance increases almost exponentially with increasing drain current and at these high pulsed drain currents the source resistance $R_{s}$ is quite high ( $R_{s}$ is $9 \Omega$ at $I_{d}=17 \mathrm{~A}$ as opposed to $1.5 \Omega$ at $\mathrm{I}_{\mathrm{d}}=4 \mathrm{~A}$ ).


Figure 5.27
IRC830 Drain Voltage Falling and Rising Edge - Without use of Kelvin Contact ( 50 V/Div. $20 \mathrm{~ns} /$ Div.).

Rise time ( $10-90 \%$ ) is approximately 10 ns , only slightly faster than turn on. The rate of rise of drain voltage (and therefore fall of drain current) is seen to slow appreciably and reverse, but this time at $\dot{\boldsymbol{V}}_{d}=250 \mathrm{~V}$. This result conflicts with that obtained with the modified IRF450 and, incidentally, with the IRC830 when switching lower current levels, where the effect of source feedback at turn off was negligible.

The voltage developed across the source bonding wire and lead when switching 17 A is shown in Figure 5.28. At turn on, the source voltage peaks at 13 V , which will, in turn, be reflected at the gate, thus current is drawn out of the gate since the gate voltage is now above the driving voltage, hence the device starts to turn off momentarily. This momentary turn off, or reduction in drain current can be observed by noticing the slight negative voltage transient measured at the source. As the source voltage falls, the drive circuit is able to resume charging the gate and the drain current begins to rise again (observed by the second transient measured at the source). This time the rate of rise of drain current is insufficient to cause the gate voltage to rise above the level of the available drive voltage.

At turn off the voltage developed across the source inductance due to falling drain current coincides with that caused by the gate drive current. (In the case of the IRF450 there is a 20 ns delay between the peak gate current and turn off initiation of the device).


Figure 5.28 IRC830 Source Voltage - Switching 300 V, 17 A. ( 5 V/Div. $20 \mathrm{~ns} /$ Div.)

It is thought to be the fact that these source transients coincide, i.e. as charge is still being withdrawn from the gate, that results in turn off being affected by source feed back in the same way as turn on. The peak voltage developed is some 15 V negative which will cause current to flow into the gate (since the n channel drive transistor will still be conducting) resulting in the drain current rising momentarily. Again as the rate of fall of drain current reduces (and in fact reverses) the drive circuit is able to resume discharging the gate and the device completes turn off. However, unlike at tum on, there is no sustained slow down in the rate of rise of drain voltage and after the initial transient, the rate of rise of drain voltage (and therefore fall of drain current) is little reduced to that before the transient.

The drain voltage falling and rising edge when employing the kelvin contact are shown in Figure 5.29 . Fall time ( $10-90 \%$ ) is approximately 5 ns , which is 2 ns slower than when switching a lower current of 6.4 A but over twice as fast as when switching without the use of a second source terminal. There is a slight slow down in the rate of fall of drain voltage at $v_{d}=175 \mathrm{~V}$ which is recovered and again at $v_{d}=60 \mathrm{~V}$ just above $V_{\text {dromos }}$. These effects are probably caused by source feedback due to the distributed inductance of the source metalisation and the bulk source resistance.

Rise time ( $10-90 \%$ ) is 3.8 ns . There is only a very slight slow down in the rate of rise of drain voltage at $v_{d}=225 \mathrm{~V}$ which has probably the same causes as those described for turn on.


Figure 5.29 Drain Voltage Falling and Rising Edge for IRC830 - With Use of Kelvin Contact ( 50 V/Div. 20 ns/Div.).

Again, comparison of Figures 5.29 and 5.27 demonstrates the considerable improvement in switching performance resulting from isolating the power and drive source connections.

### 5.2.1.2 IRC530 Switching Waveforms

Switching waveforms for the IRC630 and IRC530 are similar and so only those for the IRC530 are discussed.

Figure 5.30 shows the falling and rising edge of the IRC530 drain voltage waveform when switching $100 \mathrm{~V}, 13 \mathrm{~A}$ and when not employing the kelvin contact as a drive retum. Fall time is of the order of 12 ns. An abrupt decrease in the rate of fall of drain voltage (and therefore rise of drain current) is seen 4 ns after turn on is initiated when $v_{d}$ has fallen to 50 V . Rise time at turn off is of the order of 3.7 ns and appears not to be affected by source feedback.

Figure 5.31 shows the device source voltage transients during switching. The peak voltage at the source is 9 V , occurring some 10 ns after turn on is initiated. This reduces the available drive voltage from 14 V to 5 V which in turn reduces the rate of rise of drain current. If the source voltage is monitored at the entrance of the source lead to the package rather than by means of the kelvin contact, the amplitude of the source voltage transients is some $50 \%$ lower. This indicates that the bonding wire inductance is a major contributor to source inductance and therefore source feedback.


Figure 5.30
Drain Voltage Falling and Rising edge for the IRC530Without use of the Kelvin Contact ( 20 V/Div. $20 \mathrm{~ns} /$ Div.).


Figure $5.31 \quad$ Voltage Developed Across IRC530 Source Lead - When Switching 100 V, 13 A (5 V/Div. $20 \mathrm{~ns} /$ Div.).

Turn off is of more interest. This time there is a delay of 8 ns between the gate current induced source transient and that caused by the falling drain current. Since turn off is delayed until virtually all the charge has been removed from the gate, the negative voltage transient at the source, caused by the rapidly falling drain current, does not affect the turn off speed which, instead, is wholly governed by the time constant of the load resistance and device output capacitance. That is rise time, $t_{r}=2.2 R_{L} C_{\text {ors }}$. Taking typical figures for $C_{\text {ous }} t_{r}=3.96 \mathrm{~ns}$. Measured rise time is 3.66 ns .

This is similar to the result obtained for the modified IRF450, but not for the IRC830. Hence the delay in turn off is a function of the device current handling capability and therefore channel width and therefore output capacitance. That is for higher current types, the higher output capacitance, in association with the load resistance, delays the interruption of drain current until after the gate has discharged to below its threshold voltage.

Finally, the drain voltage falling and rising edge of the IRC530 when using the kelvin contact is shown in Figure 5.32. Fall and rise times are 7.5 ns and 3.5 ns respectively.


Figure $5.32 \quad$ Falling and Rising Edge of IRC530 Drain Voltage - When Using Kelvin Contact (50 V/Div. $20 \mathrm{~ns} /$ Div.)

To conclude, high speed switching tests on International Rectifier's range of current sensing MOSFETs has shown that use of the kelvin contact as a separate source terminal for drive purposes improves switching speed by reducing source feedback effects. In the case of the high voltage, low current device, the IRC830, both turn on and turn off times are affected. With the lower voltage, higher current devices such as the IRC630 and IRC530 only turn on times are improved, turn off being unaffected by source feedback, with or without the use of a separate source connection.

### 5.2.2 Current Sensing MOSFET Applied to HF Switching Inverter

The results of the high speed switching tests on current sensing MOSFETs show that a substantial increase in switching speed can be obtained when the kelvin contact is used as a drive return, thus isolating power and drive source connections. To test this further in a practical application, a $150 \mathrm{~W}, 7 \mathrm{MHz}$ Class E inverter was constructed using the IRC630 as the main power device. A circuit diagram of the inverter is given in Figure 5.33.


Figure 5.33 Circuit Diagram of $150 \mathrm{~W}, 7 \mathrm{MHz}$ Class E Inverter.
The circuit was constructed on a colander ground plane prototyping board, drive and power circuit earth planes were separated by removing a strip of the colander ground plane, effecting isolation. The transistor was mounted on a heat sink to which the circuit board was bolted. The transistor drain connection was made by means of a solder tag, soldered directly to the drain tab of the transistor to reduce stray inductance.

The power circuit and drive circuit were isolated, with floating supplies used in both cases. The kelvin contact was used for the drive return, and was connected to the drive circuit ground plane, the conventional source lead was connected directly to the power side ground plane. Thus, apart from stray capacitances, the only connection between the drive and power inverter circuitry was the source metalisation of the power MOSFET. The general construction, showing estimated stray capacitances, is shown in Figure 5.34.


Figure 5.34 Construction Sketch of 7 MHz Inverter.
Further design details of this inverter, using a standard IRF630 to produce up to 200 W at 7 MHz are given in Chapter 6 and can also be obtained from the following references: Hinchliffe et al. 1988 b and 1988c.

One other advantage envisaged by using a current sensing MOSFET was that the current sensing facility could be used to monitor the source current allowing over current fault conditions to be detected. The inverter could then be disabled on detection of excessive source current, thus providing a degree of protection against load mismatch or supply transients.

### 5.2.2.1 MOSFET Failure and Analysis

When applying power to the inverter at low supply voitage levels, the current sensing MOSFET appeared to work well in its unconventional mode of connection. Drain voltage and output waveforms are shown in Figure 5.35 for the inverter producing 41 W into $50 \Omega$, at a supply voltage of 25.6 V and supply current of 1.67 A, efficiency of conversion being approximately $95 \%$.

On increasing the supply voltage the MOSFET failed short circuit, drain to source, as peak drain voltage reached 100 V , the device was replaced and the inverter tested for a prolonged period (in excess of 1 hour) at the previous supply voltage without any ill effects, steady state transistor case temperature being $40^{\circ} \mathrm{C}$. Again, as the supply voltage was increased, the device failed short circuit drain to source, with the gate circuit remaining intact.


Figure 5.35
Waveforms of 7 MHz Class E Using IRC630
Upper Trace - Drain Voltage ( 50 V/Div. $50 \mathrm{~ns} /$ Div.);
Lower Trace - Output Voltage ( 50 V/Div. $50 \mathrm{~ns} /$ Div.).
After a certain amount of investigation it was found that by connecting the drive and power earth planes together by means of a copper strip soldered close to the source connections for the MOSFET, the inverter could successfully be run at output powers in excess of 150 W at 7 MHz , again the reader is referred to Chapter 6.

The failed devices were analysed by International Rectifier, and the packages opened to examine the junction area. It was discovered that the source metalisation had melted between the source pad and the sense pad in the area of the kelvin contact pad. A photograph taken of the damaged area is shown in Figure 5.36. It was concluded that the failure was caused by lateral current flow between the main source pad and the kelvin source pad sufficient to melt the source metalisation. The gate aluminium bus bars which link the polysilicon gate overlay limit this lateral current to the localised area seen. There are also signs of considerable thermal stress originating from the kelvin pad which was sufficient to cause a crack in the die. This can be seen running across the comer of the sense pad, round the sense cells and off to the edge of the chip. It is probable that at the instant of failure, additional stress was applied to the sense cells.


Figure 5.36 Damaged Area of MOSFET die: Magnification - X 50.
Since the inverter would run for extended periods at power levels up to 40 W when using the kelvin contact, it can be assumed that the kelvin contact is sufficient to carry the required gate drive current at duty cycles up to $50 \%$. Because the devices all failed at higher power levels, and since linking the ground planes cured the problems, it appeared that failure was caused by high RF currents flowing from the power circuit to the drive circuit and back to the power circuit via the device source connections (Hinchliffe et al. 1989a).

When using the kelvin contact at low duty cycles, as with the switching tests, the heating effect of this RF current would be minimal and heat dissipated into the structure of the die, but under continuous operation at high supply voltages the localised heating will cause the damage seen.

Thus at higher power levels, an RF current path is established from the power circuit to the drive circuit, via a capacitive link and back from the drive circuit to the power circuit via the kelvin contact, the source metalisation of the chip and the source lead. With reference to Figure 5.34, there are no stray circuit capacitances sufficiently large to allow high RF current flow between the power and drive ground planes, nor sufficient RF potential between these planes to cause a large RF current flow. Hence this RF current must be attributed to the reverse transfer capacitance of the MOSFET which is charged and discharged by the drain voltage swing during normal Class E operation. The main RF current paths linking the power and drive circuits are shown in Figure 5.37.


Figure 5.37 Stray RF Current Paths of Current Sensing MOSFET.
The r.m.s. current through the reverse transfer capacitance is given by the following formula (derived in Appendix VIII):

$$
\begin{equation*}
I_{c_{L_{4} m u}}=\frac{C_{d g}}{C_{1}} \times \frac{V_{o(\max )}}{R_{L}} \times 0.5675 \tag{5.3}
\end{equation*}
$$

Where: $\quad$\begin{tabular}{ll}

$V_{\alpha \text { max }}$ \& | is the maximum load voltage; |
| :--- |
| $R_{\mathrm{L}}$ | <br>


$C_{I}$ \& | is the load resistance; |
| :--- |
| is the extemal shunt capacitance |
| in the Class E inverter. |

\end{tabular}

For a supply voltage of 45 V , sufficient to produce 200 W into $50 \Omega$, the r.m.s. current through the reverse transfer capacitance and thus through the source metalisation is:

$$
I_{c_{4 / \mathrm{mu}}}=\frac{120 \times 10^{-12}}{760 \times 10^{-12}} \times \frac{141}{50} \times 0.5675=0.45 \mathrm{~A}
$$

This is not a large current for a power semiconductor to carry and it can only be assumed that the source metalisation between the kelvin and source contacts has a high RF resistance.

### 5.2.2.2 PSpice Simulation of Inverter

To back up the theoretical calculations, the circuit was simulated using PSpice. To allow analysis of the current flow through the MOSFET parasitic capacitances, the MOSFET was constructed using the PSpice ideal switch model and lumped parasitic components. The PSpice circuit model is shown in Figure 5.38 and the PSpice simulation program listing is given in Appendix VI.


Figure 5.38 Simulation Circuit of $150 \mathrm{~W}, \mathbf{7 M H z}$ Inverter.
The simulated drain voltage, ouput voltage and switch current waveforms for the inverter delivering 200 W into a $50 \Omega$ load are shown in Figure 5.39 and depict typical Class E operation. Close inspection reveals that operation is not quite ideal; the MOSFET switch turns on after the zero $\mathrm{d} v / \mathrm{d} t$ region of drain voltage but this is not sufficient to disturb high efficiency operation, or to result in a large departure from the ideal waveforms (the reader is referred to Figure 3.10 section 3.2). Simulated efficiency is approximately $91 \%$.

The current through the reverse transfer capacitance, which is identical in shape to the shunt capacitor current, is shown in Figure 5.40. The r.m.s. value of this current calculated by Probe ${ }^{8}$ is approximately 0.47 A which is in close agreement with the theoretical calculation.

LASS E 7MHz 2OOH SIMULATION USING SWITCH MODELS


Figure 5.39 Simulated Drain, Output Voltage and Switch Current Waveform in 7 MHz Inverter.


Figure 5.40 Simulated Reverse Transfer Capacitor Current in $\mathbf{7} \mathbf{~ M H z}$ Inverter.

One final point worthy of note which has been brought to light by this work is that when operating power MOSFETs at high frequencies in resonant inverters/converters, the current flow through the reverse transfer capacitance during the off period is not insignificant. Thus when designing the drive circuit, the turn off transistors must be capable of sinking tis current without excessive volt drop.

### 5.3 Switching Tests on RF Packaged MOSFETs

To conclude this section of work, switching tests were performed on an RF packaged power MOSFET: the DE501N12; and on an RF power MOSFET: the MRF150.

### 5.3.1 The DE501N12

In April of 1987 Directed Energy Corp. of the USA announced the launch of a commercially available power MOSFET housed in a microwave stripline package (Krausse 1987). A number of devices are available and one was chosen for analysis; the DE501N12 costing approximately $£ 120$ at 1988 prices. This device houses two Siliconix manufactured $\mathbb{R} 8840$ power MOSFET dice mounted on a Beryllium Oxide substrate with strip terminals used for gate, source and drain connections. Four source terminals are provided, two to each die, one pair being used for drive circuit connections and the other pair for power circuit connections. Thus not only are lead inductances reduced by use of strip line terminals, but also source feedback effects are virtually eliminated by the isolation of the drive circuit and power circuit grounds. The device has similar ratings to the power MOSFET type IRF450; input, output and reverse transfer capacitance are slightly lower due to the improved packaging of the device over a 03 style package. However, the device ratings and gate drive requirements are close enough to those of the IRF450 to allow direct comparison with the IRF450 switching tests detailed above.

The switching test circuit used was of identical design and construction to that used in tests on the modified IRF450 allowing direct comparison of results. It should be added though that the switching test circuit used is not capable of achieving the peak switching performance from the device quoted by the manufacturers (Krausse 1987) that is $500 \mathrm{~V}, 10 \mathrm{~A}$ in 1.5 ns . The switching circuit used by Direct Energy is highly specialised and employs modified RF bipolar transistors in strip line packages. Also a gate drive voitage of 25 V is used to enhance switching performance. Thus the results reported here are intended for comparison with the IRF450 switching times obtained and not to ascertain peak switching performance of the device.

Throughout the tests the gate pulse duration was held to 60 ns and the gate drive was held to 14 V as in previous tests. Drain and gate voltages were measured at the entrance of the leads to the package, coaxial probe sockets being used to reduce probe earth lead inductance effects to a minimum.

The gate drive waveform with no applied drain voltage is shown in Figure 5.41. The overshoot measured is some $50 \%$ less than that measured for the RF450 package. This is an indication of the reduction in lead parasitic inductance obtained in the RF package. Also the ringing amplitude of the gate voltage after turn off is much lower than that of the IRF450. Details of rise and fall times and voltage levels of the gate drive are given in Table 5.3 along with those for the modified IRF450 for comparison.


Figure 5.41
Gate Drive Waveform for DE501N12 (5 V/Div. 20 ns/Div.).

| Table 5.3 <br> Comparison of Gate Drives for DE501N12 and Modified IRF450. |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  | DE501N12 |  | Modified IRF450 |  |
|  | Rising edge | Falling <br> Edge | Rising <br> Edge | Falling Edge |
| Time taken to reach plateau region | 6.0 ns | 8.4 ns | 6.0 ns | 11 ns |
| Time taken to traverse plateau region | 9.8 ns | 11.3 ns | 14 ns | 14 ns |
| Time for 10-90\% Rise/Fall | 35.6 ns | 22.2 ns | 36 ns | 24 ns |
| Voltage level of plateau region | 5.44 V | 3.08 V | 8.4 V | 6.5 V |

The device was tested for drain current levels of 12 A and 25 A ; for brevity only the 25 A tests are described in detail.

The drain voltage falling and rising edge when switching 25 A and 300 V are shown in Figures 5.42 and 5.43 respectively. Fall time is approximately 5.5 ns which is 1.3 ns slower than when switching 12 A , 300 V and 2 ns faster than the modified RF 450 under the same operating conditions. Rise time is 5 ns , 1 ns slower than the modified IRF450 and again is governed by the step response of the output network. Overshoot at turn off is approximately 50 V indicating that the load circuit is under damped, the ringing frequency being 100 MHz which suggests that stray lead inductance in the drain circuit is similar to that of the modified IRF450. Switching times for the microwave packaged power MOSFET and the modified IRF450 are given in Table 5.4.

| Table 5.4 <br> Comparison of Switching Tests for Modified IRF450 and Microwave Packaged DE501N12. |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Drain <br> Current <br> A | Load <br> Resistance $\Omega$ | Drain Voltage Fall Time ns |  | Improvement \% | Drain Voltage Rise Time ns |  |
| $V_{\mu}=300 \mathrm{~V}$ |  | Modified IRF450 | DE501N12 |  | Modified IRF450 | DE501N12 |
| 12 | 27 | 5 | 4 | 20 | 6.5 | 6.9 |
| 25 | 12 | 7.5 | 5 | 50 | 4 | 5 |

Figure 5.44 shows the drain voltage falling and rising edge superimposed on the gate voltage. Again there is a delay between the gate voltage falling below threshold and the drain voltage rising at turn off. The positive going transient observed on the gate waveform just before the plateau region, observed here and in Figure 5.41, is due to voltage developed across the gate and drive source connections caused by the rapidly rising gate current. This point is misinterpreted by Krausse (Krausse 1987). The frequency and amplitude of the gate voltage ringing were both observed to increase with supply voltage for a given load, and load current, for a given supply voltage. This indicates that energy is transferred into the gate circuit via the reverse transfer capacitance on turn off, providing a degree of positive feedback. This is corroborated by the fact that momentary conduction after turn off of the device due to gate circuit ringing is greater when conducting 25 A than when conducting 12 A . There is little difference in the gate voltage waveform whether switching zero current, 12 A or 25 A except that the plateau region is seen to extend for the higher current levels and, as mentioned, the frequency and amplitude of ringing of the gate voltage waveform after turn off are slightly higher.


Figure $5.42 \quad$ Falling Edge of DE501N12 Drain Voltage: $V_{d}=300 \mathrm{~V}, I_{d}=25 \mathrm{~A}$ ( $>50 \mathrm{~V} /$ Div. $5 \mathrm{~ns} /$ Div.).


Figure $5.43 \quad$ Rising Edge of DE501N12 Drain Voltage: $V_{d}=300 \mathrm{~V}, I_{d}=25 \mathrm{~A}$ ( $>50 \mathrm{~V} / \mathrm{Div} .5 \mathrm{~ns} /$ Div.).


Figure 5.44 Rising and Falling Edge of DE501N12 Drain Voltage Waveform Superimposed on Gate Yoltage Waveform: $V_{\omega}=300 \mathrm{~V}, I_{d u}=25 \mathrm{~A}(50 \mathrm{~V} / \mathrm{Div} .5 \mathrm{~V} / \mathrm{Div} .20 \mathrm{~ns} /$ Div. $)$.

### 5.3.2 The MRF150

To conclude this section of work, switching tests were performed on Motorola's MRF150. This is an RF power MOSFET designed to be used in high frequency linear amplifiers between 3 and 30 MHz (the reader is referred to Chapters 3 and 4 for further information on the use of the MRF150 in linear amplifiers). It has a breakdown voltage of 125 volts and continuous current rating of 16 amperes. Radio frequency power MOSFETs are optimised for operation at higher frequencies, thus the reverse transfer capacitance and output capacitance are much smaller than comparable power MOSFETs. Like the DE501N12 it is housed in a strip line package and has two source connections.

To allow comparison with the previous investigations into switching speed, the same design of drive circuit was used and the gate drive pulse was held to 14 V and 60 ns.

Initial tests produced a self oscillation of approximately 34 MHz (Figure 5.45) for supply voltages above 40 V . This is a classic example of the gate circuit self resonating with positive feedback being supplied by the reverse transfer capacitance (Bullough et al. 1982, Severns et al. 1988). Radio frequency power MOSFETs have an aluminium gate structure to improve RF performance, this increases the $Q$ of the gate network over polysilicon gate structures. Thus the RF MOSFET gate has far greater tendency to sustain self oscillation than power MOSFETs.


Figure $5.45 \quad$ MRF150 Exhibiting Self Oscillation.
Upper Trace - Gate Drive (5 V/Div. 20 ns/Div.) Lower Trace - Drain Voltage (20 V/Div. $20 \mathrm{~ns} /$ Div.)


Figure 5.46 MRF150 Drain Voltage Rising and Falling Edge: $V_{d 山}=100 \mathrm{~V}, I_{d}=20 \mathrm{~A}(20 \mathrm{~V} / \mathrm{Div} .20 \mathrm{~ns} / \mathrm{Div}$.$) .$

To prevent oscillation, a gate resistance of $4.7 \Omega$ was employed, lower gate resistance values being insufficient to completely damp oscillations. The resulting switching performance is shown above in Figure 5.46. Fall time of the drain voltage is approximately 5 ns for a drain supply of 100 V and drain current of 20 A . Again turn off is delayed with respect to the gate drive falling below threshold and is govemed by the time constant of the load and output capacitance; drain voltage rise time being 3.84 ns. The inclusion of the $4.7 \Omega$ gate resistor increases turn on time by approximately 1.5 ns or $40 \%$. Turn on time for the RF power MOSFET is some 3.5 ns (or $70 \%$ ) faster than the comparably rated standard power MOSFET in a TO220 package (the IRC630), however the MRF150 is some ten times more expensive than the standard power MOSFET.

## $5.4 \quad$ Conclusions

An improvement in tum on time for an $\mathbb{R F} 450$, switching rated continuous current, in excess of two to one has been achieved by modifying a TO3 packaged device to include a second source lead. This demonstrates the considerable limiting effects of source lead inductance on switching performance.

Turn off time, though, is unaffected by source feedback (except at high pulsed currents) due to the delay between the gate drive falling edge and the initiation of fall in drain current. This effect is thought to be a function of the rate at which the output capacitance is charged by the load.

PSpice simulation results closely agree with practical measurements except for turn off time prediction. This is thought to be due to the fact that the power MOSFET model in PSpice does not incorporate a varactor effect for the reverse transfer capacitance.

The use of the kelvin contact in current sensing MOSFETs as a separate source lead improves switching performance in a similar manner and works well in low duty cycle, pulsed applications. However, lateral RF current flow through the source metalisation between the kelvin and source pad when operating at high duty cycles and high power levels destroys the devices. This suggests that the drive source and power source leads should be bonded to the same source pad.

Tests on an RF packaged power MOSFET have shown that the major improvement in switching performance results from the use of a second source terminal, eliminating source feedback. Use of strip line RF packaging techniques gives a further improvement but these are insufficient to justify the extra cost of the device. When using an RF power MOSFET, the MRF150, which has an aluminium gate structure as opposed to polysilicon, gate resonance become more pronounced resulting in self oscillation of the device.

It was again demonstrated that for high current devices, turn off is largely independent of the gate drive speed and is determined by the time constant of the output network.

This result would tend to suggest that in the Class E circuit, where rapid turn off of drain current is required, the rising drain current at turn on being sinusoidal, exotically packaged devices are not required other than at operating frequencies in the upper HF band, i.e. approaching 30 MHz .

## Chapter 6

## HIGH FREOUENCY INDUCTION HEATING PROTOTYPES

There are many applications in high frequency induction heating ( $1-10 \mathrm{MHz}$ ) where small, solid state supplies would be advantageous over present thermionic valve equipment. This section describes two solid state prototypes, a $500 \mathrm{~W}, 3.3 \mathrm{MHz}$ unit and a $150 \mathrm{~W}, 7 \mathrm{MHz}$ unit.

HIGH EREQUENCY INDUCTION HEATING PROTOTYPES
For supplies operating at frequencies below 1 MHz , standard converter/inverter configurations such as Buck, Cúk, voltage fed resonant and current fed resonant are generally quite adequate for the majority of applications. However, when operating above 1 MHz at power levels above a few tens of watts, switching losses and stray parasitic components limit the suitability of such configurations. Although the operating frequencies of Cük and Buck/Boost converters can be increased by the use of quasi resonant switch techniques (Lee 1987), a configuration more applicable to high power electric process heating applications is the Class E inverter (amplifier) developed in the 1970's by the Sokals (Sokal et al. 1975).

The Class E is highly suitable for high frequency d.c. to a.c. inverters for several reasons:

The Class E inverter load network minimises simultaneous high voltage and high current stress during switching transients by tailoring voltage and current waveforms such that the voltage across the active device rises after the current though it has fallen to zero and current through the device rises after the voltage has fallen to zero. Also, at the switching instant, the voltage slope is approximately zero allowing some tolerance for operating frequency and switching time.

It has advantages over traditional linear amplifiers (Class B, Class C) in that it is largely insensitive to component tolerances, particularly the active switching element characteristics.

The advartages accruing from Class E operation are not without penaity; there are a number of fundamental disadvantages. Although the switching element is not subject to simultaneous high current and high voltage stress, it is subject to current and voltage stresses considerably higher than occur in conventional resonant inverters. The maximum voltage ( $v_{\text {dmaxi }}$ ) impressed across the switch in relation to the supply voltage ( $V_{d d}$ ) can be high. $V_{\alpha(\max )}$ can reach values greater than $4.5 V_{d d}$, especially when operation is sub optimum. Further, when conducting, the current through the switch can reach values in excess of three times the supply current $\left(I_{d 4}\right)$. Under optimum operation with ideal components the peak voltage imposed across the switch is $3.56 \mathrm{~V}_{d d}$ and the peak collector current is $2.86 I_{d d}$

A further disadvantage is that the Class $E$ inverter has little tolerance to excessive load mismatch particularly for load impedances higher than nominal. However, in high frequency induction heating applications, typical load variations result in a lowering of the load impedance by a factor of two. This load variation is quite acceptable to the Class E inverter with little lowering in efficiency. Investigations have been undertaken into microprocessor control of a Class E unit, allowing a wide variation of load impedances to be matched to the unit and thus improving the flexibility of the induction heating power source (Hinchliffe et al. 1987g, 1988h).

### 6.1 Design Construction and Testing of Prototypes

The equations used in the design of the prototypes are given in Appendix III. For all the Class E inverters described here and in the following chapter, the computer program mentioned in Chapter 4 section 4.2.1 and listed in Appendix IV was used to compute the required Class E circuit component values.

In most high frequency electric process heating systems it is convenient to deliver the power to the load via a characteristic impedance transmission line, often a $50 \Omega$ transmission line. In order to drive into $50 \Omega$, a matching network usually needs to be placed between the Class E inverter section and the oupput. For circuits where a degree of tolerance in the operating frequency is recquired, a wide-band RF transformer provides the most efficient method of impedance transformation (Ruthroff 1959). For fixed frequency inverters a capacitor matching network provides an alternative solution (Krauss et al. 1980).

### 6.1.1 Choice of $\boldsymbol{Q}$ Value

The size of the oupput inductor, $L_{2}$, depends upon the required $Q$ factor of the Class E circuit. The required $Q$ value depends to a large degree on the application for which the Class E circuit is to be used. The higher the value of $Q$, the lower the level of harmonic components of the fundamental operating frequency at the output and the more narrow band the Class E amplifier. There are a number of trade-offs to be made in choosing the value of $Q$.

Firstly, for a given load, the value of $L_{2}$ increases with $Q$. The energy dissipated in this component increases with its value, owing to greater winding and core loss, and thus the overall efficiency of the inverter is lowered.

Secondly, ideal operation for the circuit requires that the $Q$ of the output network be sufficiently high such that the drain voltage is carried to zero before the device switches on. If the $Q$ is too high the drain voltage is taken negative, causing the integral reverse diode in the MOSFET to conduct. Usually this is not dangerous, since current commutation is from the diode to the MOSFET, allowing one half switching cycle to elapse for minority carriers in the parasitic bipolar junction transistor of the MOSFET to recombine. However, if the reverse current duration and value are too high, then minority carriers could still be present at turn off which may cause dv/dt breakdown (Severns 1984). Further, this diode conduction causes increased losses in the switch, again reducing overall efficiency as well as increasing device stress.

If the value of $Q$ is too low then the drain voltage fails to reach zero before turn on, that is the zero $\mathrm{d} v_{d} / \mathrm{d} t$ slope occurs above 0 V . If the level of the zero $\mathrm{d} v_{d} / \mathrm{dt}$ slope is above 0 V then $1 / 2 C_{1} V_{d d}^{2} f$ losses will occur in the MOSFET due to $C_{1}$ being discharged through the device at turn on. This again reduces efficiency and increases device stress. A theoretical minimum value for $Q$, in order to maintain Class E operation, is approximately 1.8 (Sokal et al. 1980). Experience has shown that, allowing for non ideal components (switching device loss, capacitor and inductor loss), a design value of $Q=5$ provides a reasonable compromise.

### 6.1.2 Choice of Active Device

Two main factors affect the choice of active device in terms of its voltage and current rating. Since the power MOSFET is intolerant to over voltage stress, devices must be chosen with a breakdown voltage of approximately five times the required supply voltage to allow for non ideal operation, supply line transients etc. The required supply voltage, for a given output power, depends upon the load resistance, the higher the load resistance, the higher the required supply voltage and therefore the higher the device breakdown rating required.

It is not always possible to choose a device which has sufficiency high breakdown voltage and yet low on resistance (for high efficiency operation) and low input capacitance (for ease of drive). A more fundamental disadvantage is that, for a given frequency, the higher the operating voltage, the lower the value required for the shunt capacitor $C_{1}$. At high frequencies this value can be below the parasitic output capacitance of the device. Although, for a given die size, device output capacitance falls with breakdown voltage; the rate at which the required shunt capacitor value falls, with respect to supply voltage, is greater than the rate at which device output capacitance falls.

## Variation of shunt capacitance with load in Class $\mathrm{E} 600 \mathrm{~W} Q=5$



Figure 6.1 Plot of Shunt Capacitance Values against Drain Voltage (Load Resistance).

This can be more clearly explained by reference to Figure 6.1 (above). Here the required shunt capacitances for a 600 W Class E inverter are.plotted for operating frequencies between 5 and 20 MHz and for different load resistance values (and therefore peak drain voltages). Also, the output capacitance for the International Rectifier Hex 5 chip size (capable of producing 600 W in a Class E inverter) is plotted for different drain-source breakdown voltages. As can be seen, although the device output capacitance falls with increased drain voltage capability, the output capacitance required at a given operating frequency falls more rapidly with increased load resistance (and therefore peak device voltage). For an operating frequency of 5 MHz , the required output capacitance approaches, asymptotically, the Hex $5 C_{o s s}$ line; at an operating frequency of 10 MHz , the Hex $5 C_{\text {oes }}$ exceeds the required shunt capacitor value at peak drain voltage levels of 250 V (load resistance of $6 \Omega$ ) and so on.

This trade-off between peak drain voltage, output capacitance and required shunt capacitor value necessitates the use of relatively low voltage, high current devices. The Class E stage being matched to the load via an impedance matching network as described previously.

The current rating of the MOSFET must be chosen in relation to the r.m.s. value of the current flowing through the device. It is not sufficient to match the peak drain current to manufacturer's quoted pulse current capability of the MOSFET since the current carrying limitations of power MOSFETs is governed by device power dissipation.

Assuming negligible drain current fall time, the current through the active device during conduction is given by (Kazimierczuk 1983):

$$
\begin{equation*}
i_{d}(\omega t)=I_{d \alpha}\left(\frac{\pi}{2} \sin \omega t-\cos \omega t+1\right) \quad 0<\omega t \leq \pi \tag{6.1}
\end{equation*}
$$

Where: $\omega=2 \pi f, f$ being the frequency of operation.

The r.m.s. current through the active device (derived in Appendix IX) is given by:

$$
\begin{equation*}
I_{d(m u t)}=\left(\frac{1}{2 \pi} \int_{0}^{\pi}\left(i_{d}(\omega t)\right)^{2} d \omega t\right)^{\frac{1}{2}} \tag{6.2}
\end{equation*}
$$

Solution of this yields:

$$
\begin{align*}
& I_{d(\mathrm{~mm})}=I_{d x}\left(\frac{\pi^{2}}{16}+\frac{7}{4}\right)^{\frac{1}{2}}  \tag{6.3}\\
& I_{d(\mathrm{mv})}=1.54 I_{d d} \tag{6.4}
\end{align*}
$$

The power dissipated in the MOSFET is simply:

$$
\begin{equation*}
P_{d}=2.377_{d d}^{2} R_{d(a n)} \tag{6.5}
\end{equation*}
$$

The calculated device rms. current can be related to the manufacturer's quoted maximum continuous current rating in order to select the required device. A figure of $I_{d}$ continuous $=1.5 I_{d d}$ is a close approximation.

Two prototypes were developed; a $500 \mathrm{~W}, 3.3 \mathrm{MHz}$ unit which has direct commercial application and a $150 \mathrm{~W}, 7 \mathrm{MHz}$ unit which can be considered as an intermediary between an induction heating and a dielectric heating supply. The frequency of 7 MHz is often used in applications such as the generation of induction coupled plasma, at power levels above 5 kW , and in metal spluttering applications at power levels of in the region of 1 kW .

### 6.1.3 The 3.3 MHz Prototype

Two increasing applications in high frequency induction heating are those of fibre optic production and cap sealing for tamper-proof packaging. Both of these application areas have grown in industrial significance in the past five years. Cap sealing especially is suitable for solid state power sources because it requires high frequency, relatively low power and ease of carriage is an advantage.

The process of cap sealing involves the heating of an aluminium disk inside the cap of a plastic container whilst the bottle or container passes beneath the induction coil. The aluminium foil is thus welded to the lip of the bottle, forming a tamper-proof seal. In order to obtain good coupling to the aluminium disk, an operating frequency of 3.3 MHz is often used, with power levels ranging from 250 W to 2 kW .

### 6.1.3.1 Design of the 3.3 MHz 500 W Prototype

The active device chosen for the $500 \mathrm{~W}, 3.3 \mathrm{MHz}$ prototype was the TO3P packaged IRF450 having a 500 V breakdown voltage, 8 A current carrying capability (at $\mathrm{T}_{\mathrm{c}}=100^{\circ} \mathrm{C}$ ), 2800 pF input capacitance ( $C_{i s t}$ ) and 600 pF ouput capacitance ( $C_{\text {ous }}$ ) (Maximum values).

Application of the design equations in Appendix III yield:

$$
\begin{aligned}
& C_{1}=810 \mathrm{pF} \\
& L_{2}=3 \mu \mathrm{H} \\
& C_{2}=1 \mathrm{nF} \\
& L_{1}=30 \mu \mathrm{H} \\
& R_{L}=12.5 \Omega
\end{aligned}
$$

Again, $C_{1}$ is made up of a typical value for the device output capacitance and an extemal shunt capacitor. The required voltage rating for $C_{1}$ and $C_{2}$ is 500 V , the r.m.s. current carrying capability of $C_{2}$ must be in excess of 6.5 A at 3.3 MHz . The capacitor types used were Unilator power RF ceramics type 103. The 500 W Class E inverter circuit diagram is shown in Figure 6.2.


Figure $6.2500 \mathrm{~W}, 3.3 \mathrm{MHz}$ Class E Inverter Circuit Diagram.
To match the output of the Class E stage to the $50 \Omega \mathrm{RF}$ load, a $500 \mathrm{~W} 1: 4$ impedance ratio transformer was constructed by winding 20 turns of a $25 \Omega$ transmission line (consisting of twisted 1.6 mm diameter enamelled wire) on a high frequency iron powder toroid (SEI type G1 grade 17) of diameter 58 mm .

This type of RF power transformer utilises the transmission line properties of the windings to assist transfer of power from primary to secondary. It is constructed as a modified auto transformer, such that leakage flux from one winding is in opposition to that of the second, thus minimising leaking

[^6]inductance. This construction method has a further advantage of reducing skin effects in the windings (Ruthroff 1959, Pitzalis 1967, Hilbers 1970, Sevick 1976). The resulting construction is shown in Figure 6.3.


Figure 6.3 Construction of $3.3 \mathrm{MHz}, 500 \mathrm{VA}$ Transformer.
The supply inductance, $L_{\mathrm{l}}$, consists of 35 turns of 1.6 mm diameter enamelled copper wire wound on an SEI Genelex core type V of diameter 32 mm . The output inductor originally consisted of 14 tums if Litz wire on an SEI high frequency iron powder core type G29 grade 33. However, the measured $Q$ of this coil was 60 giving an equivalent series resistive element of $1.1 \Omega$ resulting in a power loss of 40 W at full power. A second coil was constructed using a minimum wire length technique for air cored toroidal inductors (Murgatroyd et al. 1985).

The design equations for the minimum wire length inductor are given in the above reference and in Appendix X. Since the design involves an iterative procedure a BASIC program was written to calculate the required coil dimensions, wire length and diameter etc., the program listing is given in Appendix IV. The resulting coil has a measured $Q$ of 200 , giving a power loss of 11 W at full output power, temperature rise of the windings being approximately $70^{\circ} \mathrm{C}$.

## Design of 3.3 MHz Driver

For 3.3 MHz operation, the switching time of the device should be under 22 ns . The amount of charge flowing into and out of the gate during switching for an $\operatorname{RF} 450$ is approximately 50 nC at a gate voltage of 7 V . The current required to be sourced by the drive transistors during switching is calculated using Equation 6.6, and is 2.3 A .

$$
\begin{equation*}
I_{\text {drive }}=\frac{Q_{8(\text { platanu) }}}{t_{\text {platant }}} \tag{6.6}
\end{equation*}
$$

Where: $\quad$\begin{tabular}{ll}

$Q_{\text {sppenemu }}$ \& | is the charge into the gate |
| :--- |
| during the switching transition; | <br>

\& $t_{\text {potaeeu }}$

 

is the time taken to switch or <br>
traverse the plateau region.
\end{tabular}

The maximum allowable drive impedance can be calculated using Equation 6.7, and for a 12 V drive level, the allowable impedance is $2,2 \Omega$.

$$
\begin{equation*}
Z_{\text {dine }}=\frac{V_{\text {drive }}-V_{\text {placax }}}{I_{\text {drive }}} \tag{6.7}
\end{equation*}
$$

The total power dissipated in the drive transitors at 3.3 MHz can be calculated using Equation 6.8 and is 1.8 W .

$$
\begin{equation*}
P_{\text {dime }}=Q_{8} V_{\text {diwn }} f\left[\frac{R_{\text {dive }}}{R_{\text {dimiv }}+R_{z}}\right]+I_{C_{4, m u}}^{2} R_{\text {ds }(m)} \tag{6.8}
\end{equation*}
$$

Where: $\quad R_{\text {dive }} \quad$ is the effective output resistance of the drive transistors;
$R_{d(0 n)} \quad$ is the on resistance of the $n$ channel
turn off transistor;
$R_{z} \quad$ is the MOSFET intrinsic gate resistance;
$Q_{2}$ is the total gate charge required;
is the r.m.s. reverse transfer
capacitor current.

The resulting gate drive circuit is shown in Figure 6.4, the gate drive buffer to the DS0026 is the quad, complementary MOSFET package, the VQ7254P. The use of the buffer transistors increases the current source capability of the driver from 1.5 A to 4 A , the drive source impedance being approximately $2 \Omega$. Although there are integrated circuits available which are specifically designed for driving power

MOSFETs (for example: the Siliconix D469; the Silicon General SG3626M; the General Electric ICL7667; and the Teledyne TSC4263), tests showed that none had the high frequency capability of the National Semiconductor DS0026 MOS clock driver IC.


Figure 6.4 3.3 MHz Gate Drive Circuit.

To reduce power loss due to cross conduction, a 'dead' time between the n channel drive transistors switching off and the pchannel transistors switching on (and vice versa) is provided by TTL pulse generators. Figure 6.5 shows the resulting drive to the p and n channel buffer transistors.

The IRF450 gate drive waveform at 3.3 MHz is shown in Figure 6.6. The time taken for the gate drive to traverse the plateau region is 10 ns relating to a switching time of under 15 ns . This circuit is capable of driving the IRF450 at frequencies up to 5 MHz .


Figure 6.5 Drive Buffer Transistors Showing Dead Time. Upper Trace: VP0300 Transistor Drive (5 V/Div. 50 ns/Div.) Lower Trace: VN0300 Transistor Drive (5 V/Div. $50 \mathrm{~ns} /$ Div.).


Figure 6.6 3.3 MHz Drive to IRF450 (5 V/Div. $100 \mathrm{~ns} /$ Div.).

## Circuit Construction

The drive circuit is constructed on an earth plane PCB, all decoupling components being mounted as close as possible to the supply pins of the control circuit ICs and drive transistors. The source lead of the IRF450 power MOSFET is soldered directly to the earth plane of the drive board as is the ground connection of $C_{1}$. Similarly, to minimise drive inductance, the gate lead of the IRF450 is soldered directly to the drive track of the PCB.

The connection between the output inductor and the RF transformer is constructed of parallel copper strip so as to form a low loss, low impedance transmission line. Finally the output power to the load is delivered via a high power $50 \Omega$ coaxial cable.

The cap sealing load consists of a conical shape induction heating coil resonated with a parallel capacitor, the dynamic resistance of the circuit when coupling into the aluminium foil is $50 \Omega$ at 3.3 MHz . With the coil unloaded, i.e. without the bottle in place, the dynamic resistance rises to approximately $55 \Omega$.

The complete inverter, driving a commercial, hand held, cap sealing applicator is shown in Figure 6.7.


Figure 6.7 Complete $500 \mathrm{~W}, 3.3 \mathrm{MHz}$ Inverter Driving Hand Held Cap Sealing Coil.

### 6.1.3.2 Tests on the 3.3 MHz Prototype

The 3.3 MHz prototype has run successfully at power levels greater than 550 W , the usable operating frequency range being 3 to 4 MHz . Conversion efficiency for nominal load values is above $92 \%$ across the frequency range (Hinchliffe et al. 1988d, 1988f-g, 1988i)


Figure 6.8 $\quad$ 3.3 MHz Inverter Output Voltage Waveform: $P_{\text {out }}=500 \mathrm{~W}$ ( 50 V/Div. $50 \mathrm{~ns} /$ Div.)


Figure 6.9 $\quad$ 3.3 MHz Inverter Drain Voltage Waveform: $P_{\text {out }}=500 \mathrm{~W}$ ( $50 \mathrm{~V} /$ Div., $50 \mathrm{~ns} /$ Div.)

The output voltage waveform and drain voltage waveform for 3.3 MHz operation supplying, 500 W to $50 \Omega$ are shown above in Figures 6.8 and 6.9 respectively. The supply voltage being 110 V and supply current 4.9 A . Conversion efficiency is $93 \%$.

When running below the optimum operating frequency, the supply voltage required to produce a given output power is reduced (at the expense of an increase in supply current), resulting in a lower peak $v_{d t}$ with only a $3 \%$ reduction in efficiency. This is in agreement with theoretical analysis (Raab et al. 1977, Raab et al. 1978, Lohn 1986). Thus, with over voltage sensitive components such as power MOSFETs, it may be advantageous to run the Class E inverter at frequencies slightly below optimum, thus reducing peak $v_{d}$ stress.

The IRF450 drain and shunt capacitor current were monitored at nominal load for an output power of 100 W using a Tektronix high frequency current probe. The power was limited to avoid over stressing the probe due to its limited high frequency current capability. The drain current was measured by breaking the drain connection to the printed circuit board and putting a wire loop in place to allow insertion of the current probe. The internal area of the loop was kept to a minimum to minimise the increased drain inductance during current measurements.

The drain current and drain voltage are shown in Figure 6.10. Because the IRF450's output capacitance represents a significant proportion of the shunt capacitor, the device current does not exhibit the classical Class E shape. The constituent parts of the measured drain current are the actual FET current plus the current which flows through the device output capacitance during the off period, this results in a roughly sinusoidal drain current. The drain voltage and external shunt capacitor current are shown in Figure 6.11 and exhibit the classical Class E shape. For both oscillograms, the bandwidth limit function of the oscilloscope was used to present clear waveforms by reducing the ringing observed on the current waveforms caused by interaction between ouput and shunt capacitances, and stray lead inductance (greatly increased by introduction of the current probe and measurement loop).

To measure the actual drain current it is necessary to cancel the magnetic flux generated by the MOSFET output capacitance current which couples with the measuring device. A drain current measurement system showing this technique is given in Appendix VII. One interesting point brought to light by observation of the current waveforms is that the greater the proportion of the device ouput capacitance to the required shunt capacitance value, the lower the $d i d d t$ at the turn off transition, resulting in less radiated electromagnetic noise and less device stress.

The performance of the inverter was evaluated at $40 \%$ full d.c. voltage, supplying a range of load values from $5 \Omega(10 \%$ of nominal) to $450 \Omega(900 \%$ of nominal). Resulting supply current, peak drain voltage, power levels and efficiency are given in Table 6.1. A plot of efficiency against load value is given in Figure 6.12.


Figure 6.10
IRF450 Waveforms in 3.3 MHz Inverter: $P_{\text {out }}=100 \mathrm{~W}$. Upper Trace: Drain Current (2 A/Div. $50 \mathrm{~ns} /$ Div.); and Lower Trace: Drain Voltage ( 50 V/Div. $50 \mathrm{~ns} /$ Div.).


Figure 6.11
Shunt Capacitor Waveforms: $P_{\text {out }}=100 \mathrm{~W}$.
Upper Trace: $C_{1}$ Current (1 A/Div., $50 \mathrm{~ns} /$ Div.);
Lower Trace: $C_{1}$ Voltage ( $50 \mathrm{~V} / \mathrm{Div} .50 \mathrm{~ns} / \mathrm{Div}$.).

| Table 6.1 <br> Load tests for 500W 3.3 MHz Inverter Supply voltage $V_{\boldsymbol{\mu}}$ being 44V. |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Load Resistance $R_{L}$ $\Omega$ | Supply <br> Voltage <br> $I_{\boldsymbol{L}}$ <br> A | Input <br> Power <br> $\boldsymbol{P}_{\text {in }}$ <br> W | Peak Drain Voltage $V_{\text {drack }}$ V | Output <br> Power <br> $P_{\text {ow }}$ <br> W | Efficiency <br> $\eta$ <br> \% |
| 452.0 | 2.05 | 90.0 | 194 | 32.0 | 36.0 |
| 115.0 | 1.78 | 78.4 | 103 | 62.0 | 80.0 |
| 50.0 | 1.87 | 82.4 | 145 | 78.2 | 95.0 |
| 30.2 | 2.11 | 92.8 | 179 | 87.1 | 93.9 |
| 19.7 | 1.22 | 53.6 | 186 | 47.5 | 89.0 |
| 13.3 | 1.54 | 67.8 | 207 | 57.0 | 85.0 |
| 10.4 | 1.00 | 44.0 | 197 | 36.0 | 82.0 |
| 5.3 | 0.64 | 28.4 | 200 | 19.6 | 70.0 |



Figure 6.12 Efficiency of 3.3 MHz Inverter against Load Value.

Finally, open and short circuit tests were performed for a d.c. supply of 40 V . The short circuit was constructed of 300 mm of $50 \Omega$ coaxial cable terminated in a short circuit. Figure 6.13 shows the resulting drain voltage for an open circuit load and Figure 6.14 shows the output waveform and drain voltage waveform for a short circuit load. The circuit parameters for nominal, open and short circuit conditions for a supply voltage of 40 V are given in Table 6.2. Under ideal conditions, the ratio of peak drain voltage to supply voltage is 3.56 , for the short circuit condition this ratio increased to 5.1 (the ratio increases slightly with increasing supply voltage) and for the open circuit condition this ratio increased to 4.4 (the ratio decreases slightly for increasing supply voltage). In both open and short circuit tests, the supply current reduces from that when operating under optimum load conditions.

| Table 6.2 <br> Results of Open-Short Circuit Test On $500 \mathrm{~W}, 3.3 \mathrm{MHz}$ Inverter |  |  |  |
| :---: | :---: | :---: | :---: |
| Test Condition $\left(V_{d 山}=40 \mathrm{~V}\right)$ | Supply Current $\begin{aligned} & I_{\Delta u} \\ & \mathbf{A} \end{aligned}$ | Peak Drain Voltage $v_{\text {dupk }}$ V | Drain to Supply Voltage Ratio $v_{\text {dpp }} / V_{\text {u }}$ |
| Nominal Load | 2.16 | 145.0 | 3.6 |
| Open Circuit Load | 1.0 | 177.0 | 4.4 |
| Short Circuit Load | 0.35 | 204 | 5.1 |



Figure 6.13
IRF450 Drain Voltage in 3.3 MHz Inverter for an Open Circuit Load - $V_{d /}=40$ V. $(50$ V/Div. $50 \mathrm{~ns} /$ Div. $)$.


Figure 6.14 $\quad 3.3 \mathrm{MHz}$ Inverter Waveforms for a Short Circuit Load: Upper Trace: Output Voltage ( 10 V/Div. $50 \mathrm{~ns} /$ Div.); Lower Trace: Drain Voltage ( 50 V/Div. $50 \mathrm{~ns} /$ Div.).

The circuit can be empirically analysed for both open and short circuit conditions as follows. Under steady state short circuit conditions, the Class E inverter can be considered to have a greatly increased operating $Q$ (the only losses in the complete circuit being inductor, capacitor and device conduction losses). Since the output network is close to series resonance, peak voltages within the circuit will be higher for the higher operating $Q$. Also the required supply current will only be that required to replace the energy lost in the resonating network. For steady state open circuit conditions, the circuit is reduced to the active device, the shunt capacitor and the supply inductor. Thus when the device is switched on, the supply current through $L_{1}$ increases, when the device is switched off, the energy stored in the supply inductor is transferred to the shunt capacitor, increasing the shunt capacitor voltage. When the active device is switched on again, the shunt capacitor is discharged through the active device, and the cycle is repeated.

Thus open circuit loads are more dangerous than short circuit loads since the active device dissipates the energy transferred to the shunt capacitor from the supply inductor during the off period. This results in high $1 / 2 C V^{2} f$ loss in the switch. In either case the inverter can be protected by detecting the peak drain voltage, and closing the unit down should this voltage exceed a predetermined level. Further protection for open circuit load conditions could be provided by means of a thermocouple attached to the active device heat sink.

When the inverter was tested driving the cap sealing coil, the peak drain voltage for no load conditions (i.e. without an aluminium foil in the load coil) was only slightly higher than when the cap sealing applicator
was loaded. The aluminium foil disk which forms the tamper proof seal, adds little to the effective RF resistance of the work coil. Thus in practical applications, no damage would result to the inverter, should the bottle (and therefore RF load) be suddenly removed from the work coil.

### 6.1.3.3 PSpice Simulation Results of the 3.3 MHz Prototype

The $500 \mathrm{~W}, 3.3 \mathrm{MHz}$ inverter was simulated using PSpice to complement the practical results and also to investigate transient load conditions such as sudden open and short circuit loads. The PSpice simulation circuit used is shown in Figure 6.15 and the simulation listing is given in Appendix VI, the drive sub-circuit is identical to that shown in Figure 5.17, section 5.1.3. In this simulation, MOSFET lead inductances have been added since at these operating frequencies the influence of lead parasitic inductances cannot be ignored. The output transformer was modelled as an ideal transformer with the mutual coupling factor $K$ set to 0.999 , the required primary and secondary inductance values are related to the turns ratio using the following formula:

$$
\begin{equation*}
\frac{N_{p}}{N_{p}}=\sqrt{\frac{L_{p}}{L_{s}}} \tag{6.9}
\end{equation*}
$$

Where: $\quad \mathrm{N}_{\mathrm{p}}$ is the number of primary turns;
$\mathrm{N}_{3}$ is the number of secondary turns;
$L_{p}$ is the primary inductance;
$L_{z}$ is the secondary inductance.


Figure 6.15 $500 \mathrm{~W}, 3.3 \mathrm{MHz}$ and $200 \mathrm{~W}, 7 \mathrm{MHz}$ Inverter PSpice Simulation Circuits.

CLASS E 3. 3 MHz 500h SImelation. INCLIOING ALL MAIN PARASITIC ELEMENTS Date/Time run: 06/13/88 12: 28: $23 \quad$ Temperature: $\qquad$



Figure 6.16 Simulated Drain and Output voltage of $500 \mathrm{~W}, 3.3 \mathrm{MHz}$ Inverter.
CLASS E 3.3 MHz 500 H SIM\&ATION. INCLUOING ALL MAIN PARASITIC ELEMENTS


Figure 6.17 Simulated Drain Current and Shunt Capacitor current of $500 \mathrm{~W}, 3.3 \mathrm{MHz}$ inverter.

The simulated drain voltage and output voltage are shown above in Figure 6.16, the efficiency predicted by PSpice is approximately $95 \%$. Comparison shows that the practical and simulation waveforms bear close similarity. The simulated drain current and external shunt capacitor current are shown in Figure 6.17 (above), the affect of lead inductance results in the high frequency ringing observed on the capacitor current waveforms (both $C_{a s s}$ and $C_{1}$ ).

The gate drive waveform and drain voltage waveform are shown in Figure 6.18, the high frequency ringing observed on the gate voltage during the off period is caused by the interaction between the reverse transfer capacitance and the gate drive inductance, little of this ringing appears across the gate-source of the MOSFET (shown in Figure 6.19) although the reverse transfer capacitance current, coupled with the current sink limitation of the turn off transistors, results in a non-zero gate-source voltage during the off period. To validate the assumption that the high frequency ringing is caused by interaction between the reverse transfer capacitance and drive inductance, the simulation run was repeated with the MOSFET lead inductances removed. Gate and drain voltage for no parasitic lead inductance are shown in Figure 6.20, the gate voltage waveform is seen to be quite clean as are the drain and shunt capacitor current waveforms, shown in Figure 6.21.


Figure 6.18 Simulated Gate Drive and Drain Voltage Waveforms in 3.3 MHz Inverter.

CLASS E 3.34 Hz 500M SIMLLATION. INCLUDING ALL MAIN PARASITIC ELEMENTS



Figure 6.19 Simulated Gate-Source and Gate Drive Voltage Waveforms in $\mathbf{3 . 3} \mathbf{~ M H z}$ Inverter.


Figure 6.20 Simulated Gate and Drain Voltage Waveforms in 3.3 MHz Inverter without Lead Inductance.


Figure 6.21 Simulated Drain and Shunt Capacitor Current in 3.3 MHz Inverter without Lead Inductance.

Transient and steady state open circuit and short circuit conditions were investigated for an operating supply voltage of 110 V using PSpice. Transient conditions were simulated by either open or short circuiting the load at $t=2 \mu \mathrm{~s}$.

Drain voltage and current for a steady state short circuit condition are shown in Figure 6.22, the r.m.s. supply current being approximately 1 A . Comparison with the plots for nominal load voltage show that the drain voltage waveform is similar, although the peak drain voltage is much higher at 500 V and the duration of positive drain voltage is reduced, the drain current waveform shows that the MOSFET reverse diode conducts for approximately half of the off period because of the higher operating $Q$. If the supply voltage is reduced to 100 V , the simulation results predict that the MOSFET could withstand a steady state short circuit load condition.

Drain voltage and current for a steady state open circuit condition are shown in Figure 6.23 It is not possible in PSpice to have a true open circuit condition since this would result in a floating nodal point, thus the switch used to create an open circuit condition at $t=2 \mu \mathrm{~s}$ was given an off resistance of $30 \mathrm{M} \Omega$. The predicted r.m.s. supply current is approximately 1.1 A . The use of a $30 \mathrm{M} \Omega$ load resistor to simulate an open circuit load results in the drain waveform exhibiting a typical Class E wave shape for higher than nominal load, the peak drain voltage being 350 V , the drain current waveform clearly shows the large drain current spike as the MOSFET discharges the shunt capacitance. Hence if the device is able
to withstand the loss incurred in discharging the shunt capacitor, then steady state open circuit conditions are not dangerous. Further, if a large resistance is permanently connected across the output of the inverter the peak drain voltage can be reduced under open circuit conditions with little loss in efficiency for normal operation.

Simulation waveforms for a sudden load short circuit at $t=2 \mu \mathrm{~s}$ are described below. Drain voltage and current waveforms are shown in Figure 6.23. The drain voltage and current is seen to peak at $t=4 \mu \mathrm{~s}$, peak drain voltage being 950 V and peak drain current being 30 A . A secondary resonance is established between the supply inductor, the shunt capacitance and the output network, the resonant frequency being approximately 125 kHz . This is confirmed by Figure 6.25 which shows the supply inductor current and drain voltage, the supply inductor current is seen to resonate below zero after the short circuit is applied.

Finally, simulation waveforms of drain voltage and current and supply current for a sudden load open circuit are shown in Figure 6.26, the drain voltage is seen to peak at approximately 900 V as the excess supply inductor current is dumped into the shunt capacitor. In this case, no significant secondary resonance is established between the supply inductor and shunt capacitor as a result of the step change in operating conditions owing to the highly damped nature of the circuit.


Figure 6.22 Simulated Drain Voltage and Current in 3.3 MHz Inverter for Steady State Short Circuit.


Figure 6.23 Simulated Drain Voltage and Current in 3.3 MHz Inverter for Steady State Open Circuit.


Figure 6.24 Simulated Drain Current and Voltage in 3.3 MHz Inverter for Transient Short Circuit.


Figure 6.25 Simulated Drain Voltage and Supply Inductor Current in 3.3 MHz Inverter for Transient Short Circuit.

CLASS E 3. 3MHz 500W SIMRLATION. LOAD OPEN CIRCUITED AT T = 2US Date/Time run: 06/15/88 13:50:06 Temperature: 27.0


Figure 6.26 Simulated Drain Current and Voltage and Supply Inductor Current in 3.3 MHz Inverter for Transient Open Circuit.

It can be concluded, therefore, that the Class E inverter is able to withstand steady state open and short circuit conditions but not a sudden short or open circuit when operating at full power. However, the drain voltage waveforms suggest that the circuit can be protected by monitoring the drain voltage and closing the inverter down on the detection of an excessive drain voltage. Ideally the MOSFET would be turned on after detecting the fault condition and the supply removed from the Class E circuit since the MOSFET is better able to withstand over current than over voltage. An alternative approach is to turn the MOSFET off and clamp the drain voltage by the use of a transient absorption zener diode. With the later generation of power MOSFETs which exhibit a recoverable avalanche breakdown, the MOSFET alone could be used to discharge the excessive supply inductor current providing the supply current is within the avalanche rating of the MOSFET.

### 6.1.4 Proposed 2.4 kW 3.3 MHz Unit

The power capability of the Class E inverter can be increased by paralleling devices and/or adopting a push-pull Class E topology. In this section details are given of a proposed 2.4 kW Class E inverter along with simulated performance predictions. The proposed inverter uses four IRF450 MOSFETs, two operated in parallel in each arm of the circuit. The proposed gate drive circuit is based on the drive circuit used for the $500 \mathrm{~W}, 3.3 \mathrm{MHz}$ inverter and is shown in Figure 6.27.

Component values and ratings for each leg, i.e. the shunt capacitor, MOSFETs and supply inductance were computed for a Class E inverter capable of delivering 1200 W . Since the output network is placed on the secondary side of the transformer, $L_{2}$ and $C_{2}$, values and ratings were computed for the full 2.4 kW output power. The required output transformer turns ratio is $1: 2$, the load resistance seen by each leg of the inverter is $6.25 \Omega$. A d.c. blocking capacitor is placed in the primary circuit to avoid any d.c. bias occurring on the transformer. The circuit was designed to produce 2.4 kW for a d.c. supply of 114 V and 23 A , a $90 \%$ efficiency is assumed. The complete circuit along with component values is given in Figure 6.28.

To verify the design the circuit was simulated using PSpice. The simulation circuit used is shown in Figure 6.29. To reduce the coding required in the circuit listing (given in Appendix VI) the circuit was divided into a number of sub-circuits as shown. Simulated drain voltage for each leg and the output voltage waveform are shown in Figure 6.30, the output power into $50 \Omega$ is 2.4 kW and the predicted efficiency is $94 \%$. The drain current and voltage for a single MOSFET is shown in Figure 6.31, both voltage and current levels are well within the device ratings. The simulation supports the presumption that parallel operation of power MOSFETs in a Class E circuit is possible and that power levels can be further increased by push pull operation.


Figure 6.27 Proposed 2.4 kW Push-Pull Class E Inverter Drive Circuit.


Figure 6.28 Proposed 2.4 kW, 3.3 MHz Class E Inverter.


Figure 6.29 PSpice Simulation Circuit for 2.4 kW Push-Pull Class E Inverter.


Figure 6.30 Simulated Drain Voltages and Output Voltage for $2.4 \mathbf{k W}$ Push-Pull Inverter.
CLASS E 3.3Y Hz 2.4 KM PUSH PULL SIMULATION INC. PARASITITS.
Date/Tine run: 05/28/88 13: 13: 15 Temperature: 27.0



Figure 6.31 Simulated Drain Voltage and Current for a Single MOSFET in the $2.4 \mathbf{k W}$ Push-Pull Inverter.

### 6.1.5 The 7 MHz Prototype

Although there are a number of induction heating applications which are performed at 7 MHz , for example the generation of induction coupled plasmas, power levels are usually in the kW region. Thus the 7 MHz inverter described below should not be considered as a viable commercial proposition but as an intermediary between induction and dielectric heating frequencies.

### 6.1.5.1 Design of the 7 MHz 150 W Prototype

The active device chosen for the $150 \mathrm{~W}, 7 \mathrm{MHz}$ prototype was the RF 630 which has a 200 V breakdown voltage (drain to source), 6 A current carrying capability (at $100^{\circ} \mathrm{C}$ ), 800 pF input capacitance and 450 pF output capacitance (maximum values). Computed component values for the 7 MHz inverter are:

$$
C_{1}=870 \mathrm{pF} \quad L_{2}=630 \mathrm{nH} \quad C_{2}=1 \mathrm{nF} \quad L_{1}=6 \mu \mathrm{H} \quad R_{L}=5.5 \Omega
$$

Since $C 1$ is in parallel with the device oupput capacitance a value of 560 pF was chosen. If $C 1$ is too low then the peak drain voltage will exceed the optimum value of $3.56 \mathrm{~V}_{\text {dut }}$. A higher value of $C 1$ than optimum is less dangerous than a lower value. However, if $C_{1}$ is too large, then the drain voltage is not carried to zero before turn on and switching losses will occur. This was observed in the 3.3 MHz unit, where at low supply voltages, the relative value of the reverse transfer capacitance increases, this results in a shunt capacitor value which is slightly too large for optimum Class E operation and tum on loss occurs. In order to match the output of the Class E inverter stage to the RF load, which is nominally designed to $50 \Omega$, a $1: 9$ impedance ratio transformer was constructed using similar techniques to those used for the 3.3 MHz unit. In this case, two twisted pairs of 0.9 mm diameter enamelled copper wires (forming a $16 \Omega$ transmission line) are wound onto two ferrite ring cores (Stackpole type 57-9322) to give a 1:3 effective turns ratio (Krauss et al. 1980). The power handling capability of the transformer which measures $30 \mathrm{~mm} \times 20 \mathrm{~mm} \times 15 \mathrm{~mm}$ is in excess of 200 W at 7 MHz .


Figure 5.33 Circuit Diagram of $150 \mathrm{~W}, 7 \mathrm{MHz}$ Class E Inverter.

The radio frequency choke $L_{1}$ consists of 22 turns of 1.25 mm diameter enamelled wire wound on an SEI high frequency iron powder core type G29 grade 33. The output choke was constructed using the minimum wire length technique for single layer toroids and consists of 11 turns of Litz wire wound on a square cross sectioned toroidal former measuring $35 \mathrm{~mm} \times 14 \mathrm{~mm}$. The circuit diagram for the 150 W prototype is shown in Figure 5.33 (repeated above).

## Design of 7 MHz Driver

To maintain high efficiency, the drain current fall time must occupy less than $15 \%$ of a half cycle (Kazimierczuk 1983a). Thus for 7 MHz operation, the device should turn off in under 10 ns . The amount of charge flowing into and out of the gate during switching for an IRF630 is approximately 10 nC at a gate voltage, $v_{s}$, of 7 V . From Equations $6.6,6.7$ and 6.8 the current required to be sourced by the drive transistors during switching is approximately 1 A , the required drive impedance is $5 \Omega$ and the total power dissipated in the drive transistors is 1.7 W . The drive circuit was designed to be able to dissipate above 2 W to allow for cross conduction during switching of the drive transistors.


All capacitors in $\mu F$

Figure 6.327 MHz gate drive circuit.
The gate drive circuit is shown above in Figure 6.32 and is again based on the DS0026 MOS clock driver. The output of the driver is buffered by pairs of VN0300M and VP0300M transistors. To minimise drive inductance, the drain tabs of the buffer transistor are soldered directly to the gate lead of the IRF630, the source leads of the $n$ channel buffer transistors are connected directly to the source lead of the

IRF630. The circuit construction is described in more detail in Chapter 5, Section 5.2.2. Figure 6.33 shows the gate drive waveform at 7 MHz with no supply voltage applied to the inverter. Rise and fall times of gate drive are 10 and 10.7 ns respectively, the plateau region is traversed in 3.5 ns relating to a switching time of under 4 ns .


Figure 6.33 $\quad 7 \mathrm{MHz}$ Gate Drive to IRF630 ( 5 V/Div. $50 \mathrm{~ns} /$ Div.).

## Overload Protection

Tests and simulation results of the 3.3 MHz unit described above showed that when driving into an excessive load mismatch such as a short or open circuit, the current drawn by the Class E circuit from the supply reduces to approximately $20 \%$ of its nominal load level for open circuit conditions, and $26 \%$ of nominal load level for short circuit conditions. The ratio of peak drain voltage to supply voltage increases to approximately 5 to 1 . However, excessive drain voltage occurs during the transition from optimum load to open or short circuit at full power levels. Thus overload protection can be provided by detecting the peak drain voltage. When an over voltage condition occurs, the transistor drive is disabled, turning off the inverter.

If the voltage rating of the active device is sufficiently over rated then steady state open or short circuit load mismatch can be tolerated, however in the transition from nominal load conditions to extreme mismatch, the surplus energy stored in the supply inductor will be transferred to the shunt capacitor.

The ensuing voltage rise on $C 1$ is given by:

$$
\begin{equation*}
V_{\text {peak }}=\left[\frac{L_{1}}{C_{1}}\left(I_{F L}^{2}-I_{\text {ouls }}^{2}\right)\right]^{\frac{1}{2}} \tag{6.10}
\end{equation*}
$$

$$
\begin{array}{lll}
\text { Where: } & I_{F L} & \begin{array}{l}
\text { is the full load supply current. }
\end{array} \\
I_{\text {ouse }} & \text { is the mismatch load supply current. }
\end{array}
$$

Alternatively, if the device is protected by an over voltage clamp such as a fold back diode or transient absorption zener diode, the energy dissipated in the snubber is given by:

$$
\begin{equation*}
E_{\text {sumbose }}=\frac{1}{2}\left[L_{1}\left(I_{F L}^{2}-I_{\text {ct/x }}^{2}\right)-C_{1} V_{\text {smbumer }}^{2}\right] \tag{6.11}
\end{equation*}
$$

Where: $\quad E_{\text {surubbr }}$ is the energy dissipated;
$V_{\text {sumbser }}$ is the snubber clamping voltage.

If the inverter is shut down on over voltage conditions, then the total energy in $L_{1}\left(1 / 2 L_{F L}^{2}\right)$ is dissipated in the snubber. With the advent of controlled avalanche breakdown MOSFETs, the so called 'ruggedised" MOSFETs, then the device need not be protected, provided the rated avalanche current is greater than the d.c. supply current (Blackburn 1988).

An over voltage shut down circuit, based on the LM710 comparator IC, was incorporated into the 7 MHz prototype and is shown in Figure 6.34. $\mathrm{T}_{1}$ is a wide band high frequency transformer consisting of 8 turns of bifilar wound 0.25 mm enamelled wire on an SEI toroid type MM $623 / 20 / \mathrm{P}$, the measured phase delay of this element is less than 1 ns. The most simple method of protection is to turn the MOSFET off, a transient absorption zener diode being used to clamp the MOSFET voltage. To decouple the diodes' junction capacitance from the Class E circuit, a series diode was included and a capacitor placed across the zener diode to improve its dynamic resistance characteristics, the arrangement is shown in Figure 6.35.

Figure 6.36 shows the resulting turn off drive to the gate of the active device (lower trace) resulting from a simulated over voltage signal (upper trace). Total delay from the received over voltage signal at the input of the comparator to the gate drive of the MOSFET falling below threshold is approximately 60 ns. As was briefly mentioned in section 6.1.3.3 a better approach would be to turn the MOSFET on under fault conditions and limit the supply to the inverter by use of a fast acting current limit pre-converter. The RFC will limit the rate of rise of current to the MOSFET until the pre-converter current limits.


Figure 6.34 Over Voltage Shut Down Circuit.


Figure 6.35 Drain Voltage Clamp.


Figure $6.36 \quad$ Over Voltage Circuit Shutdown Response.
Upper Trace: Over Voltage Signal (2 V/Div. $20 \mathrm{~ns} /$ Div.); Lower Trace: Gate Drive Response (5 V/Div. 20 ns/Div.).


Figure 6.37 Complete $150 \mathrm{~W}, 7 \mathrm{MHz}$ Inverter.

One final consideration is the power dissipated in the active device when the load resistance is higher than the nominal value. As the load resistance increases, the overall $Q$ of the Class E circuit falls, resulting in non-zero drain voltage at device turn on. Any residual voltage across the shunt capacitor is discharged by the MOSFET resulting in excessive $1 / 2 C V^{2} f$ losses. Thus to protect the device adequately a thermal shut down circuit is required.

Load resistance values below nominal are generally quite safe though circuit efficiency falls as the losses in the inverter become a greater proportion of the losses in the circuit.

The complete $150 \mathrm{~W}, 7 \mathrm{MHz}$ prototype is shown above in Figure 6.37 and is contained on one 'Eurocard' size circuit board.

### 6.1.5.2 Tests on the 7 MHz Prototype

Although the unit was designed to deliver 150 W , components were sufficiently derated to allow 200 W operation, Figures 6.38 and 6.39 show drain voltage and output voltage respectively for 200 W output into $50 \Omega$ at 7.0 MHz . Drain voltage and associated gate drive at 7 MHz and 150 W are shown in Figure 6.40. Ringing observed on the drain and gate waveform is due to resonance between: the output capacitance and the stray inductance linking the shunt capacitor to the drain; and the reverse transfer capacitance and gate drive and source lead inductance. This ringing has little affect on the actual gate voltage; thus the MOSFET $R_{d r(o n)}$ is not heavily modulated by this ringing.


Figure 6.38
Drain Voltage of 7 MHz Inverter Supplying 200 W to $50 \Omega$. ( 50 V/Div. $50 \mathrm{~ns} /$ Div.)


Figure 6.39
Output Voltage of 7 MHz Inverter Supplying 200 W to $50 \Omega$. ( $50 \mathrm{~V} /$ Div. $50 \mathrm{~ns} /$ Div.)


Figure 6.40
Waveforms of 7 MHz Inverter Supplying 150 W to $50 \Omega$. Upper Trace: Gate Voltage ( 5 V/Div. $50 \mathrm{~ns} /$ Div.);
Lower Trace: Drain Voltage (50 V/Div. $50 \mathrm{~ns} /$ Div.).

Results of output power and efficiency against input power, voltage and current are given in Table 6.3.

| Table 6.3 Class E Efficiency Tests at 7 MHz |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| $\begin{gathered} \text { Input Voltage } \\ \boldsymbol{V}_{\boldsymbol{\mu}} \\ \mathbf{V} \end{gathered}$ | $\begin{gathered} \text { Input Current } \\ \boldsymbol{I}_{\mu} \\ \text { A } \end{gathered}$ | $\begin{gathered} \text { Input Power } \\ \boldsymbol{P}_{\boldsymbol{\alpha}} \\ \mathbf{W} \end{gathered}$ | $\begin{gathered} \text { Output Power } \\ P_{\text {owe }} \\ \mathbf{W} \end{gathered}$ | Efficiency <br> $\eta$ $\%$ |
| 15.1 | 0.716 | 21.06 | 19.3 | 91.7 |
| 27.6 | 1.94 | 53.66 | 50.0 | 93.2 |
| 31.7 | 2.56 | 81.1 | 75.0 | 92.5 |
| 36.3 | 2.97 | 107.8 | 100.0 | 92.7 |
| 41.9 | 3.20 | 134.1 | 125.0 | 93.2 |
| 44.9 | 3.59 | 161.3 | 150.0 | 93.0 |
| 47.1 | 4.00 | 188.8 | 175.0 | 92.7 |
| 53.2 | 4.07 | 216.7 | 200.0 | 92.3 |

The unit has been operated at a number of frequencies, by altering component values, ranging from 5 MHz to 8 MHz , in all cases the measured conversion efficiency was better than $90 \%$ (Hinchliffe et al. 1988d, 1988e).

The major areas of loss are conduction losses in the switch and copper losses in the output inductor. The output transformer dissipates little power and runs quite cool even at power levels over 200 W . For supplies where higher efficiency is required, device conduction loss can be reduced by paralleling several power MOSFETs, reducing effective $R_{\text {darar }}$.

### 6.1.5.3 PSpice Simulation Results of 7 MHz Prototype

The PSpice simulation circuit used for the 7 MHz inverter is identical to that used for the 3.3 MHz inverter, except for component values and device types, a table is included with Figure 6.15 which shows the circuit components for both the 3.3 MHz and 7 MHz inverters.

Simulated drain voltage and output voltage; drain current and shunt capacitor current for 150 W oupput are shown in Figures 6.41 , and 6.42 respectively. The efficiency predicted by the simulation is above $90 \%$. Again the simulation results agree well with practical measurements.


Figure 6.41 Simulated Drain and Output Voltage of $7 \mathrm{MHz}, 150 \mathrm{~W}$ Inverter.




Figure 6.42 Simulated Drain and shunt Capacitor Current of $7 \mathrm{MHz}, 150 \mathrm{~W}$ Inverter.

### 6.1.6 Computer Control of a Class E Amplifier

To extend the range of load impedances that the Class E inverter could be matched into, a low power ( 100 W ), medium frequency ( 2.5 MHz ) unit was developed based on the 7 MHz inverter design (Hinchliffe et al. $1987 \mathrm{~g}, 1988 \mathrm{e}, 1988 \mathrm{~h}$, Bell 1988, Hinchliffe et al. 1989b) which, under computer control, will change circuit parameters to allow efficient matching into a wide range of load impedances.

The computer (a Cuban 8 commercial control unit running BBC BASIC software) monitored, via isolating circuits, the power out compared to demanded power, the maximum drain voltage, load and drain current. If the operating conditions are out of efficient operating range of the Class E amplifier the computer will either change the operating frequency, or if this fails to bring the inverter into an efficient operating region then the computer powers down the unit and changes load circuit parameters. This is achieved by switching in or out, using radio frequency relays, differing shunt capacitances, output inductors, or output capacitances. It was found that by having three interchangeable Class E circuits (Collins 1987, Hinchliffe et al. 1987) and allowing the frequency to vary from 1 MHz through to 5 MHz then the Class E inverter could be matched into load impedance ratios of ten to one, with conversion efficiencies remaining above $85 \%$.

The resulting circuit schematic is shown in Figure 6.43 and a photograph of the VDU display whilst the unit was operating under computer control is given in Figure 6.44. Figure 6.45 shows the Class E circuit and driver mounted in the prototype unit.


Figure 6.43 Circuit Schematic of Computer Controlled Class E Inverter Circuit.


Figure 6.44 VDU Display of Controlling Computer.


Figure 6.45 Computer Controlled Class E Unit.

One of the problems encountered with the circuit was that the increased stray inductance between the MOSFET drain and the shunt capacitor introduced by the RF relays resulted in increased ringing on the MOSFET drain. This limited the maximum supply voltage which could be applied and still avoid drainsource breakdown, and thus the delivered power out.

Since the load impedance variations in high frequency induction heating applications (such as cap sealing) rarely exceeds two to one (which is within the range of the standard Class E inverter) this line of work was not investigated further.

### 6.2 Conclusions

High efficiency, high frequency units suitable for high frequency induction heating applications in the 1 to 7 MHz range have been successfully constructed and tested using standard power MOSFET packages.

Power levels in excess of 200 W at 7 MHz and 500 W at 3.3 MHz with conversion efficiencies of over $90 \%$ have been achieved. Load tests have shown that the inverter can be operated into a sufficientiy wide range of load impedances, however efficiency falls rapidly at high load values because of $1 / 2 C V^{2} f$ loss, and peak drain voltage is high under short circuit conditions.

Simulation results have supported and enhanced practical measurements and have shown that transient open or short circuit load conditions are destructive, with excessive voltage applied to the switching device, although device current does not exceed pulsed ratings. Tests have shown that the Class E inverter can be protected from load mismatch by clamping the drain voltage and shuting the inverter down on the detection of drain over voltage.

Extension of the Class E inverter's efficient load range has been investigated by combining several circuits in one inverter. However, the introduction of RF relays to switch in and out circuit elements under computer control results in excessive interconnection inductance between the MOSFET and shunt capacitors, limiting operating power.

The 3.3 MHz inverter has successfully been used to drive a commercial hand held cap sealing coil and the proposed push-pull 2.4 kW 3.3 MHz inverter is considered to be powerful enough for most cap sealing applications.


## Chapter 7

## DIELECTRIC HEATING PROTOTYPES

In this chapter a range of prototype solid state supplies designed for small scale plastic welding applications are described. Three inverters are mentioned: a $100 \mathrm{~W}, 14 \mathrm{MHz}$ unit; a $100 \mathrm{~W}, 27.12 \mathrm{MHz}$ unit; and a $150 \mathrm{~W}, 27.12 \mathrm{MHz}$ unit.

## 7 DIELECTRICHEATING PROTOTYPES

In this chapter three solid state inverters are described which are suitable for use as small scale dielectric heating power sources. Three Class E inverters are detailed: a 100 W 14 MHz supply which uses a standard power MOSFET as the switching element, and two 27.12 MHz supplies which use RF power MOSFETs as the active device.

There are a number of applications where light weight, efficient, dielectric heating supplies of approximately 100 to 200 W power output would be advantageous over present valve equipment. One specific requirement in the medical and veterinary fields is the hermetic sealing of samples into plastic containers, for example blood, saline solution etc. In this case a portable unit capable of being run off a battery supply is of value.

## $7.1 \quad 14 \mathrm{MHz}, 100 \mathrm{~W}$ Inverter

The first prototype was designed to operate at the lower dielectric heating frequency of 13.56 MHz and utilises a standard TO220 packaged power MOSFET as the switching element. 14 MHz is close to the practical upper frequency limit of power MOSFETs in standard packages. Higher frequencies can be achieved but this necessitates the use of surface mount and hybrid techniques where the drive circuits are placed on the same substrate as the power device.

### 7.1.1 Design and Construction of 14 MHz Inverter

The design output power for the 13.56 MHz inverter was 100 W , the active device being the IRF630, as used in the 7 MHz inverter. Application of the Class $E$ design program, described in the preceding chapters, resulted in the following component values for the inverter:

$$
C_{1}=340 \mathrm{pF} L_{1}=4 \mu \mathrm{H} C_{2}=436 \mathrm{pF} L_{2}=420 \mathrm{nH} R_{L}=7.24 \Omega
$$

The shunt capacitor, $C_{1}$, is made up from the output capacitance of the IRF630 ( $C_{o s e}=200 \mathrm{pF}$ average, an average value of $C_{\text {ost }}$ is chosen to compensate for the variation in $C_{o s s}$ with drain voltage), and an external capacitance of 140 pF . The supply inductor $L_{1}$ is of a Brooks coil type having a Brooks dimension ' $c$ ' of 6 mm (the reader is referred to Appendix V) and 16 turns of 1.25 mm diameter enamelled copper wire, the ouput inductor consists of 8 turns of 2 mm diameter enamelled copper wire which is wound to form a single layer solenoid of length 20 mm and diameter 15 mm .

To match the $7.24 \Omega$ output impedance to the $50 \Omega$ RF load, a capacitor matching network was designed. Since dielectric heating supplies operate within a tight frequency tolerance, wideband matching networks, such as that used in the 7 MHz converter, are not required. The most efficient narrow band matching network consists of a series/parallel capacitor network as outlined below.


Figure 7.1 Capacitor Matching Network.
With reference to Figure 7.1, for the input impedance and phase to be identical for both load networks, the following criteria must apply:

$$
\begin{equation*}
C_{s}=\frac{1}{\omega\left(R_{0} R_{p}-R_{0}^{2}\right)^{\frac{1}{2}}} \tag{7.1}
\end{equation*}
$$

Where: $\quad C_{3}$ is a capacitance in series with the inverter's required load resistance $=7.24 \Omega$;
$C_{p}$ is a capacitance in parallel with the actual $R F$ load resistance $=50 \Omega$.

$$
\begin{equation*}
C_{p}=\frac{C_{s}}{1+\frac{R_{e}^{2}}{x_{c_{s}^{2}}^{2}}} \tag{7.2}
\end{equation*}
$$

Thus the input impedance of a capacitor $C_{p}$ in parallel with a load resistance $R_{p}$ is equivalent to a capacitor $C_{2}$ in series with the load resistance $R_{0}$ (Hayward 1982). Since the inverter has an oupput capacitor, $C_{2}$, the actual required series capacitor is that which, when combined with the effective series capacitor, $C_{3}$, gives the correct value for $C_{2}$.

$$
\begin{equation*}
C_{2}=\frac{C_{3}^{\prime} \times C_{2}}{C_{1}^{\prime}+C_{2}} \tag{7.3}
\end{equation*}
$$

Rearranging gives:

$$
\begin{equation*}
C_{2}^{\prime}=\frac{C_{2} \times C_{3}}{C_{3}-C_{2}} \tag{7.4}
\end{equation*}
$$

A program was written in BASIC to calculate the required matching capacitor values (the listing is given in Appendix IV) which are as follows:

The series capacitor to replace $C_{2}=1.26 \mathrm{nF}$;
The capacitor in parallel with the $50 \Omega$ load $=570 \mathrm{pF}$.

The resulting inverter schematic is shown in Figure 7.2 along with a table of component values for all three inverters described in this chapter. The capacitors used in the inverter are Unilator type $102,1 \mathrm{kVA}$ capability high frequency ceramic.

table of component values

|  | $M_{1}$ | $L_{1}$ | $c_{1}$ | $L_{2}$ | ${ }^{5} 5_{1}$ | $C_{p}$ | Pout | F | Vod |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 14 MHz 100 W | IRF630 | 4 UH | 140pF | 0.4 HH | 1.3 nF | 570pf | 200w | 14.6 | 50 V |
| 27.12 MHz 100 W | DVD120 T | 4.40 HH | 47p f | 0.4 uth | 180p | 180pf | 100W | $27 \cdot 12$ | 60 N |
| 27.12MHz 150W | MRF150 | 0.8 uH | 200pf | 80 nH | $\infty$ | 510pf | 150W | 27.12 | 30 V |

Figure 7.2 Dielectric Heating Inverter Schematic.

### 7.1.1.1 Design of the 14 MHz Driver

Several driver designs were investigated to achieve a satisfactory gate drive for the IRF630 at 14 MHz . One of the problems encountered when attempting to use the 7 MHz gate drive circuit, discussed in Chapter 6, at 14 MHz is the excessive drive tzansistor dissipation due to shoot through current during the unavoidable duration when both the upper and lower drive transistors conduct simultaneously.

In an attempt to avoid this cross conduction, a common drain configuration was investigated as shown in Figure 7.3. In order to ensure low drive impedance, the gate drive excursion for the buffer transistors, when using a 10 V drain supply, must be from -5 V to +15 V . This increase in operating voltage for the DS0026 drive IC caused excessive power dissipation, particularly at the higher operating frequency of 14 MHz , due to the very much greater $1 / 2 \mathrm{CV}^{2} f$ loss incurred in charging and discharging the gate capacitances of the drive transistors.


Figure 7.3 Common Drain Drive Configuration.
An alternative drive circuit considered was the so called 'resonant' gate drive (Lee 1987) as shown in Figure 7.4. Operation of the circuit is as follows. Switch $\mathrm{S}_{1}$ is turned on, discharging the MOSFET gate, during the MOSFET off period the current $i_{L}$ builds, storing energy in the inductor $L$. When the switch is turned off, the energy stored in the inductor is transferred to the gate capacitance of the MOSFET, the diode prevents the inductor resonating with the input capacitance of the MOSFET. If the energy stored by the inductor at the instant of switch turn off equals the energy stored by the input capacitance of the MOSFET when the gate voltage is at $V_{a n}$, then the rise in gate voltage of the MOSFET will be that required to turn it fully on. The gate drive is not actually a resonant drive since the energy stored in the capacitor is not transferred back to the inductor at turm off of the power MOSFET, thus the power dissipated in the drive switch is effectively equal to the $1 / 2 C V^{2} f$ drive loss mentioned in the previous chapters. However no loss is incurred due to cross conduction.


Figure 7.4 Resonant Gate Drive Circuit.
There are two main disadvantages with this circuit. One is the reverse recovery current of the diode which, at high switching frequencies, will allow reverse current flow through the inductor, partially discharging the gate capacitance. The second is the peak voltage incurred across the switch on interruption of current flow through the inductor. The presence of gate and source lead inductance will allow this voltage to peak at high levels which could cause breakdown in the switch. An investigation into the use of signal diode zener diode combinations to clamp the gate voltage showed that it was impractical to provide reliable, over voltage, protection at these higher operating frequencies because of the, unavoidable, parasitic lead inductances of the voltage clamp devices.

Thus the gate drive circuit used for the 14 MHz inverter is based on the drivers reported in the previous chapters. The source impedance of the driver was reduced by paralleling three driver circuits in similar fashion to the drive circuit developed for the high speed switching tests (Chapter 5). TO-206 packaged VP0300 and VN0300 devices were employed to cater for the increased device dissipation, the resulting 14 MHz drive circuit is shown in Figure 7.5, the gate drive waveform to the IRF630 at 14 MHz is shown in Figure 7.6. Rise and fall times of the gate drive are approximately 5 ns , and the plateau region is crossed in approximately 3 ns at both turn on and turn off. There is a certain amount of under-shoot (of approximately 1 V ) at tum off due to resonance between the gate drive inductance and MOSFET input capacitance.

The 14 MHz inverter and drive circuit were constructed on an earth plane PCB, the IRF630 being mounted directly below the circuit board on a $2^{\circ} \mathrm{C} / \mathrm{W}$ heat sink. The drain connection for the IRF630 was made by means of a solder tag between the drain tab and the shunt capacitor terminal to minimise interconnection inductance. The complete inverter is shown in Figure 7.7.


Figure 7.5 14 MHz Gate Drive Circuit.


Figure 7.6 14 MHz Gate Drive Waveform (2 V/Div. $20 \mathrm{~ns} /$ Div.).


Figure $7.714 \mathrm{MHz}, 100 \mathrm{~W}$ Inverter.

### 7.1.2 Tests on $14 \mathrm{MHz}, 100 \mathrm{~W}$ Inverter

The inverter was tested for a gate drive frequency of 13.56 MHz , a drain supply voltage of 50 V , with a load impedance of $50 \Omega$ resistive. The drain and load voltage waveforms are shown in Figure 7.8.

The power supplied to the load, measured by a through-line wattmeter, was 100 W ; the d.c. power supplied to the inverter being 110 W giving a conversion efficiency of $90 \%$. The majority of the losses occur as conduction loss in the switch. Since the supply current ( 2.2 A ) and on resistance of the MOSFET are known, the MOSFET conduction losses can be calculated by applying Equation 6.5 (repeated here for convenience).

The power dissipated in the MOSFET is simply:

$$
\begin{equation*}
P_{d} \approx 2.37 I_{d d}^{2} R_{d(m)} \tag{6.5}
\end{equation*}
$$

Since the on resistance of an IRF630 is typically $0.5 \Omega$ (at $\theta_{\mathrm{J}}=60^{\circ} \mathrm{C}$ ), the conduction loss is 5.7 W , thus switching loss and inductor/capacitor loss represents less than $50 \%$ of the total losses (i.e. 4.3 W ).


Figure 7.8 Waveforms for $14 \mathrm{MHz}, 100 \mathrm{~W}$ Inverter. Upper Trace: Drain Voltage ( 50 V/Div. $20 \mathrm{~ns} /$ Div.); Lower Trace: Load Voltage ( 50 V/Div. 20 ns/Div.).


Figure 7.9
Waveforms of $100 \mathrm{~W}, 14 \mathrm{MHz}$ inverter.
Upper Trace: Gate Voltage (5 V/Div. $20 \mathrm{~ns} /$ Div.);
Lower Trace: Drain Voltage (50 V/Div. $20 \mathrm{~ns} /$ Div.).

The drain voltage waveform and gate drive waveform for 100 W output power are shown in Figure 7.9. Again ringing can be observed on the gate during the off period due to interaction between the reverse transfer capacitance and gate drive inductance. This has no observable affect on the drain voltage waveform and it can be concluded that the actual gate-source voltage sees only a small proportion of the ringing voltage.

The output power obtained for applied supply voltage does not precisely agree with the Class E design equations given in Appendix III. These predict a delivered power of over 150 W to $7.4 \Omega$ for a drain supply voltage of 50 V and an operating $Q$ of 5 . There are a number of possible explanations why the delivered power is less than the theoretical power. The design equations do not incorporate the system losses, such as conduction loss, which serve to raise the effective load impedance seen by the inverter, thereby reducing the overall $Q$ and thereby reducing the power delivered. Since the operating $Q$ is used to predict the delivered power (the lower the $Q$, the lower the delivered power), conduction loss has both a primary and secondary influence on the delivered power.

A further possible reason is that of the tighter component tolerance requirements of the capacitor matching network over a transformer matching system. Since precise matching capacitor values could not be obtained, the matching network used is not ideal. This will influence the operating characteristics of the Class E inverter.

Nevertheless the inverter was successfully operated over long periods, delivering in excess of 100 W at 13.56 MHz , with a conversion efficiency in the region of $90 \%$.

## 7.2 $\quad 27,12 \mathrm{MHz}, 100 \mathrm{~W}$ and 150 W Inverters

Experience gained with the 14 MHz inverter confirmed earlier predictions that operation of standard power MOSFETs at frequencies much above 10 MHz was difficult unless one resorted to more elaborate packages, with the drive circuit placed on the same substrate as the power device. Thus RF power MOSFETs were employed for the prototypes designed to operate at the plastics welding frequency of 27.12 MHz . The cost of developing hybrid power MOSFETs/drivers would outweigh the increased cost in employing the more expensive RF power MOSFETs.

Two inverters were designed, constructed and tested: a 100 W unit employing a DVD120T RF MOSFET which has a breakdown voltage of 225 V , continuous drain current rating of 4.5 A , an input capacitance of 400 pF , a reverse transfer capacitance of 15 pF and an output capacitance of 100 pF (MA-COM/PHI 1986); and a 150 W inverter employing an MRF150-a $125 \mathrm{~V}, 16 \mathrm{~A}$ device with an input capacitance of 350 pF , a reverse transfer capacitance of 50 pF and an output capacitance of 250 pF .

### 7.2. $\quad$ Design of RF MOSFET Gate Drive

The drive circuit developed for the 27.12 MHz inverters is shown in Figure 7.10 and uses paralleled RF bipolar transistors operated in common collector, push-pull configuration. Paralleled high speed CMOS inverters are used to buffer the TTL input drive signal. Transistor $\mathrm{Q}_{1}$, operated in common emitter
configuration, amplifies the drive signal to give a 0 to +15 V swing. Inductor $L_{1}$ is a collector peaking inductor which reduces the collector voltage rise time of $\mathrm{Q}_{1}$ and provides a degree of over-drive for the npn drive transistors, $\mathrm{Q}_{2}$ to $\mathrm{Q}_{\mathbf{3}}$.


Figure 7.10 RF MOSFET Gate Drive Circuit.
Emitter ballast resistors ( $1 \Omega$ ) are employed to ensure current sharing in the paralleled drive transistors and also serve to reduce the $Q$ of the gate network, avoiding parasitic oscillation of the RF power MOSFET (described in Chapter 5 Section 5.3.2).

The unloaded output waveform of the drive circuit is shown in Figure 7.11, rise and fall times are less than 2 ns which is at the limit of the measurement capability of the 350 MHz oscilloscope used to monitor waveforms.


Figure $7.11 \quad$ Unloaded Output of RF MOSFET Gate Driver (2 V/Div. $20 \mathrm{~ns} /$ Div.).

### 7.2.2 Design and Construction of 27.12 MHz Inverters

The computed component values for the Class E inverters are as follows:
For the 100 W inverter employing the DVD120T:

$$
\begin{aligned}
& C_{1}=82 \mathrm{pF} \\
& L_{1}=4.2 \mu \mathrm{H} \\
& C_{2}=100 \mathrm{pF} \\
& L_{2}=440 \mathrm{nH} \\
& R_{L}=15 \Omega
\end{aligned}
$$

Allowing for the contribution of the DVD120T output capacitance to $C_{1}$ a value of 47 pF was chosen for the shunt capacitance. To match the inverter to the $50 \Omega$ RF load the computed matching capacitor values are:

The series capacitor to replace $C_{2}\left(C_{s 1}\right)=180 \mathrm{pF}$
The capacitor in parallel with the $50 \Omega$ load $\left(C_{p}\right)=180 \mathrm{pF}$.

For the 150 W inverter employing the MRF150:

$$
\begin{aligned}
& C_{1}=434 \mathrm{pF} ; \\
& L_{1}=800 \mathrm{nH} ; \\
& C_{2}=560 \mathrm{pF} ; \\
& L_{2}=83 \mathrm{nH} ; \\
& R_{L}=2.8 \Omega
\end{aligned}
$$

Allowing for the contribution of the MRF150's output capacitance to $C_{1}$ a shunt capacitor value of 200 pF was chosen. To match the inverter to the $50 \Omega \mathrm{RF}$ load the computed matching capacitor values are:

The series capacitor to replace $C_{2}\left(C_{s}\right)=\infty \mathrm{F}$;
The capacitor in parallel with the $50 \Omega$ load $\left(C_{p}\right)=510 \mathrm{pF}$.

Note that in this case the value for $C_{a 1}$ is infinite, thus the output network consists simply of the shunt capacitor, $C_{1}$, the output inductor, $L_{2}$, and the matching capacitor in parallel with the load, $C_{p}$.

The circuit schematic for both prototypes is given in Figure 7.2.
Both inverters were constructed on an earth plane PCB, the RF power transistors being mounted on $0.9^{\circ} \mathrm{C} / \mathrm{W}$ heat sinks on to which the PCBs are bolted. Copper heat spreaders are used to reduce the thermal impedance between the transistors and the heat sink. Both RF transistors have multiple source connections (two in the case of the MRF150 and 4 in the case of the DVD120T), thus separate source returns and separate ground planes are used for the drive and power circuits to overcome the effects of source feedback. During testing it was observed that the drive transistors ran hot when driving the RF power MOSFET gate, the steady state case temperature of the RF bipolar transistors was measured at $95^{\circ} \mathrm{C}$. Although this case temperature is within the ratings of the drive transistors; $48^{\circ} \mathrm{C} / \mathrm{W}, \mathrm{TO} 5$ transistor case heat sinks were added to increase long term reliability.

The 100 W 27.12 MHz inverter employing the DVD120T and the 150 W 27.12 MHz inverter employing the MRF150 are shown in Figures 7.12 and 7.13 respectively. In Figure 7.13 the small coaxial oscilloscope probe sockets which were used to monitor gate, drain and output voltage waveforms can be seen. At high operating frequencies, the inductance associated with the earth lead normally used to ground the oscilloscope probe distorts the measured waveform due to its interaction with the probe tip capacitance and circuit parasitic capacitances. Coaxial probe sockets reduce the probe earth connection inductance, and also provide a reliable connection system. The difference between a waveform monitored using a conventional oscilloscope probe ground lead and the same waveform monitored using a coaxial probe socket is demonstrated in Appendix VII ('Measurement Techniques').


Figure 7.12 $100 \mathrm{~W}, 27.12 \mathrm{MHz}$ Inverter.


Figure 7.13 150 W 27.12 MHz Inverter.

### 7.2.3 Tests on 27.12 MHz Inverters

Both 27.12 MHz inverters were run at full design power for extensive periods of time (in excess of 1 hour). Oscillograms taken for both inverters are described in turn.

The drain and output voltage waveforms for the 100 W inverter operating at full power are shown in Figure 7.14. For a supply voltage of 59 V , the d.c. input power required for a delivered power of 100 W was 144 W , giving a conversion efficiency of $70 \%$. The major area of loss is conduction loss in the RF MOSFET, the calculated $R_{d(a n)}$ for the DVD120T is $3 \Omega$, thus for a supply current of 2.45 A , the r.m.s. drain current is 3.7 A resulting in a conduction loss of 42.6 W . The peak drain current is 7 A , giving a peak conduction drop of 21 V . Inspection of the drain waveform during the off period shows this conduction drop, the drain current wave-shape being well defined. Close inspection of the drain voltage waveform at device turn on reveals that the drain voltage zero $\mathrm{d} v / \mathrm{d} t$ region does not occur at 0 V , thus $1 / 2 C V^{2} f$ loss occurs at turn on. However, substituting the relevant values into the above equation reveals that turn on loss only contributes 0.8 W to the total conversion losses. The remaining 0.6 W of losses can be assumed to occur principally in the output inductor and to a lesser extent in the supply inductor.


Figure 7.14 Waveforms of $100 \mathrm{~W}, 27.12 \mathrm{MHz}$ Inverter.
Upper Trace Drain Voltage ( 50 V/Div. $10 \mathrm{~ns} /$ Div.);
Lower Trace Output Voltage ( $50 \mathrm{~V} / \mathrm{Div} .10 \mathrm{~ns} / \mathrm{Div}$. ).
The $10 \mathrm{~V}, 27.12 \mathrm{MHz}$ gate drive waveform to the DVD120T is shown in Figure 7.15, rise and fall times of the gate drive are approximately 4 and 5 ns respectively.


Figure 7.15
27.12 MHz Gate Drive to DVD120T (5 V/Div. $10 \mathrm{~ns} /$ Div.).


Figure 7.16
Drain Voltage Waveform of $\mathbf{2 7 . 1 2 \mathrm { MHz } , 1 5 0 \mathrm { W } \text { Inverter. }}$ ( 20 V/Div. $10 \mathrm{~ns} /$ Div.)


Figure 7.17 Output Voltage Waveform of $27.12 \mathrm{MHz}, 150 \mathrm{~W}$ Inverter. ( 50 V/Div. $10 \mathrm{~ns} /$ Div.)

The drain and output voltage waveforms for the 150 W inverter are shown above in Figures 7.16 and 7.17. With a supply voltage of 31.4 V and supply current of 6.3 A , the measured output power into $50 \Omega$ was 150 W , the conversion efficiency being $74.6 \%$ which is a $36 \%$ improvement over the Class C amplifier reported in Chapter 4. Again the major area of loss is conduction loss in the device. The quoted conduction drop of the MRF150 at $I_{d}=10 \mathrm{~A}$ and $v_{g}=10 \mathrm{~V}$ is 5 V giving an on resistance of $0.5 \Omega$. From Equation 6.5 the power dissipated in the MOSFET for a drain supply current of 6.3 A is 47 W .

### 7.3 Conclusions

A number of power inverters suitable for use as dielectric heating supplies have been described. A $14 \mathrm{MHz}, 100 \mathrm{~W}$ unit, utilising a standard power MOSFET has been demonstrated. This is thought to be the practical upper frequency limit of conventionally packaged power MOSFETs. Two 27.12 MHz inverters incorporating RF power MOSFETs have been described. Although the conversion efficiencies of these RF supplies is less than that encountered when using standard power MOSFETs (due to the increased conduction drop of the RF MOSFETs) the Class E inverters have proved superior to the more conventional Class C amplifier in terms of efficiency, ease of design and construction, and purity of output waveform.

Output powers in excess of 150 W at 27.12 MHz with conversion efficiencies of $75 \%$ have been achieved using a resonant switching-mode topology. It is thought that these power levels and efficiencies could be increased by parallelling devices and/or using a push-pull Class E configuration.

## Chapter 8

## CONCLUSIONS

The achievements of the work and conclusions on the adaptation of the Class $E$ inverter to, and the use of power MOSFETs in, solid state HF induction and dielectric heating supplies are outined. Recommendations for further work are given.

## 8 <br> CONCLUSIONS

The adaptation of the Class E amplifier to produce RF power for high frequency induction and dielectric heating applications has been investigated.

Following a comprehensive, critical review of power devices and circuit topologies, the power MOSFET was concluded to be the most suitable device for the generation of RF power above 1 MHz . Preliminary investigations into linear and Class $E$ amplifiers predicted that the Class E inverter is the circuit most applicable to high frequency (between 3 and 30 MHz ) electric process heating applications.

Subsequent investigations into the switching speed of the power MOSFET showed that the maximum practical switching frequency for standard power MOSFETs is between 5 and 15 MHz , depending on power rating. Switching speed could be appreciably increased by the inclusion of a second source connection to reduce source feedback. The kelvin contact in current sensing MOSFETs can be used to increase switching speed in pulsed applications but device failure occurs because of lateral RF current flow through the source metalisation when the current sensing MOSFET is applied to high frequency resonant inverters.

The development of two prototypes using standard power MOSFETs capable of producing power at HF induction heating frequencies with conversion efficiencies in excess of $90 \%$ has demonstrated that the power MOSFET can be successfully made to operate in practical applications at frequencies above 1 MHz . A $500 \mathrm{~W}, 3.3 \mathrm{MHz}$ prototype has been used to drive a commercial, hand-held, cap sealing applicator, demonstrating the suitability of the Class $E$ inverter for high frequency induction heating applications.

Three prototype units have been developed to produce RF power at the dielectric heating frequencies of 13.56 and 27.12 MHz . At the lower dielectric heating frequency of 13.56 MHz a single standard power MOSFET has successfully been used to generate more than 100 W , this is believed to be the practical upper frequency limit of standard power MOSFETs. The generation of RF power leveis above 150 W at 27.12 MHz , with high conversion efficiencies and with the use of a single active device again demonstrates the potential of the Class E inverter as a high frequency power source.

Circuit simulation using PSpice has predicted that power levels can be increased by the parallel operation of devices and/or the use of push-pull inverter topologies.

### 8.1 Achievements

The principle achievements of the work described in this thesis are given below.
(1) Three units suitable for use as dielectric heating power sources have been developed. Maximum power achieved at 27.12 MHz being in excess of 150 W with a conversion efficiency of $75 \%$.
(2) A $500 \mathrm{~W}, 3.3 \mathrm{MHz}$ inverter, utilising a single standard power MOSFET has been developed. The unit has been successfully used to drive a commercial hand-held cap-sealing applicator. Investigations into load variation effects on the Class E inverter (including open and short circuit loads) have been performed. It has been shown that the Class E inverter can be protected against extreme load mismatch by use of an over-voltage detection circuit.
(3) PSpice simulation work has supported practical measurements on the 500 W inverter. Simulation of open and short circuit transient conditions on the Class E inverter has been performed. The effect of the interaction of the reverse transfer capacitance current and the gate drive inductance has been analysed.
(4) A proposed $2.4 \mathrm{~kW}, 3.3 \mathrm{MHz}$ push-pull ClassE converter has been designed. The design has been verified using PSpice.
(5) A TO3 packaged IRF450 has been modified to include a second source lead to overcome source feedback effects. Tests have shown that an increase in switching speed in excess of two to one occurs at rated continuous current.
(6) The use of the kelvin contact as a separate drive source connection in current sensing power MOSFETs to increase switching speed in pulsed applications has been demonstrated.
(7) The failure mode of current sensing MOSFETs in HF inverters when the kelvin contact is used as a second source connection has been analysed. An equation for the r.m.s. current flowing through the MOSFET reverse transfer capacitance has been derived.
(8) Tests have shown that use of expensive RF packaging techniques for power MOSFETs do not result in a substantial improvement in switching performance over that obtained by modifying a standard package to incorporate a second source terminal.
(9) PSpice simulation results have supported practical investigations into switching performance.
(10) A $7 \mathrm{MHz}, 200 \mathrm{~W}$ prototype has been constructed which incorporates a high speed over-voltage protection circuit.
(11) High frequency drive circuits have been developed for use with standard and RF power MOSFETs.
(12) Computer programs have been written to calculate all the parameters required in the design of a Class E inverter.
(13) RF impedance matching techniques have been applied to HF power inverters.
(14) An investigation into the control, and extension of load range, of a Class E inverter by the use of a microprocessor controller has been made.
(15) Prototype linear Class AB and Class C amplifiers capable of delivering 300 W at 27.12 MHz have been constructed and their suitability for use as $\mathrm{HF}, \mathrm{RF}$ heating power sources assessed.
(16) A comprehensive, critical review of present power electronic devices and power converter/inverter circuits has been undertaken and reported.
(17) Earlier work on voltage and current fed MF induction heating power supplies has been critically reviewed.
(18) An improved method for the measurement of the intrinsic gate resistance in a power MOSFET has been demonstrated.

### 8.2 Recommendations

It is believed that the maximum switching frequency of standard power MOSFETs has been reached with this work. In order to extend the operating frequency it is necessary to modify power MOSFET packages by incorporating a second source terminal. Further increases in switching performance will result from the inclusion of the drive circuit on the same substrate as the power MOSFET die.

The power level of the Class E inverter can be increased by the use of paralleled devices and by adopting a push-pull inverter configuration. A design of a $2.4 \mathrm{~kW}, 3.3 \mathrm{MHz}$ converter has been given, it is thought that this unit could be applied to the majority of cap-sealing applications.

It is predicted that the Class E inverter can be protected against load mismatch by the detection of excessive drain voltage. In commercial units it is recommended that on the detection of this over voltage, the power MOSFET(s) should be switched on and the power supply to the inverter disabled. The supply inductor will limit the rise of drain current to below excessive levels provided that a pre-conventer with a fast acting current limit is used to supply the Class E inverter.

The operating power levels of the dielectric heating supplies can be further increased by the parallel operation of a number of inverter modules and by the use of power combining techniques similar to those used in high frequency linear amplifiers.

## APPENDICES

## Appendix I

## SIMPLIFIED CALCULATION OF MOSFET SWITCHING TIME

Considering the simplified MOSFET equivalent circuit switching a $25 \Omega$ load as shown in Figure AI.1, an approximation of the absolute minimum switching times of a power MOSFET used to switch a resistive load can be calculated.

There are three stages to the turn on and turn off process as shown in Figure AI.2.

Stage 1) Resistor-capacitor charging of the device gate up to the threshold voltage.

Stage 2) Switching or the plateau region. Here the drain voltage collapses, and the majority of charge input to the gate is absorbed by the reverse transfer capacitance, $C_{d_{g}}$, whose effective value is large during this period due to the Miller effect since the voltage gain of the stage is high. During this period the gate voltage rise is small, sufficient only to maintain the increasing drain current.

Stage 3) In this region the drain voltage has fallen and drain current is fully established. Here the MOSFET is over driven and the input capacitance, $C_{i s}$, which is made up of the gate-source capacitance, $C_{8 r}$, in parallel with the gate-drain capacitance, $C_{d g}$, (as with all depletion layer capacitances $C_{d}$ increases as the voltage across the layer falls or reverses).

Turn off is simply a reversal of the above process with the exception that the rate of rise of drain voltage is governed not only by the rate by which charge is removed by the gate but also by the charging rate of the output capacitance, $C_{d t}+C_{d g}$.


Figure AI. 1 Simplified MOSFET Equivalent Circuit.


Figure AI. 2 Ideal MOSFET Switching Waveforms.

## i Turn@n

## a Turn on Delay Time

Below threshold the change of gate voltage with time can be described by:

$$
\begin{equation*}
v_{s t}=V_{\text {dinin }}\left(1-e^{-\frac{1}{2}}\right) \tag{AI.1}
\end{equation*}
$$

| Where: | $v_{s,}$ is the gate-source voltage; <br> $V_{\text {drive }}$ is the gate drive voltage; <br> $\tau_{1}$ is a time constant given by: |
| :--- | :--- | :--- |

$$
\begin{equation*}
\tau_{1}=\left(R_{z}+R_{\text {dimu }}\right) C_{z} \tag{AI.2}
\end{equation*}
$$

Where: $\quad R_{z} \quad$ is the MOSFET intrinsic gate resistance; $R_{\text {driv }} \quad$ is the drive circuit source resistance.

Threshold voltage, $V_{b}$, is taken as the gate voltage at which the drain voltage just starts to collapse sufficiently fast such that the Miller effect of $C_{d 8}$ alters the rate of rise of gate voltage.

For an IRF450 with drain supply voltage, $V_{d 山}=300 \mathrm{~V}$, drain current, $I_{d}=12 \mathrm{~A}, V_{t}=3.5 \mathrm{~V}$, and $V_{\text {diviv }}=$ 14 V , a purely resistive load, $R_{L}$, of $25 \Omega$ and with a $1 \Omega$ drive source impedance, the turn on delay is:

$$
\begin{equation*}
t_{1}=\tau_{1} \ln \frac{V_{\text {dim }}}{V_{\text {dive }}-V_{t}} \tag{AI.3}
\end{equation*}
$$

$$
t_{1}=0.7 \mathrm{~ns}
$$

## b Turn On Rise Time

During the switching period, when $v_{d}$ is falling, the reverse transfer capacitance $\left(C_{d g}\right)$ is increased by the Miller effect.

$$
\begin{equation*}
C_{d g \text { g spccive }}=\left|A_{v}\right| C_{d g} \tag{Al.4}
\end{equation*}
$$

Where: $A_{v}$ is the voltage gain of the stage and is given by:

$$
\begin{equation*}
A_{v}=\frac{\delta v_{d r}}{\delta v_{z u}} \tag{AI.5}
\end{equation*}
$$

Region two lasts until $v_{8}$, rises to just sustain the maximum switched drain current of 12 A . That is until:

$$
\begin{equation*}
v_{s}=V_{1}+\frac{12}{g_{m}}=V_{1}+1.2 \tag{AI.6}
\end{equation*}
$$

Where: $g_{m}$ is the transconductance $\approx 10$.

During this time the drain voltage falls by 300 V and $A_{\nu} \approx 250$.
The time taken to fully tum on is thus given by:

$$
\begin{equation*}
t_{2}=\tau_{2} \ln \frac{V_{\text {dive }}}{V_{\text {divi }}-V_{t}-1.2} \tag{AI.7}
\end{equation*}
$$

$$
\begin{equation*}
\tau_{2}=\left(R_{g}+R_{\text {drive }}\right)\left(C_{s s}+\left|A_{v}\right| C_{d s}\right) \tag{AI.8}
\end{equation*}
$$

Substituting values typical of an IRF450 gives current rise time $t_{2} \approx 22 \mathrm{~ns}$

## c Time Taken to Complete Charging of Gate ( $\mathrm{t}_{3}$ )

The gate charging is completed with no further increase in $i_{d}$ or decrease in $v_{d}$, the time taken for the gate voltage to reach $99 \%$ of its final value is given by:

$$
\begin{equation*}
t_{3}=\tau_{3} \ln \frac{V_{\text {divw }}-V_{t}-1.2}{\left(V_{\text {dinu }}-V_{1}-1.2\right)(1-0.99)} \tag{AI.9}
\end{equation*}
$$

$$
\begin{equation*}
\tau_{3}=\left(R_{d \text { dive }}+R_{d}\right)\left(C_{d t}^{\prime}+C_{d d}\right) \tag{AI.10}
\end{equation*}
$$

$C_{d q}{ }^{\prime}$ is approximately ten times larger than $C_{d q}$ since the voltage across the depletion layer when $v_{d,}$ falls below $v_{g}$ is reversed. Thus the time taken to over drive the transistor $\left(t_{3}\right)$ is approximately 13 ns .

Region three is an over drive region and serves two purposes, one to ensure that conduction loss • of the MOSFET is a minimum (over driving reduces 'on' resistance slightly) and two, to provide a certain amount of noise immunity.

## ii Turn Off

## a Time Taken to Remove Excess Charge

The first turn off interval is concerned with removing the excess charge from the input capacitance, $C_{i s n}$ until the gate voltage falls to such a level as to just be able to sustain the maximum drain current flowing.

Assuming that the MOSFET drive is not reversed but taken to ground, the time taken to remove the excess charge is given by:

$$
\begin{equation*}
t_{4}=\tau_{3} \ln \frac{V_{\text {dinu }}}{V_{\text {dine }}-V_{t}+1.2} \tag{Al.11}
\end{equation*}
$$

Substituting in the relevant values gives $t_{4}=9 \mathrm{~ns}$.

## b Turn Off Fall Times

The second turn off interval concerns the time taken for the gate voltage to fall from that which will just sustain the maximum drain current to that which just prevents current from flowing (i.e. threshold). The current fall time calculation is further complicated by the time taken for the device output capacitance to charge to the supply voltage via the load.

The charging current available for $C_{i \text { ier }}$ depends on the rate of fall of the device drain current which in tum depends on the rate of fall of the device gate voltage (i.e. $\left.i_{d}=\left(v_{g z}-V_{t}\right) / g_{m}\right)$.

$$
\begin{align*}
& t=\tau_{2} \ln \left(\frac{V_{t}+\frac{i_{4}}{z_{m}}}{V_{s t}}\right)  \tag{AI.12}\\
& \tau_{2}=\left(R_{z}+R_{d c_{m}}\right)\left(C_{g a}+\left|A_{v}\right| C_{d q}\right) \tag{AI.8}
\end{align*}
$$

Here though $A_{v}$ is less than at turn on (for a purely resistive load), since the rate of rise of the drain voltage is limited by the charging time of $C_{d}$ and $C_{d y}$.

In order to keep the calculation simple at this point, it is necessary to make a number of assumptions. Assuming that the gate voltage falls to threshold in 30 ns (i.e. the time of the plateau region is the same at turn off as at tum on) and that $i_{d}$ falls linearly during this time, then the voltage available to charge the output capacitance is approximately half of the supply voltage.

During the 30 ns taken to remove charge from the gate, reducing the gate below threshold, thus reducing the drain current to zero, the drain voltage will rise to:

$$
\begin{equation*}
v_{d r}=\frac{V_{d 4}}{2}\left(1-\mathrm{e}^{-\frac{1}{4}}\right) \tag{AI.13}
\end{equation*}
$$

$$
\begin{equation*}
\tau_{4}=R_{\ell}\left(C_{d s}^{\prime}+C_{d s}\right) \tag{AI.14}
\end{equation*}
$$

Substituting in the relevant values gives $v_{d t} \approx 0.17 V_{d d}$.

As the device completes turm off, the remaining load current which flows is that needed to charge $C_{o w}$. The time taken for $v_{d d}$ to reach $90 \%$ of the supply voltage is:

$$
\begin{equation*}
t_{s}=\tau_{5} \frac{V_{d u}(1-0.17)}{V_{d u}(1-0.17)-0.9 V_{d t}(1-0.17)} \tag{AI.15}
\end{equation*}
$$

$$
\begin{equation*}
\tau_{s}=R_{L}\left(C_{d e}+C_{d}\right) \tag{AI.16}
\end{equation*}
$$

## Giving $t_{5} \approx 9$ ns

Thus the total time required to take the MOSFET from fully off to fully on and back to fully off is:

$$
\begin{equation*}
t_{\text {midching }}=t_{1}+2 t_{2}+t_{3}+t_{4}+t_{5} \tag{AI.17}
\end{equation*}
$$

For an $\operatorname{RF} 450$ switching $12 \mathrm{~A}, 300 \mathrm{~V}$ with a 14 V gate drive and drive resistance of $1 \Omega$ :

$$
t_{\text {muichine }}=75 \mathrm{~ns}
$$

The above calculation neglects the effects of lead inductance, particularly source inductance which slows switching speeds due to source feedback effects.

Appendix II
CALCULATION OF POWER DISSIPATED IN MOSFET GATE
Considering the much simplified gate equivalent circuit of Figure AII. 1 to which is applied a step change in voltage.


Figure AII. 1 Simplified MOSFET Gate Circuit.
The energy transferred to the gate during turn on is given by:

$$
\begin{align*}
& E=\int_{0}^{m} R_{z} i_{z}^{2}(t) d t  \tag{AII.1}\\
& i_{z}(t)=\frac{V_{\text {dive }}}{R_{z}} \mathrm{e}^{-\frac{1}{2}}  \tag{AII.2}\\
& \tau=R_{z} C_{i s s}
\end{align*}
$$

Where: $\quad C_{\text {iss }} \quad$ is the MOSFET input capacitance;
$i_{z} \quad$ is the gate current;
$R_{g} \quad$ is the MOSFET intrinsic gate resistance;
$V_{\text {dive }}$ is the gate drive voltage.

## Combining and integrating gives:

$$
\begin{equation*}
E=\frac{\tau}{2} \frac{V_{\text {dinu }}^{2}}{R_{s}}=\frac{1}{2} C_{i v e} V_{\text {dine }}^{2} \tag{AII.4}
\end{equation*}
$$

This energy is also extracted from the input capacitance during turn off. Thus for a switching frequency of $f_{s} \mathrm{~Hz}$, the power dissipated in the gate is given by:

$$
\begin{equation*}
P_{s}=C_{i u} V_{d i v}^{2} f_{s}=Q_{s} V_{\text {diviv }} f_{z} \tag{AII.5}
\end{equation*}
$$

Where $Q_{\boldsymbol{B}}$ is the charge transferred to and extracted from the gate during each cycle.
If the gate drive contains source resistance $R_{\text {dime }}$ then Equation AII. 5 is modified to:

$$
\begin{equation*}
P_{s}=Q_{s} V_{\text {divin }} f_{1}\left(\frac{R_{s}}{R_{\text {dive }}+R_{z}}\right) \tag{AII.6}
\end{equation*}
$$

## Appendix III

## DESIGN EQUATIONS FOR CLASS E INVERTER

The full design equations for the Class E inverter are given below; a basic Class E inverter is shown in Figure 3.10, repeated here for convenience. The well defined nature of the Class E inverter allows the design equations to be used with a high degree of accuracy. A computer program written in BASIC and incorporating these equations is given in Appendix IV. Full derivation of the design equations can be obtained from the following references: Sokal et al. 1975; Raab 1977; Redl et al. 1986.


Figure 3.10 Basic Class E Inverter.
The delivered output power of the Class E inverter is given by:

$$
\begin{align*}
P & =\frac{V_{d d}^{2}}{R_{L}} \frac{2}{\left.\frac{\pi^{2}}{4}+1\right)} f\left(Q_{L}\right)  \tag{AIII.1}\\
& =\frac{V_{d d}^{2}}{R_{L}} 0.5768\left[1.0012-\frac{0.4517}{Q_{L}}-\frac{0.4024}{Q_{L}^{2}}\right] \tag{AII.2}
\end{align*}
$$

Where: $\quad Q_{L} \quad$ is the loaded $Q$ of the output network and can take any value from 1.7879 to infinity;
$R_{L} \quad$ is the load resistance;
$V_{d d} \quad$ is the supply voltage.

The shunt capacitor $\left(C_{1}\right)$ value is given by:

$$
\begin{equation*}
C_{1}=\frac{0.21}{2 \pi f R_{L}} \tag{AIII.3}
\end{equation*}
$$

Where: $\quad f$ is the frequency of operation.

The supply inductor $\left(L_{1}\right)$ is given by:

$$
\begin{equation*}
L_{1}=\frac{10}{(2 \pi f)^{2} C_{1}} \tag{AIII.4}
\end{equation*}
$$

The output inductor $\left(L_{2}\right)$ value is given by:

$$
\begin{equation*}
L_{2}=\frac{Q_{L} R_{L}}{2 \pi f} \tag{AIII.5}
\end{equation*}
$$

The output capacitor $\left(C_{2}\right)$ value is given by:

$$
\begin{equation*}
C_{2}=\frac{1.35}{(2 \pi f)^{2} L_{2}} \tag{AIII.6}
\end{equation*}
$$

The choice of $Q_{L}$ involves a trade-off. In RF applications, the trade-off is among operating bandwidth (wider with low $Q_{\nu}$, harmonic content of the output power (lower with high $Q_{\nu}$ ), and power loss in the parasitic resistances of the load-network inductor $L_{2}$ and capacitor $C_{2}$ (lower with low $Q_{L}$ ). In power inverters, the trade-off is among power loss in the parasitic resistances of the load-network inductor $L_{2}$ and capacitor $C_{2}$ (lower with low $Q_{L}$ ), frequency range required of the variable-frequency oscillator used in the voltage control system (wider with low $Q_{\nu}$ ), and asymmetry in peak magnetising force applied to the output coupling transformer (larger with low $Q_{L}$ ). For power inverters a figure for the loaded $Q$ of 5 provides a reasonable compromise.

## Appendix IV <br> BBC BASIC PROGRAM LISTINGS

This appendix contains the listings of the BBC BASIC programs mentioned in the preceding chapters.

```
i Class E Inverter Design Program
    1 REM PROGRAM SELECT
    2 PRINT " Class E component calculation program"
    3 PRINT
    4 PRINT"Do you want to specify:"
    5 PRINT"transistor parameters (1)"
    6 INPUT"or load and power required (2)";PROG
    7F PROG = 1 THEN PROCInput1 ELSE IF PROG = 2 THEN PROCInput2
        ELSE GOTO 5
    55 PRINT:INPUT " OPERATING FREQUENCY ",F
    56 PRINT:INPUT " DESIRED Q FACTOR ",Q
110 PRINT:PRINT
170 REM NOW CALCULATE CLASS E COMPONENT VALUES
175 W=2*PI*F
180 C1=(0.1836/(W*RLOAD)**(1+0.81*Q/(Q*Q+4))
190 L2=Q*RLOAD/W
200 C2=(1/(W*Q*RLOAD))*(1+(1.11/(Q-1.7879)))
210 Ll=10/(W*W*C1)
225 VDU2:PRINT
230 IF PROG=1 THEN PRINT "REQUIRED COMPONENT VALUES FOR CLASS E"
231 IF PROG=1 THEN PRINT"RUNNING AT ";F/IE6;" MHz
    USING ";TRAN$;" ARE:"
235 IF PROG=2 THEN PRINT "REQUIRED COMPONENT VALUES FOR CLASS E"
236 IF PROG = 2 THEN PRINT"DELIVERING ";POUT;" W INTO ";RLOAD;
    " OHMS AT";F/1E6;" MHz ARE:"
240 PRINT: PRINT"Cl = ",C1
250PRINT:PRINT "L2 = ",L2
260PRINT:PRINT"C2 = ",C2
270PRINT:PRINT " L1 = ",L1
280 PRINT:PRINT "IDC = ",IDC
290 PRINT:PRINT " VDC = ",VDC
295 PRINT:PRINT " RLOAD = ",RLOAD
296 PRINT:PRINT "Q = ",Q
300 REM REQUIRED COMPONENT VALUES
310 IOUT = SQR(POUT/RLOAD)
320 VC2 =IOUT/(W*C2)
330 VC1 = VDSM
335 PRINT:PRINT"WITH 20% DERATING, REQUIRED COMPONENT RATINGS ARE:"
```

```
340 PRINT:PRINT "OUTPUT CURRENT = ",IOUT
343 PRINT "INPUT POWER = ",PIN
347 PRINT "OUTPUT POWER = ",POUT
350 PRINT:PRINT "VOLTAGE RATING CF C1 = ";VC1
355 PRINT:PRINT "CURRENT RATING OF C2 = ";IOUT/0.8
360 PRINT:PRINT "VOLTAGE RATING OF C2 = ";VC2/0.8
363 PRINT:PRINT "MAX DRAIN VOLTAGE = ";VDSM
365 PRINT:PRINT "RMS DRAIN CURRENT = ";IDRMS
370 PRINT:PRINT "PEAK DRAIN CURRENT = ";IDPK
374 PRINT
375 IF PROG = 1 THEN PRINT "POWER DISSIPATED IN DEVICE =";
    IDRMS*IDRMS*RDSON
380 FOR X=1 TO 10
390 PRINT
4 0 0 ~ N E X T ~ X ~
410 VDU3
420 PRINT "ANOTHER RUN? Y/N "
430 IF GET$ = "Y" THEN GOTO 5
4 4 0 \text { END}
1000 DEF PROCInput1
1010 PRINT:INPUT " Transistor type number ",TRAN$
1020 PRINT:INPUT " MAX VDD ",VDSM
1030 PRINT:INPUT " MAX CONTINUOUS DRAIN CURRENT AT TC = 60K ",IDCON
1040 PRINT:INPUT "DEVICE ON RESISTANCE RDSON ",RDSON
1050 REM This section calculates the max power possible
    to be delivered to load
1060 REM DERATE COMPONENT
1070 VDSM=0.8*VDSM:IDRMS=0.8*IDCON
1080 REM IPEAK=2.86IDC, VPEAK=3.56VDD,IDRMS=1.5*IDC
1090 VDC=VDSM/3.56
1100 IDC=IDRMS/1.5
1120 PIN=VDC*IDC
1130 REM ASSUMING 90% EFFICIENCY
1140 POUT = 0.9*PIN
1150 REM NOW CALCULATING REQUIRED LOAD RESISTANCE
1160 RLOAD=(0.58*VDC*VDC)/POUT
1170 REM Return original transistor ratings
1180 IDPK = IDC*2.86/0.8:IDRMS=IDC*1.5/0.8:VDSM=VDSM/0.8
1190 ENDPROC
2000 DEF PROCInpuL2
2010 PRINT:INPUT" REQUIRED OUTPUT POWER";POUT
2020 PRINT:INPUT" REQUIRED LOAD RESISTANCE";RLOAD
```

```
2030 REM Now calculate input voltage and current
2040 VDC=SQR(POUT*RLOAD/0.58)
2050 REM Assuming 90% efficiency
2060 PN :: PDUT/0.9
2070 IDC = PIN/VDC
2080 REM Calculate transistor requirements with 80% derating
2090 IDRMS = IDC*1.5/0.8
2100 IDPK = IDC*2.86/0.8
2110 VDSM = VDC*3.56/0.8
2120 ENDPROC
```

```
ii Brooks Coil Design Program
    10 REM This program calcultes the dimension and wire size for
    20 REM optimum geometry Brooks coil formers
    30 REM This program is called ..... BROOKSCOIL
    40 PRINT " Program to calculate wire diameter and dimensions of "
    50 PRINT " former for a Brooks coil inductor "
    6 0 ~ P R I N T : I N P U T " ~ R e q u i r e d ~ i n d u c t o r ~ v a l u e ~ H ~ " ; L ~
    70 PRINT:INPUT" Required current carrying capability (RMS Amps)";I
    80 PRINT:INPUT" Estimated stacking factor of wire ";S
    90 REM Assuming an allowable current density of 3A/mm^2
    100 DIA = SQR(I*4/(PI*3E6))
    110 DF = SQR((PI*DIA^2)/(4*S))
    120 N = (L/(2.029*4E-7*PI*DF))^(2/5)
    130 C = DF*SQR(N)
    140 VDU2:PRINT
    150 PRINT"Brooks coil dimensions for ";L*1E6;"uH inductor carrying"
    160 PRINT;" ";I;" amps are as follows:"
    180 PRINT:PRINT" Required wire diameter is ";DIA*1E3;" mm"
    185 IF N-INT(N)>0.5 THEN NUMBER = INT(N)+1 ELSE NUMBER = INT(N)
    190 PRINT:PRINT" Required number of turns are ";NUMBER
    200 PRINT:PRINT" Dimension of side of square of Brooks coil 'C' is "
    ;C*1E3;"mm"
210FOR X=1 TO 10
2 2 0 ~ P R I N T ~
230 NEXT X
240 VDU3
250 PRINT" Another run Y/N ?"
260 IF GET$ = "Y" THEN GOTO 60
270 END
```

```
iii Minimum Wire Length Air Cored Toroid Design Program
    10 REM Program to calculate dimensions of air cored toroids
    20 REM based on PNM'S method for minimum wire length
    30 REM The name of this program is COILCAL
    40 REM
    50 REM First determine wire diameter
    60 PRINT "Program to calculate dimensions of air cored toroids"
    70 PRINT "with square cross section"
    80 PRINT:INPUT" Specify 1)Current or 2) wire diameter";AorD
    90 IF AorD = 2 GOTO 120
    100 PRINT:INPUT"Required current handling cpapbilty A";I
    110 DIA=SQR(**4/(PI*3E6)
    120 IF AorD = 2 THEN PRINT:INPUT" Required wire diameter mm";DIA
    130 IF AorD = 2 THEN DIA=DIA/1000
    140 REM inductance
    150 PRINT:INPUT"Required inductance uH";L
    160 REM Calculation of unitless inductance
    170 Lo=2E-7*DIA
    180 L_UNTT = L/(LO*1E6)
    190 REML_UNIT =0.2522K^3/2 +0.25K SOLVE FOR K
    200 KN=(L_UNIT/0.2522)^(2/3)
    2 1 0 ~ R E P E A T ~
    215 KO=KN
    220 KN=KO+0.01*(((L_UNIT-0.2522*KO^(3/2))/0.25)-KO)
    225 PRINT KN
    230 UNTIL ABS(KN-KO)<1E-3
    2 4 0 ~ K = K N ~
    500 REM Required wire length = W = DIA*K
    510 W = DIA*K
    520 REM Number of turns
    530 N=0.6329*SQR(K)
    540 IF N-INT(N)<0.5 THEN N=INT(N) ELSE N=INT(N)+1
    550 REM Side of square of torroid
    560 A=W/(4*N)
    570 REM Minor radius
    580 S=DIA/(2*SIN(PIN))
    590 REM Taking into account wire diameter
    60 A=A-DIA:S=S+DIA/2
    610 REM out put results
    6 2 0 ~ V D U 2 : P R I N T ~
    630 PRINT"Dimensions of square sectioned toroid for inductance ";
        L;" uH"
```

```
635 PRINT"carrying ";I;" amps are:"
640 PRINT:PRINT"Wire diameter is: ";DIA*1000;" mm"
650 PRINT:PRINT"Side of square is: ";A*1000;" mm"
660 PRINT:PRINT"Minor radius is: ";S*:000;" mm"
670 PRINT:PRNT"Wire length is: ";W;" m"
680 PRINT:PRINT"Number of tums required is: ";N
681 FOR X = 1 TO 10
6 8 2 \text { PRINT}
6 8 3 \text { NEXT X}
6 8 5 \text { VDU3}
6 9 0 ~ E N D
```

```
iv Matching Capacitor Value Design.Program
    10 REM PROGRAM TO CAĹCULATE REQUIRED MATCHING CAPACITORS TO MATCH
    20 PRINT " Program to calculate matching capacitor values."
    30 PRINT:INPUT "Amplifier output impedarce (OHMs)",ZOUT
    40 PRINT:INPUT "Required load impedance (OHMs)", ZLOAD
    50 PRINT:INPUT "Class E series output capacitance",Cs1
    60 PRINT:INPUT "Operating frequency (Hz)",F
    70 W=2*PI*F
    80 REM EFFECTIVE SERIES CAPACITOR FOR MATCHED LOAD
    90 Cs2=1/(W*(SQR(ZOUT*ZLOAD-ZOUT^2)))
    100 XCs2=1/(W*Cs2)
    110 REM REQUIRED PARALLEL MATCHING CAPACITOR
    120 Cp=Cs2/(1+((ZOUT^2)/(XCs2^2)))
    130 REM REQUIRED SERIES MATCHING CAPACITOR
    140 Cs=(Cs1*Cs2)/(Cs2-Cs1)
    150 REM PRINT RESULTS
    160 VDU2
    170 PRINT"Required matching capacitors"
    180 PRINT"Class E series output capacitor = ",Cs*1E12," pF"
    190 PRINT"Parallel load capacitor = ",Cp*1E12," pF"
    192 FOR I=1 TO 10
    194 PRINT
    196 NEXT I
    200 VDU3
    210 END
```


## Appendix V <br> BROOKS INDUCTOR DESIGN EQUATIONS

The Brooks inductor is a multi-layer solenoid formed on a former of characteristic dimension ' $c$ ' (Figure AV.1). 'The coil represents the optimum design for a solenoid in terms of maximum inductance for a given length and thickness of wire and hence highest $Q$.


Figure AV. 1 Brooks Coil Dimensions.
The inductance for a given number of turns wound on a 'Brooks' former of characteristic dimension ' $c$ ' is given by:

$$
\begin{equation*}
L_{B}=2.209 \mu_{0} c N^{2} \tag{AV.1}
\end{equation*}
$$

Where: $\quad L_{B}$ is the inductance of the Brooks inductor;
$c$ is the characteristic dimension of the former,
$N$ is the number of turns of wire.
$\mu_{0}$ is the permeability of free space $\left(4 \pi \times 10^{-7}\right)$

When designing an inductor, the current and inductance required is known and what is required is the dimension of the former and the diameter and number of turns of wire. If the maximum current rating of a Brooks coil is $I_{\text {max }}$ then

$$
\begin{equation*}
I_{\max }=\frac{J_{\max } c^{2}}{N} \tag{AV.2}
\end{equation*}
$$

Where: $\quad J_{\text {max }}$ is the allowable current density.

Using Equation AV. 1 the 'backwards' design problem is solved by:

$$
\begin{align*}
& c=s \sqrt{\frac{L_{B} I_{m}^{2}}{2.029 \mu_{0} \sigma_{m}^{2}}}  \tag{AV.3}\\
& N=s \sqrt{\frac{L_{B}^{2} J_{m}}{4.117 \mu_{o}^{2} I_{m}}} \tag{AV.4}
\end{align*}
$$

## Appendix VI <br> PSPICE SIMULATION PROGRAM LISTINGS

This appendix contains the listings of the PSpice simulation programs mentioned in the preceding chapters

## i IRF450 Switching Test - 1 Source Lead

IRF450 PULSE TEST INCLUDING DRIVE INDUCTANCE. 1 SOURCE LEAD, RL=12 OHMS .OPT ACCT NOMOD LIMPTS=8001 LIST OPTS NOPAGE RELTOL $=0.01$ ABSTOL=1E-3
.OPT ITL4=40 ITL5=0
.WIDTH OUT=80
.PROBE
.TRAN/OP INS 1.2us 0.0S 1NS
*SUPPLY VOLTAGES
VDD1 10 DC 300
VDD2 60 DC 14
*RESISTIVE ELEMENTS
RLOAD 1212
*MOSFETS
*MOSFET LEAD INDUCTANCES
*IRF450 INDUCTANCES
LD1 23 10nH
LS1 40 12.5NH
LG1a 57 6nH
LGlb 78 10nH
M1 3544 IRF450
*
*CALL DRIVER SUBCIRCUITS
XDRIVEa 6089 DRIVER
XDRIVEb 6089 DRIVER
XDRIVEc 6089 DRIVER
XDRIVEd 6089 DRIVER
*
.SUBCKT DRIVER 101100105109
*INDUCTANCES
*
*SOURCE INDUCTANCES
*
LSP 101102 15NH
LSN 10810015 NH
*
*DRAIN INDUCTANCES
*
LDP 1041055 NH

```
LDN 105 106 5NH
*
*GATE INDUCTANCES
*
LGP 103 109 15NH
LGN 107 109 15NH
*
*MOSFETS
*
M1 104 103 102 102 VP0300M
M2 106 107 108108 VN0300M
*
ENDS
*DRIVE WAVEFORM
VIN }90\mathrm{ PULSE(1400 2NS 2NS 60NS 200NS)
*SELECT VIEWING POINTS
.PRINT TRAN V(5) V(2) V(4) I(RLOAD) ID(M1) IG(M1) V(7)
*IRF450 MODEL
model IRF450 NMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0
+ Vmax =0 Xj=0 Tox=100n Uo=600 Phi=.6 Rs=32.16m Kp=20.69u
+ W=1.1 L=2u Vto=3.415 Rd=.2606 Rds=1.6MEG Cbd=400p Pb=.8
+ Mj=.5 Fc=.5 Cgso=1.636n Cgdo=91p Rg=0.982 Is=1E-30)
*VP0300M MODEL
* VP0300M model created using Parts version 1.03 on 03/03/88 at 14:48
*
model VP0300M PMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0 Vmax=0
+ Xj=0 Tox=100n Uo=300 Phi=.6 Rs=.4882 Kp=10.29u W=24m
+ L=2u Vto=-4.006 Rd=.5421 Rds=500K Cbd=320p Pb=.8 Mj=.5
+ Fc=.5 Cgso=1.2n Cgdo=0.78n Rg=1.26 Is=126.1E-18)
*VN0300M MODEL
* VN0300M model created using Parts version 1.03 on 03/03/88 at 15:20
*
.model VN0300M NMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0 Vmax=0
+
Xj=0 Tox=100n Uo=600 Phi=.6 Rs=.4242 Kp=20.65u W=39m
+ L=2u Vto=1.921 Rd=0 Rds=30MEG Cbd=100.0p Pb=.8 Mj=.5
+ Fc=.5 Cgso=ln Cgdo=0.5n Rg=.243 Is=126.1E-18)
END
```


## ii

RF450 Switching Test-2 Source Leads
IRF45O PULSE TEST INCLUDING DRIVE INDUCTANCE. 2 SOURCE LEADS, R=12 OHMS .OPT ACCT NOMOD LIMPTS=8001 LST OPTS NOPAGE RELTOL=0.01 ABSTOL=1E-3
. OPT ITLA=40 IIL $5=0$
.WIDTH OUT=80
PROBE
.TRAN/OP INS 1.2us 0.0 S ins
*SUPPLY VOLTAGES
VDDI 10 DC 300
VDD2612DC 14
*RESISTIVE ELEMENTS
RLOAD 1212
*MOSFETS
*MOSFETLEAD INDUCTANCES
*RF450 INDUCTANCES (WITH EXTRA SOURCE LEAD)
LD 23 10NH
LSal 40 12.5nH
LSbl 412 12.5nH
LGla 57 6nH
LG1b 78 9nH
M1 3544 RF450
*
*CALL DRIVER SUB CIRCUITS
*
XDRIVEa 61289 DRIVER
XDRIVEb 61289 DRIVER
XDRIVEC 61289 DRIVER
XDRIVEd 61289 DRIVER

## *

.SUBCKT DRIVER 101100105109
*
*INDUCTANCES
*
*SOURCE INDUCTANCES
*
LSP 101102 15NH
LSN 108100 15NH
*
*DRAIN INDUCTANCES
*
LDP 104105 5NH
LDN 105106 5NH

```
*
*GATE INDUCTANCES
*
LGP 103 109 15NH
LGN 107 109 15NH
*
*MOSFETS
*
M1 104 103 102 102 VP0300M
M2 106 107 108 108 VN0300M
*
ENDS
VIN }912\mathrm{ PULSE(1400 2NS 2NS 60NS 200NS)
*SELECT VIEWING POINTS
PRINT TRAN V(3) V(2)V(4) I(RLOAD) ID(M1) IG(M1) I(LSal)
.PRINT TRAN I(LSb1) IS(M1) V (5,12) V(7,12) V(4,12)
*IRF450 MODEL
model IRF450 NMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0
+ Vmax=0 Xj=0 Tox=100n Uo=600 Phi=.6 Rs=32.16m Kp=20.69u
+ W=1.1 L=2u Vto=3.415 Rd=.2606 Rds=1.6MEG Cbd=400p Pb=.8
+ Mj=.5 Fc=.5 Cgso=1.636n Cgdo=91p Rg=0.982 Is=1E-30)
*VP0300M MODEL
* VP0300M model created using Parts version 1.03 on 03/03/88 at 14:48
*
.model VP0300M PMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0 Vmax=0
+ Xj=0 Tox=100n Uo=300 Phi=.6 Rs=.4882 Kp=10.29u W=24m
+ L=2u Vto=-4.006 Rd=.5421 Rds=500K Cbd=320p Pb=.8 Mj=.5
+ Fc=.5 CgsO=1.2n Cgdo=0.78n Rg=1.26 Is=126.1E-18)
*VN0300M MODEL
* VN0300M model created using Parts version 1.03 on 03/03/88 at 15:20
*
model VN0300M NMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0 Vmax=0
+ Xj=0 Tox=100n Uo=600 Phi=.6 Rs=.4242 Kp=20.65u W=39m
+ L=2u Vto=1.921 Rd=0 Rds=30MEG Cbd=100.0p Pb=.8 Mj=.5
+ Fc=.5 Cgso=1n Cgdo=0.5n Rg=.243 Is=126.1E-18)
.END
```


## iii $\quad 7 \mathrm{MHz}$ Class E Simulation Using Switch Models

CLASS E 7MHz 200W SIMULATION USING SWITCH MODELS
.OPT ACCT NOMOD LIMPTS=8001 LIST OPTS NOPAGE RELTOL=0.01 ABSTOL=1E-3
.OPT ITLA=40 ITL5=0
.WIDTH OUT $=80$
.PROBE
.TRAN/OP INS 4US 0.0S INS UIC
*SUPPLY VOLTAGES
VDD1 10 DC 45
VDD2 60 DC 12
*INDUCTIVE ELEMENTS
L1 12 6UH IC=4A
L2 23 0.63UH
*CAPACITIVE ELEMENTS
C1 20 760PF
C2 34 1.1NF
CGD 25 120PF
CGS 50 600PF
*RESISTIVE ELEMENTS
RLOAD 10050
*OUTPUT TRANSFORMER (IDEAL)
KTRANS LP LS 0.9999
LP 40 1UH
LS 10090 H
*IDEAL SWITCHES
S1 2050 SIMOD
S26570 S2MOD
S3 5070 S3MOD
.MODEL S1MOD VSWITCH(RON=0.4 ROFF=500K VON=7.5 VOFF=4)
.MODEL S2MOD VSWITCH(RON=1.25 ROFF=30MEG VON=3 VOFF=6)
.MODEL S3MOD VSWITCH(RON=0.60 ROFF=30MEG VON=6 VOFF=3)
*GATE DRIVE WAVEFORM
VIN 70 PULSE(0 1204 NS 4NS 71.5NS 143NS)
*SELECT MEASUREMENT POINTS
PRINT TRAN V(5) V(2) V(4) I(C1) I(RLOAD) I(S1) I(CGD) I(S2)
.PRINT TRAN I(S3) I(Ll)
END

### 3.3 MHz 500 W Class E Simulation

CLASS E 3.3 MHz 500W SIMULATION. INCLUDING MAIN PARASITIC COMPONENTS.
.OPT ACCT NOMOD LIMPTS=8001 LIST OPTS NOPAGE RELTOL=0.02 ABSTOL=2E-3
.OPT ITLA=40 ITL5=0
.WIDTH OUT=80
PROBE
.TRAN/OP 1NS 10US 0.0S 4NS UIC
*SUPPLY VOLTAGES
VDD1 10 DC 110
VDD2 100 DC 12
*INDUCTIVE ELEMENTS
L1 12 30UH IC=4.8A
L2 34 3UH
*IRF450 LEAD INDUCTANCE
LD1 37 5NH
LS1 80 13NH
LG1 911 13NH
*OUTPUT TRANSFORMER
*PRIMARY
LPRIMARY 601
*SECONDARY
LSECONDARY 2002
KTRNSFRM LPRIMARY LSECONDARY 0.999
*CAPACITIVE ELEMENTS
C1 30 510PF
C2 56 1NF
*RESISTIVE ELEMENTS
RLOAD 20050
*L1 SERIES LOSS RESISTOR
RL1 230.01
*L2 SERIES LOSS RESISTOR
RL2 450.20
*MOSFETS
M1 7988 IRF450
*CALL DRIVE SUBCIRCUITS
*
XDRIVEa 1001112 DRIVER
XDRIVEb 1001112 DRIVER
*
*GATE DRIVE WAVEFORM
VIN 120 PULSE(0 120 10NS 10NS 141.5NS 303NS)

```
.SUBCKT DRIVER 101 100 105109
*INDUCTANCES
*
*SOURCE INDUCTANCES
*
LSP 101 102 3NH
LSN 108 100 3NH
*
*GATE INDUCTANCES
*
LGP 103 109 3NH
LGN 107 109 3NH
*
*DRAIN INDUCTANCES
*
LDP 104 105 2.5NH
LDN 105 106 2.5NH
*
*MOSFETS
*
M1 104 103 102 102 VP0300M
M2 106 107 108 108 VN0300M
*
ENDS
*SELECT VIEWING POINTS
.PRINT TRAN V(6) V(3) V(7) I(Cl) I(RLOAD) ID(M1) IG(M1) I(L1)
PRINT TRAN V(10)
*IRF450 MODEL
.model IRF450 NMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0
+ Vmax=0 Xj=0 Tox=100n Uo=600 Phi=.6 Rs=32.16m Kp=20.69u
+ W=1.1 L=2u Vto=3.415 Rd=.2606 Rds=1.6MEG Cbd=400p Pb=.8
+ Mj=.5 Fc=.5 Cgso=1.636n Cgdo=91p Rg=0.982 Is=1E-30)
*VP0300M MODEL
* VP0300M model created using Parts version 1.03 on 03/03/88 at 14:48
*
model VP0300M PMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0 Vmax=0
+ Xj=0 Tox=100n Uo=300 Phi=.6 Rs=.4882 Kp=10.29u W=24m
+ L=2u Vto=-4.006 Rd=.5421 Rds=500K Cbd=320p Pb=.8 Mj=.5
+ Fc=.5 Cgso=1.2n Cgdo=0.78n Rg=1.26 Is=126.1E-18)
```

*VN0300M MODEL

* VN0300M model created using Parts version 1.03 on 03/03/88 at 15:20
* 

.model VN0300M NMOS(Level $=3$ Gamma $=0$ Delta $=0$ Eta $=0$ Theta $=0$ Kappa=0 Vmax $=0$
$+\quad \mathrm{Xj}=0 \mathrm{Tox}=100 \mathrm{n} \mathrm{Uo}=600 \mathrm{Phi}=6 \mathrm{Rs}=.4242 \mathrm{Kp}=20.65 \mathrm{u} \mathrm{W}=39 \mathrm{~m}$
$+\quad \mathrm{L}=2 \mathrm{u}$ Vto $=1.921 \mathrm{Rd}=0 \mathrm{Rds}=30 \mathrm{MEG} \mathrm{Cbd}=100.0 \mathrm{p} \mathrm{Pb}=.8 \mathrm{Mj}=.5$
$+$ $\mathrm{Fc}=.5 \mathrm{Cgso}=1 \mathrm{n} \mathrm{Cgdo}=0.5 \mathrm{n} \mathrm{Rg}=.243 \mathrm{Is}=126.1 \mathrm{E}-18$ )
END

## v $\quad 2.4 \mathrm{~kW} 3.3 \mathrm{MHz}$ Class E Simulation

CLASS E 3.3MHz 2.4kW PUSH PULL SIMULATION INC. PARASITICS.

* INCLUDING ALL MAIN PARASITIC ELEMENTS.
.OPT ACCT NOMOD LIMPTS=8001 LIST OPTS NOPAGE RELTOL=0.04 ABSTOL=4E-3
.OPT ITL4=40 ITL5 $=0$
.WIDTH OUT=80
PROBE
.TRAN/OP 1NS 7.5US 6US 4NS UIC
*SUPPLY VOLTAGES
VDD1 10 DC 114
VDD2 80 DC 12
*MAIN CIRCUIT DESCRIPTION
*CALL IRF450,RFC, SHUNT CAPACITOR SUBCIRCUIT
XML1Cla 10258 MLICl
XML1C1b 10468 MLIC1
* 

*DC BLOCKING CAPACITOR
CBLOCK 23 4UF
*OUTPUT TRANSFORMER (IDEAL)
KTRANS LP LS 0.9999
LP 34 10UH
LS 71040 UH
*OUTPUT CIRCUIT

C2 78 260PF
L2 89 12.05UH
RLOAD 91050
*DRIVE WAVEFORMS TO DRIVE CIRCUITS
VINa 50 PULSE(0 120 5NS 5NS 151.5NS 303NS)
VINb 60 PULSE(0 12 151.5ns 5NS 5NS 151.5NS 303NS)
*subcircuits
.SUBCKT MLIC1 101100102103104
*RFC
L1 101102 14UH IC=12A
*SHUNT CAPACITOR
C1 102100 INF

```
*CALL MOSFET AND DRIVER SUIBCIRCUIT
XMOSa 102100 103 104 MOS
XMOSb 102100103104 MOS
ENDS
.SUBCKT MOS 201 }20020620
*MOSFET LEAD INDUCTANCE
LD 201 202 5NH
LS 203200 13NH
LG 204 205 13NH
*IRF450
M1 202204203203 IRF450
*CALL DRIVER SUBCIRCUIT
XDRIVEa 207 200 205 206 DRIVER
XDRIVEb 207 200 205206 DRIVER
ENDS
.SUBCKT DRIVER 301 300 305 309
*INDUCTANCES
*SOURCE INDUCTANCES
*
LSP 301 302 3NH
LSN }3083003N
*
*GATE INDUCTANCES
LGP }303309\mathrm{ 3NH
LGN }307309\mathrm{ 3NH
*
*DRAIN INDUCTANCES
*
LDP 304 305 2.5NH
LDN }3053062.5N
*
*MOSFETS
*
M1 304 303 302 302 VP0300M
M2 306307308308 VN0300M
*
ENDS
*SELECT VIEWING POINTS
```

```
PRINT TRAN V(2) V(4) V(9,10)
*IRF450 MODEL
model IRF450 NMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0
+ Vmax=0 Xj=0 Tox=100n Uo=600 Phi=.6 Rs=32.16m Kp=20.69u
+ W=1.1 L=2u Vto=3.415 Rd=.2606 Rds=1.6MEG Cbd=400p Pb=.8
+ Mj=.5 Fc=.5 Cgso=1.636n Cgdo=91p Rg=0.982 Is=1E-30)
*VP0300M MODEL
* VP0300M model created using Parts version 1.03 on 03/03/88 at 14:48
*
model VP0300M PMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0 Vmax=0
+ Xj=0 Tox=100n U0=300 Phi=.6 Rs=.4882 Kp=10.29u W=24m
+ L=2u Vto=-4.006 Rd=.5421 Rds=500K Cbd=320p Pb=.8 Mj=.5
+ Fc=.5 Cgso=1.2n Cgdo=0.78n Rg=1.26 Is=126.1E-18)
*VN0300M MODEL
* VN0300M model created using Parts version 1.03 on 03/03/88 at 15:20
.model VN0300M NMOS(Level=3 Gamma=0 Delta=0 Eta =0 Theta=0 Kappa=0 Vmax=0
+ Xj=0 Tox=100n Uo=600 Phi=.6 Rs=.4242 Kp=20.65u W=39m
+ L=2u Vto=1.921 Rd=0 Rds=30MEG Cbd=100.0p Pb=.8 Mj=.5
+ Fc=.5 CgsO=1n Cgdo=0.5n Rg=.243 Is=126.1E-18)
END
```

CLASS E 7MHz 200W SIMULATION USING MOSFET MODELS
.OPT ACCT NOMOD LIMPTS=8001 LIST OPTS NOPAGE RELTOL=0.01 ABSTOL=1E-3
.OPT ITL $4=40$ ITL $5=0$
.WIDTH OUT=80
PROBE
.TRAN/OP INS 4US 0.0S INS UIC
*SUPPLY VOLTAGES
VDD1 10 DC 50
VDD2 60 DC 12
*INDUCTIVE ELEMENTS
L1 12 6UH IC=4A
L2 230.63 UH
*CAPACITIVE ELEMENTS
C1 20 560PF
C2 34 1.1NF
*RESISTIVE ELEMENTS
RLOAD 405.5
*MOSFETS
M1 2500 IRF630
M3 5766 VP0300M
M2 5766 VP0300M
M4 5700 VN 0300 M
M5 5700 VN0300M
*GATE DRIVE WAVEFORM
VIN 70 PULSE(0 120 4NS 4NS 71.5NS 143NS)
*SELECT VIEWING POINTS
.PRINT TRAN V(5) V(2) V(4) I(C1) I(RLOAD) ID(M1) IG(M1) I(L1)
PRINT TRAN ID(M2) ID(M3)
*IRF630 MODEL

* IRF630 model created using Parts version 1.03 on 03/03/88 at 12:51 *
.model IRF630 NMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0 Vmax=0
$+\quad \mathrm{Xj}=0 \mathrm{Tox}=100 \mathrm{n} \mathrm{Uo}=600 \mathrm{Phi}=.6 \mathrm{Rs}=.1067 \mathrm{Kp}=20.81 \mathrm{u} \mathrm{W}=.78$
$+\quad \mathrm{L}=2 \mathrm{u}$ Vto=3.356 $\mathrm{Rd}=.1641 \mathrm{Rds}=800 \mathrm{~K} \mathrm{Cbd}=1.111 \mathrm{n} \mathrm{Pb}=.8 \mathrm{Mj}=.5$
$+\quad \mathrm{Fc}=.5 \mathrm{Cgso}=1.00 \mathrm{n} \mathrm{Cgdo}=220.3 \mathrm{p} \mathrm{Rg}=3.0+\mathrm{Is}=1 \mathrm{E}-30)$
*VP0300M MODEL
* VP0300M model created using Parts version 1.03 on 03/03/88 at 14:48
* 

model VP0300M PMOS(Level=3 Gamma $=0$ Delta=0 Eta=0 Theta=0 Kappa=0 Vmax $=0$

```
+ Xj=0 Tox=100n Uo=300 Phi=.6 Rs=.4882 Kp=10.29u W=24m
+ L=2u Vto=-4.006 Rd=.5421 Rds=500K Cbd=320p Pb=.8 Mj=.5
+
Fc=.5 Cgso=1.2n Cgdo=0.78n Rg=1.26 Is=126.1E-18)
*VN0300M MODEL
* VN0300M model created using Parts version 1.03 on 03/03/88 at 15:20
.model VN0300M NMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0 Vmax=0
+ Xj=0 Tox=100n Uo=600 Phi=.6 Rs=.4242 Kp=20.65u W=39m
+ L=2u Vto=1.921 Rd=0 Rds=30MEG Cbd=100.0p Pb=.8 Mj=.5
+
    Fc=.5 Cgso=1n Cgdo=0.5n Rg=.243 Is=126.1E-18)
END
```


## Appendix VII <br> MEASUREMENT TECHNIQUES

In this appendix some of the measurement techniques mentioned in the preceding chapters are described.

## i Oscilloscope Measurements

When making voitage measurements of high frequency waveforms using a wide bandwidth oscilloscope, especially in switched mode converter/inverter applications where fast rise times occur, it is necessary to take a few precautions to obtain reliable readings.

The extra inductance introduced by the oscilloscope probe earth connection can have a significant influence on the waveform observed. The most common method of connecting an oscilloscope ground connection to a circuit is via a 150 mm earth lead, this causes significant ringing. Even a 25 mm earth connection can cause significant overshoot of rising edges. One method of avoiding this is to use a coaxial probe connection. Common mode ground interference can be reduced by running the oscilloscope coaxial lead through a ferrite core.

An example of the ringing caused by the oscilloscope probe ground lead is demonstrated in Figure AVII. 1 where two oscillograms of the TTL signal to a high frequency MOSFET driver (upper trace) and resulting gate drive voltage waveform (lower trace) are shown. In both oscillograms, the waveforms were monitored at the same point. Figure VII.1(a) shows the observed waveforms when using a standard 150 mm earth lead, apparent overshoot at the unloaded gate drive ouput is approximately 4 V with considerable ringing occurring. Figure AVII.1(b) shows the same waveforms, in this case the TTL drive signal was coupled to the oscilloscope $50 \Omega$ input via a $50 \Omega$ signal splitter, the oscilloscope probe was coupled to the gate drive output by means of a miniature coaxial socket. The overshoot measured by this technique is only 1.5 V with no significant ringing occurring.

When the voltage to be measured is with respect to a point above ground, the malpractice of 'floating' the oscilloscope either by use of an isolating transformer, or disconnection of earth lead should be avoided since this will eliminate transients by loading the circuit which reappear after disconnecting the probe.

A better method to measure floating potentials is to use a differential amplifier, using the 'add and invert' function of an oscilloscope is not a good technique since bandwidth is compromised and the common mode rejection ratio is poor at high frequencies. Unfortunately there are few wide bandwidth differential amplifiers on the market which are able to measure differential voitages above a few tens of volts.

When measuring rise times of the order of a few nano seconds it is necessary to compensate for effects of probe and oscilloscope rise times, for example a signal having a 1 ns rise time monitored using an oscilloscope having a 1 ns rise time will have an apparent rise time of 1.42 ns. Figure AVII2 gives suitable compensation curves.


Figure AVII. 1 (a) Waveforms Measured Conventionally (2 V/Div. 5 V/Div. 50 ns/Div.)


Figure AVII. 1 (b) Waveforms Measured With Sockets (2 V/Div. 5 V/Div. $50 \mathrm{~ns} /$ Div.)


Figure AVII. 2 Rise Time Compensation Curves.

## ii Method to Remove Device Output Capacitance Current From Measured Drain Current

When measuring the drain current of a MOSFET using a standard current probe, the drain current waveform is superimposed on the current flowing through the MOSFET's output capacitance. To isolate these currents it is necessary to cancel the output capacitor current flux coupled to the current measuring device. One such technique is shown in Figure AVII.3, here, a dummy MOSFET is connected in parallel with the active MOSFET in a Class E circuit, its gate is shorted to prevent conduction and is driven in parallel with the active MOSFET.

The current path to the dummy MOSFET drain is passed through the high frequency current transformer in the opposite sense to the active MOSFET current path as shown. Hence the flux created by the output capacitance current, and coupled to the current transformer, is cancelled. A suitable high frequency current transformer, which gives 1 V per amp, is shown in Figure AVII.4.


Figure AVII. 3 Method to Cancel $C_{\text {oa }}$ Current in Class E Drain Current Measurements.


Figure AVII. 4 High Frequency Current Transformer.

## iii Method to Determine MOSFET Intrinsic Gate Resistance

An improved method to determine the intrinsic gate resistance of a power MOSFET over the Bowers technique (Bowers 1982) is described here. The technique is shown in Figure AVII.5. The current flowing into and out of the gate of a power MOSFET during switching is determined by differentially measuring the voltage across an external gate resistor. At the same time the voltage level of the turn on and tum off plateau regions is measured, the voltage difference between the turn on plateau region and the turn off plateau region can, at slow switching speeds, be considered to be the result of voltage dropped across the intrinsic gate resistance as a result of the change in polarity of the gate current.


Figure AVII. 5 Circuit Used to Measure MOSFET Intrinsic Gate Resistance.

An oscillogram taken when measuring the intrinsic gate resistance of an IRF450 using this method is shown in Figure AVII.6.


Figure AVII. 6 IRF450 Gate Drive Waveforms Upper Trace: External Gate Voltage ( 5 V/Div. $100 \mathrm{~ns} /$ Div.); and Lower Trace: Inverted Gate Current (0.1 A/Div. $100 \mathrm{~ns} /$ Div.).

The intrinsic gate resistance can be evaluated from the following formula:

$$
\begin{align*}
& V_{p_{c}}=V_{p}+I_{z t} R_{z}  \tag{AVII.1}\\
& V_{p d}=V_{p}-I_{s d} R_{z}
\end{align*}
$$

(AVII.2)

Where: $\quad V_{p c} \quad$ is the externally measured turn on plateau voltage;
$V_{p d}$ is the externally measured turn off plateau voltage;
$V_{p}$ is the plateau voltage at the gate;
$I_{s c} \quad$ is the gate current during the turn on plateau region;
$I_{s d}$ is the gate current during the turn off plateau region;
$R_{g} \quad$ is the intrinsic gate resistance.

Rearranging and assuming $I_{s c}=I_{s d}=I_{s}$ gives:

$$
R_{z}=\frac{V_{p c}-V_{z d}}{2 I_{t}}
$$

## Appendix VIII

## RMS CURRENT THROUGH SHUNT CAPACITOR IN CLASS E AMPLIFIER

The voltage developed across the switch in a Class E amplifier during the off period is given by Raab (Krausse et al. 1980) as:

$$
\begin{align*}
& v_{d t}(\omega x)=\frac{V_{o_{\max }}}{B R}\left[\sin \left(\phi-\frac{\pi}{2}\right)+\cos (\theta+\phi)\right]  \tag{AVIII.1}\\
& \text { Where: } \quad \theta=\omega t \text {; } \\
& \varphi=\tan ^{-1}(-2 / \pi)=-32.48^{\circ} ; \\
& V_{\text {max }} \text { is the maximum voltage across the load; } \\
& \text { B. is the susceptance of the shunt capacitance } \\
& \text { at the operating frequency } \\
& =\omega C_{1}=2 \pi f C_{1} \text {; } \\
& R_{L} \quad \text { is the load resistance }
\end{align*}
$$

The current through a capacitor at any time is given by:

$$
\begin{equation*}
i=C \frac{\mathrm{~d} V}{\mathrm{~d} t} \tag{AVIII.2}
\end{equation*}
$$

Therefore:

$$
\begin{aligned}
i_{c_{1}}(\omega t) & =\frac{\mathrm{d}}{\mathrm{~d} t} \frac{V_{o_{\max }}}{2 \pi f R}\left[\cos \left(\phi-\frac{\pi}{2}\right)+\cos (\omega t+\phi)\right] \\
& =\frac{V_{o_{\max }}}{2 \pi f R} \frac{\mathrm{~d}}{\mathrm{~d} t}[\cos (\omega t) \cos (\phi) \\
& -\sin (\omega t) \sin (\phi)]
\end{aligned}
$$

Differentiating gives:

$$
\begin{aligned}
i_{c_{1}}(\omega t) & =\frac{V_{o_{\max }}}{2 \pi f R}[\cos (\phi)(-\omega \sin (\omega t) \\
& -\omega \cos (\omega t) \sin (\phi)] \\
& =-\frac{V_{o_{\max }}}{R}(\cos (\phi) \sin (\omega t)+\sin (\phi) \cos (\omega t)) \\
& =-\frac{V_{o_{\max }}}{R} \sin (\phi+\omega t)
\end{aligned}
$$

The r.m.s. current through the shunt capacitor is given by:

$$
\begin{equation*}
I_{c_{1} \operatorname{mu}}=\left[\left(\frac{V_{o_{\max }}}{R_{L}}\right)^{2} \frac{1}{2 \pi} \int_{0}^{\pi} i_{c_{1}}^{2}(\omega \mathrm{t}) \mathrm{d}(\omega t)\right]^{\frac{1}{2}} \tag{AVIII.5}
\end{equation*}
$$

Now

$$
\begin{aligned}
i_{c_{1}}^{2}(\omega t) & =\left(\frac{V_{o_{\max }}}{R_{L}}\right)^{2} \sin ^{2}(\phi+\omega t) \\
& =\left(\frac{V_{o_{\max }}}{R_{L}}\right)^{2} \frac{1-\cos (2(\phi+\omega t))}{2} \\
& =\left(\frac{V_{o_{\max }}}{R_{L}}\right)^{2} \frac{1-\cos (2 \phi) \cos (2 \omega t)-\sin (2 \phi) \sin (2 \omega t)}{2}
\end{aligned}
$$

(AVIII.6)

And

$$
\begin{align*}
\frac{1}{2 \pi} \int_{0}^{\pi} i_{c_{1}}^{2}(\omega t) \mathrm{d}(\omega t)= & \left(\frac{V_{o_{\max }}}{R_{L}}\right)^{2}\left(\frac{1}{4 \pi} \int_{0}^{\pi} \mathrm{d}(\omega t)\right. \\
& -\frac{\cos (2 \phi)}{4 \pi} \int_{0}^{\pi} \cos (2 \omega t) \mathrm{d}(\omega t) \\
& \left.+\frac{\sin (2 \phi)}{4 \pi} \int_{0}^{\pi} \sin (2 \omega t) \mathrm{d}(\omega t)\right) \\
= & \frac{1}{4 \pi}\left(\frac{V_{o_{\max }}}{R_{L}}\right)^{2}[\pi-\sin (2 \phi)] \tag{AVIII.7}
\end{align*}
$$

Thus

$$
\begin{equation*}
I_{C_{1} \operatorname{mu}}=\frac{V_{o_{\max }}}{R_{L}}\left[\frac{1}{4 \pi}(\pi-\sin (2 \phi))\right]^{\frac{1}{2}} \tag{AVIII.8}
\end{equation*}
$$

Substituting for $\varphi=\tan ^{-1}(-2 / \pi)=-32.48^{\circ}$ gives:

$$
\begin{equation*}
I_{c_{1} \operatorname{mat}}=\frac{V_{o_{\max }}}{R_{L}} \times 0.5675 \tag{AVIII.9}
\end{equation*}
$$

Which is the r.m.s. current through the shunt capacitor $C_{1}$.

The shunt capacitor consists of the external capacitor plus the output capacitance of the switch which in turn consists, for a power MOSFET, of the drain source capacitance plus the reverse transfer capacitance. The r.m.s. current through the reverse transfer capacitance is simply given by:

$$
\begin{equation*}
I_{c_{4} m u}=\frac{C_{\text {de }}}{C_{1}} \times \frac{V_{o_{\text {max }}}}{R_{L}} \times 0.5675 \tag{AVIII.10}
\end{equation*}
$$

## Appendix IX

## R.M.S. CURRENT THROUGH THE SWITCH IN A CLASS E AMPLIFIER

In order to obtain the maximum possible output power from a device used in a Class E amplifier, it is necessary to know its peak vcltage and current rating. With a power MOSFET the principle limitation on current (before pinch off effects are seen) is thermal heating due to the r.m.s. current through the device. Thus manufacturer's quoted pulsed current rating and continuous current rating are of little use when selecting a device for a particular application.

Therefore it is necessary to determine the r.m.s. current through the switch under optimum Class E operation. This can then be directly related to the continuous rated current of the MOSFET quoted by the manufacturers.


Figure 3.10 Basic Class E Amplifier Circuit and Ideal Waveforms.
The Class E equivalent circuit and ideal waveforms used to analyse the Class E amplifier are shown in Figure 3.10 (repeated here for convenience), the basis for analysis is to assume a sinusoidal output current through the load and 'work backwards'. It is not intended to repeat the theoretical analysis of others, merely to extend the analysis to determine a practical relationship between power MOSFET ratings and Class E operation. The reader is referred to the following references for more detailed information on Class E operation (Sokal et al. 1975, Raab 1977, Raab et al. 1978, Kazimierczuk 1983).

The drain current waveform shape is determined by the load network and is approximately a section of a sinewave (between $-32.5^{\circ}(\varphi)$ and $+147.5^{\circ}(\pi-\varphi)$ ) centred at $I=I_{\alpha}$, where $I_{\alpha}$ is the d.c. current through the switching device and is equal to the d.c. supply current to the circuit $I_{d d x}$. The angle $-32.5^{\circ}$ is the phase shift between load current and drain voltage due to the lagging nature of the load resonant circuit. That is to say the output circuit can be considered to be a resonant circuit, tuned to the switching frequency, plus a series inductance.

From Kazimierczuk (Kazimierczuk 1983) the current through the switch is given by:

$$
\begin{array}{ll}
\frac{i_{d}(\omega t)}{I_{d u}}=\frac{\pi-\theta_{f}}{2} \sin \omega t-\cos \omega t+1 & \text { for } 0<\omega t \leq \pi \\
\frac{i_{d}(\omega t)}{I_{d d}}=2\left(1-\frac{\omega t-\pi}{\theta_{f}}\right) & \text { for } \pi<\omega t \leq \pi+\theta_{f} \\
\frac{i_{d}(\omega t)}{I_{d d}}=0 & \text { for } \pi+\theta_{f}>\omega t \leq 2 \pi \tag{AIX.1c}
\end{array}
$$

Where: $\quad I_{d e}$ is the supply current
$\theta_{f}=\omega t_{f}$
$t_{f}$ is the fall time of drain current
Since there is little difference in operation between $\theta_{f}$ being equal to zero and $\theta_{f}$ being equal to $20^{\circ}$ (in fact for transistor fall times giving $\theta_{f}=40^{\circ}$ efficiency is reported to drop by only $2.5 \%$ (Kazimierczuk 1983)) the calculation is simplified by equating $\theta$ to zero.

Thus the drain current is now described by:

$$
\begin{array}{ll}
i_{d}(\omega t)=I_{d \alpha}\left(\frac{\pi}{2} \sin \omega t-\cos \omega t+1\right) & \text { for } 0<\omega t \leq \pi \\
i_{d}(\omega t)=0 & \text { for } \pi>\omega t \leq 2 \pi \tag{AIX.2b}
\end{array}
$$

During the conduction period the drain voltage is given by:

$$
\begin{equation*}
v_{d}(\omega t)=i_{d}(\omega t) R_{d s(\omega t)} \tag{AIX.3}
\end{equation*}
$$

The r.m.s. current through the switch is given by:

$$
\begin{equation*}
I_{d_{r m s}}=\left[\frac{1}{2 \pi} \int_{0}^{\pi} i_{d}^{2} \mathrm{~d}(\omega t)\right]^{\frac{1}{2}} \tag{AIX.4}
\end{equation*}
$$

Substituting in from Equation AIX.2a gives

$$
\begin{equation*}
I_{d_{r, n s} .}=\left[\frac{I_{d d}^{2}}{2 \pi} \int_{0}^{\pi}\left(\frac{\pi}{2} \sin (\omega t)-\cos (\omega t)+1\right)^{2} \mathrm{~d}(\omega t)\right]^{\frac{1}{2}} \tag{AIX.5}
\end{equation*}
$$

Let

$$
\begin{equation*}
A=\left(\frac{\pi}{2} \sin (\omega t)-\cos (\omega t)+1\right)^{2} \tag{ALX.6}
\end{equation*}
$$

Squaring and collecting terms gives:

$$
\begin{aligned}
A= & \frac{\pi^{2}}{4} \sin ^{2}(\omega t)-\pi \cos (\omega t) \sin (\omega t)+\pi \sin (\omega t) \\
& +\cos ^{2}(\omega t)-2 \cos (\omega t)+1
\end{aligned}
$$

(AIX.7)

Let

$$
A=a+b+c+d+e+f
$$

(AIX.8)

Then

$$
\begin{equation*}
\int_{0}^{\pi} A \mathrm{~d}(\omega t)=\int_{0}^{\pi} a \mathrm{~d}(\omega t)+\ldots \ldots \ldots . \int_{0}^{\pi} f \mathrm{~d}(\omega t) \tag{AIX.9}
\end{equation*}
$$

Integrating each term separately:

$$
\begin{align*}
& \int_{0}^{\pi} a \mathrm{~d}(\omega t)=\frac{\pi^{2}}{8} \int_{0}^{\pi}(1-\cos (2 \omega t)) \mathrm{d}(\omega t)  \tag{AIX.10}\\
&=\frac{\pi^{3}}{8} \\
& \begin{aligned}
\int_{0}^{\pi} b \mathrm{~d}(\omega t) & =-\frac{\pi}{2} \int_{0}^{\pi} \sin (2 \omega t) \mathrm{d}(\omega t) \\
& =0 \\
\int_{0}^{\pi} c \mathrm{~d}(\omega t) & =\pi \int_{0}^{\pi} \sin (\omega t) \mathrm{d}(\omega t) \\
& =2 \pi
\end{aligned} \tag{AIX.11}
\end{align*}
$$

$$
\begin{align*}
& \int_{0}^{\pi} d \mathrm{~d}(\omega t)=\frac{1}{2} \int_{0}^{\pi}(1+\cos (2 \omega t)) \mathrm{d}(\omega t)  \tag{AIX.13}\\
&=\frac{\pi}{2} \\
& \begin{aligned}
\int_{0}^{\pi} e \mathrm{~d}(\omega t) & =-2 \int_{0}^{\pi} \cos (\omega t) \mathrm{d}(\omega t) \\
& =0
\end{aligned}  \tag{ALX.14}\\
& \begin{aligned}
\int_{0}^{\pi} f \mathrm{~d}(\omega t) & =\int_{0}^{\pi} \mathrm{d}(\omega t) \\
& =\pi
\end{aligned}
\end{align*}
$$

Thus

$$
\begin{equation*}
\int_{0}^{\pi} i_{d}^{2}(\omega t) \mathrm{d}(\omega t)=I_{d d}^{2} \frac{\pi}{2}\left(\frac{\pi^{2}}{4}+7\right) \tag{AIX.16}
\end{equation*}
$$

And the r.m.s. current is:

$$
\begin{align*}
I_{d_{\text {ras }}} & =\left[\frac{1}{2 \pi} I_{d \alpha}^{2} \frac{\pi}{2}\left(\frac{\pi^{2}}{4}+7\right)\right]^{\frac{1}{2}}  \tag{AIX.17}\\
& =I_{d \alpha}\left(\frac{\pi^{2}}{16}+\frac{7}{4}\right)^{\frac{1}{2}} \\
& =1.54 I_{d 4}
\end{align*}
$$

Therefore the power dissipated in the switch is:

$$
\begin{equation*}
P_{d}=I_{d( }^{2}\left(\frac{\pi^{2}}{16}+\frac{7}{4}\right) R_{d(0 n)} \tag{AIX.18}
\end{equation*}
$$

The equation for current given by Kazimierczuk assumes a loaded $Q$ for the circuit of 10 . To calculate the r.m.s. current through the switch for any value of $Q$ it is necessary to use Sokal's equations as a starting point (Sokal et al. 1975).

With reference to Figure 3.10, drain current builds up from zero at the beginning of the on cycle to a peak of:

$$
\begin{equation*}
I_{d_{p k}}=I_{\alpha d}\left[1+\left(\pi_{4}^{2}+1\right)^{\frac{1}{2}}\left(1-\frac{0.5}{Q_{L}}\right)\right] \tag{ALX.19}
\end{equation*}
$$

It then decays gradually to $2 I_{d d}\left(1+0.82 / Q_{L}\right)$ at which time the transistor is turned off by the drive signal. As a first approximation the r.m.s. drain current is given by:

$$
\begin{align*}
I_{d_{m u}} & =\left[\frac{1}{2 \pi} \int_{\phi}^{\pi+\phi} I_{d_{p k}}^{2} \sin ^{2}(\omega t) \mathrm{d}(\omega t)+\frac{1}{2 \pi} \int_{\phi}^{\pi+\phi} I_{d d}^{2} \mathrm{~d}(\omega t)\right]^{\frac{1}{2}}  \tag{AIX.20}\\
& =\left[\frac{1}{2 \pi} \int_{\phi}^{\pi+\phi} A \mathrm{~d}(\omega t)+\frac{1}{2 \pi} \int_{\phi}^{\pi+\phi} B \mathrm{~d}(\omega t)\right]^{\frac{1}{2}}
\end{align*}
$$

$$
\text { Where: } \begin{aligned}
& A \equiv I_{\text {dk }}^{2} \sin ^{2}(\omega t) ; \text { and } \\
& B \equiv I_{\alpha ;}^{2} \\
& \varphi=\tan ^{-1}(-2 / \pi)=-32.48^{\circ} .
\end{aligned}
$$

Integrating separately:

$$
\begin{align*}
\frac{1}{2 \pi} \int_{\phi}^{\pi+\phi} A \mathrm{~d}(\omega t) & =\frac{I_{d p k}^{2}}{2 \pi} \int_{\phi}^{x+\phi} \sin ^{2}(\omega t) \mathrm{d}(\omega t) \\
& =\frac{I_{d p k}^{2}}{4 \pi} \int_{\phi}^{\pi+\phi}(1-\cos (2 \omega t) \mathrm{d}(\omega t) \\
& =\frac{I_{d p k}^{2}}{4 \pi}\left[\omega t-\frac{\sin (2 \omega t)}{2}\right]_{\phi}^{\pi+\phi} \\
& =\frac{I_{d p k}^{2}}{4 \pi}\left[\pi+\frac{1}{2}(\sin (2 \phi)-\sin (2 \pi+2 \phi))\right]  \tag{AIX.21}\\
\frac{1}{2 \pi} \int_{\phi}^{x+\phi} B \mathrm{~d}(\omega t) & =\frac{I_{d \alpha}^{2}}{2 \pi} \int_{\phi}^{x+\phi} \mathrm{d}(\omega t) \\
& =\frac{I_{d \alpha}^{2}}{2} \tag{AIX.22}
\end{align*}
$$

Combining to give the r.m.s. current:

$$
\begin{equation*}
I_{d_{r m J} .}=\left[\frac{I_{d_{\phi k}}^{2}}{4 \pi}\left[\pi+\frac{1}{2}(\sin (2 \phi)-\sin (2 \pi+2 \phi))\right]+\frac{I_{d \alpha}^{2}}{2}\right]^{\frac{1}{2}} \tag{ALX.23}
\end{equation*}
$$

Substituting in for $\pi$ and $\varphi$ gives:

$$
\begin{align*}
I_{d_{m t}} & =\left[\frac{I_{d p t}^{2}}{4 \pi}\left[\pi+\frac{1}{2}(-0.906+0.906)\right]+\frac{I_{d t}^{2}}{2}\right]^{\frac{1}{2}} \\
& =\left[\frac{I_{d p}^{2}}{4}+\frac{I_{d t}}{2}\right]^{\frac{1}{2}} \tag{AIX.24}
\end{align*}
$$

Substituting for $I_{\text {d } k}$ from Equation AIX. 19 gives:

$$
\begin{equation*}
I_{d r, m s .}=I_{d \alpha}\left[\frac{\left(1+1.862\left(1-\frac{.0 .5}{Q_{L}}\right)\right)}{4}+\frac{1}{2}\right]^{\frac{1}{2}} \quad \text { for } Q_{L}=10 \tag{AIX.25}
\end{equation*}
$$

For a loaded $Q$ of 10 :

$$
\begin{equation*}
I_{d_{r, m .}}=1.55 I_{d A} \quad \text { for } Q_{L}=10 \tag{AIX.26}
\end{equation*}
$$

and for a loaded $Q$ of 5 , the value of $Q$ used to design the Class E amplifiers reported in the preceding chapters:

$$
\begin{equation*}
I_{d_{r m s .}}=1.51 I_{d d} \quad \text { for } \quad Q_{L}=5 \tag{AIX.27}
\end{equation*}
$$

## Appendix $\mathbf{X}$ <br> MINIMUMWIRE LENGTH TOROIDAL INDUCTOR DESIGNEOUATIONS

The principal advantage of a toroidal inductor design over a conventional solenoid is the reduction in stray flux external to the inductor. In a solenoid, magnetic flux radiates from the ends of the solenoid and can cause interference by electromagnetic coupling to other parts of the circuit. A toroid can be considered as a solenoid with both ends coupled together. Hence the external magnetic field generated by a toroidal inductor is theoretically zero.

In order to obtain a high $Q$ it is necessary to use the least length of wire to form the inductor. A set of optimum design equations has been proposed by Murgatroyd for circular, Shafranov D and square sectioned toroids (Murgatroyd et al. 1985). The design equations for the square sectioned toroids used in the practical work are given here for the benefit of the reader.


Figure AX. 1 Square Sectioned Toroid Dimensions.
The inductance of a square-section toroid, as dimensioned in Figure AX.1, is given by:

$$
\begin{equation*}
L_{2}=\frac{\mu_{0}}{2 \pi} N^{2} A \ln \left(1+\frac{A}{S}\right) \tag{AX.1}
\end{equation*}
$$

Where: $\quad A$ is the side of the square; $S$ is the minor radius of the toroid; $N$ is the number of turns.

The side of the square is:

$$
\begin{equation*}
A=\frac{w}{4 N} \tag{AX.2}
\end{equation*}
$$

Where: $\quad w$ is the wire total length.

If the wire diameter is $d$ (determined by the maximum allowable current density) the wire contact condition is:

$$
\begin{equation*}
\frac{d}{2 S}=\sin \left(\frac{\pi}{N}\right) \tag{AX.3}
\end{equation*}
$$

The inductance, including the 'intemal' inductance of the wire, is therefore:

$$
\begin{equation*}
L_{s}=\frac{\mu_{0} N w}{8 \pi} \ln \left\{1+\frac{w}{2 N d} \sin \left(\frac{\pi}{N}\right)\right\}+\frac{\mu_{0} w}{8 \pi} \tag{AX4}
\end{equation*}
$$

It is convenient to express the inductance in terms of a scale inductance:

$$
\begin{equation*}
L_{0}=\frac{\mu_{0} d}{2 \pi} \tag{AX.5}
\end{equation*}
$$

and to express the wire length as a ratio to the wire diameter, so:

$$
\begin{equation*}
k=\frac{w}{d} \tag{AX.6}
\end{equation*}
$$

Thus Equation AX. 4 may be rewritten as:

$$
\begin{equation*}
\frac{L_{s}}{L_{0}}=\frac{N k}{4} \ln \left\{1+\frac{k}{2 N} \sin \left(\frac{\pi}{N}\right)\right\}+\frac{k}{4} \tag{AX.7}
\end{equation*}
$$

If $N$ is large, this may be approximated:

$$
\begin{equation*}
\frac{L_{s}}{L_{0}}=\frac{N k}{4} \ln \left(1+\frac{\pi k}{2 N^{2}}\right)+\frac{k}{4} \tag{AX.8}
\end{equation*}
$$

To make the derivative zero, the equation

$$
\begin{equation*}
\ln (2 x)-4 x+2=0 \tag{AX.9}
\end{equation*}
$$

where

$$
\begin{equation*}
\frac{1}{2 x}=1+\frac{\pi k}{2 N^{2}} \tag{AX.10}
\end{equation*}
$$

has to be solved. The solution, $x=0.1016$, is obtained numerically and gives the optimum value of $N$ at $0.6329 k^{1 / 2}$. When put back into Equation AX. 8 the best available dimension-less inductance ( $L / L_{0}$ ) is given as $0.2522 k^{3 / 2}+0.25 \mathrm{k}$.

A practical example given below shows the design procedure:

A square sectioned toroid is required having inductance $30 \mu \mathrm{H}$, carrying a d.c. current of 8 A . If the maximum required current density is $3 \mathrm{~A} / \mathrm{mm}^{2}$ then the required wire diameter, $d$, is 1.85 mm . The scale inductance, $L_{0}$, is calculated from Equation AX.5:

$$
L_{0}=\frac{\mu_{0} d}{2 \pi}=3.7 \times 10^{-10}
$$

The dimension-less inductance is calculated:

$$
\frac{L_{1}}{L_{0}}=81.08 \times 10^{3}
$$

The dimension-less wire length, $k$, is found by solving:

$$
\frac{L_{t}}{L_{0}}=81.08 \times 10^{3}=0.2522 k^{\frac{3}{2}}+0.25 k
$$

This is solved either graphically or iteratively to give $k=4648$.

The number of turns required is $N=0.6329 k^{1 / 2}=43.15$, the length of wire required (which must be adhered to if an accurate inductance is to be obtained) is given by:

$$
w=d \times k=8.6 \mathrm{~m}
$$

The side of the square of the former is:

$$
A=\frac{w}{4 N}=49.8 \mathrm{~mm}
$$

The minor radius of the toroid is:

$$
S=\frac{d}{2 \sin \left(\frac{\pi}{N}\right)}=12.7 \mathrm{~mm}
$$

The calculation can be checked by substituting the terms into Equation AX. 1 giving $L_{s}=29.55 \mu \mathrm{H}$, adding the self inductance of the wire gives a total inductance of $29.98 \mu \mathrm{H}$.


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[^0]:    1 Upper-case letters (e.g. $V, I$ ) are used for steady, mean and r.m.s. values, lower case letters for instantaneous values which may vary with time (e.g. $v, i$ ). Maximum, minimum and average are indicated by subscripts (e.g. $\nu_{\max } \nu_{\min }, V_{\text {ava }}$ ).

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