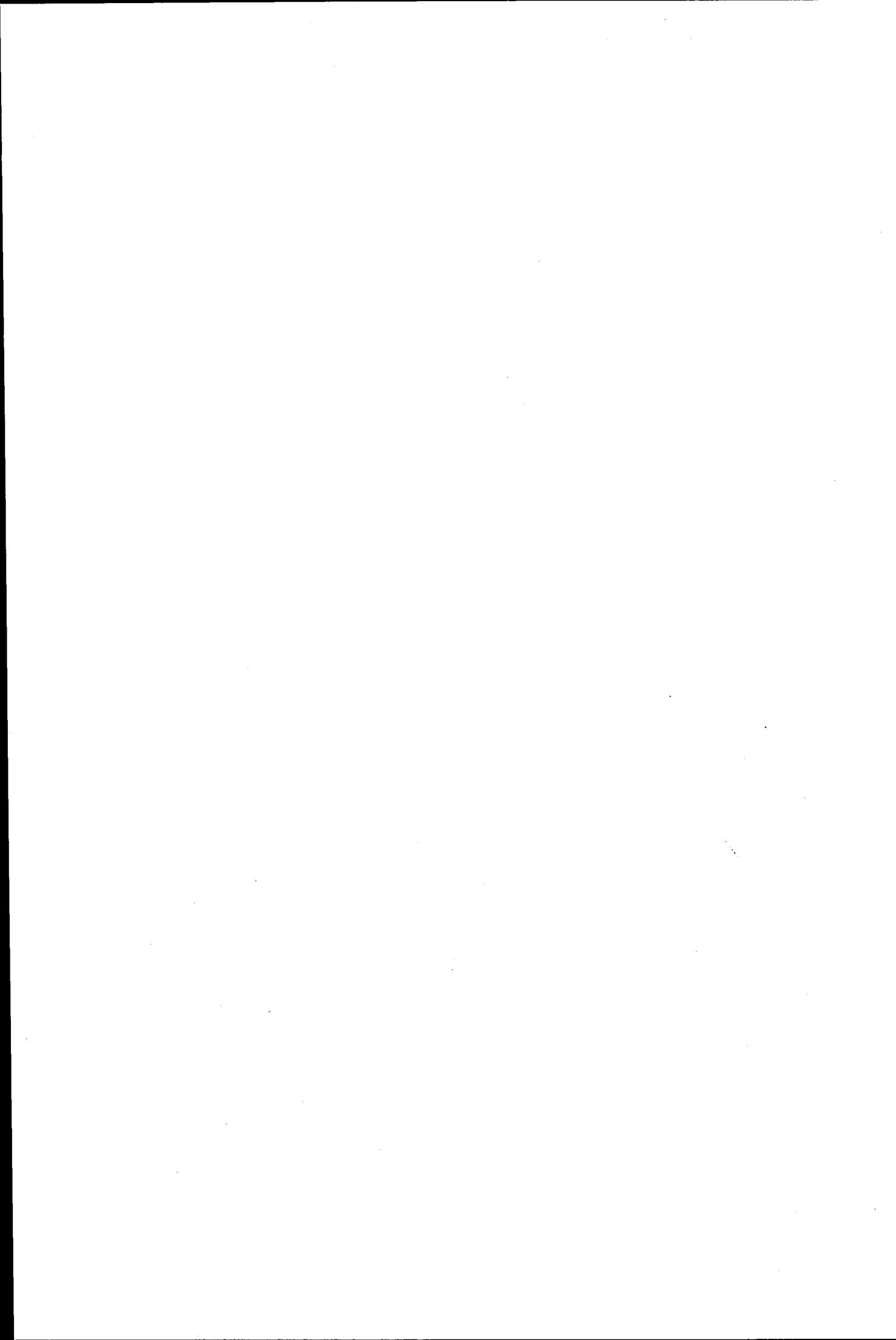


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RESONANCE MODE POWER SUPPLIES WITH POWER FACTOR CORRECTION

by

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A DOCTORAL THESIS

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*To my parents,
The debt is beyond measure
The gratitude beyond compare*

" de nier ce qui est, et d'expliquer ce qui n'est pas "

J.J. Rousseau, La Nouvelle Heloise (1761)

SUMMARY

There is an increasing need for AC-DC converters to draw a pure sinusoidal current at near unity power factor from the AC mains. Most conventional power factor correcting systems employ PWM techniques to overcome the poor power factor being presented to the mains. However, the need for smaller and lighter power processing equipment has motivated the use of higher internal conversion frequencies in the past. In this context, resonant converters are becoming a viable alternative to the conventional PWM controlled power supplies.

The thesis presents the implementation of active power factor correction in power supplies, using resonance mode techniques. It reviews the PWM power factor correction circuit topologies previously used. The possibility of converting these PWM topologies to resonant mode versions is discussed with a critical assessment as to the suitability of the semiconductor switching devices available today for deployment in these resonant mode supplies.

The thesis also provides an overview of the methods used to model active semiconductor devices. The computer modelling is done using the PSpice microcomputer simulation program. The modifications that are needed to the built in MOSFET model in PSpice, when modeling high frequency circuits is discussed. A new two transistor model which replicates the action of a GTO thyristor is also presented. The new model enables the designer to estimate the device parameters with ease by adopting a short calculation and graphical design procedure, based on the manufacturer's data sheets.

The need for a converter with a high efficiency, larger power/weight ratio, high input power factor with reduced line current distortion and reduced cost has led to the development of a new resonant mode converter topology, for power processing. The converter presents a near resistive load to the mains thus ensuring a high input power factor, while providing a stabilised dc voltage at the output with a small 100Hz ripple. The supply is therefore ideal for preregulation applications. A description of the modes of operation and the analysis of the power circuit are included in the thesis. The possibility of using the converter for low output voltage applications is also discussed.

The design of a 300W, 80kHz prototype model of this circuit is presented in the thesis. The design of the isolation transformer and other magnetic components are described in detail. The selection of circuit components and the design and implementation of the variable frequency control loop are also discussed. An evaluation of the experimental and computer simulated results obtained from the prototype model are included in the presentation.

The thesis further presents a zero-current switching quasi-resonant flyback circuit topology with power factor correction. The reasons for using this topology for off-line power conversion applications are discussed. The use of a cascoded combination of a bipolar power transistor and two power MOSFETs in the configuration has enabled the circuit to process moderate levels of power while simultaneously switching at high frequencies. This fulfils the fundamental precondition for miniaturisation. It also provides a well regulated DC output voltage with a very small ripple while maintaining a high input power factor. The circuit is therefore ideal for use in mobile applications.

A preliminary design of the above circuit, its analysis using PSpice, the design of the control circuit, current limiting and overcurrent protection circuitry and the implementation of closed-loop control are all included in the thesis. The experimental results obtained from a bread board model is also presented with an evaluation of the circuit performance. The power factor correction circuit is finally installed in this supply and the overall converter performance is assessed.

ACKNOWLEDGEMENTS

Throughout the long, arduous process of learning, I have been lucky enough to have the guidance and encouragement of so many wonderful people whose generosity and patience has known no bounds. To thank them all is beyond the capacity of reason - however, certain assistance cannot go without due recognition - therefore I will be brief :

To Dr. C.D. Manning, who - having presented me with the opportunity to pursue my academic career - has continued to offer invaluable advice and criticism, without which my task would have been insurmountable.

To my friends and associates - you will never realise the true significance of your contributions - I salute you one and all.

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CHAPTER 1

INTRODUCTION

An introduction into the need for power factor correction in power supplies is presented. The reasons for undertaking this work are given.

The optimum ac-dc converter would be one that draws a pure sinusoidal current at unity power factor from its input and produces a well regulated output voltage with hardly any ripple. In the past, much attention has been directed towards meeting the requirements of the output side with little attention being paid to the input of the power supply. The result of this has been the operation of the power supply with a very low input power factor and a considerably distorted input current waveform.

Most switch mode power supplies use large electrolytic buffer capacitors after the bridge rectifier to smooth the 100Hz ripple on the input voltage to acceptable levels, as shown in Fig.1.1. This results in very high pulses of current being drawn from the mains (see Fig.1.2). The pulses occur when the ac voltage exceeds the capacitor voltage. This is the cause of the low power factored front end and the distorted current waveforms at the input.

The average power in a conventional ac circuit can be calculated from

$$P = E * I * \text{Cos}\theta \quad (1.1)$$

where E and I are the r.m.s values of the voltage and current respectively and θ , the phase angle between the two. $\text{Cos}\theta$ is the power factor of the circuit.

However, this expression does not hold for non-sinusoidal waveforms such as those seen in the switch mode power supplies described above. For such cases, the power factor is defined as

$$\text{Power Factor} = \text{average power} / \text{apparent power} = P / E * I \quad (1.2)$$

where E and I are again the r.m.s values of the voltage and current.

In such cases, the peak currents drawn from the mains can be very high, especially at high power levels, and the above ratio can approach 2:1 resulting in a power factor of 0.5. In the past, large input chokes have often been used to overcome this disadvantage. However, the benefits of such schemes are overshadowed by the cost and space requirements involved. A viable alternative therefore would be the deployment of active power factor correction in these power supplies.

Fig.1.3 shows the maximum power available from a 240Vac, 13amp mains outlet as a function of its power factor. Typically, 1.56kW can be drawn when the power factor is 0.5. At unity power factor however, 3.12kW can be obtained - an increase of 50%.

Therefore, one benefit of power factor correction is a reduction in the amount of r.m.s current being drawn from the mains. This eliminates the need for an expensive high current line power service. A second benefit is the reduction in peak currents the front end bridge diodes must carry.

The reduction in the line current harmonic content is another benefit of power factor correction [1]. Consider the 3 phase 4 wire electrical distribution system shown in Fig.1.4. The total r.m.s current flowing in each of the lines L1, L2 and L3 is given by

$$I_{\text{rms}} = \sqrt{I_1^2 + I_2^2 + I_3^2 + \dots} \quad (1.3)$$

where I_1 , I_2 and I_3 are the fundamental, second and third order harmonics respectively.

The waveforms of both the current and voltage for a non-power factor corrected system are shown in Fig.1.5. The current in the neutral or return signal appears as a 150Hz signal. For such a system, the third order harmonic, which is 150Hz, has the same amplitude as the 50Hz fundamental frequency. Since the amplitudes of the same frequency are additive, the amplitudes of the third order harmonic of each line can be added together. It is thus possible, that the neutral wire will carry more current than any of the power lines. Unless the neutral wire is sized for this, it can be overloaded without operating the overcurrent protection on each phase.

Another area that is receiving much attention at present, is the undesirable noise and interference being introduced to the power sources from non-power factor corrected switch mode power supplies [2]. This can adversely affect the operation of adjacent equipment such as computers, communication systems, and process controls. Thus, the overcoming of such waveform distortion by employing power factor correction is of prime importance - especially in this computerised age.

Most conventional power factor correcting systems introduced so far, employ PWM techniques to overcome the poor power factors being presented to the mains. However, the ever increasing demand for smaller and lighter power processing equipment has motivated the use of higher internal conversion frequencies in the recent past. In this context, resonant converters have emerged as being superior to the conventional PWM converters. The latter suffers from switching losses and noise due to the simultaneous switching of high voltages and currents. They are more sensitive to parasitic inductances and capacitances which increase component stress or even inhibit the intended mode of operation altogether.

Resonance converters are gaining more acceptance in high frequency power applications at present. Their switching losses are low since voltage or current is zero or low during switching transients. They are less sensitive to parasitic inductance or capacitance which can make up part of the LC resonant tank circuit. In addition, sinusoidal operation results in lower radiated and line conducted EMI.

Therefore, a power factor correcting system that employs resonance mode techniques at high switching frequencies is more efficient and has a higher power to weight ratio compared to the existing PWM controlled systems.

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1. Spangler J.J., 1985, "A power factor corrected, MOSFET, multiple output, flyback switching supply", Proceedings of Power Conversion International Conf., 19-32.
2. Griffith D.C. and Resch R.J., 1986, "Working with waveform distortion micro computers to main frames", Proceedings of I.E.E.E. Applied Power Electronics Conf., 41-45.

1.2 FIGURES

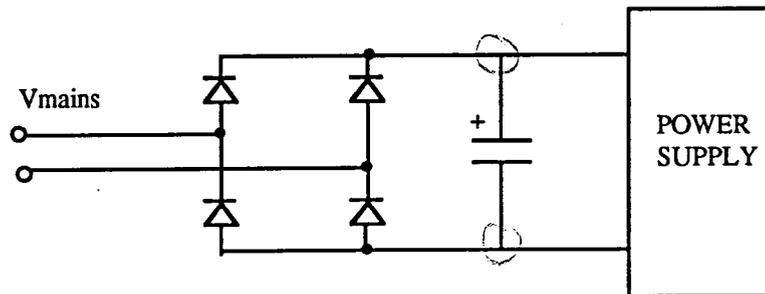


Fig.1.1 The input stage of a switch mode power supply

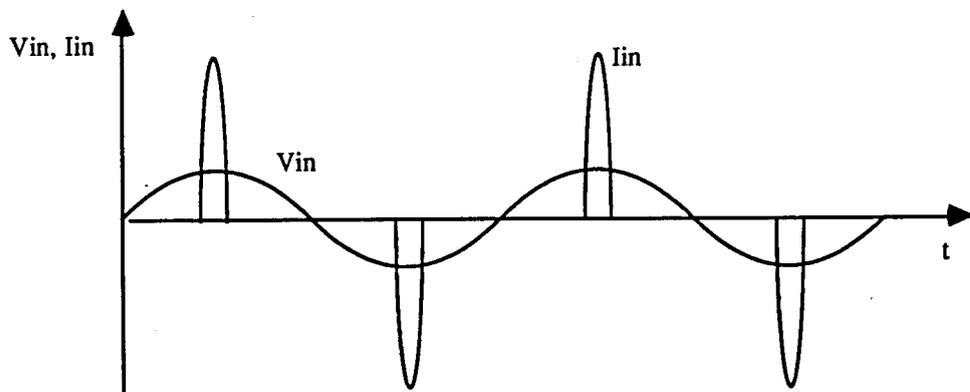


Fig.1.2 Input voltage and current

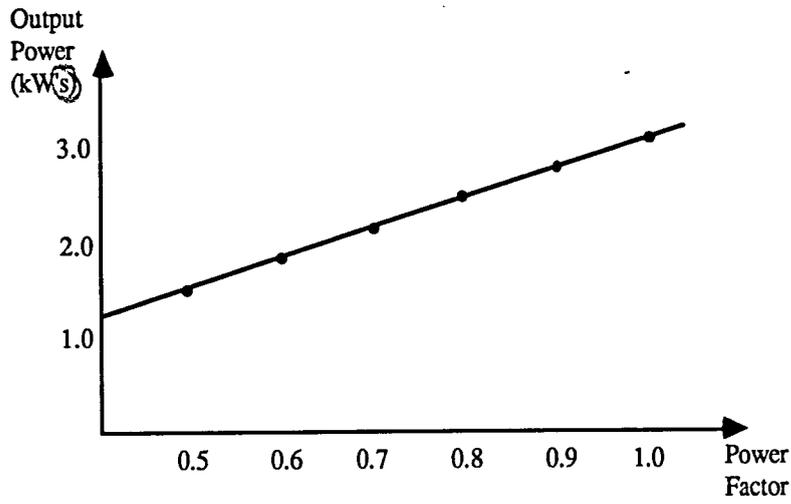


Fig.1.3 Maximum output power available from a 240Vac, 13amp mains outlet.

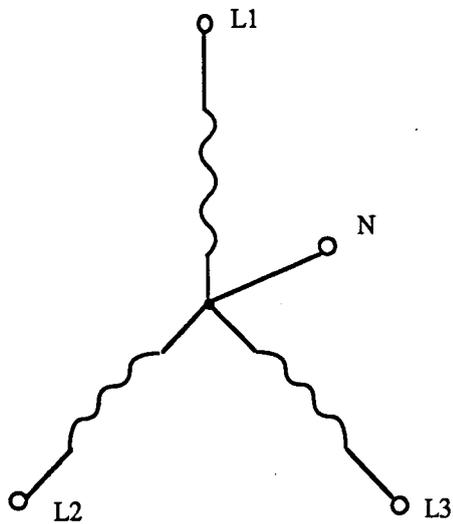


Fig.1.4 3 phase 4 wire electrical distribution system.

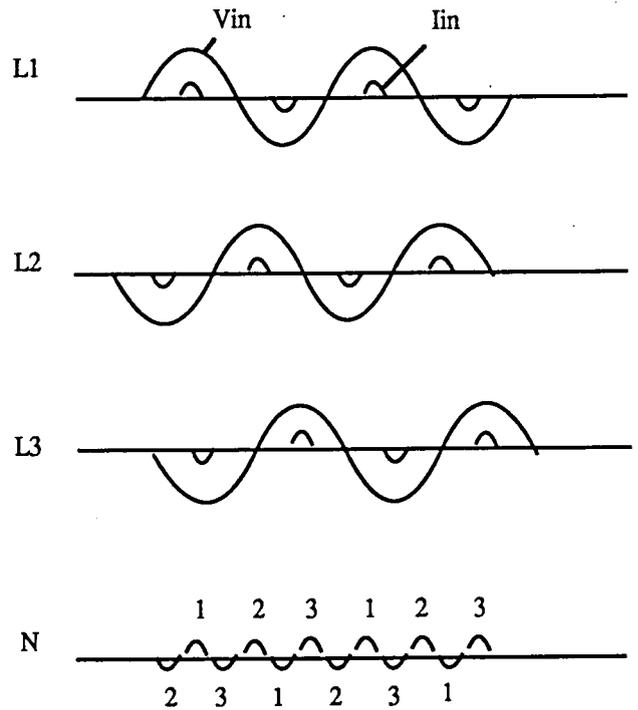


Fig.1.5 Third harmonic in the neutral line

CHAPTER 2

REVIEW

Power factor correction circuits used in commercial equipment in the past, will be reviewed in this chapter. The possibility of converting these PWM topologies to resonant mode versions is discussed in the review. Semiconductor switching devices which are suitable for employment in these resonant mode versions are also reviewed.

2.1 REVIEW OF POWER FACTOR CORRECTION CIRCUIT TOPOLOGIES

Techniques such as the continuous shaping of the input current waveform or the continuous chopping of the line current at a high frequency (dynamic power factor correction) are often used in industry for obtaining good input power factors [1]-[5]. The converter is placed between the bridge rectifier and the storage capacitor. The configuration thus presents a constant impedance to the mains resulting in a sinusoidal current being drawn at a power factor approaching unity. These converter circuits are ideal for use as pre-conditioners where the dc output voltage produced contains a small ripple at twice the mains frequency.

The modulation of the mains input voltage between the peak ac line voltage and half its value for obtaining power factors between 0.9 and 0.95, is another technique often used in the fluorescent lamp ballast industry [6][7]. A small circuit configuration built at the front end of the supply provides this modulation. The control circuit within the supply could then be used to provide a better regulated output voltage with a much smaller ripple.

2.1.1 Continuous shaping of the input current waveform technique

The continuous shaping of the input current waveform is obtained by modifying the ac-dc converter so that the input power could be pulse-width modulated.

The basic converter topology is shown in Fig.2.1. A flyback type converter circuit is employed, with a high frequency filter placed on the dc side of the bridge rectifier. The input current is controlled by varying the duty ratio δ of the switch according to a reference signal obtained directly from the line voltage. δ would therefore vary continuously at 100Hz, resulting in a sinusoidal input current being drawn at a power factor approaching unity. Variations in the dc output power levels are achieved by varying the amplitude of the ac current reference and thereby adjusting the magnitude of the input current drawn.

The stable operation of such a system, depends on the incremental dynamics of the power circuit [1]. The system dynamics are however limited by the choice of the switching frequency. If the magnitudes of the system singularities become comparable to the switching frequency, the systems dynamic response will be highly unpredictable. The difference between the line frequency and the switching frequency should therefore be made as large as possible, to give the designer adequate freedom in the choice of system dynamics.

The use of PWM techniques to achieve a high switching frequency however, gives rise to considerable switching losses in the switching devices and the associated snubber networks. Although resonance mode techniques can be used to overcome this disadvantage, the very nature of the circuit operation does not permit an easy substitution of such a technique. Also, the use of two feedback loops in the control scheme for input power factor correction and output power control, makes this technique a more complex method of power factor control.

2.1.2 Dynamic power factor correction technique

A dynamic power factor corrected PWM boost type converter circuit is shown in Fig.2.2 [5]. If the input line current to the system was chopped at a high frequency and the duration of the boost pulses kept constant to provide the required output power, the input current would automatically keep in phase with the voltage and the power factor would thus approach unity. This is the principle of dynamic power factor correction.

In Fig.2.2, the switch continuously operates at a constant frequency f_s , successively storing and releasing the energy stored in the choke L1. The energy transferred during each pulse is therefore given by,

$$\text{Energy transferred during one pulse} = \frac{1}{2} * L1 * i_{pk}^2 \quad (2.1)$$

where i_{pk} is the peak value of current at the instant of turn off. This peak current is a function of the instantaneous value of the full wave rectified line voltage V_{in} and is given by,

$$i_{pk} = \frac{V_{in} * t_{on}}{L1} \quad (2.2)$$

where t_{on} is the duration of the switch "on" time. If the pulses are held constant during a line cycle, i_{pk} would essentially modulate in phase with the input voltage. The input power factor would therefore approach unity. The power available at the output of such a system is given by,

$$P_{out} = \frac{1}{2} * L1 * \left(\frac{I_{pk}}{\sqrt{2}} \right)^2 * f_s \quad (2.3)$$

where I_{pk} is the maximum value of the pulse current at the peak voltage of the line cycle. In the system, voltage feedback is used to control the width of the base drive pulses and thereby regulate this output power.

The use of PWM techniques in the circuit however, gives rise to large switching losses and noise due to the simultaneous switching of high voltages and currents. Also, the need for processing high power levels at relatively high switching frequencies calls for the use of a considerable number of switching devices connected in parallel in the circuit [5].

The relative simplicity of such a power factor correction technique however, makes it possible for it to be deployed in many other PWM or resonant mode circuit topologies. In a resonant mode topology, output power control could be obtained by means of frequency modulation. The "on" or "off" times of the switching devices could be determined by the resonant components within the circuit.

Half and Full bridge resonant inverter circuits with dynamic power factor correction have been introduced in the past by Chambers [8]. The circuits use SCRs for processing the output power. The multiple ended structure of the inversion bridge however, results in the employment of two and four semiconductor switches in the half and full bridge versions respectively. This gives rise to more components, more gate drive requirements and more integrated circuits for control, causing the cost involved and the complexity of the circuit to rise. Also, the use of SCRs in the conversion circuit causes the switching frequency to be reduced to a low level, thus not reaping the full benefits of resonant mode power conversion.

2.1.3 Input voltage modulation technique

94% of energy in ac voltage and current waveforms flowing in resistive loads occur between 30 and 150 degrees of the positive half and 210 and 330 degrees of the negative half of a cycle.

Consider for example a 1 ohm load resistance. If an ac voltage of $1\sin t$ was applied across it, $1\sin t$ of current would flow in the resistive load. The power dissipated in the load as a result during 30 and 150 degrees of the positive half cycle is given by,

$$P_1 = \int_{30}^{150} 1\sin^2 t \, dt = 1.48 \quad (2.4)$$

The power dissipated during the whole of the positive half cycle is given by,

$$P_2 = \int_0^{180} 1 \sin^2 t \, dt = 1.57 \quad (2.5)$$

The magnitude of energy (X) that occurred during the 30 to 150 degree interval as a percentage would therefore be,

$$X = \frac{P_1}{P_2} * 100 \% = 94 \% \quad (2.6)$$

This means that the modulation of the input voltage between the peak ac line voltage and half its value (corresponds to the 30 to 150 degree interval in the positive half of the voltage waveform), gives a power factor of 0.94 to the operating system (see Fig.2.3).

As described in Section 2.1, the fluorescent lamp ballast industry has used this technique for many years for obtaining good input power factors [9]. A small circuit configuration built at the front end of the supply provides the required modulation (see Fig.2.4). The circuit works in the following manner. When the switch is on, energy is stored in the primary winding P. During this interval, energy would also be coupled to the external winding M. The winding M is phased such that the diode D1 becomes forward biased and current flows through to charge C_e . When the switch turns off, the voltages change polarity and D1 becomes reverse biased thus preventing any further current from flowing into the circuit.

The voltage across C_e is maintained at 50% of the peak ac line voltage by the steering diode D2 which becomes forward biased whenever the rectified ac line voltage drops below this value. The P:M step down ratio depends upon the voltage appearing across the winding P and the voltage required across C_e . The leakage inductance present in the transformer is used to smooth the charging current waveform.

One of the main features of this circuit configuration is its simplicity (it uses only 4 extra components) which enables it to be installed at the front end of many PWM and resonant mode circuit topologies.

2.2 REVIEW OF DEVICES

Ever since the introduction of semiconductor switching devices, circuit designers have been subjecting them to increasing levels of operating stresses and demanding that these devices perform satisfactorily under these stress conditions. The different stress demands that the devices must be able to meet are :

1. Higher blocking voltages
2. More current carrying capabilities
3. Higher di/dt
4. Higher dv/dt
5. Shorter turn-on and off times
6. Lower gate drive requirements
7. Higher operating frequencies

There are many types of switching devices that are available today which can meet one or more of these requirements but, as always, an improvement in one characteristic is usually gained at the expense of another. As a result, different devices have been optimised for different applications. The following are some of the device types used mainly in the Power Electronics industry.

2.2.1 Thyristors

The bi-stable characteristics exhibited by thyristors or silicon controlled rectifiers (SCRs) enables them to be switched between a high-impedance off-state and a low-impedance on-state. The basic thyristor structure latches in the on-state but cannot be turned off by merely changing the gate potential. Thus the only way of turning it off is to starve it of anode current for about $100\mu s$ [10]. This limits the maximum frequency of operation to below 1kHz [11]. A representative device cross section and its equivalent circuit are shown in Figs. 2.5a and 2.5b [12].

Today's thyristors can be classified into six general types, namely,

1. Phase control thyristors
2. Inverter thyristors
3. Asymmetrical thyristors
4. Reverse conducting thyristors

5. Gate-assisted turn-off thyristors

6. Light-triggered thyristors

Of these, the phase control and to a lesser extent, the inverter type thyristors generally exhibit relatively slow switching characteristics due to long commutation times and thus will not be discussed here. Light-triggered thyristors are used mainly in applications requiring very high voltage devices, such as in DC transmission lines, and again will not be covered here.

2.2.1.1 Asymmetrical thyristors (ASCRs)

An ASCR is designed specifically to block lower reverse voltages when compared to a conventional thyristor. This fact provides the ASCR with an extra degree of freedom to optimize turn-on/off times and forward voltage drops. Fig.2.6 shows the basic structure of an ASCR [13]. When compared with Fig.2.5a, the main difference here is the highly doped layer that has been inserted between the n1 base and p1 anode. This n2 layer serves as a "field stopper" and allows the n1 base region to be reduced to half the width of the n1 base seen in a conventional thyristor.

The highly doped n2 layer maintains the same forward voltage blocking capability but at the expense of a reduced reverse voltage rating determined by the p1n2 junction. The much thinner n1 base makes it possible to considerably decrease the on-state voltage drop and give the thyristor a much better high frequency switching performance.

ASCRs switching at 40kHz in series resonant circuits have been reported in the past [13]. Anti-parallel diodes were used in these applications for providing the reverse voltage blocking needed. Like conventional thyristors however, the need to allow a minimum time after conduction has ceased before turn-on (typically 5 μ s) causes the switching frequencies in ASCRs to be limited to the 50kHz region.

2.2.1.2 Reverse conducting thyristors (RCTs)

The RCT represents the monolithic integration of an asymmetrical thyristor with an antiparallel diode. Beyond the obvious advantage of the parts count reduction, the RCT eliminates the inductively induced voltage within the thyristor-diode loop (virtually unavoidable to some extent with discrete components) and essentially limits the reverse

voltage seen by the thyristor to only the conduction voltage of the diode.

Both the thyristor and diode are designed for high speed switching. The thyristor part possesses most of the features exhibited in ASCRs and the diode part exhibits fast recovery characteristics. The spectrum of voltage and current ratings of the RCT is therefore similar to an ASCR [14]. The one drawback however is the fixed ratio between the thyristor and diode current carrying capabilities for a given design.

2.2.1.3 Gate-assisted turn-off thyristors (GATTs)

"Gate-assisted turn-off" is the name given to the method of turning off a thyristor with the usual commutation of the anode current, but with the addition of a negative pulse applied to the gate during the time the forward anode voltage is reapplied. The reverse current which flows as a result helps evacuate the stored charge in the device thus reducing the turn-off time by up to 50%, compared to a conventional thyristor with the same on-state voltage drop [15]. GATTs are designed with inter-digitated gate/cathode diffusions in order to achieve fast, low-loss turn-on as well as effective gate-assisted turn-off. Therefore, together with the use of a low-loss asymmetrical diffusion structure, such a scheme gives way to a much faster thyristor operation. Turn-off times of less than $4\mu\text{s}$ have been reported in the past for 1200V,400A GATTs [16].

2.2.2 Gate turn-off thyristors (GTOs)

The GTO is a four layer PNP semiconductor device, similar in construction to a thyristor but with several design features which allows it to be turned both on and off by reversing the polarity of the gate signal. A representative device cross section and its equivalent circuit are shown in Figs. 2.7a and 2.7b [10].

2.2.2.1 Turn-on and off modes

The turn-on mode is similar to a thyristor. Injection of hole current from the gate, forward biases the cathode as seen in Fig.2.8. These holes then flow to the anode and induce electron injection from the anode emitter. Injection of holes and electrons into the base regions continue until charge multiplication effects bring the GTO into conduction. As with a conventional thyristor, only the area of the cathode adjacent to the gate electrode is turned

on initially, with the remaining area brought into conduction by plasma spreading. However, unlike in the thyristor, the GTO consists mainly of narrow cathode elements, heavily interdigitated with the gate electrode, and therefore the initial turned on area is very large and the time required for plasma spreading is small. The GTO is thus brought into conduction very rapidly and can withstand a high di/dt at turn-on.

In order to turn-off a GTO, the gate is reverse biased and the holes are extracted from the p-base as shown in Fig.2.9. Hole extraction continues until the excess carrier concentration is low enough for carrier multiplication to cease and the device reverts to the forward blocking condition.

2.2.2.2 Operating limitations

Operation of the GTO in the classical switching mode is limited by three factors, namely [18] :

1. Tail loss
2. Gate drive
3. ITCM

2.2.2.2.1 Tail loss

The turn-off of a GTO proceeds in three stages :

1. Storage time
2. Fall time
3. Tail time

During the storage time the conducting area is reduced due to a squeezing action of the gate drive, and the negative gate current increases to a peak value. The duration of the storage time depends on how rapidly the excess charge is removed by the gate and is therefore a strong function of the negative rate of fall of gate current. At the end of the storage time, the anode current falls rapidly and the negative current begins to decay as the gate junction is forced into avalanche. The avalanche condition is not damaging to the GTO and assists in the removal of stored charge from the device. During this period the blocking junction of the GTO recovers and the anode voltage rises.

After the fall time, the anode current has fallen to a low value, I_{tail} which decays more slowly. This tail period is an important factor in determining the switching losses and the operating frequency of the GTO, since the anode voltage is high during this time.

2.2.2.2 Gate drive

The negative drive been applied to the gate to turn off a GTO causes part of the main anode current to be diverted through the gate. The gate drive circuit must be capable of sinking this current. In cases where isolated gate drive is required, this would cause difficulties thus making the drive circuit quite complex.

2.2.2.3 I_{TCM}

There is an absolute maximum on-state current that a GTO can turn-off at a given dv/dt . This current is lower than the maximum the device is capable of conducting. Therefore in a conventional switching circuit where the current rises linearly, the GTO would not be used to its full potential.

If on the other hand, GTOs were installed in zero-current switching resonance circuits where the anode current falls naturally to zero, most of the limitations mentioned above could be overcome. For example if the anode current has fallen to zero, the tail losses would disappear. The complicated and expensive gate drive is caused by the need for a high current sinking capability to turn-off the anode current. Again if the anode current is zero at turn-off, the current out of the gate will be very much smaller, thus reducing the gate drive requirements to a minimum. The I_{TCM} restriction disappears because the GTO no longer controls the current via the gate. This allows the full current rating to be utilised and, the GTO being a derivative of the thyristor family, makes it possible for very large peaks of current to be passed through.

2.2.2.3 Advantages of using GTOs

The advantages of using the GTO thyristor as opposed to conventional fast thyristors in switching circuits are :

1. Simplified power circuit configuration due to the elimination of the additional

forced commutating circuit

2. Therefore, a lower volume and weight specification
3. No commutation losses
4. Greater power efficiency

Set against this is the need for a more sophisticated gate drive circuit to perform the turn-on and more particularly the turn-off function. It is estimated that the negative current required to turn-off a GTO is around one-fifth of the anode current, at a voltage no greater than the gate-cathode reverse breakdown voltage [17].

The use of GTOs in place of conventional thyristors in resonance circuits not only removes the limitations of the GTO as described in Section 2.2.2.2 but allows it to partially overcome the thyristor limitations as well [18]. For example, situations may arise in some resonance circuits during start-up where although the anode current has fallen to a low value, it does not quite reach zero. If the active device was a thyristor and the level of the anode current was higher than the holding level, the device would not commutate. The use of a GTO in such a situation overcomes this problem by forcing the device to turn-off and since the current level is low, the gate drive circuit required would be less complex.

Although the anode current falls naturally to zero in more conventional zero-current switching resonance circuits, a negative voltage is usually applied to the gate of the GTO at turn-off to keep T_q as low as possible. This negative voltage extracts some of the charge stored in the region under the cathode diffusion. The charge must be removed before the forward voltage is reapplied. The inter-digitated pattern of gate/cathode diffusions in a GTO creates a situation where none of the stored charge is far from the gate connection. The negative gate voltage therefore has a strong influence over all the stored charge, which can be quickly and efficiently extracted via the gate. This gives the GTO a T_q of less than $1\mu\text{s}$, much smaller than that possible in a GATT thyristor [18].

If the GTO is compared with the bipolar power transistor and the power MOSFET, it offers higher voltage and current carrying capabilities and the ability to withstand very high peak forward currents as seen often in resonance circuits. This feature and the advantages mentioned above makes the GTO a very attractive and economical alternative to these more popular devices, especially in single ended resonance circuits operating at high power levels.

2.2.3 Bipolar transistors

In the last decade, significant improvements have been made in the bipolar transistor technology to meet the challenges been offered by thyristors and power MOS devices. In meeting these challenges, new devices with faster switching speeds and lower switching losses have been developed that offer better performance characteristics compared to some power MOS and most thyristor devices.

The emitter design used in power transistors influences its turn-off characteristics considerably. Hollow and ring emitter structures are often used in commercial devices today for obtaining better turn-off performance [11]. In a hollow emitter structure, fast turn-off is obtained by confining conduction to the deeper emitter regions where stored energy could be more easily removed. In a ring emitter structure, series resistors are added to every emitter site to prevent current crowding and thus provide an improved turn-off performance.

The collector design plays an important role in determining switching losses and RBSOA performance of a bipolar transistor [19]. Switching losses are found to increase with collector thickness due to a large quasi-saturation region and thus more voltage tailing during turn-off. RBSOA performance on the other hand improves with increasing collector thickness due to the lower induced field caused by space charge limited current in the collector. A trade-off between the two could however be reached by using multiple epitaxial collector structures [19]. With a properly graded epitaxial layer structure, a dramatic improvement in RBSOA can be obtained while maintaining low switching losses and high current gain hold up.

For a given collector and current gain requirement, the current density of a transistor declines rapidly as the switching voltage (V_{CEO}) increases [19]. For a Darlington design however, where a monolithic driver transistor drives the base of the main power transistor, the current density is much improved compared to that of the main transistor used on its own. For applications requiring higher sustaining voltages therefore, the use of a power Darlington will result in a smaller, less expensive device for a given collector and current gain [19].

However, a bipolar transistor being a minority carrier device, often requires appreciable storage times to sweep carriers out of the base region [20]. Although these storage times could be reduced by increasing the magnitude of negative bias being applied at turn-off, it can suddenly lose its voltage blocking capability when turning off an inductive load due to secondary breakdown occurring [21]. The maximum operating frequency of a bipolar

transistor is therefore comparatively low. Although Reverse Emitter Current Drive (REC Drive) can be employed to extend this frequency, it would involve the employment of very elaborate drive circuitry [20].

2.2.4 Power MOS field effect transistors (Power MOSFETs)

The power MOSFET is a device that evolved from MOS integrated circuit technology. The motivation for the development of these devices arose due to the large base drive current requirements and limited switching speed capabilities exhibited by the conventional bipolar transistors.

The power MOSFET is turned on by charging up its input capacitance and hence is a voltage-driven device. A gate terminal isolated by silicon dioxide from the conductive channel controls the drain-to-source current flow in the device. Two successively diffused junctions define channel length thus giving it the double diffused MOS (DMOS) name. High breakdown voltage and current ratings are obtained by placing the drain on the opposite side of the wafer as shown in Fig.2.10 [22].

The introduction of power MOSFETs was originally regarded as a major threat to the power bipolar transistor [19]. Initial claims of infinite current gain for the power MOSFETs were diluted by the need to design the gate drive circuit to account for the pulse currents required to charge and discharge the high input capacitance of these devices. This was especially true in high-frequency applications where the power MOSFET was particularly valuable due to its inherently high switching speed. The high-speed capabilities were the result of current transport occurring solely via majority carriers. This eliminated the large storage and fall times observed in bipolar transistors due to minority carrier transport. The power MOSFETs were also found to exhibit safe-operating areas and their positive temperature coefficient of resistance facilitated the paralleling of these devices for higher output power levels [20]. This is far more efficient than the paralleling of bipolar transistors which require special circuit configurations to avoid thermal runaway.

These advantages are however offset by a higher on-state resistance per unit area in the power MOSFET [22]. The break-down voltage rating of the power MOSFET determines its on-state resistance. Higher breakdown voltages result in greater on-state resistances. Power MOSFETs have therefore been confined to applications requiring low breakdown voltages (less than 500V) where their on-state resistance reaches acceptable levels. The high fabrication cost involved is another reason for not seeing the power MOSFET in wide spread use, confining them to applications requiring high frequency switching only [19].

2.2.5 MOS-Bipolar combinational devices

With the discovery that power MOSFETs could not displace power bipolar transistors in high voltage applications, many researchers began to look at the possibility of combining these technologies to achieve a device which has a high input impedance as well as a low on-state resistance. By doing so, an operating characteristic is obtained which could not have been achieved if either device was used on its own.

Several bipolar-MOSFET combinational power transistor configurations such as cascade, cascode, parallel and MOSBIMOS which is a combination of the former two, have emerged in the recent past [23] [24]. The circuit configurations of all four combinations are shown in Figs.2.11 to 2.14. In most of these combinational devices, the bipolar transistor is driven by a power MOSFET. The circuit element is thus gated "on" like a power MOSFET and a lower on-state resistance is obtained since most of the output current is handled by the bipolar transistor.

2.2.5.1 Cascade configuration

The cascade configuration operates like a Darlington transistor except that the driver M1 in this case is a MOSFET. When the gate voltage is high, the input current to the switch is used to provide base current for the bipolar Q1 thus turning it on faster. This current is switched through the MOSFET M1, which has a very small turn-on time. When the gate voltage is low, M1 cuts off turning Q1 off in the process.

The MOSFET control input, anti-saturation behaviour and the absence of a separate control source for the bipolar component are the main features of this configuration. The turn-off speed however, depends on the existence of the diode D1 [23]. Without the diode, the excessive charge in Q1 decays solely due to recombination effects and the device turn-off is therefore slow. With the diode however, the Q1 turn-off would be more rapid, but at the expense of a more complicated turn-off process [23].

2.2.5.2 Cascode configuration

The cascode configuration requires a continuous base current for Q1 and a positive voltage for M1 to initiate turn-on and maintain continuous conduction through the switch. For turn-off however, a negative or zero gate bias is all that is required. Thus when the gate voltage is low, M1 turns off with Q1 then being turned off by an emitter open scheme. The

zener is used to provide a path for Q1 base current when the emitter is open-circuited.

There are several distinct advantages in using such a scheme. The first is the ease of turning off a high voltage bipolar device. The second is the small turn-off time obtained. The third is that the main transistor Q1 can operate up to its BV_{CBO} rating without secondary breakdown occurring. The MOSFET input is also an added benefit although a separate uncontrolled current source is needed for the bipolar transistor.

2.2.5.3 Parallel configuration

The parallel configuration employs two signals driven in such away that the bipolar transistor Q1 turns-on after the MOSFET M1 has turned-on but turns-off before the MOSFET turns-off. The MOSFET device thus handles the input current during switching thus permitting very high switching speeds. Since the bipolar transistor Q1 carries the input current when the whole device is not switching, conduction losses would be low. A further benefit is the ability of the bipolar transistor Q1 to operate up to its BV_{CBO} rating without secondary breakdown occurring, since the bipolar transistor is not subjected to simultaneous stresses of voltage and current. However, the price paid for these benefits is the increase in drive complexity, which must be designed in such away that specific non-simultaneous drive signals are applied to the two devices.

2.2.5.4 The MOSBIMOS switch configuration

The MOSBIMOS is a combination of a low voltage high current power MOSFET M1, a high voltage low current power MOSFET M2 and a high voltage and current bipolar power transistor Q1. By combining the best features of each of these switching devices, an operating characteristic is obtained which cannot have been achieved if either device was used on its own.

The MOSBIMOS uses the input current to the switch to provide base current for the bipolar device Q1, thus turning it on faster. This current is switched through the high voltage MOSFET M2, which has a very small turn-on time. Thus when the gate voltages are high, both M1 and M2 conduct. This provides base current to Q1 and the entire configuration turns on. When the gate voltages are low, both M1 and M2 turn-off and Q1 is thus turned off by an emitter open scheme. The zener is used for two purposes. The first is to provide a path for Q1 base current when the emitter is open circuited and the second is to provide a

path for the M2 gate discharge current at turn-off.

In this configuration, both Q1 and M2 breakdown voltage ratings are determined by the circuit in which the MOSBIMOS is installed. M1 remains a low voltage, low $R_{DS(ON)}$ device with the same current rating as Q1. M2 need only be rated for a current equal to the base current required by Q1.

The simplicity of the drive circuit, where the base current is automatically adjusted to be proportional to the input switch current, such as seen in the cascade configuration, is a main feature of this configuration thus leading to a much safer operating area. The overcoming of disadvantages such as saturation and separate control sources for the bipolar transistor are added features of this scheme.

The basic properties of all these switch configurations are summarized in Table 2.1 [25]. The diode D1 is not connected in the cascode configuration here. It is clear from the table that the properties of the bipolar and MOSFET transistors are more or less complimentary and the only way of obtaining the advantages been offered by both devices is to deploy them in a MOSBIMOS switch configuration.

2.2.5.5 The MOSBIMOS switch configuration employed in resonance circuits

Resonance converter circuits can be broadly categorised into two sections depending on the number of semiconductor switches been used. Converter topologies with a single semiconductor switch are called single ended schemes and have been derived originally from T.V. horizontal deflection circuits. The other category is the multiple ended scheme where more than one semiconductor switch is used to transform power.

Most single ended schemes proposed so far have been confined to lower input voltage applications at lower power levels. If higher input voltages at higher power levels are to be considered, semiconductor switches with high voltage and current ratings will be required. Although SCRs and GTOs have been used in the past for such applications, the price paid has been the reduction in switching speed and the increase in circuit complexity. A MOSBIMOS switching device on the other hand enables the switching frequency to be raised up to several hundred kHz while maintaining high voltage and current carrying capabilities.

The cascode version of this switch configuration described in Section 2.2.5.2, was first employed in a high voltage application by Lutteke and Rates [26]. The circuit consisted of a

120V mains driven Class-E converter, used as an electronic ballast for a 15W fluorescent lamp operating at 450kHz. The employment of such switch configurations in resonance circuits has since been presented at regular intervals with higher voltage and power levels being reached with the advent of better discrete devices.

A MOSBIMOS switch configuration employed in a 240V mains application has been presented in the very recent past by Amarasinghe and Manning [27]. The circuit consisted of a 250W zero-current switching quasi-resonant flyback converter operating at 300kHz. The high VA characteristics required by the single ended circuit was easily met by the employment of the MOSBIMOS switch. The use of this switch also enabled the switching frequency to be raised to a high value thus fulfilling the fundamental precondition for miniaturisation.

2.2.6 MOS-gated conductivity modulated devices

MOS-gated conductivity modulated devices (CMD), represent a new class of power devices which combine both the bipolar and MOS capabilities. One of the best known MOS-CMDs is the insulated gate transistor (IGT) which is also referred to as GEMFET or COMFET.

The IGT device results from the functional integration of the physics of a MOS structure for controlling current and the physics of a bipolar device for conducting the current. The advantages offered by such a scheme such as lower gate-drive power requirements, unique reverse blocking capabilities, superior safe-operating areas and high temperature performance have, however, been overshadowed by the relatively long turn-off times needed by these devices [19]. This has limited them to operating frequencies below 50kHz. Although switching frequencies of upto 250kHz have been exhibited by IGTs installed in resonance circuits, such operations have given rise to high turn-on losses and problems associated with dv/dt due to the nature of the circuit operation [28].

2.2.7 Static induction transistors (SITs)

A family of power static induction devices have been developed in the last two decades after the realisation of the power static induction transistor (SIT) in 1970 [29]. The SI thyristor, the MOSSIT and the SIT image sensor belong to this family.

The SIT is a device in which the main current flowing between the drain and the source is

controlled by the height of the potential barrier in the channel. The height of this potential barrier is capacitively controlled by the gate and drain voltage. The structure of the SIT is such that a shortened channel length has made it possible to increase the current carrying capability, reduce power-loss by multiple channels and minimize the series resistance that contributes to the saturation of the drain current. Being a majority carrier device, the SIT is suitable for high frequency operations and furthermore, a negative temperature coefficient of current makes it difficult for thermal runaway to occur thus making it suitable for high power applications.

On the negative side however, a low current gain and complicated drive circuitry has confined the SIT to a limited number of applications, although much work is presently being done to overcome these disadvantages, thus making the SIT a very attractive device for the future [20].

2.3 CONCLUDING REMARKS

Under steady state operating conditions, i.e. no continuous line or load changes, the dynamic power factor corrected converter circuit presents a good input power factor. The smoothed DC output voltage produced contains a small 100Hz rectified mains frequency ripple, with the magnitude of the ripple being determined by the output filter capacitor used. Further ripple reduction, if needed, could be provided via a simple DC-DC converter.

The input voltage modulation technique is another useful tool for providing power factor correction. The modulation circuit when installed at the input stage of a high-frequency converter, provides a near ideal supply for use in mobile applications, where the power systems weight plays a vital role.

The suitability of a switching device for deployment in a power factor correction circuit, depends upon both its operating frequency and power handling capability. These criteria are considerably affected by the particular configuration in which the device is used. Most single ended structures need semiconductor switches with high voltage and current ratings, due to the need for processing power with only a single switching element.

A GTO device was shown to be an excellent choice for such an application, especially when employed in a resonance mode circuit. For applications requiring high frequency power processing however, the MOSBIMOS switch configuration proved to be a more suitable candidate.

In the following chapters therefore, a dynamic power-factor corrected resonance circuit employing a single GTO device and an input voltage modulated, high-frequency resonance circuit employing a MOSBIMOS switch configuration, will be discussed.

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2.5 TABLES

	MOS	Bipolar (Common Emitter)	Bipolar - MOS			
			Cascade	Cascode	Parallel	MOSBIMOS
On state losses	-	+			+	
Drive power losses	+	-	+	-	-	+
Switching speed and losses	+			+	+	+
Storage time	+	-	-	+	-	+
Drive circuit requirements	+	-	+	-	-	+
SOA protection requirements	+			+	+	+

- Obvious advantages, no problems
 Moderate performance, problems can still be solved
 Obvious drawbacks, solutions more elaborate

Table 2.1 A comparison between Bipolar-MOS switch combinations

2.6 FIGURES

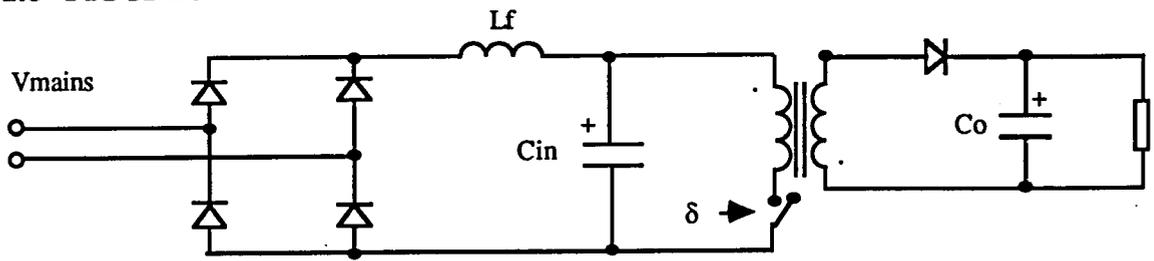


Fig.2.1 Power factor corrected flyback converter.

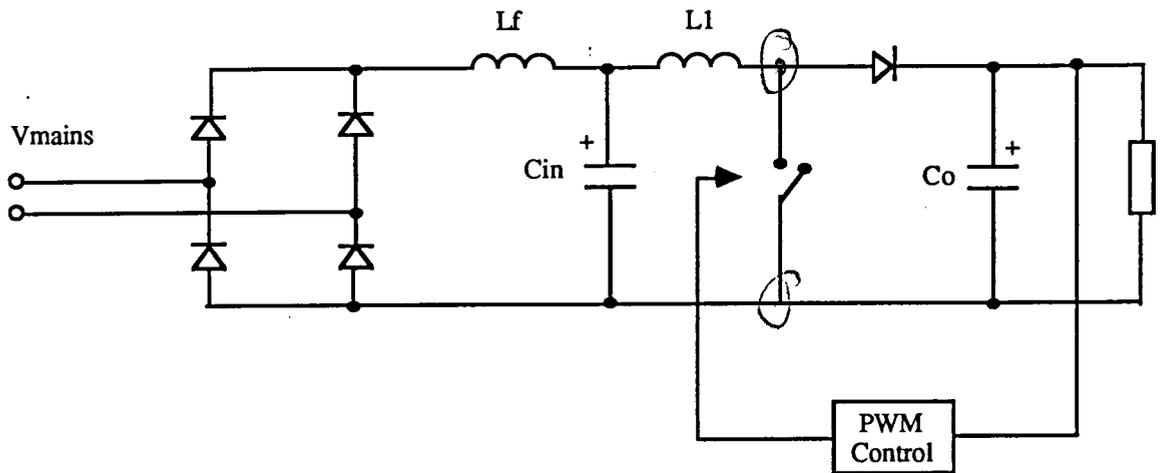


Fig.2.2 Dynamic power factor correction in a boost converter

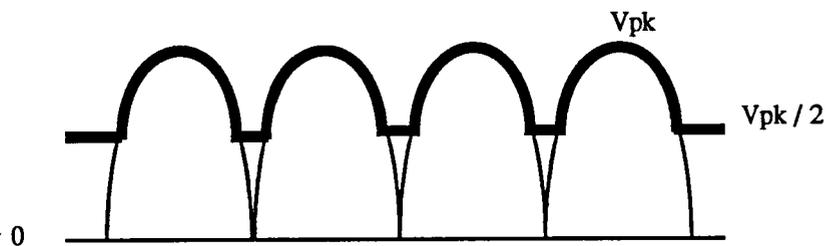


Fig.2.3 Input voltage modulation technique

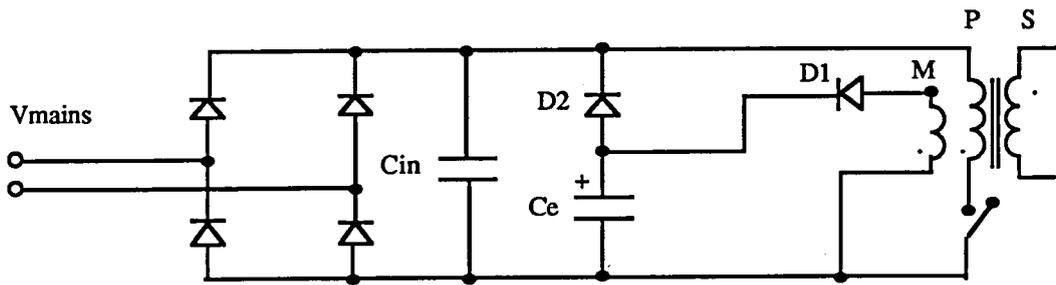
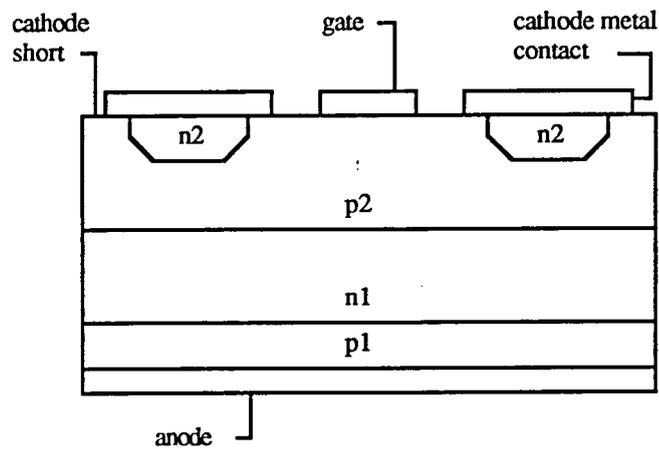
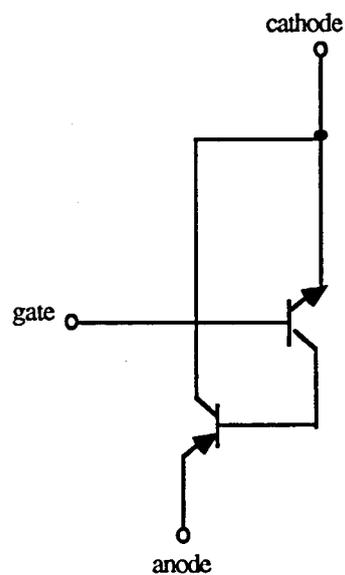


Fig.2.4 Implementation of the input voltage modulation technique



a. Simplified cross section



b. Equivalent circuit

Fig.2.5 A conventional thyristor

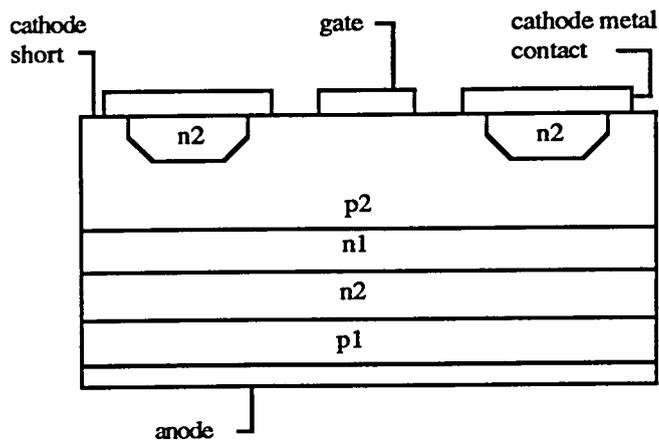
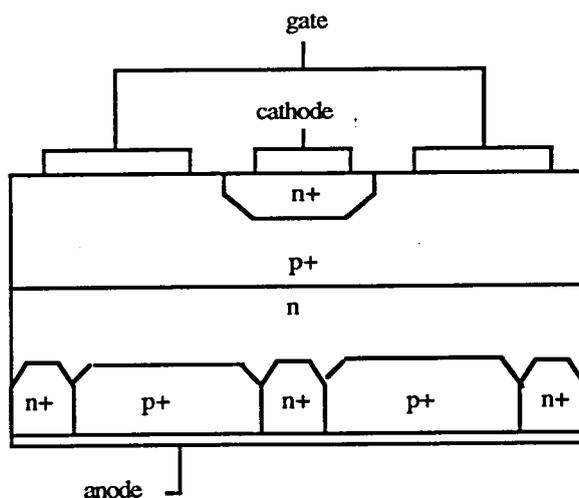
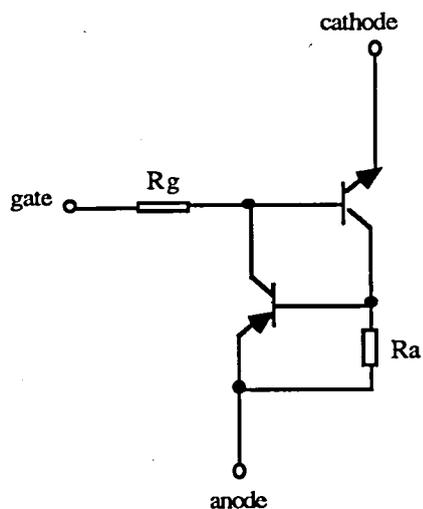


Fig.2.6 The simplified cross section of an ASCR



a. GTO cross section



b. GTO equivalent circuit

Fig.2.7 A GTO thyristor

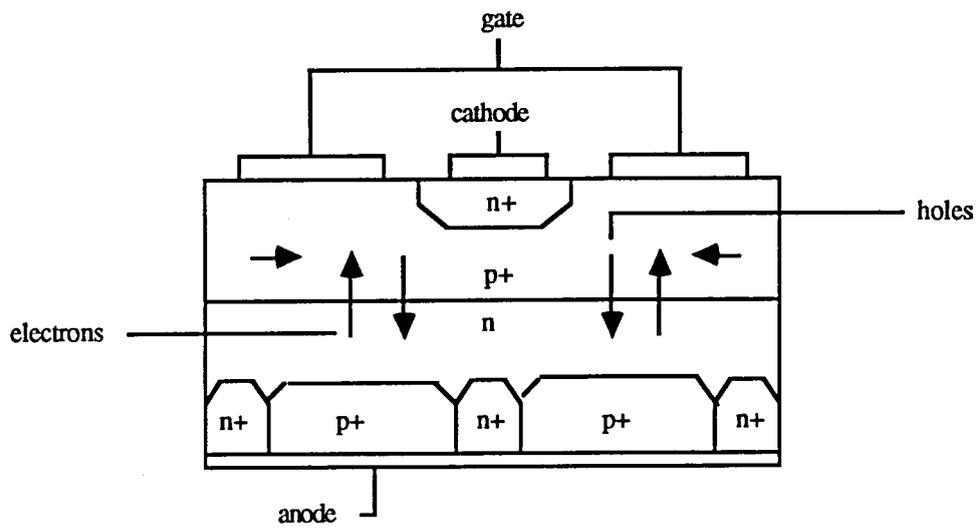


Fig.2.8 A GTO thyristor during turn-on

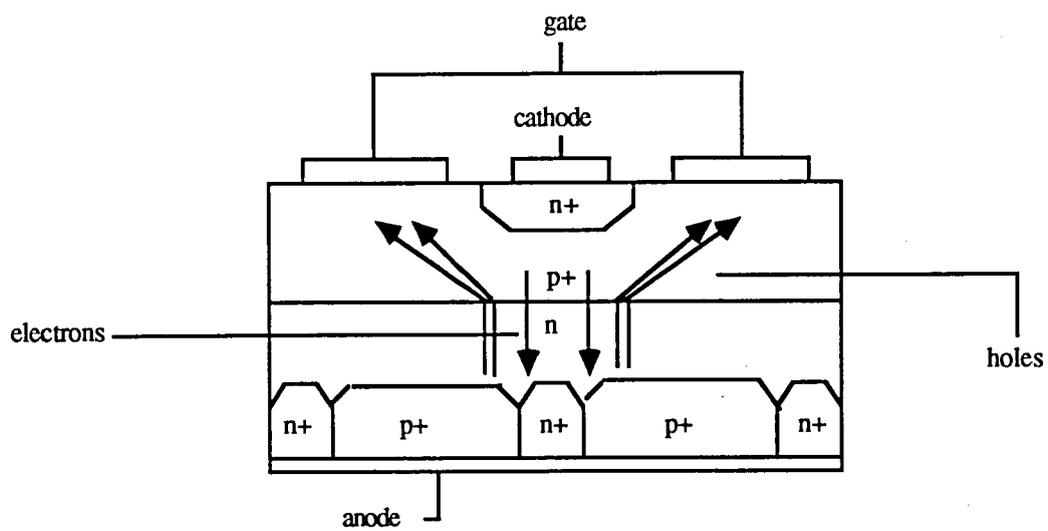


Fig.2.9 A GTO thyristor during turn-off

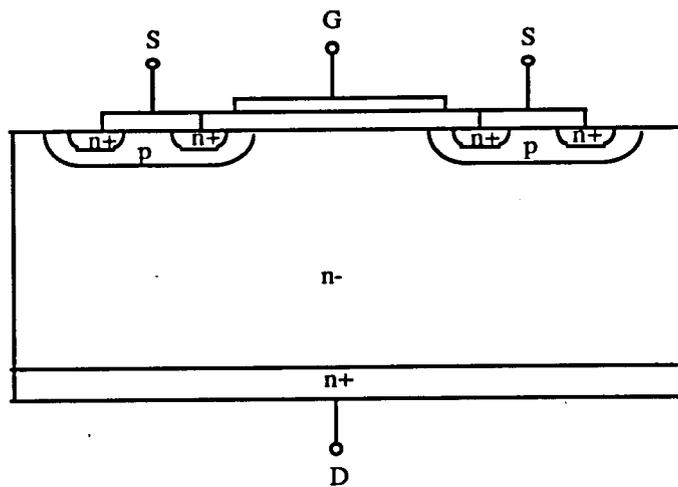


Fig.2.10 The MOSFET structure

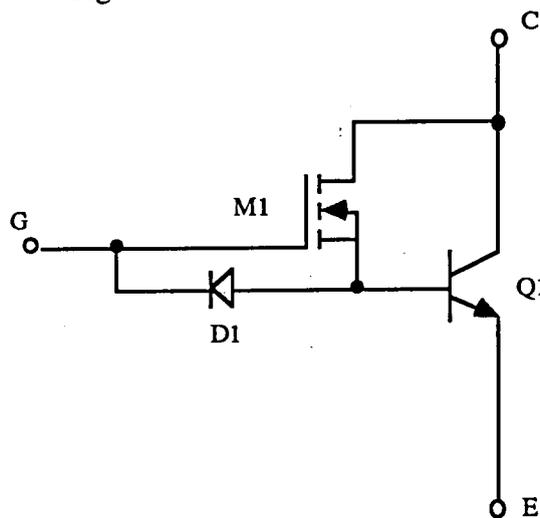


Fig.2.11 The cascode configuration

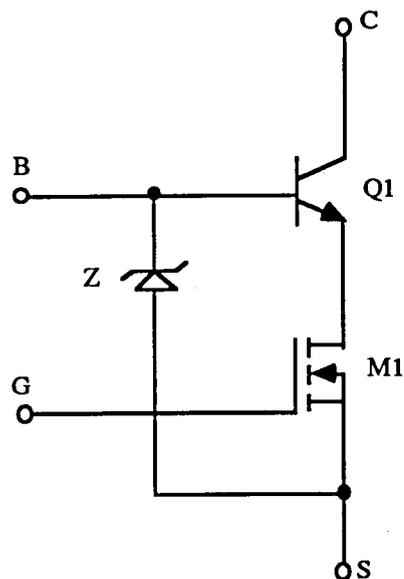


Fig.2.12 The cascode configuration

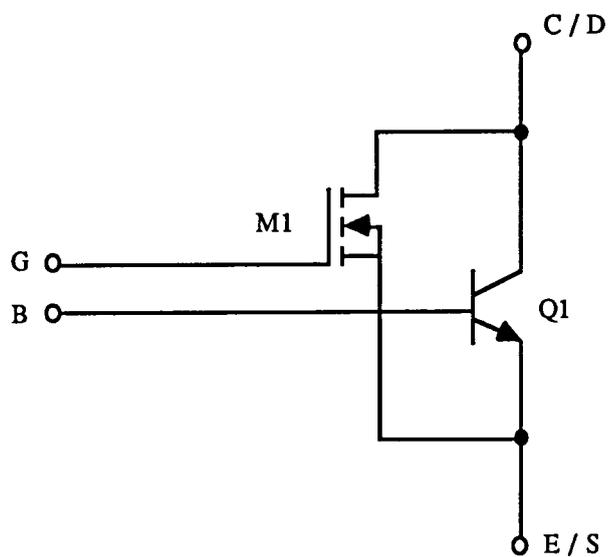


Fig.2.13 The parallel configuration

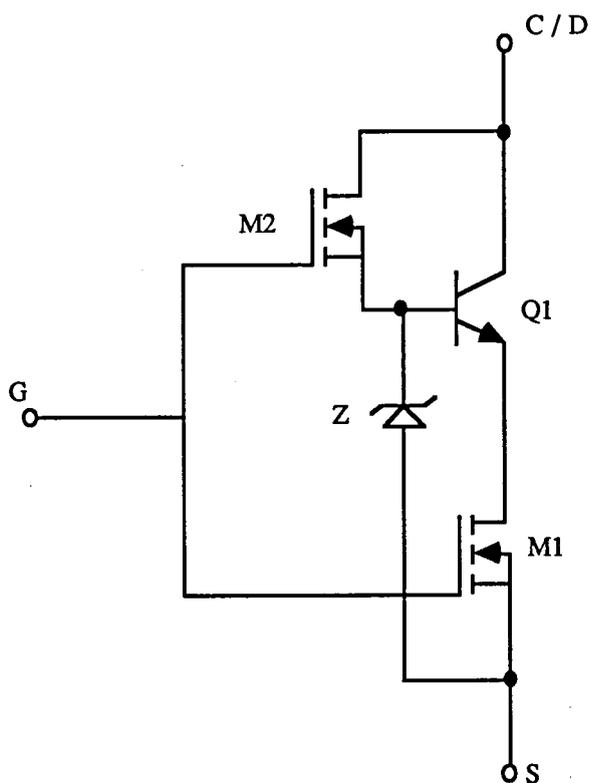


Fig.2.14 The MOSBIMOS configuration

CHAPTER 3

COMPUTER MODELLING OF ACTIVE DEVICES
USING THE PSPICE MICROCOMPUTER
SIMULATION PROGRAM

The chapter provides an overview of the methods used to model active semiconductor devices. The Parts program installed in PSpice is used to model diodes and bipolar transistors. The modifications that are needed to the Power MOSFET models in PSpice, when simulating high frequency circuits are discussed in the chapter. A two transistor model which replicates the action of a GTO thyristor is also presented.

3.1 THE ORIGINS OF PSPICE

The Computer Aided Design and Analysis (CADA) field erupted on the scene in the mid 1960s with the introduction of the ECAP computer program [1]. This gave the opportunity for design engineers to analyse circuits without having to write the defining equations for the first time. Computers, both Analogue and Digital, had long been used to solve equations, but with ECAP, a breakthrough was established - a computer program able to both write and solve the system equations automatically, with only a topological listing of the circuit components being required as the input. After several years, other CADA programs became available, many offering improvements and additional features.

The SPICE suite of programs was originated by Lawrence Nagel at the University of California, Berkeley, U.S.A in the mid 1970s. As large scale integration became possible, it was no longer feasible to simulate new circuit ideas using breadboards. A reliable software package to simulate integrated circuit behaviour was thus required. SPICE1, Simulation Program with Integrated Circuit Emphasis, was developed by Nagel to fulfil this requirement.

SPICE1 was soon followed by SPICE2 [2] with many improvements and additional features. In the late 1970s and early 1980s, SPICE2 became an "industry standard package" for electronic circuit analysis and as a CAD tool. So much so, that there were reports of it being accessed over six thousand times per month by the "Silicon Valley" industries on the mainframe computers at Berkeley.

A mainframe computer was necessary to run SPICE2 in most versions upto the late 1970s at most sites. However, with the advent of PC based SPICE software for relatively powerful microcomputers, it has become feasible to put circuit analysis tools on every engineers desk. There are several versions of SPICE, derived from the original Berkeley version, available for use on microcomputers. They could principally be differentiated from each other by their added features, performance, cost, and support [3].

The version of SPICE that is been used here is called PSpice, by MicroSim Corporation, which requires 512-kilobytes of memory, a floating-point coprocessor and a MS-DOS 2.0 (or later) operating system [4]. The addition of graphics post-processor software to this program brings the power of a smart oscilloscope to the PC-based power electronics engineering workstation.

3.2 PSPICE FOR POWER SYSTEM CAD

PSpice allows the user to simulate a circuit design before so much as touching the first piece of hardware. The response over time to different inputs, the response to different frequencies, noise and other information about the circuit are all available. In effect, PSpice allows the user to do a "computer breadboard" of the circuit before building anything.

The computer methods used in PSpice can be thought of as consisting of three layers, with each higher layer using the others below it [3]. The top layer is the matrix algorithm for solving simultaneous linear equations. The next level is that used for the solution of nonlinear algebraic equations using the Newton-Raphson iterative method in which the nonlinear equations are approximated by a sequence of linear equivalents that converge on to the actual solution. The third level reduces a system of nonlinear differential equations to their nonlinear algebraic equivalents using a trapezoidal integration algorithm and an automatic step size control to maintain the specified precision.

The program can carry out different types of analysis such as d.c., a.c., transient and analysis at different temperatures. Circuits may contain resistors, capacitors, inductors, mutual inductors, independent and dependent voltage and current sources, transmission lines and five types of semiconductor devices, namely diodes, BJTs, JFETs, MOSFETs and GaAsFETs.

3.3 MODELLING OF ACTIVE DEVICES

As described in Section 3.2, five types of semiconductor devices are available in PSpice. All these devices need to be represented by equivalent models. A model is used to assign values to various parameters which describe the device. The user can set the values of none, any or all the parameters of the model. The parameters not specified are set to their default values by PSpice.

One of the difficult areas in using analogue circuit simulators is finding accurate models for off-the-shelf parts. To the question, "Why does one need to model these devices, won't the data sheet values work?", the answer would be "yes" and "no". "Yes", for simpler devices such as a resistor which just needs the resistance value to have a complete model. "No", for more complex devices, especially semiconductor devices. For example, the physical model for predicting how a transistor operates views the transistor from the "inside". However, the manufacturer provides measurements that show the transistor operating from the

"outside". Therefore, a conversion is necessary from data sheet values to physical model parameters.

3.3.1 The Parts program

The Parts program installed in PSpice is a semi-automatic aid for determining model parameters for the active devices available in PSpice. By using Parts, the user is able to convert information from the component manufacturer's data sheets. The result would be a model representing the device by means of an equivalent circuit.

3.3.1.1 The modelling of a diode using Parts

The diode element in PSpice consists of a nonlinear current source to model the ideal diode law (Shockley equation) and reverse breakdown. A variable capacitance accounts for the semiconductor junction charge storage. The effects of both the ohmic resistance and the high-level injection are modelled by a series resistance.

Model parameters obtained for a BYT230PIV-1000 type diode and a BZY93-C10 type zener diode are given in Appendix 1.

3.3.1.2 The modelling of a bipolar transistor using Parts

The bipolar transistor element in PSpice is a more comprehensive version of the classic Gummel-Poon model. The model is implemented as an extension of the Ebers-Moll model so that it defaults to that model when the appropriate parameters are specified. The very simple Ebers-Moll model could therefore be used if the bipolar transistor is working only as a dc switch. The Gummel-Poon model takes into account effects such as β variation with time, charge-storage, basewidth modulation and temperature variations. In addition to these, the version installed in PSpice has been improved to include features such as modelling of the variable base resistance, collector-base capacitance splitting and variable forward transit time.

Again, the model parameters obtained for a BUS133A type bipolar device is given in Appendix 1.

3.3.2 Power MOSFET model

One of the key challenges facing many circuit designers at present, is the development of a useful model that replicates the behaviour of a power MOSFET switching transistor. This stems from the nature of the original SPICE MOS models, which were developed for lateral MOS IC transistors and not their cousins, the vertical DMOS power FETs. Although SPICE will model the enhancement mode MOS channel behaviour, it does not reflect the difference in drain circuit structures, particularly the body diode characteristics and the highly non linear gate-to-drain (Miller) capacitance.

The inadequacies of the standard MOS models in representing switching waveforms of MOSFET transistors prove to be significant, even for power converters designed for relatively low frequencies of operation [5]. The problem is compounded when attempting to simulate higher frequency circuits or complex power circuits which must minimize switching time errors due to dead time or conduction overlap. Due to these limitations, the usefulness of circuit simulation for design checking and analysis has been limited.

3.3.2.1 The internal MOSFET model used by Parts

Parts however uses the recently developed level 3 MOS model from University of California, Berkely, which was designed especially to model the short-channel effects of vertical DMOS power FETs.

The device is modelled as an intrinsic MOSFET with ohmic resistances in series with the drain, source, gate and bulk (substrate) as shown in Fig.3.1. The bulk is however, tied to the source in a three terminal power MOSFET device. Positive current flows from the drain through the channel to the source.

A study done by Bowers and Neinhaus [6] has indicated the importance of including the parasitic source and drain inductances to the MOSFET model. By doing so, the accuracy of the MOS dynamic model can be improved significantly. Fig.3.2 shows the MOSFET model with these inductances included. The external source inductance (in the lead connecting the source and the turn-on pulse ground return lead) also plays an important role in determining the speed of the switching transients. This inductance will therefore be added to the model when simulating the practical circuits in the latter chapters.

3.3.2.2 Modelling the variable drain-gate capacitance

As mentioned before, the drain-to-gate capacitance is a critical factor in determining the switching behaviour of a power MOSFET. This capacitance varies in value over a 100:1 ratio as the MOSFET switches between conducting and nonconducting states. A successful power MOSFET model therefore requires an accurate method of representing this variation. This must also be achieved without making excessive demands on the computational resources of the host machine.

The attempts made to simulate this drain-gate capacitance variation with voltage so far, have involved representations by polynomials based on the drain-gate voltage. A higher order polynomial is used to model the rapid transition of C_{dg} , from a high to a low value as V_{dg} increases [7]. This is achieved by the use of a voltage dependent capacitor, connected in series with a voltage-controlled voltage source. This has the effect of causing the drain-gate capacitance to decrease with increasing drain-gate voltage.

This approach however has its limitations. Most of the capacitance changes occur at gate voltages near the MOSFET threshold voltage. At high drain-gate voltages, the capacitance is small and fairly constant. Therefore, an accurate modelling of both these capacitance variations is not possible with the limited number of power series terms available.

A more recent model by Hancock [8] therefore, separates these two regions of capacitance variations, with the first region (up to a drain-gate voltage of 20V) using a nine-term polynomial to match the low voltage capacitance characteristics, and the second region using a constant capacitance to match C_{dg} at high voltages. Two switches, a JFET and a current source switch, are used to connect and disconnect the two regions.

These sub-circuit representations of power MOSFETs however, result in more complex device models, longer computation times and therefore more memory requirements. They could also give rise to problems associated with convergence, when incorporated into more complex circuit configurations. Parts however does not need such sub-circuit representations. It predicts an average capacitance value for the MOSFET and maintains this value over the entire period of operation. The method adopted by Parts in obtaining this value is as follows.

It calculates the change in the gate charge over the threshold voltage region, obtained directly from the V_{GS} vs time plot (see Fig.3.3) and predicts the average capacitance value for this time interval.

$C_{dg(av)}$ is therefore given by,

$$C_{dg(av)} = \frac{\Delta Q_g}{V_{DD}} \quad (3.1)$$

since the change in the voltage across this capacitance during this time interval is equal to V_{DD} . It could thus be seen that although this model is not as accurate as the previously discussed models, it is much more simpler to implement in a circuit. The level of inaccuracy could be measured as follows.

Consider the switching time test circuit shown in Fig.3.4. The parameters for an IRF250 type power MOSFET device, obtained by using Parts is used in the simulation. C_{dg} was obtained according to the procedure described above. A listing of the program used is given in Appendix 2.

The simulated waveforms of the gate-source and drain-source voltages and the drain current are given in Figs.3.5a - 3.5c. These results are summarized in Table 3.1 along with the published data [9]. They indicate approximately the same delay times, but longer rise and fall times. The discrepancy in the fall time is however, much greater than that observed in the rise time.

The rise and fall times are determined by the length of the threshold voltage plateau region in the gate-source voltage waveform. This region corresponds to the times during which the drain-gate capacitance is charged or discharged. In a practical circuit, C_{dg} changes from a small to a large value during turn-on and again back to a small value during turn-off. Since Parts uses an average value for the entire region of operation, its value is higher than what is observed during the initial part of the turn-on period, thus causing the rise time to increase. Similarly, since C_{dg} is higher than what is observed in real life during the latter part of the turn-off period, the fall time will increase due to the discharging of a relatively large C_{dg} at a high drain voltage.

This discrepancy in the turn-off time does not however, affect high frequency resonant circuits, operating in full-wave mode and switching off at zero-current, since the current reverses through a diode connected across the MOSFET at zero-current, thus providing sufficient time for the switch to turn-off during this period. All the circuits to be simulated in the latter chapters adopt this method of turn-off. Therefore, the MOSFET model created

by Parts could be used effectively in these circuits. Although the turn-on time is also higher than that seen in practise, the results above show that the discrepancy is relatively small and therefore would not affect the circuit performance significantly. Furthermore, using a constant capacitance would result in a much simpler model requiring less computation time and less memory requirements.

3.3.2.3 Modelling the body-drain diode

In most publications so far, the body-drain diode in a power MOSFET has been modelled with a separate diode, connected externally to the level 3 MOSFET model. The source-to-drain diode of the built in MOSFET model was not used, since its corresponding resistance was adjusted to provide satisfactory simulation of the MOSFET output characteristics in the linear region [7]. As a result, the source-to-drain diode in the MOSFET model was shut off by specifying $I_S=0$.

However, improvements made to the Parts program has enabled the user to use the body-drain diode within the power MOSFET model, without needing to create a subcircuit to represent this external diode. Furthermore, the program has also been improved so that the user could model "off" state conduction as well as switching delays without having to use a subcircuit representation, thereby again, saving on computation time and overall memory requirements.

Parts does not however model the reverse-recovery characteristics of the body diode, which could be significant in some circuit arrangements.

Parameter listings for BUZ54A and BUZ24 type power MOSFETs are given in Appendix 1.

3.3.3 GTO MODEL

PSpice, SPICE2 or HSpice have no built in models for thyristors or GTOs. It is necessary therefore, to construct from basic elements, a model which replicates the GTO action.

3.3.3.1 McEwan's GTO model

McEwan [10] devised such a model that was capable of simulating a Mullard BTV59-1000R type GTO thyristor. This model is investigated first with a view to adapting

it to model a Mullard BTW58-1300R type GTO device.

3.3.3.1.1 Model description

The model circuit is shown in Fig.3.6. RON and ROFF represent the on-state and off-state resistances respectively. IL is the GTO latching current and D3, D4, VIP and VIN monitor the magnitude and direction of the gate current. F1 is a current source whose magnitude is controlled by the current through the zero voltage sources VIP, VIN and VIK. The value of F1 is given by,

$$F1 = a(VIK) + b(VIP) - c(VIN) \quad (3.2)$$

where a, b and c are chosen in conjunction with other circuit parameters to provide the required GTO characteristics.

3.3.3.1.2 Model operation

The operation of this model hinges upon the current source F1. With no external influences IL circulates through VIK and F1, which is negative, circulates through ROFF. The voltage across ROFF ($F1 \cdot ROFF$) is the forward breakover voltage (V_{beo}) of the device.

When an anode voltage is applied, current does not flow through the model since it is blocked by the voltage across ROFF. For the GTO to switch on therefore, F1 must be made positive, which can be achieved by one of the following methods :

1. The anode voltage exceeds the forward breakover voltage. Current then starts to flow through RON, ROFF, D2 and VIK. The net current through VIK is small during this period. The positive feed-back effects from the current through VIK, reduces the current through F1 and hence the voltage across ROFF, which then allows more current to flow into the GTO. F1 becomes positive when the current entering the GTO exceeds IL. The current into the device is then diverted through RON, F1, D2 and VIK. The diode D1 provides a path for the excess current in F1 to flow.

2. Current is fed into the gate terminal. VIP measures positive gate current (flowing

into the gate) and if this is large enough, F1 can be forced positive causing the same sequence of events described in the previous method to occur, resulting in the GTO turning on.

To switch off the GTO, the current source F1 must be made negative to re-establish a blocking voltage across ROFF, which would then prevent current from flowing into the GTO. If current is extracted from the gate, VIN measures this current and a multiple of it is subtracted from the value of F1. If it is large enough, F1 becomes negative, thereby turning the GTO off in the process.

3.3.3.1.3 An appraisal of the model

Serious problems were encountered when the model was tested to ensure correct operation. PSpice uses an iterative algorithm to find the voltages at each of the nodes, at each time requested by the user during a transient analysis. The solution of the previous iteration is used as a starting point, and therefore a node voltage must not have changed too dramatically if PSpice is to converge to a new solution correctly. If PSpice initially fails to converge, then it automatically overrides the time-step specified by the user and selects a smaller one. If it still fails to converge, then PSpice will continue trying smaller and smaller time-steps until the minimum time-step is reached. If a solution cannot be computed at the minimum time-step, PSpice aborts the analysis.

When the GTO model switches on, the current through D2 rises extremely fast due to the positive feedback effects from the current through VIK. It rises so fast that PSpice cannot converge to a solution even with the minimum computed time-step, and thus the program aborts. A solution to this problem is to insert an inductor in series with D2, to slow down the rate of rise of current in the device. Unfortunately a value of at least $10\mu\text{H}$ is required, which results in an unacceptably high impedance at the frequencies at which GTOs operate at.

3.3.3.2 The two transistor thyristor model

A PNP and a NPN transistor connected back to back has been used as a thyristor model for some time now. Hu and Ki [11] developed this model for use with SPICE2 to the extent

that dynamic characteristics (e.g. rise and fall times) as well as static characteristics (e.g. breakover voltage) could be modelled. A straightforward procedure was proposed in the paper for determining the transistor model parameters from the information given on the data sheets of a thyristor. The procedure is applicable to all simulation programs that use the Gummel-Poon transistor model. Fig.3.7 shows the two transistor model. D1 and R1 have been added to the conventional two transistor model in order to accurately set the forward breakover voltage and the gate triggering current.

3.3.3.3 The two transistor GTO model

An investigation into the possibility of adopting this model to represent a GTO will be presented in this section [12]. The turn-off gain of a gate turn-off thyristor is given by [13],

$$G_{\text{gq}} = \frac{I_A}{I_G} = \frac{\alpha_2}{1 - (\alpha_1 + \alpha_2)} \quad (3.3)$$

where I_A is the anode current in the on-state, I_G the negative gate current during turn-off, α_2 the current gain of the npn transistor (Q2) and α_1 the current gain of the pnp transistor (Q1).

From the method described in Appendix 3.1, the α of each transistor for a BTW58-1300R type GTO device works out to 0.322 and 0.9 for α_1 and α_2 respectively. Therefore to turn-off a peak anode current of 25A, the gate current needed can be obtained by re-writing Eqn.3.3 as

$$I_G = \frac{I_A [1 - (\alpha_1 + \alpha_2)]}{\alpha_2} = -6.1\text{A} \quad (3.4)$$

This figure compares favourably with the figure given in the data sheets.

In determining this modelling procedure, it has been assumed that the turn-off gain remains constant during the turn-off operation (i.e. alphas remain constant). In a practical device however, the alphas are functions of current density, temperature, anode voltage and spatial distribution and a constant gate current can only be approximated [13]. Furthermore, the turn-off process involves a continuously changing current distribution within the device.

Therefore the alphas become functions of time as well. However by making α_2 as close as possible to unity and making α_1 just high enough to satisfy the on-state requirements, a high turn-off gain can be guaranteed and therefore the small variations of the alphas will have little effect on this gain [13].

3.3.3.4 The completed model

A complete procedure for extracting model parameters from the GTO data sheets is given in Appendix 3.1. The parameters BF and BR have been added to enable the user to specify the common base current gain of each transistor. A listing of the complete model is given in Appendix 3.2.

The turn-on characteristics of this GTO model are tested by incorporating the model in a resistive load circuit shown in Fig.3.8. The device switches from 250V to 5A when a current of 0.5A is passed through the gate terminal. The simulated waveforms of the gate and anode currents and the voltage across the device during the "on" period are given in Figs.3.9a,b and c.

An inductive load circuit is used to test the turn-off characteristics of the device model. The circuit used is shown in Fig.3.10. The GTO switches from a current of 5A to a voltage of 1300V when a peak reverse gate current of 3.5A is passed through the device. A snubber capacitance of 3.33nF is connected across the device to limit the rate of rise of the off-state voltage to 1.5 kV/ μ s. The simulated waveforms of the gate and anode currents and the gate and anode-cathode voltages during the "off" period are given in Figs.3.11a,b, c and d. Listings of the programs used to simulate the two circuits are given in Appendix 3.3 and 3.4.

Both these sets of results are in good agreement with the data sheet specifications, given for exactly the same operating conditions. They are summarized in Table 3.2 along with the published data. These predictions confirm that the two transistor model is equally suitable for modelling a GTO thyristor. This model is thus used to represent GTO devices in the following chapters.

3.4 CONCLUDING REMARKS

PSpice permits the design and analysis of circuits that cannot be expeditiously or economically done in any other way. It can be used to model and examine dc, small signal and transient large signal conditions. Semiconductor devices could be accurately modelled over their full range of operation using the Parts program installed in PSpice. Circuit yield can be enhanced by testing new designs using devices which simultaneously exhibit all worst-case specification parameters.

The PSpice MOSFET transistor model represents the highly non linear gate-to-drain (Miller) capacitance in the device with a constant capacitance, obtained by averaging the total variation in the capacitance over the entire operating region. It was shown that although this would result in an inaccurate modelling of the switching transients, it would not affect the switching performance of high frequency resonant circuits operating in full-wave mode and switching at zero-current significantly. The saving on the overall computation times and memory requirements when such a representation is adopted could also prove to be significant.

The PSpice program has no built in models for GTO thyristors. This disadvantage could however be overcome by building a subcircuit model that replicates the behaviour of the GTO. It was shown that such a model produced by McEwan did not permit an accurate analysis. A well established two transistor model, used to simulate SCRs was thus adopted to model the GTO behaviour. The new model enables the user to estimate the model parameters with ease by adopting a short calculation and graphical design procedure based on the manufacturer's data sheets. The procedure is applicable to all simulation programs that use the Gummel-Poon transistor model. This new model is therefore reasonably generic or "portable" between systems and implementations of PSpice, enabling designers to simulate GTO based circuits using other versions of PSpice with ease.

3.5 REFERENCES

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3.6 TABLES

Transient Period	Published Data (typical values)	Predicted Data
td (on)	20ns	27.1ns
tr	120ns	145ns
td (off)	69ns	72.5ns
tf	80ns	140ns

Table 3.1 Transient data summary for the MOSFET

Transient Period	Load Type	Published Data (typical values)	Predicted Data
td	Resistive	$< 0.25\mu\text{s}$	$.32\mu\text{s}$
tr		$< 1\mu\text{s}$	$1.06\mu\text{s}$
ts	Inductive	$< 0.5\mu\text{s}$	$.3\mu\text{s}$
tf		$< 0.25\mu\text{s}$	$.16\mu\text{s}$

Table 3.2 Transient data summary for the GTO thyristor

3.7 FIGURES

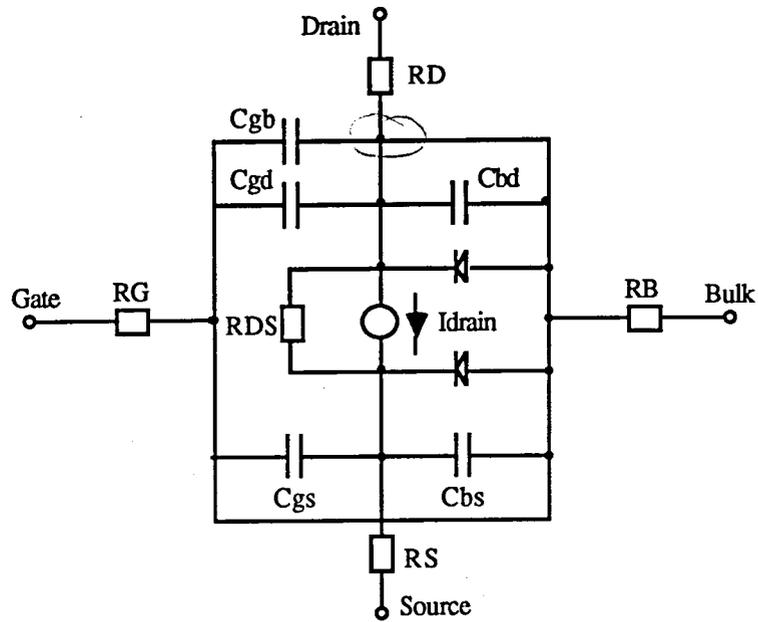


Fig.3.1 PSpice power MOSFET model

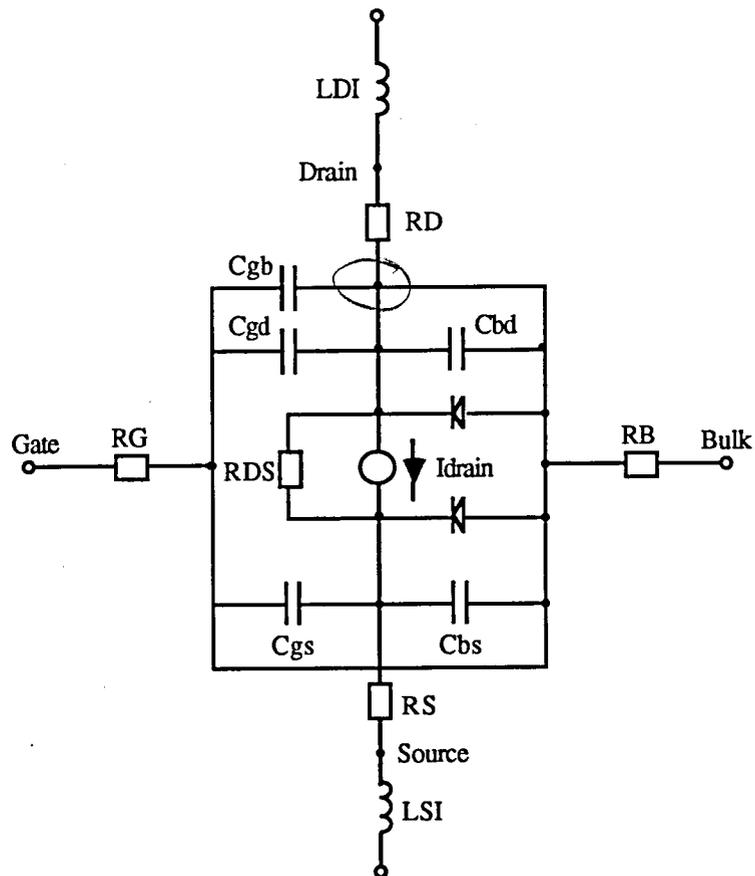


Fig.3.2 PSpice power MOSFET model with source and drain inductances

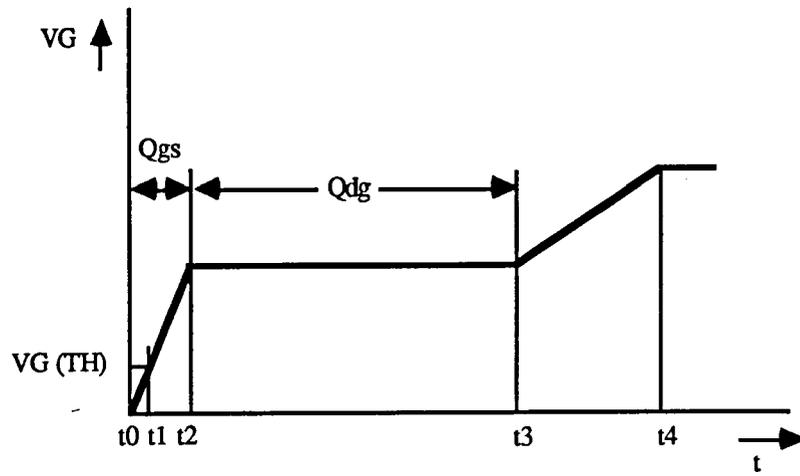


Fig.3.3 Gate charge waveform

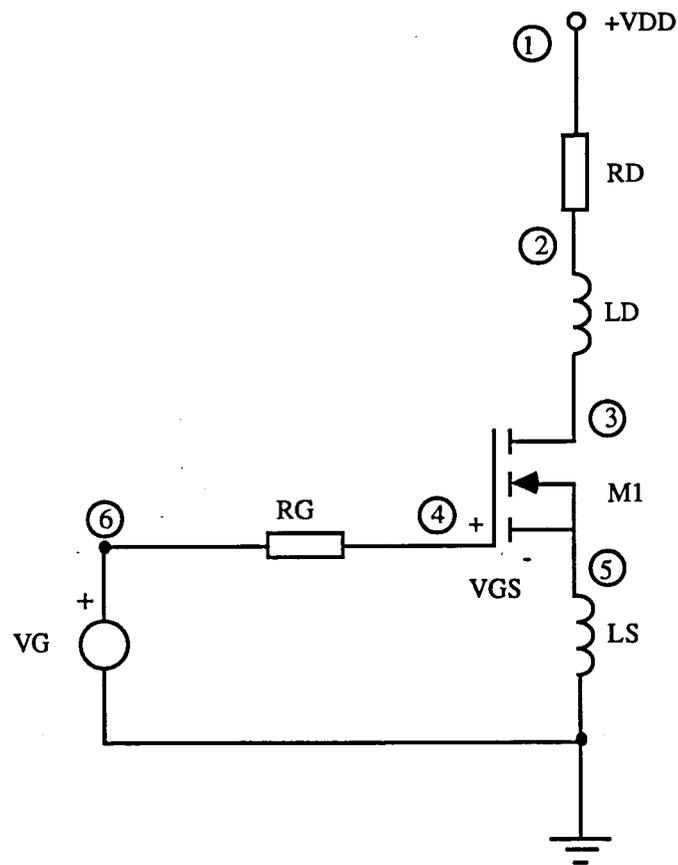


Fig.3.4 Switching time test circuit

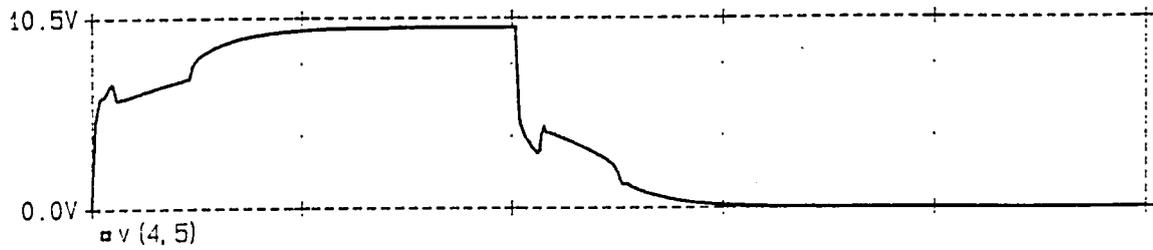


Fig.3.5a Simulated gate-source voltage waveform

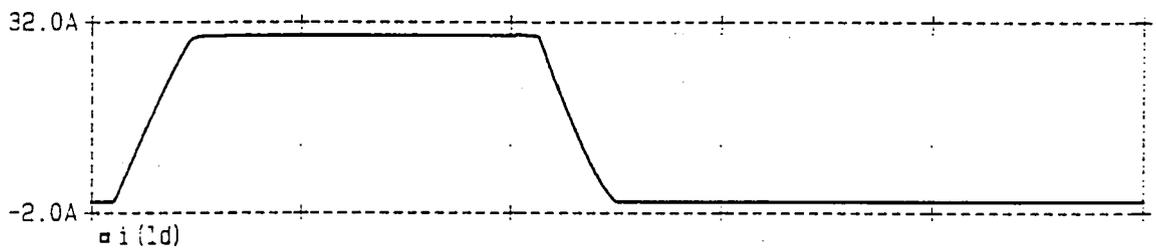


Fig.3.5b Simulated drain current waveform

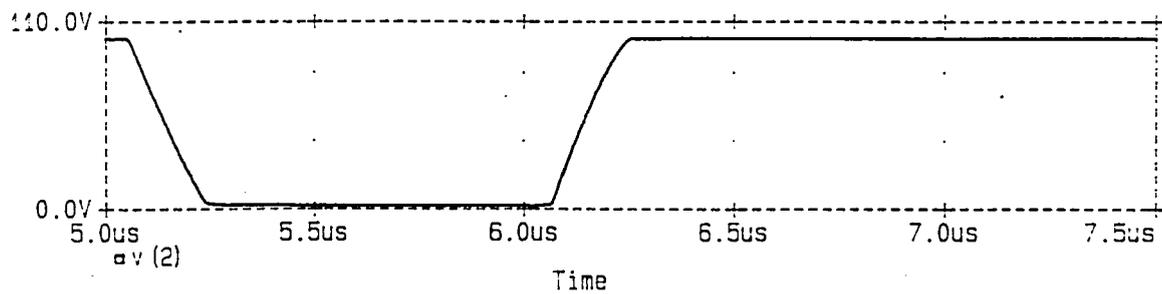


Fig.3.5c Simulated drain-source voltage waveform

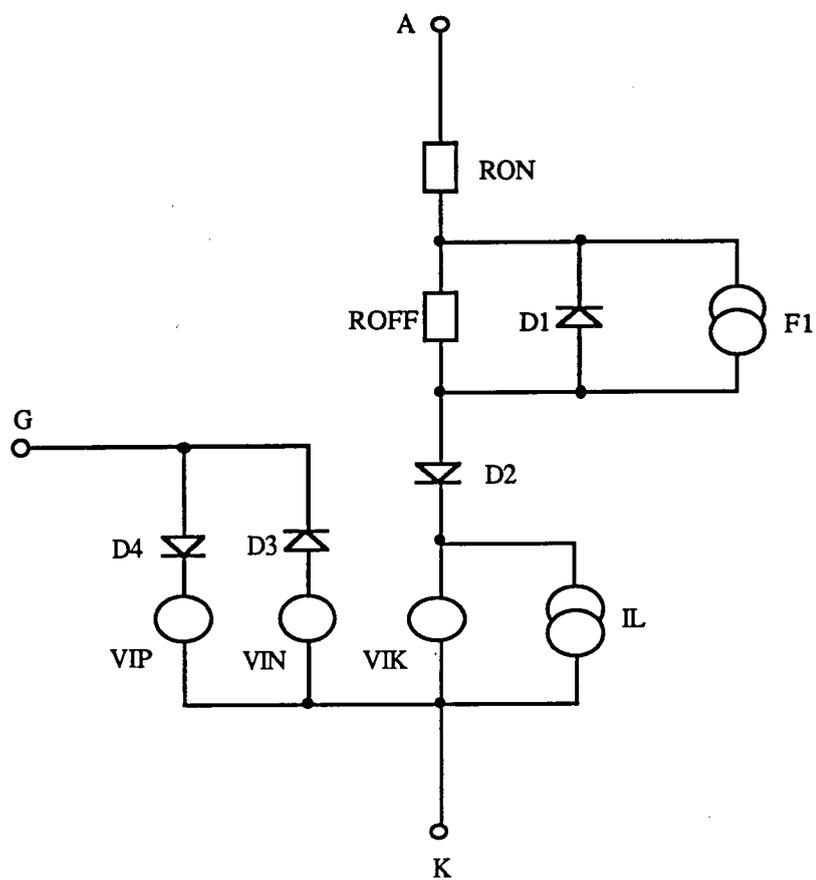


Fig.3.6 McEwan's GTO model

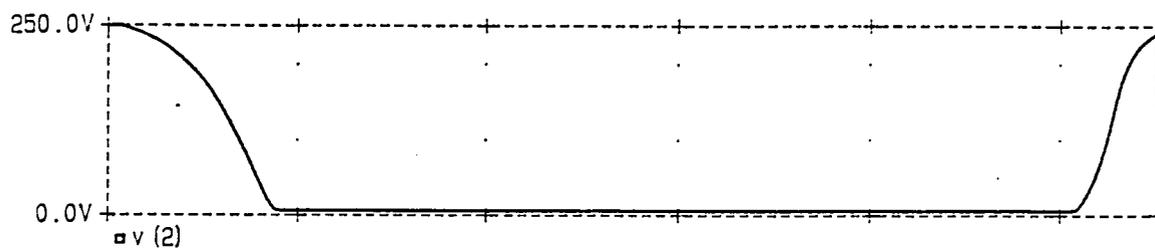


Fig.3.9a Simulated anode-cathode voltage waveform

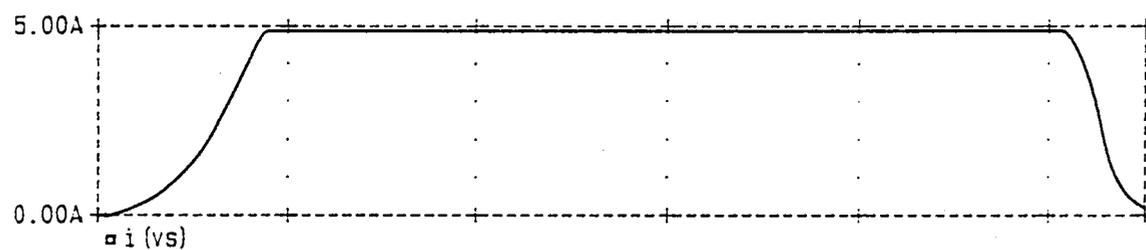


Fig.3.9b Simulated anode current waveform

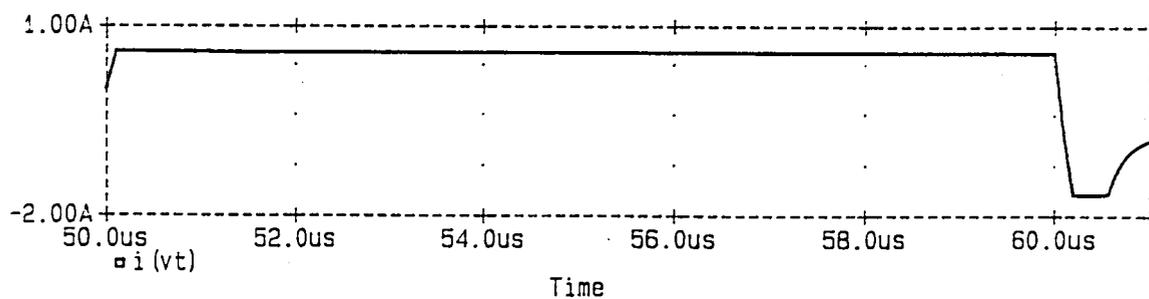


Fig.3.9c Simulated gate current waveform

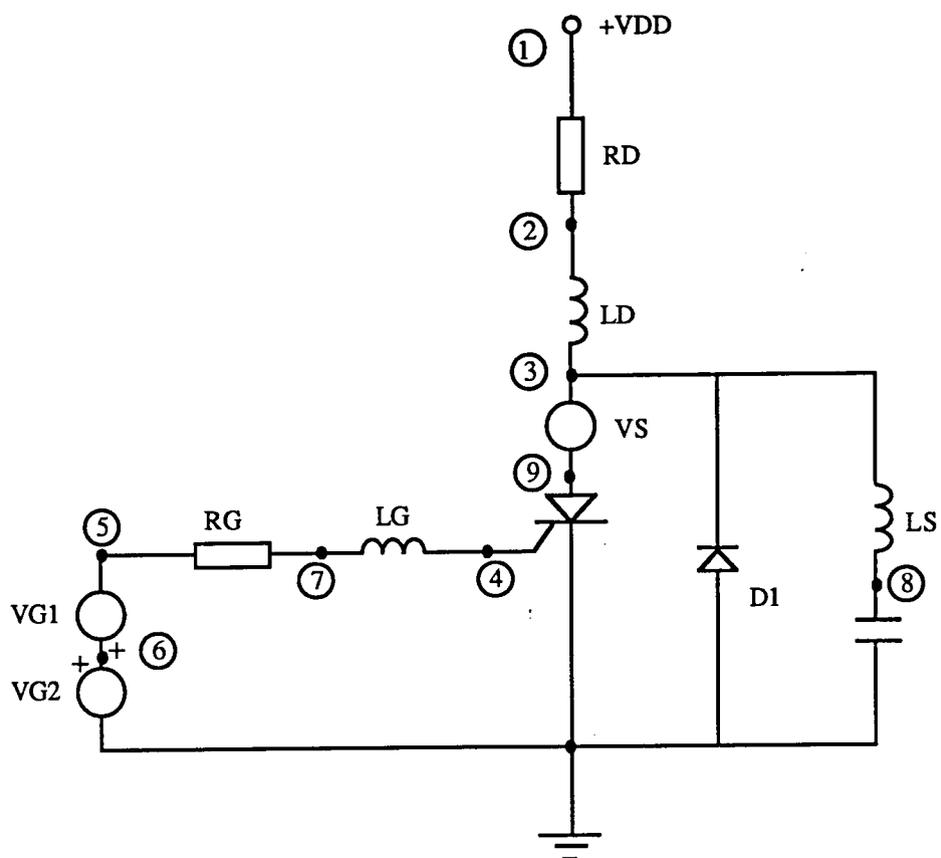


Fig.3.10 Inductive load test circuit

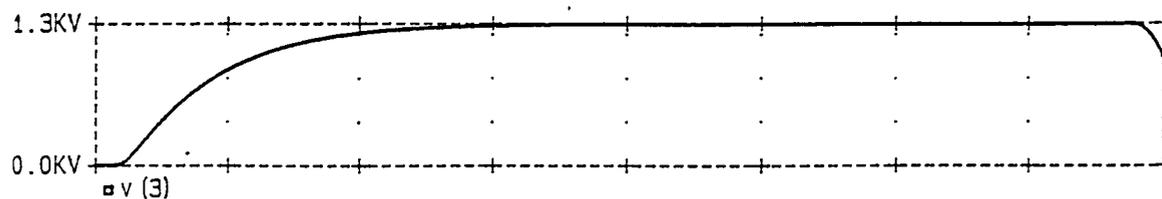


Fig.3.11a Simulated anode-cathode voltage waveform

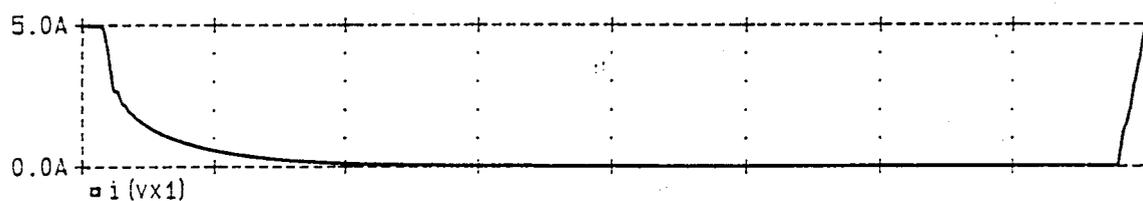


Fig.3.11b Simulated anode current waveform

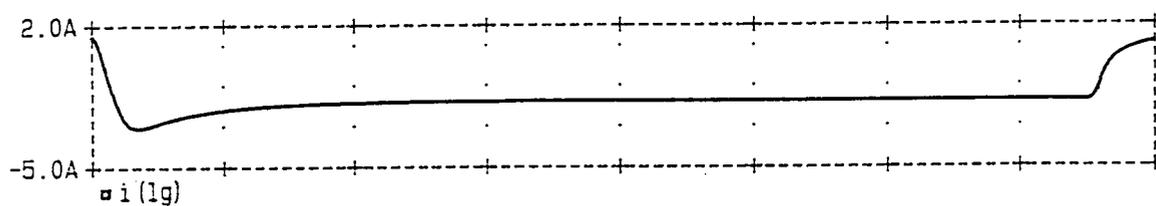


Fig.3.11c Simulated gate current waveform

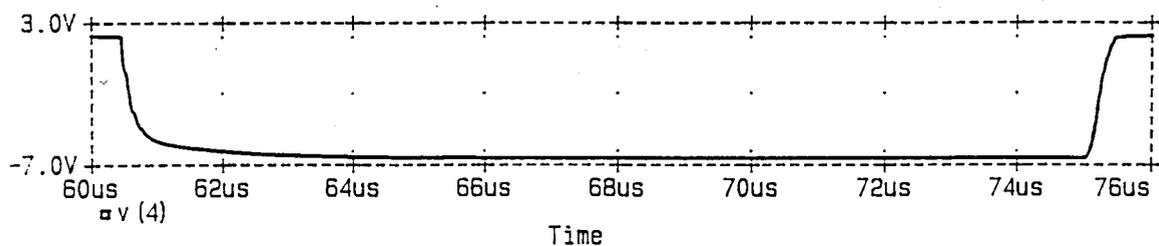


Fig.3.11d Simulated gate voltage waveform

CHAPTER 4

A RESONANCE POWER SUPPLY WITH DYNAMIC POWER FACTOR CORRECTION

A dynamic power factor corrected resonance power supply employing a single high speed GTO thyristor is introduced in this chapter. A description of the modes of operation and the analysis of the topology are included in the text.

4.1 DERIVATION OF THE TOPOLOGY

The advancement of microelectronics in recent years has prompted the development of efficient electric power conditioners that exhibit high power densities and fast transient responses. These requirements necessitate that power processing be done with high conversion frequencies.

Generally, when the conversion frequency of conventional PWM supplies nears high frequencies, their switching losses become excessive due to the simultaneous presence of a high current and a high voltage at the switch during turn-on and turn-off. However, by adding a high-frequency resonant circuit around the switch, it is possible to shape the current and voltage in such a manner that neither a high current nor a high voltage is present at the same time. Depending on how the high-frequency resonant circuit is connected to the switch, this technique could eliminate either the turn-off or the turn-on losses. The turn-off switching losses are eliminated by turning the switch off at zero current, whereas the turn-on switching losses are eliminated by turning on the switch at zero voltage.

The resonant circuit topology to be studied in this chapter, follows the principles of zero-current turn-off operation. The converter is believed to be derived from a conventional PWM boost circuit. It was first presented as a possible commercial power supply by Nijof in 1986 [1]. The presentation did not however include any clear information on the principle of operation, design procedure, method of control etc., thus necessitating the need for an extensive analysis of the converter operation [2][3].

Fig.4.1 shows the converter, where an inductor L_T and a capacitor C_T have been added to a conventional boost converter circuit to form a resonant converter. The sinusoidal current waveform generated by the waveform-shaping $L_T C_T$ resonant elements, create a zero-current condition for the switch to turn-off, thus minimizing the switching stresses and losses.

An isolated version of this circuit in which the transformer T1 also provides voltage transformation is shown in Fig.4.2. The transformer leakage inductance is used as the resonant inductor L_T . C_{b1} and C_{b2} are "dc" blocking capacitors which prevent "dc" current from flowing into the transformer. C_{b1} and C_{b2} together with C_S acts as the resonant capacitor C_T . The "on" time of the switch is determined by the resonant components of the circuit and the "off" time is varied to provide output voltage regulation against line and load changes. The circuit is completed with the output rectifying bridge B2 and the output filter

capacitor C_o .

As described in Chapter 2, a GTO thyristor is a very attractive and economical device, especially for deployment in single ended resonance circuits operating at high power levels. The high voltage and current ratings required from the switch when processing high power levels are easily met by this device. Furthermore, the very short storage time requirements of the device enables the switching frequency to be pushed to relatively high magnitudes, thus fulfilling the fundamental precondition for miniaturization.

In Fig.4.2, the switch has been represented by a high speed GTO device. A fast recovery high voltage diode connected in series with the thyristor prevents negative current from flowing, thus providing turn-off at zero current. In addition, the diode provides the required reverse voltage blocking that is needed.

Under linear operating conditions (i.e. no continuous line or load changes), with the switching frequency held constant and high relative to the rectified mains frequency, the converter circuit presents a good power factor to the mains ($>.95$). A regulated smoothed DC output voltage with a small 100Hz ripple is produced at the output, with the magnitude of the ripple being determined by the size of the output filter capacitor used. The power factor remains high for normal line and load changes. The boosting properties of the circuit enables the output voltage to be raised to levels higher than the input voltage, even with a 1:1 turns ratio of the isolation transformer. This voltage could also be stepped down by changing the transformer turns ratio. Another attractive feature of the topology is its single ended structure, enabling the processing of the output power with only a single switching element.

4.2 PRINCIPLE OF OPERATION

By replacing the transformer with its equivalent "T" model, which consists of a primary leakage inductance $L1_p$, a magnetising inductance $L2$ and a secondary leakage inductance $L1_s$, the converter circuit in Fig.4.2 could be simplified to an equivalent circuit as shown in Fig.4.3. A further approximation could be made by combining the two leakage inductances into $L1$ ($L1 = L1_p + L1_s$) as shown in Fig.4.4. In the circuit, the mains rectifier bridge has also been left out and the input voltage has been indicated by E_i .

The current through the leakage inductance $L1$ is $I1$ and the current through the inductor

L_0 , I_0 . The voltage across the "dc" voltage blocking capacitors C_{b1} and C_{b2} will be V_{b1} and V_{b2} respectively while that across C_s , V_s . The voltage across the GTO switch and the diode D1 is V_p . E_0 is the output voltage.

In order to analyse the steady-state behaviour of the circuit, the following assumptions are made, namely

1. L_2 is infinitely large. Therefore the current through L_2 is negligible.
2. $L_0 \gg L_1$
3. C_b is the combined capacitance of C_{b1} and C_{b2}
4. The output filter capacitor C_0 and the load are treated as a constant voltage source (E_0).
5. Semiconductor switches are ideal, i.e. no forward voltage drop in the on-state, no leakage current in the off-state and no time delay at both turn-on and turn-off.
6. Reactive elements of the tank circuit are ideal.

A single switching cycle can be divided into four stages of operation, namely

1. The GTO and the output rectifier bridge B2 are conducting. Both voltages V_p and V_s would have fixed values, namely 0 and $+E_0$ or $-E_0$ respectively.
2. Both the GTO and the output rectifier bridge are not conducting. The voltages V_s and V_p would vary with respect to time.
3. The GTO conducts while the output rectifier bridge is switched off. The voltage V_p now becomes zero while V_s continues to vary with respect to time.
4. The output rectifier bridge conducts but the GTO stops conducting. The

voltage V_S remains constant at $+E_O$ or $-E_O$ while the voltage V_P varies with respect to time.

Fig.4.5 shows the variations of V_P , V_S , I_O and I_1 with respect to time. The plots start at $t = T_0$ when the GTO is turned on. The output rectifier bridge has been conducting prior to the turning on of the GTO and therefore, V_S remains constant at $+E_O$. V_P drops to zero while I_1 starts to decrease again.

At time $t = T_1$, the output rectifier bridge turns off as I_1 becomes negative and therefore V_S starts to change from $+E_O$ to $-E_O$.

At time $t = T_2$, V_S reaches $-E_O$ and the bridge turns back on again. V_S remains at $-E_O$ as a result.

At time $t = T_3$, I_1 changes its direction of flow, turning the bridge off in the process. Therefore the voltage V_S starts to rise from $-E_O$ to $+E_O$.

At time $t = T_4$, I_1 exceeds I_O (i.e. $I_O + I_1 = I_{GTO}$ becomes zero), thus turning the GTO off at zero current.

At time $t = T_5$, V_S reaches $+E_O$ at which point the bridge starts to conduct.

As a result, V_S remains at $+E_O$.

At time $t = T_6$, the GTO switch is triggered back on again.

4.3 POWER CIRCUIT DESIGN ANALYSIS

In the analysis, the input voltage is assumed as being constant at the average value of the rectified line voltage E_{iav} , where E_{iav} is given by

$$E_{iav} = \frac{2E_{ipk}}{\pi} \quad (4.1)$$

E_{ipk} is the peak line voltage.

The output voltage (V_O) produced is maintained at its average value (E_O) by the large filter capacitor that is present across the load.

The expression given below for the output power has been empirically derived for steady state operation.

$$P_O = f_s C_s E_O^2 \quad (4.2)$$

This expression shows that output voltage regulation could be obtained by simply varying the switching frequency during a line cycle, to compensate for load changes that could occur during that cycle. The same criteria would apply for line changes since the output voltage depends upon the line voltage as well.

4.3.1 Determination of the resonant components

The complex nature of the circuit operation makes it difficult for a thorough analysis of the converter to be carried out. The PSpice computer programme [4] is a much simpler tool for determining the resonant components of the circuit. A flow chart describing the steps to be followed is given in Fig.4.6. The programme runs until V_O rises/falls to within 2% of the required value (E_O). The final adjustments could then be done when building the circuit.

When determining a value for C_b , it is advisable to make it to be greater than C_s so that the magnitude of V_b and therefore that of V_p is reduced.

The input inductor L_0 determines the minimum frequency of operation, f_0 in the converter circuit. If the switching frequency drops below f_0 , the converter goes into a discontinuous mode operation, at which point I_0 becomes negative and Eqn.4.2 is no longer valid. The output voltage produced will no longer be regulated. This minimum switching frequency is given by

$$f_0 = \frac{1}{2\pi\sqrt{L_T C_T}} \quad (4.3)$$

where $L_T = L_0 + L_1$

and $C_T = C_b * C_s / C_b + C_s$

Therefore,

$$L_0 = \frac{1}{C_T} \left(\frac{1}{2\pi f_o} \right)^2 - L_1 \quad (4.4)$$

The output filter capacitor is determined by the ripple requirements at the output. The pk-pk ripple voltage is given by

$$V_{\text{ripple}} = I X_c = \frac{I_{FL}}{4\pi f_m C_o} \quad (4.5)$$

where f_m is the mains frequency.

Therefore,

$$C_o = \frac{I_{FL}}{4\pi f_m V_{\text{ripple}}} \quad (4.6)$$

The capacitors C_{b1} and C_{b2} are finally determined. The magnitudes of these depend upon the levels of voltage, the total voltage across C_b , V_b must be divided by. These levels could be varied by the designer, depending upon the design requirements.

4.3.2 The input filter circuit

As stated before, when the switching frequency of the converter is held constant during a line cycle and there is no saturation in L_0 , I_0 is essentially modulated in phase with the input voltage. The power factor would thus approach unity if the system was to operate under linear conditions, with the switching frequency remaining high relative to the rectified line frequency.

However, such an operation as it stands, would cause the switched input current to contain a high level of switching frequency ripple. The elimination or reduction of this ripple to acceptable levels would therefore necessitate additional filtering, which could be

implemented with a simple LC filter circuit, connected at the input of the converter as shown in Fig.4.7.

4.4 LOW OUTPUT VOLTAGE APPLICATIONS

The magnitudes of the capacitors C_{b2} and C_S in a practical circuit are also governed by the step-up or step-down ratios of the isolation transformer. For a step-down ratio of $n_p/n_s = n$, the capacitance increases by n^2 times the value obtained from the design. Therefore, for low output voltage applications, especially at high output power levels, these capacitances reach high magnitudes at high currents, resulting in the cost involved rising.

The capacitor C_{b2} could however be removed from the circuit altogether. The unavoidable "dc" flux in the isolation transformer can be dealt with by introducing an air gap. However, when doing so, it must be ensured that L_2 remains high, so that the normal modes of operation of the circuit are not affected.

4.5 THE RESONANT POWER SUPPLY WITH A SINGLE OUTPUT DIODE RECTIFIER

The resonant power supply could be simplified further by removing the output rectifying bridge B2 [1]. The resulting circuit, which would comprise of only the primary side "dc" voltage blocking capacitor C_{b1} , the capacitor C_S and a single diode rectifier, would be simple, cheap and therefore more attractive. Such a converter circuit would also give rise to the possibility of producing multiple output voltages, as required for example by TV receivers.

There are two ways of connecting a rectifier diode to the secondary winding, namely

1. The "forward voltage rectifier" mode, where the output rectifier diode D2 conducts during the "on" period of the switch. The corresponding converter circuit is shown in Fig.4.8.

2. The "flyback voltage rectifier" mode, where the output rectifier diode D2 conducts mainly during the "off" period of the switch. The circuit depicting this operation is shown

in Fig.4.9.

These two circuit configurations, although being simple and inexpensive, would give rise to a major disadvantage in the form of a higher imposed voltage on the switching devices. The circuit in Fig.4.8 causes the positive voltage on D1 and the GTO device to increase considerably, while the circuit in Fig.4.9 causes the negative voltage on D1 and the GTO to rise.

This phenomenon can be explained with the aid of the voltage waveform V_S , shown in Fig.4.5. The "full wave" rectifier circuit clips V_S at both the positive and negative periods to the output voltage E_O . In the forward voltage rectifier mode, the negative voltage period of V_S is clipped at E_O . The positive voltage period of V_S changes from a trapezoidal shape to a half sine wave shape with a higher peak amplitude. In the flyback voltage rectifier mode, the positive voltage period of V_S is clipped to E_O . Therefore the negative voltage period gets a half sine wave shape and consequently a higher amplitude. The net result of this is therefore a higher voltage stress on the GTO thyristor or the series diode D1.

4.6 CONCLUDING REMARKS

The new resonant converter topology with dynamic power factor correction is a suitable supply for mains fed applications. It can present a near resistive load to the mains while maintaining a mains isolated dc output voltage with a low 100Hz mains frequency ripple. The employment of the GTO device in a "circuit commutated mode" (as a fast thyristor), provides an efficient and reliable method of processing high output power levels at high frequencies.

Applications requiring less accurately stabilised dc voltages can be directly served by the converter with ease. For electronic equipment requiring more accurately stabilised output voltages, the converter can be used as a "pre-conditioning" power supply. For these applications, the converter could deliver a "stabilised" dc output voltage, with the final ripple reduction taking place via simple dc-dc converters.

4.7 REFERENCES

1. Nijhof, E.B.G., 1986, "Resonant power supply (RPS) converters. The solution for mains/line pollution problems" , Proc. Power Conversion International Conf., 104-139.
2. Amarasinghe, K.A. and Manning, C.D., 1990, "A resonance power supply that provides dynamic power factor correction in capacitor input off-line converters", Proc. I.E.E.E Applied Power Electronics Conf., 563-570.
3. Amarasinghe, K.A. and Manning, C.D., 1990, "A dynamic power factor corrected resonance power supply", to be presented at the I.E.E Power Electronics and Variable Speed Drives Conf., London.
4. PSpice, Microsim Corporation, 23175 La Cadena Drive, Laguna Hills, CA 92653, USA.

4.8 FIGURES

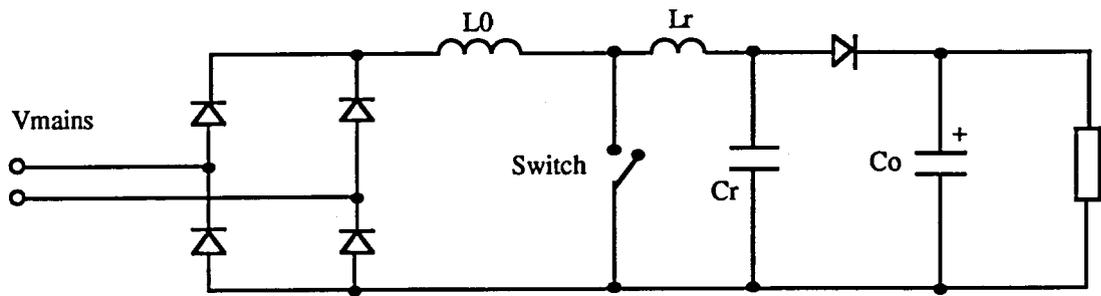


Fig.4.1 A boost resonant converter

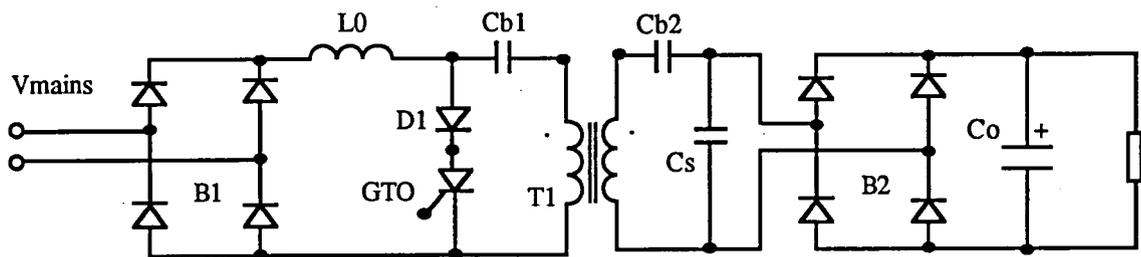


Fig.4.2 A modified version of the boost resonant converter

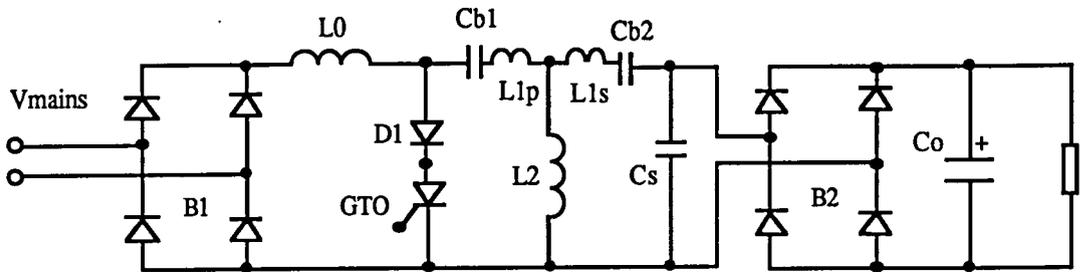


Fig.4.3 Equivalent circuit of the resonant converter

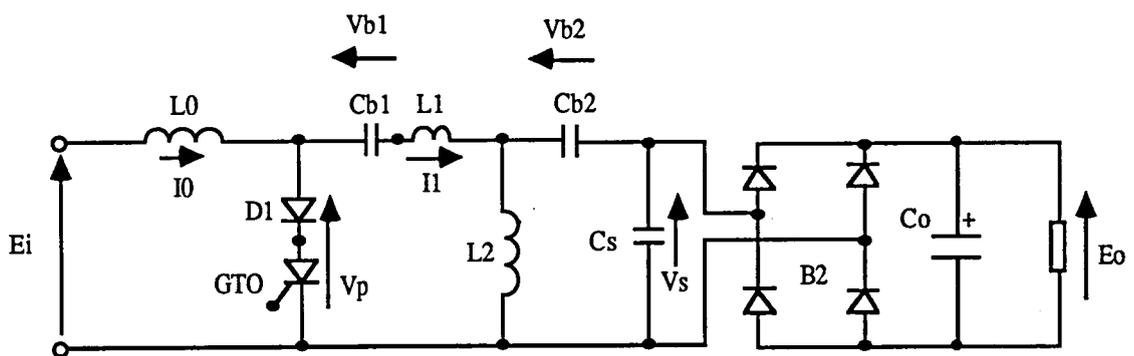


Fig.4.4 A simplified equivalent circuit

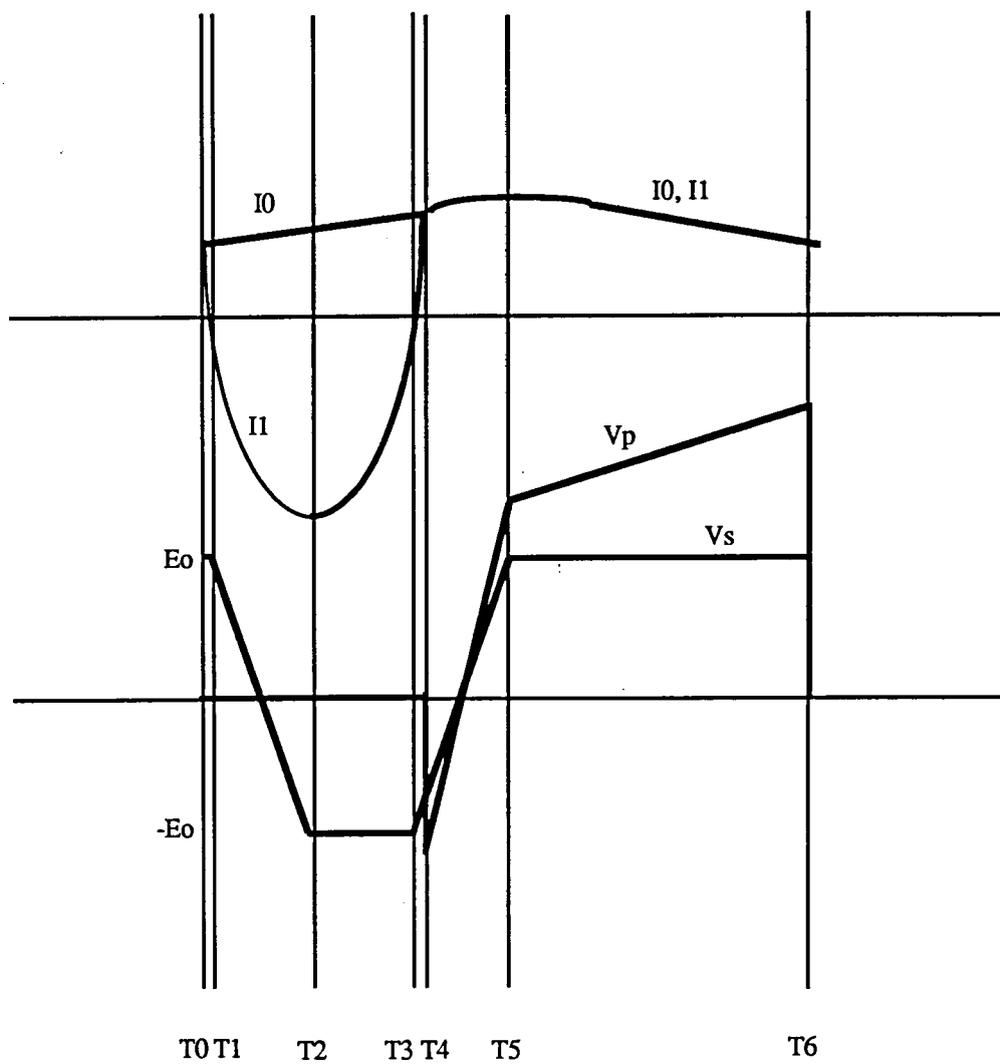


Fig.4.5 Voltage and current variations over one switching cycle

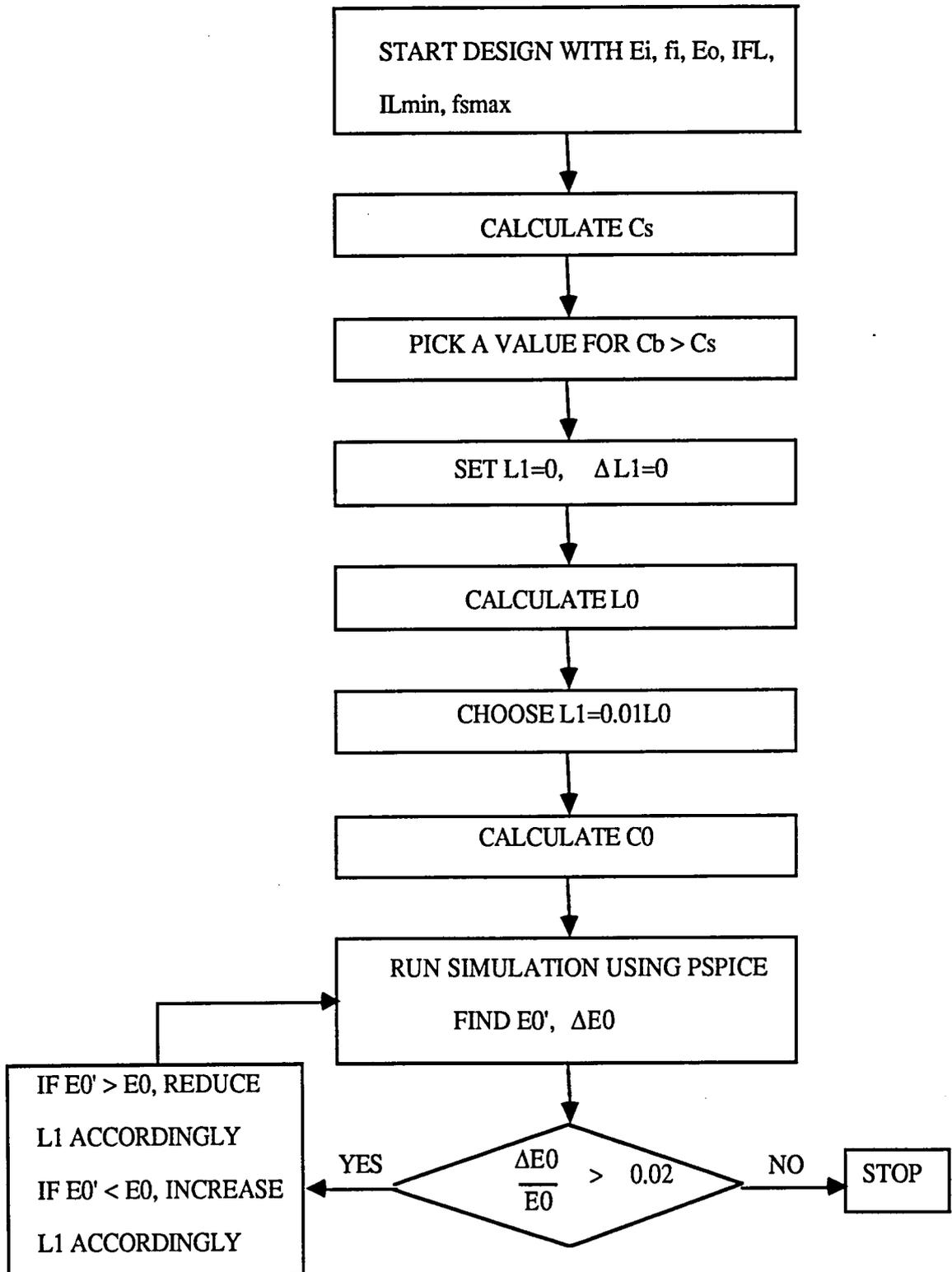


Fig.4.6 Design procedure

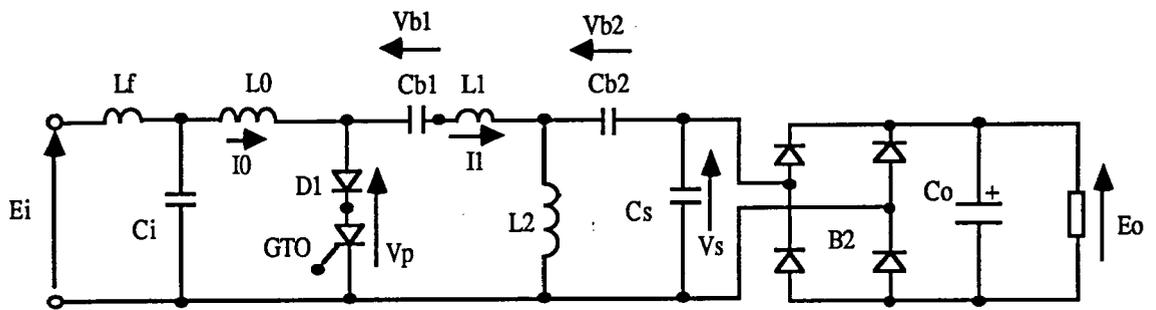


Fig4.7 The resonant converter with an input filter

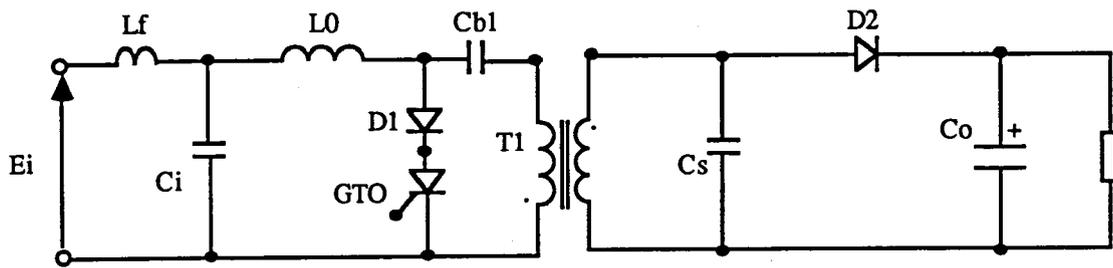


Fig.4.8 The resonant converter with forward rectified output voltage

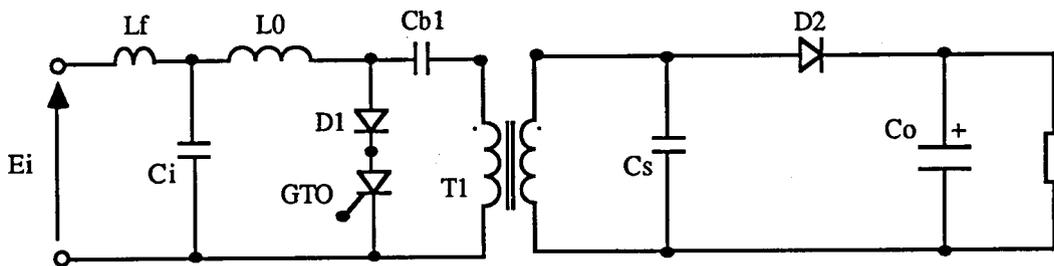


Fig.4.9 The resonant converter with flyback rectified output voltage

CHAPTER 5

A 300W PROTOTYPE CIRCUIT

The design of a 300W, 80kHz prototype model of the resonance converter described in Chapter 4, is presented in this chapter. The design of the isolation transformer and other magnetic components are described in detail. The selection of circuit components and the design and implementation of the variable frequency control loop are also discussed. The chapter is concluded with an evaluation of the computer simulated and experimental results, obtained from the prototype circuit.

5.1 DESIGNING THE CONVERTER

The design is first carried out for the transformerless resonant converter shown in Fig.5.1. L_2 is neglected in the calculations.

The input/output requirements are as follows,

Input voltage	: Single phase 240Vac, 50Hz
Output voltage	: 450±0.7Vdc at 0.19A-0.66A
Output power range	: 88W-300W
Maximum switching freq.	: 80kHz

After full-wave rectification, the steady state input voltage will vary from a minimum of zero to a peak of 340 V. The 450V output voltage produced will be stepped down to 250V at 1.2A on full load. This would mean a step-down ratio of $450/250 = 1.8$. The capacitors C_{b2} , C_s and C_o would therefore be $(1.8)^2$ times the designed values in the practical circuit.

Assuming a loss-less operation, the capacitor C_s needed to meet the input/output requirements stated above can be obtained by rewriting Eqn.4.2 in Chapter 4 as

$$C_s = \frac{P_o}{f_s E_o^2} = 18.52\text{nF} \quad (5.1)$$

For a C_b/C_s ratio of 4.66,

$$C_b = 4.66 C_s = 86.315\text{nF} \quad (5.2)$$

For a minimum output power of 88W, the minimum frequency of operation, f_o is given by

$$(P_o)_{\min} = C_s f_o E_o^2 = 88\text{W} \quad (5.3)$$

Therefore,

$$f_o = 23.5\text{kHz} \quad (5.4)$$

By substituting for f_o in Eqn.4.4 and neglecting L_1 , the required value for L_0 is obtained.

$$L_0 = \frac{1}{C_T} \left(\frac{1}{2\pi f_o} \right)^2 = 3\text{mH} \quad (5.5)$$

For an output voltage ripple requirement of 1.37V, the output filter capacitance is given by

$$C_o = \frac{I_{FL}}{4\pi f_m V_{\text{ripple}}} = 772\mu\text{F} \quad (5.6)$$

where f_m is the mains frequency.

To limit the peak to peak voltages across the capacitors C_{b1} and C_{b2} to 125V and 170V respectively, the following values are given to the two capacitors, namely

$$C_{b1} = 200\text{nF}$$

$$C_{b2} = 151.85\text{nF}$$

As stated before, the magnitude of L_1 should be such that it provides a sufficient "on" time to the switch to obtain 300W at 250Vdc at the output, when the input voltage is at its average value, E_{iav} . Computer simulation of the circuit has shown that a value of 37.6 μ H, provides a sufficient "on" time for obtaining the required output conditions at the average input voltage.

The filter capacitance selection is also dominated to a large extent by the ESR (equivalent series resistance) necessary to obtain an acceptable pk-pk ripple voltage.

$$\text{ESR} = \frac{V_{\text{ripple}}}{I_{\text{pk}}} \quad (5.7)$$

Simulated results of the 300W converter shows that $I_{\text{pk}}=15\text{A}$. Therefore, the chosen capacitor should have an ESR of less than $1.37/15 = 91.3\text{m}\Omega$ at 80kHz to satisfy this requirement.

Computer simulation has also shown that input filter components of 1.5mH and 1 μ F,

reduce the magnitude of the switching frequency ripple in the line current to acceptable levels.

5.2 TRANSFORMER DESIGN

An ideal ac transformer should transfer most of its input power instantaneously to the output, while storing only a small portion in its magnetising inductance. Consequently, its size will be smaller than other magnetic components, such as inductors or flyback transformers which provide energy storage facilities as well. This is however true, only if the full core flux swing from the negative to the positive saturation limits is permitted as shown in Fig.5.2 [1]. Core losses at low flux densities (no saturation) is made up of hysteresis, residual and eddy current losses [2]. As the frequency of the excitation current is increased from 20kHz through 100kHz to the MHz region, the major core loss limitation sets in, which imposes substantial derating of the allowable core flux swing as seen in Fig.5.3. For example, the energy loss per single cycle and unit volume of magnetic material is directly proportional to the area of the BH loop, hence proportional to the square of the peak flux density. Each time the direction of the excitation current is changed, the external energy is utilized to reorient microscopic magnetic domains, thereby producing this hysteresis loss. Consequently, the hysteresis losses increase with switching frequency [1]. In addition to this, eddy current and residual losses also become very significant at high switching frequencies [2].

The net result of all this is, that with the increase in switching frequency, the absolute amount of core losses for full flux excursions from negative to positive saturation levels is excessive and results in unacceptably high temperature rises due to the inability of the core, with its small surface, to get rid of excessive heat. Therefore, although the flux saturation level would allow much smaller core sizes to be utilized such as, for example, the one shown in Fig.5.2, the excessive core losses force the designer to "derate" the available flux density levels well below the peak saturation levels possible, by using proportionally larger cores, such as, for example, the one shown in Fig.5.3.

The solution to this problem is to use a different ferrite material which could operate with low losses at relatively high flux densities and high frequencies. The main difference between these newly developed materials and the previously existing ones is the method of core loss variation with respect to frequency. Experiments carried out by Buethker and Harper at the Philips Research Laboratories [3], have shown that at 100kHz operation, the standard Philips 3C8 type ferrite material exhibits excessive hysteresis losses. To overcome

this disadvantage, they have introduced a new ferrite material called 3C85. By doing so, they have been able to reduce considerably, the dominance of the hysteresis losses at that particular frequency and flux level. These new type of ferrite cores are therefore used in the prototype circuit.

Yet another undesirable effect which sets in at high frequencies and limits transformer design are conduction losses which arise due to skin effect. Skin effect is a tendency of the high frequency currents to concentrate on the surface of the conductor. The higher the frequency, the shallower is the depth to which current penetrates. For copper, the skin depth can be obtained from the following equation [2],

$$\delta = \frac{0.066}{\sqrt{f_s}} \text{ m} \quad (5.8)$$

where δ is in meters and f_s , the switching frequency in hertz. For 80kHz operation, $\delta = 0.23\text{mm}$, which means that any copper wire with a higher radius is essentially being wasted.

The transformer design procedure given in the Unitrode Design Manual [4], was followed when designing the magnetic components. The filter inductor L_f is made up of three strands of 0.45mm diameter enamelled copper wire. The wire is twisted together and wound on to an ETD 49 type core. 80 turns are wound on to the former and an air gap of 1.13mm is introduced to keep the core from saturating (the peak working flux density is .3T). The inductor L_0 is made in a similar manner to L_f , again with three strands of 0.45mm twisted wire. In this case, 133 turns are wound on an ETD 49 type core, and an airgap of 1.6mm is introduced.

The transformer is wound using 0.45mm wire, with 2 strands on the primary and 3 on the secondary. Again, an ETD 49 type core is used with 72 turns on the primary and 40 turns on the secondary. The leakage inductance of the transformer could be measured by finding the short circuit input impedance at each winding and then solving for the individual inductances. These leakage inductances are independent of the core characteristics. The leakage inductance in this case is increased to the required 37.6 μH when referred to the primary side by using an additional air cored inductor (.8 μH) in series with the secondary winding. The air cored inductor is made up of a few turns of twisted copper wire.

5.3 POWER CIRCUIT CONSTRUCTION

A complete schematic representation of the power stage is shown in Fig.5.4. The series and output rectifying diodes are ultra fast-recovery types with very small reverse recovery times. The input filter and the resonant capacitors are made up of metallized polypropylene type capacitors. The output filter capacitor is a 2500 μ F electrolytic. A RC snubber circuit is added across the GTO and D1 to reduce voltage overshoots and ringing due to the reverse recovery effects of D1. Without the snubber circuit, large voltage overshoots and ringing could be observed across these devices. Ringing occurs between the transformer leakage and parasitic inductances present in the circuit and the diode capacitance. This "snap" reverse recovery phenomenon is explained in more detail in the following chapter.

Interconnections between the components are made with copper strips, 0.45mm thick. The reason for using such copper strips in preference to ordinary copper wire is due the disadvantages associated with skin effect losses.

In order to simplify the ground connections, two aluminium ground plates are used. The two ground plates are isolated from each other. The ground planes are positioned so as to minimise the length of all the connections made to them, thereby helping to reduce the conduction losses.

The following protection devices are also used in the power circuit. The GTO thyristor is protected by one BZW03-C91 type zener diode and 3, BZW03-C360 type zener diodes connected in series across the device. The zener diodes clamp the forward voltage across the GTO to a maximum of 1171V. In order to protect the reverse voltage blocking diode D1, a similar arrangement is used. The reverse voltage across the diode is clamped to a maximum of 902V. 2, BZW03-C360 and 2, BZW03-C91 type zener diodes are used with a BYW96E type diode in series with them, but connected in the opposite direction. The additional diode prevents the zeners from conducting when forward biased.

5.4 CONTROL LOOP DESIGN

To ensure zero-current switching, the GTO thyristor must be turned off during the time the series diode D1 blocks the reverse voltage. Since this time is set by the resonant tank circuit and does not change, constant on-time control is required. With the on-time fixed, the switching frequency must be varied to control the output voltage.

A straight forward implementation of the control circuit using common integrated circuits is shown in Fig.5.5. The 74HCT4046 is the voltage to frequency converter. The 74HCT123 monostable is used to set the on-time of the switch. The gate drive circuit is isolated from the control circuit with a high frequency pulse transformer.

5.4.1 Gate drive circuit

Fig.5.6 shows a straight forward implementation of the gate drive circuitry, using common integrated circuits. The Hex inverting schmitt is used to sharpen the rising and falling edges of the output pulses from the comparator.

"Turn on" of the GTO is achieved as follows. When the output of the comparator swings to $+V_d$, a current flows into the base of the npn transistor T_{r3} , thus turning it on. This in turn provides a current to trigger the GTO on. The R3,C3 series combination placed across R4 helps to provide a high initial turn-on current. "Switching off" of the GTO is achieved in a similar manner. When the output from the comparator changes state, T_{r3} turns off and the pnp transistor T_{r4} turns on. The voltage at the gate of the GTO then changes its state to $-V_d$, enabling the circuit to draw out a current from the gate terminal of the device, and thus provide fast turn-off.

5.4.2 Current limiting circuit

In order to protect the active devices in the circuit, a current limiting circuit is incorporated into the control circuit. The circuit continuously monitors the peak current into the GTO thyristor and if it exceeds a certain preset threshold level, it implements shutdown by pulling the input to the 74HCT123 monostable to ground, thereby nullifying the effects of the gate drive pulses.

A straightforward implementation of the current limiting circuit using common integrated circuits is shown in Fig.5.7. The peak current through the GTO device is monitored by the current transformer T3. A Siemens N30 type ferrite toroidal core, with a 100:1 turns ratio is used for this purpose. The toroidal core is placed around the conductor feeding the GTO thyristor and the reverse blocking diode. This conductor forms the primary winding of the current transformer. The current in the secondary winding of the transformer will therefore be one hundredth that through the GTO. The voltage across the resistor R5 is therefore proportional to the current flowing through the GTO device.

When the output from the CA311E comparator changes state, the CA555 timer turns on for 1 second, during which time the output pulses from the control circuit are pulled to ground. The GTO thyristor does not turn-on during this period. At the end of this time the power supply turns on again and if the short circuit persists, the supply enters into a hiccup mode.

5.4.3 Closed-loop control circuit

Closed-loop control is obtained by feeding the output voltage into a uA723C type error amplifier which then provides the required control voltage to the voltage to frequency converter. The gain and phase plots of the open loop system, obtained by using a transfer function analyser is shown in Fig.5.8.

As described previously, with a bulk filter capacitor of acceptable cost and size, there will be a 100Hz ripple on the output voltage. This gives rise to a 100Hz control voltage component at the error amplifier output, which will oppose and reduce the ripple on the output voltage, depending upon the control loop gain at 100Hz. While this ripple reduction is a laudable goal, the 100Hz control voltage component will distort the line current waveform by causing the switching frequency to vary. This can make it impossible to achieve the desired power factor.

To prevent this distortion, the control voltage must not be allowed to change significantly during each line half-cycle. The control loop bandwidth must therefore be less than a 100Hz to keep the line current waveform distortion to an acceptable level.

Closed-loop control is provided with the network shown in Fig.5.9. The circuit shifts the dc gain by 10dB $\{=20\log(R5/R4)\}$, which provides a bandwidth of approximately 15Hz, thus ensuring a high input power factor. Although the large output capacitance will restrict the loop transient response, it cannot be considered as a major disadvantage since the capacitor allows only a small change in the output voltage for a relatively large change in the load current.

The power stage is isolated from the control stage with a HP6N135 type opto-coupler as shown in Fig.5.9.

5.5 COMPUTER SIMULATION

The PSpice computer simulation program is used to analyse the 300W prototype converter circuit. The GTO thyristor is represented by the model described in Chapter 3. The diodes present in the circuit are represented by their equivalent circuit device models, which were produced by using the Parts program (see Chapter 3). A complete equivalent circuit representation of the prototype circuit is given in Fig.5.10.

The usual method of simulating a transformer using PSpice is to specify the open circuit inductance seen at each winding and then add coupling coefficients. This technique however, tends to lose the physical meaning associated with the leakage and magnetising inductance of the transformer. Furthermore, when using transient analysis to model converter operation, the iteration procedure frequently fails to converge to a solution or gives meaningless results [5].

In order to make a transformer model that more closely represents the physical process therefore, it is necessary to construct an ideal transformer model and model the magnetising and leakage inductances separately. The ideal transformer will have a unity coupling coefficient and an infinite magnetising inductance. It will therefore preserve the voltage/current relationship shown in Fig.5.11. A supplementary equivalent circuit of the model is shown in Fig.5.12. C_{1p} and C_{1s} represent the primary and secondary winding self capacitances. The interwinding stray capacitance has been ignored in the representation. L_{1p} and L_{1s} are the primary and secondary winding leakage inductances. R_{1p} and R_{1s} are the primary and secondary winding resistances. L_m is the magnetising inductance. R_m represents the hysteresis losses in the core and n is the transformer turns ratio. This representation could be simplified further as shown in Fig.5.13. The leakage and magnetising inductances L_1 and L_m are measured by finding the short and open circuit input inductances respectively. The winding resistance R_1 could also be found by measuring the input resistance with the output terminals short circuited. C_1 is the total winding self capacitance. It is found by measuring C_{1p} and C_{1s} separately and adding them together.

The 300W isolation transformer has the following leakage and magnetising inductances, winding self capacitance and winding and hysteresis loss resistance values,

$$L_1 = 37.6\mu\text{H}$$

$$L_m = 16.5\text{mH}$$

$$C1 = 50.415\text{pF}$$

$$R1 = 0.875\Omega$$

$$R_m = 0.11\text{M}\Omega$$

Both the input filter and input inductor L_0 have winding resistances of 0.23Ω and 0.4Ω respectively. Their winding self capacitances are 41.035pF and 33.384pF respectively. The output filter capacitance has an equivalent series resistance, ESR of 1.55Ω at a 100Hz (this is when referred to the primary side). The ESR of the resonance capacitors is negligible.

Fig.5.14 shows the predicted voltage and current waveforms when the input voltage is at 216.45V (average value). These predictions are in good agreement with the experimental results presented in the following section, thus confirming the accuracy of the computer model.

A listing of the program used is given in Appendix 4.

5.6 EVALUATION OF THE POWER STAGE PERFORMANCE DATA

Figs.5.15 through to 5.19 show the voltage and current waveforms of the various circuit components. The effect of the superimposed 100Hz ripple voltage could be seen clearly on the waveforms of the power circuit components. The input current and voltage are seen to be in phase with each other. The switching frequency ripple is not present on these waveforms due to the filtering of the 80kHz component by the input filter circuit.

Fig.5.18 clearly shows the GTO turning off at zero-current. Furthermore, the voltage that appears across the switching devices starts off being negative, thus providing sufficient time for the GTO thyristor to recover. This permits the GTO to be switched at relatively high frequencies.

The converter has a full load efficiency of 81% and performed satisfactorily at various input voltage and load levels. Efficiency was calculated by dividing the product of E_o and I_o by the input power, P_i . E_o , I_o , E_i and I_i were all measured with 8010A type digital multimeters. P_i was measured with a EW604 type Feedback electronic wattmeter. Figs.5.20 and 5.21 show the variation of the switching frequency and efficiency with respect to the load current. The switching frequency data shows good correlation between the theoretical and experimental results. The slight deviation is caused by losses in the tank

circuit. In Fig.5.21, the efficiency tends to suffer when lightly loaded due to the relatively high conduction losses caused by the resonant current.

Fig.5.22 shows the variation of the input power factor with respect to the load current. On full load, the power factor is measured at 0.953. Although theoretically this power factor should be unity, in practise some distortion in the line current waveform does occur as shown in Fig.5.15, thereby holding the power factor down to such a value. This is believed to be due to the nature of the circuit operation, where the input voltage cannot be boosted up to the required output voltage, once it drops below a certain level. No line current is drawn during this period. The power factor however rises to 0.994 at 1/3 the rated load, since the switching frequency is much lower at this particular load, permitting a lower duty ratio and thus a lower input voltage from which boosting could start to take place.

A frequency spectrum of the input current waveform is shown in Fig.5.23. The measurements were taken under full load conditions (300W), with a Tektronix A6302 type current probe, a AM503 type current probe amplifier and a HP 3582A type spectrum analyzer. The even harmonics present are negligible. The odd harmonics when expressed as a percentage of the 50Hz fundamental frequency are as follows, namely

Fundamental	-	100%
3 rd Harmonic	-	16.4%
5 th Harmonic	-	10.6%
7 th Harmonic	-	4.88%
9 th Harmonic	-	2.16%
11 th Harmonic and beyond	-	less than 1%

The odd harmonics present could be reduced further if needed by increasing the filter inductance, L_f .

5.7 CONCLUDING REMARKS

As stated before, sinusoidal input current is obtained in the resonant circuit by simply operating the converter at a constant switching frequency, such that the short term average current naturally becomes proportional to the rectified input voltage. The frequency is then adjusted over several line cycles to achieve long term regulation of the output storage capacitor voltage. This approach however, produces some distortion in the input current

waveform, due to the nature of the circuit operation.

Most applications do not mind this level of distortion since the input power factor is still very high. If however an input current waveform with less distortion is needed, a more advanced version of this control technique would have to be implemented. Such a technique is proposed in Chapter 8.

5.8 REFERENCES

1. Cuk, S., Zhang, Z. and Kajouke, L.A., 1988, "Low profile, 50W/in³, 500kHz integrated - magnetics PWM Cuk converter", Proc. High Frequency Power Conversion Conf., 442-463.
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5.9 FIGURES

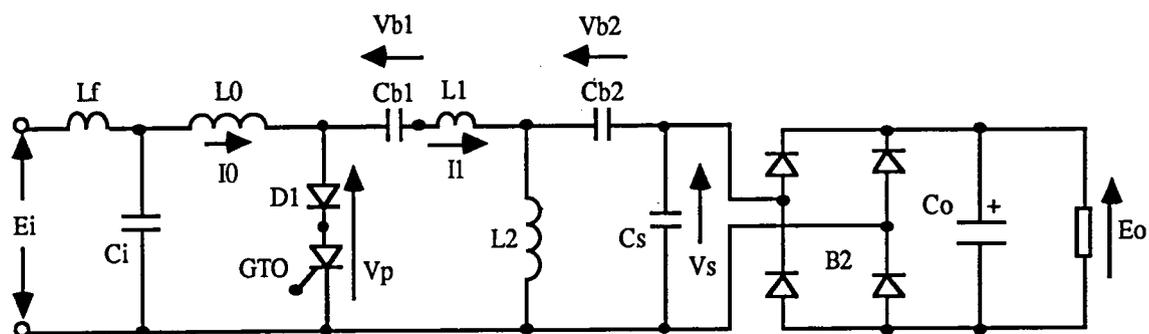


Fig.5.1 A simplified equivalent circuit of the resonant converter

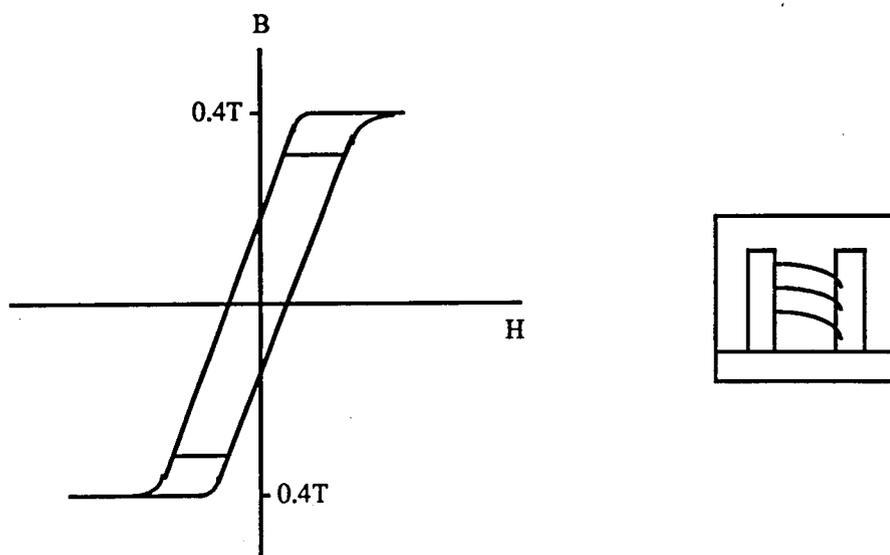


Fig.5.2 A transformer operating with a full flux swing

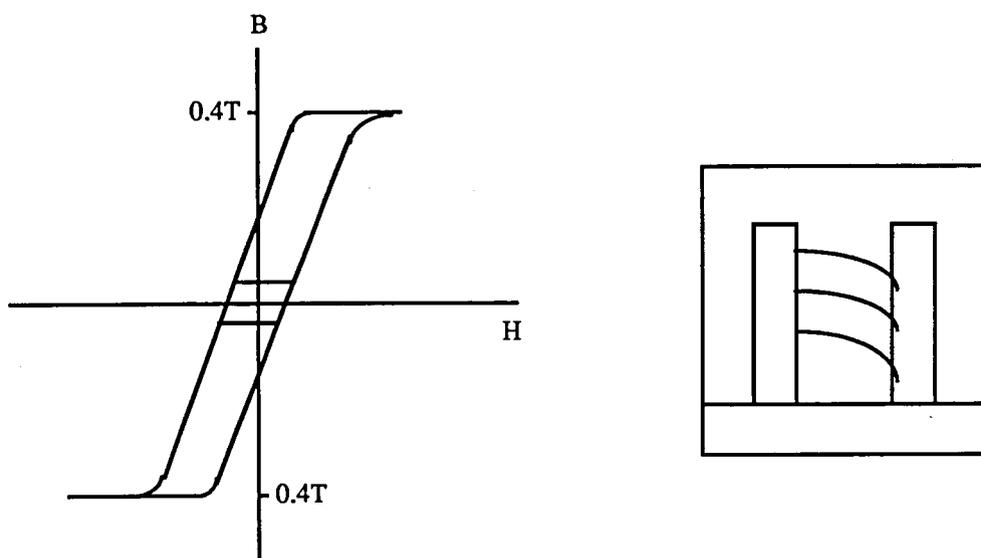
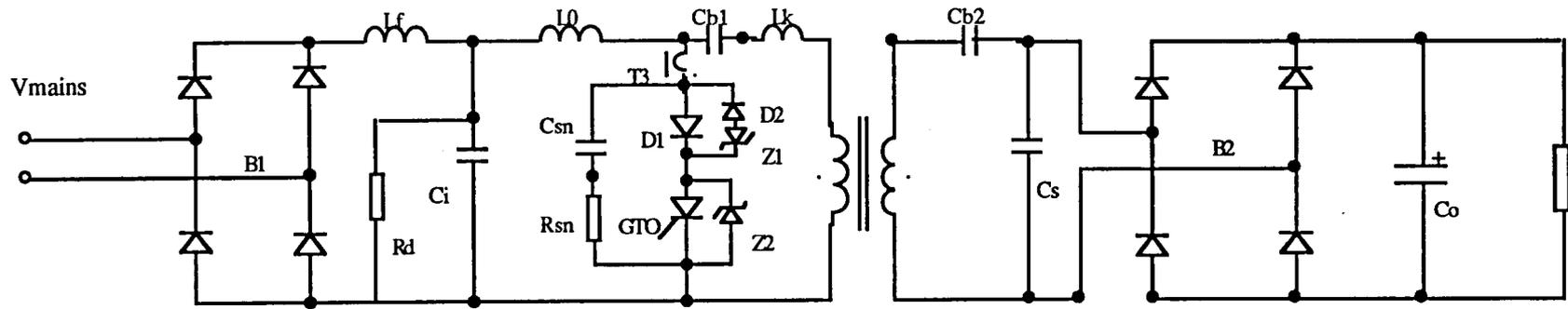


Fig.5.3 A transformer operating with a derated flux swing



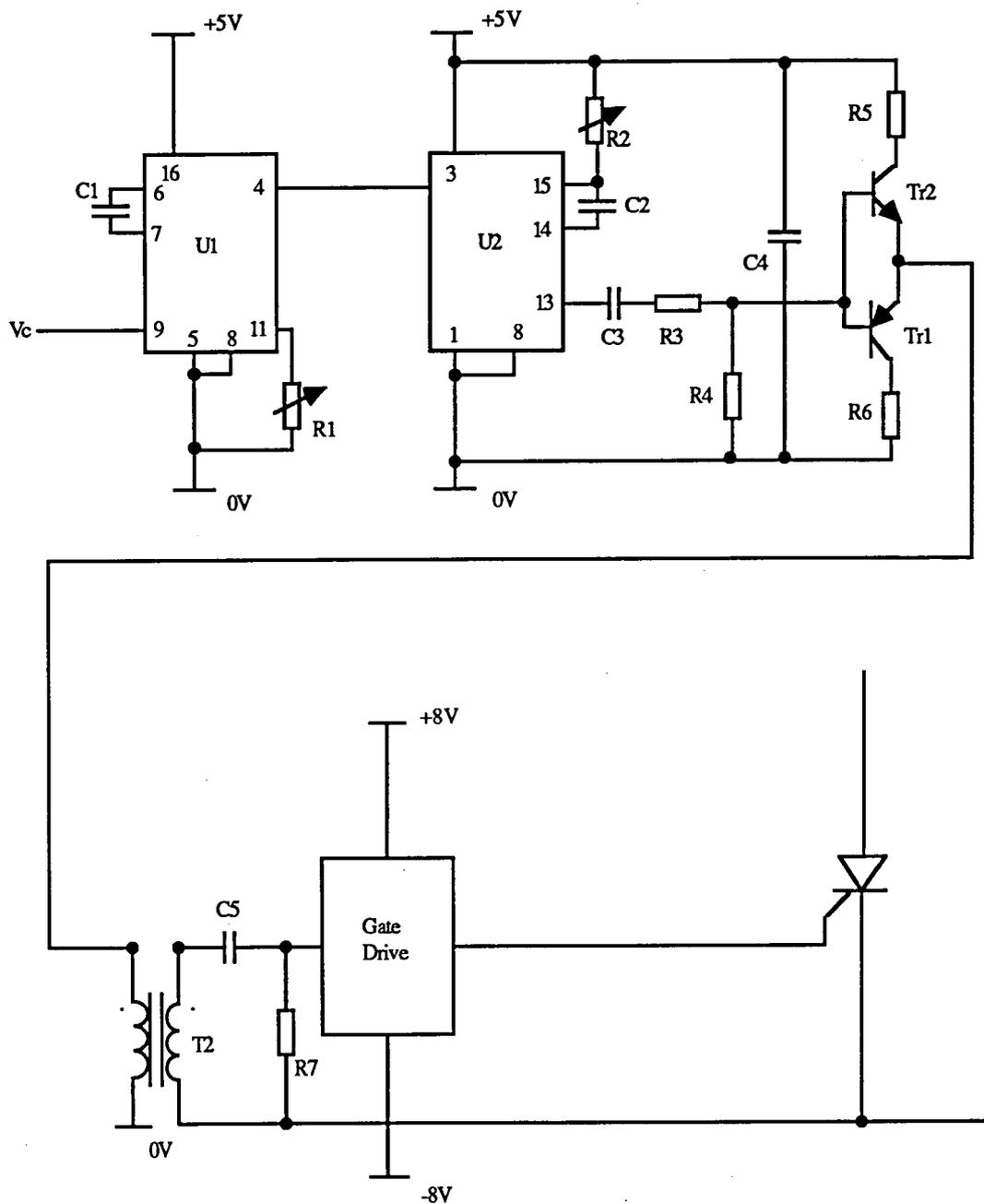
Notes:

1. $R_d=270K$
2. $R_{sn}=100$
3. $C_{sn}=1.65nF$
4. $C_i=1\mu F$
5. $C_{b1}=200nF$
6. $C_{b2}=492nF$
7. $C_s=61.6nF$
8. $C_o=2500\mu F$

9. $L_f=1.5mH$
10. $L_0=3mH$
11. $L_k=37.6\mu H$
12. $Z_1=2*BZW03C91 + 2*BZW03C360$
13. $D_1=BYT230-1000$
14. $D_2=BYW96E$
15. $B_1=4*BYX42-600$
16. $B_2=4*BYT230-1000$

17. T3=current limiting transformer

Fig.5.4 Power stage schematic



Notes :

1. U1=74HCT4046

2. U2=74HCT123

3. Tr1=ZTX451

4. Tr2=ZTX551

5. C1=1nF

6. C2=1nF

7. C3=1μF

8. C4=1μF

9. C5=0.22μF

10. R1=150K

11. R2=50K

12. R3=200

13. R4=2.2K

14. R5=25

15. R6=25

16. R7=1K

17. T2=High frequency pulse transformer

Fig.5.5 Simplified control circuit

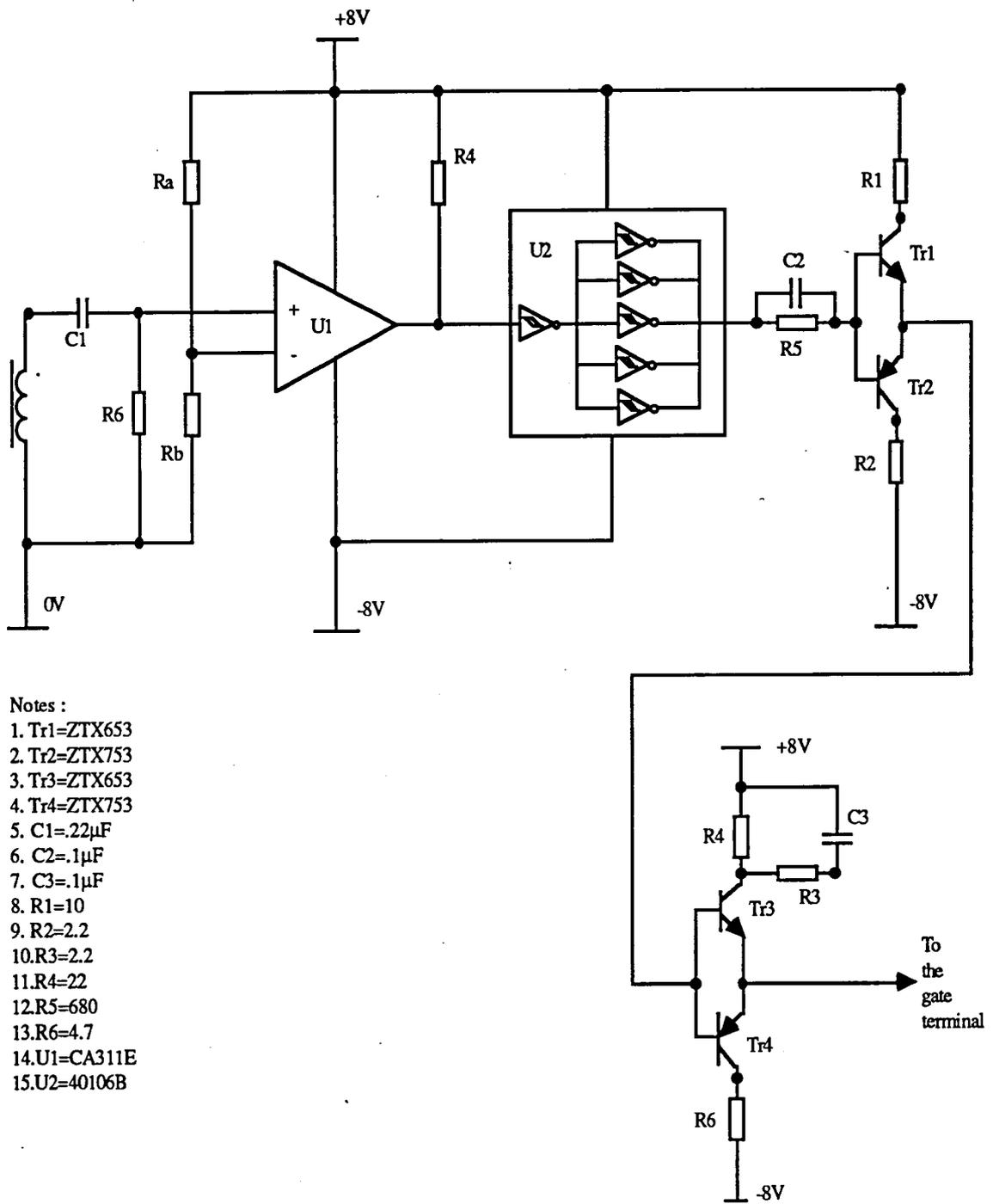
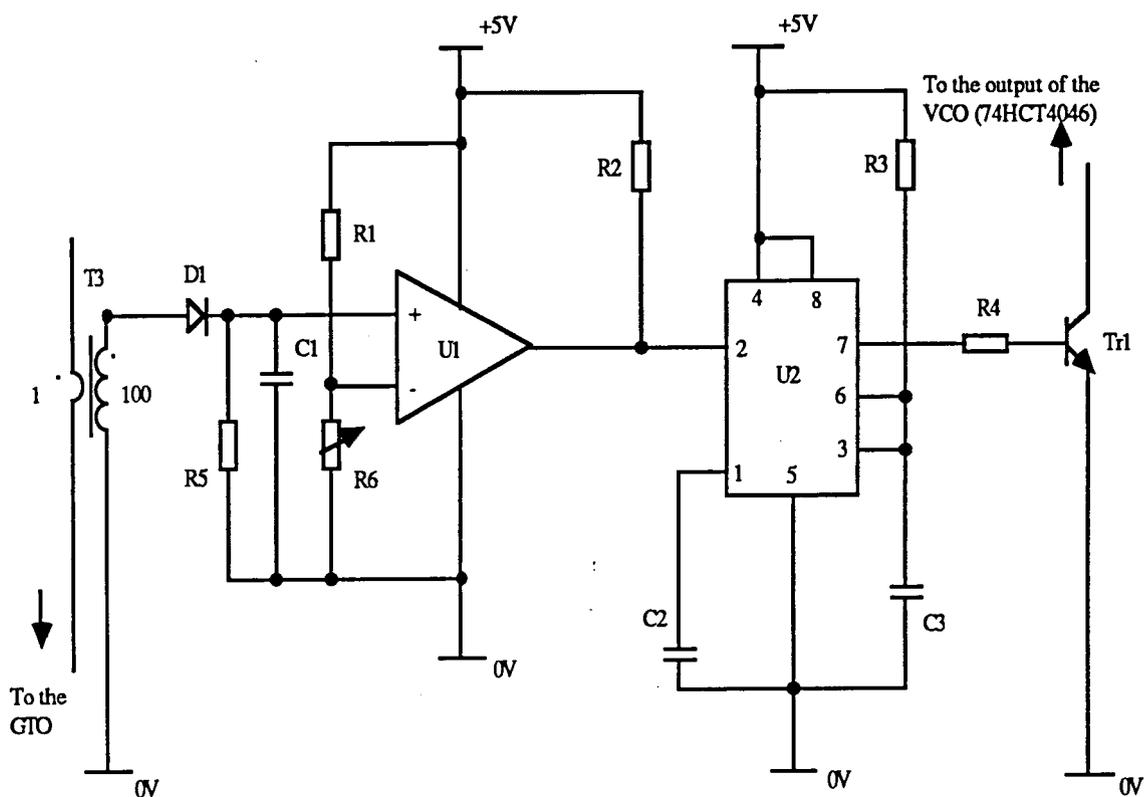


Fig.5.6 The gate drive circuit



Notes :

- | | |
|-------------------|-------------------------------|
| 1. U1=CA311E | 8. R1=1K |
| 2. U2=CA555 | 9. R2=10K |
| 3. Tr1=ZTX451 | 10. R3=470 |
| 4. D1=BA159 | 11. R4=10K |
| 5. C1=1nF | 12. R5=15 |
| 6. C2=10nF | 13. R6=1K |
| 7. C3=2.2 μ F | 14. T3=Current
Transformer |

Fig.5.7 Current limiting circuit

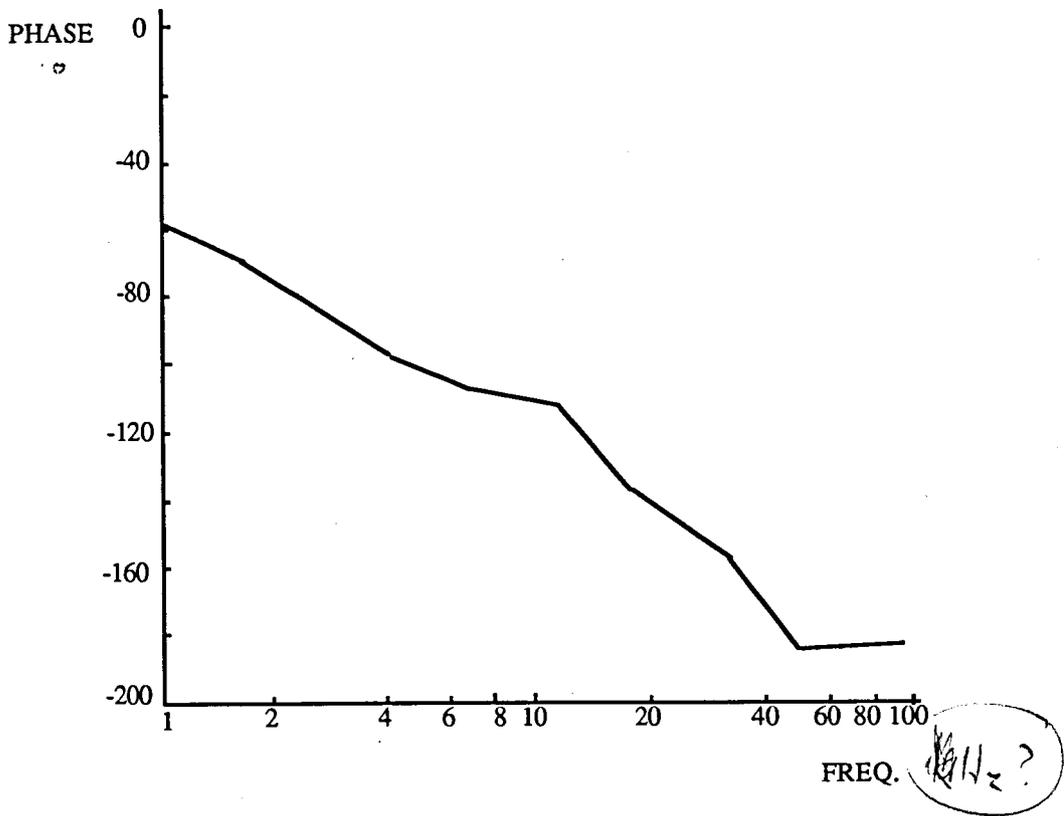
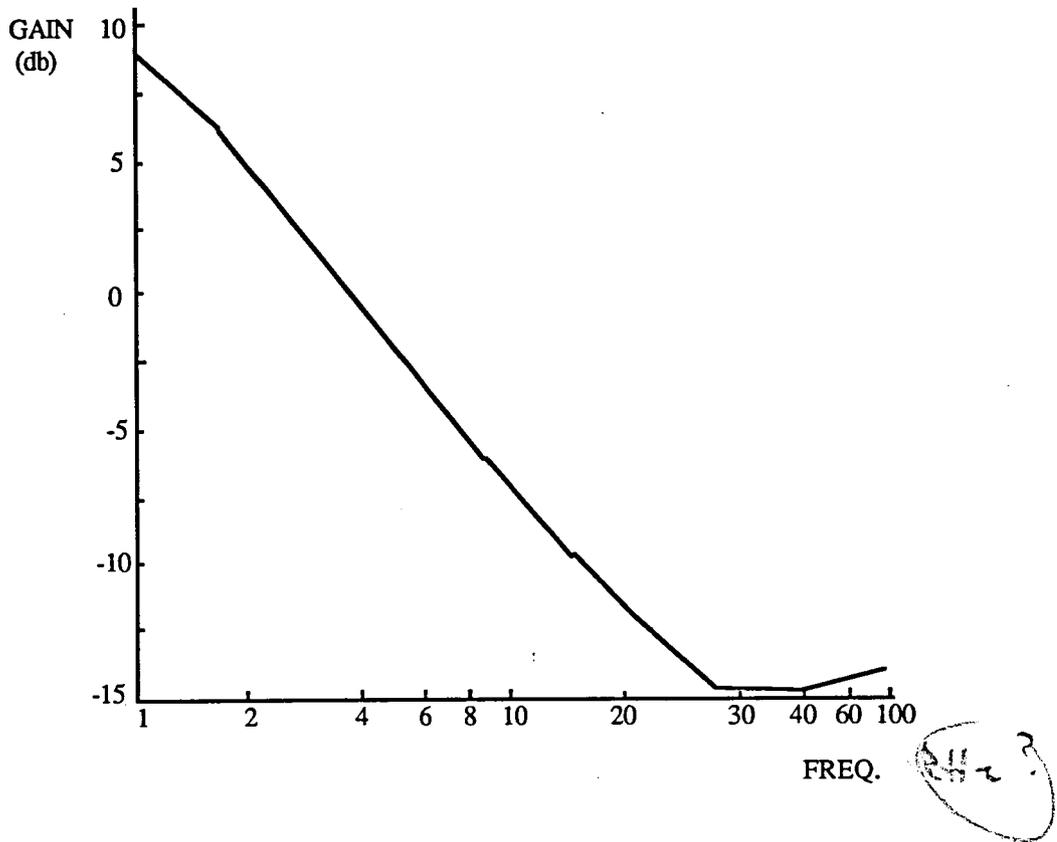


Fig.5.8 Bode plots of the open loop system

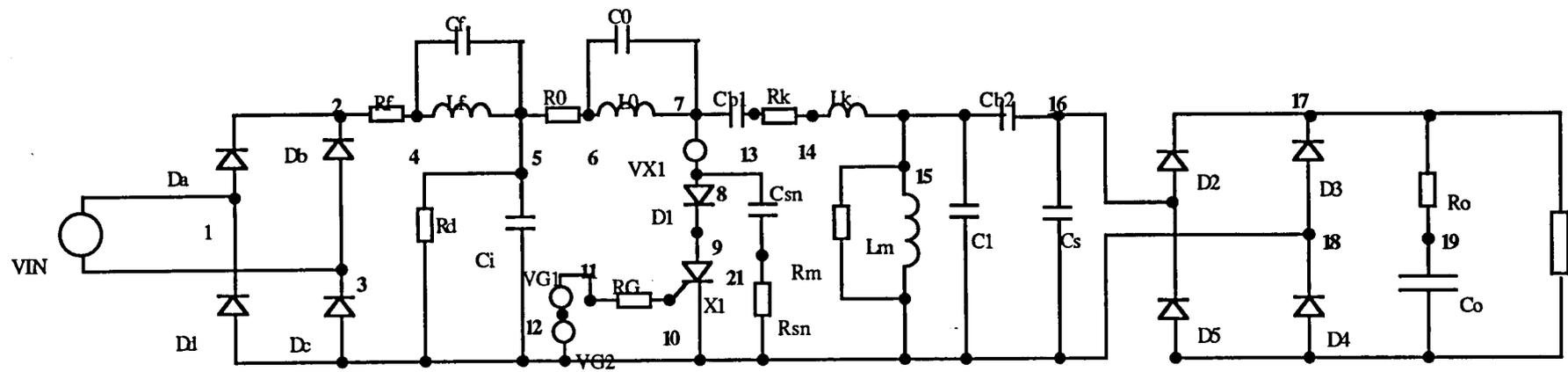


Fig.5.10 A simplified equivalent computer model of the resonance converter

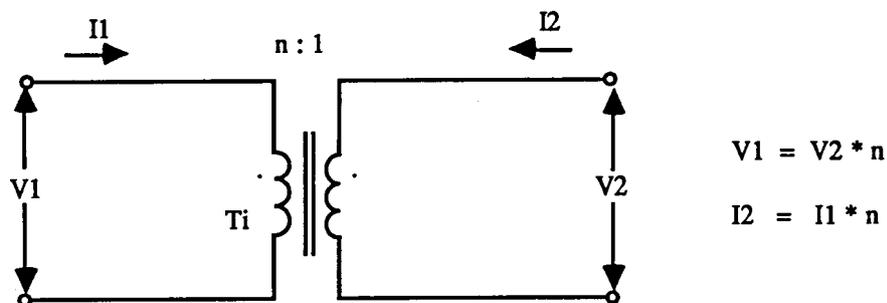


Fig.5.11 An ideal transformer i-v relationship

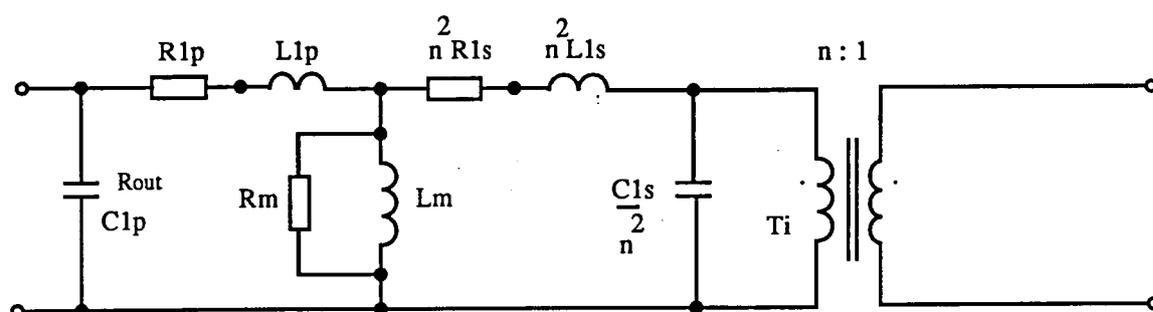


Fig.5.12 A transformer equivalent model

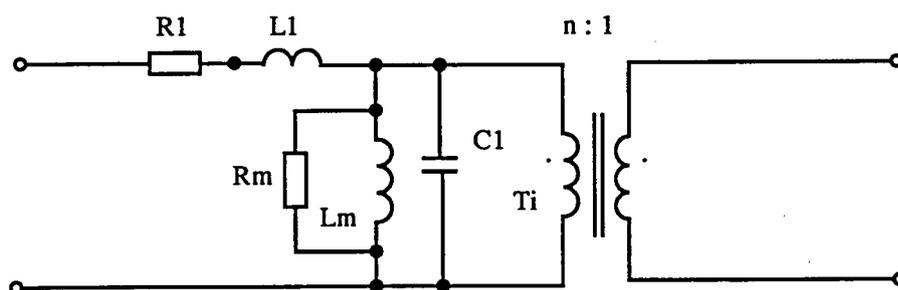


Fig.5.13 A more simplified model

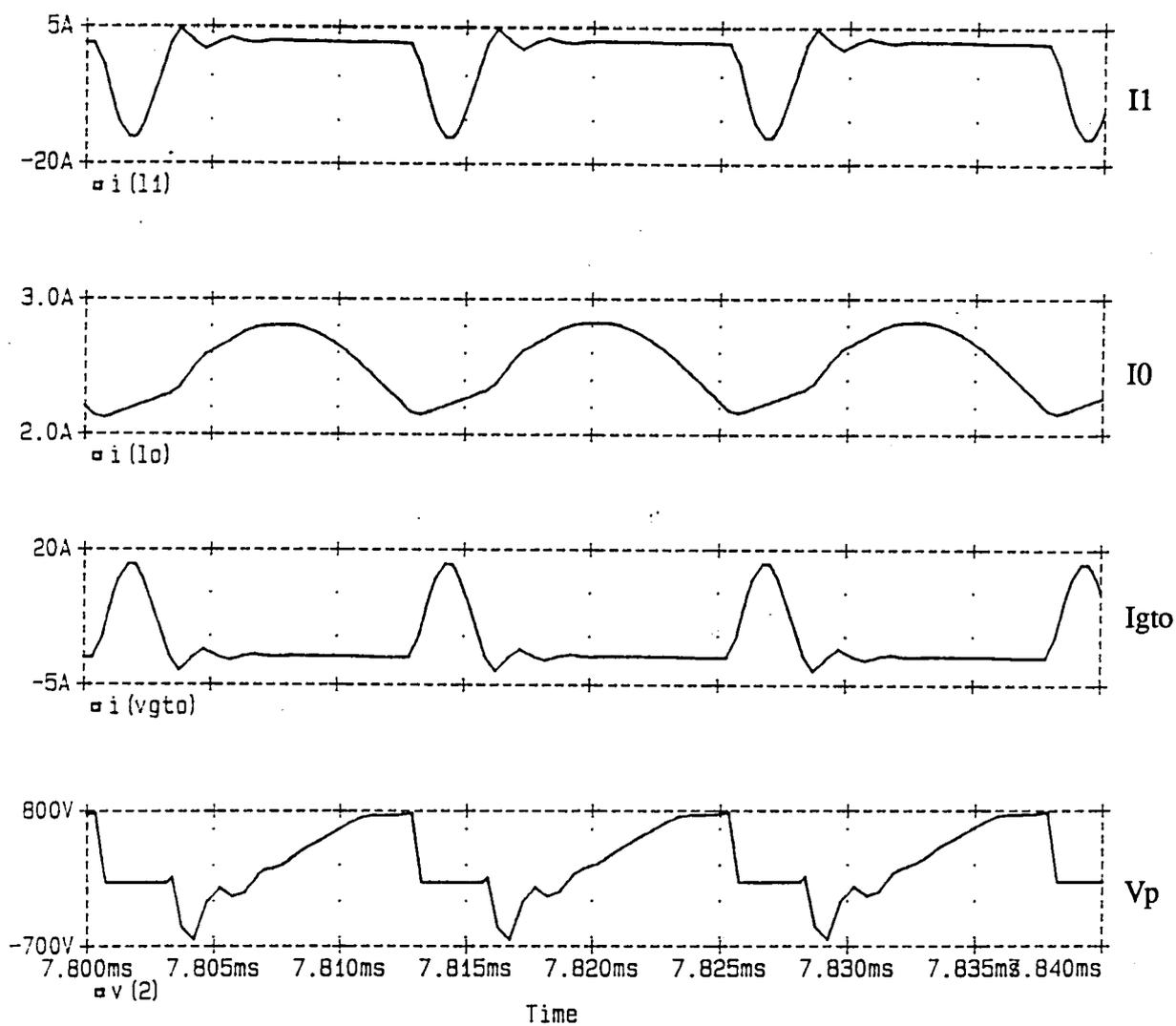


Fig.5.14a Simulated waveforms of the 300W converter at $E_i=216.45V$

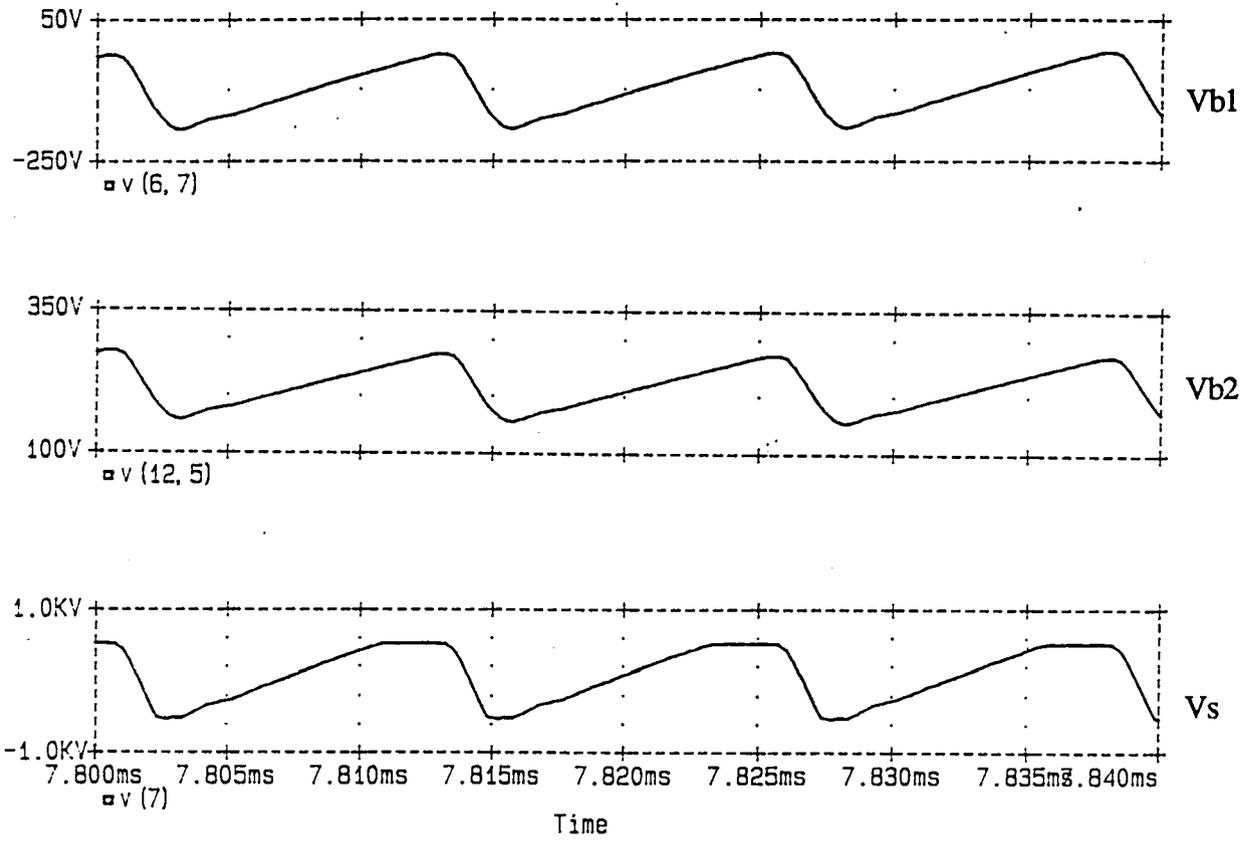


Fig.5.14b Simulated waveforms of the 300W converter at $E_i=216.45V$

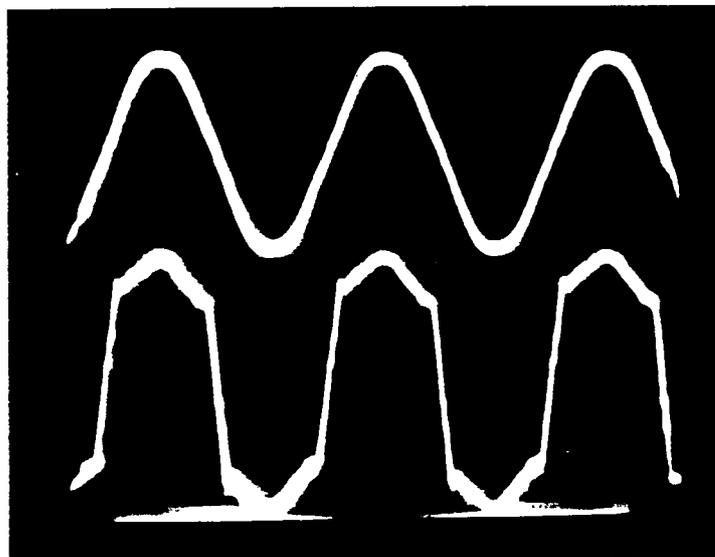


Fig.5.15 Experimental waveforms of the converter. $V_{in}=240V_{ac}$, $f_s=80kHz$

Top trace : Input voltage 200V/div, 5ms/div

Bottom trace : Input current 1A/div, 5ms/div

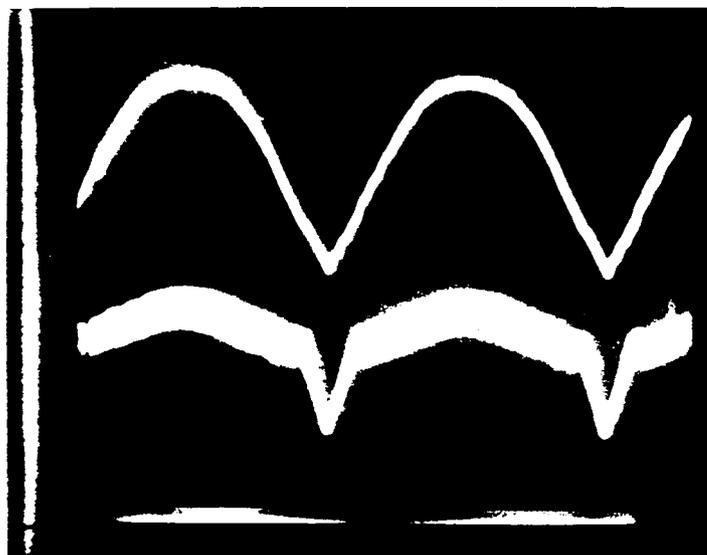


Fig.5.16 Experimental waveforms of the converter. $V_{in}=240V_{ac}$, $f_s=80kHz$

Top trace : Rectified input voltage 100V/div, 2ms/div

Bottom trace : Input Inductor current (I_O) 1A/div, 2ms/div

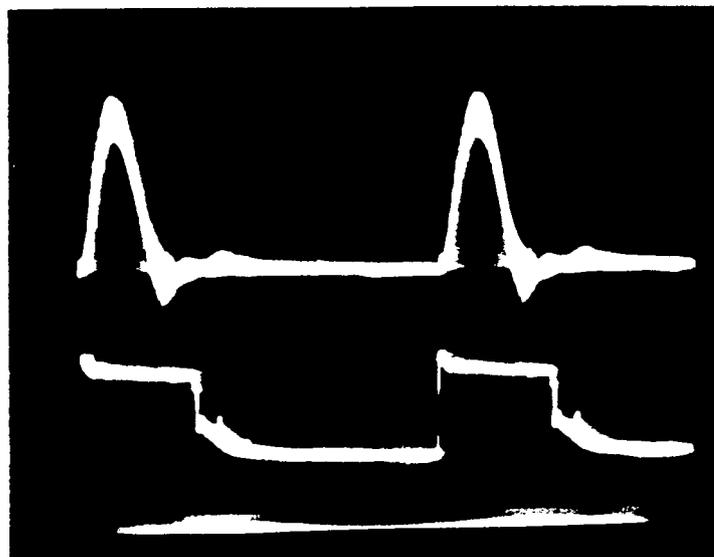


Fig.5.17 Experimental waveforms of the converter. $V_{in}=240V_{ac}$, $f_s=80kHz$

Top trace : GTO thyristor current 5A/div, $2\mu s/div$

Bottom trace : Trigger pulses 5V/div, $2\mu s/div$

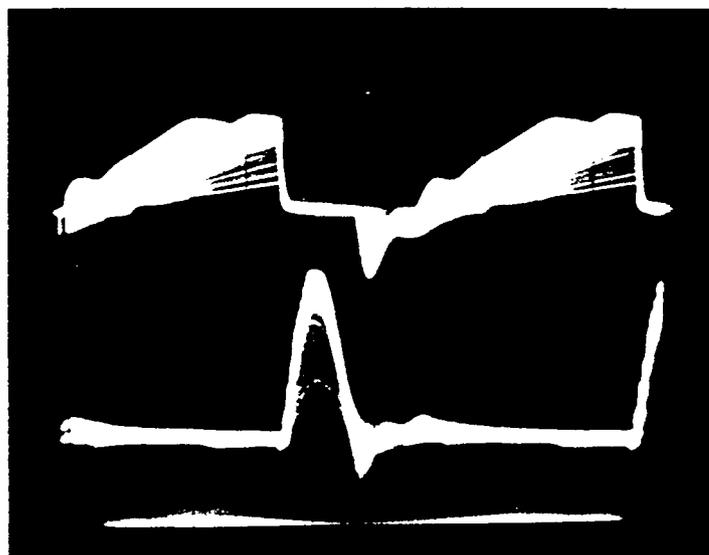


Fig.5.18 Experimental waveforms of the converter. $V_{in}=240V_{ac}$, $f_s=80kHz$

Top trace : GTO and diode D1 voltage 500V/div, $2\mu s/div$

Bottom trace : GTO thyristor current 5A/div, $2\mu s/div$

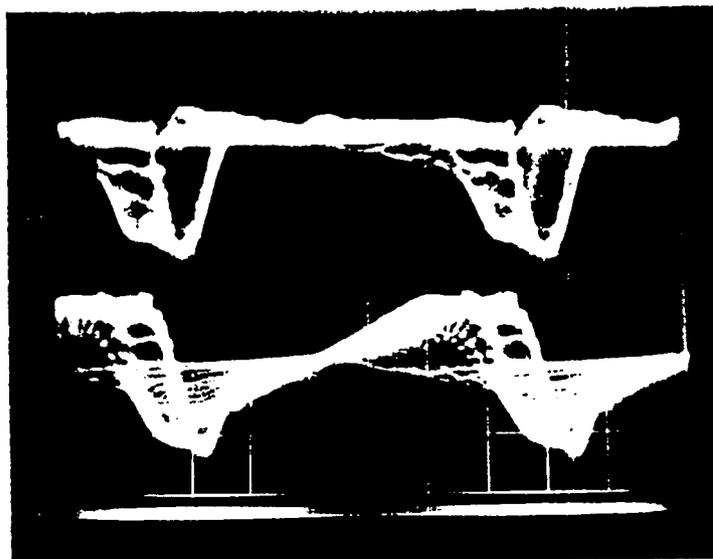


Fig.5.19 Experimental waveforms of the converter. $V_{in}=240V_{ac}$, $f_s=80kHz$

Top trace : Transformer secondary current 10A/div, $2\mu s/div$

Bottom trace : Capacitor C_s voltage 200V/div, $2\mu s/div$

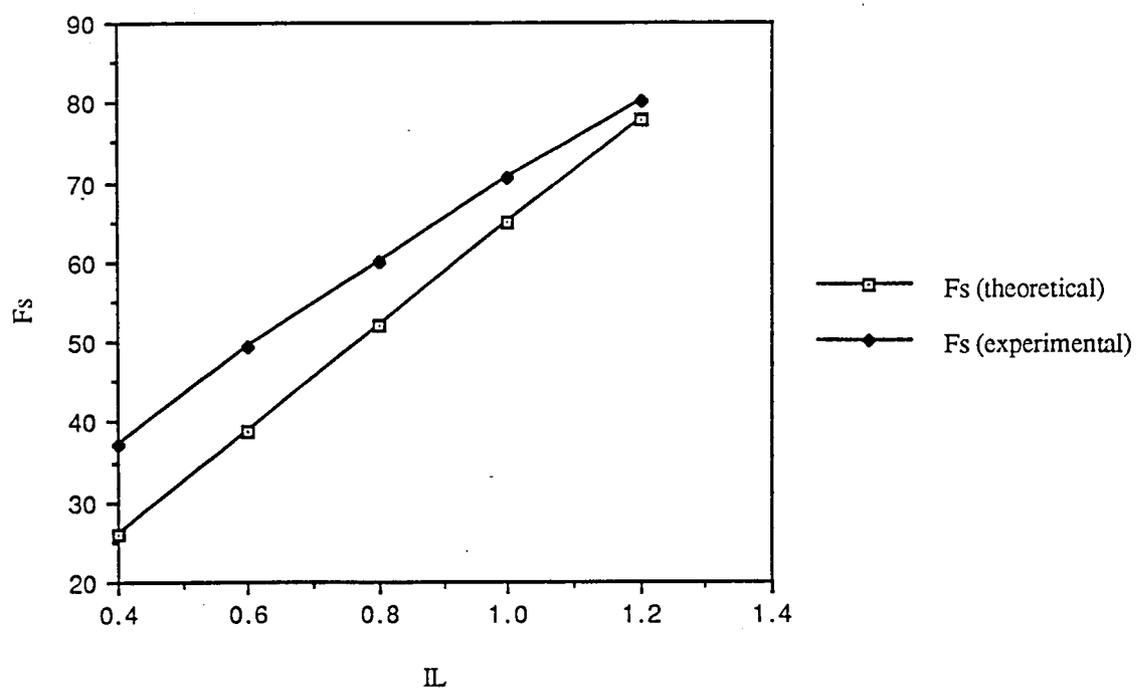


Fig.5.20 Switching frequency vs Load current

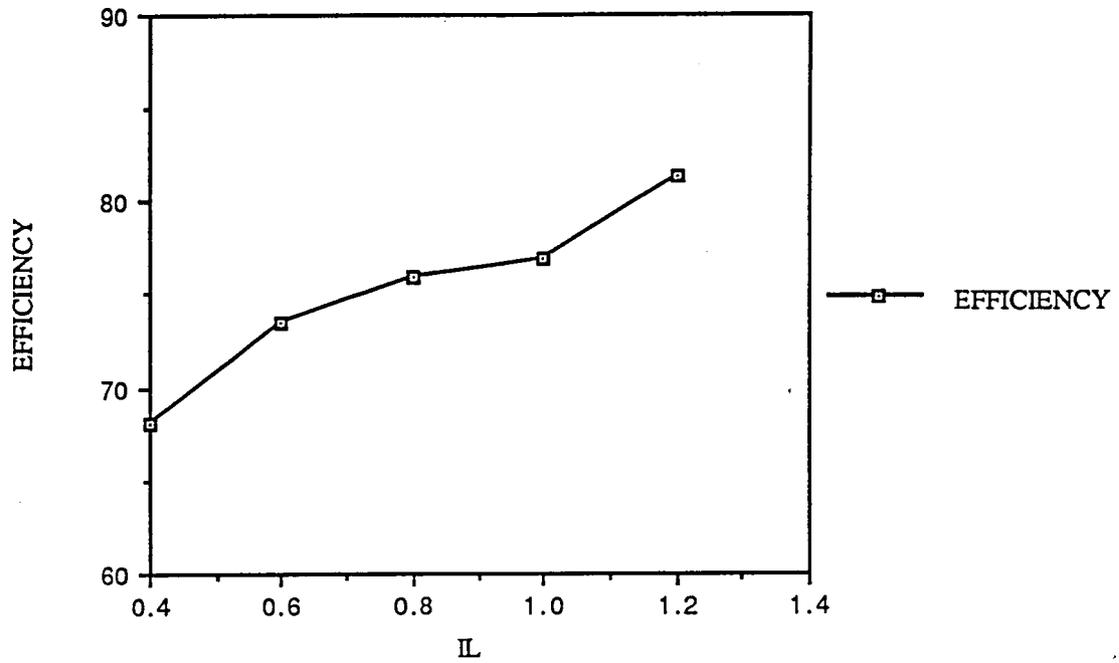


Fig.5.21 Efficiency vs Load current

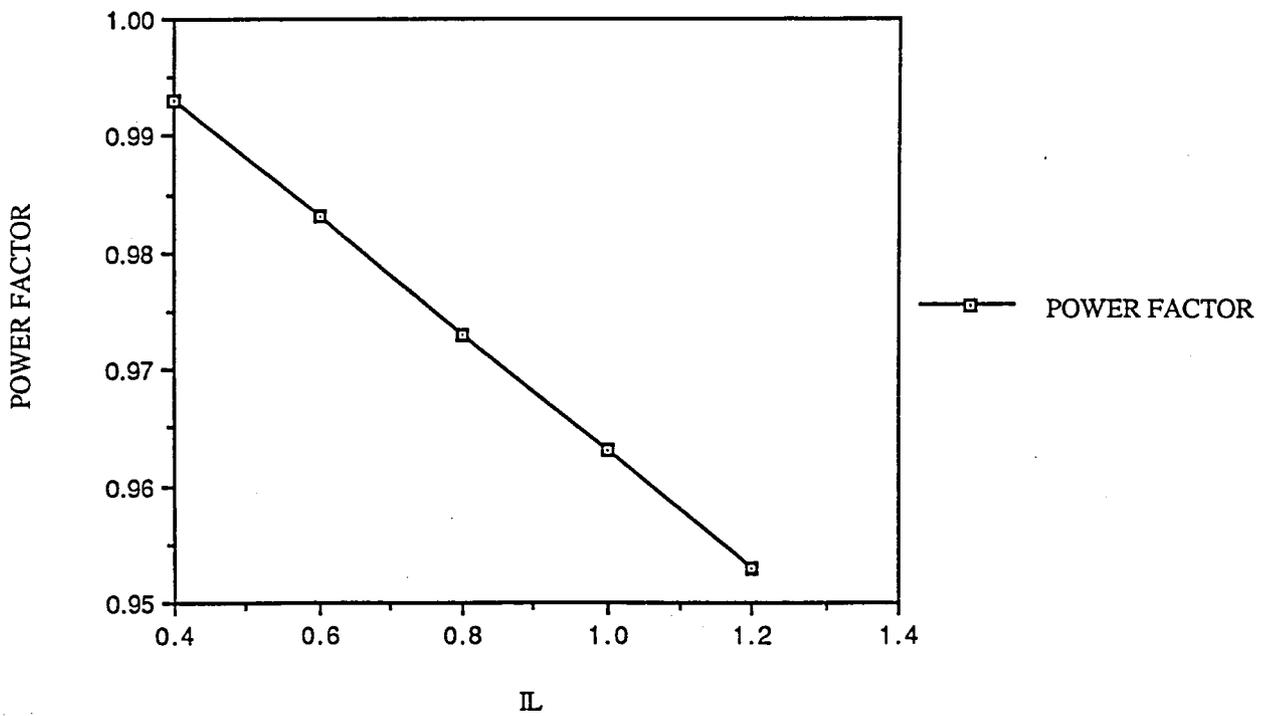


Fig.5.22 Power factor vs Load current

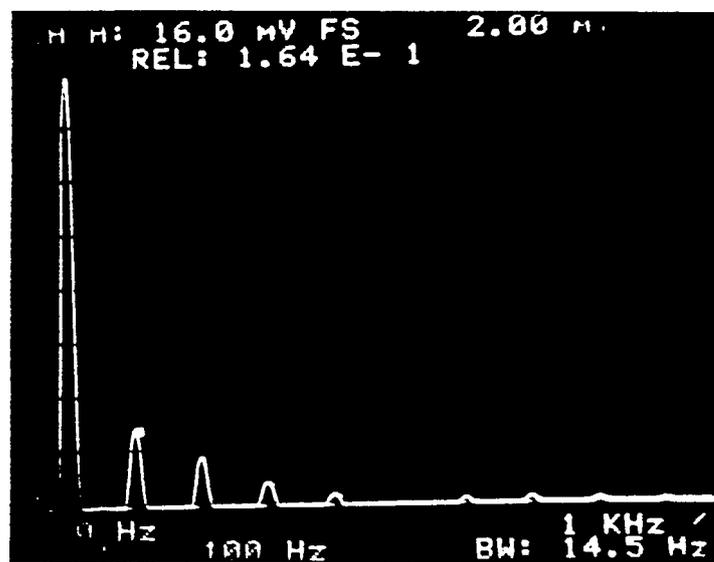


Fig.5.23 Frequency spectrum of the input current

CHAPTER 6

A ZERO-CURRENT SWITCHING QUASI-RESONANT FLYBACK CONVERTER

The chapter discusses the reasons for using a zero-current switching quasi-resonant flyback topology for off-line power applications. The design, computer simulation and the experimental results obtained from a 250W/24V converter circuit, operating at 300kHz are also presented.

6.1 INTRODUCTION

Several types of circuit topologies exhibiting zero-current switching characteristics have emerged into the commercial market since its inception in the mid 1970s [1] - [3]. In the mid 1980s, Liu and Lee proposed the "resonant switch" in order to generalise these topologies [4]. A family of converters named "quasi-resonant" emerged as a consequence of this proposal.

This new family of converters can be viewed as hybrid converters between PWM converters and resonant converters. They utilize the principle of inductive or capacitive energy storage and transfer in a similar fashion to PWM converters and the circuit topologies also resemble those of PWM converters. However, an LC tank circuit is always present near the power switch, which is used not only to shape the current and voltage waveforms of the switch, but also to store and transfer energy from the input to the output in a similar manner to the conventional resonant converter.

Most quasi-resonant converters were used at low power levels and very high frequencies at first. Frequencies in the megahertz region were selected for applications where power density was a vital factor, and to achieve these frequencies, MOSFETs were used as the switching devices. However, the parasitic junction capacitances of the power MOSFETs became a dominant factor when the switching frequency was raised above 1MHz, due to the turn-on losses and switching noise they produced when discharging [5]. Therefore the zero-current switching technique could not be used at such frequencies, without high switching on losses, which became significant even at low power levels.

To overcome this disadvantage, a novel "zero voltage switching" technique was proposed by Liu and Lee [5]. Here, the auxiliary LC resonant elements were used to shape the switching device voltage waveform at turn-on, in order to create a zero-voltage condition for the device to turn-on, thus overcoming the high turn-on losses (in the zero-current switching technique, the auxiliary resonant elements are used to shape the switching device current waveform at turn-on, to create a zero current condition for the device to turn-on).

However when this technique is used in off-line applications, the off-state voltage stress on the power switch becomes much higher than in the corresponding zero-current switching topology [6]. This value rises further as the load current increases. Therefore, no attempt is made to implement this technique. In order to keep the turn-on losses from becoming dominant, the switching frequency is kept below 1MHz.

The chapter assesses the merits and limitations of the zero-current switching quasi-resonant

circuits to find a suitable topology for use in high frequency off-line power applications. The assessment will be followed with a preliminary design of a 250W/24V converter operating at 300kHz.

The following chapter then studies the possibility of implementing the input voltage modulation technique, described in Chapter 2, in the quasi-resonant circuit selected. By doing so, a power supply could be realised which is not only small due to the high frequency of operation, but could also have a high power factored front end. And, unlike in most power factor correction circuits, the control circuit within such a power supply could be used to provide a much better regulated output voltage with a much smaller ripple.

6.2 SELECTION OF THE TOPOLOGY

There are many topological variations of the zero-current switching technique, since the family of zero-current switching quasi-resonant circuits were originally derived from their conventional PWM counterparts [4]. However, it could be said that the three most basic isolated topologies, most suitable for high frequency off-line applications are the flyback, the forward and the half bridge converter circuits shown in Figs.6.1-6.3. The high frequency resonant circuits used to shape the switch current to achieve zero-current turn-off, could be connected on to the primary or the secondary side of the isolation transformer of these circuits. Furthermore, they could operate in both half-wave as well as full-wave modes. For full-wave mode operation, a switch with bidirectional conduction is needed. For half-wave mode operation on the other hand, only a switch with unidirectional conduction is used.

A comparison of all these different topological variations will therefore be carried out to find a suitable candidate for use in off-line power applications.

6.2.1 Primary side vs secondary side resonance

The main advantage in using secondary side resonance as opposed to primary side resonance, is the possibility of using the leakage inductance of the transformer as the resonant inductor. This may overcome the need for an extra magnetic component. On the other hand, the size of the resonance capacitor in primary side resonance topologies is relatively small and has a low current, high voltage requirement. Therefore the ESR of the capacitor is not crucial [7].

Most quasi-resonant topologies today however, use secondary side resonance. A low ESR is ensured by the use of polypropylene or ceramic pulse capacitors [8].

6.2.2 Full-wave vs Half-wave

The comparison of full-wave and half-wave mode topologies is based on the sensitivity of the voltage conversion ratio (voltage gain) to load variations. Full-wave mode topologies theoretically are insensitive to load variations, since they are able to return the excessive energy in the circuit to the source. This results in a narrow frequency range of operation when regulating the converters output voltage and an easier implementation of a high-bandwidth closed-loop design [9]. The control circuit in the half-wave mode converters on the other hand, must vary the switching frequency over a wide range, and at no-load, operate at zero frequency. To overcome this phenomenon, an external load or a bleeder resistor is usually used to maintain a minimal operating frequency in these circuits. This rather low frequency of operation of these converters under light loads however, necessitates the implementation of the closed-loop control circuit with a much lower cross over frequency [9]. Furthermore, the large frequency range of operation in half-wave mode circuits, increases the size of the filter inductance needed by, at times, as much as 60 times the filter inductance of their full-wave mode counterparts [10].

Although the full-wave mode zero-current switching topologies are therefore preferable to the half-wave mode circuits, there is a practical limitation which virtually eliminates full-wave mode topologies from high-frequency off-line applications. This limitation is due to the "snap" reverse recovery characteristics of the anti-parallel diode, which, in conjunction with the resonant inductor, gives rise to a high voltage overshoot (spike) and oscillations when the diode turns off. This causes severe stress and additional dissipation in the switch. Oscillations are caused by the resonance that occurs between the resonant and parasitic inductances in the circuit and the device capacitance. The magnitude of the overshoot depends upon the circuit conditions and diode type. The spikes could be reduced by using "soft" recovery diodes. However, suitable, commercially available, fast recovery diodes are still not "soft" enough to reduce the overshoots significantly. The half-wave zero-current quasi-resonant topologies on the other hand, do not permit the anti-parallel diodes to conduct, and consequently do not suffer from this phenomenon.

Amarasinghe and Manning have however shown in the recent past [11], that the magnitude of the voltage spikes appearing in full-wave topologies can be reduced considerably with the help of a simple RC snubber circuit. Although this would reduce the efficiency of the circuit, the reduction is marginal as long as the switching frequency is not excessively high,

and the reduction of the peak voltage stress on the device is considerable.

6.2.3 Single ended vs Half bridge

Half bridge topologies are generally preferred for off-line applications due to the lower "off" state voltage stress on the switching devices, when compared with single ended topologies operating at the same supply voltage. However, the employment of a MOSBIMOS switch configuration, discussed in Chapter 2, enables the designer to use single ended topologies for off-line applications, at higher power levels, while maintaining a high switching frequency of operation [12].

Although three devices are used in the MOSBIMOS switch configuration compared to two devices in the half bridge topology, the overall cost of the MOSBIMOS is significantly less. This is because the high voltage MOSFET in the switch is needed only to pass a peak of current at turn-on and thereafter, conduct the bipolar on-state base current. Therefore, it need not have a low "on" state resistance. This helps to keep the cost down considerably. The low voltage MOSFET on the other hand, blocks only a very small voltage (determined by the zener diode used), again allowing the use of a low cost component. Although the bipolar transistor in the MOSBIMOS configuration is more expensive than the corresponding device in a half-bridge circuit, the drive requirements needed to maintain the same switching frequency is considerably less. A half-bridge circuit employing MOSFETs would again be more expensive than the cost of the single high voltage bipolar transistor in the MOSBIMOS switch. Furthermore, the drive requirements of the MOSBIMOS would also be less complex and cheaper.

Lastly, a half-bridge converter employing MOSFETs and operating in full-wave mode, needs two extra high voltage diodes connected in series with the switches to stop the slow internal body-drain diodes in the MOSFETs from conducting reverse current. These diodes must have very small reverse recovery times, thus increasing the cost of these devices further. In the MOSBIMOS configuration however, the voltage drop across the bipolar transistor, prevents the internal body-drain diode in the low voltage MOSFET from conducting and therefore the need for an extra series blocking diode is overcome.

6.2.4 Flyback vs Forward

The maximum duty cycle that a forward converter can operate at is 0.5. This is due to the converter being derived from a buck converter circuit topology. Requirements for resetting

the transformer prohibits higher conversion ratios. Furthermore, the transformer is not optimally used in a forward converter since the voltage across the transformer is only uni-directional.

A flyback converter on the other hand, can operate in both buck as well as boost modes. It would also have a positive as well as a negative voltage appearing across the transformer primary, thus making better use of the transformer core.

A zero-current switching quasi-resonant flyback converter employing a MOSBIMOS switch configuration, with secondary side resonance and full-wave mode operation, is therefore a more suitable candidate for use in off-line power applications.

6.3 PRINCIPLE OF OPERATION

The zero-current switching quasi-resonant flyback converter in Fig.6.1, could be simplified to an equivalent circuit shown in Fig.6.4 by replacing the transformer with an equivalent T-model. In the circuit, both the leakage inductances (primary and secondary) have been combined into L_1 .

Since the magnetising inductance L_2 is much larger than L_1 , it is assumed that the current through L_2 , I_2 remains constant. It has also been assumed that all the circuit components are ideal. Waveforms that accompany the circuit operation are shown in Fig.6.5.

As the switch is turned on, the current through the leakage inductor L_1 , I_1 begins to rise linearly until it reaches I_2 . The diode D_2 conducts during this interval, as a result of which the voltage across the resonant capacitor C_1 remains clamped at the output voltage, E_O .

As I_1 exceeds I_2 , current begins to be diverted into the capacitor C_1 and resonance starts to take place until I_1 drops back to zero. Due to full-wave mode operation, the current will continue to oscillate feeding energy back to the source via D_1 . The switch is turned off during this period. After the diode D_1 stops conducting, the energy stored in C_1 is discharged into the magnetising inductance. The voltage across C_1 , V_1 therefore drops to $-E_O$, after which the diode D_2 starts to conduct again, clamping V_1 to $-E_O$ in the process. The magnetising inductor L_2 then releases the stored energy to the output.

Since the switch turns on at zero-current and is turned off by current starvation, the turn

on/off losses are minimal in this circuit.

6.4 PRELIMINARY DESIGN OF A 250W / 300KHZ CONVERTER

6.4.1 Power circuit design

The flyback converter is effectively, a buck-boost converter with an isolation transformer of turns ratio $n = n_p / n_s$. The design is therefore carried out for the buck-boost circuit shown in Fig.6.4. The input/output requirements of the flyback converter are as follows,

Input voltage range	: Single phase 190-270 Vac, 50Hz
Output voltage	: 24 ± 0.05 Vdc at 5.2-10.4A
Output power range	: 125W-250W
Switching frequency range	: 150kHz-300kHz

After full-wave rectification, the steady state input voltage could therefore vary from a minimum of 268.7 Vdc to a peak of 381.9 Vdc.

The first step in the design process is the selection of the resonant tank elements, L1 and C1. Design guidelines for zero-current switching quasi-resonant converters have been derived in detail in [6]. The selection of the resonant tank elements are based upon the power converter specifications and a design constraint ζ_c . ζ_c is the ratio between the normalized load resistance $Q (= R / Z_o$ where R is the load resistance and Z_o , the tank circuit characteristic impedance) and the dc voltage conversion ratio $M (= E_o / E_i$ where E_o is the dc output voltage and E_i , the dc input voltage). Its magnitude determines whether zero-current switching takes place or not. To ensure turn-off at zero-current [6], $\zeta_c > 1$ (i.e $M > Q$).

ζ_c also plays a significant role in determining the shape of the current waveform during resonance, and hence the peak current through the switching device. A proper design would use a value of ζ_c that permits the lowest possible stress level. The normalized peak current stress on the switching device for a zero-current switching quasi-resonant

buck-boost converter is given by [6]

$$I_{pk} = I_L (1 + M) (1 + \zeta_c) \quad (6.1)$$

where I_L is the load current.

The effect of varying ζ_c is shown in Fig.6.6 [6]. It can be seen that a large value of ζ_c gives rise to a high current stress and also a higher current flow in the reverse direction through the anti-parallel diode. This is undesirable because of increased conduction losses.

A proper design would therefore make ζ_c as close as possible to one, whilst ensuring that zero-current switching took place.

Before determining the resonant tank elements, the transformer turns-ratio must be found which provides the minimal possible stress level on the switching devices. When doing so, the whole of the line voltage and load current ranges must be considered. For a zero-current switching quasi-resonant buck-boost converter, the peak current and voltage stresses are given by [6]

$$I_{pk} = I_{Lmax} (1 + M_{min}) (1 + \zeta_c \frac{M_{max}}{M_{min}}) \quad (6.2)$$

$$V_{pk} = E_o (1 + \frac{1}{M_{min}}) \quad (6.3)$$

Table 6.1 gives a summary of the peak voltage and current stresses for various step down ratios, for an optimum design ($\zeta_c = 1$), and obtained for the the input/output requirements stated above. A step down ratio of 5:1 is chosen here for a peak voltage stress level of 502V and a peak current stress level of 6.54A. However, as stated before, the design is first carried out for a buck-boost converter. The input/output requirements will therefore be changed to satisfy the 5:1 step down condition.

6.4.1.1 Resonant tank circuit design

The first step in the resonant tank circuit design is the selection of the resonant frequency,

f_r of the tank circuit. This can be found from the maximum conversion ratio and the required maximum switching frequency, f_m [6].

$$f_r \approx (f_s)_{\max} \frac{(M_{\max} + 1)}{M_{\max}} \quad (6.4)$$

For a maximum switching frequency of 300kHz, the resonant frequency is 972kHz. The resonant inductor can then be found from [6]

$$Z_o = \frac{R_{\min}}{\zeta_c M_{\max}} = \omega_r L1 \quad (6.5)$$

where ω_r is the resonant angular frequency.

The resonant inductor needed here is 17.6 μ H if ζ_c is set to 1.2 to ensure zero-current turn-off. To obtain the desired resonant frequency of 972kHz, the value of the resonant capacitor C1 is 1.523nF (with a 5:1 step down ratio, this corresponds to a value of 38nF). With the values of L1 and C1 selected, the resonant tank circuit design is complete.

6.4.1.2 Output filter design

The next stage of the design is the selection of the output filter components L2 and C_o. Since the resonant inductor L1 is already known, the value of L2 is given directly by [6]

$$L2 = L1 * \frac{\xi_c}{\xi_f} * [\pi - \cos^{-1} \left(\frac{1}{1+M_{\max}} \right) + \sqrt{(2+M_{\max})M_{\max}}] \frac{1}{1+M_{\max}} \quad (6.6)$$

where

$$\zeta_f = \left[\frac{\Delta I_L / 2}{I_{L\max}}, \frac{I_{L\min}}{I_{L\max}} \right] \quad (6.7)$$

The value of ζ_f is determined, either by a specific maximum ripple current ΔI_L or by the specified converter load range. For the given specifications, $M_{\max} = 0.45$ and $\zeta_f = 0.5$. The value of the filter inductance is therefore

$$L_2 = 5.6L_1 = 98.56\mu\text{H} \quad (6.8)$$

The output capacitor is determined by the ripple requirements at the output. The pk-pk ripple voltage is given by

$$V_{\text{ripple}} = I_L X_c = \frac{I_{L\max}}{2\pi f_{s\min} C_o} \quad (6.9)$$

where $f_{s\min}$ is given by

$$f_{s\min} = f_r \frac{M_{\min}}{1+M_{\min}} \quad (6.10)$$

For the conditions stated above, $M_{\min} = 0.31$ and therefore $f_{s\min} = 232.4\text{kHz}$. Thus for a ripple of 0.5V (this when referred to the primary side), $C_o = 2.85\mu\text{F}$ (with a 5:1 turns ratio this corresponds to 71.34 μF).

As described in Chapter 5, the filter capacitance selection is also dominated to a large extent by the ESR (equivalent series resistance) necessary to obtain an acceptable pk-pk ripple voltage. The maximum ESR permitted is given by

$$\text{ESR}_{\max} = \frac{V_{\text{ripple}}}{I_{\text{Dpk}}} \quad (6.11)$$

where I_{Dpk} is the peak current through the rectifying diode D3.

I_{Dpk} for the input/output requirements stated above is 2.72A [6]. Therefore, $\text{ESR}_{\max} = 0.18\Omega$. With a 5:1 turns ratio, this corresponds to 7.34m Ω .

6.4.2 Transformer design

The transformer is designed to operate at a flux density that is slightly below the saturation flux density of the core, so that the airgap that is needed to store the required energy becomes very small. Mullard's new low-loss 3F3 type ferrite transformer cores are used with the peak working flux density at 0.29T. By following the design procedure given in Unitorde [13], an ETD-39 core with 20 turns on the primary and an airgap of 0.63mm is selected. The magnetising inductance is set at 98.56 μ H, which was the designed value of the filter inductance L2.

As mentioned in the previous chapter, conduction losses due to skin effect could be a major problem in high frequency operation. At 300kHz the penetration depth is

$$\delta \approx \frac{0.066}{\sqrt{f_s}} \text{ m} \approx 0.12\text{mm} \quad (6.12)$$

Therefore, the primary is made up of a number of 0.25mm diameter copper wires, which are twisted together. Copper foil of 0.25mm thickness is used on the secondary.

The leakage inductance that arises as a by product of the transformer construction is used to represent the resonant inductor L1 in the buck-boost converter. A small air-cored inductor of a few turns is added in series with the transformer primary to make up the 17.6 μ H required.

6.4.3 Control loop design

To ensure zero-current switching, the switching devices must be turned off during the time the anti-parallel diode conducts. Since this time is set by the resonant tank circuit and does not change, constant on-time control is required. With the on-time fixed, the switching frequency is varied to control the output voltage. The principle of operation of the control circuit is therefore, very similar to the resonant converter described in Chapter 5. A detailed description of the design procedure will thus be avoided in this chapter.

A straight forward implementation of the control circuit using common integrated circuits is shown in Fig.6.7. The 74HCT4046 is the voltage to frequency converter. The 74HCT 123 monostable is used to set the "on" time of the switch.

The gate drive circuit is however, different to the one used in the previous design. The DS0026 I.C. is used here to satisfy the drive requirements of the power MOSFETs. The drive circuitry is isolated from the control circuit with a high frequency transformer. The transformer is wound on a Siemens R12.5-N30 type ferrite toroidal core with 10 turns of specially insulated wire on the primary.

The zener diode in the MOSBIMOS switch provides a path for the bipolar transistor base current when its emitter is open-circuited. In most applications, the zener also provides a path for the high voltage MOSFET gate current. Initial testing of the circuit however, showed a high voltage spike appearing at the gates of the MOSFETs after turn-off. This spike arose due to the high rate of rise of voltage across the switch at turn-off. The spike is coupled through the drain-gate capacitance of the MOSFET M1 into the gates of M1 and M2. Due to the large parasitic inductance associated with the current path when the two MOSFETs are driven from the same gate drive circuit, it proved difficult to effectively clamp this voltage spike to ground. This led to the MOSFETs being turned back on prematurely. A separate gate drive is therefore used for the high voltage MOSFET to overcome this problem. The zener thus provides a path for the bipolar transistor base current only.

Both gate pulses are tapped off the same transformer primary so that pulses could be applied to the MOSFETs at the same instance. Each of the secondary windings consists of 10 turns of the same insulated wire as the primary.

Current limiting and shut down are implemented by pulling the input to the 74HCT123 to ground. The peak currents through the switch are monitored with the current transformer T2. A Siemens N30 type ferrite toroidal core, with a 100:1 turns ratio is used for this purpose. When the output from the CA311 comparator changes state, the CA555 timer turns on for 1 second, during which time the output pulses are pulled to ground. The switch does not turn on during this period. At the end of this time the power supply turns on again and if the short circuit persists, the supply enters into a hiccup mode.

Closed-loop control is obtained by feeding the output voltage into the uA723 error amplifier which then provides the required control voltage to the voltage to frequency converter. The gain and phase plots of the open loop system, obtained by using a transfer function analyser, are shown in Fig.6.8. The characteristics of a second order system are evident, with a double pole at 1.89kHz corresponding to the converter filter components.

Loop compensation is achieved by using a dominant pole to roll-off the gain below the pole frequency. The compensation network is shown in Figure 6.9. Resistors R1 and R2 set the

dc gain at 5dB $\{20\log(R2/R1)\}$ and a capacitance of 15nF gives unity gain at a frequency of 1.06kHz $(1/2\pi R1C)$. By doing so, the gain is forced to zero well before the phase passes through -180 degrees.

The power stage is isolated from the control stage with a HP6N135 type opto-coupler.

6.5 COMPUTER SIMULATION

The PSpice computer simulation program is used again to analyse the 250W practical converter circuit described above. The equivalent circuit device models, which were produced by using the Parts program, are used to represent the semiconductor devices in the circuit. Listings of these model parameters are given in Appendix 1. The flyback transformer is represented by the equivalent circuit transformer model given in the previous chapter. The leakage and magnetising inductances, winding self capacitance and the winding and hysteresis loss resistances of the transformer are as follows,

$$L1 = 17.6\mu\text{H}$$

$$L_m = 82\mu\text{H}$$

$$C_w = 18.38\text{pF}$$

$$R1 = 0.098\Omega$$

$$R_m = 0.8\text{M}\Omega$$

The ESR of the resonance capacitor and the output filter capacitor is negligible.

An RC snubber network consisting of a 47 Ω resistor and a 470pF capacitor, connected in series, is added across the anti-parallel diode D2 to reduce the effects of its "snap" reverse recovery characteristics. The reasons for selecting these values are given in the following section.

The need for including the parasitic inductances in the MOSFET model to obtain a more accurate representation of the practical circuit was described in Chapter 3. The internal source and drain inductances for the BUZ24 type MOSFET are as follows,

$$\text{Internal source inductance} = 12.5\text{nH}$$

$$\text{Output source inductance} = 5\text{nH}$$

These inductances are the same for the BUZ54A type MOSFET. These four inductors, together with a 100nH external source inductance are therefore included in the computer model of the quasi-resonant flyback converter.

A complete equivalent circuit representation of the power circuit to be analysed is given in Fig.6.10. Figs.6.11 and 6.12 show the predicted voltage and current waveforms when the ac input voltage is at 190V and 270V respectively. The switching frequency has been reduced to 232.4kHz in the latter case to compensate for the increased input voltage.

A listing of the program used is given in Appendix 5.

Given below are the voltage and current stresses on the MOSBIMOS and the rectifying diode D3, calculated according to the stress analysis procedure described in [6].

Peak MOSBIMOS stresses (at 270Vac) :

$$I_{spk} = I_{Lmax} (1 + M_{min}) (1 + \zeta_c \frac{M_{max}}{M_{min}}) = 7.4 \text{ A} \quad (6.13)$$

$$V_{spk} = E_o (1 + \frac{1}{M_{min}}) = 501.8 \text{ V} \quad (6.14)$$

Peak diode stresses (the peak current occurs at 190Vac) :

$$I_{Dpk} = I_{Lmax} (1 + M_{max}) = 3 \text{ A} \quad (6.15)$$

$$V_{Dpk-pk} = 2E_o (1 + \frac{1}{M_{min}}) = 1003.6 \text{ V} \quad (6.16)$$

The stress levels obtained from the simulated results are as follows,

$$I_{spk} = 7 \text{ A}$$

$$V_{spk} = 495.4 \text{ V}$$

$$I_{Dpk} = 2.9 \text{ A}$$

$$V_{Dpk-pk} = 995 \text{ V}$$

The results produced are therefore seen to agree very closely with the peak theoretical stress levels of the switch and rectifying diode elements. The slight errors are caused by the losses in the circuit components.

6.6 POWER CIRCUIT CONSTRUCTION AND PERFORMANCE EVALUATION

A power converter board is constructed using the component values shown in Fig.6.13. The anti-parallel and output rectifying diodes are ultra-fast recovery types. C1 is made up of a 22nF, a 10nF and two 3.3nF metallized polyester type capacitors, connected in parallel to each other. The output capacitor is a combination of two, 22 μ F polycarbonate type capacitors and three, 10 μ F metallized polyester type capacitors, again connected across one another.

The snubber capacitor across the switching device is selected for a 5% loss (12.5W) in the snubber circuit [14]. Snubber losses are given by

$$P_{\text{loss}} = \frac{1}{2} C_s V_s^2 f_s \quad (6.17)$$

These losses are maximum at the highest supply voltage, at which point $V_s = 502\text{V}$ and $f_s = 232.4\text{kHz}$ [6]. Thus for a 12.5W snubber loss, $C_s = 430\text{pF}$. An RC snubber combination of 47Ω and 470pF have therefore been connected across the anti-parallel diode D1 to reduce the effects of its "snap" reverse recovery characteristics. A snubber circuit is not needed across the output rectifying diode due to the low voltage stress level on it.

The converter was found to have a full load efficiency of 83% and performed satisfactorily over the line and load conditions specified. Figs.6.14 and 6.15 show the voltage and current waveforms of the various power semiconductors. These experimental waveforms show a very close resemblance to the simulated results given in the previous section thus confirming the accuracy of the computer predictions.

As described before, the ringing on the current waveform through the switch after turn-off is caused by the resonance between the leakage inductance and the diode capacitance. This and the voltage overshoots across the switching device have been reduced considerably with the help of the snubber circuit.

6.7 CONCLUDING REMARKS

A review of the family of quasi-resonant circuits has shown that the zero-current switching flyback converter, operating in full-wave mode, is a suitable topology for off-line power applications. The use of a MOSBIMOS switch has enabled this converter to process relatively high levels of power, while maintaining the switching frequency at a high value.

The chapter also presented the design procedure for an off-line 250W quasi-resonant flyback converter, switching at upto 300kHz. The use of separate gate drives for the two MOSFETs in the MOSBIMOS, resulted in a more efficient operation of the switching device. The design was verified by the presentation of simulated and experimental results which showed a very close resemblance. The results also showed that the high voltage overshoots and oscillations occurring after turn-off of the switch could be reduced considerably with the help of a simple RC snubber circuit. High frequency design techniques were used in the design of the flyback transformer. A straight forward control circuit which gives variable frequency, constant on-time control, was also implemented in the converter.

6.8 REFERENCES

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power conversion", Proc. European Space Power Conf., 351-356.

6.9 TABLES

Turns Ratio n:1	Peak Voltage (V)	Peak Current (A)
10	622	4.07
8	574	4.68
6	526	5.75
5	502	6.54
4	478	7.80
3	454	9.91
2	430	14.1

Table 6.1 Switching stresses on a zero-current switching quasi-resonant flyback converter

6.10 FIGURES

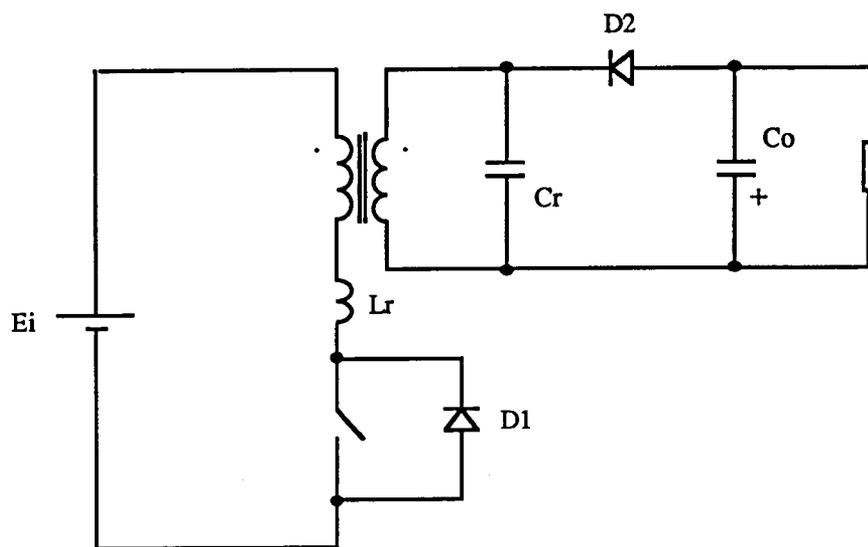


Fig.6.1 A zero-current switching quasi-resonant flyback converter with secondary side resonance and full wave operation

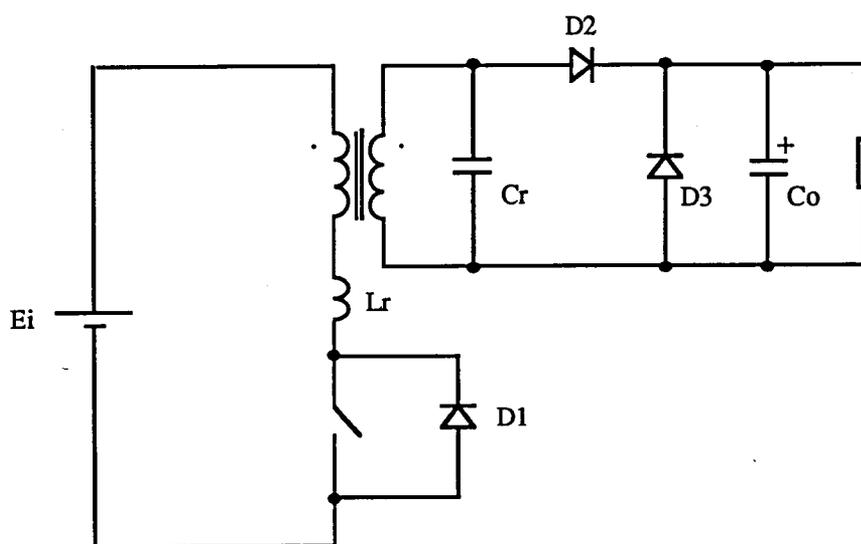


Fig.6.2 A zero-current switching quasi-resonant forward converter with secondary side resonance and full wave operation

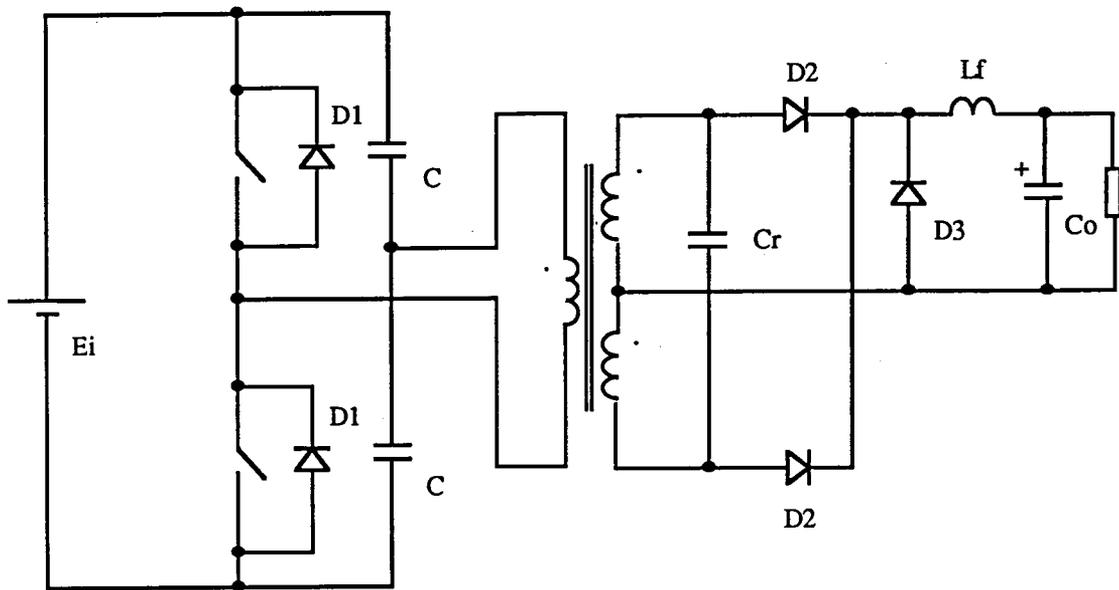


Fig.6.3 A zero-current switching quasi-resonant half bridge converter with secondary side resonance and full wave operation

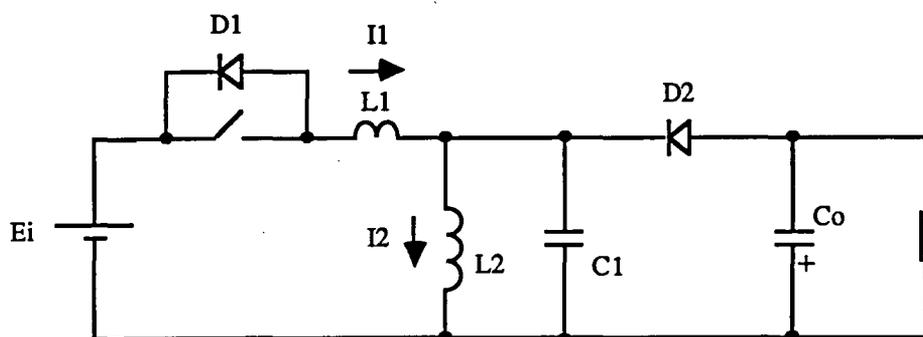


Fig.6.4 A simplified equivalent circuit of the zero-current switching quasi-resonant flyback converter

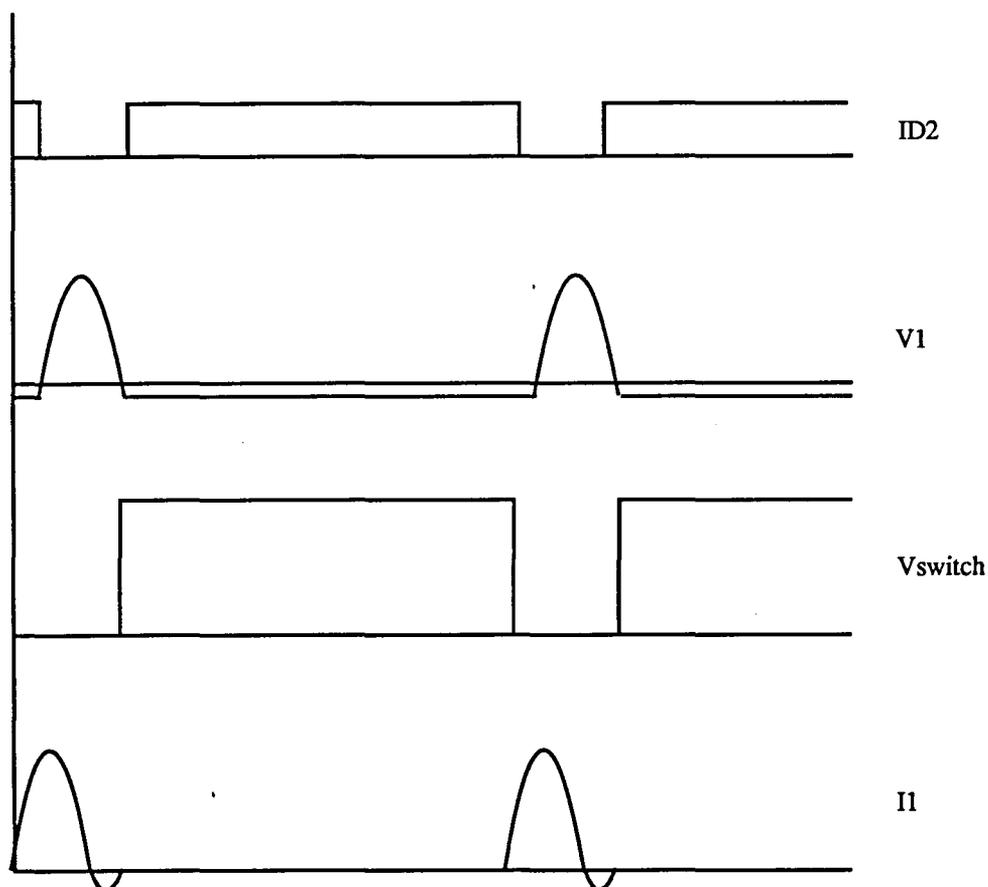


Fig.6.5 Waveforms of the zero-current switching quasi-resonant flyback converter

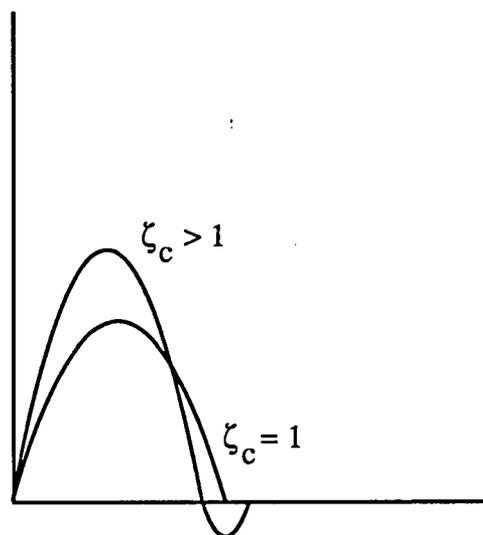


Fig.6.6 The effect of varying ζ_c

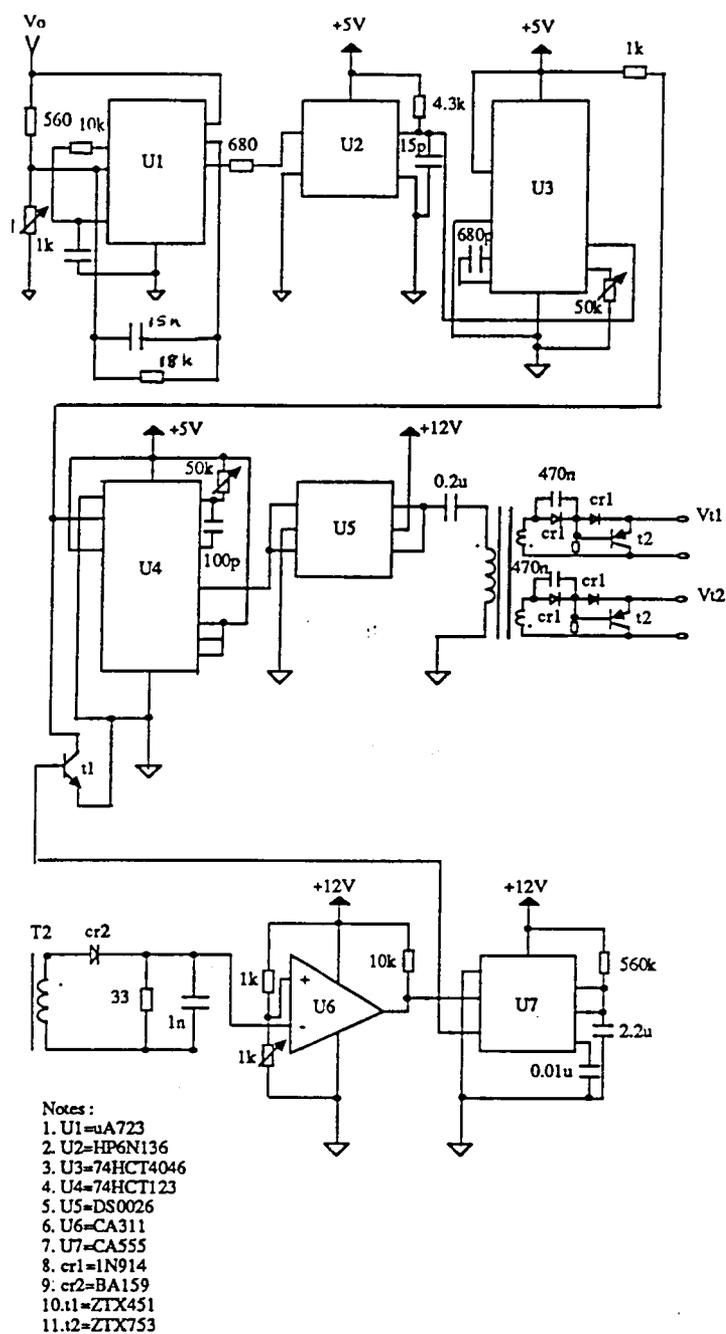


Fig.6.7 Simplified control circuit schematic

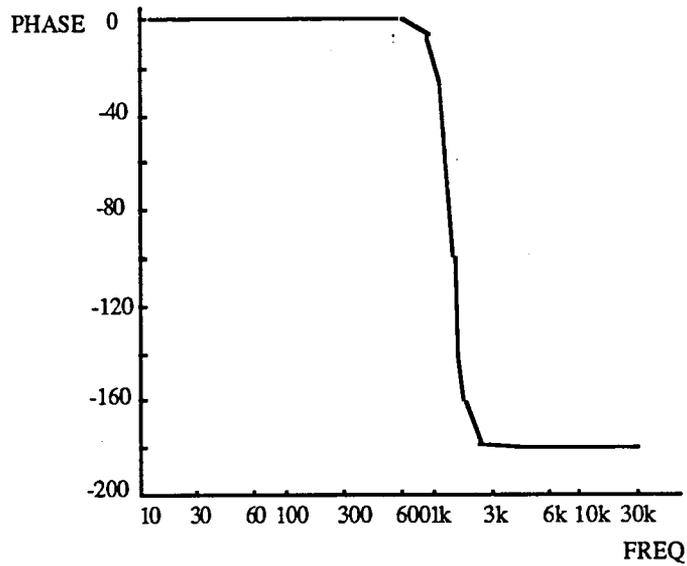
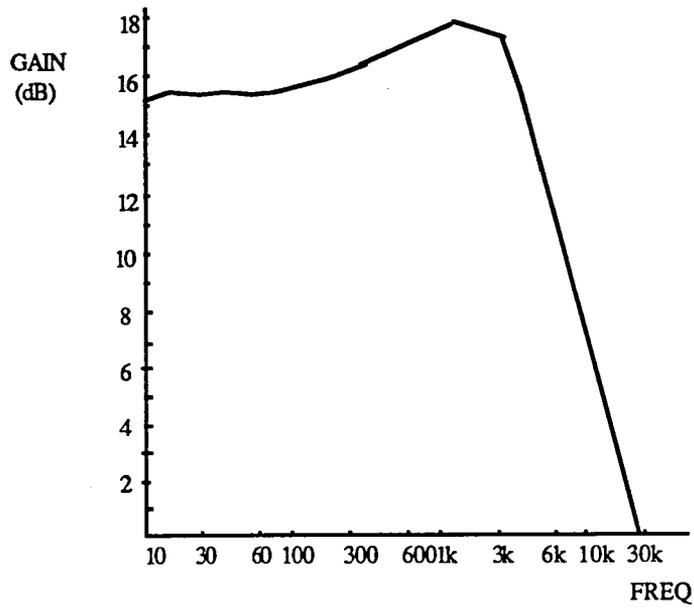


Fig.6.8 Bode plots of the open loop system

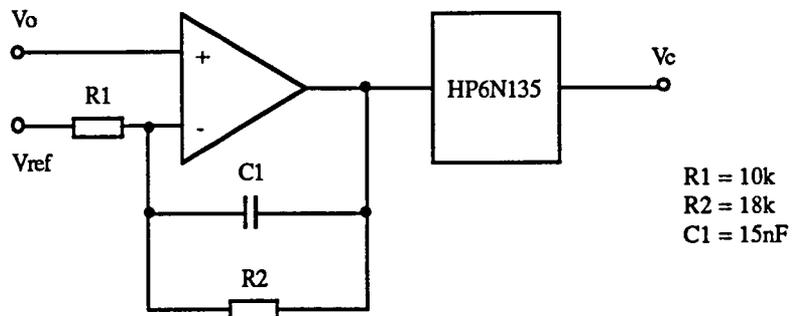


Fig.6.9 Compensation network

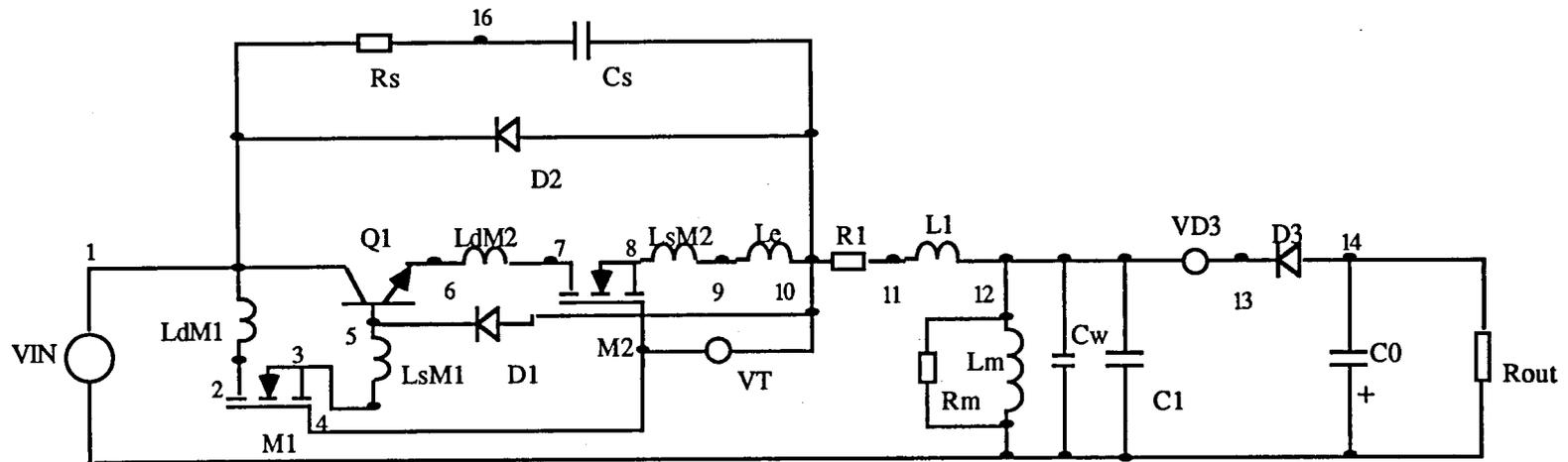


Fig.6.10 A computer model of the flyback converter

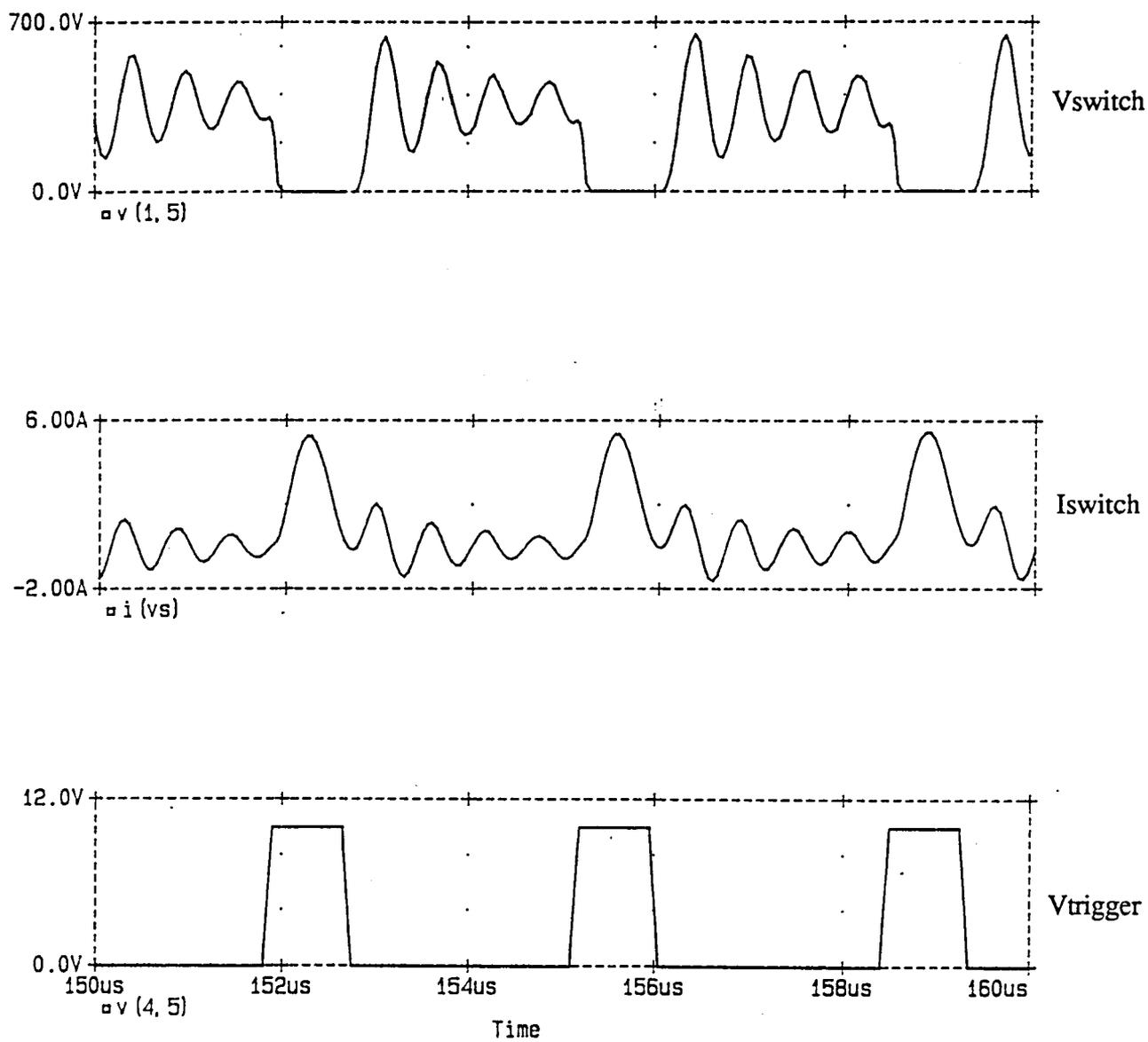


Fig.6.11a Simulated waveforms of the converter. $V_{\text{in}}=190\text{Vac}$, $f_s=300\text{kHz}$

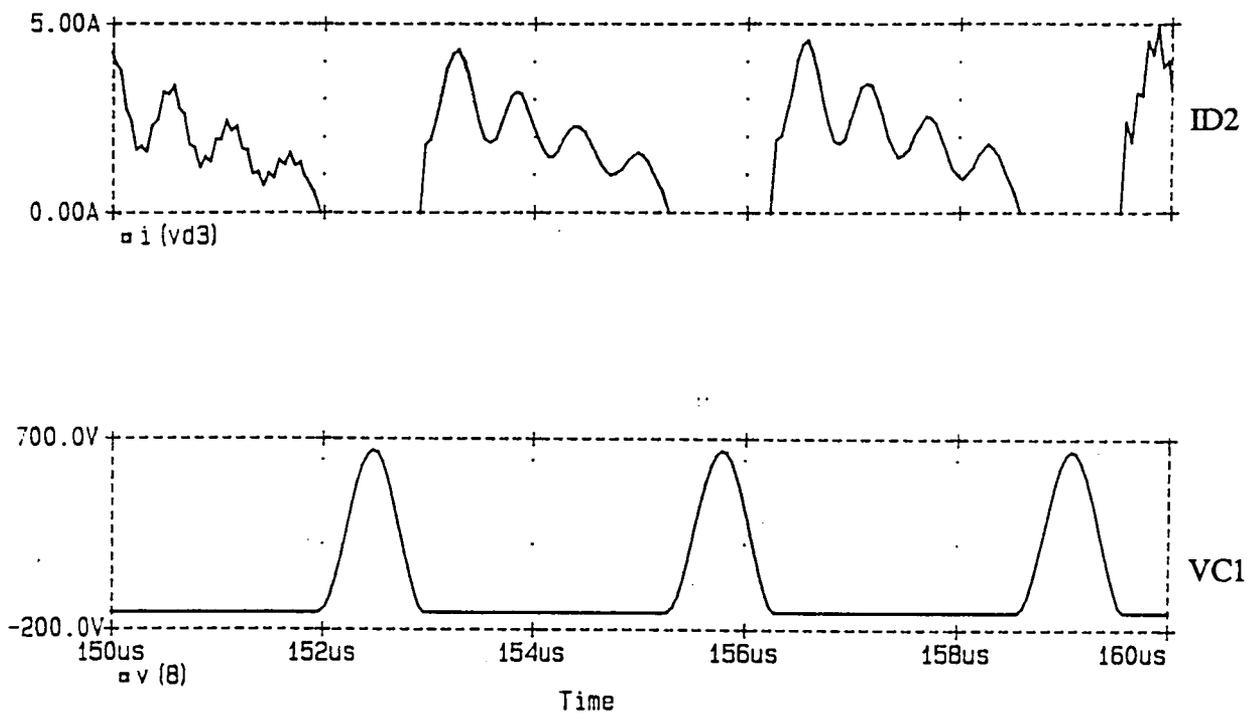


Fig.6.11b Simulated waveforms of the converter. $V_{in}=190V_{ac}$, $f_s=300kHz$

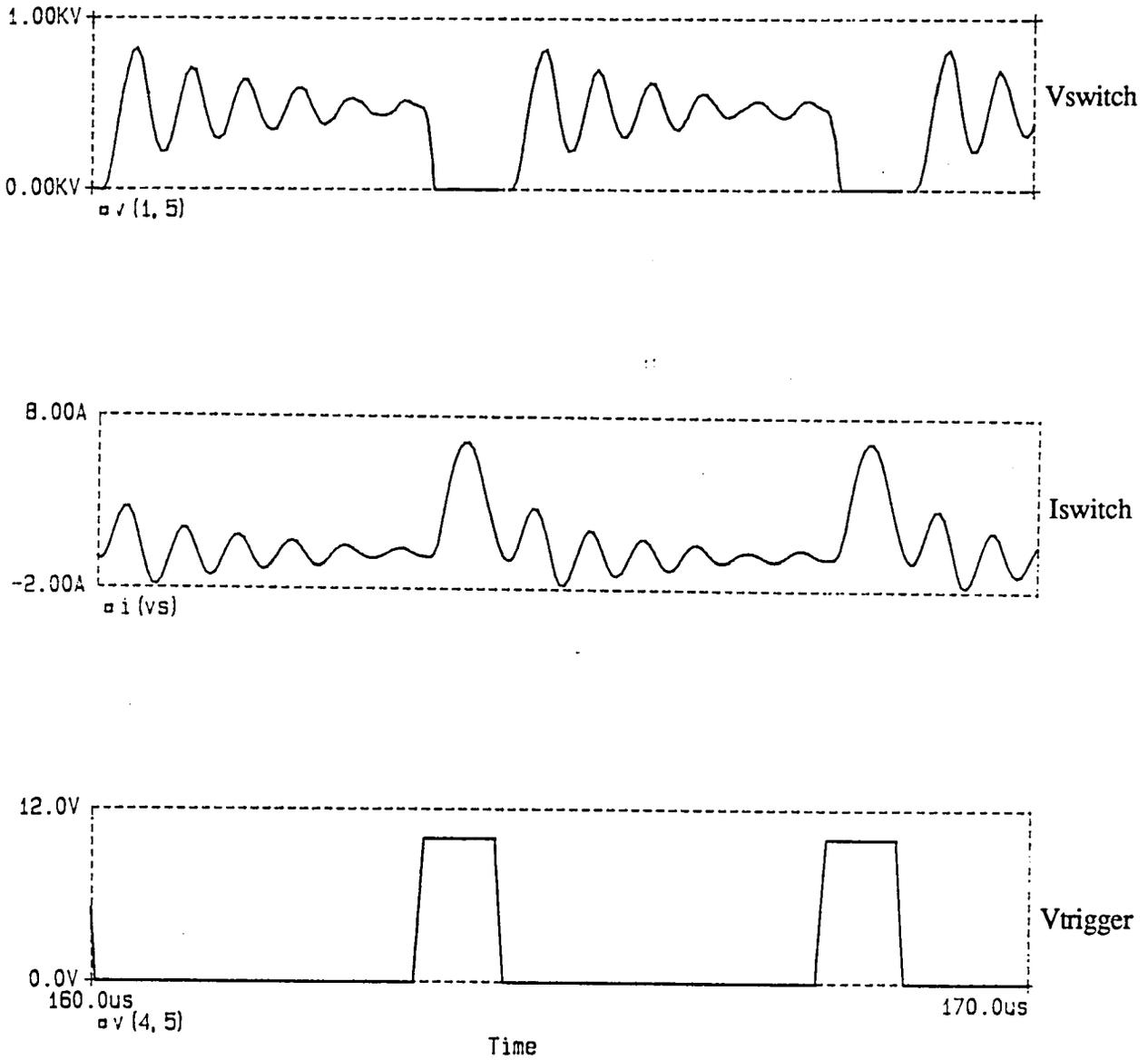


Fig.6.12a Simulated waveforms of the converter. $V_{in}=270\text{Vac}$, $f_s=232.4\text{kHz}$

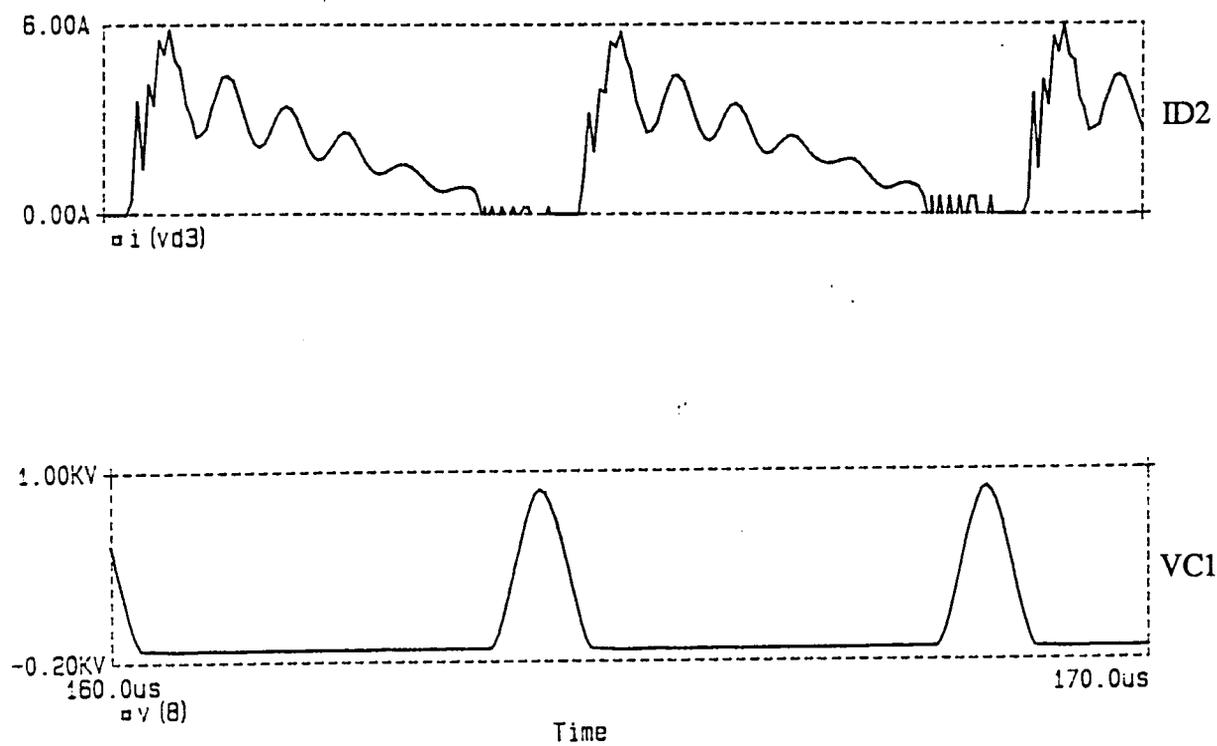


Fig.6.12b Simulated waveforms of the converter. $V_{in}=270V_{ac}$, $f_s=232.4kHz$

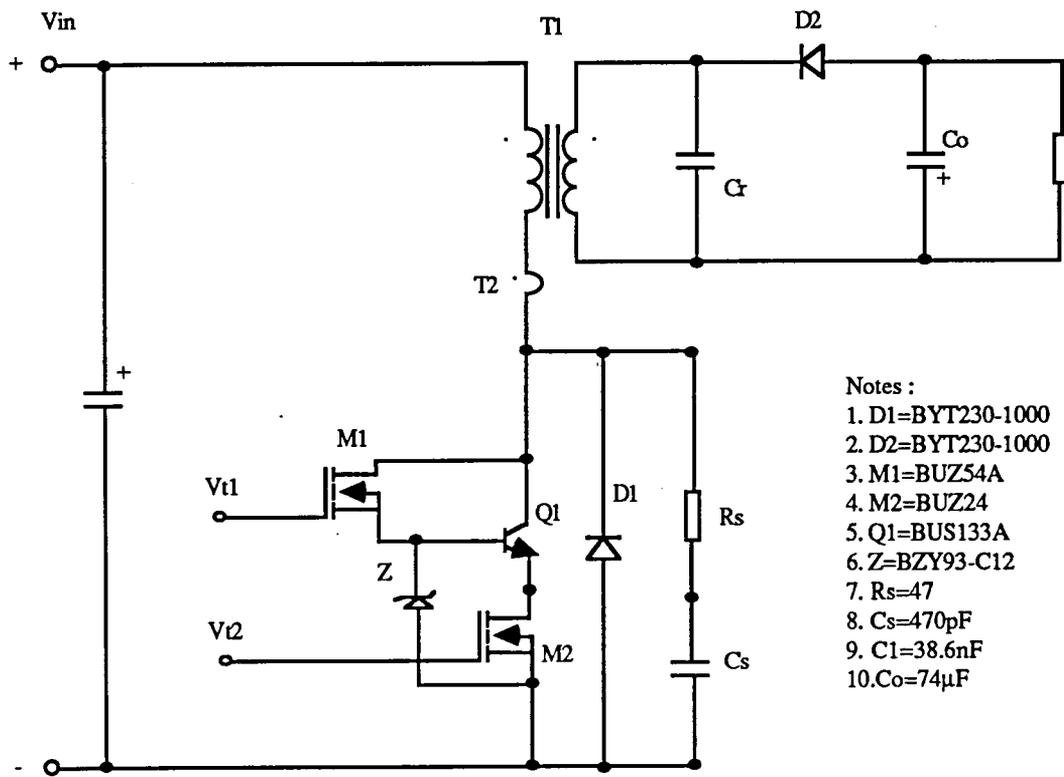


Fig.6.13 Power stage schematic

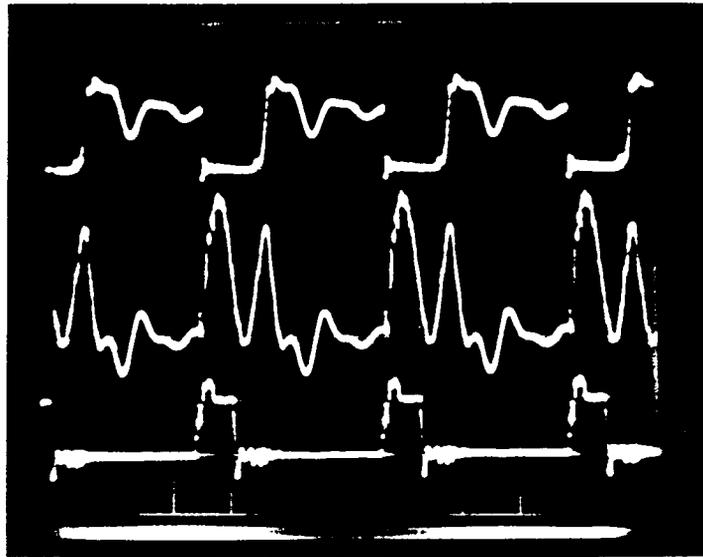


Fig.6.14 Experimental waveforms of the converter. $V_{in}=190V_{ac}$, $f_s=300kHz$

Top trace : V_{switch} 500V/div, $1\mu s/div$

Middle trace : I_{switch} 2A/div, $1\mu s/div$

Bottom trace : V_{gate} 10V/div, $1\mu s/div$



Fig.6.15 Experimental waveforms of the converter. $V_{in}=190V_{ac}$, $f_s=300kHz$

Top trace : $ID2$ 20A/div, $1\mu s/div$

Bottom trace : $VC1$ 10V/div, $1\mu s/div$

CHAPTER 7**A ZERO-CURRENT SWITCHING QUASI-RESONANT FLYBACK CONVERTER
WITH POWER FACTOR CORRECTION**

A 200W zero-current switching quasi-resonant flyback converter with power factor correction is presented in this chapter. Included is a description of the design and building of both the input voltage modulation and power stage circuits. The chapter is concluded with an evaluation of the overall converter performance.

7.1 DESIGNING OF THE CONVERTER

7.1.1 Power circuit design

As in the previous chapter, the design is first carried out for the buck-boost circuit shown in Fig.7.1. The input/output requirements of the buck-boost circuit are as follows [1],

Input voltage range	: 170Vdc-340Vdc
Output voltage	: 120±0.5 Vdc at 0.83-1.66A
Output power range	: 100W-200W
Switching frequency range	: 100kHz-200kHz

The input voltage range corresponds to the peak value and 50% of the peak value of a 240Vac, 50Hz voltage waveform. By maintaining a step-down ratio of 5:1, the output voltage produced will be 24V at 8.33A on full load. The capacitors C1 and C_O would also be (5)² times the designed values in the practical circuit.

For a maximum switching frequency of 200kHz, the resonant frequency f_r needed to meet the input/output requirements stated above is given by

$$f_r \approx (f_s)_{\max} \frac{(M_{\max} + 1)}{M_{\max}} \approx 483.3\text{kHz} \quad (7.1)$$

The design constraint ξ_c is set at 1.5. The resonant inductance and capacitance is then obtained by rewriting Eqn.6.5 in the previous chapter as

$$L1 = \frac{R_{\min}}{2\pi (f_s)_{\max} \xi_c (1+M_{\max})} = 22.4\mu\text{H} \quad (7.2)$$

and

$$C1 = \frac{\xi_c M_{\max}^2}{2\pi (f_s)_{\max} R_{\min} (M_{\max} + 1)} = 4.84\text{nF} \quad (7.3)$$

With a 5:1 step down ratio, the value of C1 corresponds to 121nF.

The inductance L2 is given by

$$L2 = L1 * \frac{\xi_c}{\xi_f} * [\pi - \cos^{-1}(\frac{1}{1+M_{\max}}) + \sqrt{(2+M_{\max})M_{\max}}] \frac{1}{1+M_{\max}} \quad (7.4)$$

For the 2:1 load range specified above,

$$L2 = 141\mu\text{H} \quad (7.5)$$

For a pk-pk ripple voltage of 1V at the output, the capacitance C_o required is obtained by rewriting Eqn.6.9 as

$$C_o = \frac{I_{L\max}}{2\pi f_{\min} V_{\text{ripple}}} = 2.95\mu\text{F} \quad (7.6)$$

with a maximum permitted ESR of

$$\text{ESR}_{\max} = \frac{V_{\text{ripple}}}{I_{\text{Dpk}}} = 0.445\Omega \quad (7.7)$$

where I_{Dpk}, the peak current through the rectifying diode D2, is 2.25A. With a 5:1 step down ratio, C_o corresponds to 73.7μF with a maximum permitted ESR of 17.8mΩ.

7.1.2 Input voltage modulation circuit design

The N_p/N_m step down ratio between the primary winding and the secondary winding connected to the modulation circuit is obtained as follows (see Fig.7.2). The peak voltage across the primary winding during switch conduction mode is equal to the peak line voltage. To obtain 50% of this value across the modulating capacitor C_e, the following condition has to be met, namely

$$N_p / N_m = 2 \quad (7.8)$$

The forward voltage drop across the diode D3 is neglected in this derivation.

The magnitude of C_e is determined by the minimum input voltage, the power circuit is designed to operate at. The modulating capacitor C_e provides power to the output for 3.33ms (60 degrees) during each line cycle. Assuming that the total output power (during the entire line cycle) is provided by C_e , the discharge current, $I_{\text{discharge}}$ needed is given by

$$I_{\text{discharge}} = \frac{\text{Output power}}{\text{Minimum Input Voltage}} = 1.176\text{A} \quad (7.9)$$

For a pk-pk ripple voltage of 4V,

$$C_e = \frac{I_{\text{discharge}} * \text{Discharge time}}{V_{\text{ripple}}} \approx 1000\mu\text{F} \quad (7.10)$$

7.2 CONSTRUCTION OF THE CONVERTER

7.2.1 Transformer design and construction

The transformer is again designed to operate at a flux density that is slightly below the saturation flux density of the core. An ETD-49 type transformer core in 3F3 type ferrite material is used in the prototype circuit, with 20 turns on the primary and an airgap of 0.75mm. The peak working flux density is taken as 0.29T. The magnetising inductance is again set at 141 μ H, which was the designed value of the filter inductance L2.

Both the primary and the 10 turns of winding feeding the modulating circuit are made up of a number of 0.25mm diameter copper wires, which are twisted together. 4 turns of 0.25mm thick copper foil is used as the secondary winding.

The leakage inductance arising due to all three windings is used to represent the resonant inductor L1 in the buck-boost circuit.

7.2.2 Power and modulating circuit construction

The power and modulating circuits are constructed using the component values shown in Fig.7.3. The diodes D1-D4 are ultra-fast recovery types. D3 has a high voltage rating to prevent the spikes that appear across it (due to its reverse recovery characteristics) from damaging it. A snubber circuit is again not needed across the output rectifying diode D2, due to the low voltage stress on it. The snubber capacitor across the switching device is selected for a 6.3% loss in the snubber circuit. As stated in the previous chapter, these losses are maximum at the highest supply voltage, at which point $V_S = 502V$ and $f_S = 100kHz$. Therefore for a 12.6W snubber loss, $C_S \approx 1nF$. An RC snubber combination of 33Ω and $1000pF$ is therefore connected across the anti-parallel diode D1 to reduce the effects of its "snap" reverse recovery characteristics.

The control and overcurrent protection circuitry remain the same as before.

7.3 EVALUATION OF THE POWER STAGE PERFORMANCE DATA

Fig.7.4 shows the input voltage and current waveforms of the converter when operating under full load conditions. The voltage is a sine wave while the current is a first order square wave. The slight ripple at the top and bottom portions of the current waveform is caused as a consequence of charging the capacitor C_e during these times.

The converter has a full load efficiency of 80%, which drops to 71% at 100W. The loss in efficiency when lightly loaded is due mainly to the increase in conduction losses in the anti-parallel diode D1 across the switch. The input power factor was measured at 0.936 on full load and remained approximately the same over the entire load range specified. All the measurements were taken with a Voltech PM1000 type AC Power Analyzer.

A frequency spectrum of the input current waveform is shown in Fig.7.5. The measurements were taken with a Tektronix A6302 type current probe, a AM503 type current probe amplifier and a HP3582A type spectrum analyzer. The even harmonics present in the waveform are negligible. The odd harmonics when expressed as a percentage of the 50Hz fundamental frequency are as follows,

Fundamental	-	100%
-------------	---	------

3 rd Harmonic	-	18%
5 th Harmonic	-	13.5%
7 th Harmonic	-	10%
9 th Harmonic	-	4.6%
11 th Harmonic	-	less than 1%

7.4 CONCLUDING REMARKS

The concept of using an inexpensive and simple power factor correction circuit in off-line power converters was demonstrated successfully in this chapter. The 3rd harmonic of the input current, when expressed as a percentage of the fundamental, was well below the 26% specified in VDE0712, Part 2. The input power factor was however, below the theoretically predicted value of 0.942 (calculated in Chapter 2), due to the wattmeter reading the total available voltage and only the current flowing into the converter.

The use of a zero-current switching quasi-resonant flyback converter as the main power stage of the circuit, gave the ability to process moderate levels of output power at high frequencies, thereby providing a supply with a high power/weight ratio. The magnitude of the switching frequency was relatively low due to the high leakage inductance arising from two secondary windings in the transformer. This high leakage inductance however, overcame the need for an extra magnetic component that would otherwise have been needed to prevent a sudden inrush of current into C_e .

7.5 REFERENCES

1. **Amarasinghe, K.A. and Manning, C.D.**, 1990, "Zero-current switching quasi-resonant flyback converter with power factor correction", to be presented at the Power Conversion and Intelligent Motion Conference, Munich, West Germany.

7.6 FIGURES

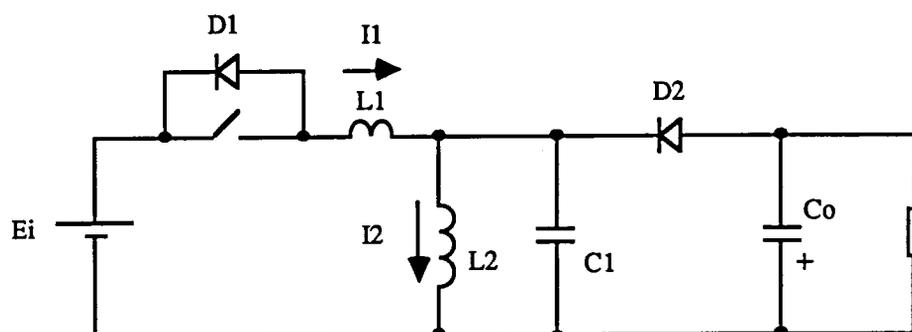


Fig.7.1 A simplified equivalent circuit of the zero-current switching quasi-resonant flyback converter

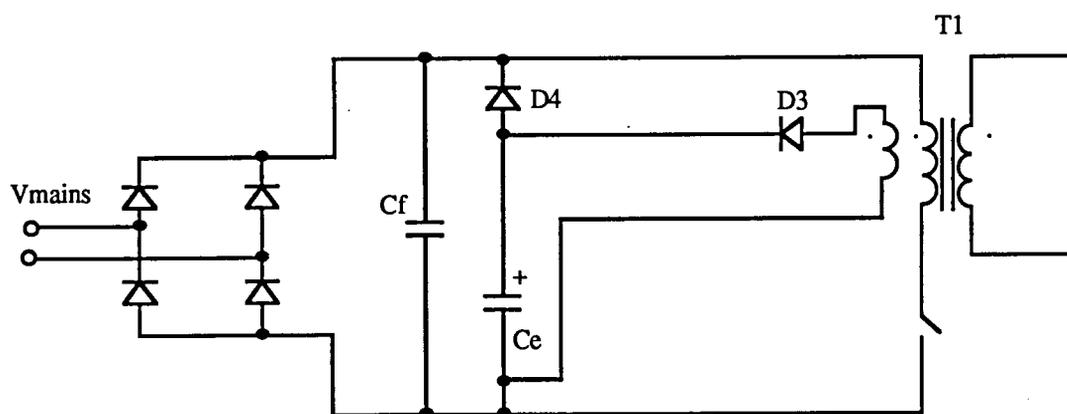


Fig.7.2 Input voltage modulation circuit

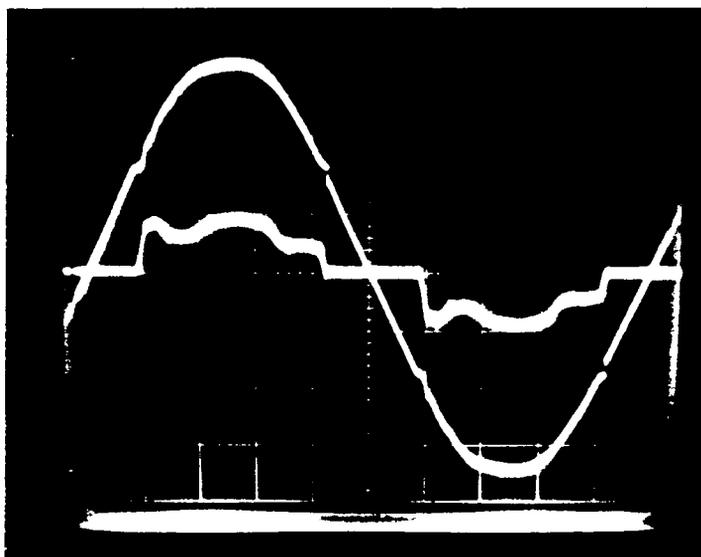


Fig.7.4 Experimental waveforms of the converter on full load (200W)

Top trace : Input voltage 100V/div, 2ms/div

Bottom trace : Input current 2A/div, 2ms/div

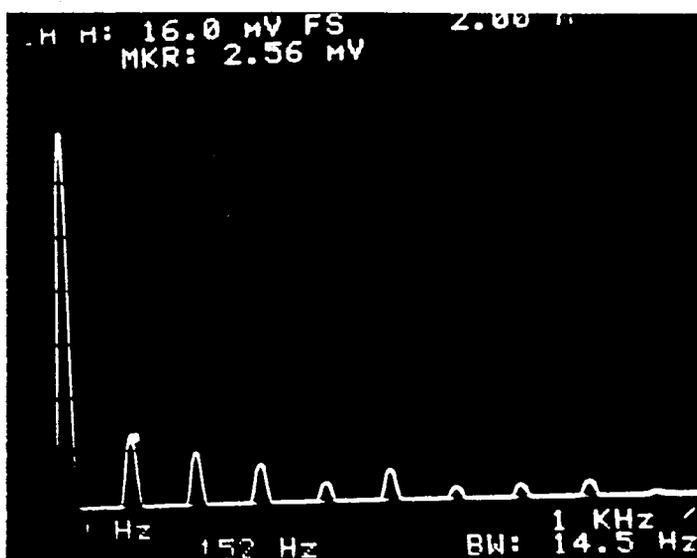


Fig.7.5 Frequency spectrum of the input current on full load (200W)

CHAPTER 8

CONCLUSIONS

The achievements of the work are outlined. Recommendations for further improvements are given.

Switching-Mode Power Supply (SMPS) technology has made vast progress in the last two decades. As a result of better devices and components, better understanding of the topology and behavior of power converter circuits, significant improvements can be found in every facet of the SMPS ; reduction in weight and size, improvement in efficiency, reduction in the level of EMI produced, reliability and stability, increase in the dynamic response and high input power factor and low line current distortion amongst others.

Still, when compared to the signal and data processing electronic circuits these SMPS's are supporting, the reduction in size and weight of SMPS's appears far less dramatic, especially in the high input power factor and low line current distortion area. With the advent of Very Large-Scale Integrated Circuits (VLSI) and High-Speed Integrated Circuits, the demand for power factor corrected SMPS's with high power density and fast dynamic response will be even greater.

One unique feature of the SMPS is that it is designed to process a large amount of power efficiently. To achieve the functions of power factor correction and line distortion reduction, power conversion, dc isolation, ripple-filtering and noise suppression without sacrificing efficiency, a SMPS circuit must rely on the extensive use of magnetic and capacitive components. Consequently, it is reasonable to conclude that the most effective way to increase the power density is to reduce the size of magnetic and capacitive components, by designing the SMPS to operate at very high frequencies.

However, in the attempt to increase the operating frequency, we encounter two major difficulties ; high switching stresses and high switching losses. The source of these difficulties is due to switching at high speeds in the harsh environment of a SMPS circuit where the power switching devices are often turned on under a capacitive load condition and turned off under an inductive load condition. These switching stresses and losses place a heavy burden on the power semiconductor devices.

In recent years, much effort has been made in search for topological improvements to SMPS circuits. Particularly, the resonant converter technology and the zero-current switching technique have made a significant impact. In this work, these techniques have been employed in active power factor correction circuits. Based on the concept of current mode resonant switches, two circuits have been developed for power levels up to 200W (suitable for mobile applications) and for power levels greater than 200W (for preregulation applications).

The preregulator circuit, developed from the conventional boost topology, used the concept of fixed frequency operation (dynamic power factor correction), where the line current

"automatically" followed the input voltage, thus providing a power factor close to unity. A smoothed DC output voltage with a small 100Hz rectified mains frequency ripple was produced at the output, with the magnitude of the ripple being determined by the size of the output filter capacitor used. The employment of a single high speed GTO device in a "circuit commutated mode" (as a fast thyristor), provided an efficient and reliable method of processing high output power levels at high frequencies. Furthermore, the built in isolation transformer in the circuit provided a means of obtaining any output voltage within reason. This would relieve any downstream converters of isolation requirements. Isolated feedback can also be eliminated in these downstream converters, making it easy and inexpensive to achieve good regulation.

Probably the greatest disadvantage of this resonant circuit however, is its inability to provide even higher input power factors (> 0.99) by reducing the level of distortion on the line current waveform. This problem is exclusive to boost type converter circuits employing the dynamic power factor correction control technique. A viable solution would be the implementation of a control technique where the preregulator is programmed to draw a sinusoidal input current, in phase with the line voltage, the current being controlled by the deviation of the output voltage from the desired value. The input current programming signal may be obtained by multiplying a half-sinusoid (usually derived from the rectified line voltage waveform) with a control voltage, which must be constant during each half-cycle. The control voltage represents the deviation of the output voltage from its desired value.

The power density of a supply is more crucial in mobile applications. Therefore in pursuit of even higher switching frequencies, but at lower power levels, the GTO thyristor had to be replaced with a switch which consisted of a cascoded combination of a bipolar transistor and a high and low voltage power MOSFET. Furthermore, these applications require a better regulated output voltage with a smaller ripple, while maintaining a high input power factor. The dynamic power factor correction technique was therefore replaced with a novel input voltage modulation technique (the circuit draws line current for only 120 degrees of the 180 degree line cycle), which maintains a high input power factor (0.93-0.94) while using the control circuit in the supply for providing better output voltage regulation. The newly developed isolated resonant boost circuit was also abandoned in preference to the zero-current switching quasi-resonant flyback topology (uses less magnetic components). The ensuing power supply is inexpensive and simple, making it ideal for mobile applications.

Computer simulation has become an ideal tool for evaluating and optimizing circuits today. It permits the design and analysis of circuits, that cannot be expeditiously or economically

done in any other way. Furthermore, semiconductor devices could be accurately modelled over their full range of operation using today's computer programs. Circuit yield can therefore be enhanced by testing new designs using devices which simultaneously exhibit all worst-case specification parameters.

The PSpice computer program was used for analysing the power factor corrected resonance circuits here. When doing so, an equivalent circuit model which replicated the action of a GTO thyristor had to be produced, since PSpice did not have built-in models for this device. A well-established two-transistor model, used for modelling SCR's, was therefore adopted for modelling the GTO behaviour. The new model enables the user to estimate model parameters with ease, by adopting a short calculation and graphical design procedure, based on the manufacturer's data sheets. Furthermore, improvements needed for the built-in MOSFET models in PSpice were also outlined, especially when analysing high frequency circuits.

To conclude, this dissertation has made a significant step towards the development of alternative techniques for high performance, high power density power factor correction circuits. It provided two promising circuit topologies for alleviating low input power factors and line current distortion, whilst simultaneously maintaining low switching stresses and losses in the semiconductor devices. This enabled the switching frequency to be pushed to high values, thus fulfilling the most important requirement for achieving miniaturisation.

APPENDICES

APPENDIX 1

MODEL PARAMETERS OBTAINED USING THE PARTS PROGRAM

A.1.1 BYT230PIV-1000

IS = 287.4E-18, RS=9.476E-3, BV=1000, IBV=100E-6, CJO=1E-12, VJ=0.75,
M=0.3333, FC=0.5, TT=63.72E-9

A.1.2 BZY93-C10

IS=325.1E-27, RS=0, BV=9.974, IBV=0.3695, CJO=1E-12, VJ=0.75,
M=0.3333, FC=0.5, TT=5E-9

A.1.3 BUS133A

IS=49.56E-12, VAF=100, BF=20.8, NE=2.366, ISE=113.1E-9, IKF=32.72,
XTB=1.5, BR=1.488E-3, NC=2, ISC=0, IKR=0, RC=0, CJC=971.6E-12,
VJC=0.75, MJC=0.3333, FC=0.5, CJE=5E-9, VJE=0.75, MJE=0.3333,
TR=2.03E-3, TF=1E-9, ITF=0, VTF=0, XTF=0

A.1.4 BUZ24

LEVEL=3, GAMMA=0, DELTA=0, ETA=0, THETA=0, KAPPA=0, VMAX=0,
XJ=0, TOX=100n, UO=600, PHI=0.6, Rs=53m, KP=20.81u, W=1.5, L=2u,
VTO=3.575, RD=0, RDS=5MEG, CBD=3.18n, PB=0.8, MJ=0.5, FC=0.5,
CGSO=1.41n, CGDO=518.5p, RG=17.95, IS=1E-30

A.1.5 BUZ54A

LEVEL=3, GAMMA=0, DELTA=0, ETA=0, THETA=0, KAPPA=0, VMAX=0,
XJ=0, TOX=100n, UO=600, PHI=0.6, RS=67.43m, KP=20.48u, W=0.41,
L=2u, VTO=3.119, RD=2.197, RDS=50MEG, CBD=686.7p, PB=0.8, MJ=0.5,

FC=0.5, CGSO=9.558n, CGDO=148.3p, RG=49.59, IS=1E-30

APPENDIX 2

PROGRAM LISTING USED TO SIMULATE THE DYNAMIC RESPONSE OF POWER
MOSFETs

DYNAMIC RESPONSE

.OPTIONS ITL5=0 LIMPTS=5000

VDD 1 0 DC 100

RD 1 2 3.3

LD 2 3 5E-9

M1 3 4 5 5 IRF250

RG 6 4 6.2

VG 6 0 PULSE (0 10 0 0 0 1U 2.5U)

LS 5 0 13E-9

.MODEL IRF250 NMOS (LEVEL=3 GAMMA=0 DELTA=0 ETA=0 THETA=0

+ KAPPA=0 VMAX=0 XJ=0 TOX=100n UO=600 PHI=0.6

+ RS=26.43m KP=20.65u W=1.5 L=2u VTO=3.435

+ RD=32.81m RDS=640k CBD=3.095n PB=0.8 MJ=0.5

+ FC=0.5 CGSO=4.271n CGDO=181.4p RG=6.931 IS=44.42n)

.TRAN 1E-8 1E-5 0 1E-9

.PROBE

.END

APPENDIX 3

GTO MODEL PARAMETERS

A.3.1 DETERMINING MODEL PARAMETERS

The parameters required refer almost exclusively to the two transistors in the model. PSpice contains a very detailed transistor model which has over 40 parameters to fully define the transistor operation. However, all these parameters are not required to provide an adequate model of the GTO. The following reference data is required. Values in the parentheses are obtained from data sheets for a Mullard BTW58-1300R type GTO device.

1. Gate triggering current, I_{GT}	(0.2A)
2. Latching current, I_L	(1A)
3. Delay time, t_d	(0.25 μ s)
4. Rise time, t_r	(1 μ s)
5. On-state device voltage drop, V_T	(3V)
6. On-state resistance, R_{ON}	(0.6 Ω)
7. Turn-off time, t_q	(750ns)
8. Max. rate of change of voltage, dv/dt	(1.5kv/ μ s)
9. Forward breakover voltage, V_{beo}	(1300V)

A.3.1.1 Value of R1

R1 sets the magnitude of the gate trigger current and can be found from

$$R1 = 0.75 / I_{GT} = 3.75 \Omega$$

A.3.1.2 D1 parameters

The diode D1 is used to set the forward breakover voltage (V_{beo}) of the GTO. The reverse breakdown voltage of the diode is equal to the V_{beo} required.

Therefore,

$$V_B = V_{beo} = 1300V$$

A.3.1.3 Q2 parameters

The Q2 parameters required are BF (forward β), IS (transport saturation current) and CJC (base-collector zero depletion capacitance).

Set α_2 to 0.9

$$BF = \alpha_2 / 1 - \alpha_2 = 9$$

$$IS = 10^{\frac{-(VT+0.74)}{0.11}} = 1 * 10^{-34} \text{ A}$$

$$CJC = 0.4 I_L \left(\frac{ton}{dv/dt} \right)^{0.5} \quad \text{where } ton = t_r + t_d$$

$$= 11.55 \text{ nF}$$

A.3.1.4 Q1 parameters

The following parameters are required for the transistor Q1, BF (forward β), BR (reverse β), IS (transport saturation current), RE (emitter resistance), TF (forward transit time) and TR (reverse transit time).

$$\alpha_1 = 1 - \alpha_2 + \frac{I_{GT}}{\alpha_2 * I_L}$$

$$BF = BR = \frac{\alpha_1}{1 - \alpha_1} = 0.475$$

IS = same as value calculated for Q2 = $1 * 10^{-34}$

RE = $R_{ON} = 0.6 \Omega$

TF = $\frac{(\beta_1 * \beta_2 - 1) \tau_r}{1.8 \beta_1} = 202 \text{ ns}$

TR = $9\tau_q = 6.75 \mu\text{s}$

A.3.2 Two transistor GTO model

```
R1 2 3 3.75
D1 2 4 DMOD
Q1 2 4 1 QMOD1
Q2 4 2 3 QMOD2
.MODEL DMOD D (BV=1300)
.MODEL QMOD1 PNP (BF=0.475 BR=0.475 IS=1E-34 RE=0.6 TF=2.02E-07
+
          TR=6.75E-06)
.MODEL QMOD2 NPN (BF=9 IS=1E-34 CJC=11.55E-09)
```

A.3.3 Program listing used to simulate the turn-on characteristics of the GTO model

```
RESISTIVE LOAD TEST CIRCUIT
.OPTIONS ITL5=0 LIMPTS=5000
VDD 1 0 DC 250
RD 1 2 50
VS 2 3 0
X1 3 4 0 GTOMOD
RG 5 7 5
VT 7 4 0
VG1 6 5 PULSE (0 6.25 10U 0 0 1U 25U)
VG2 6 0 PULSE (0 5 0 0 0 10U 25U)
```

```

.SUBCKT GTOMOD 1 2 3
R1 2 3 3.75
D1 2 5 DMOD
Q1 2 4 1 QMOD1
Q2 4 2 3 QMOD2
.MODEL DMOD D (BV=1300)
.MODEL QMOD1 PNP (BF=.475 BR=.475 IS=1.0E-34
+
RE=.6 TF=2.02E-7 TR=6.75E-6)
.MODEL QMOD2 NPN (BF=9 IS=1.0E-34 CJC=11.5E-9)
.ENDS
.TRAN 1E-6 50E-6 0 1E-7
.PROBE
.END

```

A.3.4 Program listing used to simulate the turn-off characteristics of the GTO model

```

INDUCTIVE LOAD TEST CIRCUIT
.OPTIONS ITL5=0 LIMPTS=5000
VDD 1 0 DC 1300
RD 1 2 260
LD 2 3 10E-6
VS 3 9 0
X1 9 4 0 GTOMOD
RG 5 7 2
LG 7 4 1E-6
VG1 6 5 PULSE (0 10 10U 0 0 5U 25U)
VG2 6 0 PULSE (0 5 0 0 0 10U 25U)
D1 0 3 DMOD
LS 3 8 .25E-6
CS 8 0 3333E-12
.MODEL DMOD D
.SUBCKT GTOMOD 1 2 3
R1 2 3 3.75
D1 2 5 DMOD
Q1 2 4 1 QMOD1
Q2 4 2 3 QMOD2
.MODEL DMOD D (BV=1300)

```

```
.MODEL QMOD1 PNP (BF=.475 BR=.475 IS=1.0E-34  
+ RE=.6 TF=2.02E-7 TR=6.75E-6)  
.MODEL QMOD2 NPN (BF=9 IS=1.0E-34 CJC=11.5E-9)  
.ENDS  
.TRAN 1E-6 50E-6 0 1E-8  
.PROBE  
.END
```

APPENDIX 4

PROGRAM LISTING USED TO SIMULATE THE DYNAMIC POWER FACTOR
CORRECTED RESONANT CONVERTER

300W MODEL

.OPTIONS ITL5=0 LIMPTS=5000 RELTOL=0.1 ABSTOL=1E-3 ITL4=40

VIN 1 3 SIN (0 340 50 0 0)

DA 1 2 DMOD

DB 3 2 DMOD

DC 0 3 DMOD

DD 0 1 DMOD

RF 2 4 .23

LF 4 5 1.5E-3

CF 4 5 41E-12

RD 5 0 270K

CI 5 0 1E-6

R0 5 6 .4

L0 6 7 3E-3

C0 6 7 33.4E-12

VX1 7 8 0

D1 8 9 BYT230

X1 9 10 0 GTOMOD

RG 11 10 2.2

VG1 12 11 PULSE (0 8 4U 0 0 8.5U 12.5U)

VG2 12 0 PULSE (0 8 0 0 0 4U 12.5U)

CSN 8 21 1.65E-9

RSN 21 0 100

CB1 7 13 200E-9

RK 13 14 .875

LK 14 15 37.6E-6

RM 15 0 .11MEG

LM 15 0 16.5E-3

C1 15 0 50.4E-12

CB2 15 16 151.85E-9

CS 16 0 19E-9

D2 16 17 BYT230

```
D3 18 17 BYT230
D4 0 18 BYT230
D5 0 16 BYT230
RO 17 19 1.55
CO 19 0 771.6E-6
ROUT 17 0 675
.MODEL DMOD D
.MODEL BYT230 D (IS=287.4E-18 RS=9.476E-3 BV=1000 IBV=100E-6 CJO=1E-12
+           VJ=0.75 M=0.3333 FC=0.5 TT=63.72E-9)
.SUBCKT GTOMOD 1 2 3
R1 2 3 3.75
D1 2 4 DMOD
Q1 2 4 1 QMOD1
Q2 4 2 3 QMOD2
.MODEL DMOD D (BV=1300)
.MODEL QMOD1 PNP (BF=0.475 BR=0.475 IS=1E-34 RE=0.6 TF=2.02E-07
+           TR=6.75E-06)
.MODEL QMOD2 NPN (BF=9 IS=1E-34 CJC=11.55E-09)
.ENDS
.PROBE
.TRAN 1E-6 7.9M 7.75M .5E-6
.END
```

APPENDIX 5

**PROGRAM LISTING USED TO SIMULATE THE ZERO-CURRENT SWITCHING
QUASI-RESONANT FLYBACK CONVERTER**

QUASI-RESONANT FLYBACK CONVERTER

.OPTIONS ITL5=0 LIMPTS=5000 RELTOL=.1 ABSTOL=1E-3 ITL4=40

VIN 1 0 PULSE (0 268.7 0 0 0 1S 2S)

LDM1 1 2 5E-9

M1 2 4 3 3 BUZ54A

LSM1 3 5 12.5E-9

Q1 1 5 6 BUS133A

LDM2 6 7 5E-9

M2 7 4 8 8 BUZ24

LSM2 8 9 12.5E-9

LE 9 10 100E-9

D1 10 5 BZY93

VT 4 10 PULSE (0 10 0 0 0 0.8U 3.33U)

D2 10 1 BYT230

RS 1 16 47

CS 16 10 470E-12

R1 10 11 .255

L1 11 12 17.6E-6

LM 12 0 98.56E-6

RM 12 0 .8MEG

CW 12 0 18.38E-12

C1 12 0 1.544E-9

VD3 13 12 0

D3 14 13 BYT230

CO 0 14 2.96E-6

ROUT 0 14 57.6

.MODEL BYT230 D (IS=287.4E-18 RS=9.476E-3 BV=1000 IBV=100E-6 CJO=1E-12
+ VJ=.75 M=.3333 FC=.5 TT=63.72E-9)

.MODEL BZY93 D (IS=325.1E-27 RS=0 BV=9.974 IBV=.3695 CJO=1E-12 VJ=.75
+ M=.3333 FC=.5 TT=5E-9)

.MODEL BUS133A NPN (IS=49.56E-12 VAF=100 BF=20.8 NE=2.366 ISE=113.1E-9
+ IKF=32.72 XTB=1.5 BR=1.488E-3 NC=2 ISC=0 IKR=0
+ RC=0 CJC=971.6E-12 VJC=.75 MJC=.3333 FC=.5

```
+          CJE=5E-9 VJE=.75 MJE=.3333 TR=2.03E-8 TF=1E-9
+          ITF=0 VTF=0 XTF=0)
.MODEL BUZ24 NMOS (LEVEL=3 GAMMA=0 DELTA=0 ETA=0 THETA=0
+          KAPPA=0 VMAX=0 XJ=0 TOX=100E-9 UO=600 PHI=.6
+          RS=53E-3 KP=20.81U W=1.5 L=2U VTO=3.575 RD=0
+          RDS=5MEG CBD=3.18E-9 PB=.8 MJ=.5 FC=.5
+          CGSO=2.331E-9 CGDO=141E-12 RG=65.08 IS=1E-30)
.MODEL BUZ54A NMOS (LEVEL=3 GAMMA=0 DELTA=0 ETA=0 THETA=0
+          KAPPA=0 VMAX=0 XJ=0 TOX=100E-9 UO=600 PHI=.6
+          RS=67.43E-3 KP=20.48U W=.41 L=2U VTO=3.119
+          RD=2.197 RDS=50MEG CBD=686.7E-12 PB=.8 MJ=.5
+          FC=.5 CGSO=5.777E-9 CGDO=563.1E-12 RG=32.8
+          IS=1E-30)
.PROBE
.TRAN 1E-7 200E-6 0 5E-8
.END
```

