MICROPROCESSOR CONTROLLED PWM INVERTERS FOR UPS APPLICATIONS

by

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To my parents and wife
for their encouragement, love and affection.

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SYNOPSIS

This thesis describes the implementation of microprocessor controlled single-phase and three-phase inverters for UPS applications. A carrier frequency of 18 kHz is employed in both cases, and the PWM pulses are generated directly by the microprocessor using the regular-sampled symmetric PWM strategy. Single-edge modulation as well as double-edge modulation has been implemented for single-phase and three-phase systems. Since in general, software implementation of PWM strategies require precalculated pulse width values, a scheme is proposed which enables the large quantity of such data to be handled efficiently. The scheme involves the use of a small program for calculating and transferring the data to the memory of the controller.

As the time available to the microprocessor for generating the PWM pulses is only 55.55 μs, two equations have been derived which enable the efficient implementation of the regular-sampled symmetric PWM strategy using single-edge and double-edge modulations. The equations require relatively small computation times and can easily be solved on-line by the microprocessor. The thesis also describes techniques which have been successfully implemented to overcome the problems inherent in microprocessor controlled PWM generators such as interrupt delays and the generation of three-phase waveforms with exact 120^{o} phase displacements. These techniques enable the generation of the PWM pulses in real time with respect to the carrier period without being affected by the time taken by the microprocessor to perform the necessary calculations.

The thesis further describes techniques used for synchronization of the inverter output voltage waveform in time and phase relationship with that of the mains. Frequency synchronization is achieved with the aid of a phase locked loop circuit controlled by the microprocessor. For phase synchronization, phase difference measurements are made in conjunction with the microprocessor and a novel scheme based on a software routine is utilised to ensure phase synchronization with a resolution of 0.5 degree.

Also discussed is the implementation of analogue and analogue/digital PI controllers for regulating the output voltages of the single-phase and three-phase inverters respectively. An experimental method was used to determine the transfer function of the three-phase

system and the information obtained was utilised to construct a model of the system. A software package, SYMBOL2, was then used to design the digital control algorithm which was subsequently implemented by the microprocessor. A description of the techniques used to detect instantaneously any abnormalities in the inverter output waveform and to operate the static bypass switches is also included.

A bread board model consisting of a multi-purpose designed microprocessor board and single-phase and three-phase MOSFET inverters were constructed to assess the performance of the system. The results obtained demonstrate the feasibilities of the schemes proposed and the systems generate good quality sinusoidal output voltage waveforms with low THD and exhibit fast transient responses.

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LIST OF SYMBOLS

V_T	threshold voltage
V_{GS}	gate-source voltage
V_{DS}	drain-source voltage
BV_{DS}	maximum breakdown voltage
T_j	junction temperature
T_A	ambient temperature
dI_D/dt	rate of change of drain current
dV_{DS}/dt	rate of change of drain-source voltage
C_{GS}	gate-source capacitance
C_{DS}	drain-source capacitance
C_{GD}	gate-drain capacitance
PBT	parasitic bipolar transistor
R_G	gate resistance
R_D	drain resistance
R_B	base resistance
w_m	angular frequency of modulating signal
f_R	reference frequency (PLL)
T_{HAj}	jth high level pulse width
X_{LBj}, X_{LAj}	width of low level pulses before and after T_{HAj}
T_{LAj}	jth low level pulse
f_{cmax}	maximum carrier frequency
f_{ck}	counter's clocking frequency
T_c,T	period of carrier signal
ITN_j	jth integer number corresponding to T_{HAj}
ITN_{Dj}	jth integer number corresponding to X_{LBj}
ITN_{Sj}	jth integer number corresponding to T_{LAj}
K_P	proprtional gain in PID controller
K_I	integral gain in PID controller

K_D	derivative gain in PID controller
T_R	ratio of the K_P to K_I
$t_1, t_2, t_3..t_j$	time instants
s	second
T_K	pulse width in suboptimal PWM
MAINAVL	control byte used to indicate whether mains is available or not
FREQCHART	frequency chart in the data segment
M	modulation index
E(t)	error signal
K	proportional gain
CS	code segment
DS	data segment
SS	stack segment
ES	extra segment
THD	total harmonic distortion*
LSI	large scale integration
VSD	variable speed drive
PLL	phase locked loop

* $THD = \sqrt{\sum_{n=2}^{m} (a_n / n)^2} \; / \; a_1$

CHAPTER ONE

GENERAL INTRODUCTION AND ORGANISATION OF THE THESIS

1.1 GENERAL INTRODUCTION

With the increasing use of sophisticated electronic equipment, users have become more aware of common problems caused by the imperfections of the mains power supply. These problems include over/under voltage transients, voltage sags, spikes, noise, frequency aberrations, loss of a few cycles and even complete mains failure, some or all of which can cause the malfunctioning of on-line electronic equipment. The source of the transients, spikes and noise may be other equipment working in the same area. Thunder storms/seismic disturbances can also generate noise which can cause interruptions in the supply lines. The aberration in voltage and frequency could be due to over stretched mains lines particularly during peak hours.

Various types of devices and equipment such as isolation transformers, constant voltage regulators, ferro-resonant transformers, line conditioners etc. are usually used to minimise or eliminate mains disturbances. The above mentioned devices can reduce transients, spikes and absorb high or low voltages with varied degrees of success. However, none of them can regulate the voltage under widely varying load conditions or regulate/control frequency at all and are totally unable to generate missing cycles. To provide complete protection against all the irregularities and disturbances which can be the cause of malfunctioning of the critical loads, the user must turn to the only form of power conditioning devices capable of meeting these requirements, i.e. the Uninterruptible Power Supply (UPS).

During the last decade UPS systems have undergone several major changes, mainly due to the benefit from developments in power semiconductor devices, microprocessors, maintenance-free sealed lead-acid batteries and improvements in control techniques [Khan and Manning - UPEC89]. Thus it has become one of the fastest growing fields of power electronics. UPS systems could be categorised into two types, namely, rotary and static UPS systems. The merits and demerits of both types are described and special emphasis is placed on recent developments in UPS systems such as those employing improved topologies, new devices and control techniques implemented with microprocessors [Khan

and Manning - UPEC89]. These new topologies consist of low impedance rotary UPS [Sachs - 1986], PWM UPS [Hampson - 1982, Rothwell-1985, Huyken et al - 1985], triport UPS [Murata and Harada - 1983, Tominaga et al - 1984] and hybrid UPS systems [Griffith - 1981, Krausse - 1985].

Due to the advancements in power switching device technologies and refinements in PWM techniques, the PWM UPS systems have become one of the most promising research fields in power electronics engineering. The PWM inverter and its control circuits are the most sophisticated part of a UPS system and its design determines its reliability and flexibility, and the quality of the output waveform. The main aims of the PWM inverter are to eliminate as many low order harmonics as possible at the switching stage and to effect control over voltage and frequency with a single power stage.

Improvements in digital LSI/microprocessor technologies have resulted in their frequent use in many fields of power electronics. The immediate advantages of using digital LSI/microprocessor controlled systems are that they increase the flexibility and consistency of the controller. The controller is then devoid of the inherent drawbacks of analogue controllers such as those related to component aging and temperature drift.

The microprocessor controlled implementation of PWM techniques at switching frequencies up to a few kHz have received considerable attention. These PWM generators suffer from some inherent problems associated with microprocessors. These include interrupt delays which introduces a certain degree of distortion in the output waveform and the difficulty of generating three-phase output waveforms with exact 120^{o} phase displacements. Little attention has been given to microprocessor controlled PWM inverters employing ultrasonic carrier frequencies. However, such inverters offer more flexibility in design and can result in a reduction of hardware components and an increase in reliability.

The main objectives of this research are to implement the regular-sampled PWM strategies using single-edge as well as double-edge modulation for single-phase and three-phase inverters employing an 18 kHz carrier frequency using a microprocessor and to investigate and find solutions to the problems inherent in microprocessor controlled PWM generators in general and PWM inverters for UPS applications in particular. In addition, it was intended to implement all the control functions required by such inverters in a single microprocessor.

1.2 ORGANISATION OF THE THESIS

The thesis describes the implementation of a microprocessor controlled single-phase and three-phase PWM inverters employing a switching frequency of 18 kHz. A block diagram of a microprocessor controlled UPS system is shown in Fig. 1.1. Single-edge and double-edge regular sampled PWM strategies have been used to generate PWM pulses for single-phase and three-phase inverters. To synchronise the inverter output with the mains, a PLL circuit is used in conjunction with the microprocessor to achieve frequency synchronisation, and phase synchronisation is performed with the microprocessor by utilising a novel technique. A digital PI control algorithm is utilised to regulate the output voltages.

Chapter Two gives a description of the various UPS systems and discusses their advantages and disadvantages. The different kinds of inverters being used in UPS applications are discussed so as to provide the necessary background to the understanding of various UPS systems. A comparison of power switching devices employed in inverters for UPS applications is presented with emphasis placed on the power MOSFET.

Chapter Three discusses the sinusoidal PWM strategies available in the literature. The problems encountered in generating PWM pulses using high carrier frequencies are discussed followed by an introduction to the microprocessor. The importance of using an 18 kHz carrier signal in UPS applications are discussed. A regular-sampled symmetric PWM strategy is selected for implementation because of its simplicity. Two equations to achieve single-edge and double-edge modulations are derived. Different methods of calculating the look-up tables (LUT) are presented.

Chapter Four is mainly concerned with the microprocessor controlled single-edge and double-edge modulations for single-phase as well as for three-phase PWM generators. The inherent problems in microprocessor controlled PWM generators are discussed together with the solution to overcome these. The construction of single-phase and three-phase inverters are discussed.

Chapter Five specifically deals with the design of the frequency and phase synchronisation

circuitry. A detailed description of phase difference measurement directly in electrical degrees and the implementation of phase synchronisation by the microprocessor is given.

Chapter Six describes the voltage and frequency monitoring techniques used and the calculation of the rate-of-change of frequency by the microprocessor.

Chapter Seven explains in brief, the control systems and frequency domain analysis techniques employed in its design. The chapter also investigates the practical approach to model the transfer function of the open loop system. The complete design of a digital PI controller using frequency response analysis in the w-plane is described together with its implementation by the microprocessor.

Chapter Eight presents general conclusions and some suggestions for future work are also made.

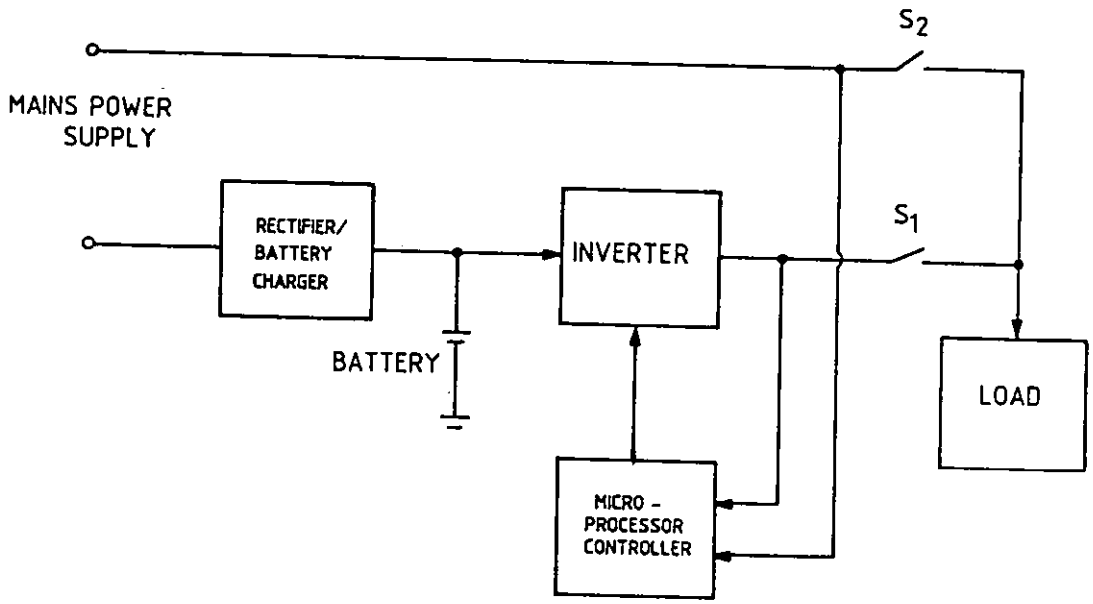


Fig. 1.1 A Microprocessor controlled UPS system.

CHAPTER TWO

UPS SYSTEMS AND POWER SEMICONDUCTOR DEVICES

In this chapter UPS systems are described with their merits and demerits. Static inverters using magnetic and electronic techniques are discussed in detail to highlight their characteristics. In addition, the most commonly used semiconductor devices in the inverter applications are also reviewed emphasizing the power MOSFETs.

2.1 UPS SYSTEMS

Due to the increase in the use of computer systems, process control systems, automatic production lines, telephone exchanges, communication networks etc., the demand for uninterruptible power supplies is increasing. UPSs are the only form of power conditioning devices available that provide protection against all the irregularities and disturbances which can be the cause of malfunctioning of the critical loads. A UPS system may consist of four major components:

i. rectifier/battery charger
ii. bank of batteries
iii. DC to AC inverter
iv. bypass/static transfer switch

The rectifier and inverter units are employed in many combinations to supply a critical load; singly, in parallel, or with a switch backed up by an engine generator set. The particular combination selected is determined by the magnitude of the load power, the pattern of anticipated AC line interruptions and the sensitivity and critical nature of the load.

In general there are two distinct methods by which a UPS can be connected to a critical load. These are categorized into on-line and standby UPS systems. Both configurations use the same number of components but differ in the way these components are connected to the critical load as shown in Figs. 2.1 and 2.2. When the on-line system is operating, the system protects the load from all kinds of aberrations in the mains supply. In the event of mains failure, the system supplies uninterrupted power from the batteries since those are permanently connected at the input of the inverter. In contrast to the on-line system, the

standby system only comes into operation when the mains failure is detected, whereas the load is normally supplied directly or through a line conditioner by the mains.

The standby UPS has the main advantage over the on-line UPS of a higher operating efficiency since it does not have to supply power at all times. The standby UPS therefore has lower running cost but the on-line UPS provides more precise voltage and stable frequency controls. The standby UPS cannot be used in those applications where loads are sensitive to frequency variations because the frequency of the mains power supply cannot be guaranteed. The on-line UPS systems are therefore preferred due to their higher quality of power delivery and reliability.

2.1.1 Rotary UPS

A standard reversible rotary UPS is shown in Fig. 2.3. Its DC/AC converter consists of a DC motor driving an AC alternator with or without a flywheel [Harris - 1987]. Stable frequency operation is achieved by regulating the speed of the DC motor and the output voltage of the alternator is regulated by the use of an automatic voltage regulator. The output voltage waveform and the frequency may be synchronized with that of the mains.

In an alternative scheme, the DC motor is replaced by a static inverter powering a three-phase synchronous motor. Further development of rotary converters includes a synchronous machine in which the motor and the generator windings are located on a single common frame as described by Sachs [1986]. The rotor is DC excited and has a damper winding which provides a low impedance to high frequency harmonic currents. The construction of the machine offers the advantage of a reduction in structural size and weight, avoidance of brushes, improvement of efficiency, reduction of source impedance and increase of system reliability. The system can therefore be regarded as an improved version of the traditional rotary UPS and its low output impedance gives it the ability to handle nonlinear loads without significant distortion in the output voltage waveforms.

2.1.2 Static UPS

In the static UPS system, a static inverter utilising power semiconductor devices is used instead of a motor and alternator. The inverter converts the DC input into AC voltage waveforms by one of the many available switching techniques, the most common of which are pulse width modulation, phase shifting techniques, quasi-square wave techniques and

magnetic techniques. The output voltage generated by these inverters generally requires filtering to reduce the harmonics and to make the waveform sinusoidal.

2.1.3 Rotary Versus Static UPS

Both UPS systems fulfil the same basic requirements of providing a reliable source of regulated power and protect the critical load from surges and brownouts. Their output voltage and frequency characteristics are almost similar and fully compatible with the requirements of the critical loads. However, the rotary UPS systems are less efficient compared to the static systems mainly due to the losses in the rotating machines. The rotary systems require longer recovery times compared to the static systems when they are subjected to step load change. The static system uses a static by-pass facility to deal with large overload currents whereas the rotary systems have the greater ability to provide the large currents required to clear the overload. Static UPS systems are available ranging from a few VA to several hundred kVA whereas rotary UPS systems are available with ratings of 15 kVA and above. The latter are more competitive above 250 kVA.

2.1.4 Batteries

A bank of batteries is invariably used in every UPS system as a reserve DC power source. The batteries are normally a secondary type which means these are electrically rechargeable. Only in a few low power applications are primary type batteries used, which are then discarded after use. The required DC voltage (24 V, 48 V, 60 V etc.) and current ratings are obtained by connecting the batteries in series and parallel combinations. The batteries provide DC input to the inverter when rectifier output voltage drops below the acceptable range.

In choosing a battery for use in UPS applications, several important aspects should be taken into consideration. These include the rate of discharge of the current, the necessary backup time and the acceptable voltage variations. In addition, reliability, environment, space, weight and cost must also be taken into account before making a decision about the type of battery to be employed. The battery size (ampere-hour) determines the time during which power can be drawn from the batteries. This time duration must be adequate either to complete an orderly shut-down of the critical load or to allow an auxiliary power source to come on-line.

For UPS applications, the choice is between two basic battery types, namely, the wet and gelled cell batteries. The wet cell batteries are available in two types; lead-acid and nickel cadmium batteries.

Lead-acid batteries are most commonly used due to their low cost, reliability and excellent performance characteristics in float applications. In the construction [O'Neill - 1984, Linden - 1984] of these batteries, highly reactive sponge lead and lead dioxide is used for negative and positive electrode respectively. A solution of sulphuric acid is used as the electrolyte. When a lead-acid battery discharges, the reactive material in both electrodes is converted into lead sulphate. Since the electrolyte is involved in the reaction, it produces and consumes water at the time of discharging and charging respectively. The state of charge of a lead-acid battery may be determined by measuring the specific gravity or the concentration of electrolyte which increases on charge and decreases at discharge [Linden - 1984].

The most common types of lead-acid batteries are the lead-calcium and lead-antimony batteries. The lead-antimony batteries are equivalent to lead-calcium in terms of current. However, their life span is only half of that of the lead-calcium and require more often equalise charging to retain their capacity. The lead-calcium batteries are more often used because they use water, which means less maintenance, and require a lower floating current [Linden - 1984]. All wet batteries under certain conditions can generate noxious gases therefore, sufficient ventilation arrangements should be made.

Sealed batteries are available in both gelled/absorbed electrolyte constructions but nickel-cadmium are more commonly used. These are alkaline in contrast to the lead-acid batteries. In a charged nickel-cadmium cell, the active materials are trivalent nickel oxide and cadmium for positive and negative electrodes respectively [Linden - 1984]. A solution of potassium hydroxide is used as alkaline electrolyte. Unlike the lead-acid batteries, the measurements of specific gravity does not provide any indication of state of charge in nickel-cadmium batteries. Nickel-cadmium batteries require monthly equalise charging as well as periodic deep discharge cycles to retain their original capacity. They have long life spans (10 years) [Wilson - 1984]. Sealed batteries are generally considered expensive for high power UPS systems but these are widely used in small portable UPS systems. Also these are preferred where improved low temperature operation and/or extremely short duration/high rate of discharge currents are required.

2.1.5 Rectifier/Battery Charger

For on-line UPS systems, the rectifier/battery chargers are used to provide power to the load and charging current required by the batteries. The rectifier/charger unit regulates the DC voltage by varying the firing angle of the SCRs. They employ 6-pulses to reduce the output filtering and to improve the input power factor. An increased number of pulses (12 or 24) per cycle can be achieved by creating additional phases in a transformer for the improvement of the input power factor and current waveforms at the higher ratings [Bobry - 1983]. For low power ratings where the above scheme is not cost-effective, boost circuits or PWM rectifiers can be used [Kocher and Steigherwald - 1982, Biswas et al - 1986, Malesani et al - 1987]. The output filtering can be reduced significantly by utilising PWM schemes but sufficient filtering is still needed so that the inverter can be operated directly from the rectifier's output whilst the batteries are disconnected.

Since the standby UPS systems are usually used for small power applications and do not supply power in normal mode, only a battery charger is required to supply the charging current or trickle charging current to compensate the internal losses of the batteries. The rectifier/chargers using SCRs are recognised as bulky and present low power factor to the mains supply [Manning and Wienberg - 1988]. In addition, it is difficult to obtain optimum constant charging current without the use of a large series inductor. Several battery chargers which are either used as separate battery chargers [Bendien et al - 1984, Lataire and Maggetto - 1985, Manning and Wienberg - 1988] or inverter reversed to charge the batteries [Kawabata et al - 1986, Manias et al - 1987] are available in the literature.

2.1.6 Static Inverters For UPS Applications

The main function of an inverter in conjunction with an output filter is to convert DC into AC voltage. The critical load is normally supplied by an inverter, the design of which determines the quality of the AC power delivered to the load. Thus, the inverter together with its control circuit should be designed to fulfil the following primary requirements.

i. The inverter should be capable of generating a good quality output waveform and the total harmonic distortion should be less than the 5 percent which is acceptable to most of the critical loads.

ii. The output voltage regulation should be within 5 percent (typically 1 percent) with fully charged/discharged state of the batteries.

iii. The transient response of the inverter to the step load change from no load to full load should be less than 5 cycles (typically less than one cycle) with voltage excursion less than 15 percent.

iv. The output frequency must be stable within ±0.005 percent (typically ±0.001percent) and the rate-of-change of frequency should not be more than 0.5 Hz per second.

v. The control circuit for operating the static switch must be capable of detecting any abnormalities in the output frequency and voltage (from the preset limits) in one second (typically after one period) and after one cycle (typically instantaneously) respectively.

vi. The output waveform must be capable of being synchronised with the mains supply within the preset limits (49 to 51 Hz).

Although several kinds of inverters exist in the literature, each meets the above requirements with varied degrees of success. All inverters use semiconductor devices as switching components but differ in the way output voltage regulation is achieved. Several techniques are available to regulate the output voltage. These can be categorised into two groups, namely magnetic techniques and electronic techniques.

2.1.6.1 Inverters Using Magnetic Techniques

The magnetic techniques are those which rely mainly on the magnetic saturation of the output transformer (i.e ferro-resonant inverter) [Patchet - 1954] or output inductors (i.e delta magnetic inverter) [Bobry - 1983] at the required output voltages.

Ferro-resonant Inverters. A single-phase thyristor inverter using a ferro-resonant transformer is shown in Fig. 2.4. The inverter produces a square wave which is applied to the primary of the ferro-resonant transformer. The transformer core is designed [Patchet - 1954] so that the secondary side should magnetically saturate at the desired output voltage. The output voltage therefore remains relatively constant over a wide range of input voltages and load variations. The capacitors connected across the secondary help to drive the core into saturation and also, in conjunction with the inductive coupling, smooth the output waveform to an acceptable distortion limit [Suozzi - 1978, Rando - 1978]. Each input is loosely coupled to the output due to the presence of the two magnetic shunts. The combination of the effective inductance of each shunt and the equivalent capacitance due to C resonates at a frequency of 50 Hz. The output voltage regulation relies on the saturation

properties of the core of the transformer. Various design techniques have been reported in the literature [Kakalec and Hart - 1971, Relation et al - 1973,Prabhu et al - 1974].

To improve output voltage regulation an additional secondary winding with a supplementary filter and a controlled inductor was utilised [Kakalec and Hart - 1971] as shown in Fig. 2.4. The magnitude of the output voltage is regulated by varying the effective value of the controlled inductor by changing the firing angle of the antiparallel connected thyristors in series with the inductor. Although a transformer in conjunction with a controllable reactor keeps the output voltage constant, the constantly changing controlling angle of the thyristors may result in instability problems especially at light loads or when the load is suddenly changed. Output voltage stability can be achieved by decreasing the loop gain of the AVR or by inclusion of a dummy load. With the adoption of the former method, the voltage regulation accuracy will deteriorate whereas the use of the latter method decreases the overall efficiency.

In an attempt to reduce the output voltage fluctuations and avoid instability problems, an alternative method consisting of a magnetic amplifier of special construction is used as a feedback component to control the firing angle of the thyristors [Harada et al - 1986]. PWM inverters are also employed to overcome the transient disturbances and to extend the range of the available input voltage to the inverter [Notomi et al - 1983]. These systems can be paralleled. An analysis has been carried out for the steady-state operation of parallel circuits and some conditions are derived for equal current sharing [Harada et al - 1985].

To achieve the three-phase output waveforms, three similar single-phase inverters are used. The three input windings of the transformers are delta connected to the AC line and the three secondary windings may be connected in delta or wye to a three-phase load. The control circuit utilised to generate the three-phase output signals is also synchronised with the mains [Notomi et al - 1983].

The UPS employing these inverters are rugged, reliable and require simple control circuits. Since these systems usually work as standby power sources, their efficiencies are considered reasonable. These systems always experience considerable overshoot upon load removal and considerable undervoltage upon addition of load because of the energy stored in the magnetic components. Since these systems use low frequency tuned filters and 50 Hz transformers, they are thought to be noisy and heavy.

Delta Magnetic Inverters. A schematic diagram of a three-phase delta magnetic system is shown in Fig. 2.5. In this system the outputs of the three-phase square wave inverter are linked to the delta connected primaries of a conventional three-phase isolating transformer. There are also delta connections between the network (inductors and capacitors) and the taps on the secondary windings. A star point is also available at the output as can be seen from Fig. 2.5 [Bobry - 1983].

Since the primary windings of the transformer have delta connection and inductors in series with the inverters, the third harmonic and its multiple will be eliminated. The input configuration therefore improves short circuit current handling capability and simplifies the filter design. All inductors at the secondary side are saturable reactors and are designed to saturate at the desired amplitude of the sine wave. The three inductors (L_4, L_5, L_6) and capacitors (C_1, C_2, C_3) are used to filter the output waveforms, whereas the other three inductors have double windings and each inductor is connected to two windings to achieve line-line voltage regulation. Thus, the delta network is inherently a three-phase regulator in contrast to the ferro-resonant inverter and it also draws sinusoidal current [Bobry - 1983].

The above mentioned technique is capable of maintaining the output voltage regulation even under unbalanced loading conditions. This type of system is however, bulky, heavy, can suffer from acoustic noise and has a relatively poor transient response.

2.1.6.2 Inverters Using Electronic Techniques

The inverters use power conversion techniques such as pulse width control and feedback control circuits to synthesize the output waveforms. These inverters can be categorised into the following types; pulse width controlled thyristor inverter, stepped wave inverter and sinusoidal pulse width modulated inverter.

2.1.6.2.1 Pulse Width Controlled Thyristor Inverters

Complementary Commutated Inverters. A single-phase bridge complementary impulse commutated inverter is shown in Fig. 2.6. The bridge configuration is equivalent to two square wave half-bridge inverters connected in cascade mode. This is the most often used configuration when pulse width controlled operation is desired in single-phase applications [Dewan and Straughen - 1975].

To generate the positive half cycle, thyristors T_1 and T_4 are turned on. At the end of the half period, the firing of the thyristors T_2 and T_3 will turn off the thyristors previously turned on. By adjusting the phase angle ϕ of thyristors T_3 and T_4 with respect to that of thyristors T_1 and T_2, the output voltage can be varied smoothly. Diodes D_1-D_4 are used for the free wheeling inductive current whereas diodes D_1'-D_4' work in conjunction with the former diodes to feed back the trapped energy of inductors (during commutation) into the DC line.

The output waveform essentially requires large filtering components to decrease the harmonic content to an acceptable level. Usually a series-parallel tuned filter is used for this purpose and which consists of a series resonant element L_sC_s and a parallel element L_pC_p. The series L_sC_s is tuned to the fundamental frequency so as to pass it without any attenuation and phase shift while at the same time it presents a high impedance to the higher frequencies. The parallel element L_pC_p in conjunction with the transformer completes the filtering. The kVA ratings of the inverter elements depend on the desired output THD and transient response characteristics [Dewan and Ziogas - 1979]. The output undershoot or overshoot may reach up to 40 percent under full load switching conditions [Chauprade - 1977].

These inverters have been used at ratings up to 100 kVA and several similar inverters can be put in parallel to obtain high power levels. The output voltage regulation is within one percent and THD can be decreased to as low as 3 per cent. The inverter can work satisfactorily with load power factor down to 0.5 and the efficiency is of the order of 80 percent [Chauprade - 1977].

Impulse Commutated Inverters. To overcome the trapped energy problems and to reduce the size of the output filter, the auxiliary commutated inverter suggested by McMurray [Bedford and Hoft - 1964] can be used with an increased number of output pulses per half cycle. Two pulses 60^o apart [Mazda - 1973, Krishnamurthy et al.- 1979] can be used to eliminate the triplen harmonics throughout the voltage control range where voltage control is achieved by varying pulse widths. In an alternative scheme, the thyristors can be operated with fixed switching angles α_1 and α_2 to eliminate third and fifth

harmonics, and voltage control is achieved by phase shifting the gate pulses of one pair with respect to the other pair of thyristors [Bedford and Hoft - 1964]. This reduces the size of the output filter. Output voltage control can be obtained by varying the pulse widths.

The auxiliary impulse commutated circuit requires more thyristors as compared to the complemetary impulse commutated inverter and can be used for higher power applications. This circuit generates severe transients across all thyristors which require snubbing components.

Three-Phase Inverter With Wye Connections. Three single-phase inverters with the outputs displaced by 120^{o} with respect to each other can be configured as a three-phase inverter where each inverter is connected to a separate isolated primary winding of a three-phase transformer as shown in Fig. 2.7 [Chauprade - 1977]. Since each phase has a separate feedback control, this configuration is well suited to unbalanced loads.

Three-Phase Inverter With Zig-Zag Connections. Three single-phase bridge inverters with their outputs coupled together by three transformers as shown in Fig. 2.8 [Chauprade - 1977]. The outputs of the transformer are connected in Zig-Zag connection. The output voltages are achieved with the composition of two single phase voltages displaced by 60^{o}. The third harmonic and its multiple harmonics would be eliminated from line and line-line voltages by virtue of the design [Chauprade - 1977]. Three element filters therefore can be utilized to obtain a THD less than 5 percent.

Three-Phase Inverter With Scott Connections. A circuit diagram is shown in Fig. 2.9. This scheme uses two single-phase inverters, A and B, where the latter's control circuit shifts its output by 90^{o} with respect to the former. The taps of the two secondary windings are arranged in Scott connections. This solution is most economical for generating three phase outputs from two inverters. The performance characteristics are similar to those of the complementary commutated single-phase inverter [Chauprade - 1977].

All the aforementioned inverters have slow transient response to step load change and are often used in high power applications.

2.1.6.2.2 Stepped Wave Inverters

The stepped wave inverters either change transformer taps or add schematically the output waveforms of several single-phase inverters with shifted controls to achieve the resultant stepped waveform which should closely approximate a sine waveform. The selection of the number of inverters can be determined from the desired level of distortion in the output waveform. Where a stepped wave inverter consists of N square wave inverters which are sequentially phase shifted by 180/N electrical degrees [Kernick and Heinrich - 1964, Heinrich - 1967], the lower order harmonics will be eliminated and the remaining harmonics have frequencies $2KN \pm 1$, where $K = 1,2,3...$ The amplitudes of the remaining harmonics are inversely proportional to their frequencies. Each inverter will share the output power equally, if and only if the output voltage of the individual inverters are adjusted properly.

Since stepped wave inverters are usually employed for high power requirements, three-phase inverters are preferred. A three-phase stepped wave inverter comprising six square wave single-phase inverters is shown in Fig. 2.10. The control circuits of the six single-phase inverters are shifted, one with respect to the other by $180^o/6 = 30^o$. Each inverter has an output transformer with three secondaries connected in cascade to neutralize 3rd, 5th, 7th and 9th harmonics [Kernick et al - 1962]. The number of inverters can be reduced to four by utilizing single-phase inverter configurations with two pulses per half-cycle [Sriraghavan - 1982]. All inverters are identical and are operated with a relative phase shift of 30^o.

The three-phase six stepped wave inverter provides very stable operation with a steady-state accuracy of the order of ± 1 percent and undershoot/overshoot within ± 10 percent. The total harmonic distortion is less than 3 percent and efficiency about 90 percent [Chauprade - 1977, Sriraghavan - 1982]. The stepped wave inverters offer inherent redundancy because the loss of one inverter does not cause failure of the complete system. It simply unbalances the output voltages and increases the THD. Although stepped wave inverters are excellent in power handling, the number of inverters and their associated control circuits make the system complex. The combined rating of the transformers is about 1.4 times the rating of the inverter. The system is therefore thought to be noisy, expensive and bulky.

2.1.6.2.3 Sinusoidal Pulse Width Modulated Inverters

The sinusoidal PWM inverters synthesize the output waveform by switching the power devices at a higher frequency than the desired fundamental frequency. The aims of such inverters are to minimise as many low order harmonics as possible and also to effect control over voltage and frequency with a single switching stage. Several PWM schemes are available in the literature but for the sake of simplicity, these can be categorized into three schemes, namely, the optimum switching strategies [Buja and Indri - 1977, Casteel and Hoft - 1978, Issawi et al - 1982], the optimal switching strategies [Geyer - 1971] and the carrier modulated switching strategies [Kretzmer - 1947, Bowes - 1975, Bowes and Clements - 1982].

Inverters employing the optimum switching strategies operate with a fixed pattern which is periodic. These switching patterns are calculated to obtain the best possible waveform for the number of switching angles permitted in a cycle. Since the pulse widths need to be varied to effect control over voltage, this becomes difficult while keeping harmonic content constant. These strategies are therefore not commonly used in inverters for UPS applications.

Inverters using time optimal strategies require an output filter for the strategy to be effected and must have closed loop control [Geyer - 1971, Kawamura and Hoft - 1984] as shown in Fig. 2.11. The permissible output variations from the sinusoidal reference are determined from the preset hysteresis in the feedback path. Since the switching frequency depends upon the amount of hysteresis and on the characteristics of the output filter and load, the inverter switching rate varies throughout the cycle. To keep the error signal minimum under a sudden load change, high switching rates are required and these need to be changed instantaneously. Thus the predictions of operating characteristics under adverse load conditions are rather complicated. Several other modified and improved control techniques [Gokhale et al - 1985, Kawamura et al - 1988] are now available in the literature that are more effective in dealing with the distortion caused by nonlinear loads. These schemes are generally used for single-phase operation and are mostly implemented by microprocessors.

Inverters using carrier modulated strategies are switched at the intersection of a triangular carrier wave with a sinusoidal modulating wave as shown in Fig. 2.11a. The most commonly used strategies are the natural sampling strategy and regular sampled switching

strategy. Voltage control is usually achieved by varying the amplitude of the sine reference waveform. The harmonic distortion in the output waveform occurs at the carrier frequency and its side bands and multiples of the carrier frequency. The magnitude of the distortion(THD) decreases with an increase in the modulation index and is therefore lowest at 100 percent modulation. The carrier modulated strategies provide inherent voltage control and lend themselves to easy implementation by a microprocessor controlled PWM generator.

Recently available UPS systems use PWM inverters with thyristors, GTOs and bipolar transistors. Although thyristors have excellent power handling capabilities, their slow switching speeds and the accompanied commutation circuitry and associated switching losses restrict the switching frequencies up to few kHz. GTO PWM inverters eliminate the commutation circuit required by conventional thyristors but at the expense of a sophisticated gate drive circuit and protection scheme.

Advances in power MOSFET and bipolar transistor technologies allow the switching frequencies of low and medium power inverters to be increased up to several tens of kHz [Okano et al - 1983, Grant and Houldsworth - 1983]. By using a high switching frequency, the least desirable harmonics are well separated from the fundamental component, thereby permiting the use of the simplest PWM strategy [Khan and Manning - PEVDs 88]. AC filtering can then be accomplished with a simple two elements LC low pass filter instead of the multicomponent tuned networks used in low frequency inverters. The use of switching frequencies above the audio range allow inverters to be realized without acoustic noise. MOSFETs are being preferred for use in inverters because of their simple gate drive circuit requirements, fast switching speeds, ease of paralleling operation and wide operating area.

2.1.7 Static Transfer Switch

Almost all UPS systems are equipped with static transfer switches which may consist of two back-to-back connected thyristors utilized in series with the mains and the output of the inverter as shown in Fig. 2.12. The static switches are used to provide further protection to the critical load in the unlikely event of the inverter failure or to enable large surge current demanded by the load to be supplied from the mains during its availability.

To transfer the load to the mains without any interruptions in power, the control circuit of the inverter must synchronize the frequency and phase with the mains. In addition, the

control circuitry to the static transfer switches must monitor the frequency and amplitude of the inverter. The circuit must respond instantaneously to the disturbances in the output waveform or any deviation from the preset frequency limits and maximum allowed rate-of-change of frequency.

2.2 POWER SEMICONDUCTOR DEVICES

The present range of power semiconductor devices available for application in power conversion equipment has developed from the original range of diodes and conventional thyristors into a large family which now includes asymmetric thyristors [Vitins - 1982], gate turn-off thyristors [Azuma et al - 1981, Tokunoh et al - 1984], asymmetric field controlled thyristors [Baliga - 1980], triacs [Thorborg - 1985], static induction transistors [Nishizawa et al - 1975, Nishizawa and Jamamushi - 1988], static induction thyristor [Nishizawa and Jamamushi - 1988, Nishizawa et al - 1988], bipolar power transistor, IGBT, and power field effect transistors [Pelly - 1982]. Some of the above mentioned devices either have a limited field of applications or are still only available in small sizes and quantities and have not yet reached such a stage of development that they can be regarded as established standard devices. It is therefore decided to discuss only this standard and popular devices used in UPS inverter applications. These are the conventional thyristor, the GTO, the bipolar power transistor and the power MOSFET.

Traditionally, conventional thyristors are used in inverter applications due to their low cost and excellent power handling capabilities. However, despite the advantages of requiring simple drive circuitry to turn the device on, they require auxiliary circuits for turn-off. This may consist of a commutating LC network/and an additional auxiliary thyristor. Furthermore, these devices have stringent requirements regarding the rate of rise of on-state current, dI/dt and rate of rise of off-state voltage, dV/dt. If the rate of rise of current is too high, an area around the gate will be overheated due to the initial on-state current concentration in that area and, consequently the device may be damaged, whereas too high a rate of rise of voltage may cause false triggering. To keep dI/dt and dV/dt within the prescribed limits, the thyristor must be series connected with an inductance and in parallel with an RC circuit.

Turn-off commutation circuit losses increase with frequency and are usually significant at high switching frequencies. Also, due to their slow switching times and need to allow sufficient time to reset the turn-off snubber, conventional thyristors are not recommended

for use in PWM inverters at high switching frequencies (>2 kHz). The turn-off commutation circuits required by conventional thyristors can be eliminated by replacing the thyristor with totally gate controlled devices such as the GTO thyristor, bipolar transistors and power MOSFET. The GTO thyristor has similar characteristics to those of the conventional thyristor but with the ability to be turned off at the gate. GTOs and bipolar transistors are widely used in VSDs and UPS applications. Since these devices do not require complex commutation circuitry, the resulting inverter should be smaller and lighter and will produce less acoustic noise than its conventional thyristor counterpart.

GTOs and bipolar transistors have almost similar turn-on drive requirements as high pulse current is required for fast turn-on followed by continuous on-drive, especially in the case of the bipolar transistor. Also, in general, both devices require large reverse currents for fast and reliable turn-off, although the transistor will turn off without reverse bias current but its turn-off will be slowed down. In the off-state both devices require benefit from reverse biased control junctions since it increases noise immunity.

The GTO thyristors suffer from a long storage time and current fall time as well as tail currents. In addition, to achieve shorter turn-off times, the turn-off gain must decrease and may reach unity [Williams - 1987]. The GTO also suffers from a relatively low dV/dt rating which necessitates rather large snubber capacitors. Unless lossless snubbers are used, the snubber capacitor loss ($^1/2CV^2f$) which is dissipated in the device at turn-on, becomes large. That is why the use of GTO thyristors have been restricted to low switching frequency applications (≤5 kHz). The bipolar power transistor can be operated at higher switching frequencies at medium power level but care need to be taken to avoid secondary breakdown problems. However, both devices require sophisticated driving circuitry, snubbing components and complicated short circuit protection schemes for reliable operation. Since increasing switching frequencies is the general tendency in power electronics, this can be increased to reasonably high values by using power MOSFETs. Recently, in many PWM inverters for VSDs and UPS applications, frequencies above the audio range have been preferred since these inverters require small filtering components and do not generate audible noise [Khan and Manning - 1988]. After taking all factors into account, the power MOSFET now appears to be the most promising device for this and many other applications and it was therefore utilized as the power switching element in the UPS inverter. The relevant characteristics of the power MOSFET are discussed in the next section.

2.2.1 The Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

A basic low power lateral structure of the metal oxide field effect transistor is shown in Fig. 2.13. This consists of a lightly doped p-type substrate into which the n^+ source and drain regions are fabricated and a thin layer of silicon dioxide insulates the aluminium gate from the silicon region. As long as the potential between gate and source is not positive, the device essentially behaves like two diodes connected back-to-back, and only a small junction reverse leakage current can flow between the drain and source. Since N-channel MOSFETs are operated with a positive gate-source voltage potential, this is called enhancement mode of operation. When the gate-source is positive, an N-type channel is induced between the drain and source. By changing the gate-source voltage, the width of the channel is controlled which effectively varies the resistance of the channel. Due to the existence of the gate oxide insulator, the gate metal and body semiconductor form a capacitor which accumulates charge. As the gate-source potential is increased, the electron density to the gate oxide exceeds the hole density and then a portion of the region between the drain and source (channel) inverts to become n-type rather than p-type. The drain-source path of the MOSFET then becomes simply an n-channel and the device behaves like a voltage controlled resistor, the control being effected by the gate potential.

The minimum positive gate voltage capable of inducing the n-conducting channel between the drain and source is known as the threshold voltage V_T. The typical output characteristics of a MOSFET are drawn in Fig. 2.14 showing the relationship between drain current I_D, drain-source voltage V_{DS} and gate-source voltage V_{GS}.

Most MOSFET manufacturers use the planar vertical N-channel DMOS structure [Severn - 1981] to overcome the inherent poor utilisation of the lateral MOS structure. In the DMOS structure, an n^- epitaxial layer is fabricated on an n^+ substrate and into which a series of p^- body regions are diffused. Then n^+ source regions are diffused within p^- regions and polycrystaline silicon gate is fabricated into the silicon dioxide insulating layer. Finally source and gate metallisation are deposited on the top surface and the drain contact is made to the bottom of the die.

A low on-resistance is achieved with the vertical DMOS structure because all interconnections are diffused between cells. The device turns on with the appropriate positive gate signal and majority carriers start flowing laterally from the source to the drain

region below the gate and vertically down towards the drain as shown in Fig. 2.15.

The range of N-channel MOSFET is more extensive than P-channel types because the N-channel devices offer better conductivity. Since the resistivity of the P-type silicon is much higher [Severn - 1981] than that of an N-type silicon, the P-channel device requires a larger active area to achieve the same on-resistance and current ratings as the equivalent N-channel device.

2.2.1.1 The Safe Operating Area (SOA)

Most semiconductor data sheets contain information on the safe operating area, maximum junction temperature, pulse currents, maximum voltage and current ratings as well as steady-state and transient thermal impedance. The SOA data contains the information about the electrical limitations which must be observed if acceptable performance and safe operation are to be achieved. The maximum safe operating area (SOA) for a typical power MOSFET (IRF 250) is shown in Fig. 2.16 at case temperature, T_C=25° C and junction temperature T_j=150° C. The peak pulse current is based on a current above which internal connections may not be guaranteed or may be damaged. The maximum continuous current is limited by the junction temperature, and a degradation will occur in maximum continuous current if the temperature is allowed to increase above the safe limit. For pulses with small duty cycles the permissible pulse amplitude is increased as compared to the bipolar power transistor. This is because the on-state resistance $R_{DS}(on)$ increases with temperature so the current is automatically diverted from a hot spot. The power MOSFETs, therefore, have four SOA boundaries; the maximum voltage limited by BV_{DS}, the maximum current limited by metallisation and lead bonds, the maximum power limit that is the power dissipation which will raise T_j from T_c to T_{jmax}, and finally the on-state resistance $R_{DS}(on)$ limited region.

2.2.1.2 Parasitic Elements And Their Effects

There are several parasitic elements present inherently in the structure of a power MOSFET and these affect the performance characteristics of the MOSFET significantly during its operational life. These parasitic elements consist of devices (bipolar transistor and diode), capacitances, inductances and resistances.

2.2.1.2.1 Parasitic Bipolar Transistor (PBT)

In the construction of the MOSFET, the normal practice is to connect the body directly to one of the n-regions. The n-region to which the body is connected is defined to be the source terminal whereas the other n-region becomes the drain terminal of the MOSFET. The body-source connection shorts the base and emitter of the parasitic npn bipolar transistor. However this short circuit cannot be perfect [Watson - 1981] because the p-region will still have some resistance so the parasitic bipolar transistor is not completely deactivated. Fig. 2.17 shows the resultant parasitic bipolar transistor in the equivalent circuit of the MOSFET. It is commonly assumed that any mechanism that permits the parasitic bipolar transistor to conduct will usually lead to the failure of the MOSFET. This can occur if dV/dt is large enough, causing a current to flow through the collector-base capacitance, C_{CB} to generate a sufficient voltage drop across R_B to turn on the parasitic bipolar device [Severn - 1981]. It is also suggested that the parasitic bipolar transistor is more likely to become active as the temperature increases. This is mainly due to the transverse potential drop beneath the MOSFET source needed to turn on the bipolar transistor decreasing with the increase in temperature (0.45 V at 100°C and 0.6V at 25°C) and the R_B resistance beneath the source increasing with the increase in temperature [Blackburn - 1985].

2.2.1.2.2 Parasitic Inverse Parallel Diode

Since the source metallisation also contacts the body of the MOSFET, the drain-body junction of the MOSFET appears as an inverse parallel diode between the source and the drain. The power MOSFET will therefore not support voltage in the reverse direction and cannot be used singly as an analogue bipolar switch.

In many power supply applications, the inverse parallel diode is considered as an advantage. This diode can be fully loaded within the power dissipation limits of the MOSFET. It would be utilised in half and full bridge PWM inverter circuits but at the expense of increased switching power losses mainly due to the longer reverse recovery time t_{rr} of the parasitic integral diode. The reverse recovery time for this diode in the IRF

250 is typically 300 ns at I_F = 30 A and dI/dt = 100 A/μs. The reverse recovery time of an inverse diode increases with the MOSFET's blocking capability so this can be a severe

problem for MOSFETs with high blocking voltages.

The use of the integral diode has two main consequences. Firstly, it causes losses in the MOSFET. Secondly, it tends to initiate conduction of the internal parasitic bipolar transistor as soon as the critical dI_D/dt and dV_{DS}/dt values are exceeded. The consequence of the parasitic bipolar transistor turning on is that the cell loses its blocking capability, current crowds into that cell and the device is destroyed [Lorenz - 1984].

To overcome this problem, a solution based on the use of a series Schottky diode and an external fast recovery free wheeling diode has been devised. The series diode blocks the current flow in the reverse direction through the MOSFET, and the current then flows in the free wheeling diode. This solution, though effective, is costly and reduces the efficiency of the power circuit.

2.2.1.2.3 Parasitic Capacitances

The gate-source capacitance, C_{GS}, gate-drain capacitance, C_{GD} and drain-source capacitance, C_{DS} are shown in the equivalent circuit of a power MOSFET in Fig. 2.17. The gate-source capacitance C_{GS} appears due to the use of silicon dioxide as a dielectric between the gate and source metallisation. To switch a MOSFET, the capacitor C_{GS} needs to be charged and discharged each time with the frequency at which the device needs to be operated. Therefore, the gate drive circuit must supply sufficient current to turn on/off at the required speeds.

The gate-drain capacitance, C_{GD} also affects the switching behaviour very seriously. This capacitor is known as the Miller effect or feedback capacitor. The negative feedback effect of the gate-drain capacitor can slow down the rate at which the channel is turned on/off. Also if the current flowing through C_{GD} is enough to raise the gate voltage to its threshold value, the device will turn on. This condition can be avoided by reducing the gate drive circuit impedance.

The drain-source capacitance, C_{DS} is the depletion layer capacitor of the PN junction (collector-base) of the parasitic bipolar transistor and therefore depends upon the drain source voltage.

2.2.1.2.4 Parasitic Resistances

Three parasitic resistances appear in the power MOSFET structure as shown in Fig. 2.17. These are the gate resistance R_G, the drain resistance R_D, and the base-emitter resistance R_B of the PBT. These resistances respectively affect the switching behaviour, power losses and failure mechanism of the power MOSFET.

Power MOSFET manufacturers use a polysilicon gate for obtaining a self aligned structure and a stable gate to oxide boundary [Watson - 1981]. In addition, aluminium connections are used for distributing the gate current to the polysilicon gates. The gate to the source junction still has some resistance due mainly to the polysilicon. A relatively large R_G will result in longer charging/discharging times and an increased threshold voltage.

The resistance R_B which exists in parallel with the emitter-base junction of the PBT is due to the imperfect short connections during body-source metallisation. A larger value of R_B makes the PBT more susceptible to becoming active even with a relatively small current flow through the collector-base capacitance.

Besides the above mentioned two parasitic resistances in the MOSFET structure, the most important resistance is the on-resistance, R_{DS} between the drain and source terminals. This resistance is composed of several other individual resistances such as bonding resistance, channel resistance, resistance of the epitaxial layer etc. For MOSFETs rated above 100 V the resistance of the epitaxial layer dominates the on-resistance and this resistance has a high positive temperature coefficient. During the on-state of the MOSFET, the saturation voltage across the device will be determined by the on-state resistance, $R_{DS}(on)$. Power dissipation in MOSFETs is therefore determined by the $I_{Drms}^2 R_{DS}(on)$ losses.

2.2.1.3 MOSFET Switching Characteristics For A Clamped Inductive Load

To explain the switching characteristics of a MOSFET, typical waveforms of the drain current I_D and drain-source voltage V_{DS} are drawn in relation to the gate-source voltage V_{GS} at turn-on and turn-off as shown in Figs. 2.18 and 2.19. It is shown in the diagram

that the application of gate-source voltage starts at time t_o and the voltage reaches the threshold voltage V_T at time t_1. The time taken therefore depends upon the input capacitance of the MOSFET and the impedance of the drive circuit. As soon as the threshold voltage is reached, the drain current starts to increase. It can be seen from Fig. 2.19 that the gate-source voltage waveform is deviated from its original path due to the following reasons: Firstly, inductance in series with the source which is common to the gate circuit develops an induced voltage due to the increasing source current. The induced voltage counteracts the applied gate-source voltage and slows down the rate of rise of voltage appearing directly across the gate-source terminals. Secondly, the gate-source voltage is affected by the so called "Miller" effect. During the period t_1 to t_2 some voltage is dropped across the stray circuit inductance in series with the drain and the drain-source voltage starts to fall. The decrease in drain-source voltage is reflected across the drain-gate capacitance which pulls discharge current through it and consequently it increases the effective capacitive load on the drive circuit. This will increase the voltage drop across the source impedance of the drive circuit and slow down the rate of rise of gate voltage. Obviously, a lower impedance drive circuit would decrease this effect. These effects can be seen throughout the period t_1 to t_2, while the current through the MOSFET reaches I_M, already flowing in the free wheeling diode and it continues into the next period t_2 to t_3. Then the current increases further due to the reverse recovery effects of the free wheeling diode. At time t_3 the free wheeling diode starts to support voltage, while the drain current and drain voltage start to fall. The rate of fall of drain voltage is now governed almost exclusively by the Miller effect and then equilibrium condition is reached under which drain voltage falls with the rate necessary for the gate-source voltage to satisfy the level of drain current established by the load. This is why the gate-source voltage falls as the recovery current of the free wheeling diode falls then it stays constant at a level corresponding to the drain current while drain voltage is falling. Obviously, the lower impedance drive circuits drive the MOSFET faster into conduction. Finally, at t_4, the MOSFET is switched fully on and then the gate to source voltage rises rapidly towards the applied voltage.

At time t_5 the gate to source voltage starts to fall during the turn off interval. At $t_6$the gate voltage reaches a level that just sustains the drain current and the device enters into the linear mode of operation. After t_6 the drain to source voltage is governed by the Miller effect and it also holds the gate to source voltage at a level corresponding to the constant drain current. The lower impedance drive circuit increases the rate of rise of drain source

voltage. At time t_7 the drain source voltage reaches its maximum and the gate voltage and drain current start to fall at a rate exclusively determined by the gate source circuit impedance. During the period t_8 to t_9, when the drain current is at zero and the drain voltage reaches it at its maximum value, the gate voltage decreases from V_T to zero at a rate determined by the drive circuit impedance.

2.3 CONCLUSIONS

It has been shown that the on-line UPS systems are the only power supplies which provide real protection from all kinds of disruptions in the mains supply. It has also been shown that PWM inverters offer more flexibility in design whilst maintaining the characteristic of being light weight, and that power MOSFETs are the most promising semiconductor devices for ultrasonic PWM inverters in UPS applications.

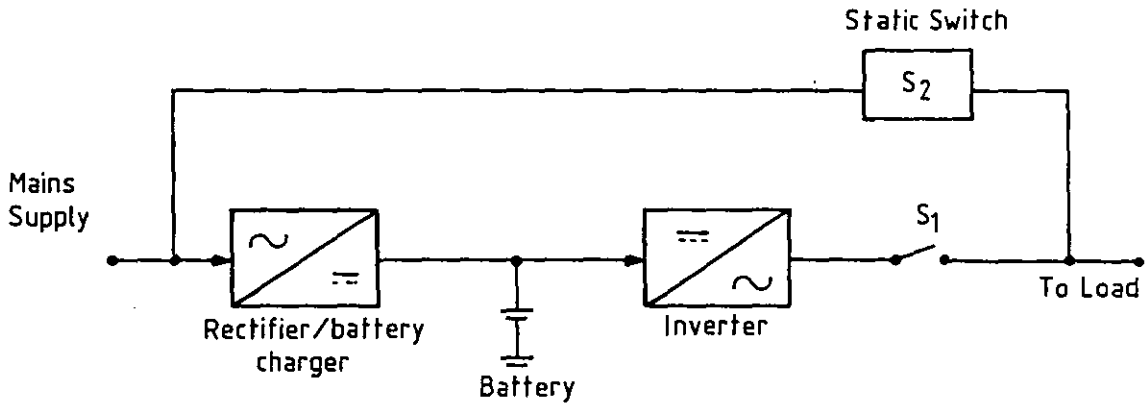


Fig. 2.1 On - line UPS

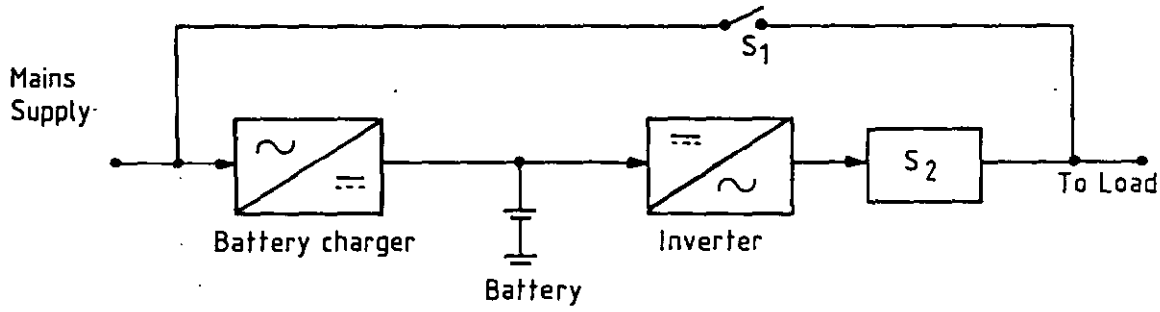


Fig. 2.2 Standby UPS

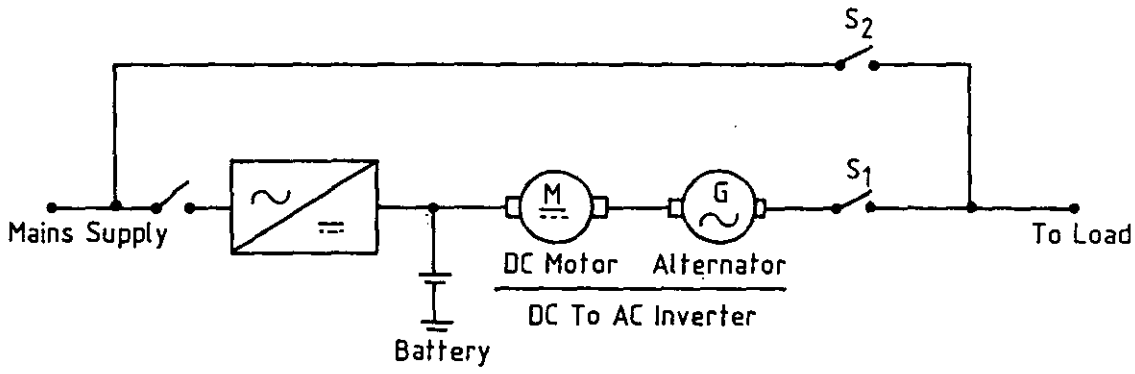


Fig. 2.3 A typical reversible rotary UPS

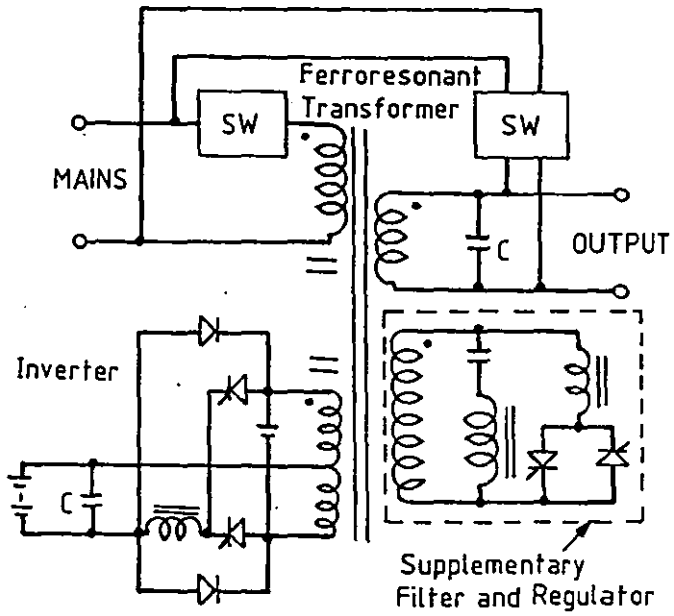


Fig. 2.4 A single - phase ferroresonant inverter.

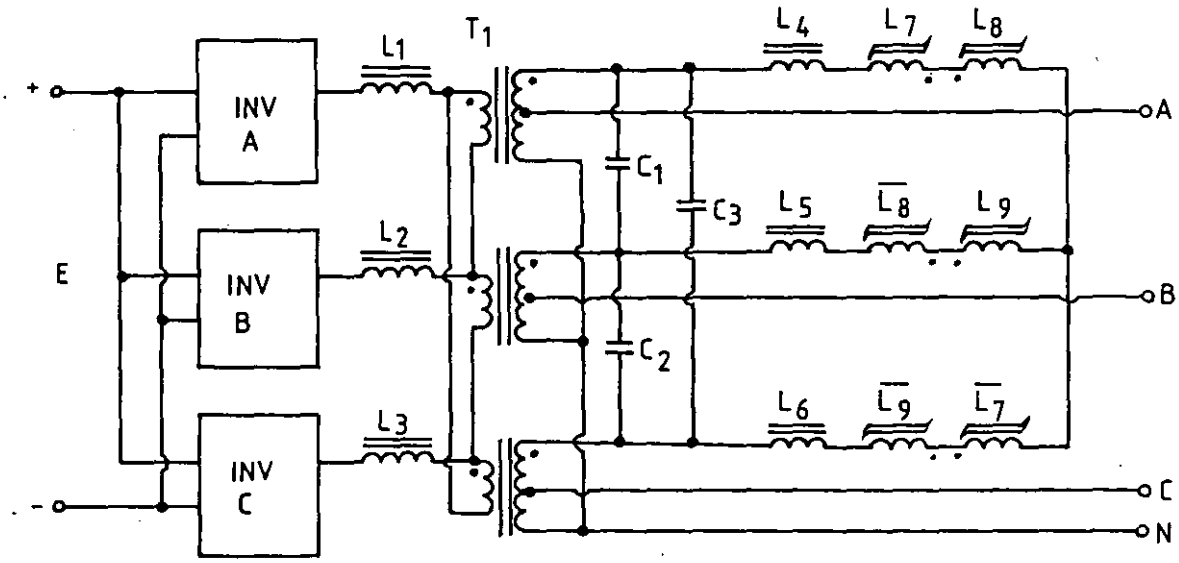


Fig. 2.5 A three-phase delta magnetic system.

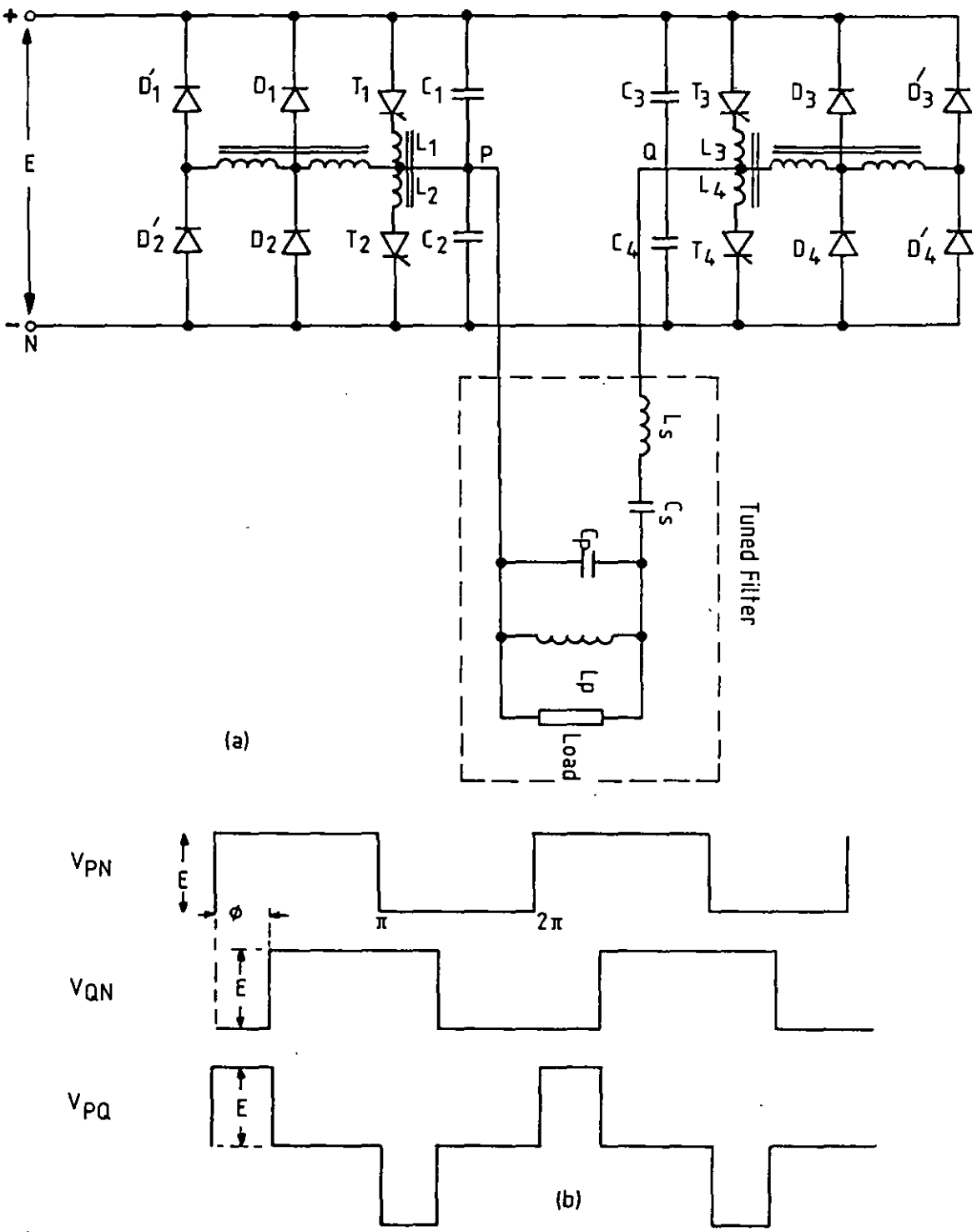


Fig. 2.6 a. Pulse - width controlled thyristor inverter.
b. Output voltage waveforms of the inverter.

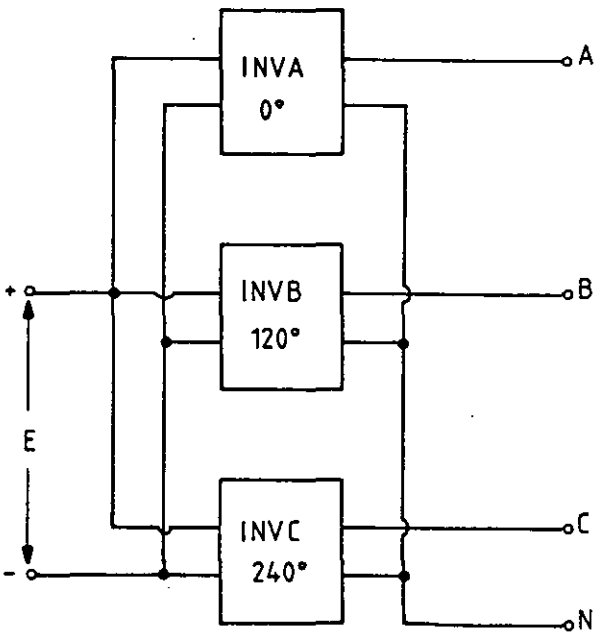


Fig. 2.7 A three - phase inverter with outputs wye - connected.

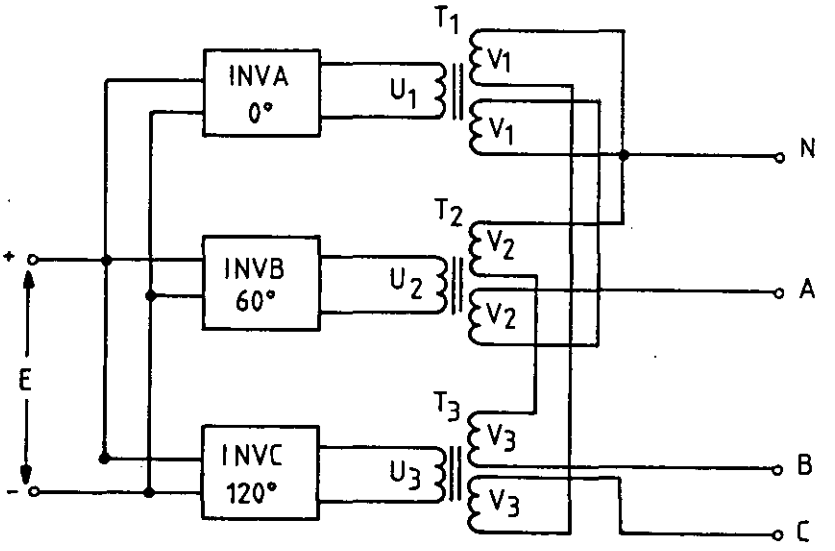


Fig. 2.8 Three - phase zig - zag configuration.

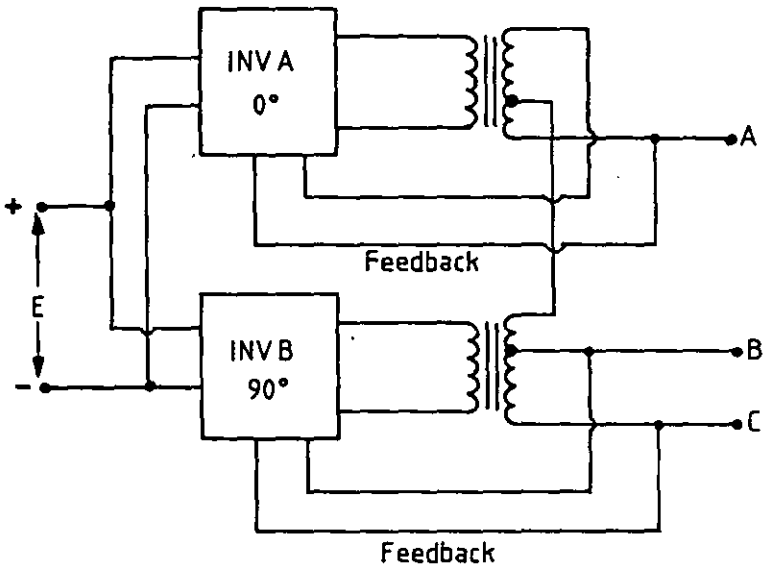


Fig. 2.9 Three - phase inverter with Scott connection.

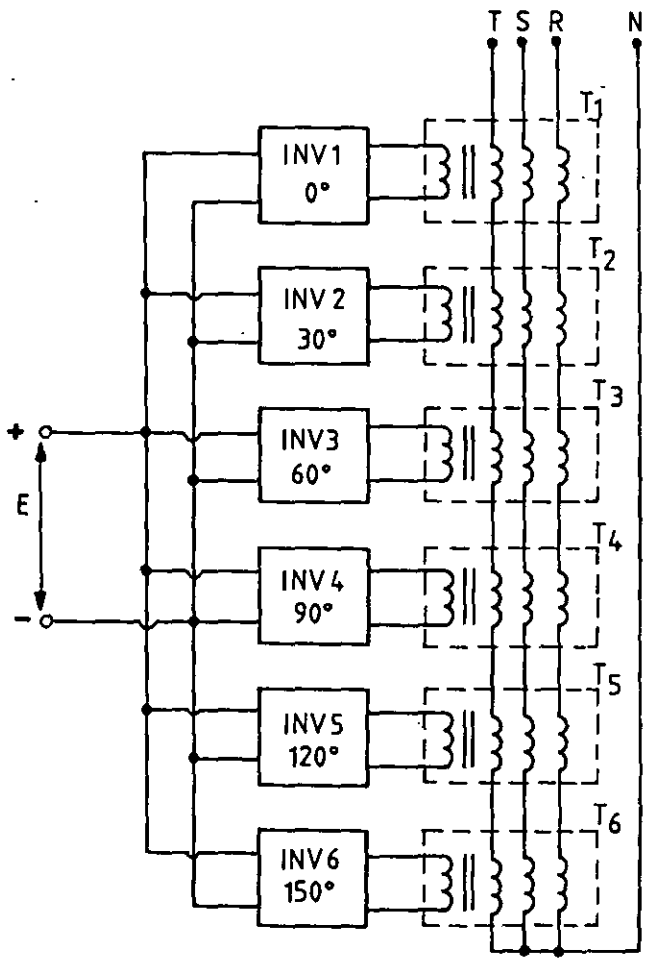


Fig. 2.10 A three - phase 6-stepped inverter.

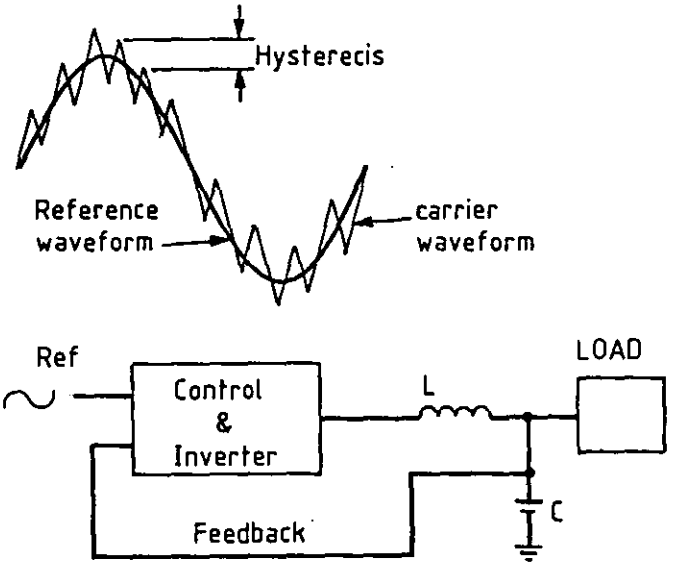


Fig. 2.11 Time Optimal Response Control

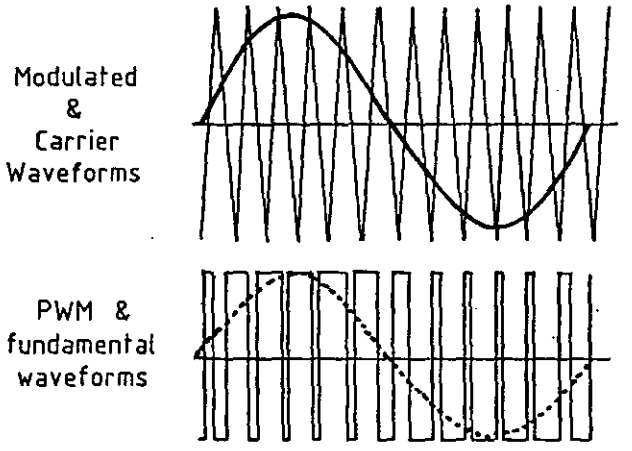


Fig.2.11a Carrier modulated waveform.

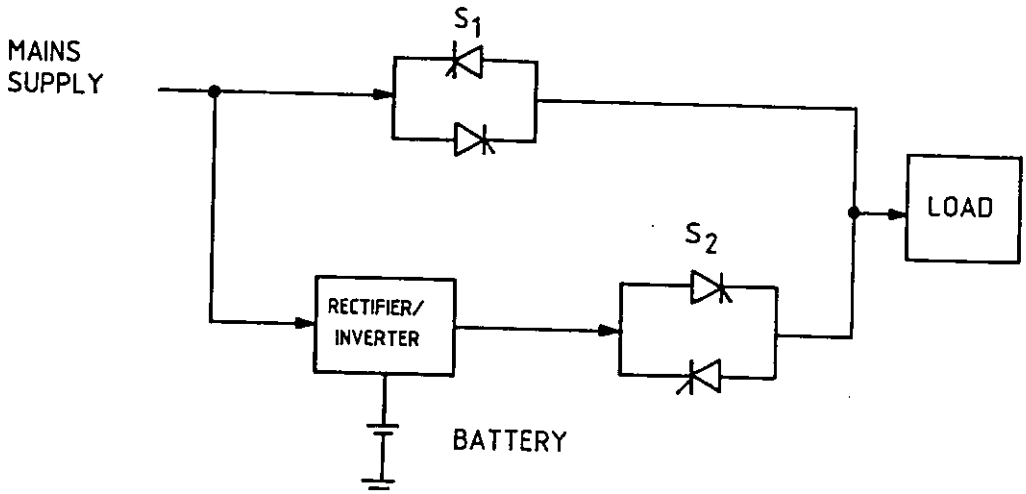


Fig. 2.12 A UPS system with static transfer switches.

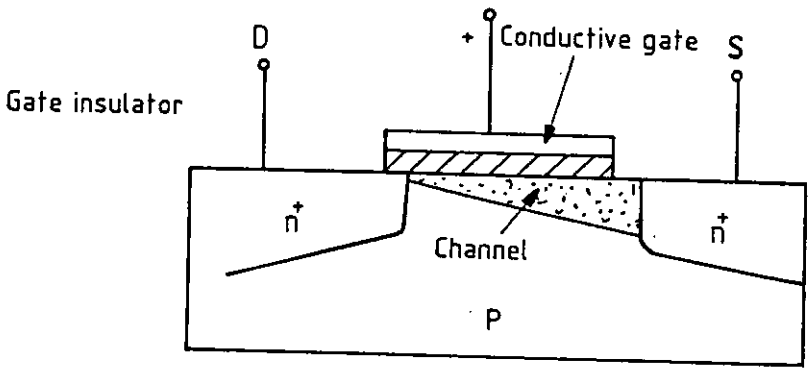


Fig. 2.13 A basic structure of an enhancement-mode MOSFET.

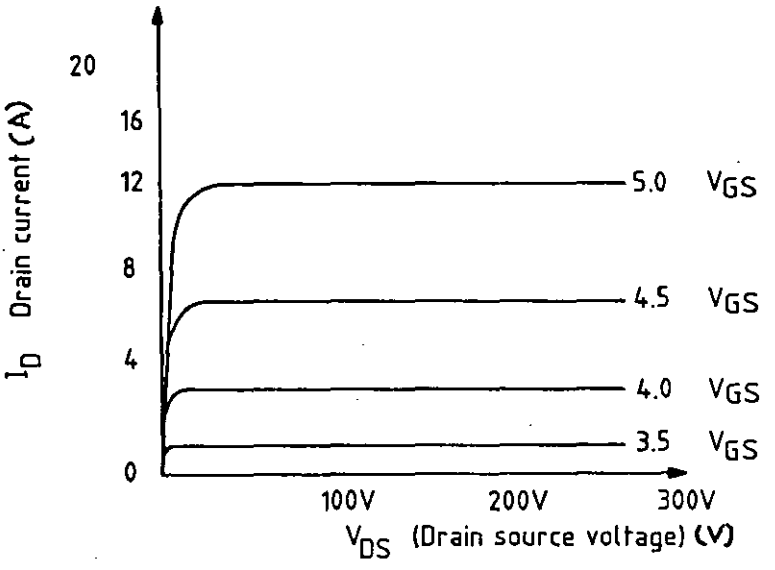


Fig. 2.14 Typical output characteristic of a N-Channel MOSFET.

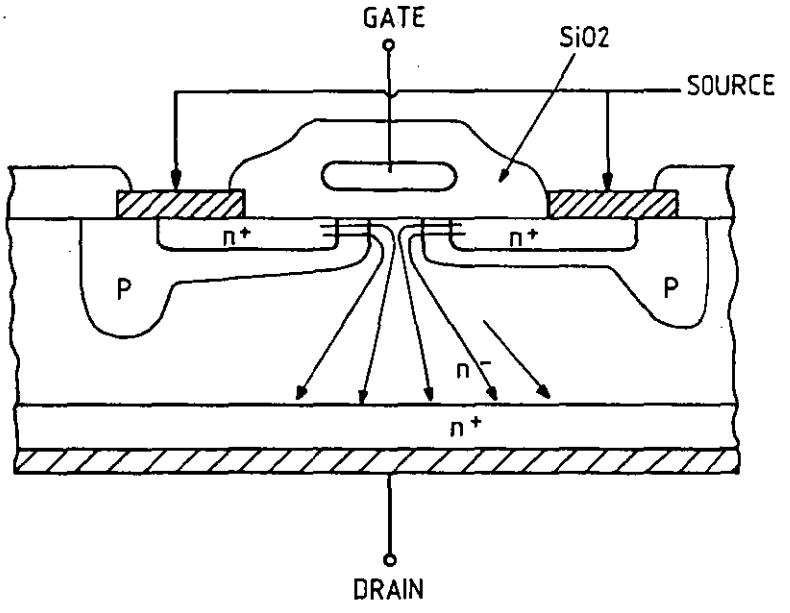


Fig. 2.15 A schematic diagram of a planar vertical DMOS MOSFET.

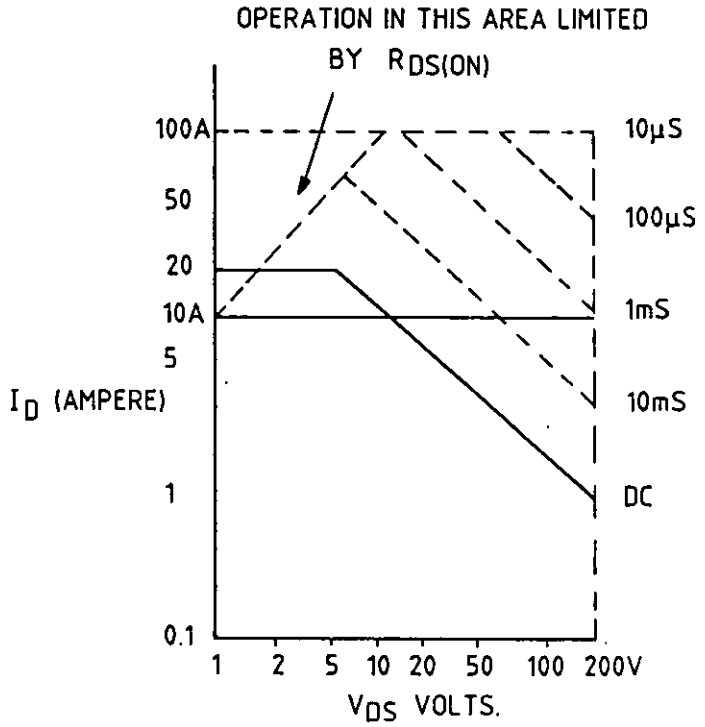


Fig. 2.16 Maximum safe-operating area for IRF 250

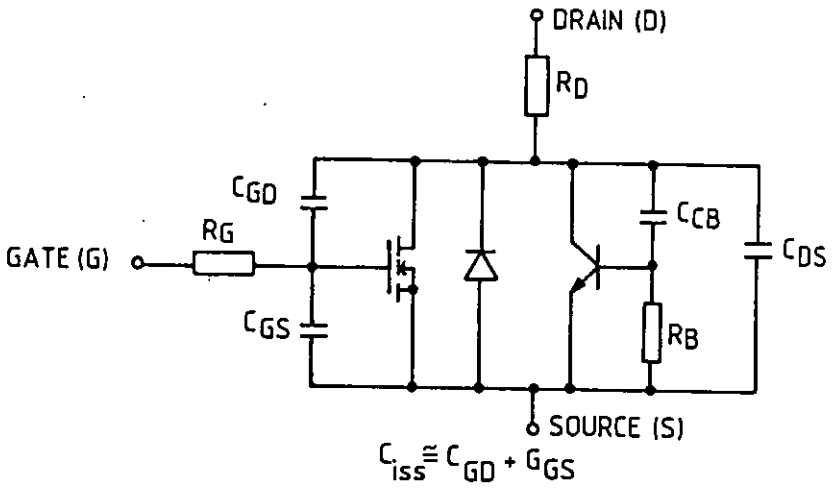


Fig. 2.17 Equivalent circuit of a MOSFET.

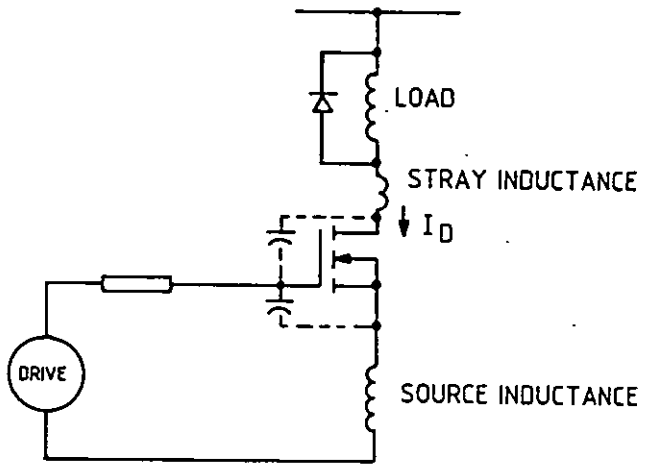


Fig. 2.18 MOSFET with inductive load

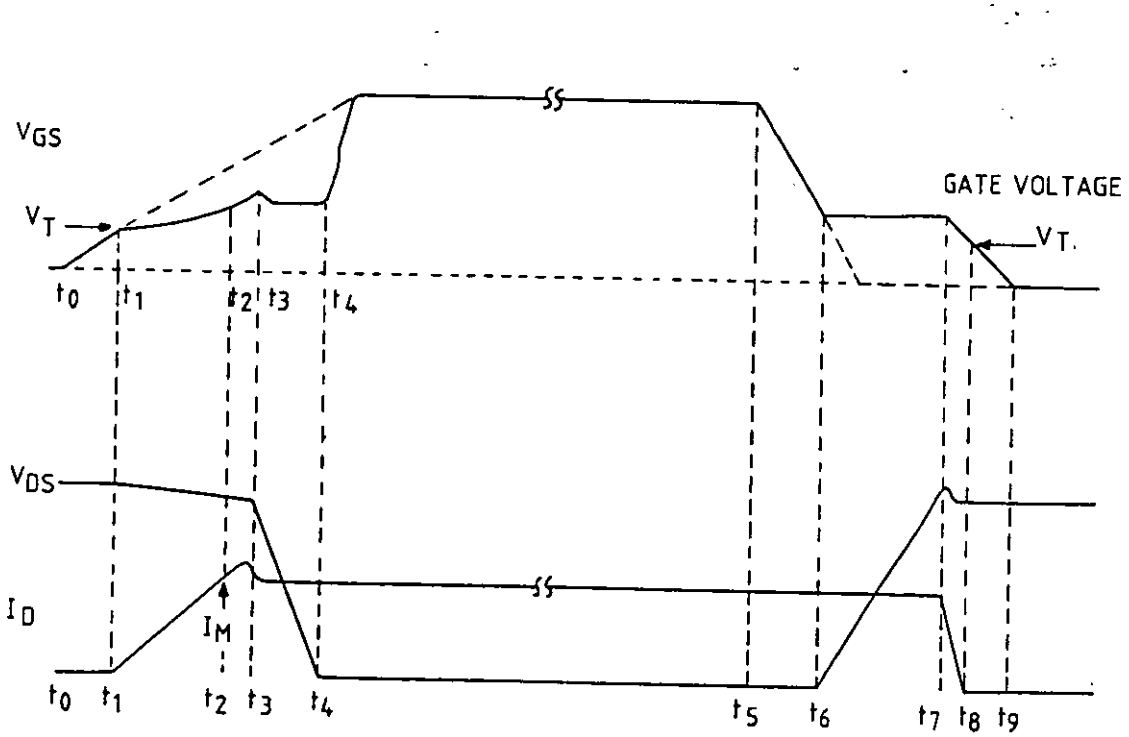


Fig. 2.19 Waveforms at turn on and turn off.

CHAPTER THREE

PWM STRATEGIES AND METHODS OF CALCULATING LOOK-UP-TABLE DATA

The basic principles, advantages and disadvantages of some PWM strategies capable of being utilised in UPS applications are described. The effects of high frequency carrier signals on the quality of the output waveform under different operating conditions are discussed together with the importance of a carrier signal of 18 kHz. The regular-sampled symmetric strategy is discussed in detail. The different methods of calculating the look-up-table (LUT) data are described together with their advantages and disadvantages.

3.1 PWM STRATEGIES

The aims of such strategies are to minimise as many low order harmonics as possible and also to effect control over voltage and frequency with a single switching stage. Several established PWM strategies are available in the literature and these could be categorised mainly into four types, namely, natural sampling strategy, delta modulation strategy, optimal switching strategy and regular sampling switching strategy.

3.1.1 Natural Sampling Strategy

The natural sampling strategy is based on the direct comparison of a sinusoidal modulating waveform with a triangular carrier waveform to determine the switching angles and therefore resultant pulse widths as shown in Fig.3.1. The resultant pulse width is proportional to the amplitude of the modulating waveform at the instant that comparison occurs [Kretzmer - 1947]. Consequently, it is not possible to define pulse widths using analytic expressions. However, it has been shown that as a result of the natural sampling process, which is non-linear, the pulse-widths T_p as shown in Fig.3.2 may be defined by a transcendental equation [Bowes and Bird -1975, Bowes - 1975]:

$$T_p = \frac{T}{2}\left[1 + \frac{M}{2}(\mathrm{SIN}w_m t_1 + \mathrm{SIN}w_m t_2)\right] \qquad (3.1)$$

where T = Period of the carrier signal,

M = Modulation index,

$w_m = 2\pi f_m$ = Angular frequency of the modulated signal,

and t_1, t_2 = Time instants of sampling of the modulating waveform.

It is not possible to calculate the widths of the modulated pulses directly due to the existing transcendental relationship and this can only be defined in terms of a series of Bessel functions by numerical techniques [Bowes and Bird - 1975, Bowes - 1975]. This can create difficulties in computer-aided design analysis and can also make it inappropriate for efficient discrete digital hardware or microprocessor software implementation.

It should be noted that as the carrier frequency is increased, the harmonic content will be reduced because more pulses per cycle in the output wave are obtained. This technique is only widely used in the analogue domain because of its simplicity and ease of implementation using analogue techniques.

3.1.2 Time Optimal Switching Strategies

The time optimal strategies are described in Chapter Two. A similiar but simplified delta modulation strategy [Ziogas - 1981] is proposed for inverter switching.

This method, shown in Fig.3.3, utilises a sine reference waveform V_R and a delta shaped carrier waveform V_C. The latter is allowed to oscillate within a defined window which has limits equally above and below the sine reference waveform V_R. The maximum carrier frequency f_{cmax} can be determined from the minimum window width and the maximum carrier slope.

The technique is to provide inherent constant volts/Hz control for a preset frequency range, a smooth transition of PWM to square-wave mode of operation and also to provide severe attenuation of low order harmonics [Ziogas - 1981, Rahman et al - 1985]. This method also ensures that a minimum number of components are used when it is implemented using analogue techniques as shown in Fig.3.4.

3.1.3 Optimal Switching Strategies

Harmonic elimination [Turnbull - 1964, Patel and Hoft, Part I - 1973 and Part II - 1974]

and optimised switching strategies [Buga and Indri - 1977, Casteel and Hoft - 1978, Issawi et al - 1982] are used to maximise a specified performance criteria such as minimisation or elimination of particular voltage harmonics or minimisation of current harmonic distortion etc. It is recognised that these switching strategies can offer significant advantages, even at low frequency ratios, therefore the total harmonic voltage/current distortion can be minimised with minimum switching losses.

These optimised switching strategies do not rely upon a well defined and recognisable modulation process of the kind associated with the natural sampled and the regular sampled strategies [Bowes - 1988]. All optimised PWM strategies are therefore, essentially developed off-line using a mainframe computer and numerical minimisation techniques to determine the optimised switching angles. Such optimised PWM switching angles are subsequently stored in the microprocessor's memory and used on-line to generate the PWM pulses in real-time. Thus, there is considerable time, effort and computing resources involved in the development of these optimised switching strategies and also its implementation often requires good switching angle resolution to achieve the predicted performance criteria. These complexities have prevented the use of the optimal strategies in many PWM inverter applications [Bowes - 1988 and MOTOR-CON88].

3.1.4 Regular-Sampled Switching Strategies

The regular-sampled PWM strategy is based on a comparison of the regularly-sampled sinusoidal modulating waveform with the triangular carrier waveform. It is a well defined modulation process and is proposed by [Bowes - 1975]. The regular-sampled PWM strategies are inherently digital, and therefore can be very efficiently implemented using either discrete digital hardware, LSI or microprocessor software techniques.

The regular sampling basically entails the sampling of the modulating wave prior to the comparison with the carrier wave. However, the rate at which the modulating wave is sampled depends upon firstly the carrier frequency and secondly the type of modulation process which could be categorised into two, namely, asymmetric and symmetric modulation processes. The regular-sampled strategies can thereby be split up into two, namely, regular-sampled asymmetric PWM strategy and regular-sampled symmetric PWM strategy.

3.1.4.1 Regular-Sampled Asymmetric PWM Strategies

In this scheme a sinusoidal modulating waveform is sampled at both positive and negative peaks of the triangular carrier waveform to generate "sample and hold" equivalent of the modulating waveform for comparison with the carrier waveform. As a result of the comparison held between these waves, the resultant PWM pulses are determined as shown in Fig.3.5. The width of the resultant asymmetrically modulated pulse may be defined in terms of these sampling times as shown in Fig.3.6 and can be calculated by the following equation.

$$T_p = \frac{T}{2}\left[1 + \frac{M}{2}(\mathrm{SIN}w_m t_1 + \mathrm{SIN}w_m t_3)\right] \tag{3.2}$$

It is to be noted that the modulating waveform is sampled at twice the carrier frequency. The method therefore provides more precise but asymmetrically modulated pulses. Its harmonic spectrum is superior to that produced using symmetric modulation. However, it significantly extends the time required for computation when it is implemented by a microprocessor using software techniques.

Further, two new versions of this strategy are now available in the literature which are, namely, the modified asymmetric regular sampled PWM strategy [Acharya et al - 1984] and the suboptimal PWM strategy [Bowes and Midoun - 1985].

3.1.4.1.1 Modified Asymmetric Regular-Sampled PWM Strategy

This scheme uses the sampling height by averaging the two successive regularly sampled points taken at both positive as well as negative peaks of the carrier triangular wave as shown in Fig 3.7.

The width of the resultant pulses may be defined by the following equation [Acharya et al - 1984]:

$$T_{pw(n+1)} = T[1 + (-1)^n M\ \mathrm{SIN}(2n - 1)T] \tag{3.3}$$

where $T_{pw(n+1)}$ = Width of (n+1)th pulse in degrees and n varies from 1to (P-1)/2 ,

T = Period in degrees i.e. 360/4P ,

P = Ratio of the carrier to the modulating waveform ,

and M = Depth of modulation to be used.

This is capable of generating more accurate switching angles, consequently it produces a waveform with lower harmonic distortion.

3.1.4.1.2 Suboptimal PWM Strategy

In contrast to other optimal strategies, the suboptimal PWM strategy [Bowes and Midoun - 1985] uses well established regular sampling techniques, together with a modified modulating signal to obtain optimised switching angles. The modulating waveform is assumed to be an arbitrary non-sinusoidal waveform as shown in Fig.3.8. The regular sampling process has made it possible to define the PWM switching angles, α_k, directly in terms of the non-sinusoidal modulating wave samples $m(T_k)$, using the following equation:

$$\alpha_k = T_k + (-1)^{k+1}\frac{T_c}{4}m(T_k) \qquad (3.4)$$

where $T_k = k\,T_c/2$ = is the sampling instant

Additionally, the harmonic spectrum of the resultant waveform for odd n can be expressed in terms of switching angles as given below :

$$A_n = \frac{4}{n\pi}\left[1 + 2\sum_{k=1}^{N}(-1)^k \mathrm{COS}(n\alpha_k)\right] \qquad (3.5)$$

where N = The number of switches in a quarter-cycle.

By combining the above two equations, a direct relationship can be obtained [Bowes and Midoun - 1985] between the optimal sampled modulating waveform, $m(T_k)$, and the harmonics of the optimised PWM waveform. After a detailed computer analysis, an optimal

modulating waveform $m(T_k)$ is used which is closely approximated by a modulating signal m(t), consisting of a sinewave plus third harmonic, of the form :

$$m(t) = M[SIN(wt) + \frac{1}{4}SIN(3wt)] \tag{3.6}$$

where m(t) is independent of frequency ratio which varies linearly with modulation depth, M.

Thus, pulse-widths in the suboptimal PWM strategy can be defined by the equation :

$$T_k = \frac{T_c}{2}[1 + \frac{1}{2}\{m(t_k) + m(t_{k+1})\}] \tag{3.7}$$

where $m(t_k)$ represents the sampled values of m(t) at regular sampling instants t_k.

In contrast to the previously described optimal switching strategies, this scheme is based upon the well defined modulation process (Regular Sampling Technique) and a linear relationship exists between the voltage of the fundamental component and the modulation index, M.

3.1.4.2 Regular-Sampled Symmetric PWM Strategies

This is the simple PWM strategy. In this strategy, the sinusoidal modulating waveform is sampled at every positive peak of the triangular carrier waveform prior to the comparison to be made with the carrier waveform as shown in Fig.3.9. It can be seen from Fig.3.6 that the width of each resultant pulse is determined by a single sample-and-hold value of the modulating waveform, leading to the conclusion that both edges of the resultant pulse are equidistant from their centre points.

With reference to Fig.3.6 the width of the resultant pulse for symmetric double-edge and single-edge modulation can be expressed as [Bowes and Mount - 1981, Bowes and Clements - 1982]

$$T_p = \frac{T}{2}[1 + M\,SIN(w_m t_1)] \qquad (3.8)$$

where T is the time period of a carrier signal.

In contrast to the asymmetric regular-sampled technique, the symmetric regular-sampled technique requires the sampling frequency equal to the frequency of the carrier signal. Thus, it has the advantage of requiring less processing time over the preceding PWM strategy when it is implemented by a microprocessor using software techniques.

3.1.5 The Importance Of Carrier Signal In PWM Strategies

In most of the PWM strategies, the switching angles are determined in relation to the carrier signal. Thus, its shape, the ratio of the carrier signal to the modulating signal and its time-phase relationship with the modulation waveform have certain important consequences on the quality of the output waveform. The following sections illustrate the effects of a carrier signal on the output waveform for various categories of PWM techniques.

3.1.5.1 Single-Edge And Double-Edge PWM

The natural-sampled and regular-sampled PWM strategies can be implemented either using single-edge or double-edge modulation. As shown in Fig.3.2 double-edge modulation results by the comparison made between the sinusoidal modulating waveform and the triangular carrier waveform, whereas the single-edge modulation process uses a saw-tooth waveform as the carrier signal for comparison with the sinusoidal modulating waveform as can be seen from Fig.3.10. Thus, for single-edge modulation, the change in modulation index M results only in one-edge being modulated, the other edge of the PWM pulse remaining fixed (unmodulated), contrary to the double-edge modulation process. Although single-edge modulation results in a waveform with greater subharmonic content than a double-edge modulated waveform, at high frequencies the amplitude of the subharmonics in both types would be significantly reduced and may be considered negligible. Single-edge modulation has the advantage of requiring less components as compared to double-edge modulation [Khan and Manning - 1988].

3.1.5.2 Asynchronous And Synchronous PWM

In general the PWM waveforms are generated as a result of the comparison made between a modulated wave and a carrier wave. If the carrier signal is not synchronised in time-phase with the modulating waveform, the PWM generation process is said to be asynchronous. In this process a fixed frequency carrier signal is used which means that at all output frequencies, the ratio of the carrier frequency to the output frequency is not an integer. It has been shown [Jayne et al - 1977] that the output waveform can contain components of a lower frequency than the wanted components and even a DC component i.e. zero frequency can appear in the output waveform at certain frequency ratios. During over modulation, the carrier frequency and modulating frequency are generally non commensurable, and pulses would appear and disappear cyclically. This will give rise to further undesirable frequency components in the output waveform.

In the synchronous PWM strategy, the carrier frequency is always an integer multiple of the modulating frequency. As a result of the synchronism existing between the two waveforms, all the unwanted frequency components which appear in the PWM waveform will be a multiple of modulating frequency, f_m. The lowest frequency harmonic will be at twice f_m and no low frequency components, other than the fundamental will appear [Jayne et al - 1977]. Several contradictory statements can be seen in the literature about the carrier frequency to the modulating frequency ratios for various synchronous PWM strategies. Firstly it is concluded [Pollman - 1982] that the odd frequency ratios which are multiples of three produce better harmonic spectra than the even frequency ratios. In some papers [Zubek et al - 1975, Grant and Barton - 1980, Green and Boys - 1982] it is described that the frequency ratio must be an odd multiple of three whereas Varnovitsky [Varnovitsky - 1983] showed, after detailed analysis, that even frequency ratios multiple of three produce better harmonics spectra.

However, when a single carrier signal is used to generate synchronous PWM pulses for three-phase system, it eliminates the need for the frequency ratio to be odd and multiple of three. Thus any suitable carrier frequency may be utilised to generate the PWM pulses for three-phase [Khan and Manning - PESC89]. Only odd harmonics (3rd, 5th, 7th, 9th, ... ∞) will be generated in phase voltage whereas harmonics multiple of three would be cophasal and thereby produce no current in a suitably connected three-phase load.

It has been shown [Jayne et al - 1977, Grant and Seidner -1981] that the synchronous PWM method is much superior to the asynchronous PWM scheme with regard to THD. The only criticism about the synchronous operation is that since the carrier and the modulating waveforms have to be synchronised, the carrier frequency must vary over as wide a range as the output frequency. This scheme could advantageously be used in inverters for UPS applications where output frequency is essentially constant [Khan and Manning - 1988].

3.1.5.3 Ultrasonic Carrier Signal

All PWM schemes use a carrier signal at a frequency several times higher than the modulating frequency. From the preceding PWM strategies, it is clear that the harmonic content in the PWM waveform can be improved significantly if α higher frequency ratio of the carrier signal to the modulating signal is used. As the ratio of the carrier to modulating frequency is increased, the side bands of the carrier frequency will also move away from the fundamental component.

Advances in power MOSFET and bipolar transistor technologies allow the switching frequency of the inverter to be increased up to several tens of kHz. The use of carrier frequencies above the audio range have some important consequences which may be summarised as follows :

1. At higher switching frequencies, the significantly improved harmonic spectra of the output waveform makes it practical to apply the simplest regular-sampled symmetric strategy, either implementing with single-edge or double-edge modulation [Khan and Manning - UPEC88].

2. A high ratio of the carrier to the modulating frequency provides the wide separation of the fundamental frequency component and the least desirable frequency components in the output waveform. Thus, output filtering can be accomplished with relatively small and inexpensive components.

3. By using ultrasonic carrier frequencies, inverters can be realised without the acoustic noise associated with the magnetic components.

4. Raising the ratio of the carrier to the modulating frequency gives more precise control over the output waveform synthesisation. By choosing a suitable method of generating the PWM pulses, a phase synchronisation technique can easily be devised based upon the addition or subtraction of a segment, equal to a period of the carrier signal, from the output waveform [Khan and Manning - PEVDs 88].

5. By choosing a suitable ratio (i.e. 360) of the carrier to the modulating frequency, a scheme based on software can be utilised to generate exactly the 120^{o} phase displacements required by three phase systems [Khan and Manning - PESC 89].

6. High switching frequencies could decrease the inverter efficiency because of the switching and snubbing losses. These losses can be minimised by incorporating fast switching devices such as power MOSFETs which can be operated without snubbing networks.

7. One difficulty which can arise due to the use of a high carrier frequency for a microprocessor controlled PWM generator, is that the time available to the microprocessor for pulse width computation is very short. In a three-phase system using an 18 kHz carrier frequency, the widths of the three pulses have to be calculated within 55.55 microseconds. A very fast microprocessor with an efficient instruction set is therefore needed, since it is required that it implements all other functions in software required by such inverters.

3.1.6 The Choice Of The Microprocessor

To meet the abovementioned system requirements a microprocessor with a very fast processing speed is needed. The most important considerations in designing a microprocessor controlled PWM generator are the type of microprocessor together with its instruction set to be used, the speed at which it can be clocked and the programming language to be employed for software development.

The main requirements of the system are that it has to handle 8-bit data to generate the PWM pulses and that 16-bit calculations are to be performed to implement some control tasks. Thus, the 16/8 bit 8088-2, 8 MHz microprocessor manufactured by Intel corporation was chosen. This microprocessor has a 16-bit internal architecture with an 8-bit data bus and 20-bit memory address range. The 8088 CPU provides longer access times to

peripherals due to its modern architecture (i.e. pipe-line). This makes it possible for slow devices to be interfaced with the microprocessor without generating wait-states. The instruction set provides twenty four different addressing modes, and this enables the microprocessor to address the complex data structure in a single instruction. To enhance the arithmetic and input/output capabilities of the 8088 microprocessor, the Intel 8087 numerical processor and the 8089 input/output processor can be used in parallel with the microprocessor.

3.1.7 Summary Of PWM Strategies

In the previous sections some well established PWM strategies, which could be used in UPS applications, have been discussed. These are summarised as follows : The natural sampling and delta modulation switching strategies are mostly implemented using analogue components. The computer aided analysis of these two strategies is quite complex and also their implementation, using discrete digital components or by software in microprocessor controlled systems, is also rather complicated and may result in the use of a large number of components. Consequently, the implementation of both strategies is not attractive for microprocessor controlled PWM generators.

Since the harmonic elimination and optimal switching strategies require precalculated switching angles to maximise certain performance criteria, determination of switching angles involves considerable time, effort and computing resources and their implementation also demands good switching angle resolution. It is difficult to change both edges of the PWM pulses symmetrically when the modulation depth is increased/decreased in an attempt to regulate the output voltage under different load conditions. These problems have prevented the use of optimal PWM strategies in UPS applications.

Finally, the regular-sampled strategy is well established and now exists in many variations :

* Asymmetric PWM strategies
* Modified asymmetric PWM strategy
* Suboptimal PWM strategy
* Symmetric PWM strategy.

The symmetric PWM strategy has the advantage over the other strategies of requiring less computation time since this uses one sample to determine both edges of a pulse, whereas all the other techniques require two samples per carrier period. Although the quality of the

output waveform is determined by the number of samples being taken to define a modulating waveform, the symmetric PWM strategy can generate output waveform of similar quality as that generated by the others especially when the higher ratio of the carrier frequency (18 kHz) to the modulating frequency (50 Hz) is to be employed. The regular-sampled symmetric PWM strategy is chosen to be used in single-phase and three-phase microprocessor controlled PWM generators using single-edge as well as double-edge modulation.

3.1.8 The Chosen PWM Strategy

The simplest regular-sampled symmetric PWM strategy has been adopted for use in generating the PWM pulses as shown in Fig.3.9. Since the modulating and carrier waveforms are synchronised, the first sampling instant t_1 will be equal to $T_c/4$. The first high level pulse width can therefore be expressed by the following equation :

$$T_{HA1} = \frac{T_c}{2}\left[1 + M\sin w_m\left(\frac{T_c}{4}\right)\right] \tag{3.9}$$

Because in the symmetric PWM strategy the modulating signal is sampled once in each carrier period, the second sampling instant t_2 will be held at time instant $(T_c + T_c/4)$. The second high level pulse width is then given by :

$$T_{HA2} = \frac{T_c}{2}\left[1 + M\sin w_m\left(\frac{T_c}{4} + T_c\right)\right] \tag{3.10}$$

and the jth high level pulse T_{HAj} is given by

$$T_{HAj} = \frac{T_c}{2}\left[1 + M\sin w_m\left(\frac{T_c}{4} + jT_c\right)\right] \tag{3.11}$$

For achieving double-edge modulation, the corresponding low level pulse is given by the equation [Tez and Akhrib - 1985] :

$$T_{LAj} = T_c - \left(\frac{T_{HA(j-1)} + T_{HAj}}{2}\right) \tag{3.12}$$

The Eqn.(3.12) involves an addition, a division and a subtraction to obtain the low level pulse widths. The calculation of T_{LAj} can be simplified as follows; since both edges of the PWM pulses are determined by a single sample, both edges are equally modulated or displaced with respect to their centre points as shown in Fig.3.11. One carrier period can be expressed as :

$$T_c = X_{LAj} + T_{HAj} + X_{LBj} \tag{3.13}$$

and

$$T_c - T_{HAj} = X_{LAj} + X_{LBj} \tag{3.14}$$

X_{LBj} and X_{LAj} are the low level pulses before and after the high level pulse width T_{HAj} corresponding to a carrier period. It can be clearly seen from the above equation that the widths of the low level pulses (X_{LAj} and X_{LBj}) depend on the high level pulse width and the carrier period. Since the widths of both these pulses are equal in value by virtue of the symmetric strategy and the carrier period is constant, the widths of the low level pulses X_{LAj} and X_{LBj} in relation to the prospective carrier period and high level pulse width, T_{HAj} can be calculated from the following equation [Khan and Manning - PEVDs88].

$$X_{LAj} = X_{LBj} = \frac{T_c - T_{HAj}}{2} \tag{3.15}$$

The above equation may be solved in software by the microprocessor. One mathematical operation in generating T_{LAj} is eliminated because the high and low level pulses are produced in relation to the prospective carrier period. This is achieved by the use of two counters and by the inclusion of the carrier signal as a real time reference waveform to generate the PWM pulses.

The complete low level pulse T_{LAj} between the two consecutive high level pulses, $T_{HA(j-1)}$ and T_{HAj}, is automatically constructed from

$$T_{LAj} = X_{LA(j-1)} + X_{LBj} \tag{3.16}$$

This technique is devised to overcome the problems inherent in microprocessor controlled generators which will be explained later in detail in Chapter Four.

To achieve single-edge modulation a sawtooth carrier signal is used for the comparison with the symmetrically sampled sinusoidal modulating waveform. With reference to Fig.3.12, a low level pulse width T_{LAj} can be calculated directly from the difference between the carrier period and the high level pulse width [Khan and Manning - UPEC88]:

$$T_{LAj} = T_c - T_{HAj} \tag{3.17}$$

The pulse width expressions for the other phases B and C of the three-phase system can be obtained by introducing phase displacements of 120^o and 240^o into the sine term of Eqn.(3.11).

Since counters are to be employed to generate the required pulse widths and are decremented at each period of the counter's clock, the actual integer number, ITN_j corresponding to a particular pulse width, and which is to be loaded into the counter, is obtained by multiplying the high level pulse width, T_{HAj} by the counter's clocking frequency, f_{ck} . These integer numbers are therefore obtained by solving the equation.

$$ITN_j = f_{ck} \cdot T_{HAj} \tag{3.18}$$

In a similar manner, integer numbers corresponding to the low level pulses X_{LBj}, X_{LAj} and T_{LAj} can be obtained to implement double-edge and single-edge modulation. The corresponding equations may be written as

$$ITN_{Dj} = f_{ck} \cdot X_{LAj} \tag{3.19}$$

for double-edge modulation and

$$ITN_{Sj} = f_{ck} \cdot T_{LAj} \tag{3.20}$$

for single-edge modulation.

As can be seen from Eqns.(3.11) and (3.18), the calculation of the integer numbers corresponding to the pulse widths T_{HAj} involves additions, multiplications and a sine function. Thus, if Eqns.(3.11) and (3.18) are to be solved on-line, considerable time consuming computations would be required to obtain the integer numbers ITN_j. A software-based implementation using a general purpose microprocessor is therefore not possible especially when a high carrier frequency is to be utilised. It was therefore decided to calculate off-line the integer numbers corresponding to the high level pulse widths. To maintain the output voltages at a fixed level under different supply voltages and load conditions, Eqn.(3.18) is solved for M=0.75 to 0.975 with a step of 0.005. The equation is solved for a quarter of a cycle and the results are stored in the form of look-up-tables.

For similar reasons Eqns.(3.19) and (3.20) cannot be used directly to calculate on-line the integer numbers corresponding to the low level pulse widths. However, if T_{HAj} is known in the integer domain (ITN_j), the integer number ITN_{Dj} corresponding to the low level pulse widths for double-edge modulation can be calculated on-line by solving Eqn.(3.15) directly in integer domain.

The integer numbers ITN_{Sj} corresponding to the low level pulse widths for single-edge modulation may be more easily realised on-line as a byproduct of the technique used to generate the PWM pulses as explained in Chapter Four.

3.2 METHODS OF CALCULATING THE LOOK-UP-TABLE DATA

As explained above, the calculations involved in solving Eqns. (3.11) and (3.18) are performed off-line and the results stored as look-up-tables in the memory of the system. This scheme therefore increases the throughput of the general purpose microprocessor

which would also be capable of performing more efficiently the other functions required by the system. There are two methods of performing the off-line calculation of the look-up-table (LUT) data during initialisation and calculation of LUT data using a separate system.

3.2.1Calculation Of LUT Data During Initialisation

This technique requires the use of additional hardware or software packages with the existing microprocessor to perform the required calculations. The hardware component may consist of an Intel 8087 numerical processor which can be used as a parallel processor. This numerical processor is expensive and, if used would add to the cost and complexity of the system. For these reasons an alternative method namely, emulation of 8087 by software, was considered.

Since an Intel 8088 microprocessor is to be used, the trigonometric and arithmetic capabilities of the 8087 may be realised by using its emulation software instead of employing the 8087 itself. The full 8087 emulator is a software package which completely and exactly duplicates all the functions of the 8087. This method requires two source programs to be used [Khan and Manning - UPEC88], one in pascal-86 and another in ASM86 for solving Eqns. (3.11) and (3.18). These two source programs are separately compiled and their object files are linked with the necessary run-time support libraries supplied with pascal-86 [Intel Corporation, Pascal - 86 software manual - 1986] and the object file of the program used to generate the PWM pulses. This method requires nearly 32 K bytes of memory space and takes a considerably long time which is deemed unacceptable.

3.2.2Calculation Of LUT Data On A Separate System

The disadvantages of the previous method can be overcome by calculating the LUT data on a separate system. Usually, this involves the use of a separate computer for the calculations of LUT data which is then transferred into the memory by a typing-in process. When the LUT data is large, the transferring process becomes time consuming and cumbersome [Khan and Manning - PEVDs88].

Since an Intel series III was used to develop the software for an Intel 8088 microprocessor, a small program (PROG1.SRC) was written [Appendix I] in pascal-86 to

solve Eqns.(3.11) and (3.18). The object file of the program is linked to the necessary run-time support and interface libraries (P86RN0.LIB, P86RN1.LIB, P86RN2.LIB, P86RN3.LIB, CELL.87, EH87.LIB, 8087LIB and LARGE.LIB) available in directory named PASC86.86 [Intel Corporation, Pascal-86 Software manual, 1986]. The resultant linked object file is made 'RUN' thereby computing the integer numbers ITNj and storing these in the form of look-up-tables in a newly opened file, 'Tables' [Appendix II].

The main program (for generating the PWM pulses and to implement other controls) is written in assembly language[Appendix III]. The concept of modular programming is utilised and therefore the object files are linked together and relocated using an 8086-based LINK.86 and LOC.86 respectively.

3.3 CONCLUSIONS

The synchronous regular-sampled symmetric PWM strategy is chosen since it has the advantage over other PWM schemes of requiring a minimum number of calculations to generate the PWM pulses. The equations derived to calculate the low level pulses require less computation time and enable the system to generate low and high level pulses corresponding to the prospective carrier period.

In addition, this technique effectively divides the output wave into equal segments which may be used for synchronisation purposes and to generate three-phase output waveforms with the exact phase relationships.

The method chosen for calculating the LUT data utilises the same system used to develop the software for the microprocessor.

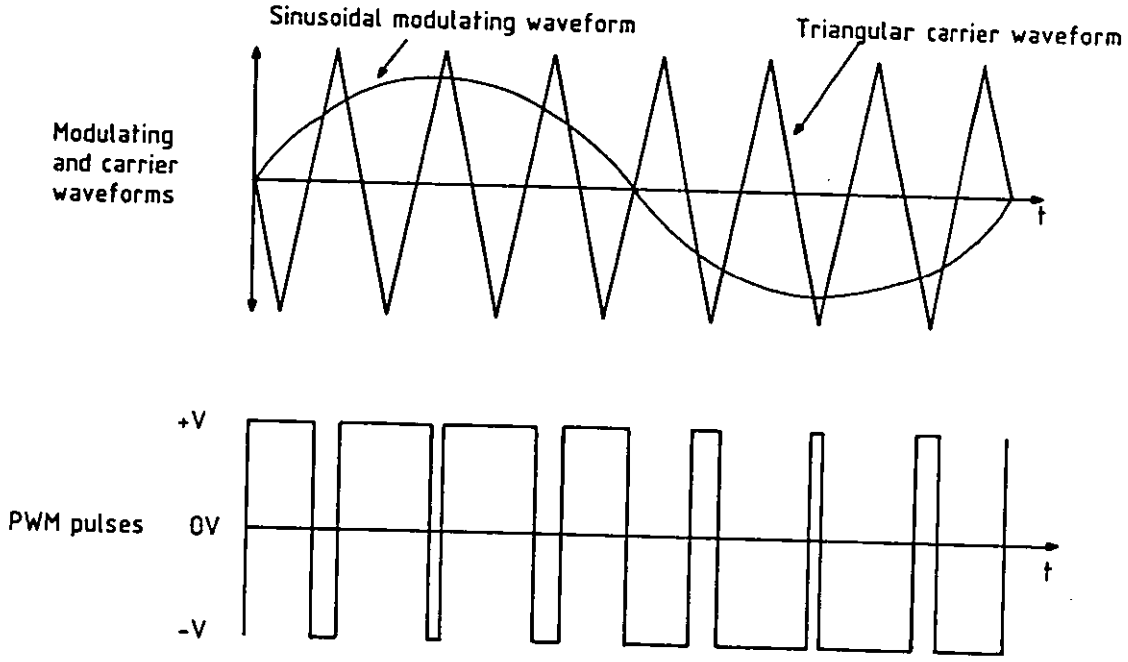


Fig. 3.1. Natural - sampled PWM process.

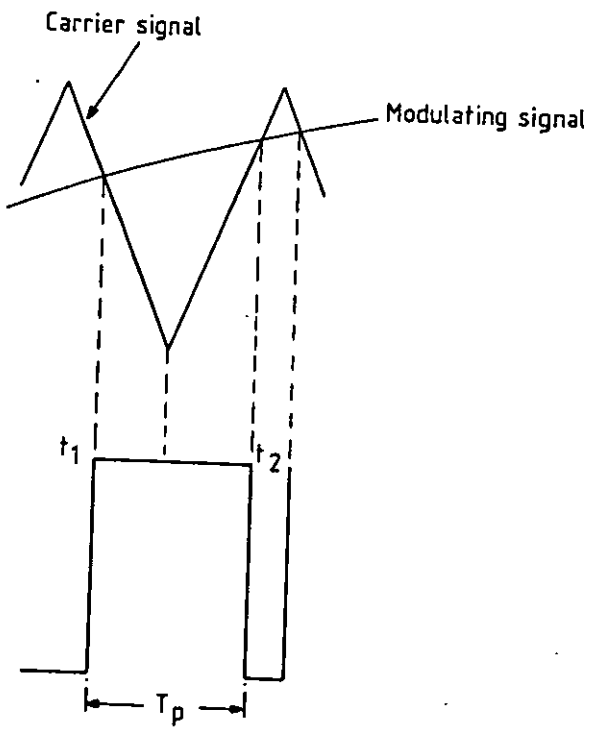


Fig. 3.2. Details of single pulse for natural-sampled PWM.

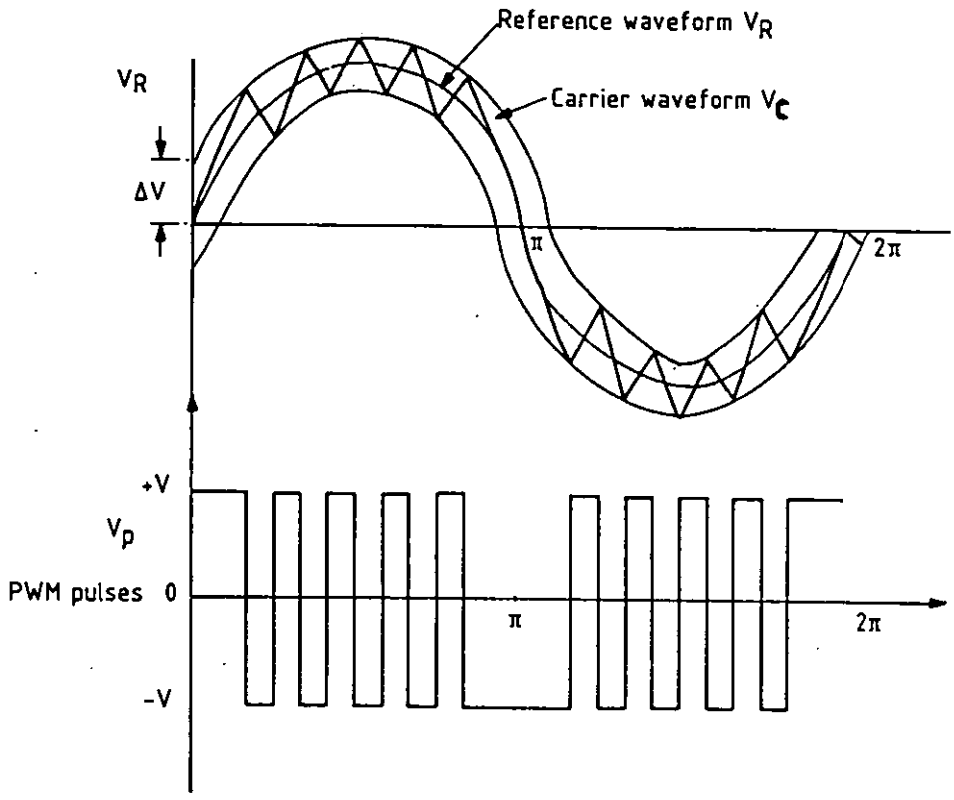


Fig. 3.3. Delta modulation waveforms.

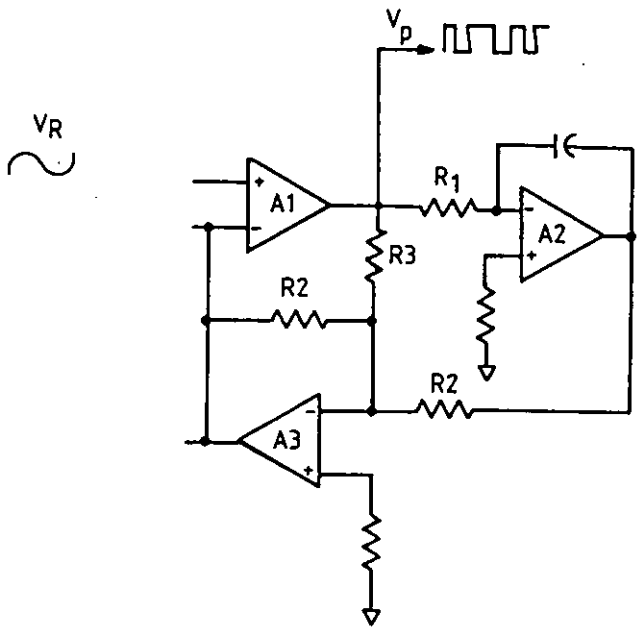


Fig. 3.4. A practical circuit for generating Delta-modulated pulses.

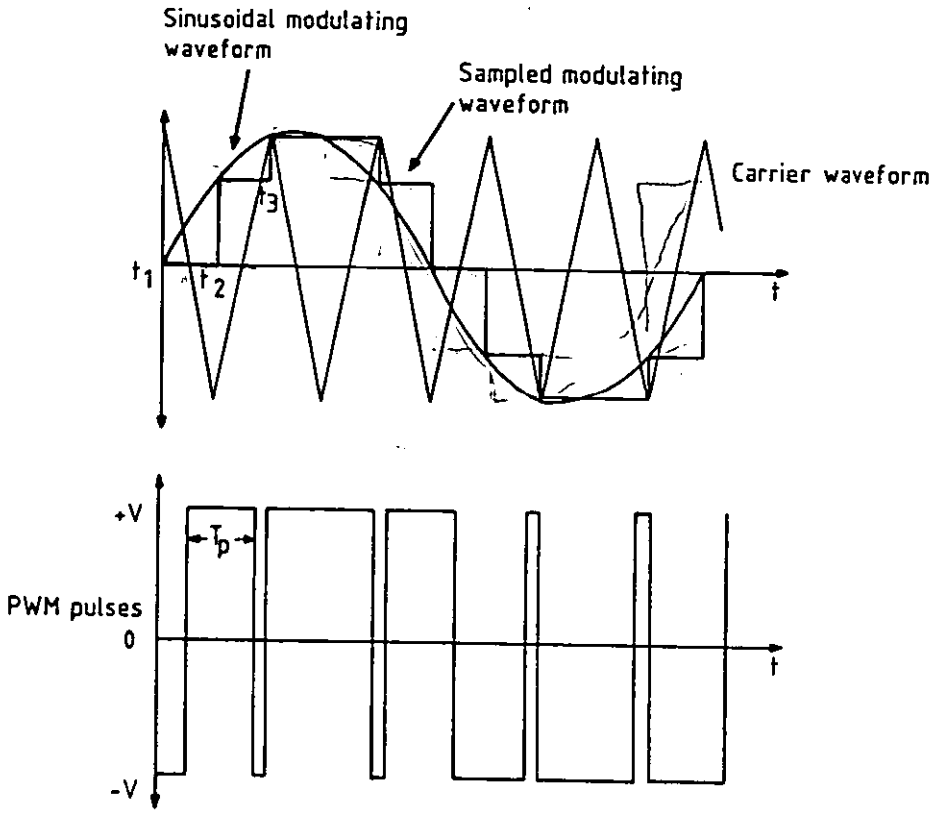


Fig. 3.5. Regular-sampled asymmetric PWM process.

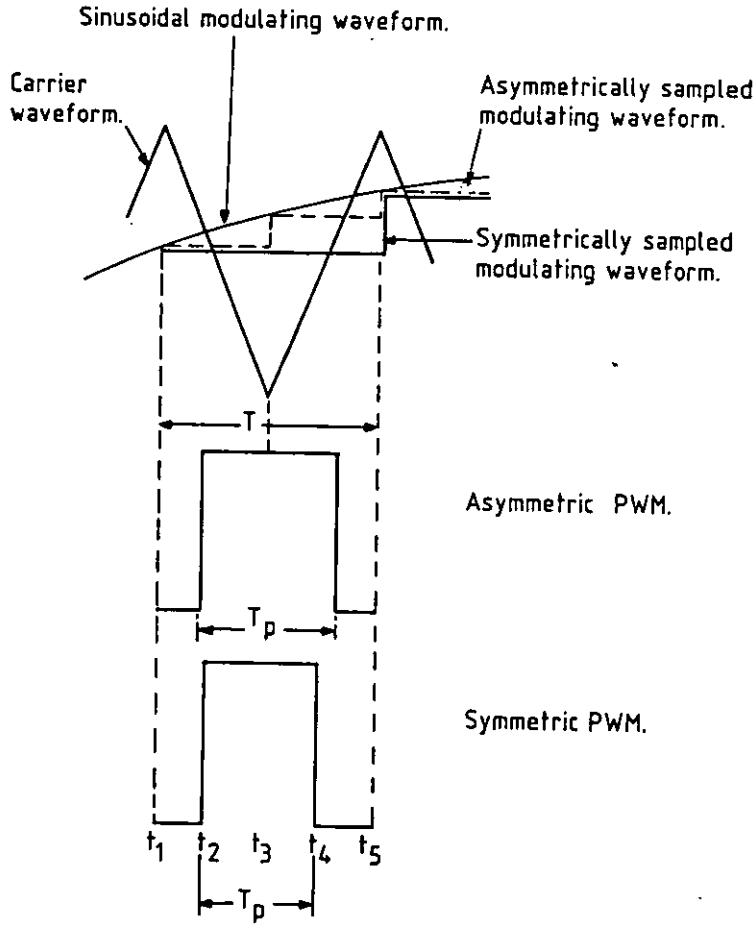


Fig. 3.6 REGULAR-SAMPLED ASYMMETRIC AND SYMMETRIC PWM.

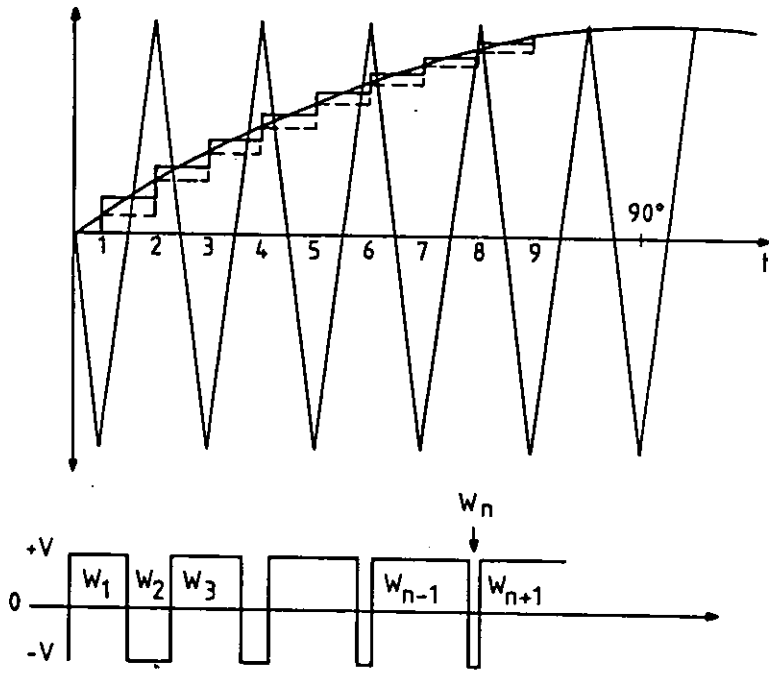


Fig. 3.7. Modified regular-sampled asymmetric PWM process.

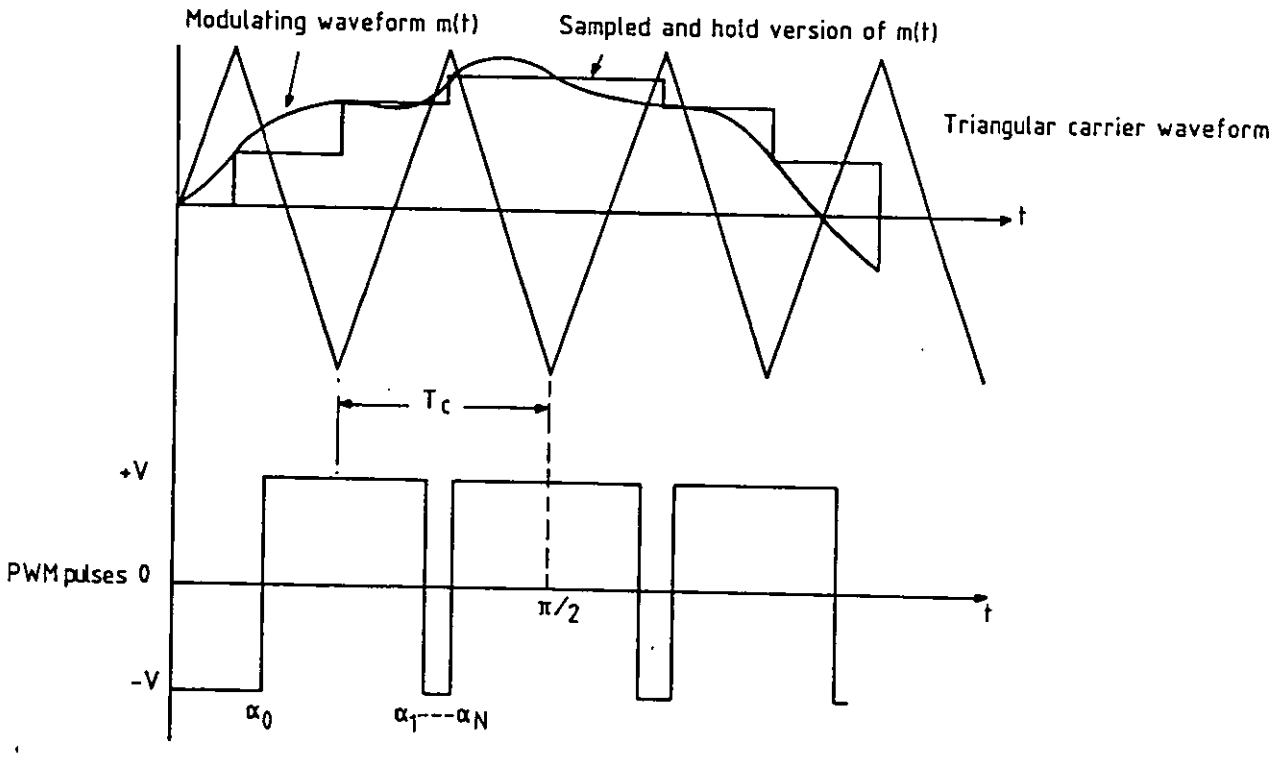


Fig. 3.8. Suboptimal regular-sampled asymmetric PWM process.

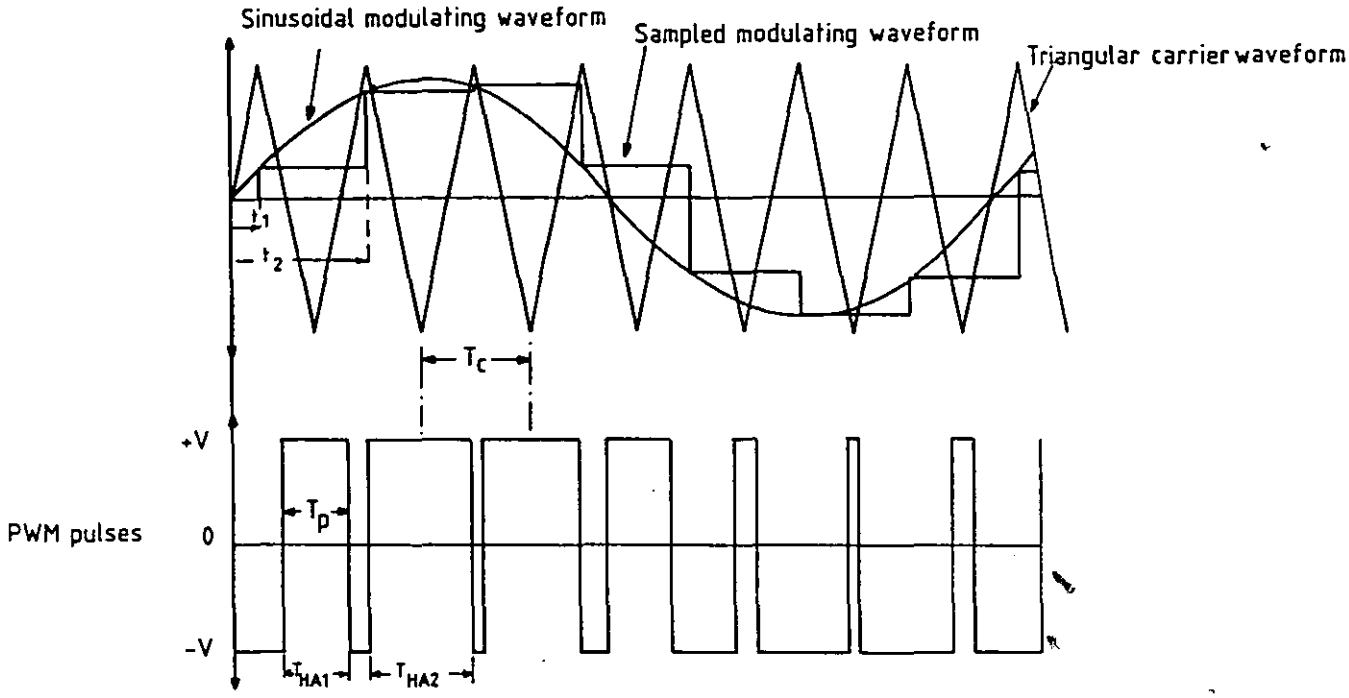


Fig. 3.9. Regular - sampled symmetric PWM process.

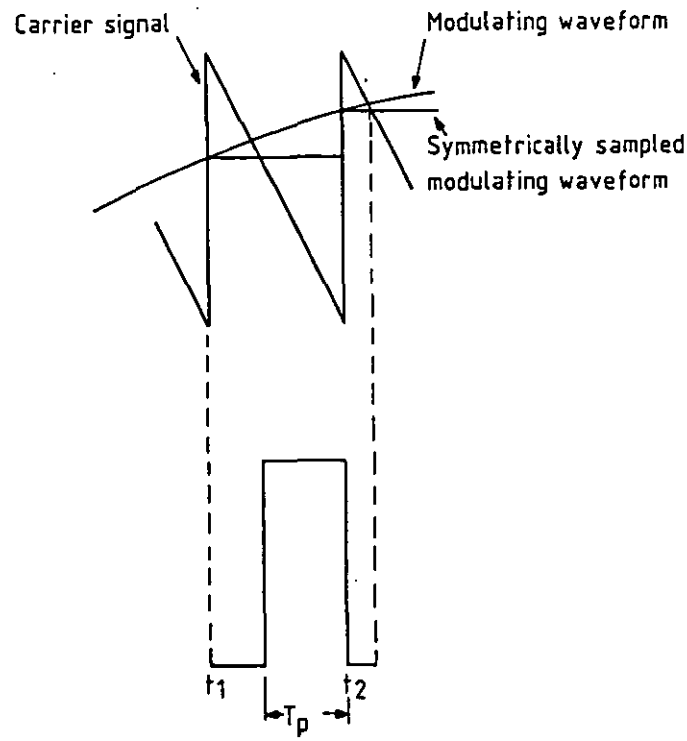


Fig. 3.10. Single-edge modulation process.

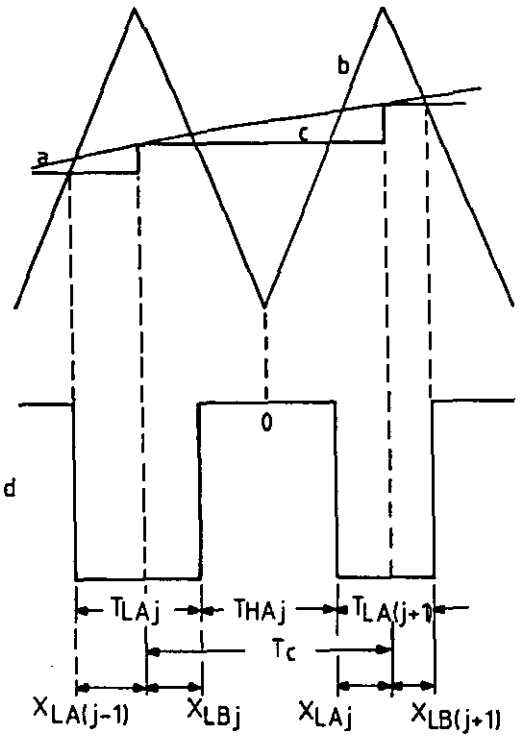


Fig. 3.11. Symmetric regular sampled double-edge PWM

(a) Modulating signal
(b) Carrier signal
(c) Sample hold modulating signal
(d) PWM signal

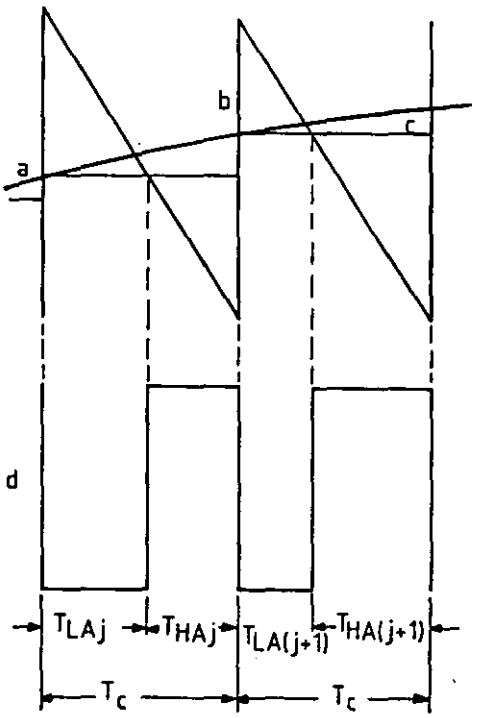


Fig. 3.12. Symmetric regular sampled single-edge PWM.

(a) Modulating signal
(b) Carrier signal
(c) Sample/hold modulating signal
(d) PWM signal

CHAPTER FOUR

CONTROLLER AND IMPLEMENTATION OF REGULAR SAMPLING STRATEGIES

This chapter describes the design of a multi-purpose microprocessor controller board and the construction of associated circuitry required for single-phase and three-phase inverters. Single-edge as well as double-edge modulation has been implemented for both cases employing the 18 kHz carrier frequencies.

This chapter also describes the successful implementation of the proposed techniques to overcome the problems associated with microprocessor controlled generators.

4.1 SYSTEM HARDWARE DESIGN

The central part of the system hardware is a microprocessor controller board, the design of which will be described in detail. This chapter also includes the design of the gate drive circuitry, interface feedback board, single-phase and three-phase MOSFET inverters. Other control circuits are described in the appropriate chapters.

4.1.1 The Microprocessor Controller Board

The microprocessor controller board is shown in Fig.4.1. The multipurpose microprocessor board, based on an 8 MHz 8088D-2 CPU, is wired-up in minimum mode with demultiplexed bus. This means that no provision is made for parallel processing. Since several peripherals have to share the address lines as well as data bus lines, two 74LS373 latches and a 74LS245 transceiver are used to provide heavy bus buffering. The 8088D-2 CPU provides $\overline{\text{DEN}}$ and DT/$\overline{\text{R}}$ to control the transceiver and ALE to latch the addresses.

To generate the clock signal required by the 8088D-2 CPU, an 8284A clock generator is utilised with a 24 MHz crystal which provides two clock signals of different frequencies at pins CLK and PCLK. The CLK output is one third of the crystal frequency and is used to drive the CPU and PCLK is a peripheral clock whose output is a half of the CLK output. The PCLK clock signal is used for measurement purposes and to generate other reference

clock signals.

The memory space and I/O space are treated in parallel by the 8088 processor but collectively called memory structure or mapping. A one megabyte space is available for memory addressing and this can be divided into four arbitrary segments (CS, DS, SS, ES), each containing at most 64k bytes but the first 256 ports are directly addressable, whereas the addresses of the other ports need to be moved in register DX. The address lines A12-A15 and signal IO/$\overline{M}$ are used to select the memory devices, and the address lines A3-A7 and IO/$\overline{M}$ signal are used for decoding the other peripheral devices by employing two 74S288 PROMs as shown in Fig.4.1. The detail of the memory addresses and I/O peripherals addresses are shown in the memory mapping diagram in Fig.4.2.

The memory of the controller consists of an 8K bytes type HN27C64G-15 Eraseable-Programmable-Read-Only-Memory (EPROM) and a 32K bytes type HM62256P-12 Random-Access-Memory.

An 82C59A-2 Programmable Interrupt Controller (PIC) is used to interrupt the microprocessor in real-time since interrupt driven software is to be utilised. The PIC is programmed in the edge-triggered and automatic end-of-interrupt modes [Intel Corporation Vol.I]. This device can cause an interrupt by pulling one of the 82C59A's interrupt request pins (IR0-IR7) high. Only two interrupt request pins, IR0 and IR1, are utilised. All unused interrupts are masked off as well as interrupt request pins are strapped to ground to avoid false triggering. Interrupts caused by the signals at these pins are known in software by INTR72 and INTR73 respectively. INTR72 is caused by the 18 kHz frequency carrier signal to generate the PWM pulses in real-time, whereas INTR73 is being generated at 1.11ms intervals to implement the PI control algorithm. Since INTR72 has top priority and is being generated at 55.55 μs intervals, it will be serviced several times during INTR73 routine servicing.

An 82C55A Parallel Peripheral Interface (PPI) is used to interface the hardware circuitry utilised to calculate Eqn.(3.15) on-line as is required to generate double-edge modulated three-phase PWM pulses. This device is programmed as three independent output ports PORTA, B, and C. The detail of the hardware utilised for this purpose will be given in the PWM generation section. A 2516 EPROM is used to interface the feedback circuit with the microprocessor controller board.

Five 8254 Programmable Interval Timers (PIT) CTA, CTB, CTC, CTD and CTE are utilised and each counter has three independent 16-bit counters which can be programmed in a variery of modes [Intel Corporation Vol.II]. The counter CTA1 is programmed in a square wave mode to generate the 18 kHz carrier signal and its connections are shown in Fig.4.1. The counters CTA0 and CTA2 are programmed in square wave and hardware retriggerable one-shot modes respectively. The functions of these counters are to provide interrupt signals to start the sample and hold process and to interrupt the microprocessor at intervals of 1.11ms to implement the PI control algorithms. The timing waveform diagram is shown in Fig.4.3.

The counters CTB0, CTB1 and CTB2 of CTB are used to generate the PWM pulses and are programmed in hardware retriggerable one-shot modes. The particular pin connections scheme, shown in Fig.4.1, is used to generate the single-phase and three-phase PWM pulses implementing single-edge modulation. The same counters will be utilised to generate the double-edge modulated PWM pulses for a single-phase as well as for a three-phase system with modified pin connections.

The counters CTC, CTD and CTE are utilised in conjunction with the frequency synchronization, phase synchronization and voltage monitoring circuitry and are also controlled by the microprocessor controller.

A single-step circuit is also incorporated during the development stage, and is shown in Fig.4.1. The single-step circuit allows operation of the microprocessor to be manually controlled via a switch. This is done by controlling the pin RDY1 which remains normally at high level. By operating the switch S1, the circuit provides only one pulse to the CPU so that the processor can proceed to perform one further operation only. This circuit provides the ease of testing software routines as well as hardware components during the initial stages of the development.

4.1.2 Feedback Circuitry

The feedback circuitry is utilised to convert the output voltages into digital signals and to feed these into the microprocessor controller board to implement the closed loop control system. The step-down output voltages are fed into a three-phase bridge rectifier. A potentiometer VR is utilised for adjusting the output voltage at the required level. An error amplifier is utilised, the output of which is set at 5 V when zero error exists, as shown in

Fig.4.4. Its output signal increases from 5V as the error in the output voltage increases and vice versa.

A LF398 sample and hold circuit is utilised to provide constant voltage during the A/D conversion process. The DC and AC zeroing is accomplished by adjusting potentiometer P2 and P1 respectively.

A ZN448 A/D converter is wired up to achieve unipolar operation [Ferranti Semiconductors]. The on-chip clock is utilised together with a capacitor C1=1nF and series potentiometer P5=2kΩ. The clock frequency (100 kHz) is adjusted by varying P5.

To perform calibrations at the minimum and maximum input signals (0 and 10V), the A/D converter is wired up in auto conversion mode. To adjust the A/D converter's output for maximum signal input, the full scale minus $1\frac{1}{2}$ LSB is applied at the input A_{IN}, and then P3 is adjusted so that the least significant bit output just flickers between 0 and 1 with all other bits at 1. For adjusting the output for zero input signal, an input signal of 19.5mV (1/2 LSB) is applied at the input A_{IN} and P4 is adjusted so that the least significant bit flickers between 0 and 1 with all other bits at 0.

The sample and hold circuit receives sampling command signals from the output of CTA0 through the monostable M1, which provides a sampling period of 1ms. At the completion of the sampling period the sample and hold circuit holds the sampled signal until the next sampling pulse arrives and it also starts the A/D conversion process by supplying a pulse at pin CON through the monostable M2 as can be seen in Fig.4.3. When the A/D converter completes the conversion, it raises the pin $\overline{\text{BUSY}}$ high which is used to latch the data at the output of the 74LS373 8-bit latch. The output of the latch holds the data until the next sample arrives and is interfaced to the microprocessor controller board. It can be seen clearly from Fig.4.3 that the sampling and conversion process is being completed within the period of 1.11ms and is synchronised with the interrupt INTR73 signal.

4.1.3 Switching Lag-Times and MOSFET-Gate Drive Circuitry

It is common practice to provide sufficient length of lag-time between the switching off of the upper device and the switching on of the lower device in the same leg of an inverter bridge circuit and vice versa. By doing so the devices will not be able to conduct

simultaneously, thus avoiding a direct short circuit across the DC line. Although this avoids direct DC line short circuit, this process introduces low order harmonics in the output waveform as described herewith. During the lag-time, when both switching devices are off, the output potential will be determined by the load current instead of the switching devices. In this period one of the phase diodes will be conducting which effectively connects the load to the positive or negative DC line. The potential developed during lag-time is a part of the output waveform and is responsible for introducing the unwanted low order harmonics.

Extensive studies have been carried out [Evans and Close - 1987, Murai et al - 1987] to establish the degree of the distortion and its dependence on the relationship between the carrier frequency and lag-times. A correction circuit is also described [Murai et al - 1987] and it is recommended that the product of the lag-time and the carrier frequency should be kept as small as possible to obtain an output waveform with minimized additional distortion. It is clear from the results contained in the above two references that harmonic distortion is dependent on the magnitude of the lag-time employed, whereas the required lag-time depends on the type and the size of the power switching devices utilized. When power MOSFETs are to be employed, lag-times in the range of a few hundred nano-seconds can be used. In this application the lag-time is equal to 300ns and this is arranged by the monostable M_1 and M_2 as shown in Fig.4.5.

In this power MOSFET inverter application, the gate drive circuit must provide isolation between the power circuit and the control circuitry and must be capable of handling large duty ratios. Optocouplers or transformers are the best known devices to achieve DC isolation. The former requires extra floating power supplies, whereas the main difficulty normally associated with the latter is that the transformer core flux must be reset every half cycle to avoid saturation. This is rather difficult to achieve with a PWM signal since the volt-second products are different in each half cycle due to the nature of the PWM pulses.

The gate drive requirements of power MOSFETs are much more simpler than other gate controlled devices as explained in Chapter Two. The total drive power needed is small since only the short pulses required to charge/discharge the gate-source capacitance need be transmitted by the coupling transformer. The PWM waveform can be transmitted as a series of short on/off pulses corresponding to the rising and falling edges of the PWM pulses. Such a technique has been described in the literature [Gyma et al - 1980]. In this scheme two separate pulse transformers are used to transmit on and off pulses to the

MOSFET where on pulse charges the gate capacitance through a diode which becomes reverse biased when the pulse is removed, thereby allowing MOSFET to remain on due to the charged gate capacitance. The second pulse (off pulse) turns on a bipolar transistor connected in parallel to the gate-source capacitance to discharge the capacitance. The MOSFET remains in its off state until an on pulse is reapplied. Although this method achieves a large duty cycle range, it does not allow for a negative gate voltage to increase noise immunity when the device is supposed to be off, nor does it provide adequate protection against spurious turn on resulting from the induced gate current via C_{GD} due to fast changes in drain source voltages. The MOSFET may be turned on by the parasitic charge developed at the gate-source capacitor when the gate drive circuit is of high impedance, as it is after the off pulse has been stored.

Another method for storing the on and off states on the gate capacitance of a power MOSFET utilises two small MOSFETs and making use of their integral diodes for storing positive on and negative off signals. A single pulse transformer and a push-pull driver were proposed by [Wood - 1985]. This arrangement limits the duty cycle range at high frequencies. It also makes the gate drive circuit complex and requires an extra negative power supply to generate a negative pulse for switching off the device.

The circuit proposed for use in the present application uses the same concept of storing the on and off states on the MOSFET gate capacitance for driving the upper devices of the inverter. For switching on and off, short pulses of 300ns durations are generated by the gating circuitry as shown in Fig.4.5. These pulses are passed through National Semiconductor DS0026 high speed low impedence drivers. The outputs of two drivers are fed to the primary of a pulse transformer through a capacitor to avoid a DC component being impressed across the winding. The positive on pulse charges up the capacitor C2 and the gate source capacitor C_{GS}. At the end of the short 300ns pulse, transformer T1's primary winding is clamped to zero volts and capacitor C2 will remain charged at 12.6V, this potential being determined by the drop across D1 and the voltage rating of the zener diode ZD1. Thus, ZD1 provides protection against the discharge of C2 at the negative or falling edge of the short turn on pulse. Consequently, C_{GS} will remain charged at approximately 0.6 volts (V_{BE} of Q_1) above C2's potential i.e. 13.2V, thus fully enhancing the MOSFET. The MOSFET remains in conduction until the negative off pulse arrives and discharges C2 via ZD1 and D1 to -0.6V. Q_1 becomes forward biased in the process and dicharges C_{GS} , thus turning off the MOSFET. As the negative off pulse diappears the

capacitor C2 stays fully discharged to approximately zero volts. When the MOSFET is in the off state, a charge may be transmitted to the gate capacitance through the parasitic drain-gate capacitance due to a high $(dV_{DS})/dt$ across the drain-source of the device. As soon as the voltage level at the gate exceeds 0.6 volts, the transistor's emitter-base junction becomes forward biased. Transistor Q_1 then provides a short circuit across the gate capacitance and discharges it effectively. In this way the combination of a diode D3, transistor Q_1 and the capacitor C2 provides permanent safeguard against spurious turn on when the MOSFET is supposed to be in the off state.

For the lower switching devices, the PWM signal is fed through the optocouplers and then connected to the gates through the high speed drivers, DS0026. For the three lower MOSFETs, a single floating power supply is used. This arrangement uses only one buffer per MOSFET and less components.

The combination of the two schemes, makes the drive circuit simple and low cost. A waveform diagram showing the working principle of the gate drive circuitry is shown in Fig.4.6. Turn-on and turn-off switching waveforms of a power MOSFET driven by the transformer-coupled gate drive circuit are shown in Figs.4.7a and 4.7b respectively. These figures show that the turn-on time is approximately 100 ns and turn-off time is less than 100 ns.

4.1.4 Power Circuit And Filter

The circuit diagrams of the single-phase half-bridge and three-phase inverters are shown in Fig.4.8 and 4.9 respectively. International Rectifier IRF 250 power MOSFETs were used as the switching devices in both circuits. Schottky diodes type 10TQ030 are employed in series with each power MOSFET to prevent the body diode from conducting. Reverse current flow is handled by a fast recovery anti-parallel diode type BYV29-400, with a 50ns reverse recovery time.

Simple low pass filters are utilised consisting of ferrite cored inductors and Wima metalized polyester MKS capacitors. For the single-phase half-bridge inverter, a capacitor is used in series between the inverter and the transformer so that DC voltage should not appear across the transformer. For three-phase, the capacitors of the output filter are connected in delta as this configuration results in the use of capacitors of lower individual ratings than for the

star configuration. The output of the filter is connected to a small three-phase transformer to close the loop.

4.2 SOFTWARE OPERATION AND PWM GENERATION PROCESS

After switching on the control power supplies, the first task of the software is to send the respective control words to the peripherals in order to select the appropriate modes of their operation. These modes are described in this and subsequent chapters for the individual devices where these are used. The microprocessor then establishes the interrupt vectors in the RAM. In order to make provisions for storing data temporarily in the memory, 4-byte locations and 25 word locations are reserved in the data segment to implement the digital filter in the PI alogrithms and to calculate the rate-of-change of frequency from period measurements respectively.

As described previouly, the integer numbers corresponding to T_{HAj} are calculated for a quarter of a cycle and transferred into EPROM as look-up-tables. All of these look-up-tables are subsequently transferred into the RAM after calculations for the required length to generate the output waveforms. Then the microprocessor transfers the offset address of the table RAMADDR in the register Base Pointer (BP) where this table contains the addresses of the look-up-tables. The Base register BX and the Source Index (SI) registers are initialized with zero and are used to retrieve integer numbers from the selected look-up-tables. These will eventually be loaded to the programmable counters to generate the PWM pulses.

Since the microprocessor also controls a PLL circuit, it loads the integer number corresponding to the 50 Hz output to counter CTC1. It then waits for the start signal from the start/stop circuit. Once the start button is pressed, it enables the counter CTA1 which generates the 18 kHz carrier signal. The microprocessor starts receiving interrupt signals from the counters CTA1 and CTA0 to generate the PWM pulses and to implement the PI control algorithms respectively. The PWM generation process can be stopped by pressing the stop button of the start/stop circuit.

When the microprocessor returns from the interrupt mode, it checks and makes certain that the frequency and phase of the inverter are synchronised with the mains power supply. The flow chart of the main program controller is shown in Fig.4.10.

4.2.1 Effects Of The Interrupt Delays On PWM Waveform Generation

Two types of PWM generators can be employed to generate PWM pulses using digital techniques. These generators can employ discrete digital components or microprocessors. The delays inherent in discrete digital hardware or interrupt delays in the microprocessor causes shifts to occur in the switching angles of the PWM waveform and introduces distortion. A digital modulator using discrete components to minimize such effects in PWM generator using discrete digital components has been proposed [Manias et al - 1987]. To find a solution to the problem of interrupt delays in microprocessor controlled PWM generators, it is first necessary to discover the nature of the interrrupt delays and to ascertain their effects on the output waveforms.

The microprocessor is inherently a serial device, and it therefore operates in a sequential manner. To perform some functions at particular time instants, the microprocessor needs to be interrupted at that time instant. The actual response of the microprocessor to interrupt servicing would depend upon three factors.

(i) The microprocessor will only respond when it reaches the end of an instruction execution cycle, and is about to fetch the next instruction opcode. This time will vary depending upon the instruction being executed at every interruption time.

(ii) The microprocessor saves the present status and address of the next opcode to be executed after servicing the interrupt routine, and then it picks the address of the interrupt routine from the interrupt vectors.

(iii) In an interrupt service routine, it saves all registers to be used in the interrupt routine and then starts performing the actual job for which it has been interrupted.

(iv) Execution of the actual opcode written to perform the required function will take a certain amount of time which entirely depends upon the type and number of the codes utilised.

Since interrupt driven software is to be employed for generating the PWM pulses, the response time of the microprocessor to the actual interrupt servicing routine may be varied at every interruption time. The varied response time [Khan and Manning - UPEC88] and the time taken to service the interrupt routine causes inaccuracies to occur in the switching

edges and inevitably introduces a certain degree of distortion in the PWM waveform [Bowes and Mount - 1981]. An additional counter has been proposed to reduce the distortions [Bowes and Davies - 1985]. This may improve the switching angle accuracies to some extent but does not completely eliminate the effects of interrupt delays on the PWM waveform.

It should be noted that there will be a time delay before the interrupt delays will be invariably introduced in multiple interrupt systems, when two or more interrupts occur simultaneously, as is usually the case in three phase PWM generators. These interrupt time delays would become accumulated over a cycle of the output voltage waveform, with the result that the output frequency becomes less than the required value [Akhrib - 1986]. Also the response time of the microprocessor varies with different interrupts [Khan and Manning - UPEC 88] and the total time delay depends upon the number of pulses used in a cycle. Consequently, the output frequency will start fluctuating and it also becomes impractical to retain the 120^{o} phase displacements between phases [Khan and Manning - PESC89]. These situations are highly undesireable for UPS systems.

In an attempt to solve the problem of generating three-phase PWM pulses with the correct 120^{o} phase displacements between phases, three interrupts together with an additional counter and a software routine have been reported [Akhrib - 1986]. This system does not eliminate completely the distortion effects in the output waveform even at low frequencies, and is totally unsuitable for use at high carrier frequencies. For complete elimination of the distortion effects of interrupts delays from the output waveforms, a scheme utilizing a single interrupt and a square carrier waveform is employed. This scheme is equally valid for single-phase as well as three-phase PWM generators. The detail of the functional scheme can be seen in the following sections on the PWM generation process.

4.2.2 Single-Phase PWM Using Single-Edge Modulation

Since integer numbers ITN_j corresponding to the T_{HAj} are stored in the EPROM for a quarter of a cycle for different modulation indices, the microprocessor completes calculations for a half cycle and transfers the data into the RAM as the look-up-tables data. A counter CTB0 is used to generate the PWM pulses for a single-phase system. This counter is programmed in hardware retriggerable one-shot mode [Intel Corporation, Vol.II]. In this mode, the output of the counter will go low on the rising edge of the gate input and will become high at the end of a count. The hardware connections of the counter

CTB0 can be seen in Fig.4.1 where its gate is connected to the inverted output of the counter CTA1 which generates the 18 kHz carrier signal and its clock pin is connected to the PLL circuit.

Since interrupt driven software is utilised and integer numbers ITN_j corresponding to the high level pulse widths T_{HAj} for positive half cycles are arranged in the RAM as look-up-tables, the integer numbers ITN_j corresponding to the T_{HAj} for the negative half cycles are calculated on-line by the microprocessor. The PWM generation process can be explained with reference of Fig.4.11. The rising edge of the carrier signal (output of counter CTA1) interrupts the microprocessor and its inverted output is used to trigger the counter CTB0 which then starts the counting down process utilising the integer number loaded in the first half of the carrier period. In the meantime (at the next interrupt) the microprocessor will fetch/ and calculate the next appropriate integer number and transfer it to the counter CTB0 without disturbing the count in progress. This would be loading at the next trigger pulse as can be seen from Fig.4.11. The above process would be repeated with the period of the carrier frequency. Due to the constant period of the carrier frequency, the low level pulse width T_{LAj} obtained by the above procedure, satisfies Eqn.(3.17). This eliminates the need of calculating T_{LAj} by the microprocessor. Thereby this PWM generation process simplifies the design for a single-phase PWM generator.

The harmonic spectrum at the output of the counter is shown in Fig.4.12. The amplitudes of the second and third harmonics are -47.5 dB and -46.0 dB, and all other individual harmonic components are lower than -50.0 dB with respect to the fundamental 50 Hz component.

The flowchart of the interrupt INTR72 routine utilised to generate single-edge modulated PWM pulses is given in Fig.4.13.

4.2.3 Single-Phase PWM Using Double-Edge Modulation

In contrast to the single-edge modulation, to implement double-edge modulation both edges need to be modulated equally. Therefore, information concerning both edges is required beforehand. To implement double-edge modulation, Eqn.(3.15), i.e.

$$X_{LBj} = \frac{T_c - T_{HAj}}{2}$$

is utilised. Since integer numbers corresponding to the high level pulses T_{HAj} for a quarter of a cycle are stored in the EPROM, the integer numbers corresponding to the rest of the cycle are calculated and transferred into the RAM. With the aid of these integer numbers, Eqn.(3.15) is computed on-line in the integer domain by the microprocessor.

Two counters CTB0 and CTB1 are wired up as shown in Fig.4.14. These two counters are used in conjunction with the microprocessor for generating the low and high level pulses (X_{LBj}, T_{HAj}, X_{LAj}) as shown in Fig.4.15. Since counter CTA1 generates the 18 kHz square wave carrier signal, its positive going edge is used to interrupt the microprocessor whilst its inverted output triggers counter CTB0. Upon interruption, the microprocessor fetches the integer number corresponding to T_{HAj} from the selected look-up-table and outputs this to counter CTB1. The microprocessor then performs the calculations stipulated by Eqn.(3.15) in the integer domain to obtain an integer number corresponding to X_{LBj} and outputs this to counter CTB0. This counter is therefore used for providing time intervals equal to X_{LBj}. On receiving a trigger pulse, counter CTB0 starts counting down and its output remains low until the count is finished as shown in Fig.4.15. Then the output of CTB0 triggers counter CTB1 for generating the high level pulse T_{HAj}. X_{LAj} is achieved just by waiting for the next trigger pulse to start $X_{LB(j+1)}$ after the completion of T_{HAj}.

It is clear from Fig.4.15 that the microprocessor is being interrupted at every positive going edge of the carrier square wave signal and the counter CTB0 is triggered by the positive edge of the inverted carrier signal so as to provide the maximum available time (half carrier period) to the microprocessor. The output waveform will therefore be consistent in relation to the carrier signal without being effected by the time taken by interrupt routine servicing. Thus there will be no distortion added by the PWM generator.

The harmonic spectrum of the PWM signal is shown in Fig.4.16. The amplitudes of the third, fifth and seventh harmonic components are -46.5 dB, -50.0 dB and -50.0 dB with respect to the fundamental 50 Hz component.

The flow chart of the interrupt INTR72 routine utilised to calculate Eqn. (3.15) on-line for implementing double-edge modulation is shown in Fig.4.17.

4.2.4 Three-Phase PWM Using Single-Edge Modulation

To generate the PWM pulses for a three phase system, three counters are utilised and their connections are shown in Fig.4.1. As described previously, the high level pulses are calculated off-line and the corresponding integer numbers stored in the EPROM whereas the low level pulses are achieved by using the carrier signal as a reference waveform. To generate the three-phase PWM signal with exact 120^{o} phase displacements, the number of ITN_j's are increased from 360 to 600 values and transferred into the RAM. Since the ratio of the carrier frequency to the modulating frequency results in 360 equal segments i.e. 360^{o}. These equal-segments are then used as a reference to generate the three-phase PWM waveforms with exact 120^{o} phase displacements using the same look-up-table.

As can be seen from Fig.4.11, the rising edge of the carrier signal interrupts the mircoprocessor and its inverted output triggers the counters CTB0, CTB1 and CTB2 simultaneously. On interruption, the microprocessor fetches three integer numbers from the selected look-up-table by displacing the phase B and C pointers 120^{o} and 240^{o} respectively with respect to phase A. It then outputs the integer numbers to the appropriate counters CTB0, CTB1 and CTB2 to generate the three-phase output PWM pulses. These counters therefore provide the time intervals equal to the corresponding high level pulse widths for each phase whereas the low level pulse widths are achieved just by waiting for the next trigger pulse to start the next high level pulses. Thus, the PWM generation process eliminates the need of actually computing Eqn.(3.17) by the microprocessor. This scheme provides sufficient time to the microprocessor to output the integer numbers to the counters so that the PWM pulses can be generated independently of the time taken by the microprocessor. The output pulses are therefore consistent with the carrier signal which is used as a real time reference. It is clear from Fig.4.11 that a single carrier waveform is used in the PWM generation process for the three phases simultaneously. Consequently, there will be no accumulated time delays over a cycle. This scheme is therefore capable of generating the distortionless three-phase output waveforms with exact 120^{o} phase displacements.

The harmonic spectra at the controller output for phases A, B and C are shown in Fig. 4.18. The amplitudes of the second and third are -47.5 dB and -46.0 dB respectively in

relation to the fundamental whilst all other harmonic components are lower than -50.0 dB for the phase A. Other phases B and C have similar harmonic spectrum as can be seen in Fig. 4.18. The triplen harmonics would not appear in the output voltages for suitably connected loads.

The flow chart of the interrupt INTR72 routine utilised to generate three-phase PWM pulses using single-edge modulation process is shown in Fig.4.19. It can be seen from the flow chart that the microprocessor is not calculating Eqn. (3.17) itself by software. This is realised by the technique used in the PWM generation process.

4.2.5 Three-Phase PWM Using Double-Edge Modulation

To generate double-edged PWM pulses for a three phase system Eqn.(3.15) needs to be solved three times at every interruption time. To achieve this, the clocking frequency of the microprocessor needs to be increased beyond its specification if all other functions are to be performed by the microprocessor. It is therefore required to use hardware components to perform some calculations required by Eqn.(3.15). A circuit diagram is shown in Fig.4.20 which aids the microprocessor to generate the PWM pulses for phase A. This circuit is interfaced with the microprocessor controller board through PORTA which is a part of the PPI with the other two output ports, PORTB and PORTC, for phases B and C respectively.

Since counter CTA1 generates a square wave carrier signal whose positive edge interrupts the microprocessor, the negative edge triggers M1 to provide a trigger pulse to the binary counters B1 and B2. Upon interruption the microprocessor picks three integer numbers displaced by 120^{o} and 240^{o} with respect to phase A from the selected look-up-table and then outputs them to the counters and ports: CTB0 and PORTA, CTB1 and PORTB, and CTB2 and PORTC, to generate the PWM pulses for phases A, B and C respectively. On the following negative edge of the carrier signal, the binary counters B1 and B2 will start counting up from zero as shown in Fig. 4.15. Each output of the binary counters is compared by a digital comparator with the integer number obtained from the outputs of the function generators F1 and F2. The latter subtract the integer number ITNj from the integer number corresponding to the carrier period. Division by two is achieved by connecting the outgoing lines (function generator) to one lower in order to the Q-input of the 8-bit digital comparator. To start pulse X_{LBj} a trigger pulse output by monostable M1 is used to restart the counting of the counters B1 and B2 from zero. When the counts of the counters equal

the integer number at the Q-input of the comparator, a pulse is generated at pin $\overline{(P=Q)}$ which is used to trigger the counter CTB0 (for phase A) after passing through the half-count compensator circuit based on the monostables M2 and M3, as shown in Fig.4.20. This circuit delays the triggering pulses to the counter CTB0 equal to the half-count (half period of the clocking frequency) only when the integer number after subtraction is odd. The least significant bit F0 is used to select the delay line. The odd integer number's least significant bit (LSB) enables the buffer of the delay line whereas the even number's LSB selects the buffer without the delay line. The other half, X_{LAj} of the low level pulse is obtained automatically since the carrier signal having constant period is used as a real-time reference.

Similiar circuits are used to generate the PWM pulses for phases B and C. The scheme used for generating the PWM pulses is similiar to the scheme detailed in section 4.2.3 apart from the additional hardware components. This method provides the microprocessor with the maximum available computation time i.e. equal to the half-period of the carrier frequency.

The harmonic spectrums at the controller output for phases A, B and C are shown in Fig. 4.21. The amplitude of the largest harmonic component (the third) is -46.0 dB and all other individual odd harmonic components are lower than -50.0 dB with respect to the fundamental 50 Hz component. The triplen harmonics are cophasal with the suitable connected load. The flow chart of interrupt INTR72 routine is given in Fig. 4.22. This shows that the microprocessor is generating PWM pulses in conjunction with the hardware interfaced through the output ports PORTA, PORTB and PORTC. The 120 and 240 displacements with respect to the phase A are used to select the integer numbers from the selected look-up-table for generating three phases with exact 120^{o} phase displacements. Three-phase output voltage waveforms are shown in Fig. 4.23. These clearly show that each waveform is exactly 120^{o} apart from each other.

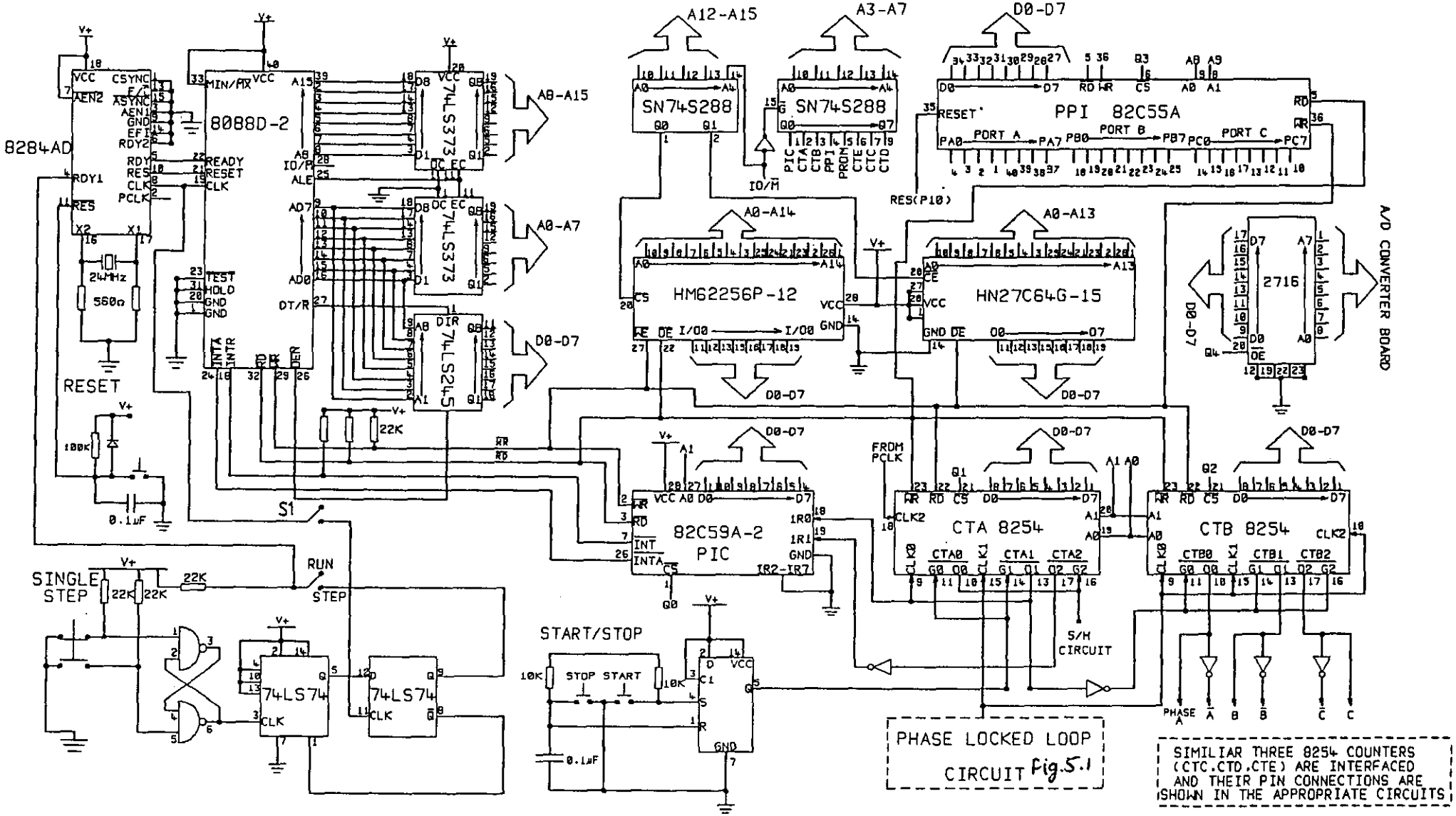


FIG 4.1 THE MICROPROCESSOR CONTROLLER BOARD

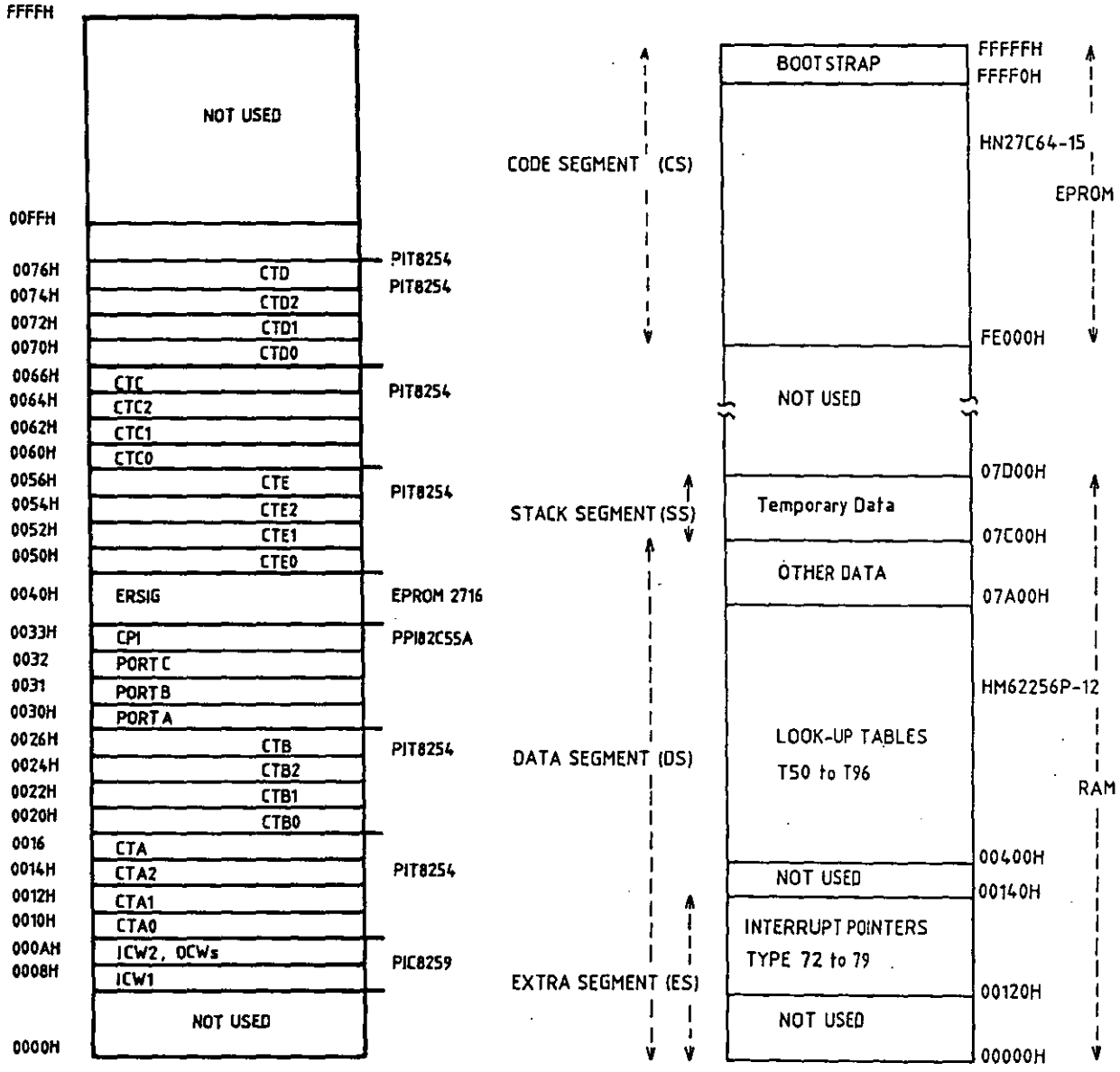


Fig. 4.2 INPUT/OUTPUT AND MEMORY MAPPING.

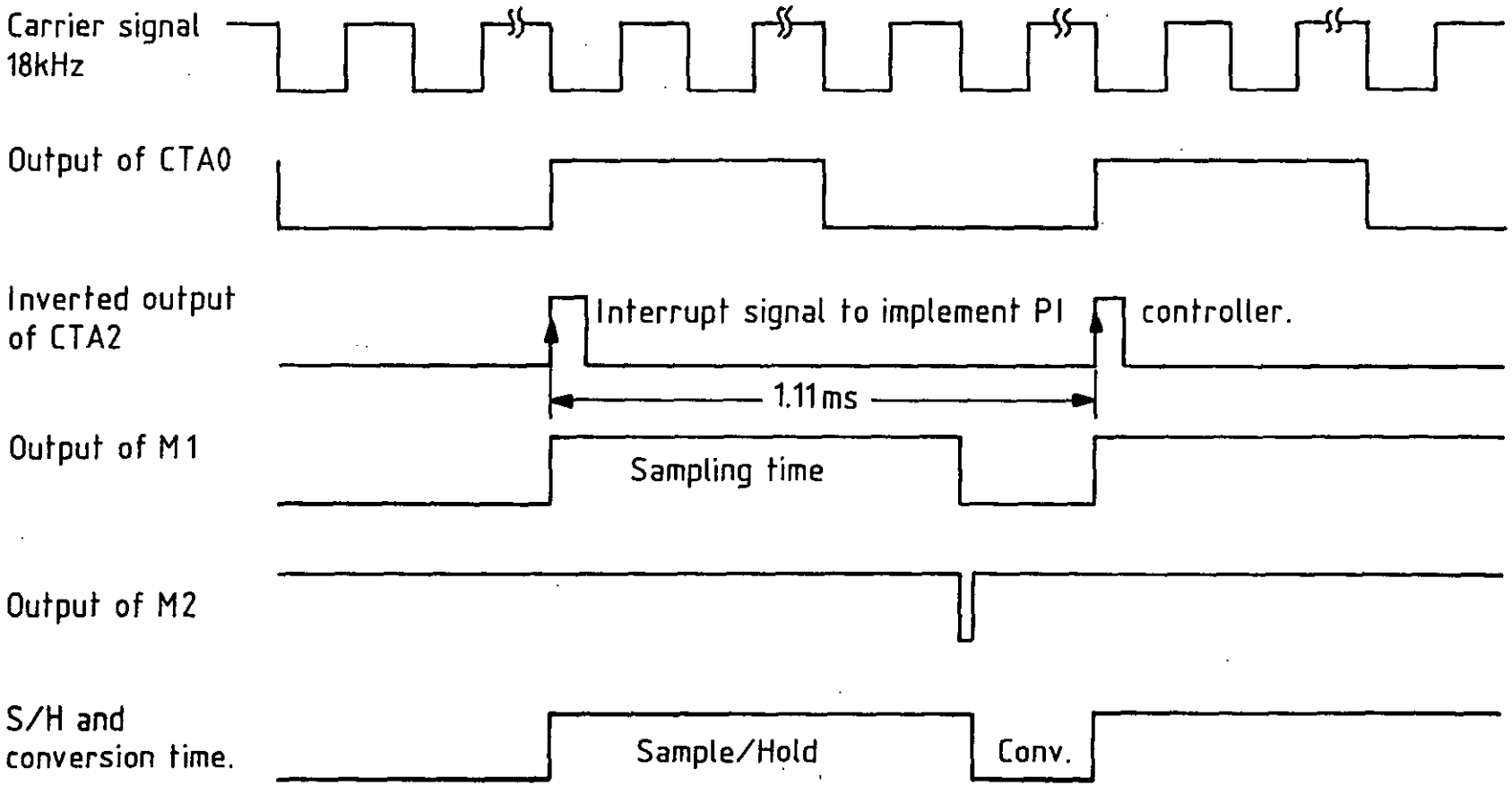


Fig. 4.3 SAMPLE/HOLD AND A/D CONVERSION PROCESS SYNCHRONIZED WITH THE INTERRUPT SIGNAL TO IMPLEMENT PI CONTROLLER.

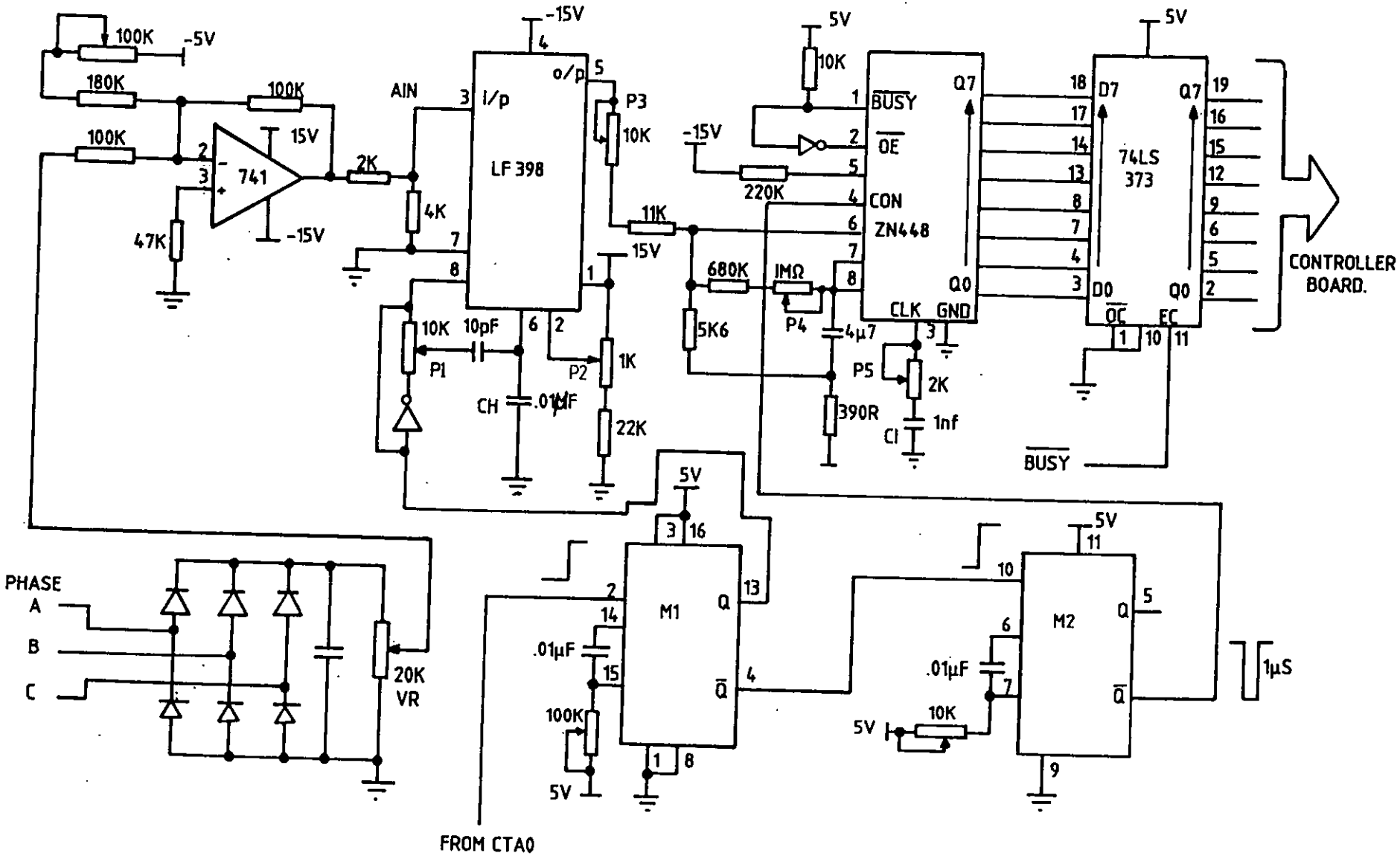


Fig. 4.4. FEEDBACK CIRCUIT.

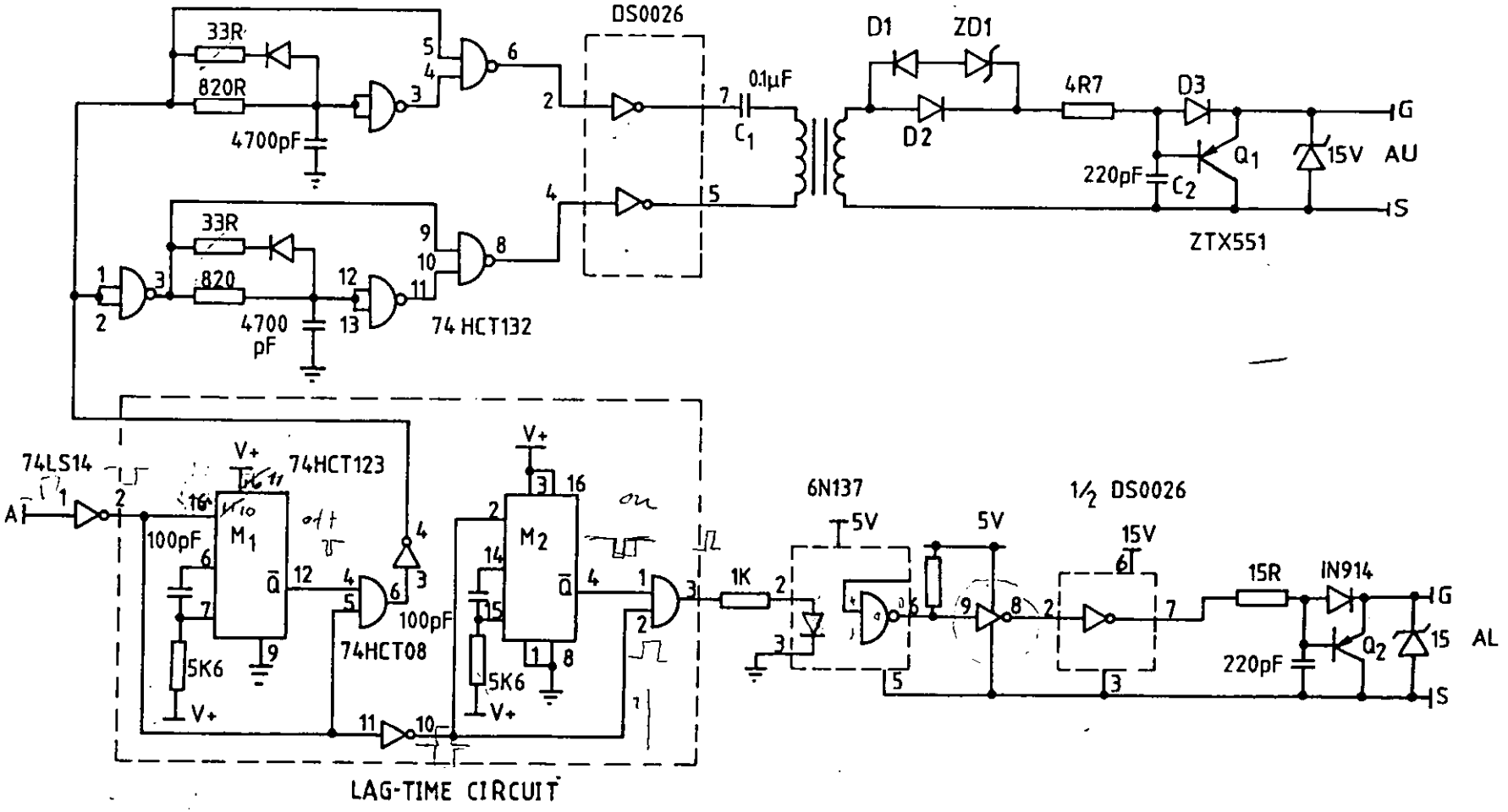


Fig 4.5 M O S F E T GATE DRIVE CIRCUIT FOR ONE PHASE.

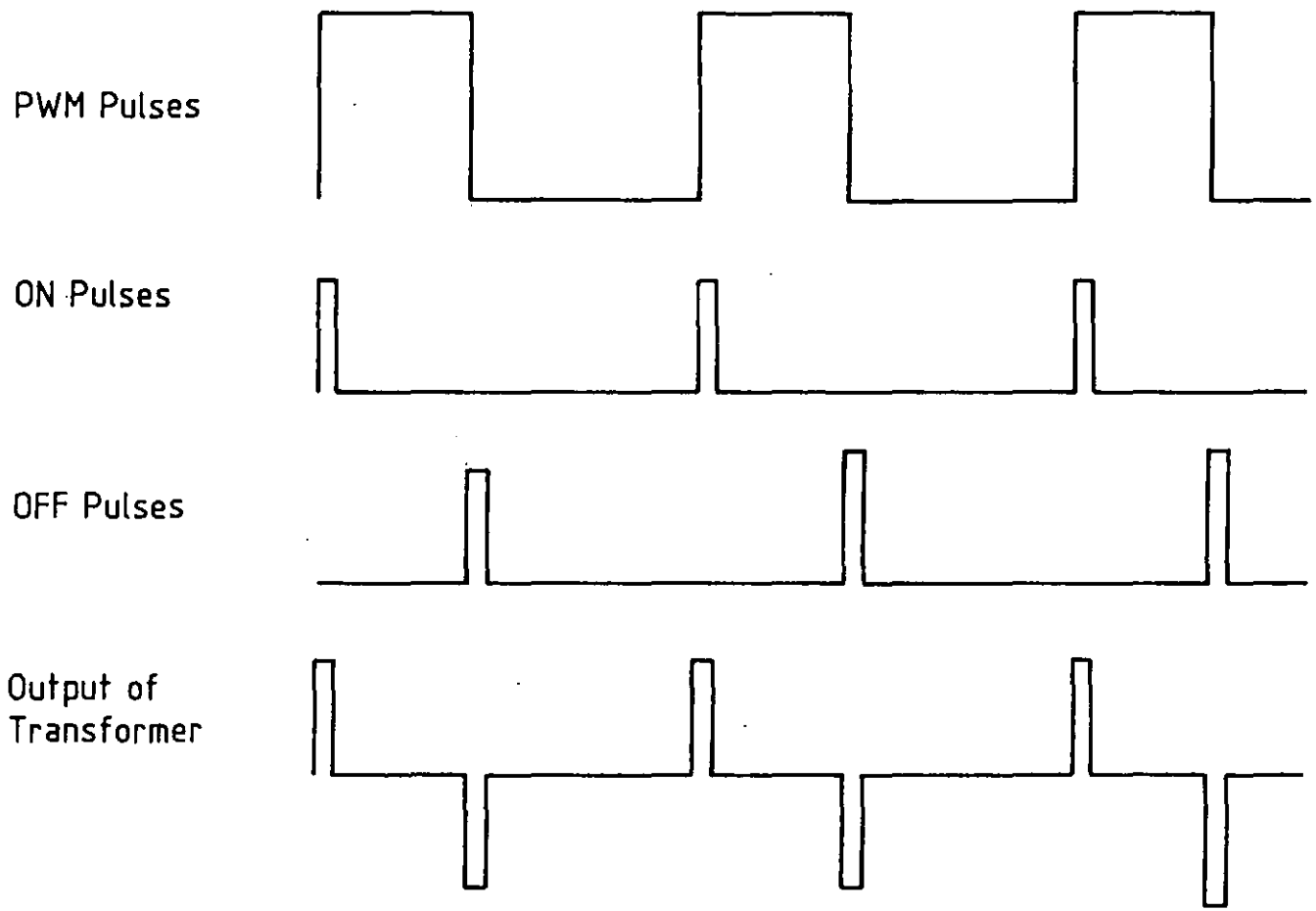


Fig. 4.6. Working principle of the gate drive circuitry.

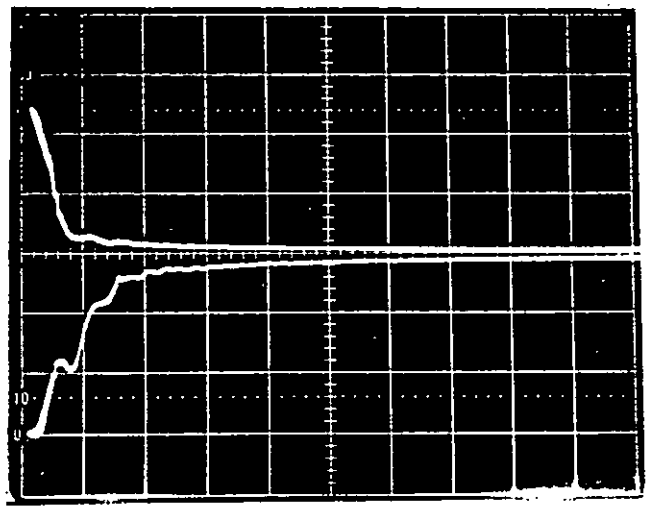


Fig. 4.7a. Turn ON of MOSFET
Upper Trace: V_{DS} 20V/DIV
Lower Trace: V_{GS} 5V/DIV
Time 200 ns/DIV

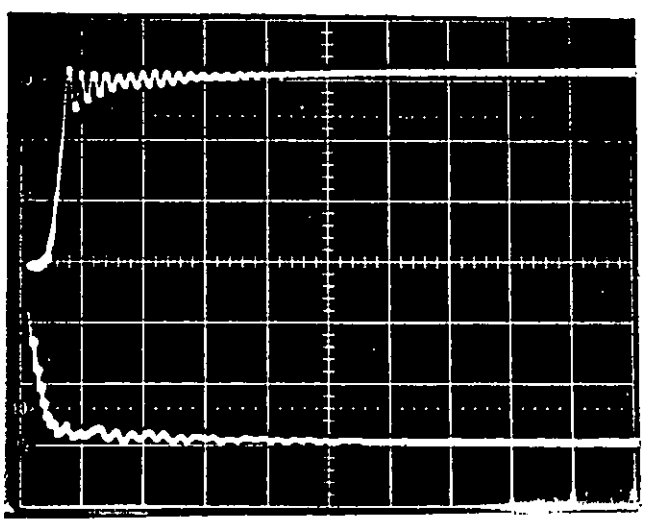


Fig. 4.7b. Turn OFF of MOSFET
Upper Trace: V_{DS} 20V/DIV
Lower Trace: V_{GS} 5V/DIV
Time 200 ns/DIV

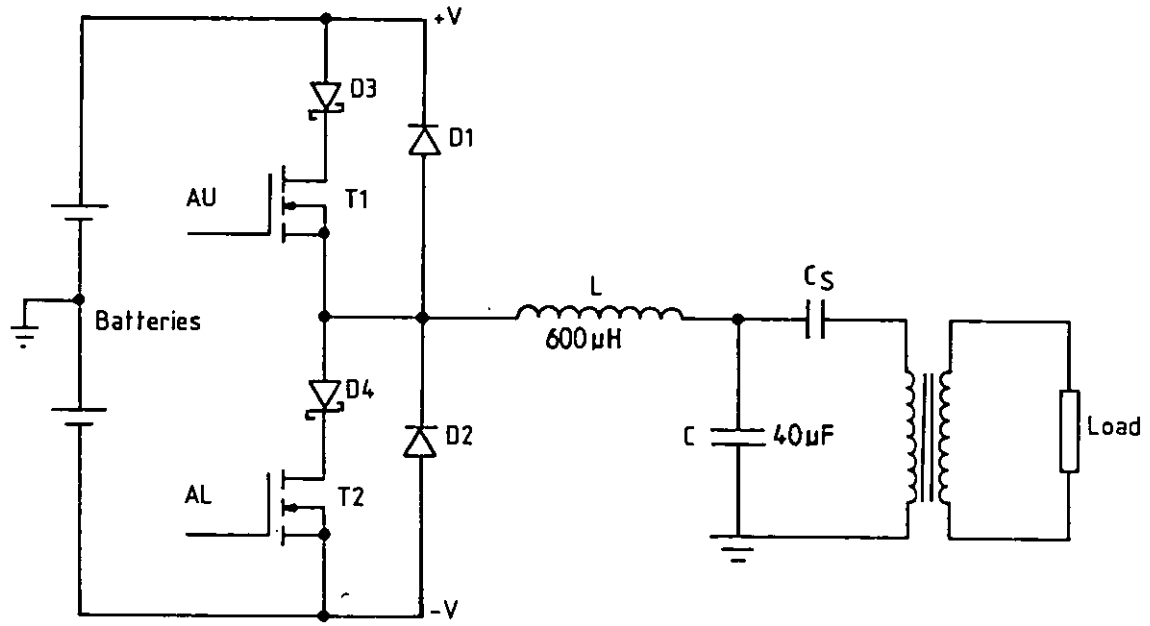


Fig. 4.8 Half - bridge MOSFET inverter.

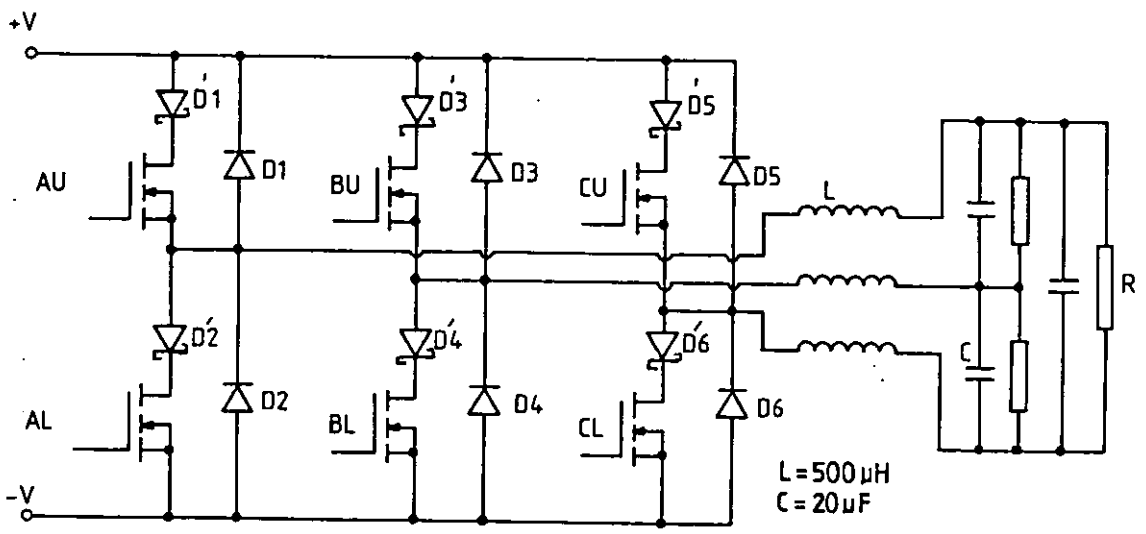


Fig. 4.9 Three - phase MOSFET inverter.

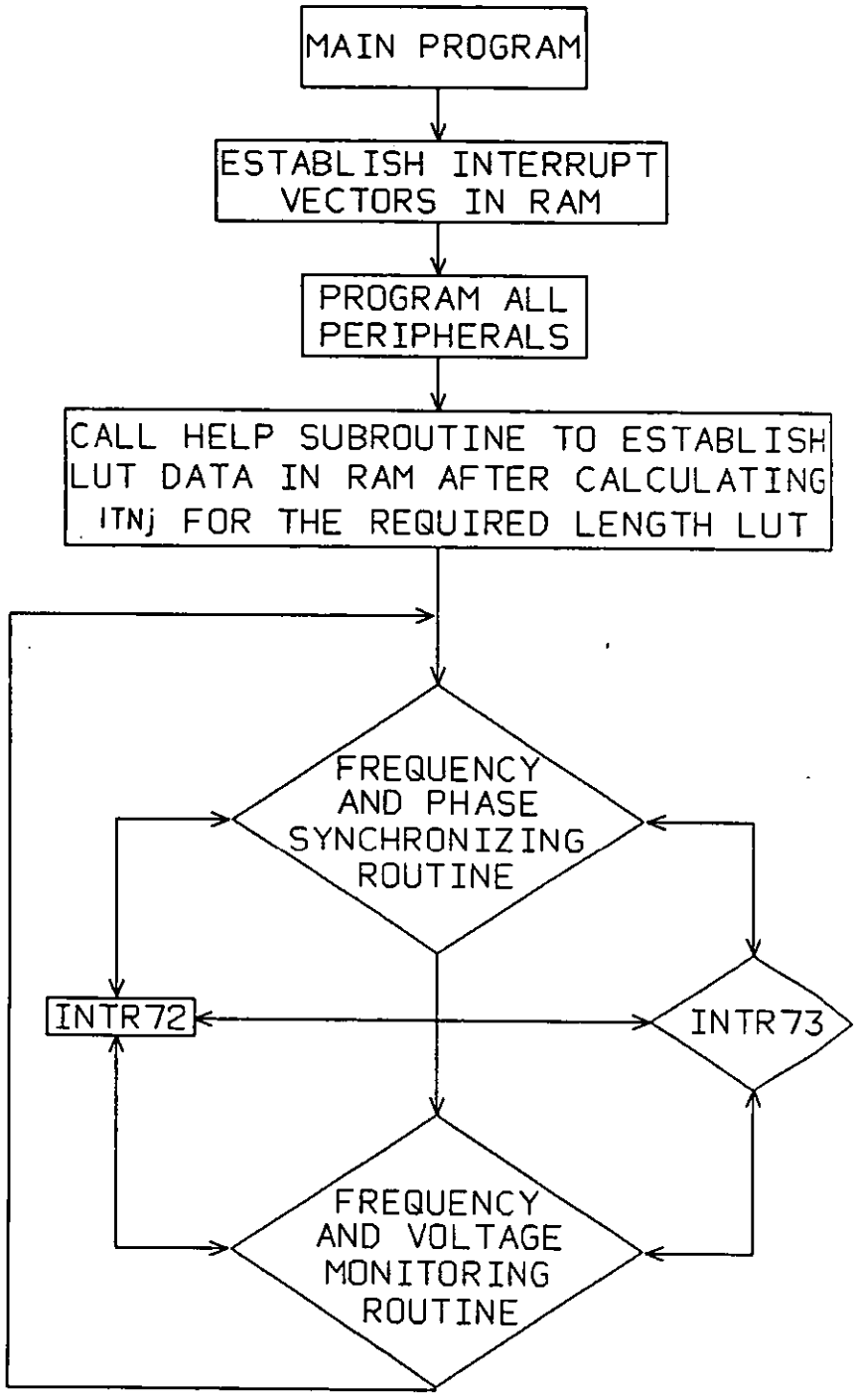


Fig. 4.10 Flowchart of the main program controller.

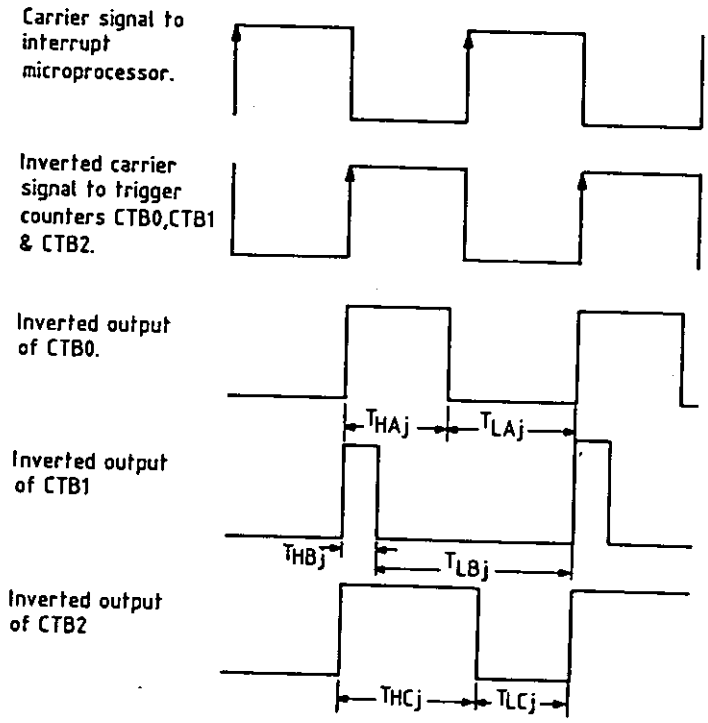


Fig. 4.11 SINGLE-EDGE PWM WAVEFORM GENERATION PROCESS.

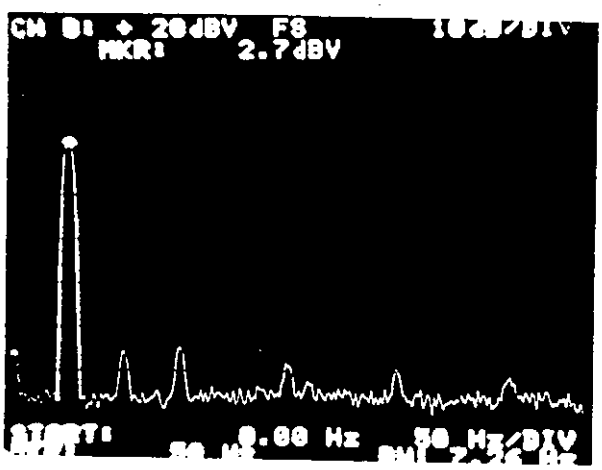


Fig.4.12 Harmonic spectra at the output of the single-edge PWM generator

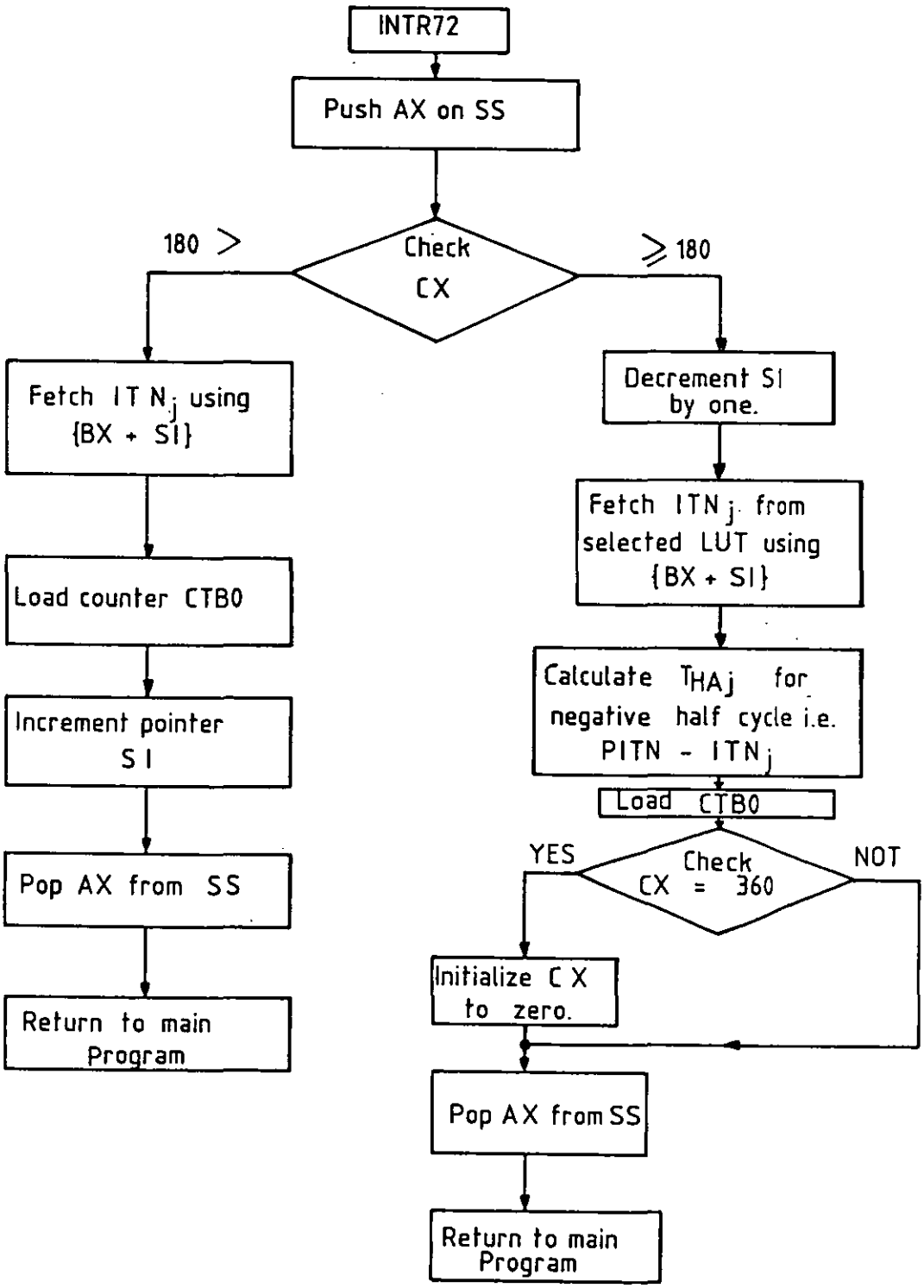


Fig. 4.13. Flow chart of Interrupt 72 in case of Single- phase PWM using single-edge modulation.

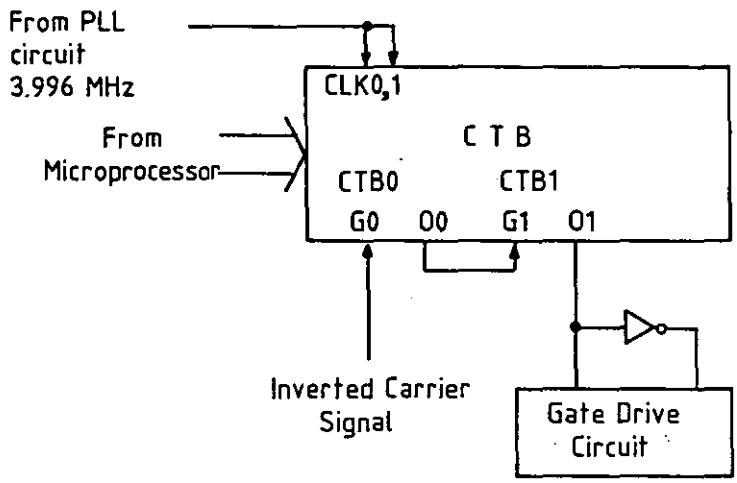


Fig. 4.14 PWM GENERATOR FOR DOUBLE-EDGE MODULATION.

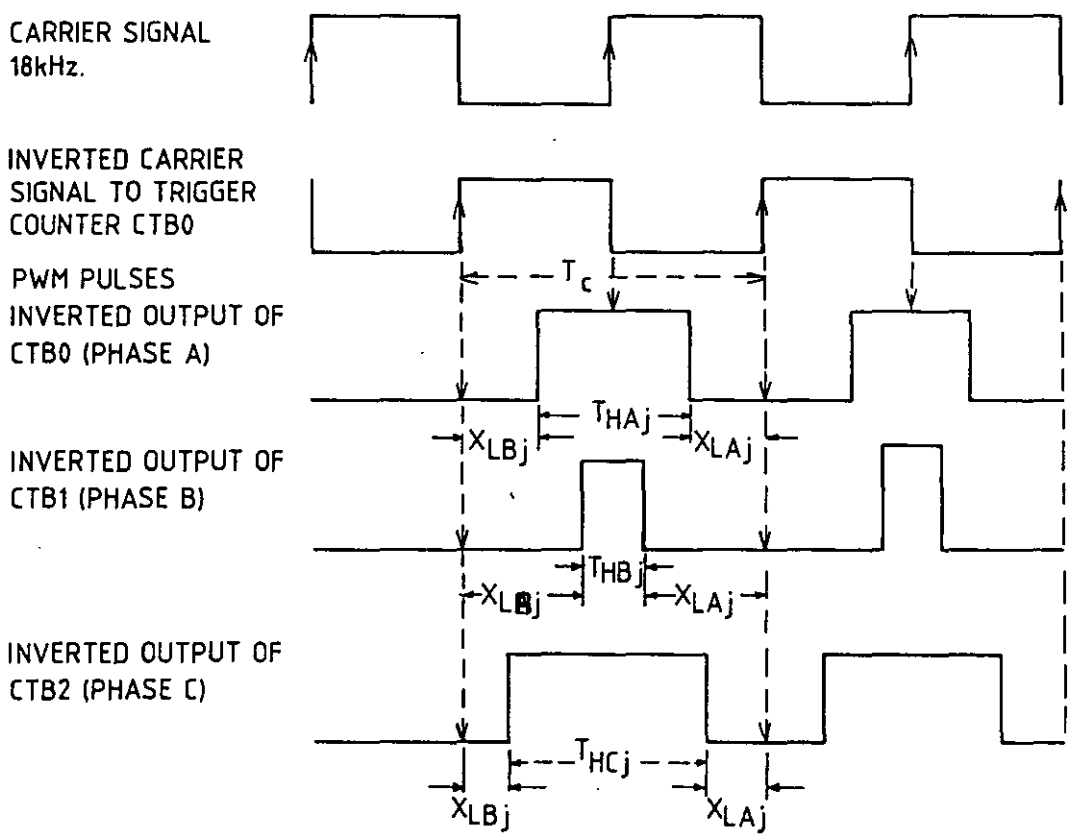


Fig. 4.15 WAVEFORM GENERATION PROCESS.

Fig.4.16. Harmonic spectra at the output of PWM generator

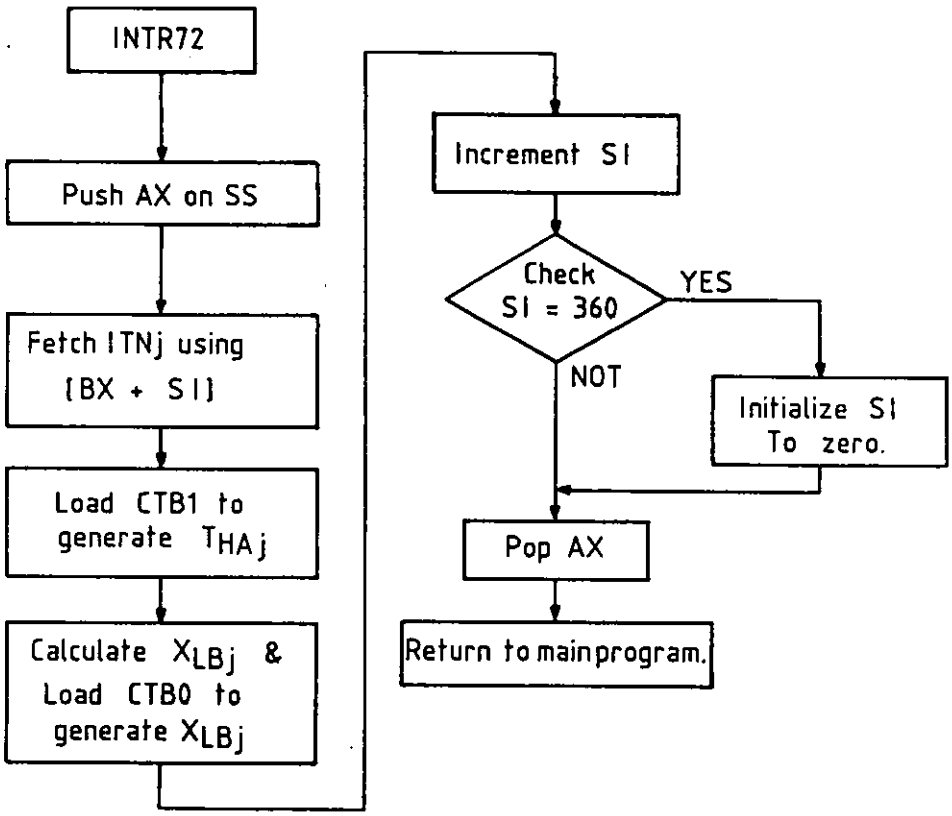
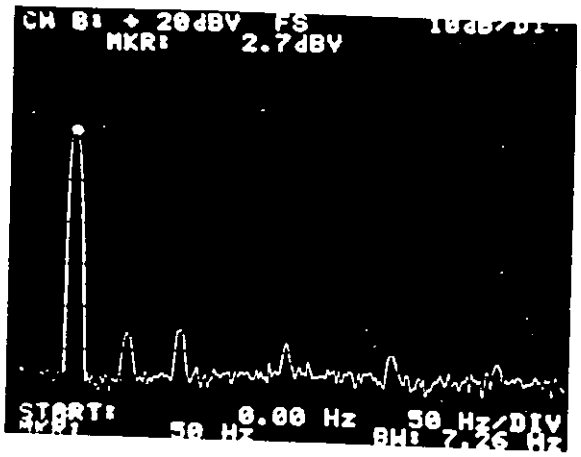
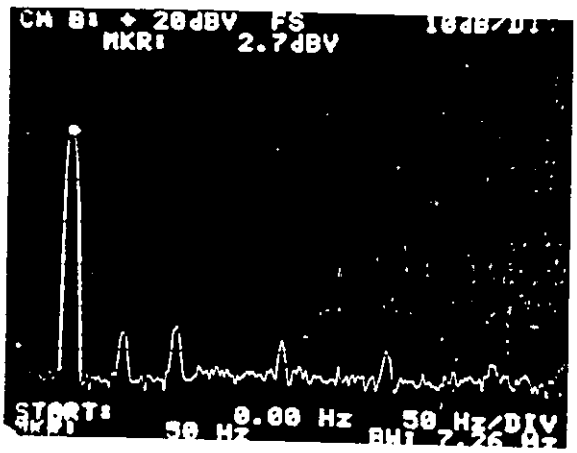


Fig. 4.17. FLOW CHART OF INTERRUPT 72 IN CASE OF SINGLE-PHASE PWM USING DOUBLE-EDGE MODULATION.

Phase A



Phase B



Phase C

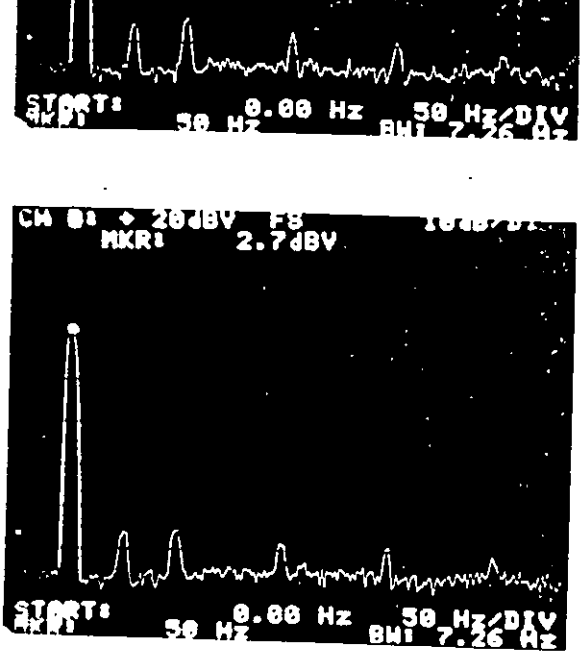


Fig. 4.18. Harmonic spectra at the output of the single-edge PWM generator

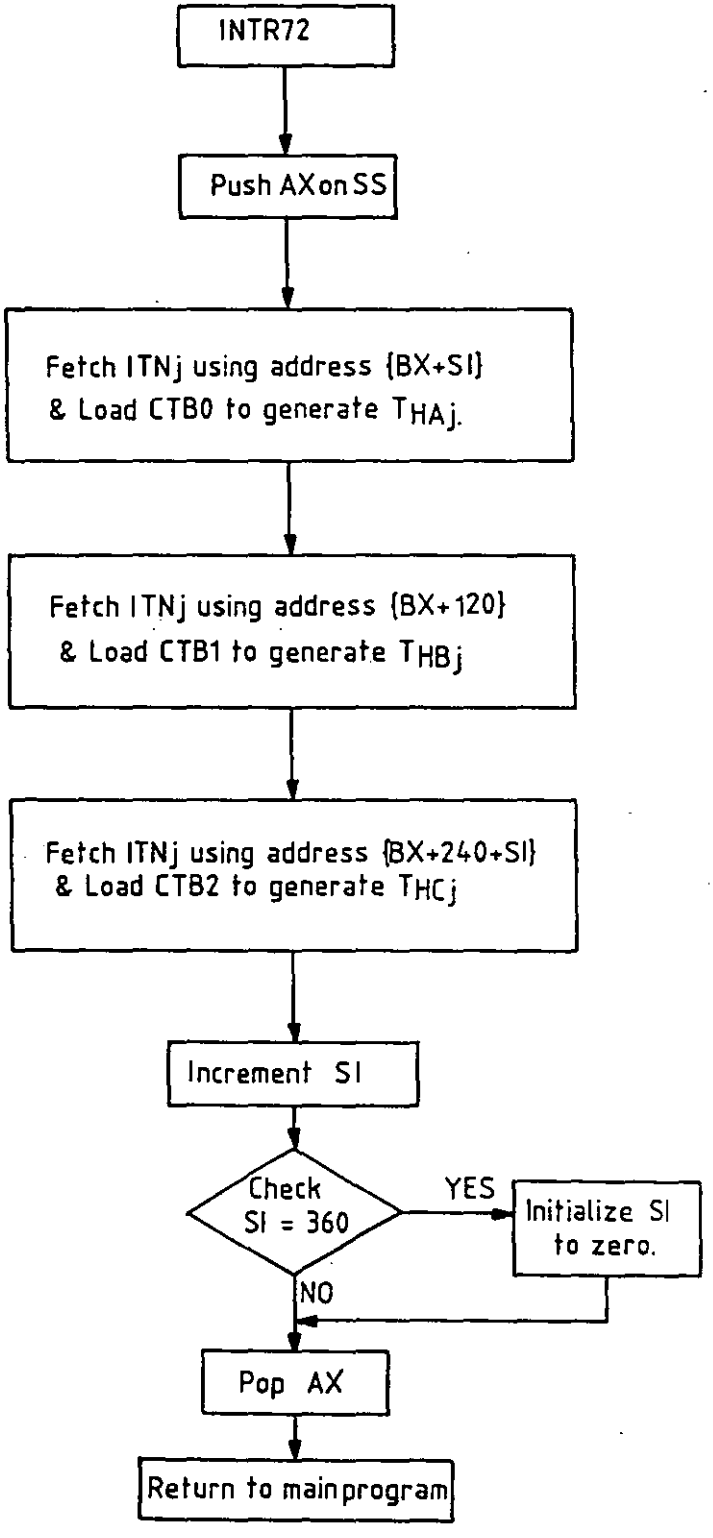


Fig. 4.19 FLOW CHART OF INTERRUPT 72 IN CASE OF THREE-PHASE PWM USING SINGLE-EDGE MODULATION.

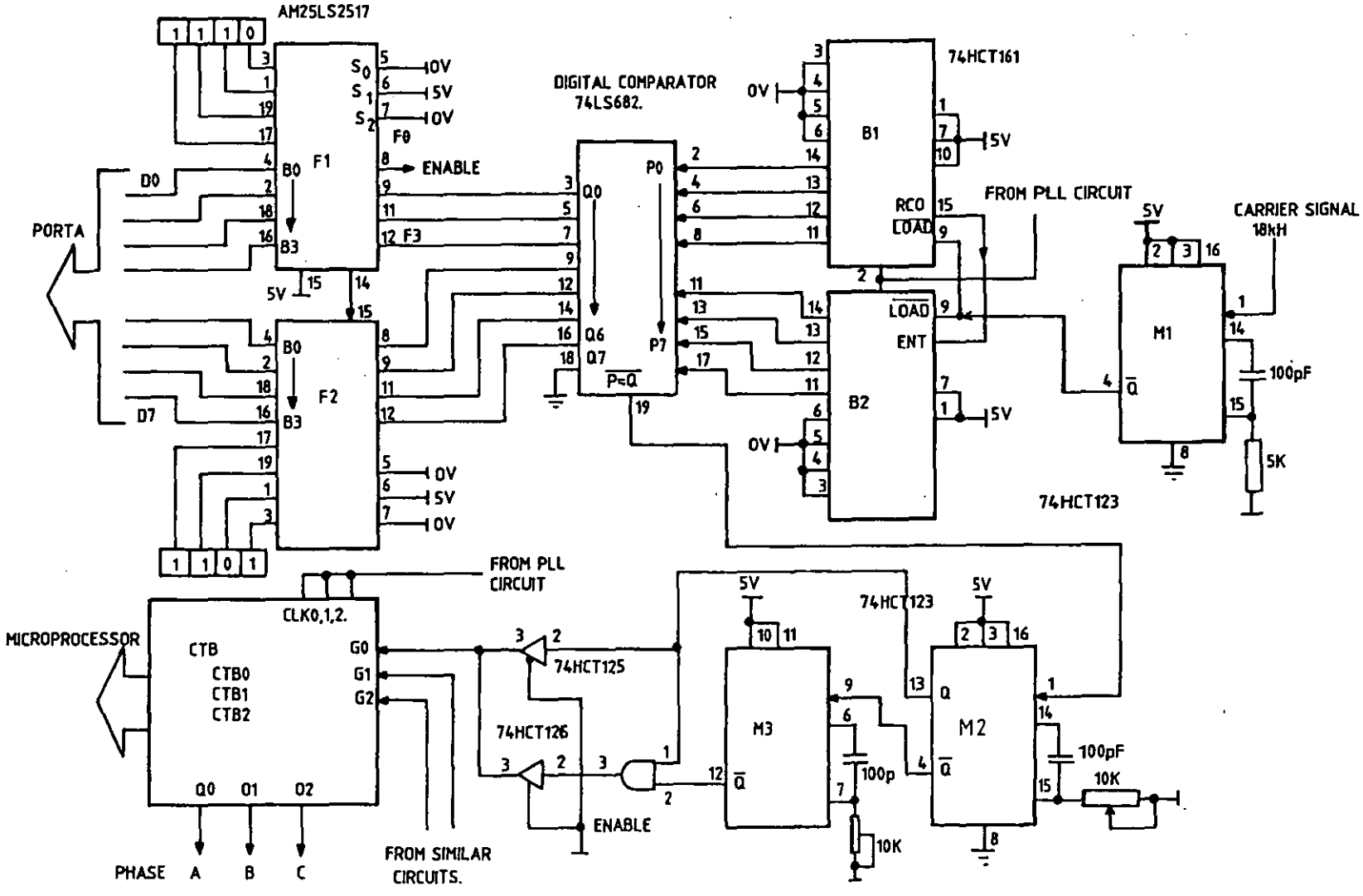
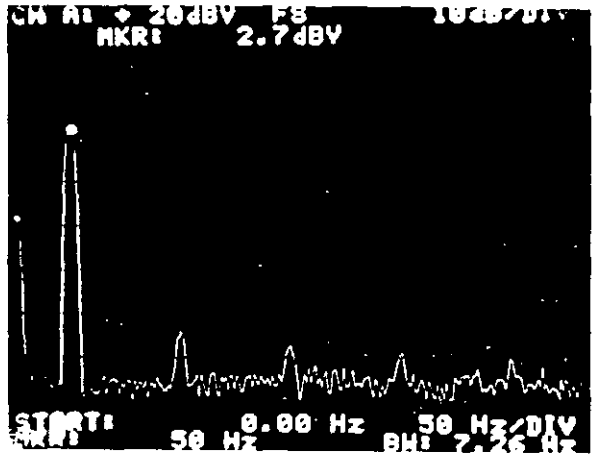
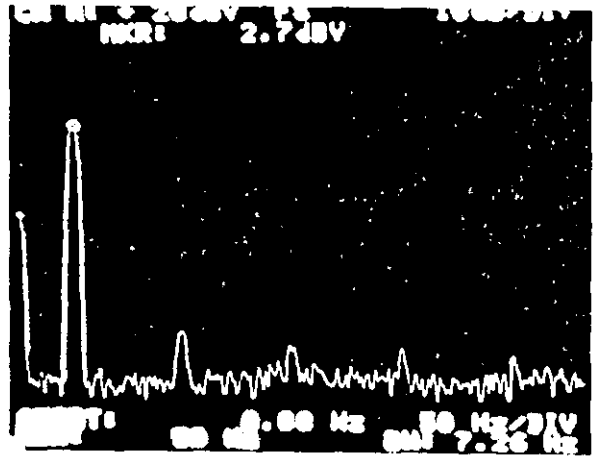


Fig. 4.20. PWM GENERATOR FOR PHASE A.

Phase A



Phase B



Phase C

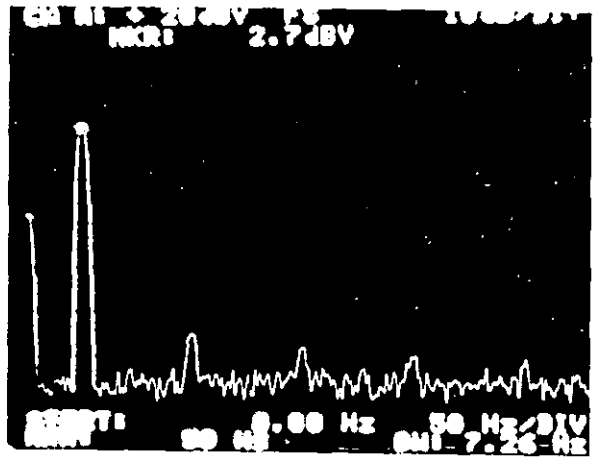


Fig. 4.21. Harmonic spectra at the output of the double-edge PWM generator

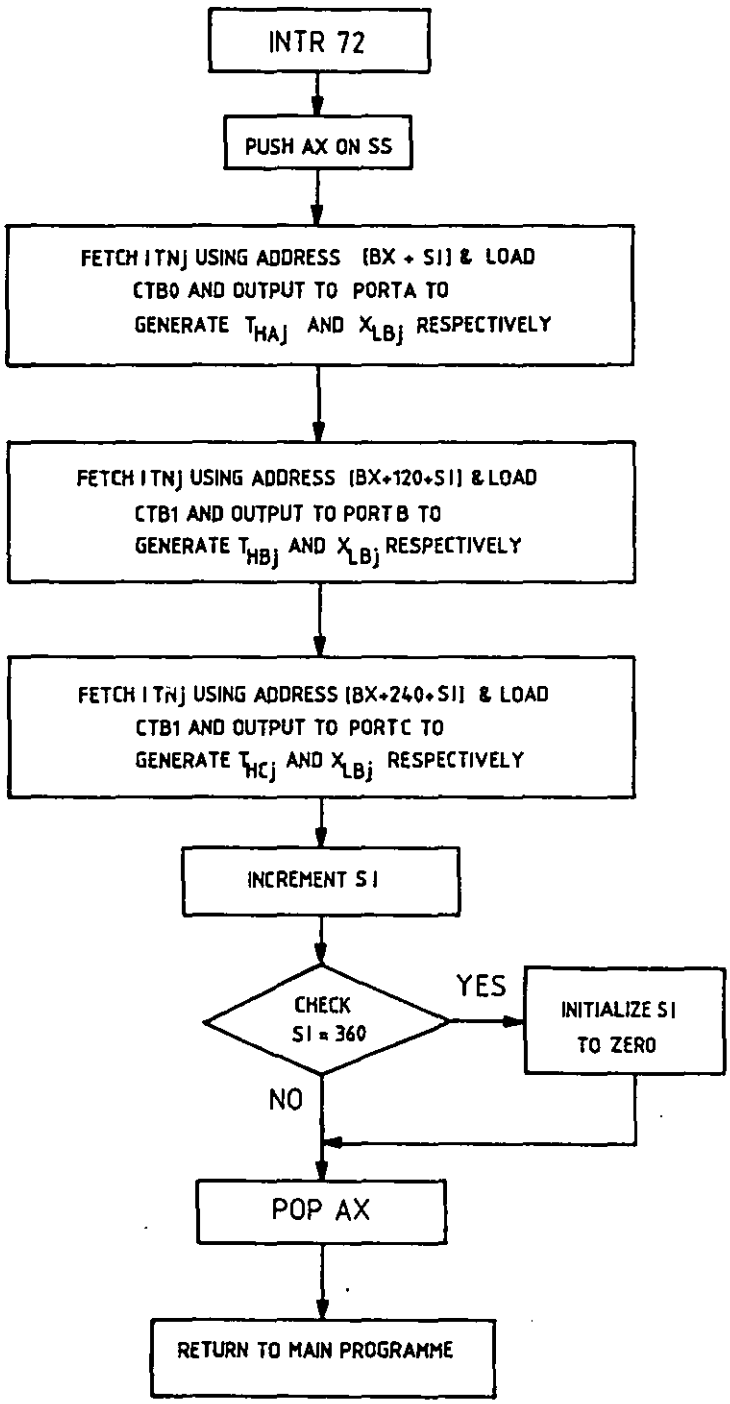


Fig. 4.22 FLOW CHART OF INTERRUPT 72 IN CASE OF THREE-PHASE PWM USING DOUBLE-EDGE MODULATION.

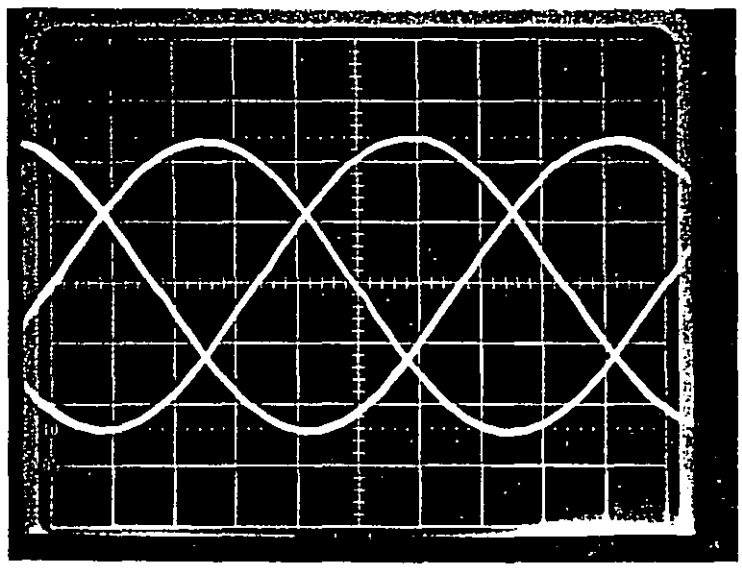


Fig. 4.23. Three-phase output voltage waveforms
Scale: 20V/DIV, 2ms/DIV

CHAPTER FIVE

FREQUENCY AND PHASE SYNCHRONISATION

Since a UPS system requires its output frequency and phase synchronised with the mains, this chapter describes a frequency synthesizer using a standard PLL circuit controlled by the microprocessor and a novel phase synchronising technique also implemented by the microprocessor. In order to measure the phase difference between the two signals, a phase difference detection circuit is utilised which works in conjunction with the microprocessor and to generate the synchronised output waveform, a software routine is employed.

5.1 FREQUENCY SYNCHRONISATION

When a UPS system needs to be operated in parallel with the other systems or the provision for a static bypass switch is to be made, the control circuitry of the system must be capable of ensuring frequency synchronisation. To achieve this entirely by digital means, such as by microprocessor control, the mains frequency needs to be measured precisely. This information can then be used by the microprocessor to generate the required output frequency.

Two schemes are described in the literature. One scheme uses a digital-to-analogue converter and a voltage controlled oscillator, and implements the PLL functions by software for generating synchronised firing signals for a three-phase rectifier with a resolution of 0.5^{o} [El-Amawy and Mirbod - 1988]. Another scheme described is a microprocessor controlled digital frequency synthesizer employing a standard PLL circuit. A fixed frequency reference signal is used and the gain of the PLL circuit is modified by the microprocessor as required by the system [Khan and Manning - PESC89]. Since this scheme measures the mains frequency by performing period measurements and then updates the gain of the PLL circuit, it requires a large number of look-up-tables for proper synchronisation even to follow the mains frequency from 49 Hz to 51 Hz, whereas the former technique is merely designed for the rectifier control circuit. A simplified microprocessor controlled frequency synchronisation technique is used.

5.1.1 Frequency Synthesizer

The circuit diagram for the digital frequency synthesizer is shown in Fig. 5.1. A zero crossing detector ZCD1 provides a square wave output from the mains input. A combination of the gates A_1, A_2, A_3 and an inverter is utilised to select the mains input or a crystal controlled fixed frequency of 50 Hz from the output of the counter CTC1. This is controlled by the least significant bit of the "PORTA"; a low bit allows the PLL circuit to follow the mains frequency, whereas a high bit connects the input of the 74HCT4046A PLL circuit to the fixed 50 Hz reference frequency signal. The phase comparator PC1 is utilised which is an EXCLUSIVE-OR network since PC1 configuration allows the VCO to oscillate at the centre frequency when there is no input signal or when there is noise on the input signal. A D-type flip-flop and a 16-bit counter CTC0 (programmed in square wave mode) are utilised to achieve the number N equal to 2x39960. To obtain the centre frequency f_0 = 3.996 MHz, the values of R_1 = 3 kΩ and C_1 = 4 nF are utilised. The combination of R_1 and C_1 provides the locking range of $2f_L$ = 500 kHz. A low pass filter based on R_3 = 5 kΩ and C_2 = 2 μF is utilised to prevent any large frequency swing in the output in response to large step changes in frequency demand. The rate-of-change of frequency will be checked by the microprocessor as will be explained in the next chapter.

At start-up, the reference frequency signal f_R = 50 Hz is obtained from the output of the counter CTC1, which is programmed in a mode to generate the square wave output required by the PLL type utilised. The output of ZCD1 is connected to the gate G2 of the counter CTC2 after dividing by two to perform the period measurements of the mains. The counter CTC2 is programmed in readback command mode, which enables the microprocessor to check the output pin status and to read the content of the counter by software. If the mains frequency is within the specified limits, the microprocessor connects the mains frequency signal by outputting zero at the PORTA, otherwise the crystal controlled reference frequency remains connected to the PLL circuit to generate the 50 Hz frequency output. In the latter case, the microprocessor also inserts zero in the control byte "MAINAVL" which means that the mains is not available otherwise it contains 0FFH. The microprocessor reads the counter CTC2 to ensure that the mains frequency is within the specified limits and also updates the byte "MAINAVL". This control byte is always checked before transferring load from the inverter to the mains as will be explained in the next chapter.

5.2 Phase Difference Measurement And Synchronisation

The frequency synchronising technique as previously described synchronises the inverter output frequency with that of the mains. Both the inverter and the mains supplies may have the same frequency but may differ in phase. The effective transfer of the load would then not be possible without disturbances and it would not be possible to operate the inverter in parallel with the mains supply. To synchronise the inverter output waveform in phase with the mains, it is vital for the microprocessor controlled system to measure the phase difference digitally and to ensure phase synchronisation by the microprocessor.

New schemes are described to measure the phase difference between the two signals of the same frequency by the microprocessor, and a software based technique is devised for generating the synchronised output waveform. The schemes utilised are capable of providing phase difference directly in electrical degrees with a resolution of 0.1 degree and to generate synchronised inverter-output waveform with an accuracy of the 0.5 degree.

5.2.1 Phase Difference Measurement Circuit

The circuit diagram of the Phase Difference Measurement (PDM) circuit is shown in Fig. 5.2. This circuit generates the signals to enable the microprocessor to read the phase difference between the mains and inverter output waveforms.

As can be seen from Fig. 5.2, the step-down voltages from the mains and the output of the inverter are fed to the inputs of the zero crossing detectors ZCD1 and ZCD2 respectively.

Monostables M1 and M2 each produces output pulses of 13.5 μs duration at every negative going zero crossing points of the inverter output waveform and the mains respectively. The Q-outputs of the monostables are NORed and then fed into the gate G0 of the counter CTD0. The counter is programmed in hardware retriggerable one-shot mode with readback command and its one-shot is 20.4 ms which is equal to the period of the minimum output frequency (49 Hz). When both signals are in phase, the counter receives trigger pulses through the NOR gate at regular 20 ms intervals and its output remains low, otherwise it goes high. The microprocessor checks the output pin of the counter CTD0 by software in every cycle to ensure the phasing of the two signals.

The outputs of M1 and M2 also set and reset respectively the flip-flop F1, the Q-output of which provides a pulse width equal to the phase difference between the two signals. A Single-Pulse-Selector (SPS) circuit is also utilised to provide a complete single pulse whenever it is enabled.

When the microprocessor finds the output of the counter high, it generates an enabling pulse via counter CTD2 to enable the SPS circuit. The enabled SPS circuit then allows the pulse to be let through to the counter CTD1.Then counter CTD1 starts and keeps counting down so long as its gate is raised high. The counter is clocked with the180 kHz frequency signal output of the counter CTE2 derived from the frequency synthesizer so that the counter can generate directly the phase difference in electrical degrees and with the resolution of 0.1 degree.

5.2.2 Phase Synchronisation

As explained in Chapters Three and Four, the pulse widths are calculated and the PWM pulses are generated in relation to the prospective carrier period. In addition the carrier frequency is varied to synchronise the inverter output frequency with that of the mains. Thus, the ratio of the carrier frequency to the output frequency always remains constant i.e 360. The technique used for generating the PWM pulses effectively divides a cycle into 360 equal segments. Also, a record of which segment is currently being constructed is updated in the look-up-table pointer (i.e SI) by the microprocessor. A segment may therefore be used as a step for phase synchronisation.

The scheme based on a software routine for incrementing/decrementing the pointer was utilised. It was also decided to limit the amount of increment or decrement in the pointer to one per cycle so as to limit the amount of distortion introduced in the PWM waveform. The microprocessor checks the availability of the mains by checking the control byte "MAINAVL". If it finds "OFFH" it then proceeds to the next step required for phase synchronisation, otherwise it takes no further action as there is no mains reference present and the PLL circuit is using the crystal controlled fixed reference signal of 50 Hz. In the former case, the microprocessor checks the output status of the counter CTD0 in each cycle to determine whether both signals are in phase with each other. In the latter case, the microprocessor performs the following steps to ensure the correct phasing of the two signals:

1. It loads the counter CTD2 to provide a 10 μs pulse to enable the single-pulse-selector circuit which in turn lets through a pulse to the counter CTD1.
2. In the next cycle, it reads the counter CTD0 and decides whether the inverter output waveform leads or lags that of the mains: The inverter leads if the content of the counter is less than 1800, otherwise it lags. The decision about whether the pointer should be incremented/decremented or considered as synchronised is based on the following facts :
   a. If the inverter output voltage waveform leads or lags the mains supply voltage waveform by an angle equal to or less than 0.5^{o}, it will be considered synchronised.
   b. The pointer will be incremented by one in each cycle until both waveforms become synchronised if the following condition occurs:

      $179.9^{o} \geq$ Inverter lags $> 0.5^{o}$

   c. The pointer will be decremented by one in each cycle until both waveforms become synchronised if the following condition occurs:

      $180^{o} \geq$ Inverter leads $> 0.5^{o}$

   The flow chart of the subroutine is shown in Fig. 5.3.

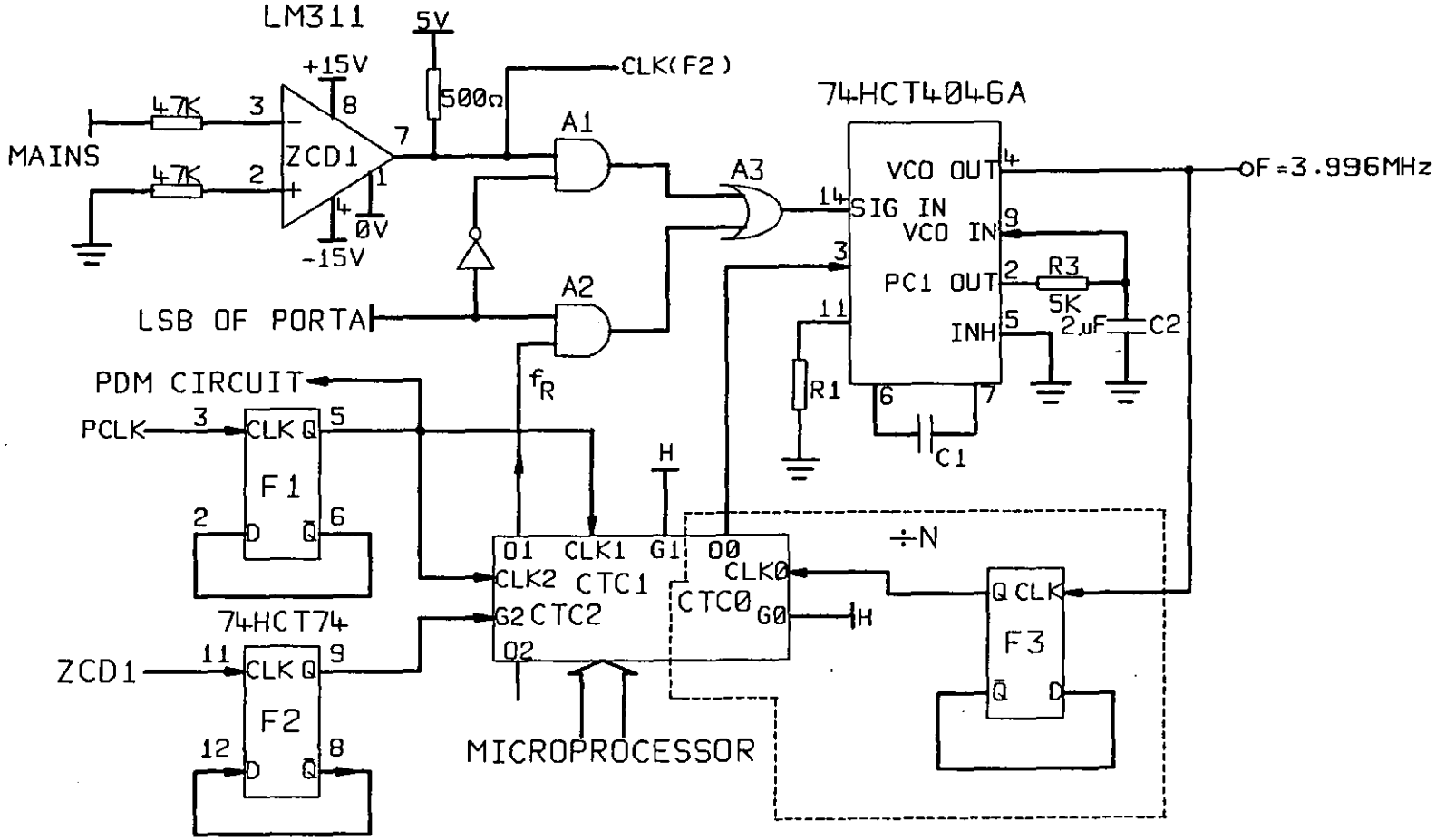


FIG 5.1 CIRCUIT DIAGRAM OF THE FREQUENCY SYNTHESIZER

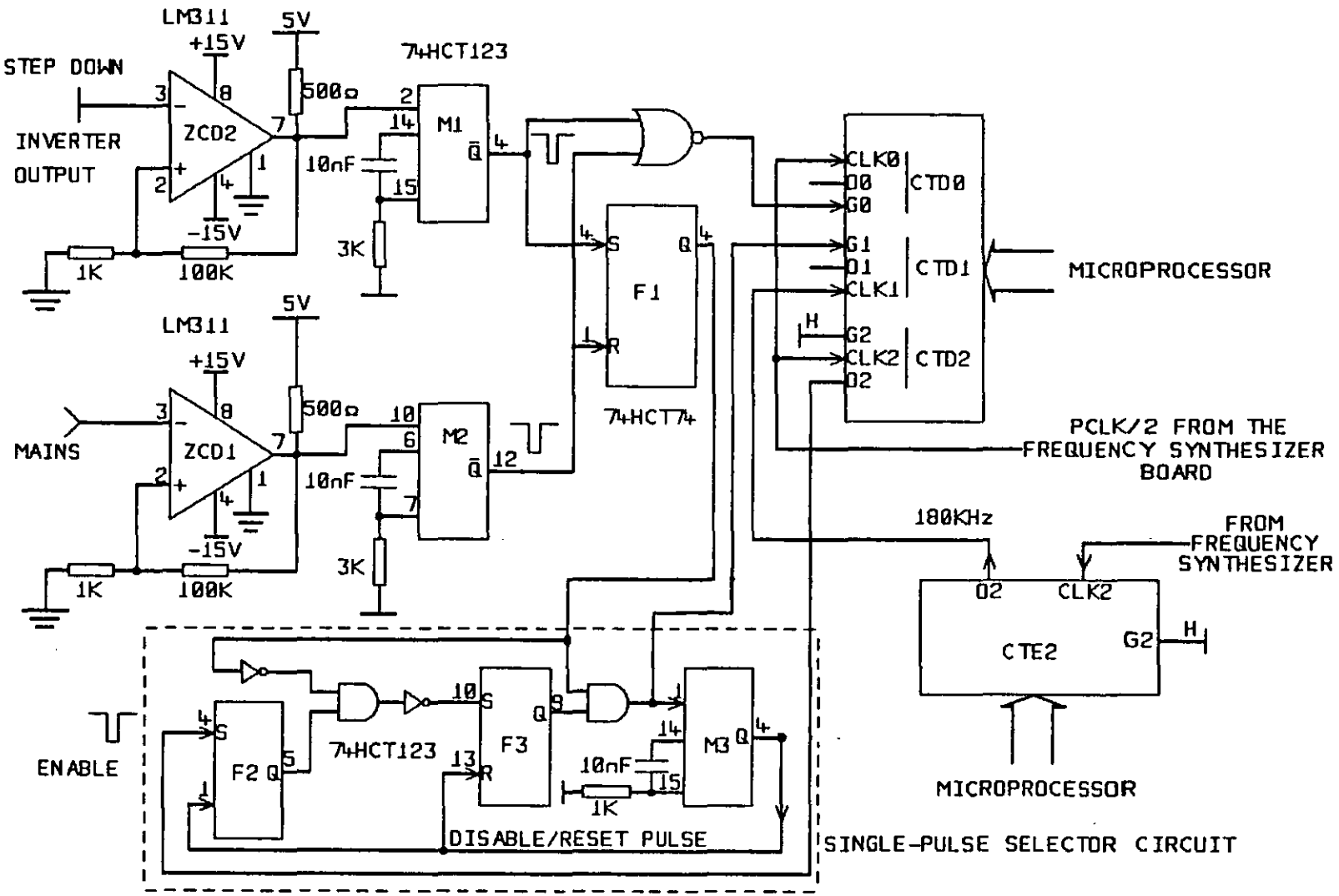


FIG 5.2 PHASE DIFFERENCE MEASUREMENT (PDM) CIRCUIT

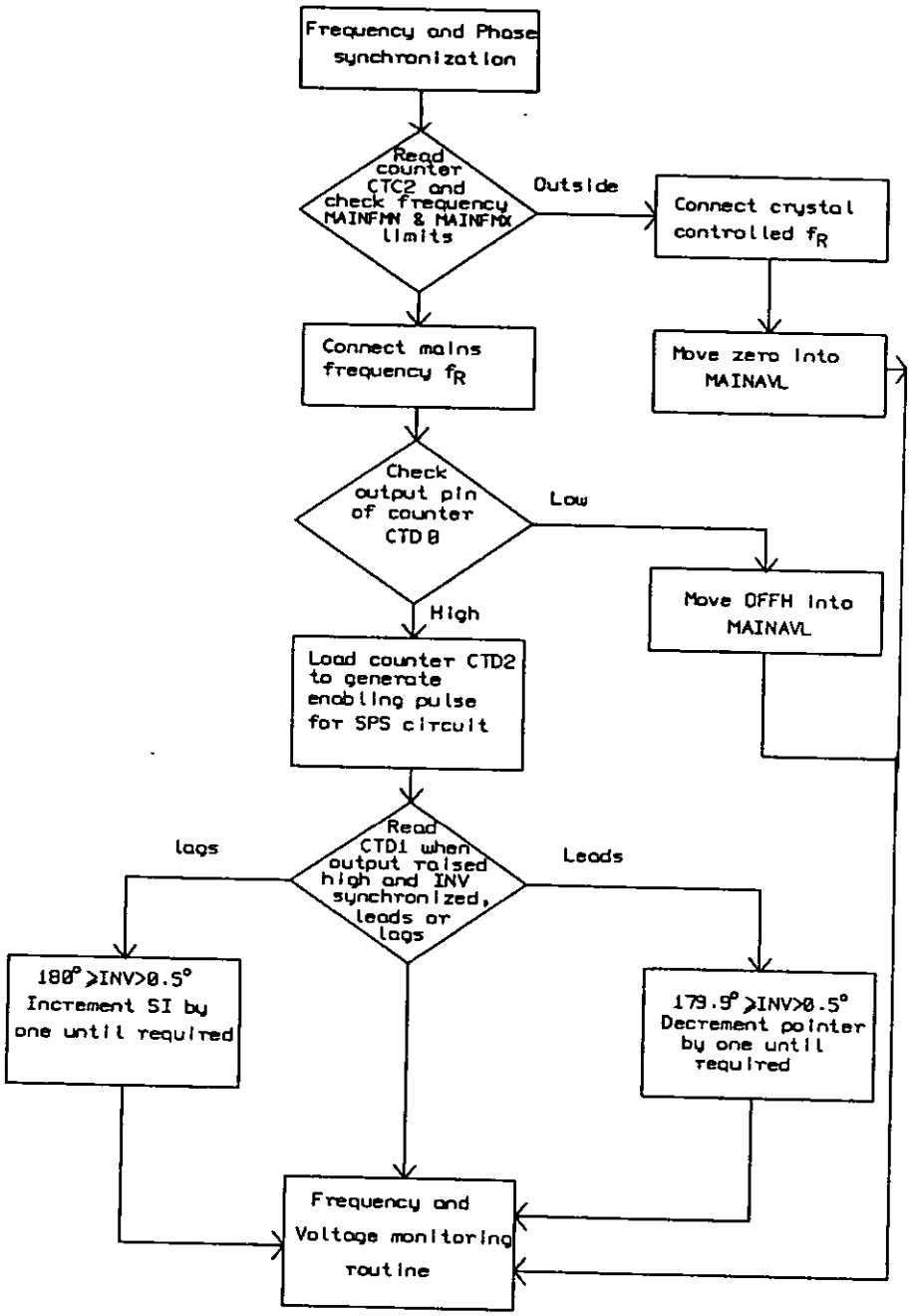


Fig 5.3 The flow chart of Frequency and Phase Synchronization routine

CHAPTER SIX

FREQUENCY AND VOLTAGE MONITORING TECHNIQUES FOR OPERATING STATIC TRANSFER SWITCHES

Since static transfer switches are normally employed for the uninterruptible transfer of load to an alternative source in case of any abnormalities in voltage and frequency, a control circuit capable of detecting abnormalities with fast response is required. This chapter is concerned with the frequency, rate-of-change of frequency and voltage monitoring techniques. The frequency measurement and rate-of-change of frequency are determined by the microprocessor, whereas to monitor the voltages, a rectified sine wave reference is generated and constantly compared with the output waveform.

6.1 STATIC TRANSFER SWITCHES (STS)

Almost every UPS system has some sort of alternative power source so that the load can be transferred to the available source in case the UPS inverter starts malfunctioning. To transfer the load from one source to another, three types of output switches are commonly used; electromechanical, static and a hybrid of the two, and the selection of these normally depends upon the type of load and the level of power.

However, standard UPS systems are equipped with static transfer switches where a single switch is comprised of two power SCRs connected antiparallel in series with the load as shown in Fig. 6.1. These can transfer the load between the inverter output and the alternative power source fast enough to accomplish a "no break" in power during transition. To achieve this, the inverter must have circuits to make sure that the output waveform produced by the inverter is synchronised in time-phase relationship with that of the mains. In addition, the control circuits for the static transfer switches must have capability of quick detection of the abnormalities in the frequency and voltages with fast response.

6.2 QUICK FREQUENCY MONITORING TECHNIQUES

In order to protect the critical loads from excessive frequency variations, a frequency measurement technique equipped with fast response is required and which also enables to

calculate the rate-of-change of frequency. Some loads may or may not be sensitive to frequency instability; switching power supplies can accept a wide frequency variation whilst some CRT displays demand 50 Hz ± 0.01%. The rate-of-change of frequency is especially important for installations employing motors such as disk drives in computer systems. A sudden change in frequency could result in an unacceptable high inrush current to the motor. Consequently, the maximum slew rate allowed for most critical loads is about 0.5 Hz/s. The speed of detection of minimum/maximum frequency limit and the maximum permitted rate-of-change of frequency are extremely important for the quick activation of the static transfer switches.

Considering the measurent of the 50 Hz power line frequency, conventional counters using a one-second gate pulse may display 49 or 51 Hz, with ±1 count error. Increased resolution can be obtained at the expense of increased time of measurement, for example using a 10-second gate pulse, but this increased time will be impractical for this application. Period measurements can be made to obtain a high resolution and fast response. Associated period measurement techniques have been used for minimum/maximum frequency indication [Venkateswaran and Seshadri - 1980, Rathore et al - 1987]. These use a large number of discrete digital components and lack versatility.

In this project, a scheme using a zero crossing detector ZCD1, a flip-flop and a 16-bit digital counter CTE0 in conjunction with the microprocessor is utilised to perform period measurements as shown in Fig. 6.2. The counter CTE0 is programmed in readback command mode and it starts counting down as soon as the signal at the gate goes high and it stops counting with a low level signal at the gate. The microprocessor reads CTE0 25 times in one second in the alternate cycles and stores the values in a table, FREQCHART, which is used to determine the rate-of-change of frequency. Every time the microprocessor reads the counter, it compares the newly taken reading with numbers corresponding to the minimum and maximum preset frequency limits which are 49 Hz and 51 Hz respectively. If the reading is within the specified limits only then will the microprocessor proceed further to calculate the rate-of-change of frequency, otherwise it activates the static transfer switch by outputting the byte CONTFSS at the port, PORTA after setting high its most significant bit.

In order to calculate the rate-of-change of frequency, the microprocessor shifts all the values one bit forward by discarding the 25th value from the table FREQCHART, and then stores the newly taken reading at the top of the table. It then compares the newly taken

reading with the 25th value to determine the rate-of-change of frequency since it is considered a straight line from 49 Hz to 51 Hz on the time versus frequency graph. If it finds the rate-of-change of frequency less than 0.5 Hz per second it does not take any action otherwise it activates the static transfer switch. This scheme enables the system to check the minimum/maximum frequency limits and rate-of-change of frequency in the alternate cycle of the nominal 50 Hz output.

6.3 DIGITAL TECHNIQUES FOR DETECTION AND MEASUREMENT OF DISTURBANCES OF LOAD VOLTAGE

6.3.1 General

Almost all recently designed UPS systems are equipped with PWM inverters which are essentially switched at frequencies higher than the required output frequency. This enables the harmonics of the switching frequency and its side bands to be filtered out with the use of low pass filters having small inductors and capacitors (instead of filters tuned at the 50 Hz fundamental frequency) and which endows the system with fast transient response. Small filtering components are liable to store rather less energy, thus necessitating the need for fast detection of voltage disturbances.

Some voltage sensing methods have been investigated [Dewan and Ziogas - 1977]. These are developed for feedback control systems, and are based upon a comparison between the output signal and a DC reference signal. The resulting error signal is integrated. These methods suffer from integration delays which cannot be tolerated for quick detection. A method for quick detection of voltage disturbances is discussed [Jeftenic and Gvozdenovic - 1987] in which the rectified output voltage is integrated over the period T/4 and compared with the DC reference at the end of each selected period. This method has a minimum limit of detection period T/4. Another analogue technique [Biswas et al - 1987] reported is based on the constant comparison of the output waveform with a phase-locked reference sine wave. This circuit is liable to generate a phase shifted output waveform (due to the phase comparator's output filter) at the instant of sudden change in phase/frequency at the output. Consequently this could initiate false activation of the static switch. The aforementioned techniques rely entirely on analogue circuitry, and also are not flexible and are unsuitable for monitoring distorted waveforms.

6.3.2 Description And Working Principle Of The Circuit

The circuit adopted consists mainly of the following parts; a sinewave reference generator with a zero crossing detector, a window comparator, a disturbance pulse width limit adjuster, a precision full-wave rectifier and a 16-bit counter in conjunction with the microprocessor. The complete circuit diagram is shown in Fig.6.2.

The step-down voltages from the output of the inverter are fed to the inputs of the zero crossing detector, ZCD1 and the precision full-wave rectifier. The monostables M1 and M2 each produces output pulses of 56 μs duration at positive and negative zero crossing points respectively. These pulses reset and restart the counting of the binary counters B1 and B2, the output lines of which are used to provide addresses to a PROM for outputting the stored sinewave values. As the counter is incremented, a new digital number is provided to the input of the digital to analogue converter which converts the digital number to an analogue signal. This analogue signal is amplified by the linear amplifier, A1 for providing the synchronised sine wave references, whereas the high voltage reference, V_{HR} and the low voltage reference, V_{LR} are generated with the aid of two potentiometers. These potentiometers can be calibrated at different voltage settings so that the reference voltage may be changed even during operation if it is deemed to be necessary.

The output of the inverter rectified by the precision full-wave rectifier is fed to the input of the window detector through a diode for comparison with the lower and upper preset limits. Both the reference voltage and the rectified output of the inverter are passed through the diodes to minimise the zero crossing notch points as shown in Fig.6.3, otherwise a superimposed zero crossing may have raised the window detector output high. This enables the magnitude of the reference voltage to be set almost at the same value of the input voltage and to construct a circuit devoid of false triggering. A monostable M4 with a variable resistor, V_{pw} is utilised to provide the inhibition period variable from a few micro-seconds to 10 ms. The Q-output of M4 is ANDed with the output of the window comparator. The ANDed output is ORed with the frequency error signal to be generated by the microprocessor and its output is again ANDed with the voltage obtained from the inhibition switch, S_I which provides a high level signal at the input of the AND gate in enabled mode, otherwise a low level signal. The switch S_M is used to activate the static switch manually. Another switch, S_D is used to enable/disable the disturbances let through

to the counter, CTE1 which is used to measure the duration of the disturbances whenever these are required to do so.

Since the counters are reset at every zero crossing and the 18 kHz carrier signal is used to clock the counters, the output of the digital to analogue converter is forced to be synchronised with the inverter output waveform without any complications. As the rectified output waveform is compared with the synchronous reference waveform, any deviation of the output waveform from this will be instantaneously detected by the window detector circuit. When the output voltage is within the specified limits, the output of the comparator stays at zero otherwise it changes state from low to high. This change of state will initiate the static transfer action, with the static transfer switch being fired after the inhibition period set by the disturbances pulse-width adjuster.

The amplitude window detector provides a high pulse of duration equal to that of the disturbances in the output voltage. The rising edge of the pulse enables the counter CTE1 and its output goes low and remains low until the disturbance is over. The microprocessor reads the counter and saves the value in memory or it could display the newly measured disturbances. Since no video terminal is interfaced to the controller board, this program routine is simply abandoned. The control circuit is tested and its output signal is shown in Fig. 6.4 together with the inverter output waveforms at the time of its failure. It can be seen in the figure that the action of the control circuit is instantaneous and this can be delayed by introducing the inhibition period if it is required. Since no static switch is utilised physically and only the control circuit with the required software was developed, the program routine used to measure the frequency and voltage disturbances was simply abandoned so that the microprocessor does not execute unnecessary codes. The flow chart of that subroutine is shown in Fig. 6.5.

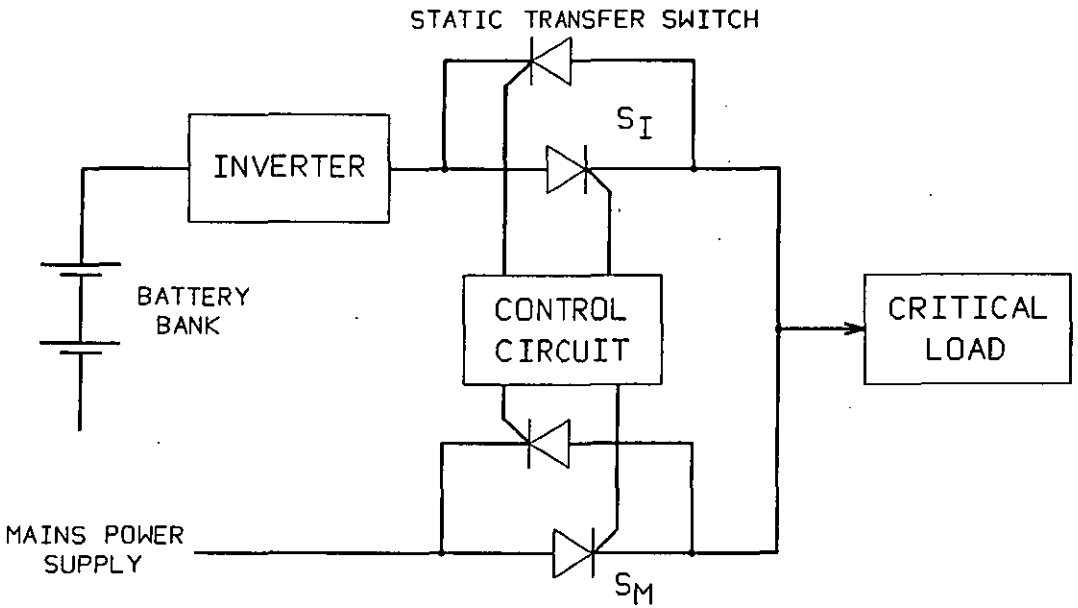


FIG 6.1. A UPS SYSTEM WITH STATIC TRANSFER SWITCHES

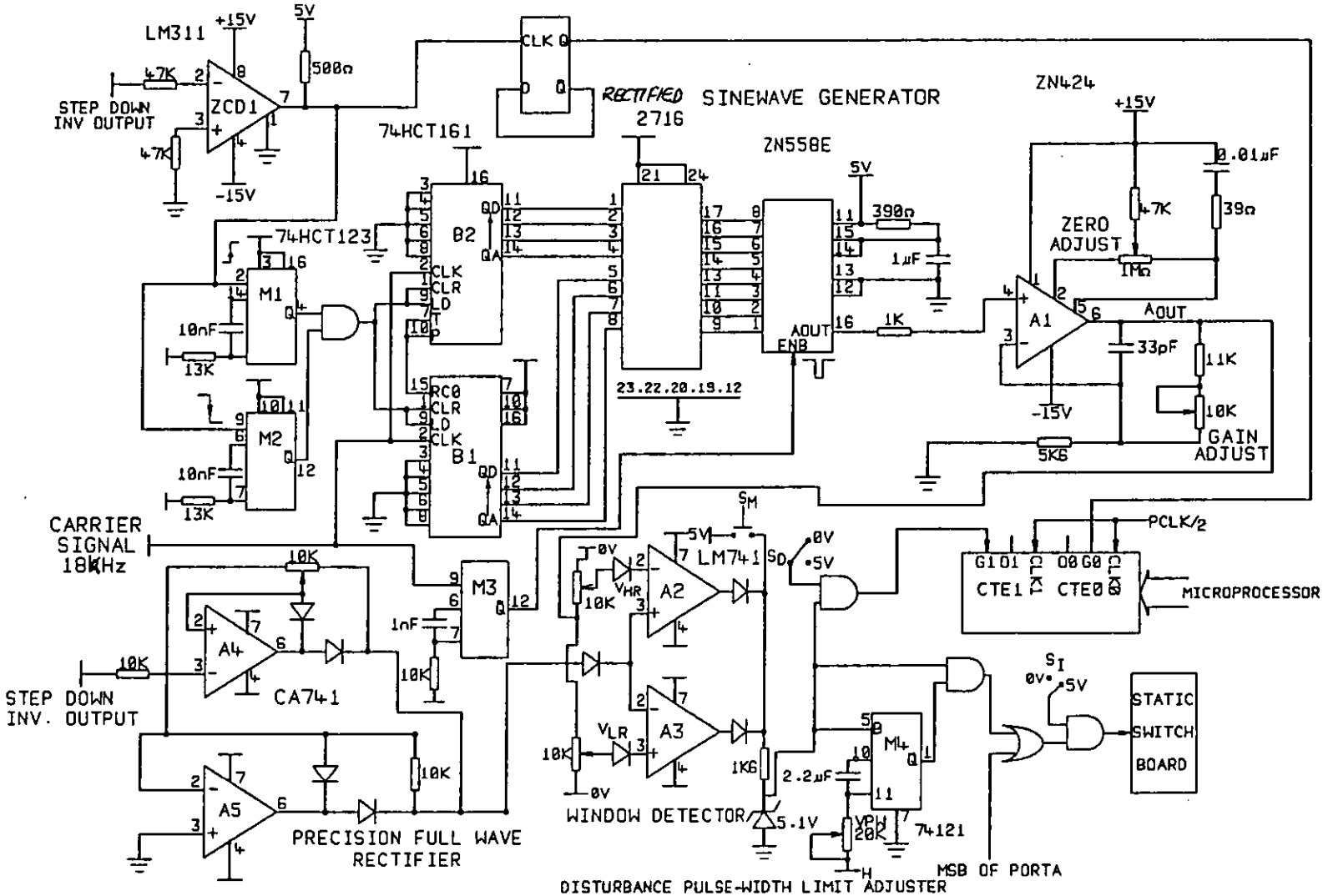


FIG.6.2 FREQUENCY AND VOLTAGE MONITORING CIRCUITRY

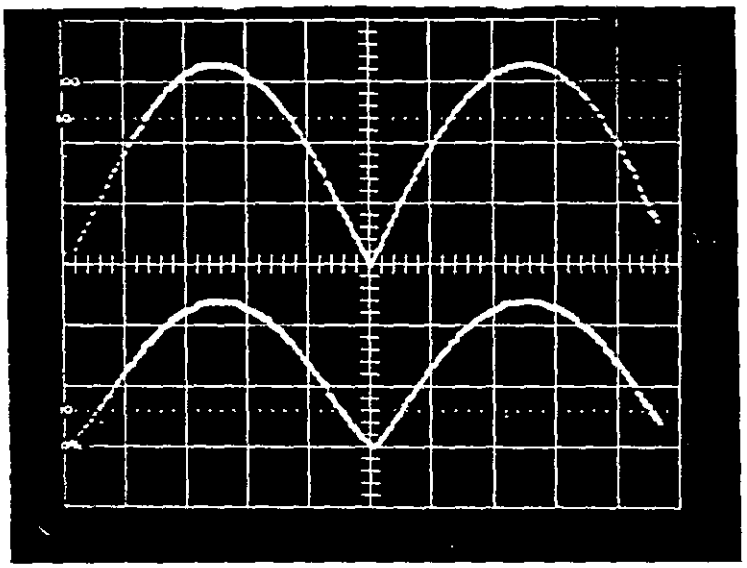


Fig. 6.3. Rectified sine reference waves with and without diodes in series
Upper Trace without diode
Lower Trace with diode
Scale: 1V/DIV, 2ms/DIV

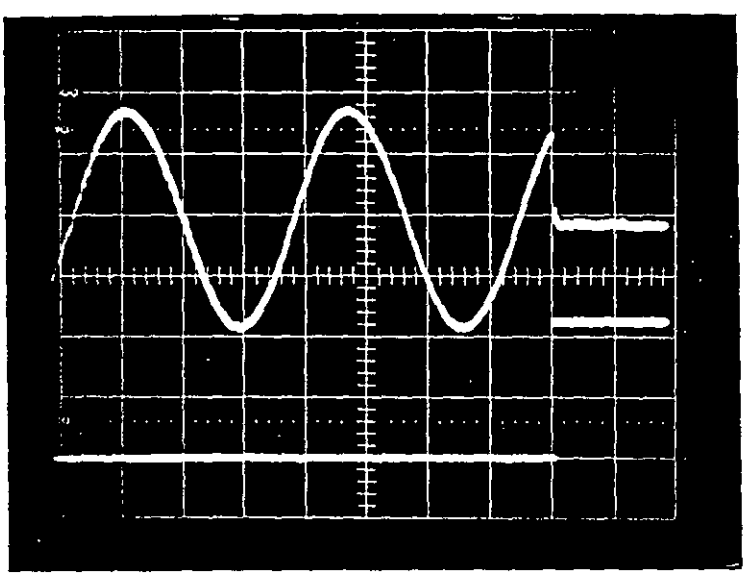


Fig. 6.4. Operation of control circuit
Upper trace; Inverter output waveform
Scale: 1V/DIV
Lower trace; Output of the control circuit
Scale: 2V/DIV, 5ms/DIV

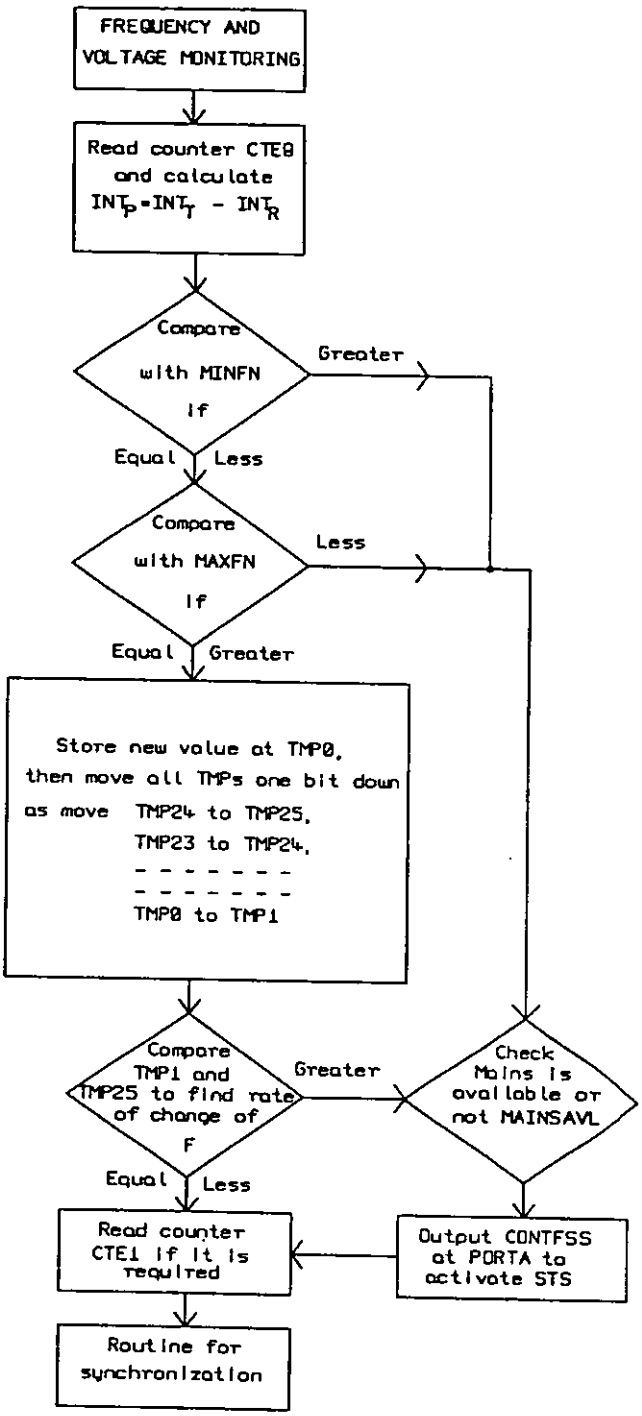


Fig 6.5 The flowchart of the frequency and voltage monitoring routine

CHAPTER SEVEN

CONTROL SYSTEMS

This chapter describes the PI controllers which are utilised to regulate the inverter output voltages. For the single-phase inverter an analogue PI controller is used, whereas for the three-phase system both analogue and digital PI controllers are utilised. In the design of the digital PI controller, an experimental method was adopted to determine the transfer function of the three-phase system from which a model of the system was constructed. A software package, SIMBOL2, was then used to design a digital control algorithm in the w-plane to be directly implemented by the microprocessor.

7.1 OPEN AND CLOSED LOOP CONTROL SYSTEMS

An open-loop dynamic control system can be represented by the general block diagram shown in Fig. 7.1. This system is activated by a signal input where no provision is made in this system for the supervision of the output and no mechanism is provided to compensate any deviation occurring due to the system components. Although it is preferable to operate a system in an open-loop mode whenever possible, the output performance so achieved more often fails to obtain the required performance criteria. Thus a closed-loop system is mandatory as it is the only system that can fulfil the demanding performance requirements. However, it must be carefully designed.

A closed-loop system is shown in Fig. 7.2. This system obtains the current status of the output and generates an error signal proportional to the difference between the input and the output. A closed-loop system drives the output until it approaches the input in an attempt to reduce the error signal to zero. Consequently, any difference between the actual and desired output status will be automatically compensated by virtue of the closed-loop control.

The main purpose of the closed-loop control system is to reduce the error signal to zero and keep it zero at all times, but this is not possible in practice. In general the performance of the closed-loop system is a function of the measurement accuracy of the disturbances, stability, sensitivity and dynamics of the system. Performance criteria generally are specified by total harmonic distortion in the output waveform, steady-state output voltage regulation and transient response.

A closed-loop system must be stable under all possible operational conditions which include changing command signals, disturbances and any change in loop parameters. Any system can be regarded as a stable system as long as variations in the reference signal result in controlled changes in the system output. Consider the feedback control system shown in Fig. 7.2. The closed-loop transfer function of the system is:

$$\text{Gain} = \frac{\text{Output}}{\text{Input}} = \frac{G(s)}{1 + G(s)H(s)} \tag{7.1}$$

where the product of G(s) and H(s) is known as the open-loop transfer function, G(s) is the transfer function of the forward path, and H(s) is the transfer function of the feedback path. When the product of G(s)H(s) becomes equal to $1\angle 180^{o}$ at any frequency, then the system becomes unstable. This is the Nyquist criterion. The degree of the stability of a closed-loop system can be defined in terms of two parameters, namely, gain margin and phase margin, both easily can be obtained from a Bode plot of the system transfer function. The gain margin is the amount by which the product $|G(s)H(s)|$ is less than unity at a phase angle of -180^{o} whereas the phase margin is the amount by which the phase is short of -180^{o} at unity gain (i.e. 0 dB), as shown in Fig. 7.3.

7.2 FREQUENCY RESPONSE ANALYSIS

Analytical techniques can be employed to determine the transfer function of the system. However, if it is complicated or not feasible to obtain the transfer function through analytical means, several standard test signals such as step, ramp and sinusoidal signal can be used for this purpose.

In digital control systems, analysis is often carried out in the z-domain. However, the frequency response method is not a practical tool in the z-domain because the e^{jwt} term inherent in z-domain analysis destroys the simple character that is the attraction of the frequency domain analysis. This difficulty, however, can be overcome by transforming the pulse transfer function in the z-plane into that in the w-plane. This transformation, commonly called the w-transformation, is a bilinear transformation given by:

$$z = \frac{1 + (T/2)w}{1 - (T/2)w} \tag{7.2}$$

After the w-transformation, the frequency oriented design techniques can be used to design a controller. The resulting controller may then be transformed back to the z-domain to develop a digital control algorithm.

In addition, the advantages of using the w-domain in contrast to the usual s-domain approach, are that the effects caused by sampling are modelled and taken into account at the early design stage rather than being considered at a later discretization [Leigh-1985].

7.3 PID CONTROLLERS

The Proportional Integral Differential (PID) controllers are most widely used in most control systems. The block diagram of an analogue PID controller is shown in Fig. 7.4 which shows that the PID controller is acting on the error signal E(t) obtained from the difference between the reference signal R(t) and the feedback signal C(t). The transfer function of the analogue PID controller can be written as:

$$G(s) = \frac{U(s)}{E(s)} = K_P + \frac{K_I}{s} + sK_D \tag{7.3}$$

The output of the controller in the time-domain is

$$U(t) = K_P E(t) + K_I \int E(t)dt + K_D \frac{dE(t)}{dt} \tag{7.4}$$

Eqn. 7.4 shows that the proportional control multiplies the error signal E(t) by a chosen constant K_P, the integral control multiplies the integral of the error signal E(t) by K_I and the derivative control generates a signal proportional to the time derivative of the error signal. Derivative term provides the stabilising influence on the system by anticipating the overshoot. The designer's main task is to choose the suitable values for the constants K_P, K_I and K_D so that the operating system meets the desired performance criteria.

The simplest form of a controller can be realised by using a single term proportional control. This type of controller always generates an output signal proportional to the error

signal and is known as a proportional controller.Thus, the tuning of Kp to the correct value ensures that the controlled system output attains the set point in a fast manner. However, a controller containing only a proportional term is an uncompensated one and it leads to a sizable steady-state error signal. The steady-state error can be minimised by introducing an integral control term, since the integral of a constant error produces a ramp signal which tends to change the system output in such a way that the error signal is eventually reduced to zero. When a PI controller responds to a unit step error, the output of the proportional control rises instantly by an amount Kp. As long as the error persists, the integral control term continues to increase the system output with a constant rate. Since varying the values of K_P and K_I results in varied degrees of overshoot and rise time responses of the system, the controller can be tuned to achieve the required performance. If the dynamics of the basic uncompensated system are such that the PI controller is adequate to give good system response, then the more complex PID controller is not necessary, and the simpler PI controller may be employed.

7.3.1 The Analogue PI Controller

Single-phase and three-phase power MOSFET inverters with their filter components are shown in Figs. 4.8 and 4.9. The approximate transfer function of the inverter and filter could be described as:

$$P(s) = \frac{K_n}{s^2LC + s\frac{L}{R} + 1} \tag{7.5}$$

where K_n is the gain of the inverter, L is the output filter inductor, C is the filter capacitor and R is the load. It can be seen from the above that the system is of second order. A proportional plus integral control can therefore be utilised and the equation for such a controller in the time domain can be written as:

$$U(t) = KE(t) + \frac{K}{T_I}\int E(t)dt \tag{7.6}$$

The proportional and integral time constants are chosen to ensure stability and to give

adequate dynamics of the closed-loop system. The circuit diagram of the analogue PI controller is shown in Fig. 7.5. The filtered step-down output voltage was fed to the input of A1 and then its output is inverted by A2 before being fed to the sample and hold circuit. The output of the inverting amplifier is limited to 10 V and the detailed connections are described in section 4.1.2. The A/D conversion process and its synchronisation with the signal for interrupt INTR73 is shown in Fig. 4.3. However, in this application, a 300 μs sampling period was used because the microprocessor does not have to compute any control algorithm. An EPROM containing integer numbers is interfaced to the A/D converter board, the output of which is being read by the microprocessor at 300 μs intervals. This EPROM contains integer numbers from 1 to 46 since the 46 look-up-tables are used and these are linearly distributed in 0 to 255 address locations. It is clear from Fig. 4.3 that the sampling and conversion process works in relation to the interrupt signal responsible to cause interrupt INTR73. In this way the microprocessor reads the EPROM and outputs the integer number from the selected look-up-table to the counters in order to generate the appropriate PWM pulses to maintain the output voltage at the preset level. Since the microprocessor reads the processed error signal of the analogue PI controller from the EPROM, it does not require any computation time.

The design of the analogue controller was based on the approximate transfer function of the system. To achieve the required performance, a trial and error method was employed. The circuit diagram of the used analogue PI controller is shown in Fig. 7.5. The output voltages of the single-phase and three-phase inverters under step load change are shown in Figs. 7.6 and 7.7 respectively.The single-phase inverter recovered to nominal in less than three cycles whereas the three-phase inverter's recovery time is within a half cycle.

The voltage harmonic spectrums of single-phase inverter with single-edge as well as for double-edge modulation under seven amperes resistive load are shown in Figs. 7.8 and 7.9 respectively. The second and third harmonics in Fig.7.8 are -47.5 dB and -45.0 dB respectively but in in Fig.7.9 only the third harmonic has amplitude -45.0 dB relative to the fundamental. The fifth and seventh harmonics are approximately -50.0 dB each relative to the fundamental and all other individuals are well below - 50.0 dB.

7.3.2 The Digital PI Controller

When the PI control algorithm is to be designed for implementation by the microprocessor,

the sampling period needs to be chosen very carefully. It should be long enough so that the required calculations can be performed within the available period. Since the microprocessor is being periodically interrupted at the rate of the carrier frequency and requires a computation time of 25 μs to perform the required calculations at every interruption, it cannot execute other program routines continuously for more than 25 μs. As the interrupt INTR72 responsible for generating the PWM pulses has been given a higher priority, this interrupt will therefore be serviced even during the interrupt INTR73 used to implement the PI control algorithm. On the hand, the sampling frequency should be high enough so as not to degrade the performance of the controller. The basic sampling theorem states that a sampled continuous signal may be constructed from its samples, if and only if, the frequency contents of the signal is lower than $w_S/2$. Considering the sampling period of 1.11 ms, this condition is satisfied with the basic 50 Hz modulating waveform. However, as the bandwidth, w_b of the system approaches the sampling frequency, w_S, this condition is violated in the transient states. To minimise the distortion in the output voltage during fast transient disturbances, the control algorithm needs to be carefully designed. This requires accurate knowledge of the parameters of the system. This can be facilitated by adopting an experimental approach to determine the transfer function of the system. The design of the digital control algorithm can then be carried out in w-plane since it results in more accurate and precise control. Also designing in the w-plane allows the designer to adopt well known frequency domain analysis techniques.

7.3.2.1 Designing Of The Digital PI Controller

For designing the digital control algorithm, the frequency response analysis is used. In order to determine the frequency response of the open-loop system, the Bode plot is obtained through an experimental set up employing a Transfer Function Analyser (TFA) as shown in Fig. 7.10. The TFA's internal oscillator was used to generate the required sine wave signal which is fed to the input of the system. The system's response is taken from the bridge rectifier and fed to the input correlator of the TFA. For these tests, the TFA was programmed to generate sinusoidal waveforms of amplitude ±5 V and frequencies from 1 Hz to 1 kHz. The time period of 10 seconds was provided to ensure steady-state conditions were reached at every point. The frequency response plots (gain and phase) of the system obtained from the transfer function analyser are shown in Fig. 7.11. In the tests, a sampling period of 300 μs was utilised so that the controller should have negligible effect

on the frequency response analysis.

Looking at the Bode plot obtained from this arrangement, it can be seen that the gain and phase are constant up to 600 Hz and 100 Hz respectively. After that the phase lag is increasing towards 180^{o} but the gain still not having changed much until the 1 kHz frequency is reached. This implies that the system has a zero in the right half plane. A software package, SIMBOL2, was utilised in the analysis to produce a transfer function that best fitted the measured response.

When a good compromise fit was obtained, the transfer function was finalised as given below:

$$G_p(s) = \frac{0.4(1 - sT_2)}{s(1 + sT_1)(1 + sT_2)} \tag{7.7}$$

where $1/T_1 = 2350$ rad/s and $1/T_2 = 6250$ rad/s. The above equation can then be written as:

$$G_p(s) = \frac{940(6250 - s)}{s(2350 + s)(6250 + s)} \tag{7.8}$$

To obtain the digital equivalent of $G_p(s)$, the step-invariance method can be used as follows:

$$G_p(z) = Z\left[\frac{1 - e^{-Ts}}{s} G_p(s)\right] \tag{7.9}$$

$$= \left(\frac{z - 1}{z}\right) Z[G_p(s)]$$

$G_p(s)$ is expanded into partial fractions and the above equation rewritten as:

$$G_p(z) = \left(\frac{z - 1}{z}\right) Z\left[\frac{0.4}{s} - \frac{0.882}{s + 2350} + \frac{0.482}{s + 6250}\right] \tag{7.10}$$

After z-transformation, the above equation can be written as:

$$G_p(z) = \left(\frac{z-1}{z}\right)\left(\frac{0.4z}{(z-1)} - \frac{0.882z}{(z-A)} + \frac{0.482z}{(z-B)}\right) \tag{7.11}$$

where $A = e^{-aT}$, $B = e^{-bT}$

and $a = 2350$, $b = 6250$ and $T = 1.11 \times 10^{-3}$ second

After substituting the above values and simplifying, Eqn. 7.11 can be written as:

$$G_p(z) = \frac{K_1 z + K_2}{z^2 - K_3 z + K_4} \tag{7.12}$$

where $K_1 = 0.335513048$, $K_2 = 0.034669298$

$K_3 = 0.074615621$ and $K_4 = 7.14866385 \times 10^{-5}$

The transfer function $G_p(z)$ needs to be transformed into the w-plane, by using a bilinear transformation, so that the frequency response methods can be used on the discrete control system.

The bilinear transformation is defined as:

$$z = \frac{1 + w\frac{T}{2}}{1 - w\frac{T}{2}} \tag{7.13}$$

where T is the sampling period. By introducing Eqn. 7.13 into Eqn. 7.12 and after simplifying it can be written as

$$G_p(w) = \frac{(K_1+K_2)-K_2Tw+(K_2-K_1)T^2\frac{w^2}{4}}{(1-K_3+K_4)+(1-K_4)Tw+(1+K_3+K_4)T^2\frac{w^2}{4}} \tag{7.14}$$

By substituting the values of K_1, K_2, K_3, K_4 and T, the above equation is written as

$$G_p(w) = \frac{0.370182 - 3.848292\text{x}10^{-5}w - 9.266739\text{x}10^{-8}w^2}{0.925455 + 1.10992065\text{x}10^{-3}w + 3.3103\text{x}10^{-7}w^2} \tag{7.15}$$

By replacing w by jv, conventional frequency response techniques can be used to determine the frequency response of the system.

$$G_p(jv) = \frac{0.370182 - 3.848\text{x}10^{-5}jv - 9.266\text{x}10^{-8}j^2v^2}{0.9254558 + 1.109\text{x}10^{-3}jv + 3.310\text{x}10^{-7}j^2v^2} \tag{7.16}$$

The Nichols Chart of $G_p(jv)$ of the uncompensated system is shown in Fig. 7.13. This curve needs to be shifted upwards so that it becomes tangential to the closed loop contour at the required frequency (935 rad/s) with reasonable gain and phase margins.

Considering the expression for the PI controller, the compensation network will have a transfer function of the form [Forsythe - 1988]:

$$C(s) = \frac{K}{s}(1 + sT_R) \tag{7.17}$$

Therefore,

$$C(jw) = \frac{K}{jw}(1 + T_R jw) \tag{7.18}$$

At $w = w_m$, where

$$K = \frac{Mw_m}{\sqrt{1 + w_m^2 T_R^2}}$$

and

$$T_R = \frac{1}{w_m}\tan(90 - \phi)$$

By choosing $\phi = 45^o$, $w_m = 935$ rad/s and $M = 6$ dB ≈ 1.995, and introducing these values in the above equations, $K = 1315$ and $T_R = 1.0695 \times 10^{-3}$ s are obtained.

After introducing the values of K and T_R in Eqn. 7.18, it can be written as

$$C(w) = 1315\left(\frac{1 + 1.0695 \times 10^{-3} w}{w}\right) \tag{7.19}$$

Replacing w by $(2/T(1 - z^{-1})/(1 + z^{-1}))$ and after simplifying the above equation can be written as:

$$C(z) = \frac{1315[(\frac{T}{2} + 1.0695 \times 10^{-3}) + (\frac{T}{2} - 1.0695 \times 10^{-3})z^{-1}]}{(1 - z^{-1})} \tag{7.20}$$

Introducing the sampling period $T = 1.11 \times 10^{-3}$ s in the above equation and simplifies to:

$$C(z) = \frac{2.14(1 - 0.316z^{-1})}{(1 - z^{-1})} \tag{7.21}$$

The difference equations for the digital control algorithm can be written as:

$$y(k) = X_e(k) + y(k-1) \tag{7.22}$$

$$X_o(k) = 2.14[y(k) - 0.316y(k-1)] \tag{7.23}$$

The signal flow diagram for the above equations can be seen in Fig. 7.13. To simplify the above equations for the software implementation, the value of the y(k) is introduced in Eqn. 7.23 to give:

Then Eqn. 7.23 can be written as:

$$X_o(k) = 2.14[X_e(k) + 0.68y(k-1)] \tag{7.24}$$

Since the rectified output voltage is compared with the fixed DC reference voltage and it contains the ripple of frequency f_R=300 Hz and of amplitude 5.71% of the DC output, filtering is required based upon the three sampling instants to smooth out the ripple period. This is achieved by using a simple digital averaging filter with a transfer function of the form:

$$F(z) = \frac{1 + z + z^{2}}{3}$$

$$F(z) = \frac{0.33z^{-2} + 0.33z^{-1} + 0.33}{z^{-2}} \tag{7.25}$$

The microprocessor samples and averages the error signal at 1.11 ms intervals. It then implements Eqn. 7.24 by software and determines which look-up-table needs to be output to reduce the existing error signal. The flow chart of the digital control algorithm with the utilised gain values is shown in Fig. 7.14. The frequency response of the uncompensated system is shown in the form of a Nichols chart in Fig. 7.15. This shows that the phase and gain margins are 60^{o} and 8.3 dB respectively when the proportional gain was 2.14. Results were obtained for different proportional gain values of 1.75, 2.0 and 2.125 and these are given in Figs. 7.16, 7.17 and 7.18 respectively. These results show that by varying the proportional gain value the transient response to the step load change are also varied. The proportional gain value 2.125 is selected as this gave superior results. This digital control algorithm enables the output voltages to recover to within 1% of nominal in

10 ms under step load change and produces a sine waveform output very similar to that of the open-loop system. The digital regulator has output voltage regulation less than 1 percent. Three voltage harmonic spectra for line voltages using single-edge modulation with seven amperes resistive load, are shown in Fig. 7.19. The amplitudes of the second, fifth and seventh harmonics are -47.5 dB, -52.0 dB and -50.5 dB and all other individual harmonics are lower than -60.0 dB with respect to the 50 Hz fundamental as shown in Fig. 7.19 for phase AB. The other phases, BC and CA, have similar harmonic spectra. The harmonic spectra for double-edge modulation under similar load conditions are shown in Fig. 7.20. The amplitude of the fifth and seventh harmonics are -49.5 dB and -52.0 dB and all other individual harmonics are lower than -60.0 dB with respect to the 50 Hz fundamental and the other phases, BC and CA, have similar harmonic spectra. It can be seen from these figures that there are no third harmonics in the line voltage.

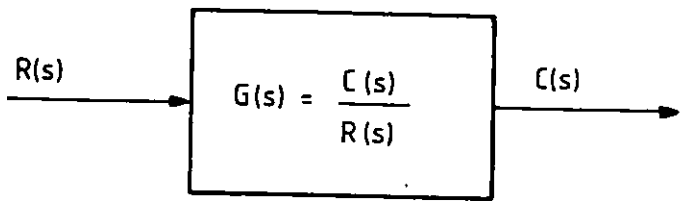


Fig. 7.1 Open-loop system.

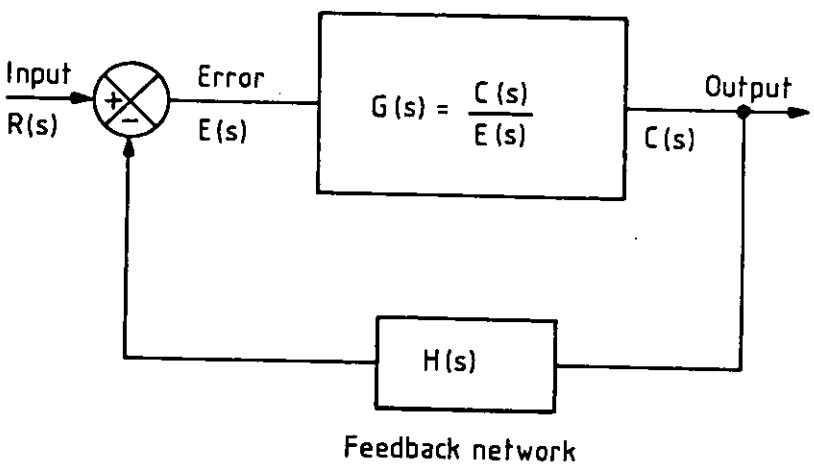


Fig. 7.2 Block diagram of closed-loop system.

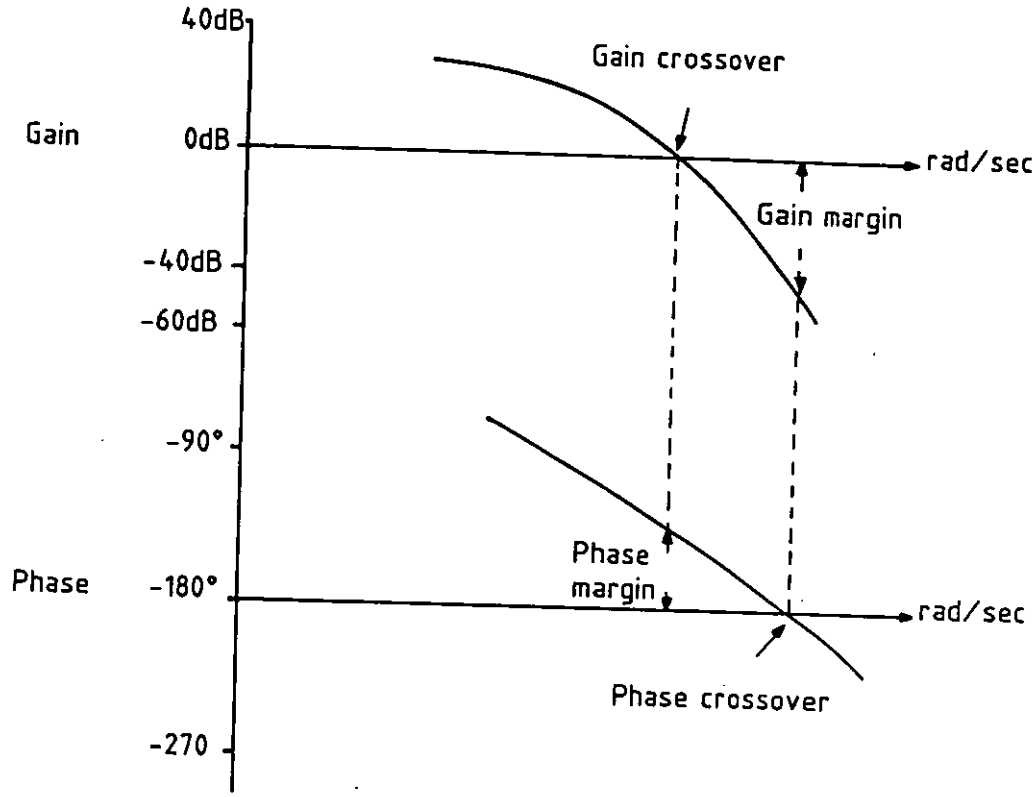


Fig. 7.3 Bode plot showing gain and phase margin.

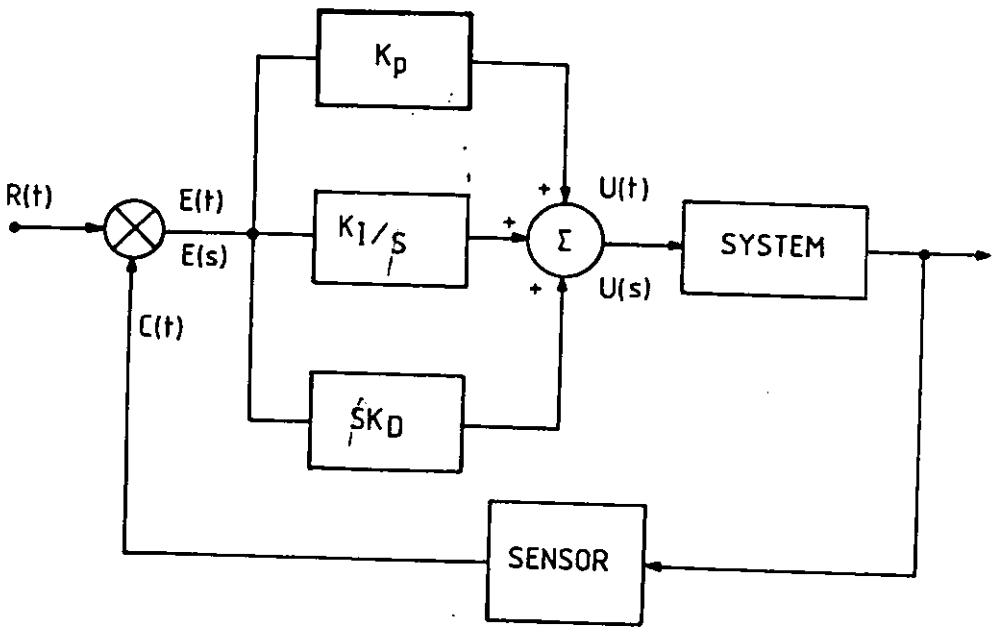


Fig 7.4 An analogue PID control system.

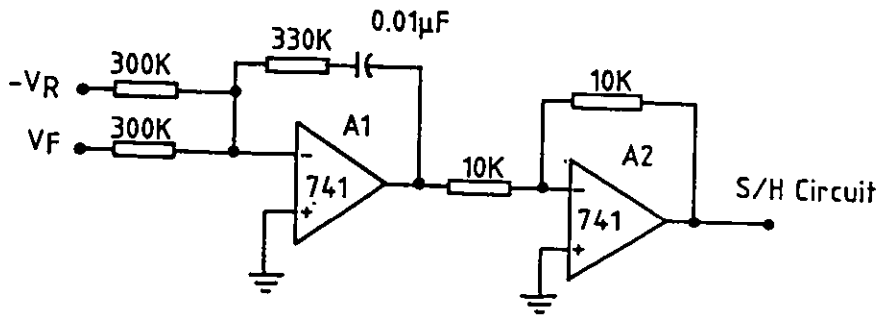


Fig. 7.5 Analogue PI controller.

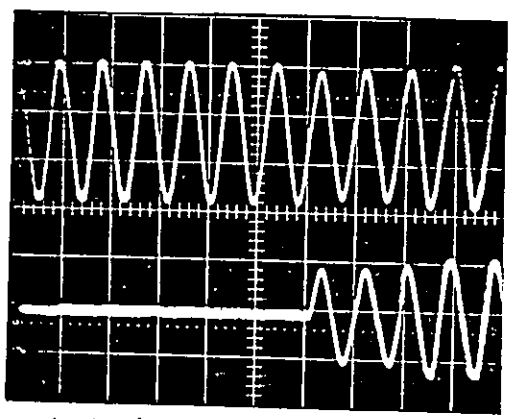


Fig. 7.6. Inverter output voltage and current waveform under step-load changes

Upper trace: 20V/DIV; 20ms/DIV
Lower trace: 10A/DIV

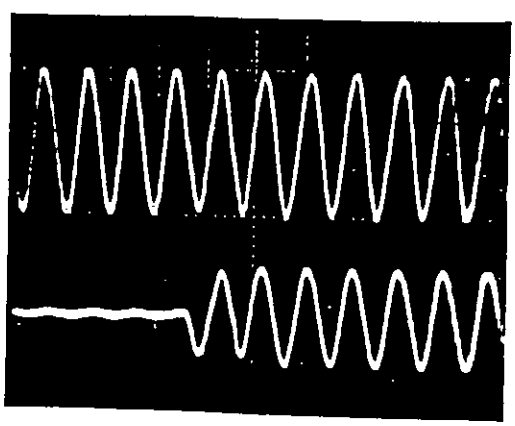


Fig. 7.7. Inverter output voltage and current waveform under step-load change

Upper trace: 20V/DIV; 20ms/DIV
Lower trace: 10A/DIV

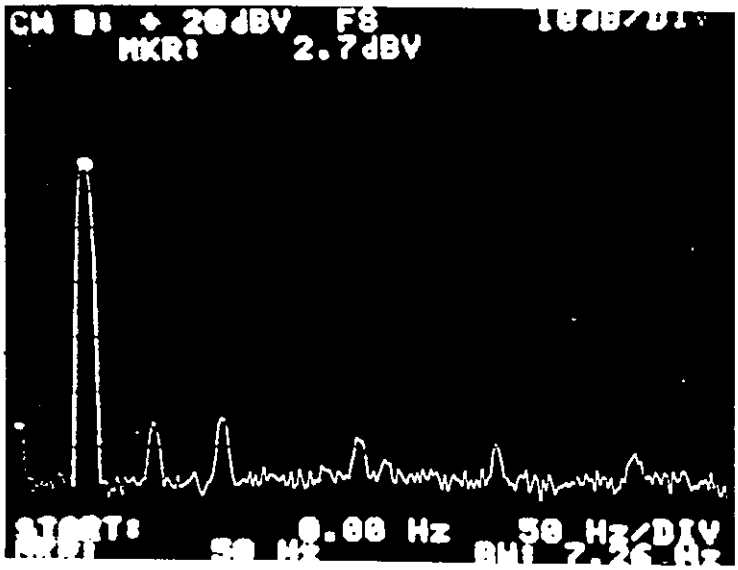


Fig. 7.8 Voltage harmonic spectrum with single-edge modulation

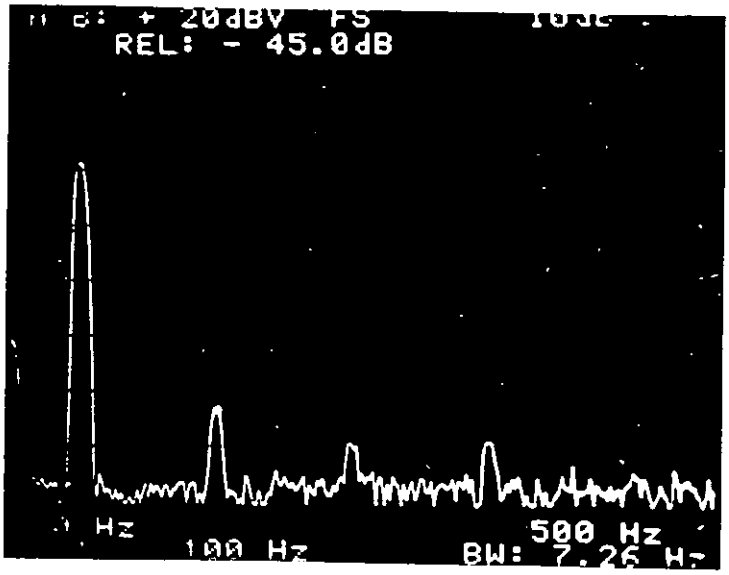


Fig. 7.9 Voltage harmonic spectrum with double-edge modulation

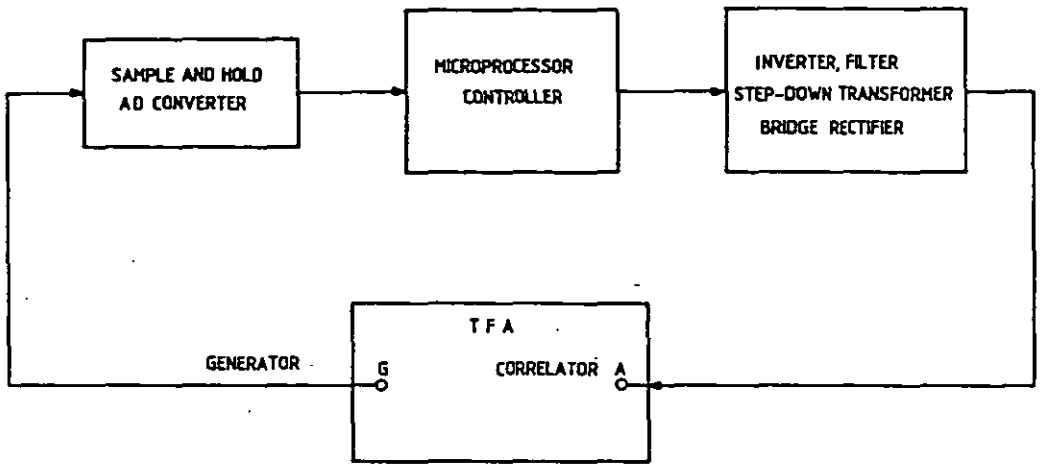


Fig. 7.10 Open-loop test configuration.

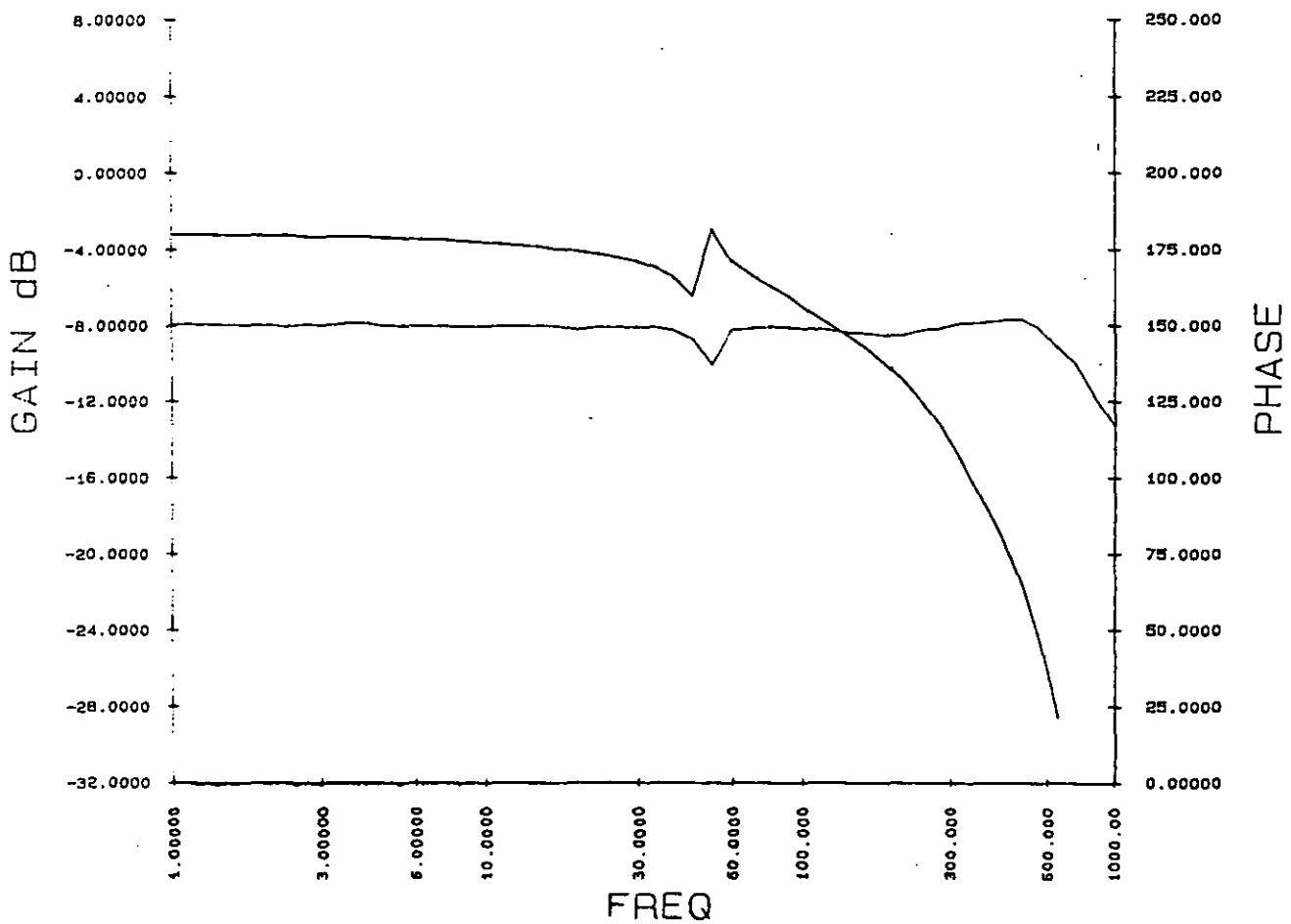


Fig. 7.11 Bode plot of the open loop system

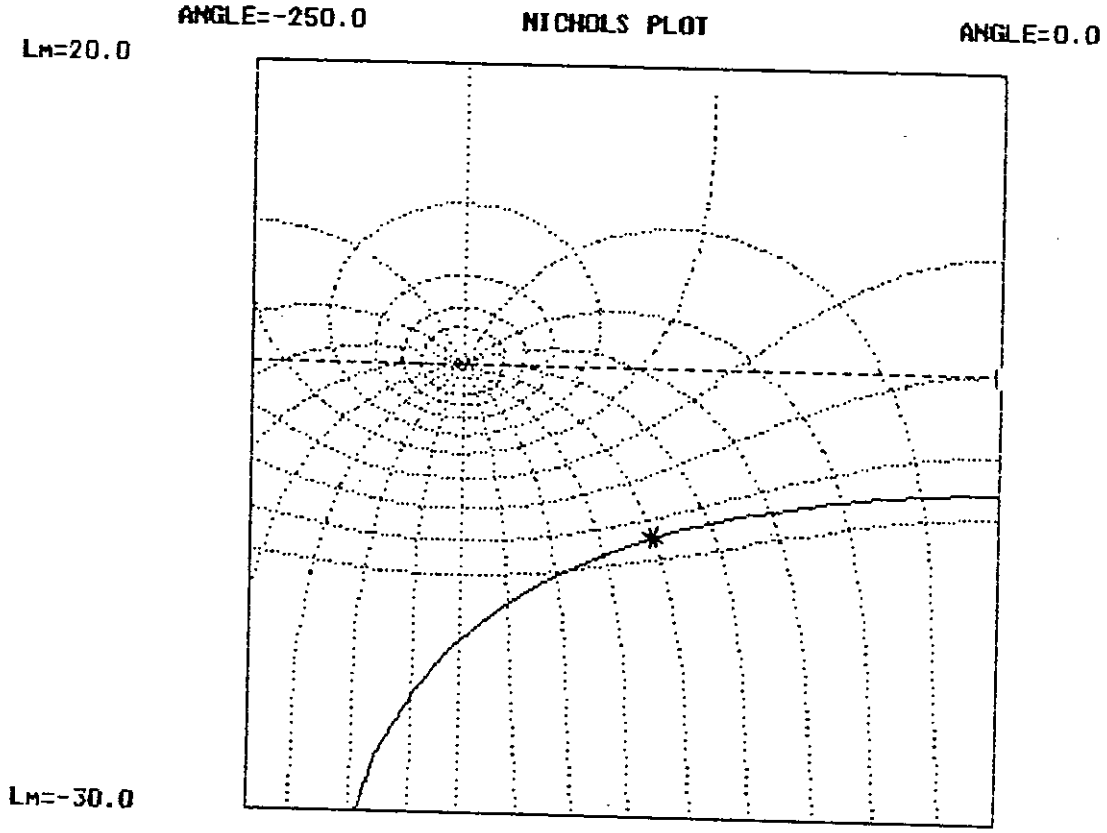


Fig.7.12 Nichols chart of the modelled system
* (935 rad/s, 116°, -11.33 dB)

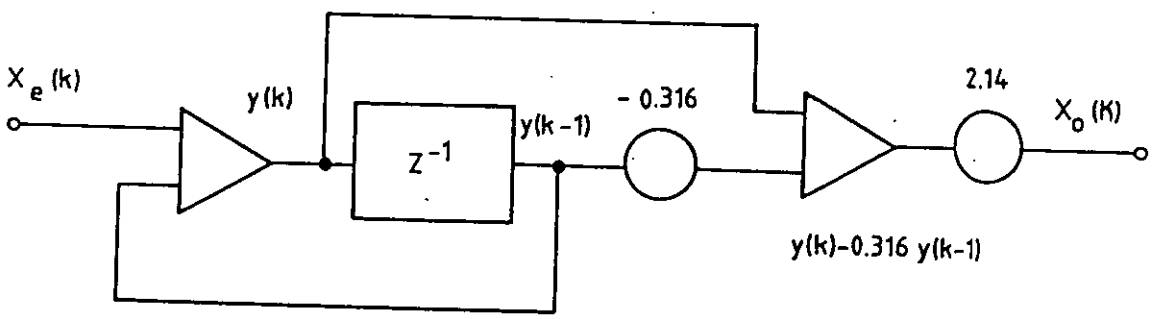


Fig. 7.13 Signal flow diagram of the digital control algorithm.

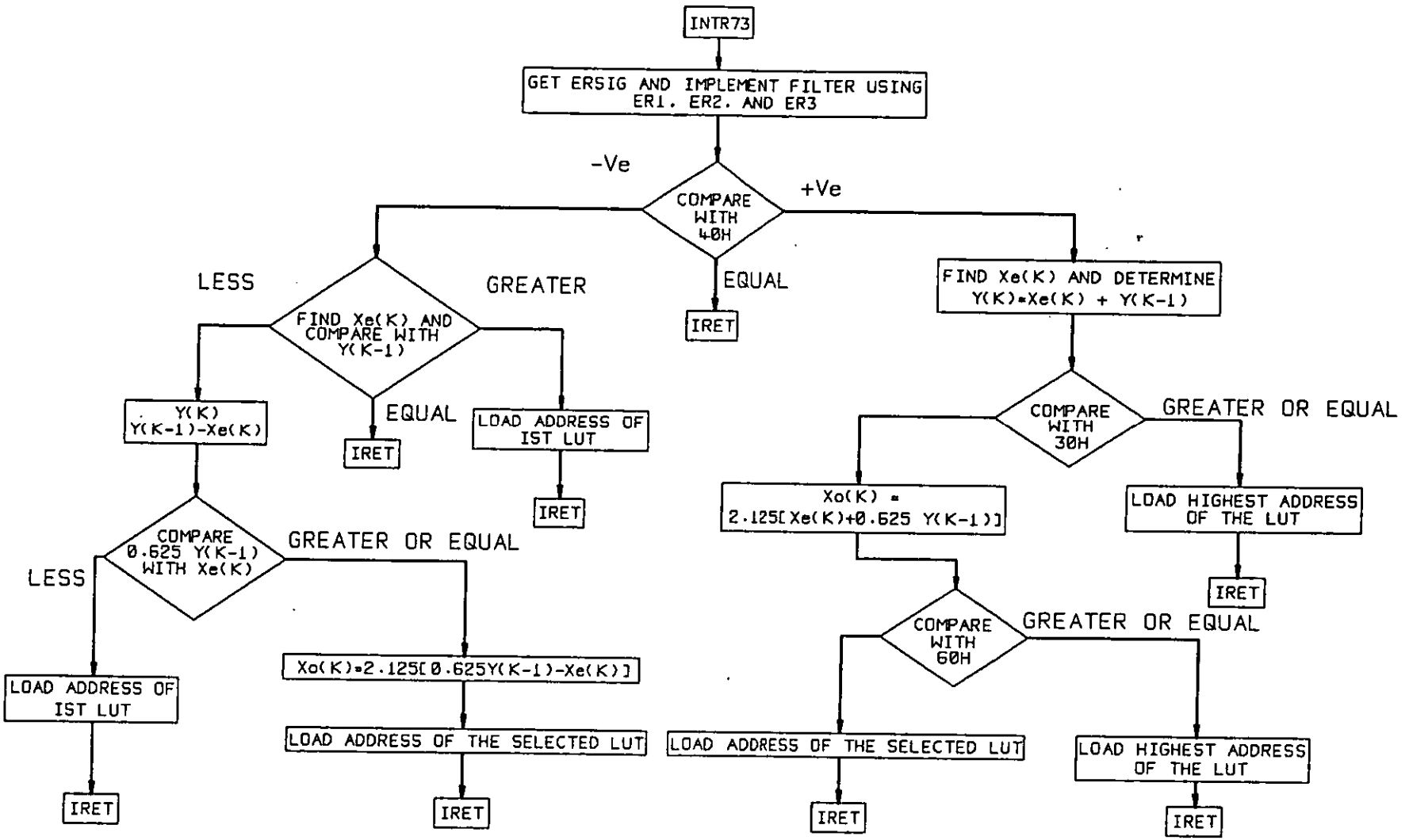


FIG. 7.14 Flow Chart Of The Digital Control Algorithm

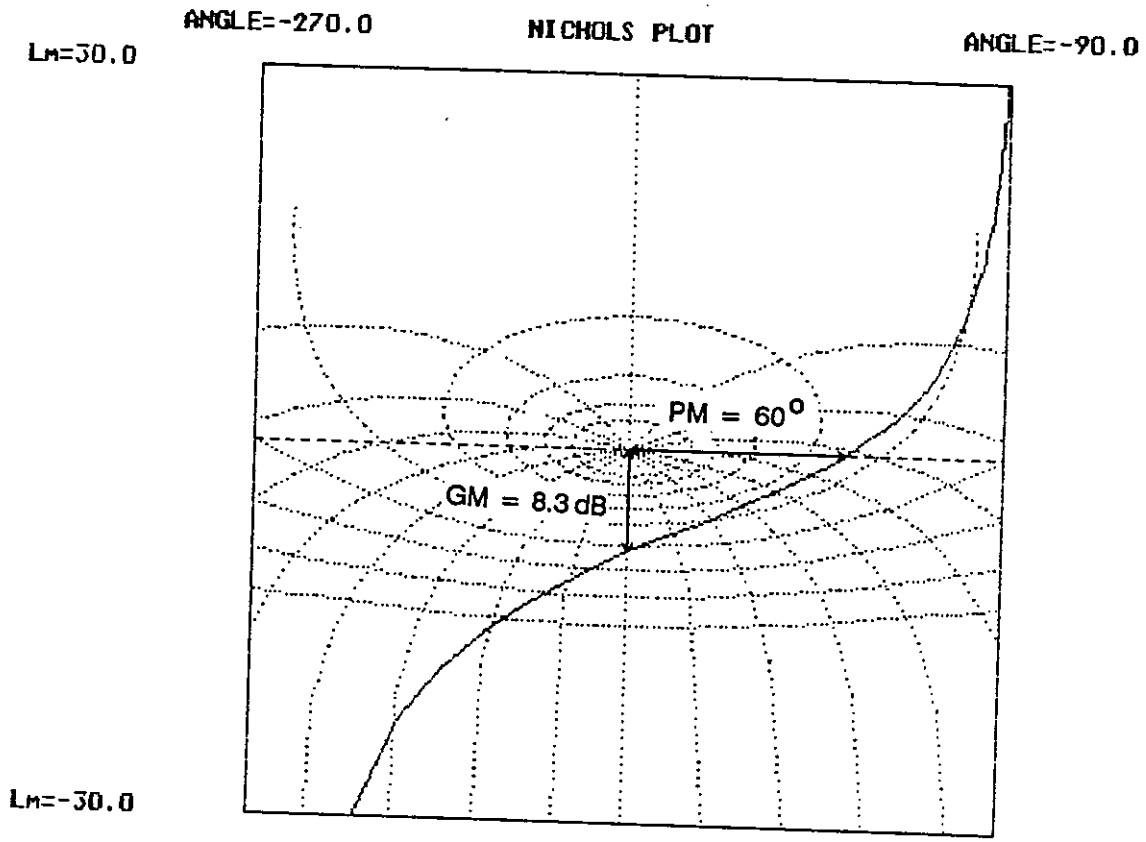


Fig. 7.15 Nichols chart of the compensated system
GM = 8.3 dB, PM = 60°

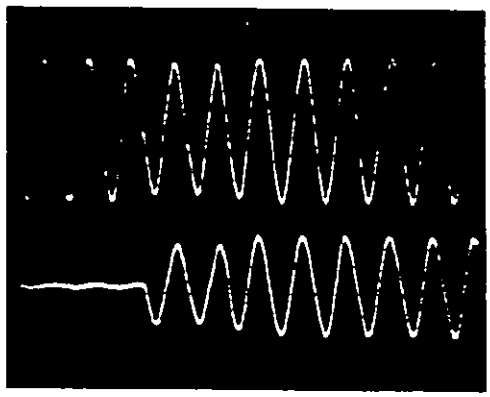


Fig.7.16. Inverter output voltage and current waveform under step-load change with proportional gain 1.75

Upper trace: 20V/DIV; 20ms/DIV
Lower trace: 10A/DIV

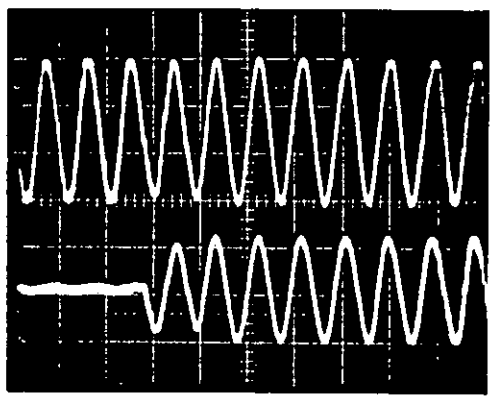


Fig.7.17. Inverter output voltage and current waveform under step-load change with proportional gain 2.0

Upper trace: 20V/DIV; 20ms/DIV
Lower trace: 10A/DIV

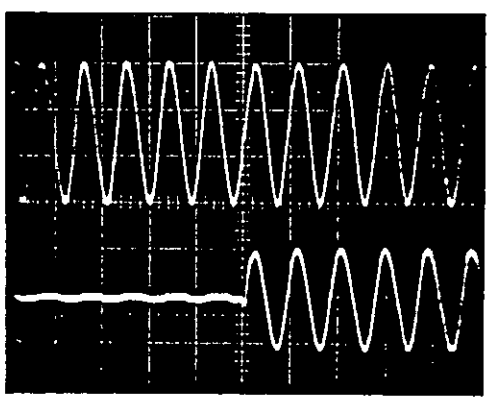
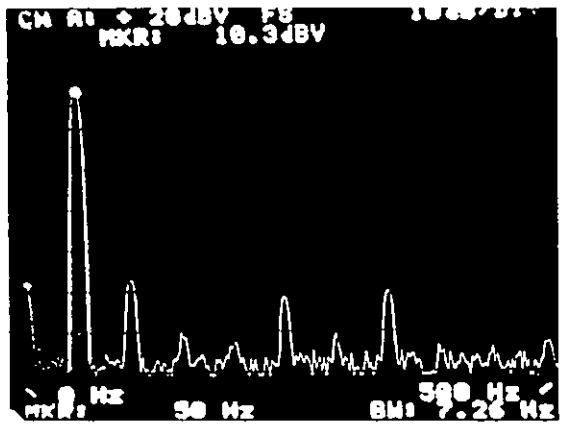


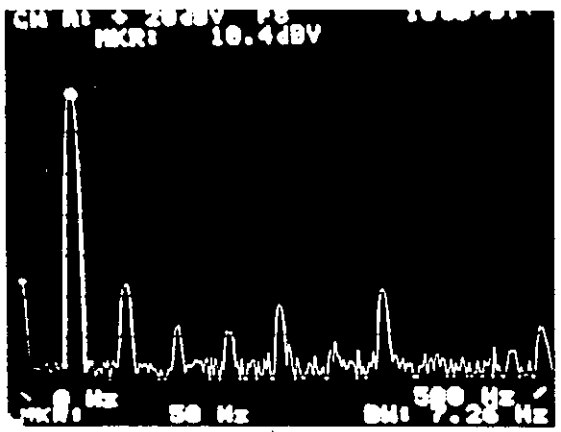
Fig.7.18. Inverter output voltage and current waveform under step-load change with proportional gain 2.125

Upper trace: 20V/DIV; 20ms/DIV
Lower trace: 10A/DIV

Phase AB



Phase BC



Phase CA

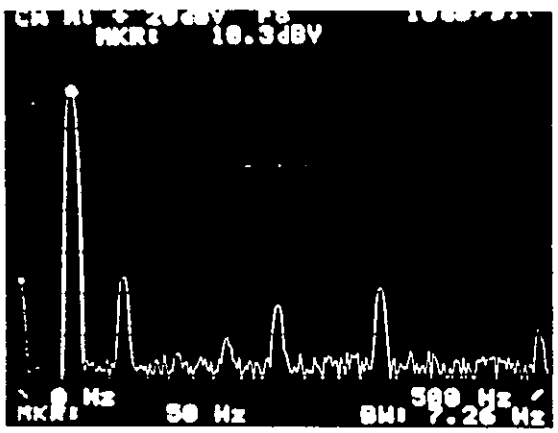
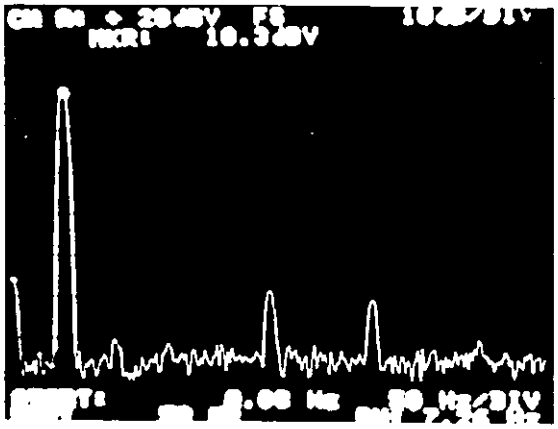
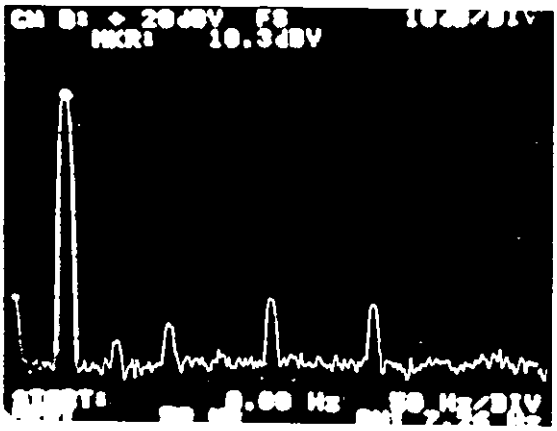


Fig. 7.19 Harmonic spectrum of line voltages with single-edge modulation

Phase $_{AB}$



Phase $_{BC}$



Phase $_{CA}$

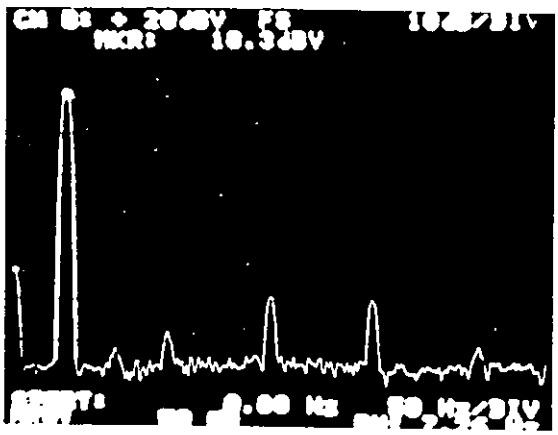


Fig. 7.20 Harmonic spectrum of line voltages with double-edge modulation

CHAPTER EIGHT

CONCLUSIONS AND SUGGESTIONS FOR FURTHER WORK

This chapter presents the conclusions arising from the results described in the previous chapters and gives suggestions for further research work.

8.1 CONCLUSIONS

The results obtained from the implementation of different methods for calculating the look-up-tables data suggest that it is advantageous to calculate the required data using the same system employed for software development purposes. This scheme overcomes the cumbersome and time consuming job of typing-in data.

Two equations, Eqns. 3.15 and 3.17,are derived to calculate the low level pulses for the double-edge and single-edge modulation processes respectively using the regular sampled symmetric strategy. Eqn. 3.15 requires less computation time as compared to other equations available to date in the literature for performing the same task, whereas Eqn. 3.17 does not need to be solved by the microprocessor, it being realised by the scheme used to generate the PWM pulses.

As described in Chapter Four, the interrupt driven software is utilised for the generation of the PWM pulses for single-phase as well as three-phase systems. The technique is based upon the use of Eqn. 3.15, and the real time reference waveform (carrier signal) enables the interrupt driven microprocessor controlled PWM generator to generate the PWM pulses independently of the time taken by the interrupt service routine and inherent interrupt delays, thereby producing distortionless output waveforms.

From the harmonic spectrums of the PWM generators discussed in Chapter Four, it can be concluded that the single-edge modulation process produces one additional harmonic component i.e. the second harmonic, and all other harmonics are almost as obtained from the double-edge modulation process. Since the amplitude of the second harmonic is very small, it can still be used in almost every application. In addition, single-edge modulation has the advantage of requiring less processing time and hardware components as compared to double-edge modulation.

Since the PWM generation technique effectively provides equal segmentation of the output waveform, the total number of segments in a cycle are equal to the ratio of the carrier frequency to the modulating frequency. By choosing this ratio equal to 360, it enabled the generation of the three-phase output waveforms with exact 120^{o} phase displacements by software techniques, and it also made possible to use only one interrupt for generating the three-phase PWM pulses.

Experimental results obtained from the three-phase systems confirm that if a single-phase carrier signal is utilised in generating the three-phase PWM pulses using the synchronous regular sampled strategy, it eliminates the need for the ratio of the carrier frequency to the modulating frequency to be odd.

In Chapter Five a PLL circuit is described which works in conjunction with the microprocessor. A phase difference measurement scheme is implemented which enables the phase difference to be measured directly in electrical degrees with the resolution of 0.1 degree. The PWM generation technique, together with the use of a higher carrier frequency of 18 kHz, provides a novel and efficient method of phase synchronisation with the mains for microprocessor controlled UPS inverters. Synchronisation is effectively achieved with a resolution of 0.5 degree. The decision to limit incrementing/decrementing the pointer to one was made in order to limit the amount of distortion introduced in the output waveform.

The results presented in Chapter Six show that the response of the voltage monitoring circuitry is instantaneous to the voltage deviations from the reference waveforms. Subsequent action to the voltage deviation can be delayed by introducing an inhibition period. To measure the frequency and to calculate the rate-of-change of frequency, period domain measurements are made which result in less computation requirements and faster response times.

Transient responses, with the analogue PI controllers, of single-phase and three-phase inverters were presented in Chapter Seven. The single-phase inverter recovered to nominal in less than three cycles whereas the three-phase inverter's recovery time was within a half cycle. The former is slower because it requires rather more filtering due to the presence of 100 Hz ripple in the rectified feedback voltage. Steady-state performance of the controller in both cases is similar, with output voltage regulation being less than one percent. The total harmonic distortion in the single-phase inverter output voltage waveform is less than

3% with the largest single harmonic component being the third, approximately 0.56%. This is well below the generally accepted specification of 5% total harmonic distortion, with the largest single harmonic component less than 3%.

The experimental approach used to model the transfer function, together with the designing of the digital PI controller in the w-plane proved very effective and accurate, and provides precise design parameters of the controller. It has also been shown that a relatively long sampling rate could be used if the designing technique is purely digital. The results and discussion presented in Chapter Seven show that the digital PI controller has similar steady-state characteristics as its counter part analogue controller. Output voltage regulation is less than one percent and total harmonic distortion is also less than one percent. The results prove that an efficient digital PI controller can be implemented for this application by using an 8-bit microprocessor.

The use of power MOSFETs and their simple drive circuitry in the UPS inverters allow these to be designed using high frequency carrier signals, resulting in high quality output voltage waveforms. The use of an 18 kHz switching frequency provides the means of simplifying the design of the microprocessor controlled PWM generators, and allows the use of simple low pass output filters.

The control functions required by the UPS inverter: the generation of the PWM pulses, the digital PI control algorithm, the phase synchronisation,the frequency measurement and computation of the rate-of-change of frequency, are performed directly by the microprocessor.The microprocessor, however, only performs a supervisory role in the PLL circuit and the voltage monitoring circuitry. Since one microprocessor performs almost all the required control functions, a single integrated circuit could be realised that would result in enhanced reliability.

8.2 SUGGESTIONS FOR FURTHER RESEARCH WORK

1. The digital PI controller presented in this report works well only under balanced load conditions. When the output load becomes unbalanced, this will introduce distortion and produce unbalanced output voltages. To reduce the distortion in the three-phase output voltage when operating with unbalanced loads, the range of the digital averaging filter should be increased to nine samples with increased word length.

2. Design a regulator which uses a separate sine reference waveform for each phase separately and employing instantaneous feedback of the output waveform to determine the error signal. This will provide instant control over output voltage waveform, thus enabling unbalanced and nonlinear loads to be properly dealt with.

3. To eliminate the requirement of the 50 Hz output transformer, the power circuit configuration, with the switching waveforms shown in Fig. 8.1, may be used. The control circuit used to generate single-edge modulated PWM pulses shown in Fig. 4.1 can be utilised to generate the switching waveforms illustrated in Fig. 8.1. To enable such a system to handle nonlinear loads with minimum distortion, the regulator described above may be used.

4. The performance of the HEXFET III generation devices in the inverter circuit without the support of the series blocking and antiparallel diodes, should be thoroughly investigated. Comparison should then be made with other MOSFETs of the same ratings but with the inclusion of the diodes, calculating the losses in the power circuit in both cases.

5. Determine the optimised switching angles to eliminate the undesired harmonics in the output waveform in reference to the high frequency (i.e. 18 kHz) carrier signal such that the resultant optimised PWM waveform should have a switching frequency around 2 kHz. This optimised switching waveform can be generated in relation to the 18 kHz signal without any shifts in switching angles. Such a system can then be used for UPS systems of large output power ratings which, of necessity, switch at lower frequencies ($\approx$ 2 kHz) since they employ the larger slower power semiconductor switches such as bipolar transistors, GTOs or thyristors.

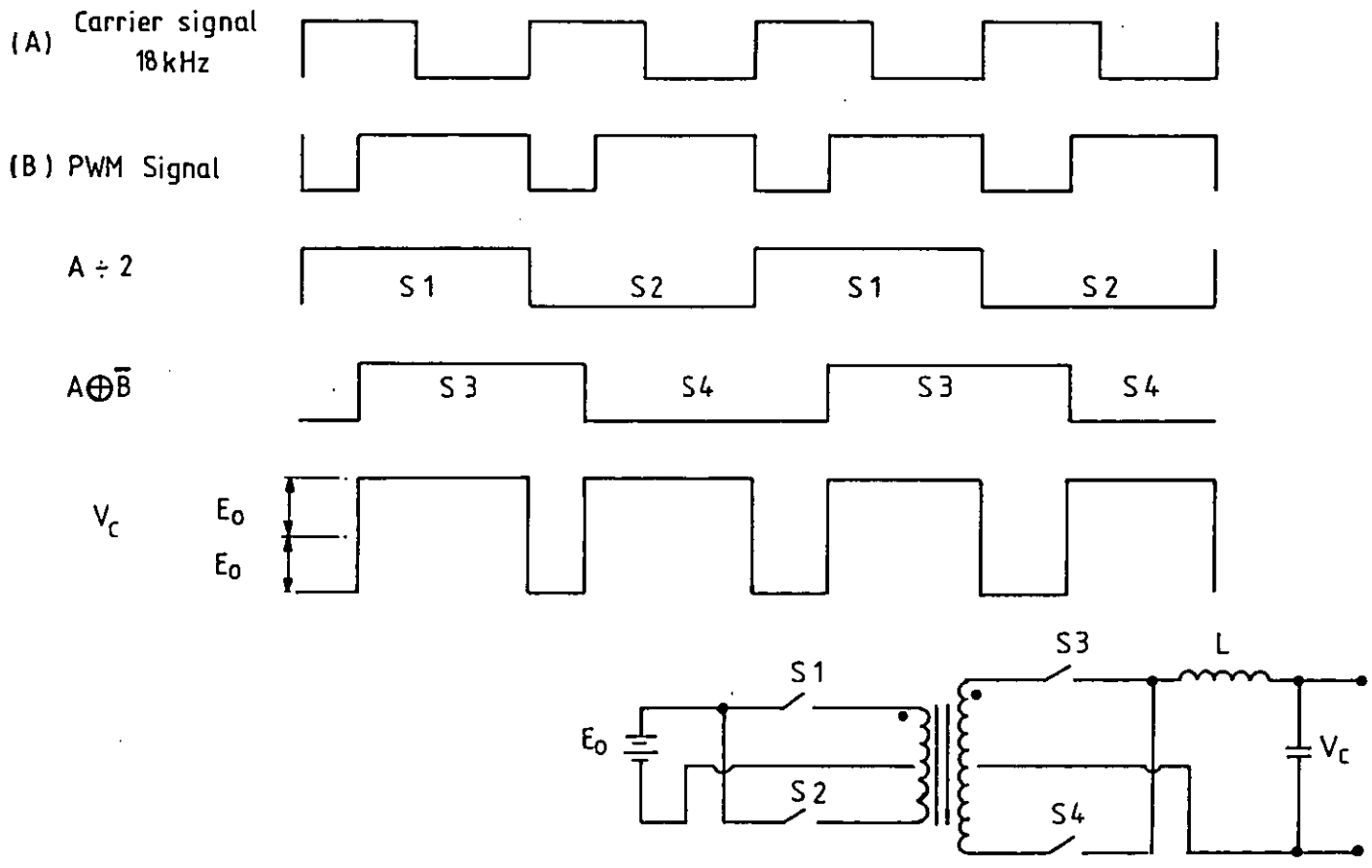


Fig 8.1 Inverter with its switching waveforms.

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APPENDIX I

LISTING OF PROG1.SRC AND DEVELOPMENT PROCEDURE

```
PROGRAM PWM2(OUTPUT);
(*THIS PROGRAM CALCULATES THE HIGHLEVEL PULSES*)
(* USING THAJ=Tc/2+Tc/2*MSINWmT1*)
(*USING MODULATION INDEX 0.75 TO 0.97*)
(* WITH STEP OF 0.005*)
(*WHERE T IS TIME PERIOD OF CARIER FREQ. 18KHZ)*)
(*T1 IS THE SAMPLING INSTANT*)
(*TO GET PULSE WIDTH IN INTEGER,ITNJ ABOVE Eqn.*)
(* IS MULTIPLIED WITH COUNTER'S*)
(*CLOCKING FREQUENCY,Fck*)
(* TPJ*Fck =Fck(Tc/2+Tc/2*M*SIN(Wm*(4*J+1)))*)
(* ITNJ=P1+P2*SINP4*(4*J+1)*)
(*WHERE P1=Tc/2*Fck=55.55555E-6/2*3.59660E6=110.01655*)
(*P2=P1*M=110.01655/200=0.5550823E*)
(*P4=Pi/720=0.004363323*)
CONST
P1=111.01655;
P3=0.5550823;
P4=0.004363323;

VAR
Y:REAL;
TP: TEXT;
R,I,M,J:INTEGER;
LTP:TEMPREAL;
BEGIN
   REWRITE(TP,'PS:TABLE1');
   WRITELN(TP,'NAME LOOOKUPTABLES');
   WRITELN(TP,'CODE SEGMENT BYTE PUBLIC  CODE');
   WRITELN(TP,'PUBLIC I50,I100');
   I:=150;
   FOR  M:=0 TO 46 DO
   BEGIN
      WRITE(TP,'I',I-100);
      FOR J:=0 TO 90 DO
      BEGIN
         Y:=(P4*4*J+P4);
         LTP:=(P1+P3*I*SIN(Y));
         WRITELN(TP,' DB ',LTRUNC(LTP));
      END;
(* WRITELN( 'I',I);*)
      I:=I+1;
   END;
```

```
WRITE(TP,'RAMADDR');
R:=405H;
WRITELN(TP,' DW ',R);
FOR M:=0 TO 48 DO
BEGIN
R:=R+256H;
WRITELN(TP,' DW ',R);
END
;
WRITELN(TP,'CODE ENDS');
WRITELN(TP,'END');
END .


RUN PASC86 :F9:PROG1.SRC

RUN  LINK86 :F9:PROG1.OBJ,P86RN0.LIB,P86RN1.LIB,&
P86RN2.LIB,P86RN3.LIB,CEL87.LIB,EH87.LIB,&
E8087.LIB,E8087,LARGE.LIB TO :F9:PROG1.86 BIND

RUN :F9:PROG1.86
```

APPENDIX II

LOOK-UP-TABLES

```
NAME LOOOKUPTABLES
CODE SEGMENT BYTE PUBLIC 'CODE'
PUBLIC I50,I51,I52,I53,I54,I55,I56,I57,I58,I59
PUBLIC I60,I61,I62,I63,I64,I65,I66,I67,I68,I69
PUBLIC I70,I71,I72,I73,I74,I75,I76,I77,I78,I79
PUBLIC I80,I81,I82,I83,I84,I85,I86,I87,I88,I89
PUBLIC I90,I91,I92,I93,I94,I95,I96
PUBLIC RAMADDR
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CODE ENDS
END
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APPENDIX III

LISTING OF OMAAD.SRC AND DEVELOPMENT PROCEDURE

```
NAME CONTROLLER

EXTRA SEGMENT;AT 0H*****
ORG 120H
TP72IP DW INTR72;IR0
TP72CS DW ?
TP73IP DW INTR73;IR1
TP73CS DW ?
TP74IP DW INTR74;IR2
TP74CS DW ?
TP75IP DW INTR75;IR3
TP75CS DW ?
TP76IP DW INTR76;IR4
TP76CS DW ?
TP77IP DW INTR77;IR5
TP77CS DW ?
TP78IP DW INTR78;IR6
TP78CS DW ?
TP79IP DW INTR79;IR7
TP79CS DW ?

EXTRA ENDS;**************
DATA  SEGMENT ;AT 0000H
ORG  400H
ER1 DB (0)
ER2 DB (0)
ER3 DB (0)
;LOOK-UP-TABLES
ORG 405H
T50   DB 258H DUP (0)
ORG 65DH
T51    DB 258H DUP (0)
ORG 885H
T52   DB 258H DUP (0)
ORG 0A0DH
T53 DB 258H DUP (0)
ORG 0D65H
T54 DB 258H DUP (0)
ORG 0FBDH
T55 DB 258H DUP (0)
ORG 1215H
T56 DB 258H DUP (0)
ORG 146DH
T57 DB 258H DUP (0)
ORG 16C5H
T58 DB 258H DUP (0)
ORG 191DH
T59 DB 258H DUP (0)
ORG 1B75H
T60 DB 258H DUP (0)
ORG 1DCDH
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T61 DB 258H DUP (0)
ORG 2025H
T62 DB 258H DUP (0)
ORG 227DH
T63 DB 258H DUP (0)
ORG 24D5H
T64 DB 258H DUP (0)
ORG 272DH
T65 DB 258H DUP (0)
ORG 2985H
T66 DB 258H DUP (0)
ORG 2BDDH
T67 DB 258H DUP (0)
ORG 2E35H
T68 DB 258H DUP (0)
ORG 308DH
T69 DB 258H DUP (0)
ORG 32E5H
T70 DB 258H DUP (0)
ORG 353DH
T71 DB 258H DUP (0)
ORG 3795H
T72 DB 258H DUP (0)
ORG 39EDH
T73 DB 258H DUP (0)
ORG 3C45H
T74 DB 258H DUP (0)
ORG 3E9DH
T75 DB 258H DUP (0)
ORG 40F5H
T76 DB 258H DUP (0)
ORG 434DH
T77 DB 258 DUP (0)
ORG 45A5H
T78 DB 258H DUP (0)
ORG 47FDH
T79 DB 258H DUP (0)
ORG 4A55H
T80 DB 258H DUP (0)
ORG 4CADH
T81 DB 258H DUP (0)
ORG 4F05H
T82 DB 258H DUP (0)
ORG 515DH
T83 DB 258H DUP (0)
ORG 5385H
T84 DB 258H DUP (0)
ORG 560DH
T85 DB 258H DUP (0)
ORG 5865H
T86 DB 258H DUP (0)
ORG 5ABDH
T87 DB 258H DUP (0)
ORG 5D15H
T88 DB 258H DUP (0)
ORG 5F6DH
T89 DB 258H DUP (0)
ORG 61C5H
T90 DB 258H DUP (0)
```

```
ORG 641DH
T91 DB 258H DUP (0)
ORG 6675H
T92 DB 256H DUP (0)
ORG 68CDH
T93 DB 256H DUP (0)
ORG 6825H
T94 DB 258H DUP (0)
ORG 6D7DH
T95 DB 258H DUP (0)
ORG 6FD5H
T96 DB 258H DUP (0);722DH

;OTHER DATA
MAINAVL DB (0)
COUNT1  DW (0)
COUNT2  DW (0)
TMP0     DW  (0)
TMP1     DW  (0)
TMP2     DW  (0)
TMP3     DW  (0)
TMP4     DW  (0)
TMP5     DW  (0)
TMP6     DW  (0)
TMP7     DW  (0)
TMP8     DW  (0)
TMP9     DW  (0)
TMP10     DW  (0)
TMP11     DW  (0)
TMP12     DW  (0)
TMP13     DW  (0)
TMP14     DW  (0)
TMP15     DW  (0)
TMP16     DW  (0)
TMP17     DW  (0)
TMP18     DW  (0)
TMP19     DW  (0)
TMP20     DW  (0)
TMP21     DW  (0)
TMP22     DW  (0)
TMP23     DW  (0)
TMP24     DW  (0)
TMP25     DW  (0)

DATA  ENDS
```

```
STACK SEGMENT ;AT 7A0H*****

     DW  OFFH DUP (?)

     TOP_STACK  LABEL WORD
STACK ENDS
;*************************
CODE SEGMENT  BYTE PUBLIC 'CODE'
ASSUME CS:CODE,ES:EXTRA,DS:DATA,SS:STACK
EXTRN I50:BYTE,I51:BYTE,I52:BYTE,I53:BYTE,I54:BYTE,I55:BYTE,I56:BYT
EXTRN I57:BYTE,I58:BYTE,I59:BYTE,I60:BYTE,I61:BYTE,I62:BYTE,I63:BYT
EXTRN I64:BYTE,I65:BYTE,I66:BYTE,I67:BYTE,I68:BYTE,I69:BYTE,I70:BYT
EXTRN I71:BYTE,I72:BYTE,I73:BYTE,I74:BYTE,I75:BYTE,I76:BYTE,I77:BYT
EXTRN I78:BYTE,I79:BYTE,I80:BYTE,I81:BYTE,I82:BYTE,I83:BYTE,I84:BYT
EXTRN I85:BYTE,I86:BYTE,I87:BYTE,I88:BYTE,I89:BYTE,I90:BYTE,I91:BYT
EXTRN I92:BYTE,I93:BYTE,I94:BYTE,I95:BYTE,I96:BYTE
EXTRN RAMADDR:WORD
PUBLIC UTART

CICW   EQU 06H; A1=0 ADDR FOR ICW1
COCW   EQU 0AH; A1=1 ADD FOR ICW2,OCWS

;****PIT**8254-2****

CTA   EQU  016H; A0,A1=1, FOR CW
CWTA0 EQU  016H; MOD 3 SQ.WAVE
CWTA1 EQU  056H; MOD 3, SQ. WAVE
CWTA2 EQU  092H; MOD=1,MONO-SHOT
CTA0  EQU  010H; COUNT ADDR
CTA1  EQU  012H; COUNT ADDR
CTA2  EQU  014H; COUNT ADDR

;*****PPI***82C55A***

CPI   EQU  033H;ADDR FOR CW
CWP   EQU   80H;
PORTA EQU 030H;O/P PORTA
PORTB EQU 031H;I/P PORTB
PORTC EQU 032H;O/P PORTC

;<<<<<PWM><COUNTER B><82C54A

CTB  EQU 026H;MONO-SHOT
CWB0 EQU 012H;MOD-1
CWB1 EQU 052H;MOD-1
CWB2 EQU 092H;MOD-1
CTB0 EQU 020H
CTB1 EQU 022H
CTB2 EQU 024H

;****PIT**8254-2****
CTC   EQU  063H; A0,A1=1, FOR CW
CWC0  EQU   36H; MOD3 SQ.WAVE
CWC1  EQU   52H; MOD3 SQ.WAVE 50Hz Ref.
CWC2  EQU  080H; MOD=1
CTC0  EQU  060H; COUNT ADDR
CTC1  EQU  061H; COUNT ADDR
CTC2  EQU  062H; COUNT ADDR
```

```
;****PIT**8254-2****
CTD    EQU  073H; A0,A1=1, FOR CW
CWD0   EQU   32H; MOD1 MONO-SHOT 20.4ms
CWD1   EQU   70H; MOD0 Phase Difference
CWD2   EQU   90H; MOD0
CTD0   EQU  070H; COUNT ADDR
CTD1   EQU  071H; COUNT ADDR
CTD2   EQU  072H; COUNT ADDR
;****PIT**8254-2***
CTE    EQU  043H; A0,A1=1, FOR CW
CWE0   EQU  030H; MOD0
CWE1   EQU  070H; MOD0
CWE2   EQU  096H; MOD=1
CTE0   EQU  040H; COUNT  ADDR
CTE1   EQU  041H; COUNT  ADDR
CTE2   EQU  042H; COUNT  ADDR

;   SAMPLING EPROM

ERSIG EQU 040

UTART:CLI
      MOV AX,EXTRA;
      MOV ES,AX ;
      MOV AX,DATA
      MOV DS,AX
          MOV AX,STACK;STACK 7A00H
          MOV SS,AX
      MOV SP,OFFSET TOP_STACK;7FF0H

;LOAD INTERRUPT  VECTOR

TYPES:MOV  AX,OFFSET INTR72;LOAD TYPE 72
      MOV  ES:TP72IP,AX
      MOV  ES:TP72CS,CS
      MOV  AX,OFFSET INTR73
      MOV ES:TP73IP,AX
      MOV ES:TP73CS,CS
      MOV AX,OFFSET INTR74
      MOV ES:TP74IP,AX
      MOV ES:TP74CS,CS
      MOV AX,OFFSET INTR75
      MOV ES:TP75IP,AX
      MOV ES:TP75CS,CS
      MOV AX,OFFSET INTR76
      MOV ES:TP76IP,AX
      MOV ES:TP76CS,CS
      MOV AX,OFFSET INTR77
      MOV ES:TP77IP,AX
      MOV ES:TP77CS,CS
      MOV AX,OFFSET INTR78
      MOV ES:TP78IP,AX
      MOV ES:TP78CS,CS
      MOV AX,OFFSET INTR79
      MOV ES:TP79IP,AX
      MOV ES:TP79CS,CS
```

```
;<<<<<<<<<<<<<<82C59A_2>>>>>>>>>>>>>
SET59:MOV AL,13H;EDGE  ICW1,1BHLEVEL
          OUT CICW,AL;  AD1=0
          MOV AL,48H; INTR72 ICW2
          OUT COCW,AL;  AD1=1
          MOV AL,07H;NORMAL_EOI_FNM ICW4
          OUT COCW,AL; AD1=1
      MOV AL,0FCH;IR0,1 ENABLED
          OUT COCW,AL;   AD1=1

;<<<<<<INTIALIZE><82C54-2>>>>

SETCTA:MOV   AL,CWTA0; MOD=3 *PI*CONTR*<CTA0>*
       OUT  CTA,AL  ;
       MOV   AL,014H;DIVIDES CARRIERFREQUENCY
       OUT  CTA0,AL
       MOV AL,CWTA1;Carrier 18KHz
           OUT CTA ,AL
           MOV AX,0DEH;0E0H
           OUT CTA1,AL
           MOV AL,CWTA2
           OUT CTA,AL
           MOV  AL,036H
           OUT CTA2,AL

;>>>>>>INTIALIZE><PWM><COUNTER B 82C54
         MOV AL,CWB0;CW FOR CNTB0
         OUT CTB,AL
         MOV AL,55H
         OUT CTB0,AL
         MOV AL,CWB1;CW FOR CNTB1
         OUT CTB,AL
         MOV AL,0AAH;
         OUT CTB1,AL
         MOV AL,CWB2;CW FOR CNTB2
         OUT CTB,AL
         MOV AL,4CH
         OUT CTB2,AL
;>>>>>>INTIALIZE><><COUNTER C 8254
         MOV AL,CWC0;PLL Loop-Counter
         OUT CTC,AL
         MOV AL,18H
         OUT CTC0,AL
         MOV AL,9CH
         OUT CTC0,AL
         MOV AL,CWC1;50Hz Ref erence
         OUT CTC,AL
         MOV AL,3CH
         OUT CTC1,AL
         MOV AL,9CH
         OUT CTC1,AL
         MOV AL,CWC2; Mains Frequency
         OUT CTC,AL
         MOV AL,00H
         OUT CTB2,AL
         MOV AL,0FAH
                 OUT CTC2,AL
```

```
;>>>>>>INTIALIZE><><COUNTER D 8254
        MOV AL,CWD0;MONO-SHOT 20.4ms to detect Sync
        OUT CTD,AL
        MOV AL,58H
        OUT CTD0,AL
        MOV AL,9FH
        OUT CTD0,AL
            MOV AL,CWD1;To Measure Phase DiFFerence
            OUT CTD,AL
            MOV AL,68H;1388H
            OUT CTD1,AL
            MOV AL,13H
            OUT CTD1,AL
            MOV AL,CWD2;To Generate Pulse for SPS
            OUT CTD,AL
            MOV AL,20H
            OUT CTD2,AL
;>>>>>>INTIALIZE><><COUNTER E 8254
            MOV AL,CWE0  ;For Inverter Frequency
            OUT CTE,AL
            MOV AL,00H
            OUT CTE0,AL
            MOV AL,0FAH
            OUT CTE0,AL
            MOV AL,CWE1 ;For Voltase Disturbances Measurement
            OUT CTE,AL
            MOV AL,00H
            OUT CTE1,AL
            MOV AL,0FAH
            OUT CTE1,AL
            MOV AL,CWE2  ;To Generate 160 kHz
            OUT CTE,AL
            MOV AL,16H
            OUT CTE2,AL
;********INTIALIZE  82C55

SET55:MOV AL,CWP;PORTA O/P  PORTB & PORTC I/P
      OUT CPI,AL

;*****ESTABLISH THE DATA SEGMENT
    MOV SI,0H
    MOV DI,0H
    LEA BP,CS:I50
        LEA BX,T50
    CALL HELP
        LEA BP,CS:I51
        LEA BX,T51
        CALL HELP
        LEA BP,CS:I52
        LEA BX,T52
        CALL HELP
        LEA BP,CS:I53
        LEA BX,T53
        CALL HELP
        LEA BP,CS:I54
        LEA BX,T54
        CALL HELP
        LEA BP,CS:I55
```

```
        LEA BX,T55
        CALL HELP
        LEA BP,CS:I56
        LEA BX,T56
        CALL HELP
        LEA BP,CS:I57
        LEA BX,T57
        CALL HELP
        LEA BP,CS:I58
        LEA BX,T58
        CALL HELP
        LEA BP,CS:I59
        LEA BX,T59
        CALL HELP
    LEA BP,CS:I60
        LEA BX,T60
        CALL HELP
        LEA BP,CS:I61
        LEA BX,T61
        CALL HELP
        LEA BP,CS:I62
        LEA BX,T62
        CALL HELP
        LEA BP,CS:I63
        LEA BX,T63
        CALL HELP
        LEA BP,CS:I64
        LEA BX,T64
        CALL HELP
        LEA BP,CS:I65
        LEA BX,T65
        CALL HELP
        LEA BP,CS:I66
        LEA BX,T66
        CALL HELP
        LEA BP,CS:I67
        LEA BX,T67
        CALL HELP
        LEA BP,CS:I68
        LEA BX,T68
        CALL HELP
        LEA BP,CS:I69
        LEA BX,T69
        CALL HELP
    LEA BP,CS:I70
        LEA BX,T70
        CALL HELP
        LEA BP,CS:I71
        LEA BX,T71
        CALL HELP
        LEA BP,CS:I72
        LEA BX,T72
        CALL HELP
        LEA BP,CS:I73
        LEA BX,T73
        CALL HELP
        LEA BP,CS:I74
        LEA BX,T74
        CALL HELP
```

```
        LEA BP,CS:I75
        LEA BX,T75
        CALL HELP
        LEA BP,CS:I76
        LEA BX,T76
        CALL HELP
        LEA BP,CS:I77
        LEA BX,T77
        CALL HELP
        LEA BP,CS:I78
        LEA BX,T78
        CALL HELP
        LEA BP,CS:I79
        LEA BX,T79
        CALL HELP
LEA BP,CS:I80
        LEA BX,T80
        CALL HELP
        LEA BP,CS:I81
        LEA BX,T81
        CALL HELP
        LEA BP,CS:I82
        LEA BX,T82
        CALL HELP
        LEA BP,CS:I83
        LEA BX,T83
        CALL HELP
        LEA BP,CS:I84
        LEA BX,T84
        CALL HELP
        LEA BP,CS:I85
        LEA BX,T85
        CALL HELP
        LEA BP,CS:I86
        LEA BX,T86
        CALL HELP
        LEA BP,CS:I87
        LEA BX,T87
        CALL HELP
        LEA BP,CS:I88
        LEA BX,T88
        CALL HELP
        LEA BP,CS:I89
        LEA BX,T89
        CALL HELP
LEA BP,CS:I90
        LEA BX,T90
        CALL HELP
        LEA BP,CS:I91
        LEA BX,T91
        CALL HELP
        LEA BP,CS:I92
        LEA BX,T92
        CALL HELP
        LEA BP,CS:I93
        LEA BX,T93
        CALL HELP
        LEA BP,CS:I94
        LEA BX,T94
```

```
          CALL HELP
          LEA BP,CS:I95
          LEA BX,T95
          CALL HELP
          LEA BP,CS:I96
          LEA BX,T96
          CALL HELP


    MOV AX,0H
    MOV DI,AX
    MOV SI,AX
    MOV BX,AX
    MOV DX,AX

     LEA BP,CS:RAMADDR
     MOV BX,CS:[BP+DI];DI-0H
          DUMMY: STI

 AGAIN:MOV CX,0FFFFH
 DUMMY1:DEC CX
          CMP CX,0H
              LOOPNE DUMMY1
          MOV CX,0H
          MOV DI,0H

BACK5:NOP

;Frequency and Phase Synchronisation
FPSYNC:MOV AL,0E8H
            OUT CTC,AL;Latch status
            IN AL,CTC2
       CMP AL,80H;Check output pin
            JG  FINDF;Read Frequency
  MAL:MOV MAINAVL,0FFH
            JMP FVMR ;Frequency Voltage Monitoring
FINDF:MOV AL,0D8H;Latch Count
            OUT CTC,AL
            IN AL,CTC2;Read count LSB
            MOV CL,AL
            MOV AL,00H;Load count LSB
       OUT CTC2,AL
       IN AL,CTC2;Read count MSB
       MOV CH,AL
       MOV AL,0FAH;Load count MSB
       OUT CTC2,AL
            XCHG CX,AX
       MOV CX,0FA00H
       SUB CX,AX
       CMP AX,09F6CH;MAINMN
            JG MAINA
            CMP AX,9928H;MAINMX
            JL MAINA
       MOV MAINAVL,0FFH;Mains available
            MOV AL,0H
            OUT PORTA,AL;Enable A1 in Fig.5.1
```

```
    ;Phase Synchronisation
          MOV AL,0E2H;Latch Status CTD0
       OUT CTD,AL
       IN AL,CTD0
          CMP AL,80H;Output pin
       JL MAL
       MOV AL,20H;Enable SPS Circuit
          OUT CTD2,AL
TRAGN:MOV AL,0E4H;Latch Status CTD1
          OUT CTD,AL
          IN AL,CTD1
          CMP AL,80H
       JL TRAGN
       MOV AL,0D4H;Latch Status CTD1
       OUT CTD,AL
       IN AL,CTD1
       MOV CL,AL
       MOV AL,00H;Load Count LSB
       OUT CTD1,AL
       IN AL,CTD1
       MOV CH,AL
       MOV AL,0FAH;Count MSB
       OUT CTD1,AL
       XCHG AX,CX
       MOV CX,0FA00H
       SUB CX,AX
       CMP AX,5H
       JLE FVMR;NOACTION
       CMP AX,3595D
       JGE FVMR;NOACTION
       CMP AX,180D
       JGE LAGC
LEADC:MOV COUNT1,AX
LEAD1:DEC COUNT1
        DEC SI
       JMP FVMR
LAGC:MOV COUNT2,AX
LAG1:DEC COUNT2
       INC SI
       JMP FVMR
MAINA:MOV MAINAVL,0H
       MOV AL,0H
       OUT PORTA,AL;Connect 50 Hz Rreference
  ;Frequency and Voltage Monitoring
         ;Read CTE0
FVMR:MOV AL,0E2H
          OUT CTE,AL;Latch Status CTE0
          IN AL,CTE0
          CMP AL,80H
      JG  FVMR
DOSYNC:CMP COUNT1,0H
        JG LEAD1
        CMP COUNT2,0H
        JG LAG1
        JMP FVMR
        NOP
```

```
FINVF:MOV AL,0D2H;Latch Count CTE0
          OUT CTE,AL
          IN AL,CTE0;Read count LSB
          MOV CL,AL
      MOV AL,0H;Load Count LSB
      OUT CTE0,AL
          IN AL,CTE0;Read count MSB
      MOV CH,AL
      MOV AL,0FAH;Load Count MSB
      OUT CTE0,AL
      XCHG AX,CX;INTr
      MOV CX,0FA00H;INTT
      SUB CX,AX
      MOV AX,CX
      CMP AX,9F6CH;MINFN
      JG  OPSS1
      CMP AX,0992BH;MAXFN
      JL  OPSS1
      JMP FCHART
OPSS1:NOP
       JMP OPSS
 ;Up-date Frequency Chart
FCHART:MOV TMP0,AX
       MOV AX,TMP24
       MOV TMP25,AX
       MOV AX,TMP23
       MOV TMP24,AX
       MOV AX,TMP22
       MOV TMP23,AX
       MOV AX,TMP21
       MOV TMP22,AX
       MOV AX,TMP20
       MOV TMP21,AX
       MOV AX,TMP19
       MOV TMP20,AX
       MOV AX,TMP18
       MOV TMP19,AX
       MOV AX,TMP17
       MOV TMP18,AX
       MOV AX,TMP16
       MOV TMP17,AX
       MOV AX,TMP15
       MOV TMP16,AX
       MOV AX,TMP14
       MOV TMP15,AX
       MOV AX,TMP13
       MOV TMP14,AX
       MOV AX,TMP12
       MOV TMP13,AX
       MOV AX,TMP11
       MOV TMP12,AX
       MOV AX,TMP10
       MOV TMP11,AX
       MOV AX,TMP9
       MOV TMP10,AX
       MOV AX,TMP8
       MOV TMP9,AX
       MOV AX,TMP7
```

```
        MOV TMP8,AX
        MOV AX,TMP6
        MOV TMP7,AX
        MOV AX,TMP5
        MOV TMP6,AX
        MOV AX,TMP4
        MOV TMP5,AX
        MOV AX,TMP3
        MOV TMP4,AX
        MOV AX,TMP2
        MOV TMP3,AX
        MOV AX,TMP1
        MOV TMP2,AX
        MOV AX,TMP0
        MOV TMP1,AX
    ;Find the rate of change of frequency
        MOV CX,TMP25
        CMP AX,CX
        JG RATLF
        SUB AX,CX
        CMP AX,190H;0.5Hz/Sec
        JG OPSS
 RATLF:XCHG AX,CX
        SUB CX,AX
        CMP CX,190H
        JG  OPSS
        JMP MESD
 OPSS:CMP MAINAVL,0H
        JE MESD
        MOV AL,80H;CONTFSS
        OUT PORTA,AL
;Read CTE1 to measure disturbances
 MESD: MOV AL,0E4H
        OUT CTE,AL;Latch Status CTE1
        IN AL,CTE1;Read count LSB
        CMP AL,80H;Output pin
        JGE  MESD1
        JMP DOSYNC
 MESD1:MOV AL,0D4H
        OUT CTE,AL;Latch count CTE1
        IN AL,CTE1
        MOV CL,AL
        MOV AL,0H;Load Count LSB
        OUT CTE1,AL
        IN AL,CTE1;Read MSB
        MOV CH,AL
        MOV AL,0FAH;Load Count MSB
        OUT CTE1,AL
        XCHG AX,CX
        OUT PORTB,AL
        MOV AL,AH
        OUT PORTC,AL
;INTR73:IN AL,ERSIG;Analogue Controller
       ADD AL,CL
       SHR AL,1
       SHL AL,1
       MOV AH,0H
       MOV DI,AX
       MOV BX,CS:[BP+DI]
       IRET
```

```
;ESTABLISH THE DATA SEGMENT******
 HELP:MOV SI,0H
      MOV DI,0H
 PW90:MOV AL,CS:[BP+SI]
          MOV [BX+SI],AL
          INC SI
          CMP SI,90
          JNE PW90
          MOV DI,89
PW180:MOV AL,[BX+DI]
          MOV [BX+SI],AL
          INC SI
          DEC DI
          CMP SI,180
          JNE PW180
       MOV DI,0H

PW360:MOV AL,[BX+DI]
          MOV DL,0DEH;PERIOD NUMBER
          SUB DL,AL
          XCHG AL,DL
          MOV [BX+SI],AL
          INC DI
          INC SI
          CMP DI,180
          JNE PW360
          MOV DI,0
PW600:MOV AL,[BX+DI]
          MOV [BX+SI],AL
          INC DI
          INC SI
          CMP SI,601
          JNE PW600
          RET
;LOAD THE LOOK_UP TABLE ADDRESSES
LOOKUP:MOV SI,0H
           MOV AX,0405H
           MOV [BX+SI],AL
           XCHG AH,AL
           INC SI
           MOV [BX+SI],AL;HIGH BYTE ADDR
           XCHG AH,AL
TBLADDR:ADD AX,258H
           INC SI
                MOV [BX+SI],AL
                XCHG AH,AL
                INC SI
                MOV [BX+SI],AL;HIGH BYTE ADDR
                XCHG AH,AL
                CMP SI,10H
                JNE TBLADDR
        MOV BX,405H
        RET
```

```
;<*<*<*<*INTERRUPT SUBROUTINES*>*>*>*>
INTR72: PUSH AX
        MOV AL,[BX+SI]
                ;OUT PORTA,AL
        OUT CTB0,AL
        MOV AL,[BX+120+SI]
                ;OUT PORTB,AL
            OUT CTB1,AL
            MOV AL,[BX+240+SI]
                ;OUT PORTC,AL
            OUT CTB2,AL
            INC SI
            CMP SI,168H;359
            JGE REFS1
        POP AX
            IRET
 REFS1:MOV SI,0H
       POP AX
       IRET

INTR73:STI
       PUSH AX
       IN AL,ERSIG;     ERROR SIG EQU 040H
           MOV ER1,AL
           ADD AL,ER2
           SHR AL,01H
           ADD AL,ER3
           SHR AL,01H
           MOV AH,ER2
           MOV ER3,AH
           MOV AH,ER1
           MOV ER2,AH
   ;FIND ERSIG IS +VE OR -VE
      CMP AL,040H;020H  ;RFDIG
      JG PPI    ;INC VOLTAGE
      JL NPI     ;DEC VOLTAGE
      POP AX
      IRET
PPI: SUB AL,040H
     MOV AH,AL
     ADD AH,DL ;XE+Y[K-1]
     CMP DL,030H;3CH;5CH;78H;2DH;05AH
     JGE SUPMAX1
         SHR DL,01H    ;0.5
         MOV DH,DL
         SHR DL,01H ;0.25
     SHR DL,01H ;0.125
     ADD DL,DH;0.50+0.125
     ADD AL,DL
     MOV DL,AH;SAVE Xe
     MOV AH,AL
     SHL AL,01H ;2
     SHR AH,01  ;0.50A
     SHR AH,01  ;0.25A
     SHR AH,01  ;0.125
     ADD AL,AH ;2+0.125
     CMP AL,05CH
     JG  SUPMAX2
```

```
        SHR AL,01
        SHL AL,01
        AND AH,0H
        MOV DI,AX
        MOV BX,CS:[BP+DI]
        POP AX
        IRET

 SUPMAX1:MOV DL,030H;5CH;078H
 SUPMAX2:MOV DI,05CH; 45 * 2=90
           MOV BX,CS:[BP+DI];
           POP AX
           IRET

NPI:MOV AH,040H;
    SUB AH,AL
    MOV AL,AH
    CMP AL,DL
    JG SUPMIN1
    MOV AH,DL
    SUB DL,AL ;Y(K-1)-Xe(K)
    SHR AH,01H;.5
    MOV DH,AH
    SHR DH,01H;0.25
    SHR DH,01H;0.125
    ADD AH,DH; 0.50+0.125
    CMP AL,AH
    JG SUPMIN2
    SUB  AH,AL
    MOV AL,AH
    SHL AL,01H;*2
    SHR AH,01H;.5
        SHR AH,01H ;.25
        SHR AH,01H ;.125
        ADD AL,AH ;2+.125
        AND AH,0H
        SHR AL,01
    SHL AL,01;MK EVEN
    MOV DI,AX
    MOV BX,CS:[BP+DI]
    POP AX
    IRET
SUPMIN1:AND DL,0H
SUPMIN2:MOV DI,0H
          MOV BX,CS:[BP+DI]
          POP AX
          IRET

;<<<<<<<<INTR78 FOR TP    AT M
INTR74:IRET
INTR75:IRET
INTR76:IRET
INTR77:IRET
INTR78:IRET
INTR79:IRET
   CODE ENDS
        END UTART
```

```
RUN ASM86 :F9:OMAAD.SRC

RUN ASM86 :F9:TABLES

RUN LINK86 :F9:OMAAD.OBJ,:F9:TABLES.OBJ&
   TO :F9:OMAAD.86

RUN LOC86 :F9:OMAAD.86&
ADDRESSES(SEGMENTS(EXTRA(0H),DATA(000H),&
STACK(7A00H),CODE(0FE000H)))&
RESERVE(06000H TO FDFFFH) START(UTART) BOOTSTRAP

RUN OH86 :F9:OMAAD

S9600

COPY :F9:OMAAD.HEX TO :TO:
```