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Power Factor Corrected Transformerless Three Phase PWM Converter for UPS Applications

by

Malcolm E. Fraser

A Doctoral Thesis submitted in partial fulfilment of the requirements for the award of Doctor of Philosophy of the Loughborough University

June, 1996

Department of Electronic and Electrical Engineering

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To my family

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Synopsis

This thesis describes the research of a new transformerless three phase PWM converter for uninterruptible power supplies (UPS) applications. The removal of the bulky three phase transformer in larger power UPS can provide a significant saving in weight and cost of the overall system.

The converter consists of a new four-wire rectifier coupled with a four-wire inverter via a dc bus. The supply and load neutral may be connected together without any neutral current flowing into the utility regardless of the load on the inverter. This allows the load to be at the same potential as the utility.

The rectifier, inverter and complete UPS and control system are described in detail and simulation results are used extensively to backup the theory. An experimental prototype of the four-wire rectifier provides further confirmation of the principles.

A further proposal to digitize the system is given. This would reduce the size of the required control circuit and simplify the hardware requirements.

Acknowledgements

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Table of Contents

List of Principle Symbols		viii
---------------------------	--	------

Chapter 1: Introduction

1.1	Introduction
1.2	Utility Disturbances
1.3	Uninterruptible Power Supplies
1.4	Transformerless On-Line UPS 4
1.5	Simulation Techniques
	1.5.1 Fortran and Tensor Analysis
	1.5.2 SPICE
	1.5.3 SABER
	1.5.4 Matlab and Simulink 10
1.6	Structure of Thesis 11
Dia	grams

Chapter 2: The Transformerless Four-Wire Power Factor Corrected Reversible Boost Rectifier

2.1	Introduction	
2.2	Principles of Rectification	
	2.2.1 Diode Rectifiers 15	
	2.2.2 Power Factor	
	2.2.3 Four-Wire Diode Bridge Rectification 17	
2.3	Actively Controlled Rectification	
	2.3.1 Basic Switch-Mode Converter Topologies 19	
	2.3.2 Controlling the Line Currents of Rectifiers using DC-DC Converters 21	

	2.3.3	Rectification with Bidirectional Power Flow
	2.3.4	Buck Type AC-DC Converter
2.4	A Ne	w Four-Wire Rectifier
2.5	Contr	rol
	2.5.1	Feedback, Response and Stability
	2.5.2	Switch Mode Control Methods
	2.5.3	Average Current Mode Control of the Four-Wire PFCR
	2.5.4	Choosing the Compensator Parameters
		2.5.4.1 Current Loop Parameters
		2.5.4.2 Voltage Loop Parameters
	2.5.5	Reactive Power Flow
	2.5.6	The DQN Rotating Reference Frame
	2.5.7	Feedforward
2.6	Filter	Values and Harmonics
	2.6.1	Boost Inductance
	2.6.2	DC Bus Capacitance
	2.6.3	L-C Front-End Filter
	2.6.4	Reactive Power Compensation
	2.6.5	High Frequency Harmonics 43
2.7	Simu	lation Results
	2.7.1	Filter Parameters
	2.7.2	Control Parameters
	2.7.3	SABER Schematic
	2.7.4	Step-Load Response
	2.7.5	Unbalanced Supply Voltages 49
2.8	Conc	lusions
Dia	grams	
Sim	nulatio	n Schematics/Results

Ch	apter	3: Four-Wire Inverters
3.1	Introd	uction
3.2	Princi	ples of Inversion
	3.2.1	Single Phase Inverters 69
	3.2.2	Three Phase Inverters
3.3	Distor	tion
3.4	Distor	tion Reduction Using Pulse Width Modulation Techniques
	3.4.1	Selected Notching Modulation
	3.4.2	Natural Sampling
3.5	Four-	Wire Inverter Topologies
3.6	Contr	ol
	3.6.1	Voltage Mode Control
	3.6.2	Current Mode Control
	3.6.3	Choosing the Compensator Parameters
		3.6.3.1 Current Loop Parameters
		3.6.3.2 Voltage Loop Parameters
	3.6.4	Load Current Feedforward
• •.	3.6.5	Load Current Feedforward with Nonlinear Loads
	3.6.6	The DQN Rotating Reference Frame
3.7	Filter	Values
	3.7.1	Filter Inductance
	3.7.2	Filter Capacitance
3.8	Simul	lation Results
	3.8.1	Filter Parameters
	3.8.2	Control Parameters
	3.8.3	SABER Schematic
	3.8.4	Step-Load Change
	3.8.5	Nonlinear Load
	3.8.6	Step-Load Change with Current Feedforward
	3.8.7	Nonlinear Load with Current Feedforward

	3.8.8 Step-Load Change using the DQN Reference Frame		
	3.8.9	Steady-State Comparison of the D-Q-N and A-B-V Reference \ensuremath{Frames} .	95
3.9	Concl	usions	97
Dia	grams		99
Sim	ulation	a Schematic/Results 1	106

Chapter 4: The Transformerless Four-Wire AC-DC-AC Converter for UPS Applications

4.1	Introduction
4.2	A New Four-Wire AC-DC-AC Converter
4.3	Harmonics
	4.3.1 Definitions of Power 117
	4.3.2 Power Flow in the AC-DC-AC Converter
	4.3.3 Required DC Bus Capacitance 119
	4.3.4 Supply Line Harmonic Distortion
4.4	DC Bus Centre-Point Balancing 122
	4.4.1 Centre-Point Balancing using Additional Control 123
	4.4.2 Centre-Point Balancing using an Extra-Leg of Switches 124
	4.4.2.1 Voltage Mode Control 124
	4.4.2.2 Current Mode Control 125
	4.4.2.3 Use of the Centre-Point Balancing Circuit to Remove
	Voltage Ripple 127
4.5	Connection of the Battery Backup
	4.5.1 Direct Connection to the DC Bus
	4.5.2 Connection to the DC Bus via a DC-DC Converter
	4.5.3 Connection via the Rectifier Front-End 129
4.6	Simulation Results 129
	4.6.1 Filter Parameters
	4.6.2 Control Parameters 130

	4.6.3	Step-Load Change
	4.6.4	Unbalanced Load 132
	4.6.5	Unbalanced Load with Lower Bandwidth Rectifier Voltage
		Controller 133
	4.6.6	DC Load 133
4.7	Concl	usions
Dia	grams	
Sim	ulatior	Schematic/Results

Chapter 5: A Practical Implementation of the Four-Wire Power Factor Corrected Boost Rectifier

5.1	Introd	uction
5.2	Power	r Circuit Design 147
	5.2.1	Soft-Start of the Rectifier
	5.2.2	IGBT Modules 148
	5.2.3	Filter Components 149
		5.2.3.1 DC BUS Capacitors 149
		5.2.3.2 Boost Inductors 149
		5.2.3.3 Front-End L-C Filter 150
	5.2.4	Measurement Transducers 150
	5.2.5	IGBT Gate Drivers 151
5.3	Contr	ol Circuit Design
	5.3.1	The Power Supply Board 153
	5.3.2	The Main Control Board 153
		5.3.2.1 A-B-C / D-Q-N Transformations 153
		5.3.2.2 Phase Locked Loop 154
		5.3.2.3 PI Controllers 155
		5.3.2.4 Balancing Control Circuit 156
	5.3.3	DSP Board 156

5.3.3.1 Hardware
5.3.3.2 Software
5.3.4 PWM Board 160
5.3.5 Protection Board
5.3.6 Control Parameters 162
5.4 Experimental Results 163
5.4.1 Harmonic Analysis 164
5.4.2 Steady-State and Transient Performance
5.4.3 Bidirectional Power Flow 167
5.5 Conclusions
Diagrams
Photographs of the Prototype Four-Wire Rectifier
Experimental and Simulation Results

Chapter 6: Proposals for Digital Control of the Four-Wire Rectifier

6.1	Introd	luction	
6.2	Digitized Average Current Controller		
	6.2.1	Sampling and Data Acquisition 193	
	6.2.2	Software and Variables 194	
	6.2.3	Digital Filters	
		6.2.3.1 The z-Domain and the δ Function	
		6.2.3.2 A Digital PI Filter	
	6.2.4	A-B-C, D-Q-N and α - β -o Reference Frames	
	6.2.5	Average Current Control	
	6.2.6	Stability	
6.3	Predic	ctive Average Current Controller 201	
	6.3.1	The Basis of Predictive Control 201	
	6.3.2	Space Vector Modulation for Three-Wire Rectifiers	
	6.3.3	Per-Phase Modulation	

	6.3.4 Average Current Control			
	6.3.5	Practical Requirements		
		6.3.5.1 Hardware		
		6.3.5.2 Software 205		
	6.3.6	Voltage Loop		
	6.3.7	Front-End L-C Filter		
6.4 Simulation Results using Predictive Control		ation Results using Predictive Control		
	6.4.1	Filter Parameters and Control Parameters 207		
	6.4.2	SABER Schematic		
	6.4.3	Steady-State and Transient Response		
6.5	Concl	usions		
Dia	grams			
Sim	ulatior	Schematic/Results		

Chapter 7 Conclusions:

		Summary, Further Work and Further Applications			
7.1	Summary				
7.2	2 Further Work				
7.3	Further Applications				
	7.3.1	Single Converter Four-Wire UPS 226			
	7.3.2	Four-Wire Active Filter			
	7.3.3	Three Phase Induction Motor Drive 228			
Diag	grams				
References					

Appendix

.

DSP Software Listings		37
-----------------------	--	----

List of Principle Symbols

a, b, c		 denotes three phase stationary reference frame quantities
d, q, n		 denotes two phase synchronously rotating quantities
α,β,ο		 denotes two phase stationary quantities
\mathbf{C}_{dc}		dc bus capacitance (per rail), F
C_{f}		filter capacitance
C_{fi}	-	inverter filter capacitance
C _{fr}	-	rectifier filter capacitance
C _s		dc smoothing capacitance of bridge rectifier
d	~	duty cycle (time-varying)
D	~	duty cycle (steady-state)
f_{ci}	~	current loop crossover frequency, Hz
f _{cv}		voltage loop crossover frequency
f _s	-	switching frequency
Gi	-	current loop feedback gain
$\mathrm{G}_{\mathfrak{m}}$		modulator gain
G,	-	voltage loop feedback gain
h	_	harmonic number
I(t)	_	time-varying amplitude of line currents, A
i _{a, b. c}		three phase currents
I _{ave}	-	average inductor current
I _{boost}		ripple current in L _{boost}
I _{dc}		dc load current
iL	_	inductor current

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I_{Lf}	-	ripple current in L _r
I _{max}		maximum of inductor ripple current
I _{min}	-	minimum of inductor ripple current
I _{ni}		peak inverter neutral current
i _o	_	output current
I _{ph}	-	phase current
Δi_{boost}		ripple current of boost inductor
Δi_{fall}	_	fall in inductor current
Δi_{lf}	_	ripple current of filter inductor
Δi_{rise}		rise in inductor current
K _i		integral constant of PI controller
K _{ii}		integral constant of current loop PI controller
K _{iv}		integral constant of voltage loop PI controller
K,		proportional constant of PI controller
K _{pi}	_	proportional constant of current loop PI controller
К _{ру}	_	proportional constant of voltage loop PI controller
F		· · · · · · · · · · · · · · · · · · ·
L	-	centre-point balancing circuit inductor, H
L _{boost}		rectifier boost inductance
L_{f}	_	filter inductance
L_{ti}	_	inverter filter inductance
L _{fr}	_	rectifier filter inductance
M,	-	amplitude modulation index
M _f		frequency modulation ratio
P _i (t)	-	time varying inverter output power, W

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R		load resistance, Ω
R _c		ESR of dc bus capacitor
S _c		slope of carrier waveform
Sm	-	slope of modulating waveform
t _n		nth sample period
t _{off}	_	off-time of switch
t _{on}	-	on-time of switch
T _s	_	switching/sample period
V _{a, b, c}		three phase voltages, V
\mathbf{V}_{ce}	-	IGBT collector/emitter voltage
\mathbf{V}_{dc}	_	dc bus voltage
V_{dc}^{+}	-	positive rail dc bus voltage
V _{dc}		negative rail dc bus voltage
V_i	-	input voltage
$\mathbf{V}_{\mathbf{k}}$	_	kth vector voltage
V_{L}	-	voltage across inductor
Vo	-	peak inverter output voltage
$\mathbf{V}_{\mathtt{ph}}$		phase voltage
$V_r(t)$		dc bus ripple voltage
Vs	-	supply voltage
ω		angular frequency of mains, rad/s
ω,		pole of filter
ω _{zesr}		zero caused by dc bus capacitor ESR

Introduction

1.1 Introduction

This chapter provides an overview to the research into transformerless three phase uninterruptible power supplies. Firstly, the typical disturbances to three phase supplies are discussed. Secondly, a description of uninterruptible power supplies is given.

Computer simulations were used extensively throughout the research and the results are given at the end of each chapter to demonstrate circuit and control principles and performance. As such a description of the various simulators used in the project is given in this chapter.

1.2 Utility Disturbances

For three-phase systems the ideal supply should be three perfect 50Hz sine waves exactly 120° with respect to one another, with a fixed voltage magnitude. In practice there are disturbances to the supply often caused by other loads on the supply interacting with the impedance of the supply. Some of these disturbances are described below [1] :-

Overvoltage (Surges) - The supply voltage magnitude rises significantly above the nominal for more than 1 cycle. This is often caused by the sudden switching off of large loads from the supply or load switching at substations.

Undervoltage (Sags) - The supply voltage magnitude falls significantly below the nominal for more than 1 cycle. This is often caused by loads being switched on to the

supply.

Brownout - This is a long duration sag in the supply voltage and can last up to several days. This is often caused when the mains supply distribution cannot cope with the demand.

Blackout (Outage) - The system voltage is completely lost. This may be caused by supply generating faults, accidents, blown fuses caused by a short circuit or overload, or other abnormal conditions.

Voltage Spikes - Spikes are superimposed on the 50Hz waveform and occur occasionally. This is often caused by the switching on or off of inductive loads or locally grounded lightning strikes.

Chopped Voltage Waveform - Repetitive chopping of the supply voltage waveform. This is often due to switching converters.

Harmonics - Usually low order harmonics of the fundamental frequency are present on the supply voltage. This is often caused by nonlinear loads such as diode bridge rectifiers.

EMI - Electromagnetic interference and electrical noise may be conducted or radiated from its source. This can be caused by high frequency electronic equipment, load switching, welding and lightning strikes.

From the above it can be seen that the typical supply is far from ideal. In applications requiring a more stable and reliable supply an uninterruptible power supply is usually specified. The typical uninterruptible power supplies used in such situations will now be discussed briefly.

1.3 Uninterruptible Power Supplies

Uninterruptible power supplies (UPS) are intended for use on critical processes in industrial, computer and medical applications. Two main requirements must be considered: to provide continuous power to the critical load within a certain tolerance range under various supply and load conditions, and to minimize the distortion caused to the utility voltage due to harmonic currents. The latter point is now particularly important with the recent introduction of European legislation restricting the harmonic pollution caused by a system connected to the mains utility.

There are three main types of UPS [2], these are :-

On-Line - The UPS supplies continuous power to the load, often using an ac-dc converter followed by a dc-ac converter (double-conversion). When the mains supply fails the power is supplied from the battery. A static bypass switch is used to connect the load directly to the mains in case of UPS failure or overload. An on-line UPS is suitable for use on poor mains supplies and for use with highly critical loads.

Fig. 1.1 shows a typical solid-state on-line UPS system with a rectifier and an inverter and includes a static bypass switch and filters for the input, output and dc bus. Galvanic isolation from the supply may be provided by using a 50Hz transformer connected either at the utility or the load. An alternative is to provide the isolation using a high frequency transformer with a high frequency chopping converter in the dc bus.

Off-Line - Unlike the on-line UPS shown in Fig. 1.1, an off-line UPS does not have a rectifier to supply the dc bus. It consists of a battery, battery charger supplied from the utility, inverter and output transformer, and will usually have transient and radio frequency interference (rfi) conditioning. During permissible supply voltage conditions, the load is supplied directly from the utility. If a power failure occurs, then the inverter supplies power to the load from the battery via a bypass switch, and as such the load may

experience a break in supply for up to 10ms. An off-line UPS is suitable for many loads that can be operated safely when connected to a reasonable quality supply. It provides a lower cost solution and has a higher efficiency than the on-line system.

Line-Interactive - This is similar to the off-line UPS, but allows the output voltage to be boosted during a reduction in supply voltage. One method of achieving the required boost in output voltage is to use a tap-change transformer on the output of the system. The boost facility reduces the number of occasions of running on the battery power and helps to maintain a full charge on the battery ready for when a full power failure occurs. A line-interactive UPS is suitable for use where sags and surges occur frequently on the mains supply.

1.4 Transformerless On-Line UPS

For three phase systems, even when galvanic isolation is not required, a transformer must be used so that when the supply neutral and load neutral are connected together, a utility neutral current is prevented from flowing. Fig. 1.2 shows a typical three-phase ac-dc-ac converter with a front-end delta-star transformer for use with an on-line UPS. The transformer allows the utility and load neutrals to be at the same potential, enabling fault currents to flow freely back to the utility via the earth. If the on-line UPS fails, then a bypass to the load from the UPS inverter to the supply is readily achieved as the load neutral is permanently connected to the utility neutral. The three phase transformer also allows the step-up of voltage which is required due to losses in the converters, in addition to providing the system transformation from three-wire to four-wire, as well as enabling the load neutral to be connected directly to the utility neutral.

The removal of the large, utility frequency transformer in a three phase UPS would provide significant savings in cost and weight of the overall system. However, the associated problems of removing the transformer in a system where galvanic isolation is

not required must be overcome. The main objectives of the research are therefore to investigate the feasibility of a three-phase uninterruptible power supply without the requirement of a transformer where galvanic isolation is not required whilst maintaining a connection between the load and the utility neutral points, and to investigate suitable control strategies to enable the UPS to provide a power factor corrected front-end to the utility, and to enable the UPS inverter to cope with various loads including high crest factor loads.

1.5 Simulation Techniques

Computer simulation enables a circuit or process to be tested without the need to build the system and can enable rapid changes to be made of a circuit as required. Complicated control systems may be tried without the need to build the circuit or program a processor. In high power applications, using computer simulation allows the flexibility to try new power topologies and ideas without the risk to personal safety and without the possibility of destroying expensive equipment. It may not be practical or cost effective to experiment with high power equipment.

Of course, once the system has been simulated successfully, the ultimate test is to build the system to prove the system is practically feasible and works generally as the simulation predicted.

There are many different simulators and simulation techniques available [3]. The modelling of the system may be achieved at different levels :-

- A detailed circuit model is used over only a few cycles of the utility to evaluate such things as steady-state and transient responses, stresses on the devices and snubber evaluations, power losses and efficiency evaluations, inductor nonlinearities and the use of more accurate component models.
- Ideal models of switches and diodes are used to simplify the simulation and

enables longer simulation runs to be achieved.

- To further reduce simulation time, a linearized average model of the pulse width modulation (PWM) process [4] may be used but this method has the disadvantage that the associated switching ripple currents of the real system are lost.
- A linearized average model of the whole system may be used and this allows the system to be simulated in the frequency domain.

During the early part of the research, Fortran and then PSpice were used for transient circuit analysis. Later on, SABER became available and subsequently used. SABER is a very powerful circuit simulation package and as such all transient simulation results presented in the thesis are generated from SABER. Matlab and Simulink were used to analyze frequency domain models. These packages are described here.

1.5.1 Fortran and Tensor Analysis

A circuit can be modelled using a high level language from first principles. The typical high level programming language used is Fortran 77 which is widely available and was originally designed for solving numerical problems. The process of writing a program to simulate a circuit initially has a long learning curve, is very time consuming, requires many lines of code to simulate even the simplest of circuits and can take a long time to 'debug' a program. However, the simulation is very flexible in what can ultimately be achieved, as direct control over the simulation is available.

The chosen method adopted for the circuit analysis is Kron's Tensor Analysis [5, 6, 7] and a brief description of the method is given here. Fig. 1.3 shows an example network to be simulated. It consists of three branches, and in this case each branch is made up from a voltage source, a resistor, inductor and a capacitor. A matrix equation consisting of the three branch equations is given as :-

$$[e_{b}] + [V_{b}] = [Z_{b}] \cdot [i_{b}] = [R_{b}] \cdot [i_{b}] + [L_{b}] \cdot [p_{b}] + [C_{b}^{-1}] \cdot [p^{-1}i_{b}]$$
(1.1)

where p = d/dt. The circuit is also realized as a two-mesh network and the matrix equation is :-

$$[e_m] + [V_m] = [Z_m] \cdot [i_m] = [R_m] \cdot [i_m] + [L_m] \cdot [pi_m] + [C_m^{-1}] \cdot [pi_m]$$
(1.2)

The mesh voltage $[V_m] = 0$ using Kirchoff's voltage law.

A transformation or conversion matrix [c] which consists of only 0's, 1's and -1's is used to convert the mesh currents to branch currents :-

A branch current = Σ mesh currents passing through the branch

$$[i_b] = [c] \cdot [i_m] \tag{1.3}$$

The power in the two networks is invariant and the following relationships can be derived [5] :-

$$[e_{m}] = [c]_{l} [e_{b}]$$
(1.4)

$$[Z_m] = [c]_i \cdot [Z_b] \cdot [c] \tag{1.5}$$

For the circuit shown in Fig. 1.3 the branch and mesh matrices are :-

$$\begin{bmatrix} e_{b} \end{bmatrix} = \begin{bmatrix} e_{1} \\ e_{2} \\ e_{3} \end{bmatrix}, \begin{bmatrix} i_{m} \end{bmatrix} = \begin{bmatrix} i_{a} \\ i_{b} \end{bmatrix}, \begin{bmatrix} R_{b} \end{bmatrix} = \begin{bmatrix} R_{1} \\ R_{2} \\ R_{3} \end{bmatrix}, \begin{bmatrix} L_{b} \end{bmatrix} = \begin{bmatrix} L_{1} \\ L_{2} \\ L_{3} \end{bmatrix}, \begin{bmatrix} C_{b}^{-1} \end{bmatrix} = \begin{bmatrix} C_{1}^{-1} \\ C_{2}^{-1} \\ C_{3}^{-1} \end{bmatrix}$$

The branch matrices are converted to mesh matrices using Eqns. 1.4 and 1.5 using the conversion matrix :-

$$[c] = \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ 1 & -1 \end{bmatrix}$$

The mesh equations may be solved numerically using an iterative integration technique such as Runge-Kutta, but first Eqn. 1.2 must be converted into two ordinary differential equations (o.d.e.'s). This may be achieved by using the substitution for the mesh capacitor voltage matrix as $[V_{cm}]$. This gives the two o.d.e.'s to be solved as :-

$$[pV_{cm}] = [C_m^{-1}] \cdot [i_m]$$
(1.6)

$$[pi_m] = [L_m]^{-1} \{ [e_m] - [R_m], [i_m] - [V_{cm}] \}$$
(1.7)

After each iterative solution of the mesh equations, the branch currents may be obtained using Eqn. 1.3.

The Numerical Algorithm Group (NAG) is an additional piece of software that may be used with Fortran 77. This contains many mathematical functions including those for matrix manipulation and various numerical integration routines.

So far, circuits containing only linear elements have been discussed. However power electronics consist of nonlinear devices such as diodes and active switches. If the nonlinear elements are modelled as ideal components then meshes can be added or removed from the current state of the simulation. An overall master conversion matrix describes the possible meshes of the system, but a subconversion matrix is used during a particular state in the simulation and extracts the mesh columns from the master matrix when required. Using a subconversion matrix can simplify the requirements of the

software and reduce simulation time.

The subconversion matrix changes if a point of discontinuity (p.o.d) occurs. For a diode this occurs when the forward current reaches zero (or attempts to reverse) or when the diode becomes forward biased. For an active switch the subconversion matrix changes when the switch is turned on or off. As the iteration time of the integration process is finite the p.o.d may occur in between time steps and thus an interpolation is required to the exact p.o.d and a re-integration must be performed to this point. After a p.o.d. has occurred the new state space equations must be set up before the process re-begins.

1.5.2 SPICE

SPICE was developed in the early 1970's at the University of California, Berkeley. SPICE stands for Simulation Program with Integrated Circuit Emphasis. Although the generic SPICE is freely available there are many commercial versions, such as PSpice, which include graphical circuit entry, various libraries of component models and graphical post-processors. Built in models include resistors, capacitors, inductors, voltage and current sources and semiconductor devices such as diodes, BJT's and MOSFET's. Hirerachical design is possible by the use of subcircuits. The main simulations possible are dc analysis, ac or small signal analysis, and transient or time analysis.

SPICE is widely available and used for power electronic simulations. The time steps are automatically adjusted, but still results in very long simulation run times due to sharp discontinuities caused by switching action and the simulation often fails to converge.

The use of close loop systems can be very difficult or impossible to simulate, especially a controller associated with a switch mode power supply (SMPS). Attempting to model a controller or other component or device with the inflexible models in SPICE can prove

to be very difficult. An extension used in PSpice is the analogue behavioral modelling which allows nonlinear, Laplace and frequency functions and lookup tables to be used. This simplifies the modelling of a controller and greatly improves convergence.

1.5.3 SABER

SABER is a computer simulator for dynamic nonlinear systems and as such is well suited to the simulation of power electronics. SABER is a mixed mode simulator suitable for modelling both analogue and digital circuits. There are many models (templates) provided, but a 'MAST' modelling language allows complete freedom to develop new models. As well as electrical systems SABER can model an entire system such as controllers (Laplace, z-domain), mechanical systems and hydraulic all working together. Fortran, Pascal and C models may be linked into SABER. A graphical front-end for the circuit input is available as well as a graphical post-processor.

Simulation time increases linearly with time rather than quadratically with the size of the system. Hierarchical design is also possible and simulation time increases sublinearly with the size of the system in this case.

Problems with convergence are minimal when modelling a closed-loop power electronics system. The numerous component models available, the complete flexibility of the MAST language and the ability to mix various technologies in a simulation make SABER a powerful computer simulator.

1.5.4 Matlab and Simulink

Matlab is designed as a general equation solver rather than for specific use as a circuit simulator. The system must be provided in terms of differential equations and transfer

functions such as the Laplace domain.

During the research Matlab has been used to model a system in the frequency domain to establish if a particular controller is suitable and stable by providing a bode plot under various load or supply conditions, or controller parameter changes. A system may be simulated in the time domain, but is better suited to average models rather than switched models.

Simulink provides a graphical interface to Matlab and enables a block diagram of readily available transfer functions and other functions to be used and quickly connected together to form a system.

1.6 Structure of the Thesis

Chapter 2 describes the reasons a transformer is often used in three-phase UPS systems and how the system would fail to operate correctly without its presence. The basic principles of rectification are discussed and a proposed four-wire rectifier and average current mode controller is given in detail. The four-wire rectifier enables the transformer to be removed from the system whilst maintaining many of the benefits of having a transformer.

Chapter 3 describes the principles of inversion and a three phase four-wire inverter is described in detail. The use of average current mode control is investigated and its performance evaluated under various load conditions.

The four-wire rectifier and four-wire inverter are connected together to provide the transformerless ac-dc-ac converter and is described in Chapter 4. Although the inverter may be operated under many different control strategies, average current mode control is used to complement that of the rectifier. The interaction between the rectifier and

inverter is investigated. Methods of interfacing the storage battery in UPS systems are given.

Chapter 5 provides a practical implementation of the four-wire rectifier using an analogue controller described in Chapter 2. A description of the design of the power circuit and controller is given in detail. Practical results are provided and compared to the simulation results.

During the period of research an evaluation was performed on the digitizing of the controller for the four-wire rectifier. Two proposals are given in Chapter 6 with a strong practical emphasis of implementation on readily available digital signal processors (DSP) and microcontrollers.

The conclusions in Chapter 7 provide an overall summary of the research, discusses associated further work that may be done with the transformerless UPS, and gives suggestions for alternative use of the transformerless UPS and four-wire rectifier.



Fig. 1.1 Typical On-Line UPS Block Diagram



load and filter







The Transformerless Four-Wire Power Factor Corrected Reversible Boost Rectifier

2.1 Introduction

This chapter describes a new transformerless, four-wire, power factor corrected, reversible, boost rectifier. The rectifier allows connection to a three phase four-wire supply without the need for a transformer and has a power factor of unity.

The discussion will begin with a look at conventional diode bridge rectification [1, 8] and then at the more sophisticated actively controlled rectifier and the new four-wire rectifier. The control is described in detail and simulation results show the performance of the rectifier.

2.2 Principles of Rectification

2.2.1 Diode Rectifiers

In power electronic applications rectification is the principle of converting the ac utility voltage to a dc voltage. Most rectifiers are now made from solid-state components the most common of which are the basic diode rectifiers.

Rectifiers falls into one of two main categories: half-wave and full-wave rectifiers of which there are various single phase or polyphase versions.

Fig. 2.1 shows a single phase half-wave rectifier and its associated current and voltage waveforms. The main problem with this rectifier is that it draws a dc component of current from the supply and requires a large dc side filter capacitor to reduce the 50Hz ripple voltage.

Fig. 2.2 shows a single phase full-wave rectifier with a dc capacitor to reduce voltage ripple and a supply line inductance to improve the input current waveform. This rectifier has the advantage of having no dc component of current on the supply side. A smaller dc side filter capacitor is required to reduce the 100Hz ripple voltage. The problem with using a dc side filter is that the supply side current becomes discontinuous and results in a distorted current waveform. A larger value of capacitance results in a supply side current waveform that has a higher peak. However, the supply side inductance helps to improve this.

For higher power applications three phase rectifiers, also known as six pulse rectifiers, are commonly used. They have the advantage of requiring a smaller dc side filter as the ripple voltage is 300Hz. Also, the rectifier does not require a neutral connection. Fig. 2.3 shows a six pulse diode bridge rectifier with an L-C filter on the dc side and with ac line filter inductance.

So far only uncontrollable diode rectifiers have been discussed. In many cases controllable rectification is required. This involves replacing some or all of the diodes by controllable switches such as thyristors. The thyristors are 'fired' after an appropriate delay known as the firing angle and thus chopping part of the supply voltage waveform and reducing the mean dc voltage. The greater the firing angle the lower the mean dc voltage. The disadvantage of this is that it further distorts the current waveform and reduces the power factor.

2.2.2 Power Factor

It is worth discussing at this stage the definition of *power factor* [9]. If the distorted supply voltages and supply currents are represented by the Fourier series:-

$$v = \sqrt{2}V_{1}\sin(\omega t) + \sqrt{2}V_{2}\sin(2\omega t + \dot{\phi}_{2}) + \dots \sqrt{2}V_{n}\sin(n\omega t + \dot{\phi}_{n})$$

$$i = \sqrt{2}I_{1}\sin(\omega t + \dot{\phi}_{1}) + \sqrt{2}I_{2}\sin(2\omega t + \dot{\phi}_{2}) + \dots \sqrt{2}I_{n}\sin(n\omega t + \dot{\phi}_{n})$$
(2.1)

The RMS V and I becomes :-

$$V = \sqrt{V_1^2 + V_2^2 + \dots + V_n^2}$$

$$I = \sqrt{I_1^2 + I_2^2 + \dots + I_n^2}$$
(2.2)

The definition of power factor is :-

$$PF = \frac{Total \ Power \ Supplied}{V \times I} = \frac{V_1 I_1 \cos\phi_1 + \dots + V_n I_n \cos(\phi_n - \phi_n)}{V \times I}$$
(2.3)

If the supply is stiff the voltage distortion is small and an approximated power factor is given by :-

$$APF = \frac{I_1}{I} \cdot \cos \phi_1 \tag{2.4}$$

It is usually desirable to have a power factor of unity. The fundamental current to total rms current is sometimes referred to as the *distortion factor* and $\cos \phi_1$ as the *displacement power factor*.

2.2.3 Four-Wire Diode Bridge Rectification

If a three phase rectifier is to be supplied from a four-wire utility (three lines plus neutral)

then a three phase star-delta transformer is often used even when galvanic isolation is not required. Fig. 2.4 shows a three phase bridge rectifier with the neutral connected to the centre-point of the dc bus using a centre-tapped capacitor bank in an attempt to remove the transformer. This results in a massive neutral current flowing in to the utility neutral which is mainly third harmonic.

The simplest way to understand why this harmonic occurs is to consider the bridge as two three phase half-bridge rectifiers as shown in Fig. 2.5. The neutral provides the return path for the load current, if these two neutral currents are combined then this results in the neutral current shown in Fig. 2.5. With different ac and dc side filters the neutral current harmonics vary, but the third harmonic still dominates.

The addition of the neutral connection causes triplen harmonic currents to flow in the supply lines. This has the further result of giving a higher dc bus voltage than that possible without the neutral connection.

It is undesirable to have any neutral current in a three phase system if it can be avoided. Fig. 2.6 shows the use of a standard three phase bridge rectifier used in conjunction with a star-delta transformer, thus preventing a supply neutral current from flowing when supplying from a four-wire utility.

2.3 Actively Controlled Rectification

Increasing restrictions by the electricity distributors and European Legislation on the levels of harmonic pollution requires greater awareness of the use of the rectifiers connected to the utility and the distortion caused to the voltage supply waveform [10, 11].

A conventional diode bridge rectifier puts harmonics currents into the supply which causes distortion to the supply voltage waveform due to the supply impedance. This

affects other equipment connected to the utility. As the utility must supply the harmonic currents and reactive current as well as the active current this leads to a reduced power factor and a reduction in the available active power supplied from the utility. This also leads to extra losses in transmission lines and other distribution equipment.

The traditional method of reducing the low order harmonic currents returned to the supply is with the use of large passive L-C filters. This increases the cost and size of the rectifier. It is now becoming more popular to use actively controlled rectifiers which can shape the input line current, thus requiring smaller ac line filter components and giving a better power factor.

2.3.1 Basic Switch-Mode Converter Topologies

Switch-mode converters provide an efficient way of converting power from one voltage or current level to the desired voltage or current level. The high efficiency is possible due to the semiconductor switch either operating with near zero voltage across it or zero current through it, i.e. the switch is either fully on or fully off. The switching frequency is much higher than the frequency which is being tracked.

With the wide availability of gate turn off switch devices such as GTO's, bipolar junction transistors, MOSFET's and IGBT's most modern actively controlled converters now use these switches.

There are three basic types of dc-dc converters and it will be shown how these are applied to ac-dc converters later: these are the buck (step-down), boost (step-up) and buck-boost (step-down/step-up) converters. The topologies are shown in Fig. 2.7.

Fig. 2.8 shows a typical switch pattern applied to the converters. The ratio of the on-time to the switching period of the switch is known as the duty cycle D :-
Four-Wire Rectification

$$D = \frac{t_{on}}{T_s}$$

$$D' = 1 - D = \frac{t_{off}}{T_s}$$
(2.5)
(2.6)

Table 2.1 summarizes the relationship between average input and output voltage and currents. Other basic dc-dc topologies include the Ćuk converter.

Topology	Input-Output Ratios	Output Voltage Range	Output Polarity
Buck	$\frac{V_o}{V_i} = \frac{I_i}{I_o} = D$	0 - V _i	positive
Boost	$\frac{V_o}{V_i} = \frac{I_i}{I_o} = \frac{1}{1 - D}$	V _i - ∞	positíve
Buck-Boost	$\frac{V_o}{V_i} = \frac{I_i}{I_o} = \frac{D}{1 - D}$	0 - ∞	negative

Table 2.1 Basic DC-DC Converters

2.3.2 Controlling the Line Currents of Rectifiers using DC-DC Converters

If a standard diode bridge rectifier is used in conjunction with a dc-dc converter then the line currents can be kept under the control of the switch. Fig. 2.9 shows a single phase bridge rectifier used with a dc-dc boost converter [1, 13].

The current in the boost inductor L_{boost} is forced to follow a fully-rectified sinusoidal current which is in phase with the supply voltage. This results in a sinusoidal current flowing from the supply in phase with the supply voltage, thus achieving unity power factor. The ripple current 'seen' by the supply is at the switching frequency of the dc-dc converter which is usually much higher than the utility frequency.

For this circuit to work the output voltage must be greater than the peak of the supply voltage. The ripple voltage on the dc bus is a second harmonic of the supply frequency. A large capacitance is required to attenuate this component.

A three phase version of the circuit in Fig. 2.9 is discussed in [14] and a buck-boost version in [15] all using only one switch. Problems can arise with the input current not being sinusoidal due to zero current intervals of $\pi/3$. This can be overcome by placing the inductor on the ac supply side and operating in a discontinuous conduction mode (the inductor current is allowed to fall to zero during each switching cycle of the dc-dc converter) [12].

2.3.3 Rectification with Bidirectional Power Flow

The standard diode bridge rectifier and dc-dc converter of Fig. 2.9 may be replaced with the actively controlled rectifier of Fig.2.10. This requires four bidirectional current switches, but has the advantage of allowing bidirectional power flow. The topology is of a boost type, so the dc bus voltage must be greater than the peak of the ac supply

voltage. The supply side current (boost inductor current) is controlled to be sinusoidal and in phase with the supply voltage.

Fig. 2.11 shows a half-bridge single phase version [16]. This has the advantage of only requiring two bidirectional switches.

Extensive publications are available on the topology of three phase, bidirectional boost rectifiers shown in Fig. 2.12 [1, 10, 11, 17, 18, 19, 20]. The three boost inductor currents are controlled to be sinusoidal, each of the three phases providing a third of the power to the dc bus. No low order harmonics are present on the dc bus (unless they are caused by the load).

2.3.4 Buck Type AC-DC Converters

The other main type of active ac-dc converter is of a buck type or step-down converter [21, 22]. Fig. 2.13 show the topology. As the configuration is of a buck type, the dc bus voltage must be less than the peak of the ac line voltage.

There are disadvantages associated with this topology compared with the boost topology due to the diodes in series with the switches :-

- The diodes cause an additional forward voltage drop thus increasing power losses
- The input currents are discontinuous thus requiring larger input filters
- Power flow is unidirectional

2.4 A New Four-Wire Rectifier

A new transformerless, four-wire, power factor corrected reversible boost rectifier which draws no current from the neutral supply is discussed in this section.

The topology of the new four-wire power factor corrected rectifier (PFCR) [23, 24] is shown in Fig. 2.14. It consists of six bidirectional switches, boost inductors in the supply lines and a split capacitor bank to which the supply neutral is connected.

To prevent neutral current from flowing the three line currents must add to zero. This is achieved by drawing sinusoidal currents in each line of equal amplitude and exactly 120° apart :-

$$i_{ns} = i_{a} + i_{b} + i_{c}$$

= $I(t)[\sin(\omega t) + \sin(\omega t - 120^{\circ}) + \sin(\omega t + 120^{\circ})]$
= 0 (2.7)

To allow full control of the switches the dc bus voltage must be greater than the peak voltage of the supply. Also, taking into account the potential across the inductor at the supply frequency this gives :-

$$\frac{V_{dc}}{2} > \sqrt{2} \sqrt{V_{ph}^2 + I_{ph}^2 L_{boost}^2 \omega^2}$$
(2.8)

The switches in each leg are switch alternatively, using a Pulse Width Modulation (PWM) control scheme, with the proviso of a deadperiod (underlap) to prevent both switches being on simultaneously which would cause a short circuit across the dc bus. To enable a sinusoidal current to flow in the boost inductors a sinusoidal voltage must be achieved at the mid-point of each pair of switches.

2.5 Control

To fulfill the conditions of Eqns. 2.7 and 2.8 a control strategy must be realized. This section will describe a proposed method using classical analogue control techniques.

2.5.1 Feedback, Response and Stability

There are two main categories of control: open-loop and closed-loop [25] :-

Open-loop control consists of a controller and a controlled process. A reference is applied to the controller the output of which forms the actuating signal; the actuating signal then controls the controlled process to produce the desired output.

Closed-loop control uses a feedback signal of the output which is compared to the reference (Fig. 2.15). This can result in more accurate control and reject the effects of parameter variation. Also, the response and stability of the overall system can be more readily manipulated and to this effect a closed loop system is used for the four-wire PFCR.

How a system responds is often chosen in two ways: time domain and frequency domain. In the time domain the output should rapidly follow the input (or demand) with little overshoot and without oscillation. In the frequency domain the relative stability of the system can be determined by measuring the Gain and Phase Margins of the transfer function G(s)H(s).

The use of Bode plots is a simple method of obtaining these margins and an example is shown in Fig. 2.16. The Gain Margin is the distance between 0dB and the G(s)H(s) plot at -180°. The Phase Margin is the distance from -180° and the G(s)H(s) plot at 0dB.

2.5.2 Switch Mode Control Methods

The four-wire PFCR controller must control two signals: the input currents and the output voltage. To do this a two loop control system is required. The inner loop controls the input currents and the outer loop controls the output voltage. Such a control system is

termed current mode control.

The basic block diagram is shown in Fig.2.17. The difference between the measured voltage and the reference voltage is passed through the voltage loop controller. This signal is then multiplied by three sine wave templates each 120° apart to form the three phase current references. The sine wave templates are at the supply frequency and are locked to the supply voltage. The current references and the measured inductor currents form the inputs to the current controllers. Due to the nature of the four-wire converter, each current mode controller and each leg may be considered separately and independent from one another.

There are different forms of current mode controllers which are widely used in dc-dc converters. There use in ac-dc converters is also possible. The three main types will be discussed here :-

The first is the *hysteresis* controller, also known as the bang-bang controller. This is a popular form of control because of its simplicity. The inductor current is controlled so that the peak to peak current remains constant. The inductor current is allowed to fall above and below the reference current by a preset amount $\Delta I_L/2$ within a tolerance band. When the inductor current reaches the end of the tolerance band the switches in the leg change over as appropriate. Direct control over the true average inductor current is achieved.

The main disadvantage with this control is that the switching frequency varies over the cycle of the mains making it difficult to choose filter components. The switching frequency will also depend on the tolerance band chosen and the size of the boost inductance.

The *peak* current mode controller [26] allow for a fixed switching frequency. In this scheme a clock pulse is used to turn on or off the switches in the appropriate leg to cause

25

the current in the boost inductor to rise. When the current reaches the current reference the switches are turned on or off to allow the current to fall.

Peak current mode control requires slope compensation at duty cycles greater than 0.5, else subharmonic instability occurs. Perfect compensation is achieved by adding a negative ramp to the reference which has a slope 1/2 the downslope of the measured inductor current. It has also been shown that subharmonic instability can occur at duty cycles less than 0.5 [27]. In an ac-dc converter, where the duty cycle is continually changing, implementing perfect slope compensation can be difficult.

Another disadvantage is problems with noise because of the need to sense the peak current (with a shallow ramp). Also, as the peak of the inductor current follows the reference a peak to average current error exists which varies with duty cycle.

A variation of peak current mode control is valley mode control. In this method the valley of the inductor current ripple follows the reference.

A newer form of current mode control is *Average* Current mode control [28]. In this scheme the difference between the inductor current and the current reference is passed through a compensation network, the output of which is the modulating waveform. This signal is compared to a sawtooth or triangular carrier wave to produce the PWM switch patterns. This gives the advantage of fixed switching frequency and true average current control [29]. In choosing the compensation network parameters a frequency domain model of the converter is required.

2.5.3 Average Current Mode Control of the Four-Wire PFCR

An average current mode control scheme is chosen for the four-wire power factor corrected rectifier due to the reasons given in section 2.5.2. A block diagram of the

control is shown in Fig. 2.18. The dc bus voltage is measured and compared to the reference giving the voltage error. This is passed through a proportional and integral (PI) controller. The PI controller gives a high gain at low frequencies, but has a filtering effect on higher frequencies. The output of the PI controller gives the reference current amplitude for the three inner current loops.

The reference current amplitude is multiplied by each of the three sine wave templates, each 120° apart and locked to the utility frequency, to give the actual current references. Perfect sine wave templates must be used regardless of any distortion in the phase voltage to prevent a neutral current from flowing and to draw sinusoidal line currents.

Each current reference is compared to its respective boost inductor current to give the current errors. These errors are passed through PI controllers to give the modulating waveform signals. The PWM waveforms are generated by comparing the modulating waveform with a triangular carrier wave (Fig. 2.19).

2.5.4 Choosing the Compensator Parameters

The choice of parameters for the PI controllers for the voltage and current loops are very important to the steady state and dynamic performance and stability of the converter. To assess the performance the loop gain (transfer function G(s)H(s) Fig.2.15) of the inner current loop is examined and the compensator is set as required. Then the loop gain of the outer voltage loop is examined and its compensator is set. Generally, the highest gain-bandwidth is required whilst maintaining a stable system. The crossover frequency occurs at 0dB of G(s)H(s).

When considering the characteristics of the converter the boost inductance and dc bus capacitance dominate the bode plot at low frequencies. In voltage mode control with only one control loop a double LC pole occurs, leading to a maximum -180° phase shift before

27

any compensation is added. The compensator either has to have a crossover frequency low down in frequency to give ample phase margin before the -180° phase shift occurs or a derivative (lead) term must be used in the compensator. In current mode control, at low frequencies, a single pole due to the inductor occurs in the current loop and a single pole due the capacitor occurs in the voltage loop (the inductance is 'buried' in the current loop). This leads to simpler compensator design.

To enable an analysis of the dynamics of the converter a linearized small signal model is required. A low frequency small signal model of the conventional dc-dc boost converter has been derived in [30]. The basis of the model is shown in Fig. 2.20 along with the boost converter topology. Although the 4-wire PFCR boost converter topology is different to the basic dc-dc boost converter an analogy can be made between the two.

The model is derived by holding the state variables at a particular operating point and perturbating the steady-state duty ratio D so that :-

 $d = D + \hat{d} \tag{2.9}$

$$d' = 1 - d = D' - \hat{d}$$
 (2.10)

where \hat{d} is the time-varying perturbation of the duty ratio D. This leads to corresponding perturbations of the averaged state variables :-

$$v_o = V_o + \hat{v}_o \tag{2.11}$$

$$i_L = I_L + \hat{i}_L \tag{2.12}$$

2.5.4.1 Current Loop Parameters

The inner current loops controls the inductor current in each of the three phases. Only one of the current loops needs considering, as each of the three compensators has the same parameters.

From Fig. 2.20 the voltage across the inductor L is given as :-

$$V_{L} + \hat{v}_{L} = V_{l} - D'v_{o} - D'\hat{v}_{o} + \hat{d}V_{o} + \hat{d}\hat{v}_{o}$$
(2.13)

The last term $d\hat{v}_{o}$ in the above equation is negligibly small and may be neglected. The small signal inductor voltage is thus :-

$$\hat{v}_{L} = \hat{d}V_{a} - D'\hat{v}_{a} \approx \hat{d}V_{a}$$
(2.14)

where $D\hat{v}_o$ has been neglected at frequencies above the power circuit filter resonance $\omega_0 = D'/\sqrt{(LC)}$. Thus, the small signal relationship between inductor current and duty ratio is given as :-

$$\frac{\hat{i}_L}{\hat{d}} = \frac{V_o}{j\omega L}$$
(2.15)

This equation gives the power section gain with a maximum phase lag of -90° and is independent of load, thus making it the best place to roll-off the gain.

The PI compensator is used to roll-off the gain as desired without adding significantly to the phase lag, this is given in the Laplace domain by :-

$$PI(s) = K_{pi} + \frac{K_{ii}}{s}$$

$$(2.16)$$

where K_{pi} is the proportional constant and K_{ii} is the integral constant. The Bode plot of

this function is shown in Fig. 2.21.

The proportional part of the PI gain (above the PI zero where the phase lag tends towards 0°) is used to set the position of the 0dB crossover frequency of the current loop. The feedback gain of the current loop G_i will also affect the position of the crossover frequency.

By rearranging Eqn. 2.25 and multiplying by the proportional gain K_{pi} and the feedback gain G_i , the current loop crossover frequency is obtained, assuming a carrier waveform with unity amplitude. For the case of the 4-wire rectifier $V_0 = V_{dc}/2$ giving :-

$$f_{cl} = \frac{V_{dc}G_{l}K_{pl}}{4\pi L_{boast}}$$
(2.17)

If the zero of the PI controller is placed at one half the crossover frequency f_{ci} [2.21] then the PI controller will add approximately an extra 27° to the phase lag giving a total of -117° phase lag. This corresponds to a phase margin of 63°. Thus the integral constant is calculated using :-

$$\frac{K_{ii}}{K_{pi}} = \frac{(2\pi f_{ci})}{2} \implies K_{ii} = \pi K_{pi} f_{ci}$$
(2.18)

The current loop bandwidth is chosen as high as possible. The main limitation on the bandwidth is the switching frequency, which can be no higher than half the switching frequency according to Nyquist's sampling theory. The higher frequency portion of the current loop is modelled as a sampled data system. An approximated transfer function of this model is given by a complex pair of right-half plane (RHP) zeros [27] :-

$$H(s) = 1 + \frac{s}{\omega_n Q_z} + \frac{s^2}{\omega_n^2}$$
(2.19)

where $Q_z = -2/\pi$ and $\omega_a = \pi/T_s$ and where T_s is the switching period. A plot of this

function is shown in Fig. 2.22. The additional phase lag caused by this function will lead to a reduction in the current loop phase margin and so should be taken into account when choosing the current loop crossover frequency.

An additional pole may be added to the compensator above half the switching frequency with little effect on the performance of the current loop. This helps reduce high frequency noise [29].

Another concern of the current loop system is limiting the maximum slope of the modulating waveform to no more than the slope of the carrier waveform [28]. This will prevent subharmonic oscillations occurring and prevent multiple switching of the converter occurring (a switch switching faster than the specified switching frequency). The slope of the modulating waveform is mainly due to the inductor current :-

$$\frac{di_{L}}{dt}_{\max} = \frac{\hat{V}_{ph} + \frac{V_{dc}}{2}}{L_{boost}}$$
(2.20)

At the switching frequency this slope will be multiplied by the feedback gain G_i and the proportional gain of the PI controller K_{pi} . The slope of the triangular carrier waveform of unity amplitude is $4f_s$. Therefore :-

$$G_{i} K_{pi} \frac{di}{dt_{\max}} < 4f_{s}$$
(2.21)

An allowance should also be given for the small amount of ripple coming from the voltage loop via the current loop reference.

The modulator affects the current loop gain due to the slopes of the carrier waveform S_c and the modulating waveform S_m [29]. The PFCR modulator gain is given by :-

$$G_m = \frac{4}{(S_c + S_m)T_s}$$
(2.22)

The slope of the carrier waveform will affect the position of the crossover frequency f_{ci} and stability of the current loop.

2.5.4.2 Voltage Loop Parameters

The main consideration for the choice of voltage loop parameters is the dc bus capacitance providing a pole on which the voltage loop gain can crossover 0dB. The inductor is 'hidden' within the current loop. There are two other considerations: a zero due to the ESR of the dc bus capacitance and a RHP zero that is encountered in boost type converters.

The ESR zero is not usually too much of a problem. An additional pole may be added to the compensator to counter the effects of the ESR zero. The RHP zero, however, is more difficult to deal with as it causes a raise in gain by 20 dB/decade in a similar way to a conventional zero, but with 90° phase *lag* [31].

Considering the model in Fig. 2.20 the time-varying output current i_o is :-

$$i_{o} = I_{o} + \hat{i}_{o} = D'I_{L} + D'\hat{i}_{L} - \hat{d}I_{L} - \hat{d}\hat{I}_{L}$$

= $D'I_{L} + D'\hat{i}_{L} - \hat{d}I_{L}$ (2.23)

Thus, the ac component \hat{i}_{ρ} is :-

$$\hat{i}_{o} = \hat{i}_{L}D' - I_{L}\hat{d}$$

$$(2.24)$$

Substituting for \hat{d} from Eqn. 2.15 this gives :-

$$\frac{\hat{i}_o}{\hat{i}_L} = \frac{V_i}{V_o} - \frac{j\omega LI_L}{V_o}$$
(2.25)

The first term is constant with frequency and has no phase shift. The second term

dominates at higher frequencies with an increasing gain, but with a phase lag of 90°, that of a RHP zero. The RHP zero is calculated by equating the two terms in the above equation :-

$$\omega_{i} = \frac{V_{i}}{LI_{L}}$$
(2.26)

For the 4-wire PFCR the input voltage and input current are both sinusoidal :

 $V_i(t) = \sqrt{2}V_{ph} \sin(\omega t)$ and $I_L(t) = \sqrt{2}I_L \sin(\omega t)$ where V_{ph} and I_L are the rms phase voltage and rms supply current respectively. Substituting in Eqn. 2.26 gives :-

$$\omega_{z} = \frac{\sqrt{2}V_{ph}\sin(\omega t)}{\sqrt{2}LI_{L}\sin(\omega t)} = \frac{V_{ph}}{LI_{L}}$$
(2.27)

By balancing the input and output power of the rectifier, I_L can be represented by :-

$$I_L = \frac{V_{dc}^2}{3RV_{ph}}$$
(2.28)

which gives :-

$$\omega_{\mu\nu\rho} = \frac{3V_{\rho\nu}^2 R}{LV_{dc}^2}$$
(2.29)

This is independent of the time varying supply voltage, but is dependent on the load. The lowest frequency at which the RHP zero will occur is on full-load

From [31] the pole in the voltage loop due to the power circuit is given as :-

$$\omega_p = \frac{2}{RC_{eq}} \tag{2.30}$$

where $C_{eq}=C_{dc}/2$. Also, a zero exists due to the equivalent series resistance of the capacitors :-

$$\omega_z = \frac{1}{R_c C_{dc}} \tag{2.31}$$

where R_c is the ESR of the dc bus capacitors.

The output from the voltage PI controller I^{*} sets the amplitude of the current for each of the three phases. This in turn controls the amount of power delivered to the load. By balancing the input power with the output power and assuming at low frequencies that the closed current loop acts as a constant gain equal to the reciprocal of the current loop feedback gain $(1/G_i)$ then :-

$$I_{dc} = \frac{3}{\sqrt{2}} \frac{V_{ph}}{V_{dc}G_{i}} I^{*}$$
(2.32)

In terms of small signal variables, this is represented by :-

$$\hat{l}_{dc} = \frac{3}{\sqrt{2}} \frac{V_{ph}}{V_{dc} G_l} \hat{i}^{*}$$
(2.33)

Above the pole of the voltage loop power circuit, the small signal output voltage to reference current is approximated by :-

$$\frac{\hat{v}_o}{\hat{i}'} = \frac{\hat{i}_{dc}}{j\omega C_{eq}\hat{i}'} = \frac{3V_{ph}}{j\sqrt{2}\omega C_{eq}V_{dc}G_i}$$
(2.34)

This gives a phase lag of 90° and is independent of load and so makes a good place to roll-off the gain in the voltage loop.

The voltage loop PI compensator is used to roll-off the voltage loop gain. Similar to Eqn. 2.16 this is given as :-

$$PI(s) = K_{pv} + \frac{K_{iv}}{s}$$
(2.35)

Four-Wire Rectification

The position of the 0dB crossover frequency in the voltage loop is set by K_{pv} . By rearranging Eqn. 2.34 and multiplying by K_{pv} and the voltage loop feedback gain G_v the crossover frequency is :-

$$f_{cv} = \frac{3}{2\pi\sqrt{2}} \frac{V_{ph} G_v K_{pv}}{V_{dc} G_l C_{eq}}$$
(2.36)

As for the current loop, the zero of the PI controller is placed at one half the crossover frequency f_{cv} . This gives the PI integral constant as :-

$$K_{iv} = \pi K_{pv} f_{cv}$$
 (2.37)

The crossover frequency should be set to about 5 - 10 times lower than that of the current loop to avoid the current loop 'chasing' the voltage loop. It should also be much lower than the RHP zero and the ESR zero to maintain ample phase and gain margins.

A second pole may be added to the voltage loop compensator to cancel the effect of the ESR zero. At higher frequencies the current loop gain will tend to roll-off thus helping to alleviate the effect of the RHP zero.

2.5.5 Reactive Power Control

The control of the 4-wire PFCR shown in Fig. 2.18 may be further extended to include a facility to control the amount of reactive power drawn from the utility. Such a facility may be desirable to allow the PFCR to compensate for the reactive power drawn by other equipment connected to the utility or compensate for a front-end filter connected to the PFCR.

Fig. 2.23 show the extended control. This has a cosinusoidal term added to each current controller reference. The amplitude of the cosinusoidal terms is set by $I_{reactive}^{*}$. If the reactive current is negative then a lagging or inductive current will flow, if it is positive

then a leading or capacitive current will flow.

2.5.6 The DQN Rotating Reference Frame

The d-q [32] and d-q-n reference frames as used in control of three phase converters transform the sinusoidal voltage and current signals (the stationary a-b-c reference frame) into dc equivalents. The direct axis (d-axis) represents the active power flow and the quadrature axis (q-axis) represents the reactive power flow in the system. The d-q reference frame is suitable for 3-wire systems. For 4-wire systems the n-axis is required and, where the transformation is of current, represents the neutral current. The use of the d-q-n reference frame in a 4-wire inverter is given in [33].

To convert from the stationary a-b-c reference frame to the rotating d-q-n reference frame a transformation matrix is used. To convert back the inverse of the transformation matrix is used. The transformations are given as :-

 $i_{dqn} = T(\theta)i_{abc} \tag{2.38}$

$i_{abc} = T^{-1}(\theta) i_{dqm}$		(2.39)
------------------------------------	--	--------

 $T(\theta) = \frac{2}{3} \begin{bmatrix} \sin(\theta) & \sin(\theta - 120^\circ) & \sin(\theta + 120^\circ) \\ \cos(\theta) & \cos(\theta - 120^\circ) & \cos(\theta + 120^\circ) \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix}$ (2.40)

$$T^{-1}(\theta) = \frac{3}{2} [T(\theta)]^{T}$$
(2.41)

where
$$i_{abc} = \begin{bmatrix} i_{a} \\ i_{b} \\ i_{c} \end{bmatrix}$$
, $i_{dqm} = \begin{bmatrix} i_{d} \\ i_{q} \\ i_{n} \end{bmatrix}$

and $\theta = \omega t$

 ω is the angular frequency of the current to be transformed into the dc equivalents. In the case of the PFCR this is 314.2 rads⁻¹ for a 50Hz utility supply.

The transformation of the control into the d-q-n reference frame has a significant improvement of the steady-state control of the 50Hz current . In the stationary reference frame the loop gain of the current loop at dc is theoretically infinite due to the PI compensator. At 50Hz, though, the loop gain has significantly reduced. Thus, an error occurs between the current reference and the measured current. At reduced load this error increases. In the rotating reference frame the 50Hz currents are transformed to dc quantities taking advantage of the theoretically infinite gain of the PI compensator at dc. Thus, there is a zero steady-state current error under all load conditions.

Fig. 2.24 shows the average current mode control of the 4-wire PFCR with the current loops operating in the d-q-n rotating reference frame. The measured boost inductor currents are passed through the transformation to produce the required d-q-n equivalents. There are three current loops for the d, q and n axis. The reference for the d-axis which represents the active power required comes from the voltage loop. As this signal is already dc no transformation of this reference is required. The reference for the q-axis is usually set to zero for zero reactive power flow. The reference for the n-axis is set to zero as no neutral current should flow in the converter.

The d-q-n current errors are passed through PI compensators as before to produce the d-qn modulating waveforms. These are converted back into the a-b-c reference frame to produce the a-b-c modulating waveforms for the pulse width modulator.

In the current loops a 50Hz frequency component is shifted down to dc. At higher frequency components where the crossover frequency occurs in the current loops there

37

is little effect. Thus, the same parameters may be used for the compensators as discussed in section 2.54.

2.5.7 Feedforward

The use of load current or load power feedforward is often used in current mode control systems. The load current (or load power) is measured and a feedforward signal is derived which is added to the current reference derived from the voltage loop. This signal effectively by-passes the slow voltage feedback signal and is used to improve the steady-state and dynamic response due to load variations.

For the 4-wire PFCR the feedforward signal is obtained by balancing the dc output power with the required ac input power. The required feedforward signal is :-

$$I_{ff} = \frac{\sqrt{2}V_{dc}I_{dc}}{3V_{ph}}$$
(2.42)

where I_{dc} is the measured load current, V_{ph} is a constant representing the nominal rms phase voltage and V_{dc} is a constant representing the nominal dc bus voltage. If load power feedforward is required (rather than load current feedforward) then V_{dc} is a measured value and gives a more accurate representation.

The use of feedforward with the 4-wire PFCR has detrimental effects on the neutral current transients and supply current harmonics and is thus not recommended. This is outlined below :-

Neutral Current Transients - When a step-load is put on to the 4-wire PFCR the feedforward signal I_{ff} will be a step demand for the current loops. As each of the three phase currents have to change by different amounts and the current loop cannot follow

a step demand instantaneously a temporary unbalance of supply currents may occur potentially resulting in a large neutral current.

Thus, it is recommended that only a voltage feedback loop is used to provide the references to the current loops, the bandwidth of the voltage loop being 5 - 10 times lower than the current loops.

Supply Current Harmonics - If any harmonics occur on the dc bus, say due to an inverter drawing pulsating power connected as the load to the rectifier, then using load current feedforward will demand the supply to draw pulsating power and draw low order harmonics from the supply.

2.6 Filter Values and Harmonics

An important part of the design of the rectifier is the choice of filter components. The size of the boost inductance determines how much ripple current returns to the utility. The size of the dc bus capacitance determines how well the bus holds its voltage during a transient load change and absorbs harmonic or cyclic power from the load. Further attenuation of ripple current is achieved by using a front-end L-C filter.

2.6.1 Boost Inductance

To calculate the ripple current in each boost inductor a single phase may be considered. Fig. 2.25 show an equivalent circuit for calculating the ripple current. The voltage applied to the rectifier side of the inductor is either $V_{dc}/2$ or $-V_{dc}/2$ assuming a constant dc bus voltage. In each switching period T_s the current in the inductor will rise by Δi_{rise} in time DT_s and fall by Δi_{fall} in time (1-D)T_s where D is the duty cycle of switches in the leg.

39

Four-Wire_Rectification

Using V=Ldi/dt and assuming that at the high switching frequency the ripple current rises and falls linearly then :-

$$\Delta i_{rise} = (v_s + \frac{V_{dc}}{2}) \frac{DT_s}{L}$$
(2.43)

$$\Delta i_{fall} = (v_s - \frac{V_{dc}}{2}) \frac{(1 - D)T_s}{L}$$
(2.44)

Assuming that over one switching period the average inductor current varies by a small amount, then $\Delta i_{rise} \approx -\Delta i_{fall}$ and the duty cycle is given by :-

$$D = \frac{V_{dc}/2 - v_s}{V_{dc}}$$
(2.45)

Thus, the duty cycle varies with the supply voltage over one cycle of the utility. By substituting D from Eqn. 2.45 into Eqn. 2.43 (or Eqn. 2.44) the ripple current is :-

$$\Delta i_{boast} = \Delta i_{rise} \approx -\Delta i_{fall} = \frac{V_{dc}^2/4 - v_s^2}{V_{dc} f_s L} \qquad (pk-pk)$$
(2.46)

and this also varies with supply voltage, the maximum ripple current occurs when the supply voltage reaches zero in its cycle :-

$$\Delta i_{boostmax} = \frac{V_{dc}}{4 f_s L} \qquad (pk-pk) \tag{2.47}$$

By choosing the required maximum ripple current in the boost inductor the required boost inductance may be calculated using Eqn. 2.47.

2.6.2 DC Bus Capacitance

Although a high frequency ripple voltage does appear on the dc bus due to the capacitive impedance and ESR of the capacitors the main choice for the dc bus capacitors depends on how well the dc bus has to remain at its nominal value during a transient load and how well the capacitors attenuate harmonics on the dc bus due to the load.

The response to transient loads on the dc bus depends on the size of capacitance and on the voltage loop.

If the load is simply resistive then no harmonics occur on the dc bus voltage due to the load. If the load is a four-wire inverter as intended for this rectifier then this could result in harmonics being injected into the dc bus. This occurs when the total power of the inverter load is time variant, i.e. the power is cyclic.

2.6.3 L-C Front-End Filter

To reduce the ripple current returned to the utility from the rectifier Eqn. 2.47 shows that either the boost inductance should be increased or the switching frequency increased. Increasing the boost inductance will increase the size and cost of the inductor whilst increasing the switching frequency will increase the losses of the rectifier. An alternative is to use a front-end L-C filter. Fig. 2.26 show the 4-wire PFCR with an additional front-end filter. This will reduce ripple current in the lines and the neutral of the utility.

Fig. 2.27 shows an equivalent circuit for the L-C filter in one of the phases where the rectifier is replaced with a harmonic current source. The attenuation of the ripple current due to the filter is :-

. ...

$$\frac{I_{Lf}}{I_{boost}} = \frac{1}{1 - \omega^2 L_f C_f}$$
(2.48)

where I_{Lf} and I_{boost} are the ripple current in the filter inductor and boost inductor respectively.

The worst case ripple current occurs when the supply voltage is zero in its cycle. At this point the boost inductor ripple current approximates an isosceles triangle (D=0). The Fourier series of this waveform is given by :-

$$i(t) = \frac{4\Delta i_{boostmax}}{\pi^2} [\sin(2\pi f_s t) - \frac{1}{9}\sin(6\pi f_s t) + \frac{1}{25}\sin(10\pi f_s t) - ...]$$
(2.49)

By combining Eqns. 2.47, 2.48 and 2.49 and ignoring the negligible effect of the terms above the fundamental of Eqn 2.49 the peak ripple current in the filter inductor is :-

$$\Delta i_{Lf} = \frac{V_{dc}}{\pi^2 L_{boos} f_s (1 - 4\pi^2 f_s^2 L_f C_f)} \qquad (pk)$$
(2.50)

The resonant peak of the front-end L-C filter should be kept at as high a frequency as possible, preferably above the current loop bandwidth to avoid affecting the current loop dynamics greatly.

In choosing the ratio of $L_{f}/(L_{f}+L_{boost})$ as 1/2 gives the least amount of supply side ripple current, but a ratio between 1/5 and 1/10 still gives an adequate use of the combined inductance whilst giving a lower boost inductor current ripple and a small front-end filter inductance (and a higher resonant frequency of the front-end filter).

2.6.4 Reactive Power Compensation

The addition of the front-end L-C filter will cause a phase shift to occur between the

supply current and voltage. This is due to the front-end filter drawing reactive power at 50Hz. The amount of phase shift will vary with load and thus the power factor will vary with load.

The amount of reactive power drawn by the front-end filter is usually small in comparison to the active power drawn by the rectifier, even-though, the PFCR can be made to compensate for the reactive power by setting the quadrature (q) axis to the required value.

The reactive current drawn by the front-end filter is capacitive in nature and is given by:-

 $I_{reactive} = V_{ph} \omega C_f \tag{2.51}$

The quadrature axis reference is set to the peak of the required reactive current and multiplied by the current loop feedback gain :-

 $i_{q} = -\sqrt{2}V_{ph}\omega C_{f}G_{i}$ (2.52)

A negative i_q^* reference implies a inductive (lagging) current is drawn and a positive reference implies a capacitive (leading) current is drawn.

The PFCR may be used to compensate for other reactive loads connected to the supply by adjusting the reactive current reference accordingly.

The kVA rating of the PFCR must be increased to take in to account any reactive power drawn from the supply.

2.6.5 High Frequency Harmonics

The higher frequency harmonics depend upon the modulation technique. Fig. 2.19 shows

a PWM technique using a triangular (double edged) carrier waveform. This gives harmonics at the carrier frequency and at its multiples. Around these frequencies are sidebands at harmonic h [1]:-

$$h = j(M_{\ell}) \pm k \tag{2.53}$$

where M_f is the ratio of the carrier frequency to modulating frequency. For odd values of j only even values of k exist, and for even values of j only odd values of k exist.

Another form of PWM technique is with the use of a sawtooth (single edged) carrier waveform. This produces a different spectra to that of the double edged carrier. The sidebands of the carrier and its multiples exist at all values of k.

2.7 Simulation Results

To demonstrate the performance of the 4-wire PFCR a SABER simulation has been used operating in the dqn reference frame. Although ideal switches were used in the simulation, the power rating of the simulated rectifier was chosen based on the considerations of a converter design using real switches.

The converter can be fabricated using any one of the three main semiconductor power switches employed in hard switched PWM converter circuits. The high operational voltages and relatively large power for three phase systems together with the requirement for high efficiency, reduced weight, size and cost suggests the use of an IGBT will best achieve these aims. The IGBT combines the easy input control characteristics of the power MOSFET with the high off-state and low on-state voltage characteristics of the bipolar junction transistor (BJT) [34].

The power rating of the converter simulated is set at 80kW and the switching frequency

set at 15kHz. This power rating was chosen as it can be achieved by readily available single module IGBT's (example Toshiba) when used in a hard switched PWM converter switching at 15kHz. A higher switching frequency will increase the switching losses whilst a lower switching frequency will increase the size of the inductors. A 15kHz switching frequency therefore is a good compromise to achieve high efficiency and a compact converter.

The rectifier is supplied from a three phase, 4-wire utility at 400 volts (230 volts phase). The dc bus voltage is chosen as 800 volts which satisfies Eqn. 2.8 and gives plenty of margin for supply voltage fluctuations and dips in the dc bus voltage from the nominal.

2.7.1 Filter Parameters

The filter parameters are chosen using the equations in Section 2.6.

The peak of the rms supply current will be 164A per phase on full-load. If the peak ripple in the boost inductor is chosen as one-third of this, then the boost inductance required is 122μ H per phase using Eqn. 2.47.

Further attenuation is achieved by using a front-end L-C filter. The attenuation is chosen to give 5% of the boost inductor current in the filter inductor at the switching frequency i.e. a 20:1 reduction, and the filter inductance L_f as approximately one-fifth the boost inductance (25µH). Using Eqn. 2.48 this gives the filter capacitance C_f as 85µF. This corresponds to a worst case ripple current of about 2.5A (peak) using Eqn. 2.50.

Although only a small amount of dc bus capacitance is required for a resistive load to the PFCR, its intended use will be for UPS applications with an inverter load. This will inject harmonics on to the dc bus due to cyclic power from the inverter. This must be provided by a relatively high dc bus capacitance for a high power converter. The dc bus

45

capacitance per rail C_{de} is chosen as 10mF.

The power and filter components are summarized below :-

$$\begin{split} P_{\text{rating}} &= 80 \text{ kW} & f_{\text{s}} &= 15 \text{ kHz} & V_{\text{ph}} &= 230 \text{ V} & V_{\text{dc}} &= 800 \text{ V} \\ L_{\text{boost}} &= 122 \,\mu\text{H} & C_{\text{dc}} &= 10 \,\,\text{mF} & L_{\text{f}} &= 25 \mu\text{H} & C_{\text{f}} &= 85 \,\mu\text{F} \end{split}$$

2.7.2 Control Parameters

The control parameters are chosen using the Equations in section 2.54.

The boost inductor current and dc bus voltage are measured to provide the feedback signals to the controller. These signals, obviously, have to be reduced in magnitude for a physical control circuit to cope with. The feedback gain for the voltage loop is chosen as $G_v = 1/100$ and for the current loop $G_i = 1/25$.

A current loop crossover frequency is chosen as 3kHz. From Eqn. 2.17 this gives the proportional gain of the PI controller in the current loop $K_{pi} = 0.144$. This also satisfies Eqn 2.21 for the limiting of the slope of the modulating waveform to no more than the slope of the carrier waveform and leaves enough margin for any additional slope coming from the voltage loop.

The integral gain of the PI controller is set according to Eqn. 2.18 as $K_{ii} = 1357$ rads⁻¹ which corresponds to a phase lag of -117° at the crossover frequency. This phase lag is further increased by 37° due to the sampling effect in Eqn. 2.19. Thus, the phase margin is 26° which is quite adequate. The effects of ringing will be limited as no step demands will be placed on to the current loop due to the filtering effect by the voltage loop on the current loop demand.

The voltage loop crossover frequency is set to one-tenth of the current loop bandwidth and is thus chosen as 300Hz. The proportional gain is calculated using Eqn. 2.36 to give $K_{pv} = 62$ and the integral gain is calculated using Eqn. 2.37 to give $K_{iv} = 58.4$ krads⁻¹ which corresponds to a phase margin of 63°.

The worst case RHP zero occurs at full-load (R= 8Ω) at 2.6kHz (Eqn. 2.29) which is well above the voltage loop bandwidth.

Estimating the capacitor ESR as approximately $20m\Omega$ per capacitor this gives an ESR zero as approximately 800Hz. To counter this a pole is added at this frequency in the voltage compensator.

The reactive power drawn by the PFCR due to the front-end L-C filter is small compared to the rating of the converter, nevertheless a compensating reactive power is made to flow to counter this. Using Eqn 2.52 i_{g}^{*} is set to -0.347.

The control parameters are summarized below :-

G _i = 1/25	$K_{pi} = 0.144$	$K_{ii} = 1357 \text{ rads}^{-1}$
$G_v = 1/100$	$K_{pv} = 62$	$K_{iv} = 58.4 \text{ krads}^{-1}$
$\omega_{zest} = 5 \text{ krads}^{-1}$	$i_q^* = -0.347$	

2.7.3 SABER Schematic

The rectifier design is entered through the SABER schematic editor Design Star. Fig. 2.28 shows the power circuit schematic. It consists of six ideal switches with antiparallel diodes, a split capacitor across the dc bus and a resistive load which may be switched in or out. The circuit is supplied from a three phase supply via the boost inductors and L-C front-end filter. A small resistance $(1m\Omega)$ is added in series with the

boost inductors to enable the boost inductor currents to be measured. 'Same Page Connectors' are used for connection to the control schematic, enabling a reduction in wires.

Fig. 2.29 show the control circuit schematic. Rather than being made up of discrete components such as operational amplifiers, the control circuit is operated in the control domain. Control blocks such as PI controllers, filters and voltage sources are readily available from a control menu in Design Star. To connect between the analogue and control domain conversion blocks are available. The voltages measured across the $1m\Omega$ resistors are converted using the conversion blocks. The conversion blocks have an inbuilt gain which is set to $1000 (1/1m\Omega)$ to obtain the equivalent boost inductor currents in the control domain. In a similar way the dc bus voltage is measured and converted to the control domain.

The voltage error is passed through a PI controller and a low pass filter (to cancel the ESR zero). This forms the reference for the d-axis current. The boost inductor currents are passed through a transformation matrix T to obtain the dqn currents. The transformation block is a sub-circuit with a number of sinusoidal sources to achieve the conversion of the matrix of Eqn. 2.40. The transformation is locked at 50Hz to the red phase supply voltage. The d, q and n error signals are passed through PI controllers and are converted back to the a-b-c reference frame using another sub-circuit T⁻¹. The modulating signals are then compared to a 15kHz triangular wave and passed into a switch controller sub-circuit. In this sub-circuit two signals are provided one simply the logical inverse of the other and then to two switch drivers.

Although no deadband is used and ideal switches are used this still represents a close approximation and reduces simulation time.

48

2.7.4 Step-Load Response

The first set of simulation results are for a step-load response on the PFCR. The PFCR is operated at full-load R=8 Ω . After 25ms the load is switched out and then back in again at 45ms.

Fig. 2.30 show the supply phase voltages and currents. The supply currents are sinusoidal and in phase with the voltages. Fig. 2.31 shows the supply neutral current. No low order harmonics exist, the neutral current consist of a high frequency switching ripple.

Fig. 2.32 show the dc bus voltage. A small amount of high frequency switching ripple is superimposed on the bus voltage. During the step-load changes the response of the dc bus voltage is very good with little undershoot or overshoot with a rapid, well damped settling period.

Fig. 2.33 shows the current in the red phase boost inductor which may be compared with the supply current to demonstrate the attenuation of the front-end filter.

2.7.5 Unbalanced Supply Voltages

In practical systems, the supply voltage may not be balanced. The PFCR has been simulated with unbalanced supply voltages. The red phase voltage is at the nominal rms voltage of 230 volts, the yellow phase is 10% higher with an rms voltage of 256 volts and the blue phase is 10% lower with an rms voltage of 207 volts. This corresponds to a supply voltage unbalance of 20%. The PFCR is operated at full-load (R=8 Ω).

Fig. 2.34 shows the supply phase voltages and currents. A distortion occurs in the supply current. This can be explained as follows: the unbalanced supply voltage causes a cyclic power to be drawn from the supply at 100Hz. This results in a small amount of 100Hz

voltage ripple to occur on the dc bus. This signal is fed back via the voltage loop and amplified by the voltage loop compensator which becomes a 100Hz current demand. This signal is multiplied by the 50Hz template in the dqn transformation matrix causing additional 50Hz and 150Hz to flow in the supply currents.

The small amount of 50Hz current present in the supply neutral shown in Fig. 2.35 is mainly due to the circulation of 50Hz current in the front-end L-C filter due to the unbalanced supply voltage. The PFCR itself is only responsible for a small amount of this 50Hz current due to the controller not tracking the currents ideally.

Fig. 2.36 shows the dc bus voltage. It is very difficult to see the small amount of 100Hz voltage ripple due to the cyclic power drawn from the supply.

To reduce the distortion caused to the supply currents due to the feedback of the ripple voltage on the dc bus either the voltage loop bandwidth must be reduced or a notch filter used to remove the 100Hz voltage component from the voltage feedback signal.

2.8 Conclusions

This chapter has described the various conventional rectifiers and their effect on the utility and dc bus. The use of actively controlled rectifiers has significant advantages over conventional rectification. They allow reduced harmonic currents returning to the supply and improved power factor, require much smaller filter components and have a better regulation of the bus voltage. There are many different and novel methods of three phase active rectification; the advantages and disadvantages have been described in some detail.

A new four-wire power factor corrected rectifier has been presented. It does not require a transformer to prevent neutral currents from flowing, but relies on the control to prevent

the flow of neutral current. The rectifier is of a boost type configuration providing a stepup of voltage so no longer relies on the transformer for this facility.

An average current mode control scheme has been used allowing accurate control of the supply currents and good regulation of the dc bus voltage. The choice of compensator parameters of both the current and voltage loop has been explained in detail and problems to look out for, such as the RHP zero in the voltage loop, when choosing the compensators. Operating the control in the rotating dqn reference frame gives a significant improvement to the steady-state control of the supply currents under all load conditions.

The choice of filter components was covered which includes the boost inductances and the dc capacitance. Further attenuation of the supply ripple current is achieved through the use of a small front-end L-C filter. Any phase shift of the phase currents with respect to the phase voltage due to the L-C filter can be cancelled by adjusting the amount of reactive power drawn by the PFCR as appropriate.

Simulation results using SABER have shown the effectiveness of the converter. Under various loading conditions the converter responds well and has a small amount of low frequency neutral current flowing. Under unbalanced supply conditions the supply currents may be distorted which may be remedied using a low voltage loop bandwidth or notch filter in the voltage loop feedback. Any low order harmonic neutral current flowing into the supply is mainly due to 50Hz currents circulating in the front-end filter.







Fig. 2.2 Full-Wave Rectifier with Filter



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Fig. 2.4 Four-Wire Rectifier with Centre-Tapped Capacitors



Fig. 2.5 Four-Wire Rectifier Split into Two Half-Bridge Rectifiers







Fig. 2.7 Basic DC-DC Converter Topologies



Fig. 2.8 Duty Cycle



Fig. 2.9 Single Phase Active Rectifier with Controllable Input Currents



Fig. 2.10 Single Phase Active Rectifier with Bidirectional Power Flow



Fig. 2.11 Half-Bridge Single Phase Active Rectifier


Fig. 2.12 Three Phase Active Boost Rectifer



Fig. 2.13 Three Phase Active Buck Rectifier



Fig. 2.14 Four-Wire Power Factor Corrected Boost Rectifier



Fig. 2.15 Closed-Loop Control System







Fig. 2.17 Basic Control of the 4-Wire PFCR



Fig. 2.18 Average Current Mode Control of the 4-Wire PFCR







Fig. 2.20 Average Linearized Model of the Boost Converter



Fig. 2.21 Bode Plot of Proportional and Integral Controller



Fig. 2.22 Bode Plot of Sampled Data System Model



Fig. 2.23 Control of the 4-Wire PFCR with Reactive Power Control







Fig. 2.25 Equivalent Circuit of the Boost Inductor



Fig. 2.26 Four-Wire PFCR with Front-End L-C Filter



Fig. 2.27 Equivalent Circuit of the L-C Front-End Filter



Fig. 2.28 80kVA 4-Wire PFCR SABER Power Circuit Schematic





Fig. 2.29 80kVA 4-Wire PFCR SABER Control Schematic



Fig. 2.30 Step-Load Change - Supply Voltages and Currents



Fig. 2.31 Step-Load Change - Supply Neutral Current





Fig. 2.32 Step-Load Change - DC Bus Voltage



Fig. 2.33 Step-Load Change - Red Phase Boost Inductor Current





Fig. 2.34 Unbalanced Supply Voltage - Supply Voltages and Currents



Fig. 2.35 Unbalanced Supply Voltage - Supply Neutral Current





Four-Wire Inverters

3.1 Introduction

This chapter describes the four-wire inverter that complements the four-wire rectifier. Four-wire inverters allow for loads that may be considerably unbalanced.

The basis of inversion is discussed along with three-phase inverters and four-wire inverters. The control of the inverter is important in providing the required regulation to the load and is discussed in detail. Simulation results are used to highlight the performance of the four-wire inverter.

3.2 Principles of Inversion

Inversion is the principle of converting dc power to ac power at a desired voltage or current and frequency. Most inverters use solid state devices all of which require some form of controllable switch.

There are two main categories of inverters: voltage-fed and current-fed. As the inverter is to be supplied principally from the four-wire rectifier with a fixed dc bus voltage (Chapter 2) only voltage-fed inverters will be discussed.

3.2.1 Single Phase Inverters

Fig. 3.1 shows the basic topology for a single phase bridge inverter. It consists of four

switches and four anti-parallel diodes and as such four-quadrant operation is available. Gate controlled switches such as bipolar junction transistors (BJT's), MOSFET's, IGBT's, and GTO's.

The basic form of output provided is a *square-wave* voltage at the required fundamental output frequency. This is achieved by alternatively switching S1, S2 and S3, S4. Control of the output voltage may be achieved by introducing zero periods into the square-wave. This is known as *quasi-square wave*. An alternative and superior method of control is the sinusoidal PWM technique.

A half-bridge single phase inverter is shown in Fig. 3.2. This consist of two switches with associated anti-parallel diodes. The return path for the current is via a centre-tapped dc supply which may be provided by a centre-tapped capacitor connected across the dc bus.

3.2.2 Three Phase Inverters

A three phase inverter is shown in Fig. 3.3. It consists of six switches and six antiparallel diodes. The load shown is connected in star configuration, but may also may connected in delta. This inverter also allows for bidirectional power flow.

The basic form of output is obtained by switching each switch in the leg of inverter alternatively with a conduction of angle 180° at the required fundamental frequency. This results in a quasi-square wave line output voltage. The rms value of the fundamental line voltage is $\sqrt{6V_{dc}}/\pi$ [34].

3.3 Distortion

Ideally, the output from an inverter should be a sine wave. Often the output is distorted and harmonics are present in the waveform. If the distorted output voltage waveform is represented as :-

$$v = \sqrt{2}V_1 \sin(\omega t) + \sqrt{2}V_2 \sin(2\omega t + \phi_2) + \dots + \sqrt{2}V_n \sin(n\omega t + \phi_n)$$
(3.1)

and the total RMS as :-

$$V = \sqrt{V_1^2 + V_2^2 + \dots + V_n^2}$$
(3.2)

then the total harmonic distortion (THD) of the voltage waveform is given by :-

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1}$$
(3.3)

The power factor of the output voltage and current waveforms is also used and the definition has been explained in Section 2.2.2.

3.4 Distortion Reduction Using Pulse Width Modulation Techniques

Square wave and quasi-square wave output voltages have high low order harmonic contents. In a three-wire three phase system these low order harmonics are the 5th, 7th, 11th, etc. harmonics. To attenuate these components large filters are required. The use of pulse width modulation (PWM) reduces the output voltage harmonics and the size of the required filter.

3.4.1 Selected Notching Modulation

Selective harmonics elimination of the output waveform is achieved by adding notches to each half-cycle of the fundamental voltage waveform [34, 35, 36]. For each harmonic to be removed a notch is required per 90°. The position and width of each notch is precalculated using a computer. The output voltage may be altered by varying the input voltage or by adding an extra notch. The operation of the switches has to be precise to prevent additional low amplitude harmonics occurring. The additional switching occurring during one cycle of the fundamental output frequency will increase switching losses in the inverter.

3.4.2 Natural Sampling

With the availability of faster and higher power switches one of the most popular forms of inverter control is natural sampling. A modulating waveform is compared with a triangular carrier waveform. The intersection of the two waveforms forms the required PWM pulses (Fig. 2.19).

The frequency of the carrier is usually much higher than the modulating waveform. Ideally the only low order harmonic present in the voltage waveform is that of the modulating waveform. A small filter is required to attenuate the high frequency harmonics of the carrier. The much higher switching frequency results in even higher switching losses, but results in a lower distortion in the output voltage.

The output voltage is varied by varying the ratio of the amplitude modulating waveform to the amplitude of the carrier waveform. This is known as the amplitude modulation index M_a .

Other variations of this analogue modulation technique include the use of a sawtooth

carrier waveform resulting in single-edge modulation rather than a triangular carrier which results in double-edged modulation.

Over modulation [37] is sometimes used in order to generate higher output voltages from a given dc supply. This is achieved by adding third harmonic components to the modulating fundamental waveforms, and is known as the harmonic injection technique. The third harmonic component disappears in the three phase waveform.

The normal modulation process is sometimes halted for a period symmetrical about the peak of the output voltage [37]. The switches are either fully on or off. This reduces the switching losses whilst not having a significant affect on the output voltage harmonics.

3.5 Four-Wire Inverter Topologies

A UPS has to be able to supply a considerable unbalanced load. To prevent the output voltages becoming unbalanced a four-wire output is required which includes a connection for load neutral current.

There are three main methods of supplying a four-wire load from a three phase inverter [38] :-

- A delta-star transformer provides a connection for the neutral at the star-point (Fig. 3.4). This has the advantage of providing galvanic isolation, the facility to step-up the required output voltage and the leakage inductance of the transformer can be used as filter inductance. The main disadvantage is the requirement of a low-frequency power transformer.
- A fourth-leg may be used to provide the neutral connection (Fig. 3.5). This

allows for instantaneous phase voltages up to the dc supply V_{dc} and allows for free-wheeling states to be selected in individual phases [39].

• A centre-tapped supply may be used for the neutral connection. This is commonly achieved by using a centre-tapped capacitor connected across the dc bus (Fig. 3.6). This is a simpler method than above requiring no extra switches or additional control.

All of the above topologies (Figs. 3.4 - 3.6) are shown with L-C filters to reduce the switching frequency harmonics to the load.

As a centre-tapped capacitor is used for the four-wire rectifier, the same centre-tapped capacitor will be used in the inverter to provide the load neutral connection.

3.6 Control

The objective of the inverter controller is to regulate the output voltage. Analogue control methods are discussed in this section.

The inverter may be operated in open-loop control or closed-loop control. Open-loop control is the simplest, but a number of disadvantages are associated with this. These include problems with component variation and poor control over the steady-state and dynamic response of the output voltage. As an L-C output filter is commonly used, the phase shift caused by the filter is difficult to compensate for under all load conditions.

Closed-loop control overcomes the above problems. There are two main categories of this form of control for inverters. These are voltage mode control and current mode control which will be considered in the continuous mode of operation.

The inverter topology is a step-down or buck derived converter. If the supply voltage is stiff then each phase may be considered independent from one another.

3.6.1 Voltage Mode Control

The general form of a voltage mode controller is shown in Fig. 3.7 for one phase of the inverter. The output voltage is compared to the required sinusoidal reference. This error signal is passed through a compensator C(s) and forms the modulating signal which is then compared to a triangular wave carrier to obtain the required PWM pulses.

The voltage mode controller compensator has to be set to provide a high loop gainbandwidth characteristic whilst maintaining stability. A linearized small signal model of the power circuit is shown in Fig. 3.8 for the basic buck converter which is much simpler than the boost converter.

The model is derived by holding the state variables at a particular operating point and pertubating the steady-state duty ratio D ($D=V_o/V_i$). The same state variables used in Eqns. 2.9 - 2.12 may be used. Neglecting the ESR (R_e) of the capacitor from the model in Fig. 3.8 the output voltage is given as :-

$$V_o + \hat{v}_o = \frac{V_i(D + \hat{d})}{s^2 L_j C + L/R + 1}$$
(3.4)

Rearranging in terms of small signal values this gives :-

$$\frac{\hat{v}_{o}}{\hat{d}} = \frac{V_{i}}{s^{2}L_{f}C + sL/R + 1}$$
(3.5)

For the four-wire PFCR $V_{dc}/2$ is substituted for V_i .

The power circuit phase will reach a maximum of -180° phase lag before any

compensation is added. Two solutions exist for choosing a compensator: either roll-off the gain well before the resonant frequency $\omega_o = 1/\sqrt{LC}$ or use a lag-lead compensator. The use of a lag-lead compensator allows for a higher loop gain-bandwidth and will be explained here.

The transfer function of the compensator is :-

$$C(s) = \frac{K(s/\omega_1 + 1)(s/\omega_3 + 1)}{(s/\omega_2 + 1)(s/\omega_4 + 1)}$$
(3.6)

The compensator has two zeros and two poles. One of the poles can be placed at the origin to provide high gain at lower frequencies and the two zeros are placed at ω_0 to cancel the double pole at the resonant frequency of the power circuit. The crossover frequency of the loop can be set above ω_0 by the constant K. This will give a phase lag at the crossover frequency of between -90° and -180°. The other pole is typically placed at the position of the ESR zero of the filter capacitor to cancel the effects of this. The ESR zero is given by :-

$$\omega_z = \frac{1}{R_c C_f} \tag{3.7}$$

Below the crossover frequency the phase lag may approach or go beyond -180° especially near the resonant frequency of the power circuit. This is known as conditional stability [28] and is quite acceptable. Problems may occur during start up conditions of the converter or during large output changes when the bandwidth of the system may momentarily change.

A major disadvantage of voltage mode control is the slow response to input voltage changes. A solution to this problem is to use line voltage feedforward. To achieve this the amplitude of the triangular carrier wave varies in direct proportion to the input voltage. This provides very good rejection to input voltage changes.

3.6.2 Current Mode Control

A block diagram of a current mode controller as applied to the four-wire inverter is shown in Fig. 3.9 for one phase. This is essentially a two control loop design. The output voltage is measured and compared to the required sinusoidal reference. This forms the voltage error which is then passed through the voltage loop controller. This forms the reference filter inductor current which along with the measured filter inductor current provide the inputs to the current mode controller.

The use of current mode control has a number of advantages over voltage mode control. These are :-

- Only a single pole occurs in the control-to-output characteristic, thus simplifying compensator design
- Allows some form of current limitation by limiting the demand to the current loop
- Input voltage feedforward is inherent, thus providing very good rejection of input voltage disturbances
- Allows equal current sharing between modular converters operating in parallel

There are three main types of current mode controller: the *hysteresis*, *peak* and *average*. The basis of these controllers was discussed in Section 2.5.2 and because of the advantages stated for average current mode control, an investigation into its application for the four-wire PFCR will be described here [40].

A block diagram of the proposed average current mode controller is shown in Fig. 3.10 for one phase of the inverter. The output (load) voltage is measured and compared to the sinusoidal reference. The voltage error signal is passed through a PI controller to give the reference current for the filter inductor. This is compared to the actual filter inductor current and passed through another PI controller to give the required modulating signal. The PWM pulses are generated by comparing the modulating signal with the triangular

carrier waveform.

3.6.3 Choosing the Compensator Parameters

Using the model in Fig. 3.8 of the linearized small signal model of the buck converter the required parameters for the compensators of the current and voltage loops can be obtained.

3.6.3.1 Current Loop Parameters

The current loop controls the filter inductor current. From Fig. 3.8 the inductor current is given as :-

$$I_{L} + \hat{I}_{L} = \frac{V_{I}(D + \hat{d})(sC_{f} + 1/R)}{s^{2}L_{f}C_{f} + sL/R + 1}$$
(3.8)

Thus, the small signal relationship between inductor current and duty cycle at frequencies above the resonant frequency $\omega_0 = 1/\sqrt{(LC)}$ is :-

$$\frac{\hat{l}_{L}}{\hat{d}} \approx \frac{V_{I}}{j\omega L_{f}}$$
(3.9)

This gives a maximum phase lag of -90° and is independent of the load. The current loop gain can be forced to crossover 0dB by using a PI controller. The transfer function is given below :-

$$PI(s) = K_{pl} + \frac{K_{ll}}{s}$$
(3.10)

The proportional gain is used to set the frequency of the current loop crossover frequency. The feedback gain of the current loop G_i will also affect the position of the crossover frequency. By equating the current loop gain to 1 (0dB) the crossover frequency may be obtained. By assuming a carrier waveform with unity amplitude and setting $V_i = V_{dc}/2$ this gives :-

$$f_{ct} = \frac{V_{dc}G_{t}K_{pt}}{4\pi L_{f}}$$
(3.11)

The zero of the PI controller may be placed at one half the crossover frequency in a similar way to Eqn. 2.18. This will correspond to a phase margin of 63°. This gives an integral constant of :-

$$K_{ii} = \pi K_{pi} f_{ci} \tag{3.12}$$

If the resonant frequency of the power circuit ω_o approaches or is above the required current loop crossover frequency then it makes it very difficult or impossible to crossover on the pole of the filter inductor and Eqn. 3.11 is no longer valid (particularly if a small filter capacitor is used).

As discussed for the rectifier in Section 2.5.4.1, the bandwidth of the current loop can be no higher than half the switching frequency. At higher frequencies the current loop is modelled as a sampled data system given in Eqn. 2.19. The additional lag incurred by this function should be taken into account when choosing the current loop crossover frequency.

An additional pole may also be added to the compensator above half the switching frequency to help in reducing high frequency noise.

Concern over slope limitation of the inductor current is relevant to the inverter as with the rectifier and Eqns. 2.20 - 2.22 apply.

3.6.3.2 Voltage Loop Parameters

One of the main considerations when choosing the voltage loop parameters is the output filter capacitor. Unlike the rectifier, however, there is no RHP zero in the voltage loop. A zero occurs due to the ESR of the output capacitor.

From the model in Fig. 3.7, neglecting the ESR zero, the relationship between output voltage and inductor current is :-

$$V_{o} + \hat{v}_{o} = \frac{I_{L} + \hat{i}_{L}}{sC_{f} + 1/R}$$
(3.13)

There is a pole in the voltage loop due to the power circuit:-

$$\omega_p = \frac{1}{RC_f} \tag{3.14}$$

The zero in the voltage loop due to the ESR (R_c) of the output capacitor is :-

$$\omega_z = \frac{1}{R_c C_f} \tag{3.15}$$

In terms of small-signal values the output voltage to inductor current from Eqn. 2.14 at frequencies above ω_p is approximated to :-

$$\frac{\hat{v}_o}{\hat{i}_L} \approx \frac{1}{sC_f} \tag{3.16}$$

This has a maximum of 90° phase lag and is independent of load.

The voltage loop PI controller is used to force the voltage loop to crossover 0dB at the required frequency. The transfer function is :-

$$PI(s) = K_{pv} + \frac{K_{iv}}{s}$$
 (3.17)

The position of the voltage loop crossover frequency is found by equating the voltage loop gain to 1 (0dB). The voltage loop gain includes the voltage loop feedback gain G_v and the closed loop gain of the current loop which at low frequencies can be approximated to a constant equal to the reciprocal of the current loop feedback gain $(1/G_i)$.

Above the power gain pole ω_p the proportional gain of the PI controller K_{pv} sets the crossover frequency :-

$$f_{cv} = \frac{G_v K_{pv}}{2 \pi G_i C_f}$$
(3.18)

The integral constant is found in a similar way to Eqn. 2.13 this gives a phase margin of 63°:-

$$K_{\mu\nu} = \pi K_{\mu\nu} f_{c\nu} \tag{3.19}$$

The crossover frequency should be set to about 5 -10 times lower than the current loop.

Sometimes the required crossover frequency of the voltage loop is less than the pole ω_p in the voltage loop due to the power circuit especially towards full load if a small filter capacitance is used. This makes it difficult to crossover on the pole of the capacitor and Eqn. 3.18 is no longer valid under all load conditions. In many cases a stable voltage loop can still be achieved, but the crossover frequency and phase margin of the voltage loop may vary with load and should be noted.

A second pole may be added to the voltage loop compensator to cancel the effect of the ESR zero.

3.6.4 Load Current Feedforward

The controller must be capable of tracking a 50Hz output voltage. At 50Hz the gain of the voltage loop is limited. Thus an error will occur between the output voltage reference and the actual output voltage. If the pole of the power circuit occurs above 50Hz then the error will vary with load, worse case being on full-load.

The use of load current feedforward can improve the steady-state and transient response of the voltage loop under all load conditions. Load current feedforward effectively bypasses the slow voltage feedback loop and provides a reference to the inner current loop directly from the measured output current. An additional feedforward signal of the output filter current may also be added to the current loop reference [41].

Fig. 3.11 shows the average current mode controller with the addition of load current feedforward and filter capacitor current feedforward. The filter capacitor current may be derived from the reference voltage if the capacitance is known.

3.6.5 Load Current Feedforward and Nonlinear Loads

UPS systems often have to supply nonlinear loads. Many such critical loads are computers. Typically the computer will contain a switched mode power supply (SMPS) which converts the line level ac supply voltage to a raw dc voltage at its front end using a conventional full-bridge rectifier with smoothing capacitor. This demands a current waveform with a high crest factor and can result in considerable clipping of the inverter output voltage if the voltage loop response of the inverter is poor.

It would be natural to use load current and filter capacitor current feedforward to improve the output voltage waveform when supplying a nonlinear load. It has been shown [40] that its use may cause the inverter control system to become highly unstable particularly

when the filter capacitor of the inverter is much smaller than the smoothing capacitor of the load, even when the control parameters are adjusted to take into account the extra capacitance present in the load. The basis of this instability will be described here.

To simplify the understanding one phase is considered. Fig. 3.12 shows a typical nonlinear load on one phase of the inverter. If the load is considered during conduction of the diode bridge rectifier then an equivalent lumped model is shown in Fig. 3.13. The measured quantities are shown for the inductor current, the output voltage and the load feedforward signal. The filter capacitor current feedforward signal has little effect on the stability and so is neglected.

Fig. 3.14 shows a simplified linearized control model block diagram of one phase of the inverter for a resistive load without the use of current feedforward. This may be compared with the model of Fig. 3.15 which includes the use of load current feedforward. The current loop feedback and load current feedforward have been lumped together to give a new equivalent current feedback loop. The model in Fig. 3.16 includes the smoothing capacitor C_s of Fig. 3.13.

The use of load current feedforward in Fig. 3.15 significantly alters the dynamics of the system. The dominant pole in the overall voltage loop of the power stage due to the filter capacitor and load resistance (Eqn. 3.14) is now moved to the origin. This boosts the gain of the voltage loop at low frequencies. Thus the use of load current feedforward provides better tracking under all load conditions at lower frequencies compared to a system without feedforward.

The addition of the smoothing capacitor in the load (Fig. 3.16) has a dramatic affect on the dynamics of the system. The crossover frequency of the power gain of the current loop was mainly due to the filter inductor (Eqn. 3.9) but in the new current loop is now reduced by a factor of $C_{f}/(C_{f}+C_{s})$. Thus the inner current loop bandwidth is reduced significantly. As the voltage loop relies on a current loop crossover frequency of 5-10

times that of the voltage loop a larger smoothing capacitor C_s can result in a phase margin in the voltage loop that is very small or possibly negative. It can also lead to a much reduced gain margin.

The simplest method to increase the stability of the voltage loop is to reduce the PI constants. Unfortunately this will reduce the gain in the voltage loop and worsen how well the system tracks the reference.

Fig. 3.13 shows that the inverter system may be in two possible states; when the diode bridge is conducting and the model of Fig. 3.15 is relevant, and when the diode bridge is not conducting and the model of Fig. 3.16 is relevant with $R=\infty$. Thus the inverter dynamics of the voltage loop may move from a system with a large phase margin to a system of a small (or negative) phase margin depending on whether the diode bridge is conducting or not.

Even though the system when the diode bridge is conducting may have a small phase margin or even be unstable, if the period the diode bridge is conducting is small enough (when the smoothing capacitor is being charged) then the overall system may not become unstable. When the diode bridge ceases to conduct and the system enters a stable period this may be enough to pull the output voltage back to tracking the reference .However, it is advisable to make sure the system always has a positive phase margin under all required load conditions.

The capacitance 'seen' on the output of the inverter is C_f when the diode bridge is not conducting and is the parallel combination C_f / C_s when the diode bridge is conducting (Fig. 3.13). The voltage loop PI parameters should be chosen for C_f alone as this is the worst case for the crossover frequency (highest crossover frequency).

To improve the stability of the system the PI parameter values can be reduced at the expense of the ability of the output voltage to track the reference. If a stability problem

still occurs with the use of load current feedforward then a filter capacitance C_f of similar size to that used in the load C_s could be used. However, this requires a much larger filter capacitor resulting in the need for uprated inverter switches to take the larger reactive current flowing in the inverter filter capacitor, and such a large filter capacitor would probably therefore be impractical.

3.6.6 The DQN Rotating Reference Frame

The d-q-n rotating reference frame transforms the three phase sinusoidal stationary voltage and current signals into dc equivalents. If it is used in the control of the inverter it can improve the steady state response of the inverter at the 50Hz frequency. This is achieved by effectively moving the 50Hz components down to dc in the frequency spectrum, thus taking advantage of the very high gain of the PI controllers at dc.

The d-q-n reference frame has been used to improve the response of the rectifier discussed in Section 2.5.6. The transformations are given between the stationary a-b-c and rotating d-q-n reference frames in Eqns. 2.38 - 2.41.

Fig. 3.17 shows a three phase inverter average current mode controller operating in the d-q-n reference frame without any current feedforward. The inductor currents $i_{a, b, c}$ and the output voltages $v_{a, b, c}$ are converted into the d-q-n quantities with the use of the transformation T(θ). The signals are converted back to stationary a-b-c quantities before the PWM stage. The same controller parameters may be used for the PI controllers as discussed in Section 3.6.3.

A dc quantity is set for the reference v_d^* which represents the peak of the required output voltage in the direct axis. The quadrature voltage reference v_q^* and the zero sequence voltage reference v_q^* are usually set to zero.

The effectiveness of using the rotating reference frame is greatest when the inverter is supplying a balanced, linear load. Under unbalanced loads a significant neutral current may flow. When this happens the demand in the current loop of the n-axis is higher, but the n-axis is not a dc quantity as with the d and q axes. Thus, the gain in the n-axis current loop is not theoretically infinite and a steady-state error may occur.

Under nonlinear loads harmonics of the fundamental 50Hz component exist in the output current. The d-q-n reference frame only moves the 50Hz component and not the harmonics to a dc quantity in the frequency spectrum. Thus, at the harmonic frequencies there is not an infinite gain provided by the PI controller and again a steady-state error may occur due to these harmonics and cause a distortion in the output voltage.

3.7 Filter Values

The use of the L-C output filter on each phase of the inverter will attenuate the output voltage ripple to required levels and is dependent upon the value of the L-C components and the switching frequency. Each phase of the inverter may be considered independently from one another due the neutral connection.

3.7.1 Filter Inductance

The size of filter inductance is chosen to limit the ripple current to required levels. Fig. 3.18 show an equivalent per phase circuit to calculate the ripple current The voltage supplied to the output filter is either $V_{dc}/2$ or $-V_{dc}/2$ for a fixed dc bus voltage.

During each switching cycle period T_s the inductor current will rise during the period DT_s and fall during the period (1-D) T_s where D is the on-state duty cycle. It will be assumed that the inductor current rises and falls linearly. Using V=Ldi/dt this leads to the equations :- 1.1

Four-Wire Inverters

$$\Delta i_{rise} = \frac{DT_s}{L_f} (V_{de}/2 - v_o) \tag{3.20}$$

$$\Delta i_{fall} = \frac{(1 - D)T_s}{L_f} (-V_{dc}/2 - v_o)$$
(3.21)

Over one switching period T_s the rise of current will approximate the fall in current $\Delta i_{rise} \approx -\Delta i_{fall}$ giving the duty cycle as :-

$$D = \frac{1}{2} + \frac{v_o}{V_{dc}}$$
(3.22)

By substituting Eqn. 3.22 into Eqn. 3.20 (or Eqn. 3.21) the ripple current is give by :-

$$\Delta i_{L} = \Delta i_{rise} \approx -\Delta i_{fall} = \frac{T_s}{V_{dc}L_f} (V_{dc}^2/4 - v_o^2) \qquad (pk-pk)$$
(3.23)

The worst case ripple occurs when $v_0=0$ and D=1/2 giving :-

$$\Delta i_{L|\max} = \frac{V_{dc}}{4f_s L_f} \qquad (pk-pk) \tag{3.24}$$

For the required maximum filter inductor current the value of filter inductance may be calculated using the above equation.

3.7.2 Filter Capacitance

Once the required filter inductance has been chosen the required filter capacitance may be chosen to limit the maximum output voltage ripple to the required level.

Fig. 3.19 shows the filter inductor current where it reaches its maximum at $v_0=0$. The points t_1 and t_2 occur when the current is zero and $(t_2 - t_1)=T_s/2$. To simplify the

calculation of the output voltage the ESR of the capacitor and the load resistance will be neglected giving an approximate output ripple voltage. The ripple current shown in Fig. 3.13 will produce a ripple voltage Δv_0 given below [42] :-

$$\Delta v_o = \frac{1}{C_f} \int_{t_1}^{t_2} i \, dt \tag{3.25}$$

The integral part of the above equation is equivalent to the shaded area A in Fig. 3.19 :-

$$A = \frac{\Delta i_{L|\max}}{2} \cdot \frac{T_s}{2} \cdot \frac{1}{2}$$
(3.26)

This gives a maximum output ripple voltage of :-

$$\Delta v_o = \frac{\Delta i_{L|\text{max}}}{8f_s C_f} \qquad (pk-pk) \tag{3.27}$$

The output filter capacitance is chosen for the required maximum output voltage ripple using the above equation.

3.8 Simulation Results

To demonstrate the performance of the inverter a number of SABER simulations have been run. The inverter control used is average current mode control and the use of feedforward and operating in the d-q-n reference frame is demonstrated.

The rating of the converter is 80kVA 0.8 power factor (p.f.). The switching frequency is 15kHz. The inverter is supplied from a 800V dc bus and the required output phase voltage is 230V at 50Hz.

3.8.1 Filter Parameters

The filter components are chosen using the equations in Section 3.7.

The peak of the rms of the output current for one phase is 164A. If the maximum filter inductor ripple current is limited to one-third of 164A then the required filter inductance is approximately 125μ H using Eqn. 3.24.

The peak of the rms of the output voltage is 325V. If the maximum output ripple voltage is limited to 2% then the required filter capacitance is approximately 70μ F using Eqn. 3.27.

The dc bus capacitors are chosen to be 10mF each to complement the four-wire rectifier of Chapter 2.

The power and filter components are summarized below :-

$P_{rating} = 80 kW$	$f_s = 15 kHz$	$V_{ph} = 230V$	$V_{dc} = 800V$
$C_{dc} = 10 mF$	$L_{f} = 125 \mu H$	$C_f = 70 \mu F$	

3.8.2 Control Parameters

The control parameters are chosen using the equations in Section 3.6.3.

The filter inductor current and output voltage are measured to provide the feedback signals to the controller. The feedback constant for the voltage loop is $G_v = 1/50$ and for current loop $G_i = 1/25$.

In a practical system the current loop crossover frequency is generally chosen to be no more than one-fifth of the switching frequency to ensure adequate phase margin is provided. With a switching frequency of 15kHz the current loop crossover frequency is

therefore chosen as 3kHz. The values for the filter parameters L_f and C_f previously determined result in a resonant frequency f_o of 1.7kHz in the power circuit. As f_o is relatively close to the desired crossover frequency this makes it very difficult to set the compensator parameters using Eqns. 3.11 and 3.12 to give exactly a 3kHz crossover frequency. Nonetheless, Eqns. 3.11 and 3.12 were used to calculate the PI parameters. The model of Fig. 3.14 was used to determine the resulting current loop crossover frequency as approximately 750Hz higher than desired. Although the higher current loop crossover frequency will result in a lower current loop phase margin it was considered worthwhile to investigate the performance of the system with the parameters so chosen.

The voltage loop crossover frequency is chosen to be 300Hz (10 times lower than that for the current loop). The required PI parameters for the voltage loop are found using Eqns. 3.18 and 3.19. Towards full-load the dominant pole in the voltage loop (Eqn. 3.14) is greater than 300Hz and as such Eqns. 3.18 and 3.19 become invalid. The voltage loop crossover frequency now varies with load. However, the model in Fig. 3.14 can be used to show that the voltage loop remains stable.

The control parameters are summarized below :-

G _i = 1/25	$G_v \approx 1/50$
$K_{pi} = 0.147$	$K_{pv} = 0.264$
$K_{ii} = 1388 \text{ rads}^{-1}$	$K_{iv} = 249 \text{ rads}^{-1}$

3.8.3 SABER Schematic

The inverter design is entered through the schematic editor Design Star. Fig. 3.20 shows the inverter power circuit schematic for one phase of the inverter. Small value resistors $(1m\Omega)$ are used to measure the filter inductor current and the output current. A small amount of resistance is used between the dc source and dc bus capacitance to help the simulator. Fig. 3.21 shows the inverter power circuit schematic for the full three phase

four-wire inverter. Ideal components are used and no deadperiod is introduced between switching times of the switches in one leg of the inverter.

Fig. 3.22 shows the basic average current mode controller for the power circuit in Fig. 3.20. Connections between the control and power circuit are made using 'same page connectors'. The triangular carrier wave has an amplitude of 1 per unit. The output of the current loop PI controller is limited to 0.99 per unit to prevent integrator wind-up and over modulation. A switch controller subcircuit provides two signals for the two switches; one simply the logical inverse of the other. 'Electrical to Control' blocks are used to transform between the analogue and control domains and have a gain of 1000 $(1/1m\Omega)$ when used to measure the current through the $1m\Omega$ resistors.

Fig. 3.23 shows the extended controller which includes load current feedforward and filter capacitor current feedforward. The filter capacitor current feedforward is derived from the reference voltage using a 1st order polynomial control block to represent the transfer function sC_f . A high frequency zero is required in this control block, however, to enable the simulation to work.

Fig. 3.24 show the d-q-n control schematic for the three phase four-wire inverter power circuit in Fig. 3.21. The measured output voltages and filter inductor currents are transformed to d-q-n values using two T subcircuits. The modulating signals are converted back to a-b-c values using the T^{-1} subcircuit. The feedback gains G_v and G_i are set inside the 'Electrical to Control' blocks.

3.8.4 Step-Load Change

The first simulation demonstrates a step-load change from no-load to full-load (21kW) placed on the output of one phase of the inverter shown in Fig. 3.20 using the basic control of Fig. 3.22. A resistor is used to load the converter to full-load R= 2.5Ω . After
25ms the load is switched in and switched out again at 45ms.

Fig. 3.28 shows the reference output voltage and the actual output voltage. The output voltage does not track the reference ideally and is worse on full-load due to the reduced gain at 50Hz in the voltage loop. The output voltage during no-load is slightly higher than the reference. This is due to an overshoot in the closed loop gain of the voltage loop just before the break frequency at around 50Hz due to a lack of damping and is can be seen in the Bode plot in Fig. 3.25 provided by using the approximate model in Fig. 3.14. The transient from full-load to no-load is worse as the current loop PI controller hits the limits of the modulator and the modulator enters a nonlinear period.

3.8.5 Nonlinear Load

The load on one phase of the inverter in Fig. 3.20 is replaced by a nonlinear load. The load chosen is a diode bridge rectifier and smoothing capacitor (Fig. 3.12) which may be typical on a computer UPS system. The current drawn by the diode bridge rectifier has a high crest factor load.

The load resistance of the bridge rectifier is set to 4.5 Ω . Typically the smoothing capacitor used in the front-end full-bridge rectifier of a SMPS will be 2 μ F/W. For a 21kW SMPS this works out to be about 42mF.

The PI parameters of the voltage loop are unchanged and despite the large smoothing capacitor used in the load the system is stable.

Fig. 3.29 - 3.31 show the waveforms of the inverter with a nonlinear load. The output voltage of the inverter (Fig. 3.29) does not track the reference well. The output voltage is clipped during the peaks of the inverter output current. The crest factor of the inverter output current (Fig. 3.30) is much lower than that obtained when the load is supplied

from a stiff ac voltage source and subsequently the average bridge rectifier output voltage is lower.

Although the inverter output voltage is distorted this may be acceptable for some systems as long as the output voltage of the bridge rectifier remains within permissible limits.

3.8.6 Step-Load Change with Current Feedforward

The control system is changed to that of Fig. 3.23 which includes the feedforward signals of load current and filter capacitor current in an attempt to improve the response of the system. The same step-load change is used as in Section 3.8.4.

Fig. 3.32 shows the reference and actual output voltage of the converter. If the waveforms are compared to those in Fig. 3.28 it can be seen that the steady-state response of the inverter under all load conditions has improved significantly and the transient response has also improved significantly.

The approximate model in Fig. 3.16 of the voltage loop which includes feedforward is used to provide the bode plot in Fig. 3.27 of the inverter during full-load. The Bode plot is virtually load independent and as such the output voltage of the inverter tracks the reference well under all load conditions.

3.8.7 Nonlinear Load with Current Feedforward

The load is changed to the nonlinear load in Section 3.8.5 but with the use of load current and filter capacitor current feedforward. The model in Fig. 3.16 is used to show that when the diode bridge rectifier is conducting the system becomes unstable and can be seen clearly in the Bode plot of Fig. 3.26. Although the diode bridge rectifier only conducts for a short period the overall system remains stable.

The results of the SABER simulation with the PI parameters as previously calculated gave unacceptable performance due to the erratic behaviour of the system. To reduce the instability during diode bridge rectifier conduction the voltage PI proportional constant K_{pv} is reduced by a factor of 2 and the integral constant by a factor of 4. Although the model of Fig. 3.16 was used to show that the system was unstable during diode bridge rectifier conduction the overall system remained stable and the erratic behaviour was no longer evident.

Fig. 3.33 - 3.35 show the waveforms of the inverter. The inverter output voltage now follows the reference much better than without feedforward. The disturbances at the peak of the voltage waveform are relatively small considering the high peaks of the inverter output current.

The inverter output current shown in Fig. 3.34 has a much higher crest factor and the average output voltage of the bridge rectifier is much higher. The inverter output is now comparable to a stiff ac voltage supply, i.e. the inverter has a low output impedance.

As previously stated during the period that the diode bridge rectifier is conducting the system is unstable and the system may become very erratic. To prevent the system going unstable during these periods a simulation has been run with the modulation process halted for a period symmetrical about the peaks of the output voltage waveform. During this period the switches are either connected to +400V or -400V without any PWM switching.

Figs. 3.36 - 3.38 show the waveforms of the inverter with the modulation process halted at the peaks of the output voltage waveform for a symmetrical period of 2ms. The control is now nonlinear. Fig. 3.36 shows the output voltage and the period where the modulation process is halted can be seen. After the nonlinear period the output voltage

recovers and normal modulation resumes. Fig. 3.37 shows the inverter output current. Fig. 3.38 shows the output voltage of the bridge rectifier which is now slightly larger.

3.8.8 Step-Load Change using the D-Q-N Reference Frame

To demonstrate the performance of the inverter in the d-q-n rotating reference frame a full three phase four-wire inverter is simulated. The power circuit is shown in Fig. 3.21 and its control in Fig. 3.24. The filter inductor currents and output voltages are transformed to d-q-n quantities. No current feedforward is used.

A 2.5 Ω resistor is used to load each phase of the inverter. The load is switched in at 25ms and switched out again at 45ms.

Fig. 3.39 shows the reference and output voltages. The output voltage tracks the reference well under all loads unlike the waveforms in Fig. 3.28 which operates in the ab-c reference frame. However the transient response is poor and from full-load to noload the controller enters a nonlinear period when the limits of the modulator are reached. Ringing occurs and is worsened as the three phases now interact with one another due to the nature of the d-q-n controller.

3.8.9 Steady-State Comparison of the D-Q-N and A-B-C Reference Frames

A number of simulations have been run to demonstrate the differences in the steady-state response of the four-wire inverter under no-load, full-load and unbalanced load conditions. The inverter output voltage waveforms generated in the time simulation are used to generate a Fourier analysis of the waveform using SABER's Fast Fourier Transform (FFT) utility of which the 50Hz component is of interest.

Under full-load conditions each phase is loaded with a 2.5Ω resistance. Under

unbalanced load the red and yellow phases are load with 2.5Ω resistors and the blue phase has no load. Table 3.1 lists the magnitude and phase of each phase of the output voltage of the inverter under the various conditions. Ideally this should be $325 \angle 0^\circ$, $325 \angle -120^\circ$ and $325 \angle +120^\circ$ for the red, yellow and blue phase respectively.

In the a-b-c reference frame the full-load and no-load results show that the output voltage does not track the reference ideally. On no-load the output voltage is higher than the reference due to overshoot in the closed loop gain around the 50Hz frequencies. On full-load the tracking is much worse due to the reduced gain in the voltage loop at 50Hz. However, in the d-q-n reference frame the output voltage tracks the reference very well.

Under unbalanced loads in the a-b-c reference frame the error in each phase of the output voltage depends on the load in the respective phase. In the d-q-n reference frame the system could not be made to track the references in a linear mode and hit the limits of the modulator in each phase frequently. This resulted in a highly distorted waveform and as such a comparison could not be made in Table 3.1. However, a rough shape of a sine wave was produced and from this it could be seen that the error in the 50Hz component of the output voltage is more evenly spread between phases, but the voltage error is still large compared to the balanced case.

The reason why an error exist in the unbalanced load condition and not the balanced condition when using the d-q-n reference frame is because a neutral current flows which has to be tracked by the n-axis compensators. Unlike the d-axis and q-axis the n-axis does not move the 50Hz components down to dc and as such cannot take advantage of the infinite gain at dc of the PI controller and thus a steady-state error exists.

A-B-C Reference Frame		D-Q-N Reference Frame	
	Full-Load		Full-Load
Va	211.3 ∠ -37.5°	V _a	324.6 ∠ 0°
V _b	211.2 ∠ -157.5°	V _b	324.4 ∠ -120°
V _c	211.1 ∠ 82.5°	V _c	324.6 ∠ 120°
	No-Load		No-Load
Va	353.8 ∠ -1.8°	V _a	324.9 ∠ 0°
V _b	353.8 ∠ -121.8°	V _b	324.9 ∠ -120°
V _c	353.8 ∠ 118.2°	V _c	324.9 ∠ 120°
	Unbalanced Load		Unbalanced Load
Va	211.0 ∠ -37.4°	V _a	?
V _b	211.2 ∠ -157.6°	V _b	?
V _c	354.3 ∠ 118.3°	V _c	?

Table 3.1 Comparison of the A-B-C and D-Q-N Reference Frames

3.9 Conclusions

This chapter has described the principle of power inversion. For unbalanced three phase loads a 4-wire inverter topology is required of which a split-capacitor bus has been chosen as the method of providing the neutral connection to complement the 4-wire rectifier in Chapter 2.

Various pulse width modulation techniques have been discussed. The natural sampling method gives a low distortion at the expense of increased switching losses.

The output voltage of the inverter may be controlled using voltage mode control or current mode control. Current mode control has an number of advantages over voltage

mode control.

The use of average current mode control has been demonstrated. The choice of compensator parameters has been described in detail. Due to the use of small filter capacitors the resonant frequency of the power circuit is high. If the resonant frequency is too close to the required current loop crossover frequency it can be very difficult to choose a compensator accurately.

The basic average current mode control is further extended to include filter capacitor current and load current feedforward to improve the steady-state and dynamic response of the inverter output voltage. If load current feedforward is used with nonlinear loads instability problems may occur due to a large capacitance in the load.

The choice of filter components has been described for the filter inductor and filter capacitor.

The inverter using average current mode control has been simulated under various conditions using SABER. Current feedforward has been shown to improve the steadystate and transient response of the inverter for linear and nonlinear loads. The use of load current feedforward with a nonlinear load may cause a period during which the system is highly unstable. However the system may recover during the stable period, but may result in erratic output voltages. Forcing the system to hit the limits of the modulator during the period when instability would otherwise occur will allow the system to remain stable.

An alternative to improve the steady-state response of the inverter is to operate the control in the d-q-n rotating reference frame. Operating in the d-q-n reference frame however does not improve the transient response and may cause a worse response due to the interaction between phases caused by the transformation. Under unbalanced load conditions the steady-state response of the inverter is worsened.



Fig. 3.1 Single Phase Bridge Inverter



Fig. 3.2 Single Phase Half-Bridge Inverter



Fig. 3.3 Three Phase Bridge Inverter



Fig. 3.4 Three Phase Inverter with Delta-Star Transformer



Fig. 3.5 Three Phase Inverter with Fourth Leg



Fig. 3.6 Three Phase Inverter with Centre-Tapped Capacitor



Fig. 3.7 Voltage Mode Controller for One Phase of the Inverter



Fig. 3.8 Average Linerized Model of the Buck Power Circuit



Fig. 3.9 Current Mode Controller for One Phase of the Inverter



Fig. 3.10 Average Current Mode Controller for One Phase of the Inverter



Fig. 3.11 Averge Current Mode Controller with Current Feedforward



Fig. 3.12 One Phase of the Inverter Loaded with a Diode Bridge Rectifier and Smoothing Capacitor

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Fig. 3.13 Equivalent Lumped Model of Circuit in Fig. 3.12



Fig. 3.14 Approximate Linearized Model of Inverter -Resistive Load



Fig. 3.15 Approximate Linearized Model of Inverter -Load Current Feedforward and Resistive/Capacitive Load



Fig. 3.16 Approximate Linearized Model of Inverter -Load Current Feedforward and Resistive Load



Fig. 3.17 Three Phase Inverter Average Current Mode Controller Operating in the DQN Reference Frame



Fig. 3.18 Equivalent Per Phase Circuit of Inverter Output Filter



Fig. 3.19 Inverter Filter Inductor Current at its Maximum



Fig. 3.20 Inverter SABER Power Circuit Schematic (One Phase)



Fig. 3.21 Inverter SABER Power Circuit Schematic (Three Phase)



Schematic









Fig. 3.25 Approximate Closed Voltage Loop Bode Plot of Inverter for a Resistive Load





Four-Wire Inverters



Fig. 3.27 Approximate Open Voltage Loop Bode Plot for a Resisitve Load with Load Current Feedforward

Four-Wire Inverters



Fig. 3.28 Reference and Output Voltages - Step-Load Change



Fig. 3.29 Inverter Reference and Output Voltages - Nonlinear Load



Fig. 3.30 Inverter Output Current - Nonlinear Load



Fig. 3.31 Bridge Rectifier Output Voltage - Nonlinear Load





Fig. 3.33 Reference and Output Voltage - Nonlinear Load with Current Feedforward







Four-Wire Inverters



Fig. 3.37 Inverter Output Current -Nonlinear Load with Current Feedforward and Nonlinear Control



The Transfomerless Four-Wire AC-DC-AC Converter for UPS Applications

4.1 Introduction

A new transformerless four-wire ac-dc-ac converter is presented in this chapter. The converter is the combination of the four-wire power factor corrected rectifier described in Chapter 2 and the four-wire inverter described in Chapter 3. The main application of the ac-dc-ac converter is for transformerless three phase uninterruptible power supplies.

The interaction between the rectifier and the inverter will be discussed including the harmonics in the system. Additional measures are required to ensure the dc bus centre-point remains balanced for practical systems and solutions are given.

In UPS systems batteries are required to maintain the required output during supply failures and methods of interfacing the batteries to the ac-dc-ac converter are discussed.

Finally, simulation results demonstrate the operation of the ac-dc-ac converter.

4.2 A New Four-Wire AC-DC-AC Converter

The transformerless four-wire ac-dc-ac converter [24] is shown in Fig. 4.1 which includes a front-end L-C filter on the rectifier. The supply neutral is connected to the load neutral, thus the load is at the same potential as the supply. As the star point (neutral point) of the utility is usually connected to earth, then a direct current path to earth is available should any faults occur in the load.

The load may operate with significant unbalance which will result in inverter neutral currents flowing. This current has a preferential path into the centre point of the dc bus. None of the inverter neutral current returns to the utility neutral. The utility neutral current will be zero as the rectifier is controlled to draw no neutral current (apart from a small amount of high frequency switching ripple).

The use of a transformer in some ac-dc-ac converters allows the voltage in the system to be stepped up to allow for losses in the system. Even though no transformer is present in this system this is not a problem as the rectifier is used to step-up the voltage to the dc bus and the inverter is used to step-down the required voltage to the load.

4.3 Harmonics

In Chapters 2 a rectifier has been described with a purely resistive load, and in Chapter 3 the inverter has been described when supplied by a stiff dc source. Connecting the two together will cause interactions between the two systems. The most profound effect being that of harmonic currents and power flowing in the inverter, to the dc bus and then the rectifier.

4.3.1 Definitions of Power

In an ac system the **real** or **active** power flow is that associated with a current that is in phase with the voltage, say a resistive load. For a balanced three phase system the total active power flow is constant with time, i.e. is time invariant. The **imaginary** or **reactive** power flow is that associated with a current that is 90° out of phase with the voltage, say an inductive load (lagging power) or a capacitive load (leading power). Again, for a balanced three phase system the total reactive power flow is time invariant and equates to zero. However, the three phase source must supply the reactive current for each phase of the load.

The cyclic or pulsating power flow is associated with either a single phase or an unbalanced three phase system. The time variant part of the power in an unbalanced system pulsates at twice the line frequency. Other factors that may cause power pulsations at other frequencies are associated with harmonic currents flowing in the load due to nonlinear loads or harmonics in the supply voltage.

4.3.2 Power Flow in the AC-DC-AC Converter

The flow of power in the ac-dc-ac converter is shown in Fig. 4.2. Ideally, the utility supplies only an active, non-cyclic power, i.e. the ac-dc-ac converter is 'seen' as a resistive load to the utility.

The load on the inverter may demand active, reactive and cyclic power. The utility supplies the non-cyclic active power to the load. The required non-cyclic reactive power is supplied by the inverter itself, i.e. the reactive power circulates around the inverter and sums to zero. The cyclic power is supplied from the dc bus capacitors and results in a voltage ripple on the dc bus.

The supply filter and load filter also demand reactive power and this circulates around the rectifier and inverter respectively.

4.3.3 Required DC Bus Capacitance

To enable the correct flow of power as shown in Fig. 4.2 the dc bus capacitors must be chosen large enough to limit the voltage ripple on the dc bus (due to cyclic power) to an acceptable level and hold up the dc bus voltage during a transient load. The controller of the rectifier must be set not to allow cyclic power to be drawn from the utility.

One of the main flows of cyclic power occurs during an unbalanced load. This results in a 100Hz ripple voltage occurring on the dc bus. One method to limit the dc bus ripple voltage without using large dc bus capacitors is to balance the instantaneous power from the utility to that of the instantaneous power of the load [43]. Whilst this may be acceptable for a balanced linear load power, such as that demanded by an induction motor, it is not acceptable where the load is unbalanced or nonlinear as this would cause harmonic currents to flow in the utility and thus large dc bus capacitors are required.

The amplitude of the ripple voltage may be calculated by balancing the output power of the inverter with that of the dc bus. Fig. 4.3 shows an equivalent circuit of the dc bus capacitors where the two dc bus capacitors are lumped as one so that $C=C_{dc}/2$. The output power of the inverter for a linear load is :-

$$P_{i}(t) = \frac{V_{o}}{2} [I_{at} + I_{bi} + I_{ci} - I_{ni} \cos(2\omega t + \alpha)]$$
(4.1)

where α is the phase angle of the load neutral current relative to the red phase supply voltage. By equating the power in the dc bus to the inverter output power and neglecting the relatively small dc bus ripple voltage in the calculation of dc bus power then the instantaneous inverter dc input current is given by :-

$$i_{dc}(t) = I_{dc} - i_{r}(t) = \frac{V_{o}}{2V_{dc}}[I_{dl} + I_{bl} + I_{cl} - I_{nl}\cos(2\omega t + \alpha)]$$
(4.2)

Assuming the non-cyclic active power of the inverter is supplied by the rectifier and the

cyclic power is supplied by the dc bus capacitors then the capacitor ripple current is :-

$$i_r(t) = \frac{V_o I_{nt}}{2V_{dc}} \cos(2\omega t + \alpha)$$
(4.3)

and the ripple voltage is :-

$$v_r(t) = \frac{1}{C} \int i_r(t) dt = \frac{V_o I_{nl}}{4\omega C V_{dc}} \sin(2\omega t + \alpha)$$
(4.4)

Therefore the peak ripple voltage across the dc bus with C replaced by $C_{dc}/2$ is :-

$$V_{r} = \frac{V_{o}I_{ni}}{2\omega V_{dc}C_{dc}}$$
(4.5)

During an unbalanced load a 50Hz current flows through the dc bus capacitor connected to the positive rail and the negative rail. This results in a 50Hz voltage ripple component in each bus capacitor. Nominally, the two dc bus capacitances are of the same value resulting in equal but opposite 50Hz ripple voltages which cancel when measuring across the dc bus. If a difference exists between the capacitances of the positive and negative rails then the ripple voltages will not cancel exactly resulting in a small 50Hz ripple voltage component across the dc bus.

A nonlinear load on the inverter will draw cyclic powers at various frequencies resulting in ripple voltages at various frequencies on the dc bus. Another source of cyclic power will be the utility if the supply voltage is unbalanced or contains harmonics again resulting in ripple voltages on the dc bus.

4.3.4 Supply Line Harmonic Distortion

Ideally there should be no harmonic currents drawn from the utility. If there is a ripple voltage on the dc bus then this may result in a small amount of harmonic current being

drawn from the supply. This is due to the rectifier voltage loop compensator amplifying the voltage error including the ripple voltage which, in the case of the rectifier control operating in the d-q-n reference frame, results in a current demand in the d-axis of not only a dc quantity but harmonics also.

The neutral current drawn from the supply will still be zero despite there being harmonics in the line currents as each phase has the same amplitude current reference.

For the case of the unbalanced load the 100Hz dc bus voltage ripple of Eqn. 4.5 is fed back to the voltage loop of the rectifier controller. The feedback signal due to this ripple voltage is :-

$$V_{\alpha} = G_{\nu} V_{\nu} \sin(2\omega t + \alpha) \tag{4.6}$$

where G_v is the feedback gain of the voltage loop of the rectifier. The gain of the PI controller in the rectifier at the second-harmonic frequency 2ω is :-

$$G_{PI} = \sqrt{K_p^2 + \frac{K_i^2}{(2\omega)^2}}$$
(4.7)

Multiplying the feedback signal by the gain of the PI controller and also by the sine wave template (sin ωt in the red phase) and dividing by the current loop feedback gain G_i of the rectifier then the current reference in the red phase due to the voltage ripple is :-

$$i_{ref}(t) = \frac{G_{PI}G_{v}V_{r}}{G_{i}}\sin(2\omega t + \alpha + \beta) \sin\omega t$$

$$= \frac{G_{PI}G_{v}V_{r}}{2G_{i}}[\sin(3\omega t + \alpha + \beta) - \sin(\omega t + \alpha + \beta)]$$
(4.8)

where β is the phase lag of the PI controller. Assuming the rectifier can follow the reference exactly then the red phase current contains a fundamental component of current which is out of phase with the red phase voltage and a third-harmonic component and

similarly in the other two phases. The third-harmonic current in the supply is :-

$$I_{s3} = \frac{V_r G_v}{2G_i} \sqrt{K_p^2 + \frac{K_i^2}{4\omega^2}}$$
(4.9)

Any other frequency f of ripple voltage on the dc bus will result in two harmonic currents in the supply of frequency $f \pm 50Hz$.

To reduce the effects of dc bus harmonics voltages resulting in supply harmonics, a notch filter may be placed in the rectifier voltage feedback path or the bandwidth of the rectifier voltage loop may be lowered to minimize the harmonic content of the supply currents. Reducing the voltage loop bandwidth of the rectifier will impair the transient response of the rectifier.

4.4 DC Bus Centre-Point Balancing

The positive and negative rails of the dc bus should nominally stay at the same but opposite potential relative to the centre-point. As the ac-dc-ac converter has a symmetry about the centre-point, in theory the two dc bus rail voltages should be the same.

In practice, however, the converters may produce unsymmetrical effects such as differing deadbands in the switches, differing voltage measurement resistances across each rail for the rectifier feedback signals, and a dc component of current may be drawn from the inverter. This will lead to more current being drawn from one of the dc bus capacitors compared to the other. Even if this difference is small this would lead to a rapid increase in one dc bus voltage and rapid decrease in the other until it is beyond the operating bounds of both the rectifier and inverter.

To maintain a balance between the two dc bus voltages two solutions are proposed :-

- an additional control circuit for the rectifier
- an additional switching leg is added to the power circuit

4.4.1 Centre-Point Balancing using Additional Control

A simple solution to balancing the dc bus voltage is by using an additional control circuit. The difference between the two dc bus voltages is measured and passed through a compensator to form a dc current reference. This is then added to each of the three current references of the rectifier controller to demand a small amount of dc current from the supply to correct the voltage imbalance.

In the case of the rectifier control being operated in the d-q-n reference frame the dc current reference cannot be added to the d-axis current reference as a dc signal represents a 50Hz component. Instead the dc current reference may be used for the n-axis reference which is a stationary quantity. This will demand equal amounts of dc current from each line of the three phase supplies and a small amount of dc neutral current will flow.

Fig. 4.4 shows the additional control required. The dc bus voltage difference error signal is passed through a low pass filter (LPF) and compared to a reference of zero. The gain of the LPF is kept low as only a small amount of dc current should be drawn from the utility. A limiter is also used to guarantee only a small dc current is drawn. The zero of the LPF is set to below the utility frequency to prevent any harmonics on the dc bus causing harmonic currents to flow in the neutral.

Although this method provides a simple and cheap solution to balancing the dc bus it is only suitable for very small differences in current being drawn from the two dc bus capacitors so that only very small amounts of dc current is drawn from the supply.

4.4.2 Centre-Point Balancing using an Extra-Leg of Switches

An alternative to drawing a small amount of dc from the utility to balance the dc bus is to redistribute the energy between the positive rail capacitor and the negative rail capacitor. Fig. 4.5 shows the additional leg of switches connected to the centre-point via an inductor. The inductor provides intermediate energy storage when distributing energy between the two dc bus capacitors.

The two switches are switched alternatively using a PWM switching pattern with the proviso of a deadband when considering real switches to prevent a short circuit across the bus. The balancing circuit may be considered as a buck-type configuration.

The simplest method of control would be open-loop switching with a duty cycle of 1/2 thus setting up an average potential at the centre-point of the switches of half the dc bus voltage. To provide a better response to voltage differences and a well damped system, and take into account any unsymmetrical components in the switching pattern of the extra leg, such as deadtimes, a closed-loop system should be used.

Two fundamental methods of closed-loop control of the additional switches are voltage mode control and current mode control both of which are independent of the rectifier and inverter controllers. The power dynamics of the controller depend upon the dc bus capacitors and the inductor L.

4.4.2.1 Voltage Mode Control

Fig. 4.6 shows a voltage mode controller. The difference voltage is measured and compared to the required reference of zero. If the crossover frequency of the loop is set above the resonance frequency of the dc bus capacitors and inductor L, then the phase lag of the power gain can reach a maximum of -180°. Thus a lag-lead compensator is

required so that the phase margin at the crossover frequency can be increased. The output of the compensator is compared to a triangular carrier wave to produce the required pulse width modulation pulses.

4.4.2.2 Current Mode Control

The use of a current mode controller has a number of advantages over the voltage mode controller. The compensators in the current loop and voltage loop are simpler to choose as the current loop power gain reaches a maximum of -90° phase lag due to the inductor above the resonance frequency and the voltage loop power gain also reaches a maximum of -90° phase lag due to the dc bus capacitors. The current in the inductor L may also be limited by the controller. The disadvantage is that the inductor current L must be measured.

Fig. 4.7 shows the current mode controller. The difference voltage is measured and compared to the reference of zero. The voltage error signal is then passed through a PI compensator. This then forms the inductor current reference. The reference is compared to the actual measured inductor current. The current error signal is passed through a PI controller and the output compared with a triangular carrier wave to produce the PWM waveforms.

Above the resonant frequency of the centre-point balancing circuit the small-signal power gain of the current loop is dependent upon the inductor L and is approximated to :-

$$\frac{\hat{i}_{L}}{\hat{d}} \approx \frac{V_{dc}}{2j\omega L} \tag{4.10}$$

The PI compensator is used to roll-off the gain at the required frequency, the Laplace function is given as :-

$$PI(s) = K_{pi} + \frac{K_{ii}}{s}$$

$$(4.11)$$

The current loop crossover frequency can be calculated in a similar manner as described in Section 2.5.4.1 and is given as :-

$$f_{cl} = \frac{V_{dc}G_{l}K_{pl}}{4\pi L}$$
(4.12)

where G_i is the feedback gain of the measured inductor current. For a phase margin of 63° the integral constant is given as :-

$$K_{ii} = \pi K_{pi} f_{ci} \tag{4.13}$$

Eqns. 2.19 - 2.22 from Chapter 2 which deal with the modulation process are also valid here.

The small-signal power gain of the voltage loop is dependant on the dc bus capacitors and there is no dominant zero at low frequencies. At low frequencies the closed current loop gain is approximated to $1/G_i$. The small-signal response is approximated to :-

$$\frac{\hat{\mathbf{v}}_o}{\hat{\mathbf{i}}} = \frac{1}{j\omega C_{ac}G_i} \tag{4.14}$$

The PI compensator for the voltage loop is given as :- .

$$PI(s) = K_{pv} + \frac{K_{iv}}{s}$$
 (4.15)

The voltage loop 0dB crossover frequency is found by multiplying Eqn. 4.14 by the PI proportional constant K_{pv} and the voltage loop feedback constant G_v :-

$$f_{cv} = \frac{G_v K_{pv}}{2\pi G_v C_{dc}}$$
(4.16)

The integral constant is given similar to Eqn. 4.13 :-

$$K_{\mu\nu} = \pi K_{\mu\nu} f_{c\nu} \tag{4.17}$$

The voltage loop crossover frequency is chosen to be 5 - 10 times lower than the current loop crossover frequency.

Further advantages of the balancing circuit is that it may be used to balance harmonic difference voltages rather than just the dc component. These voltage components may occur if the dc bus capacitances differ. Also a considerable amount of dc current could now be allowed to flow in the output of the inverter.

The current rating of the switches may be much lower than those used in the rectifier and inverter circuits, and is dependent on how much unsymmetrical components of current are allowed to flow. The switching frequency may also be lower especially if only dc components of unbalanced voltage are compensated for. However, a higher switching frequency is advantageous in minimizing the inductor L switching ripple current.

4.4.2.3 Use of the Centre-Point Balancing Circuit to Remove Voltage Ripple

In theory it should be possible to use the centre-point balancing circuit to remove the overall bus voltage ripple and thus reduce the required dc bus capacitance. However, this method simply moves the problem of supplying cyclic power from the capacitors to the balancing circuit inductor and requires an inductor with a very large current rating.

4.5 Connection of the Battery Backup

To complete the UPS system a battery backup is required to hold up the dc bus voltage for a specified period of time during a blackout of the supply. Details of battery
technology [9] are beyond the scope of this thesis and this section therefore only deals with the interconnection of the batteries to the dc bus.

4.5.1 Direct Connection to the DC Bus

The simplest method is to connect the battery to the dc bus when battery backup is required. This can be achieved by use of a thyristor as shown in Fig. 4.8. A battery charger is used to charge the battery from the utility during normal operation.

For a transformerless application the dc bus voltage is about 800V. This is a larger voltage than that predominately used for batteries of around 400 - 500V [44] and poses a safety issue at higher voltages.

4.52 Connection to the DC Bus via a DC-DC Converter

To allow the relatively low voltage batteries to feed the higher voltage dc bus a dc-dc converter in a boost configuration may be used. Fig. 4.9 shows the circuit configuration using a buck and boost converter. The battery voltage is less than the dc bus voltage. Either switch S1 or S2 is used and is switched using a PWM switch pattern at high frequency.

Switch S2 allows the circuit configuration to be used as a boost circuit when the battery backup is required. This also has the advantage of maintaining a constant dc bus voltage even when the voltage of the batteries drops during discharge.

Switch S1 allows the circuit configuration to be used as a buck circuit during normal operation to allow the battery to be charged from the dc bus.

The obvious control technique is to use a current mode controller as this provides better control over the current in to or out from the battery via the inductor.

An alternative configuration is to connected the centre point of the batteries to the centrepoint of the dc bus and use two buck and boost converters as shown in Fig. 4.10. This provides the advantages of requiring switches with a lower voltage rating, connection of the batteries around the centre-point of the dc bus (neutral) and individual control of the positive and negative rail voltages. The obvious disadvantages are the requirement of extra switches and control circuits.

4.5.3 Connection Via the Rectifier Front-End

Another method is to connected the battery via the rectifier front-end as an alternative to the utility when there is a blackout. An additional inverter provides an alternating voltage from the battery to the rectifier [45] as shown in Fig. 4.11. The additional inverter provides a square voltage at the utility frequency. This has the advantage of requiring low frequency switches and simple control for this inverter.

The rectifier operates in the same way as if being supplied by the utility. However, the shape of the input current is not limited to a sine wave when being supplied from the battery and the rectifier can be made to draw a trapezoid current to limit the peak input current especially if the battery voltage falls considerably below that of the nominal utility voltage. This allows smaller rectifier boost inductors to be used [45].

4.6 Simulation Results

A number of SABER simulations have been run to demonstrate the performance of the four-wire ac-dc-ac converter. The converter chosen is a combination of the rectifier

simulated in Section 2.7 and the inverter of Section 3.8. The controller used for the rectifier is the same as that shown in Fig. 2.29 operating in the d-q-n reference frame and for the inverter, the controller is the same as shown in Fig. 3.20 operating in the a-b-c reference frame with output current and capacitor filter current feedforward.

Fig. 4.12 shows the SABER schematic for the complete ac-dc-ac converter and includes a centre-point balancing circuit. The schematic of the controller for the balancing circuit is shown in Fig. 4.13.

The ac-dc-ac converter is rated at 80kVA, 0.8p.f. and the switching frequency of the rectifier, inverter and centre-point balancing circuit is 15kHz as explained in Chapter 2 and Chapter 3. The input and output phase voltage is 230V at 50Hz. The dc bus capacitance is 10mF per rail and the centre-point balancing circuit inductor L is 125μ H.

4.6.1 Filter Parameters

The filter parameters are the same as chosen in Sections 2.7 and 3.8 and are summarized below :-

Rectifier: $L_{fr} = 25\mu H$ $C_{fr} = 85\mu F$ $L_{boost} = 122\mu H$ Inverter: $L_{fi} = 125\mu H$ $C_{fi} = 70 \,\mu F$

4.62 Control Parameters

The control parameters for the rectifier and inverter are the same as chosen in Sections 2.7 and 3.8 and are summarized below :-

Chapter 4	·		Four-Wire AC-DC-AC Converter
Rectifier:	$G_i = 1/25$	$k_{pi} = 0.144$	$k_{ii} = 1357 rads^{-1}$
	$G_v = 1/100$	$k_{pv} = 62$	$k_{iv} = 58.4 \text{ krads}^{-1}$
	$\omega_{zesr} = 5 \text{ krads}^{-1}$	$i_q^* = 0.347$	
Inverter:	$G_i = 1/25$	$k_{pi} = 0.147$	$k_{ii} = 1388 \text{ rads}^{-1}$
	$G_v = 1/50$	$k_{pv} = 0.264$	$k_{iv} = 249 \text{ rads}^{-1}$

The control parameters of the current mode controller for the centre-point balancing (CPB) circuit are chosen for a current loop crossover frequency of 3kHz and a voltage loop crossover frequency of 300Hz using Eqns. 4.12, 4.13, 4.16 and 4.17. These are summarized below :-

CPB:
$$G_i = 1/10$$
 $k_{pi} = 0.059$ $k_{ii} = 555.17 \text{ rads}^{-1}$
 $G_v = 1/100$ $k_{pv} = 188.50$ $k_{iv} = 177.65 \text{ krads}^{-1}$

4.6.3 Step-Load Change

The first simulation is a resistive step-load change placed on the output of the inverter. The ac-dc-ac converter is simulated without the centre-point balancing circuit. The load changes from no-load to full-load (21kW per phase) at 25ms and from full-load back to no-load at 45ms. Figures 4.14 - 4.16 show the voltage and current waveforms of the converter.

Fig. 4.14 shows the three phase supply phase voltages, the input currents and neutral current. No low order harmonic currents are present in the supply neutral. Fig. 4.15 shows the output of the inverter in terms of the load voltages, load currents and load neutral current. Fig. 4.16 shows the dc bus voltage.

4.6.4 Unbalanced Load

The load on the output of the inverter is replaced by a resistive unbalanced load. The load on the red phase is set at half load (10.5kW) and on the yellow and blue phases set at full-load (21kW). Figures 4.17 - 4.19 show the converter waveforms.

Fig. 4.17 shows the three phase supply voltages, the input currents and neutral current. It can be seen that the input currents are heavily distorted, although no low order harmonics are present in the supply neutral. Fig. 4.18 shows the inverter output load voltages, currents and load neutral current. Fig. 4.19 shows the dc bus voltage which contains a small amount of 100Hz ripple. A Fast Fourier Transform (FFT) using SABER performed on the voltage waveform gives a 100Hz component of 1.19V_{pk}.

The ripple voltage on the dc bus is due to the unbalanced load caused by the demand for cyclic power by the inverter. This ripple voltage in turn is fed back via the rectifier voltage loop and becomes a reference for the rectifier current controllers. This results in a third harmonic and an additional out of phase fundamental component in each of the supply currents.

Using Eqn. 4.5 to predict how much 100Hz component of voltage is present on the dc bus gives a value of $5.26V_{pk}$. However, this equation assumes that the rectifier draws only active current which in this simulation it is clearly not. The rectifier is supplying part of the cyclic power and is reducing the 100Hz ripple on the dc bus.

The third harmonic current in the supply due to an unbalanced load is predicted by Eqn. 4.9 which gives a value of $16.6A_{pk}$. An FFT performed on the supply current waveforms gives a value of $16.3A_{pk}$ which is comparable.

4.6.5 Unbalanced Load with Lower Bandwidth Rectifier Voltage Controller

To reduce the supply current harmonics the bandwidth of the voltage controller of the rectifier is reduced. The new voltage loop crossover frequency is chosen as 50Hz. The corresponding PI constants of the rectifier voltage loop controller are $K_{pv} = 10.33$ and $K_{pi} = 1622$ rads⁻¹. Figures 4.20 - 4.22 show the new voltage and current waveforms.

Fig. 4.20 shows the three phase input voltage and current waveforms, and the supply neutral current. The distortion of the input currents is less with the lower bandwidth controller. Fig. 4.21 shows the output load voltages, currents and load neutral current. Fig. 2.22 shows the dc bus voltage which now has a larger 100Hz ripple. An FFT shows this to be $5.43V_{pk}$ which is closer to that given by Eqn. 4.5 of $5.26V_{pk}$.

An FFT of the input current gives a the third harmonic component of the $7.1A_{pk}$ which is comparable to that given by Eqn. 4.9 of $7.2A_{pk}$.

4.6.6 DC Load

The ac-dc-ac converter is simulated with a load that has a dc component of current present. For this simulation the centre-point balancing circuit is included. Each phase is loaded with a 4Ω resistance in parallel with a half-bridge rectifier with a 20Ω resistance on the output. This corresponds to a dc current in each phase of the inverter output of $5.18A_{pk}$ and a dc current in the load neutral of $15.54A_{pk}$. Figures 4.23 - 4.28 show the voltage and current waveforms of the converter.

Fig. 4.23 shows the three phase input voltage and current waveforms, and the supply neutral current which has no low order harmonic components. Fig. 4.24 shows the inverter output load voltages, current and neutral current. A small dc component can be seen in the load neutral current.

Fig. 4.25 shows the differential dc bus voltage and Fig. 4.26 and 4.27 shows the dc bus voltage of the positive and negative rails respectively with respect to the neutral connection. Fig. 4.28 shows the inductor current of the balancing circuit, the dc component of which is equal to the dc component of the load neutral current. The balancing circuit has maintained a balanced dc bus even with a considerable dc component of output current.

4.7 Conclusions

This chapter has presented a new transformerless four-wire ac-dc-ac converter. The supply neutral and load neutral are connected together.

Ideally the utility can be made to supply only active power to the converter even when the load on the inverter may be unbalanced or nonlinear. The dc bus capacitance must be chosen large enough to absorb the cyclic power of the load without causing excessive dc bus ripple voltage. The rectifier voltage control loop must not allow a current reference to be generated that contains considerable harmonics. Even if the supply line current does contain harmonics the supply neutral current remains effectively zero.

In practice a method must be used to maintain a balance between the positive and negative rail voltages, an unbalance between these voltages may occur due to unsymmetrical effects of the converters such as the switching patterns or because a dc component of current is drawn by the load. Two solutions have been proposed. These are an additional control for the rectifier which is suitable for small unsymmetrical components and is a low cost solution, and an additional switching leg connected across the dc bus which is suitable for correcting large dc components of load current. The simpler method of control would be suitable for many applications.

As the main application of the ac-dc-ac converter is for UPS's a battery backup is

Four-Wire AC-DC-AC Converter

required. Simply connecting the battery straight to the dc bus is not feasible at the high dc bus voltages this converter operates at. One alternative method is to use a dc-dc converter to step the battery voltage up to the required bus voltage. This also has the advantage of providing dc bus regulation during the period of power being supplied by the battery. Another alternative is to connect the battery to the front-end rectifier via an additional three-phase inverter which switches at the utility frequency. The rectifier provides the step-up or boost of voltage required. This method does not require an additional high frequency converter.

Simulation results have demonstrated the performance of the four-wire ac-dc-ac converter. During a step-load change or unbalanced load no low order neutral current flows in the utility.

An unbalanced load has been shown to indirectly cause current harmonics to flow in the utility due to ripple on the dc bus. The harmonics can be reduced by reducing the voltage loop bandwidth of the rectifier. This however will impair the transient response of the rectifier. A notch filter may be used in the rectifier voltage feedback loop, but in practice there may be a number of troublesome frequencies to remove and will also impair the transient response of the rectifier. A combination of lower voltage loop bandwidth and the use of a notch filter to remove the most troublesome frequency from the rectifier voltage feedback path (from the dc bus voltage) may be the best solution.

Simulation results have also demonstrated the use of the additional leg of switches for use as a centre-point balancing circuit for a load containing a large dc component of current.











Fig. 4.3 Equivalent Circuit of DC Bus



Fig. 4.4 DC Bus Balancing Controller Diagram



Fig. 4.5 DC Bus Balancing Circuit



Fig. 4.6 Balancing Circuit Voltage Mode Controller



Fig. 4.7 Balancing Circuit Current Mode Controller



Fig. 4.8 Direct Battery Connection to DC Bus



Fig. 4.9 Battery Connection via DC-DC Converter



Fig. 4.10 Battery Connection via DC-DC Converter with Connection to Centre-Point



Fig. 4.11 Battery Connection Through Rectifier Front-End via a Three-Phase Inverter



Fig. 4.12 Four-Wire AC-DC-AC Converter - SABER Schematic

Chapter 4





Cudep

Four-Wire AC-DC-AC Converter





Fig. 4.14 Supply Voltages, Supply Currents and Supply Neutral Current -Step-Load Change



Fig. 4.15 Output Voltages. Output Currents and Output Neutral Current -Step-Load Change



Step-Load Change

Four-Wire AC-DC-AC Converter





Fig. 4.17 Supply Voltages, Supply Currents, Supply Neutral Current -Unbalanced Load



Fig. 4.18 Output Voltages, Output Currents, Output Neutral Current -Unbalanced Load



Fig. 4.19 DC Bus Voltage - Unbalanced Load



Fig. 4.20 Supply Voltages, Supply Currents and Supply Neutral Current -Unbalanced Load (Low Bandwidth Rectifer Controller)



Fig. 4.21 Output Voltages, Output Currents and Output Neutral Current -Unbalanced Load (Low Bandwidth Rectifier Controller)



Fig. 4.22 DC Bus Voltage -Unbalanced Load (Low Bandwidth Rectifier Controller)

Four-Wire AC-DC-AC Converter



Chapter 4

Fig. 4.23 Supply Voltages, Supply Currents and Supply Neutral Current -DC Load using Half-Bridge Rectifier



Fig. 4.24 Output Voltages, Output Currents and Output Neutral Current -DC Load using Half-Bridge Rectifier







DC Load using Half-Bridge Rectifier

A Practical Implementation of the Four-Wire Power Factor Corrected Boost Rectifier

5.1 Introduction

This chapter describes a practical implementation of the four-wire power factor corrected boost rectifier. The prototype built is rated at 1.5kW suitable for connection to a 400V three phase four-wire supply with a dc bus voltage of 800V. The controller chosen is an analogue current mode controller operating in the d-q-n rotating reference frame as described in Chapter 2.

The design for the power stage of the circuit and the controller are described in detail.

A resistive load is used to test the performance of the rectifier. Bidirectional power flow is demonstrated by connecting a dc voltage source in the load. Experimental results are given and are compared with equivalent SABER simulation results.

5.2 Power Circuit Design

The power circuit consists of the six switches with anti-parallel diodes, the three boost inductors, the dc bus capacitors and the front-end L-C filters (Fig. 5.1). Hall effect transducers are used to measure the three boost inductor currents and the two dc bus voltages.

The power circuit, including the transducer measurement board, is mounted in an earthed

metal enclosure and provides electrical protection from the high voltages and helps to reduce electromagnetic interference emitted from the power circuit.

5.2.1 Soft-Start of the Rectifier

As the rectifier is of a boost type configuration its operating conditions requires a dc bus voltage greater than the peak of the utility (Eqn. 2.8). Initially, the dc bus voltage is zero and requires a method of soft-starting to limit the high inrush current that would otherwise occur in charging the dc bus capacitors.

The simplest method of soft-start is to use resistors in series in each phase of the supply. A resistance of 50Ω is used in each phase. The rectifier is used as a conventional three phase bridge rectifier to charge up the dc bus capacitors on no load. During this period, a small amount of neutral current will flow. The resistors are then shorted out to allow normal operation and although the dc bus voltage will not be quite high enough the current-mode controller of the IGBT's will rapidly pull the dc bus voltage to the correct level.

The switches used to short out the soft-start resistors may be back-to-back thyristors or triacs which could be operated automatically by checking the dc bus voltage. However, for this prototype a three phase contactor is used and is controlled manually. Another three phase contactor is used to isolated the mains supply from the rectifier.

5.2.2 IGBT Modules

The main core of the power circuit is the insulated gate bipolar transistor (IGBT) modules. Three IGBT modules are used. Each module contains two IGBT's and associated built-in anti-parallel diodes to form one leg of the rectifier. The modules are

rated for a maximum voltage of 1200V and current of 50A. These are mounted on a heat-sink to aid cooling.

These modules were made available for the project and although their ratings were far in excess of what was required for the experimental prototype, their easy mounting arrangements and high power ratings made them attractive for use to demonstrate the practical feasibility of the converter and its controller.

5.2.3 Filter Components

The choice of filter components was discussed in Chapter 2 and the equations in Section 2.6 are used in selecting the value of filter components for the prototype.

5.2.3.1 DC Bus Capacitors

The dc bus capacitors have been chosen large enough to absorb harmonics caused by the supply. Two electrolytic capacitors are used and the per rail capacitance C_{dc} is 1500µF rated at 450volts. This value of capacitance will limit the ripple on the dc bus due to supply harmonics to negligible levels. The ESR of each capacitor may vary considerable especially with frequency. A measurement of the ESR at 50Hz gives an ESR of approximately 90m Ω and at 15kHz approximately 55m Ω .

5.2.3.2 Boost Inductors

The value of boost inductance is chosen to allow a maximum amount of switching ripple current to flow through it. At full-load of 1.5kW the peak of the 50Hz component of current is 3.07A. The maximum ripple current is set to 35% of 3.07A which gives

 $\Delta i_{boostlmax} = 1.08 A_{pk}$.

A nominal switching frequency of 15kHz is chosen as this is just above many people's audible range and gives a good compromise between switching losses and inductor size in this hard switched PWM converter. Also a higher f_s will result in prohibitive switching losses in the IGBT's that will be employed in an 80kVA converter. The actual switching frequency used is $f_s = 15,625$ Hz, this value is easily derived from a crystal oscillator as described later on in this chapter.

This value of switching frequency gives a boost inductance $L_{\text{boost}} \approx 6\text{mH}$ from Eqn. 2.47.

5.2.3.3 Front-End L-C Filter

The front-end L-C filter further attenuates the switching ripple component of current back to the utility. A value of attenuation is chosen to give a 20:1 reduction at the switching frequency. A filter inductance of $L_f = 500\mu$ H is chosen and by using Eqn. 2.48 this gives a filter capacitance of $C_f \approx 4\mu$ F. An actual value of $C_f = 4.4\mu$ F was employed, this being made up of two 2.2 μ F 600V polypropylene capacitors connected in parallel.

By using Eqn. 2.50 the peak ripple current in the filter inductor is $\Delta i_{if} = 0.16 A_{pk}$. The inductance of the supply will increase the effective overall filter inductance and further attenuate the ripple current back to the supply.

5.2.4 Measurement Transducers

Hall effect transducers are used to measure each of the three boost inductor currents and the two dc bus voltages and to provide isolation between the power circuit and the control circuit. The current transducers are connected in series with the boost inductors and give full scale output signal corresponding to maximum. The isolated output current signals are connected to precision resistors (0.1% tolerance) providing the required voltages representing the current loop feedback signals. The relationship between the measured currents and the voltage signals is 1:1, i.e. a transresistance of 1Ω . The bandwidth of the current transducers is stated as 150kHz.

The voltage transducers are connected to each of the dc bus rails with respect to the centre-point via a $47k\Omega$ resistor (5% tolerance). The isolated output current signals are connected to resistors in series with trimming potentiometer providing the required voltage representing the voltage loop feedback signals. As variations may occur in the $47k\Omega$ measurement resistor the trimming potentiometer is used accordingly. However, the required accuracy of the voltage loop is not as high as that required for the current loops.

5.2.5 IGBT Gate Drivers

Six gate drivers are provided; one for each IGBT. The gate drivers amplify the control signals from the controller and provide enough driving current for the gates.

The signal from the controller is isolated on each board via an optoisolator. The six gate driver circuit boards are mounted on a mother board which supplies each daughter board with an isolated power supply via a high frequency transformer with six secondary windings. The supply for the mother board itself is provided from a 20V dc bench power supply.

The six control signals from controller are connected to the gate driver mother board via a ribbon cable. The control signals are at TTL level connected in series with $1k\Omega$ resistors to limit the current into the optoisolators.

Protection of each IGBT is provided on each gate driver board. A connection is made to the collector of the IGBT to sense a fault condition such as an overload or shoot through which occurs when $V_{ce(sat)} > 7V$. The circuit will provide a minimum of 1µs pulse width. The drive signal is removed if a fault is detected.

The gate drive signal swings from +15V to -5V with respect to the emitter, the negative bias aiding in the noise immunity of the circuit.

5.3 Control Circuit Design

The control circuit consists of a number of circuit boards. These are :-

- A power supply board that supplies the power to each of the circuit boards
- The main control board
- A digital signal processor (DSP) board connected to a personnel computer (PC)
- The PWM modulator board
- A protection board that checks for supply current overload and checks that the dc bus voltage is within its range
- A centre-point balancing circuit

Fig. 5.2 shows the layout of the control circuit. The boards are produced on double sided PCBs, but only the supply rails, holes and some interconnections for the ICs and discrete components exist. The remaining interconnection are made using wire-wrap. This enables a more rapid production of the prototype board.

5.3.1 The Power Supply Board

This board supplies an unregulated voltage of approximately \pm -26 volts to each of the boards and consists of a transformer, single phase bridge rectifier and two electrolytic capacitors. Each board has its own regulators to provide \pm 15V, -15V and \pm 5V where required. This helps in reducing noise problems.

Decoupling capacitors of 0.1μ F between supply and ground of each integrated circuit (IC) are used extensively throughout the circuit boards. A separate digital ground is also used where possible. This further helps to reduce noise.

5.3.2 The Main Control Board

The main control board performs the a-b-c to d-q-n transformations of the measured boost inductor currents, performs the function of the PI controllers for the voltage and current loops and transforms the modulating signals from the d-q-n reference frame back to the a-b-c reference frame.

TTL compatible (HCT and ACT) digital IC's are used throughout to maintain compatibility with the DSP buses and to improve noise immunity.

5.3.2.1 A-B-C / D-Q-N Transformations

Fig. 5.3 shows the block diagram of the a-b-c to d-q-n transformation. Six sine wave templates are required. The sinusoidal terms are used to derive the d-axis quantity, the cosinusoidal terms are used to derive the q-axis quantity, and the n-axis quantity is simply the summation of the three input currents. Six analogue multipliers are required. The summers are achieved using summing operational amplifiers (op-amps).

To derive the sine wave templates an EPROM lookup table could be used in conjunction with a digital to analogue converter (DAC). As there are a number of sine templates to derive and because of availability a DSP was used with six DAC's to generate the templates.

If multiplying digital to analogue converters (MDAC) are used then the analogue multipliers are not required. The MDAC's chosen are operated in a four quadrant mode and have a resolution of 12-bits. The MDAC's are connected directly to the DSP data bus which forms one input (the digital input). The other input to the MDAC is the analogue signal, in this case the boost inductor feedback signal. The maximum output of the MDAC is $\pm 10V$ where 10 volts represents the maximum inductor current of 5A, i.e. the feedback gain of the current loop is 2.

A similar system is used for the transformation of the modulating waveforms from d-q-n back to a-b-c (Fig. 5.4) and requires another six MDAC's.

5.3.2.2 Phase Locked Loop

To synchronize the sine wave templates to that of the utility a phase locked loop (PLL) is used. Fig. 5.5 shows the block diagram of the PLL. A 50Hz reference signal is obtained from the output of a transformer connected to the red phase utility voltage. This signal is passed through a zero crossing detector (ZCD) which provides a TTL signal at the same phase as the input reference. Hysteresis is provided in the ZCD to prevent multiple crossings around the zero volt level of the reference signal due to noise.

The output of the ZCD forms the reference to the actual PLL (4046) which consists of a digital phase detector, a voltage controlled oscillator (VCO) and a counter/divider. The output of the divider is compared with the output of the ZCD and a signal proportional to the phase difference is passed to a VCO. The larger the input signal to the VCO the

greater the output frequency which is at TTL level and has a nominal frequency of 102.4 kHz. The output is connected to the clock of a counter via a D-type flip-flop which is connected to the 20MHz DSP clock, thus synchronizing the counter with the DSP. The counter also acts as a divider to give a nominal 50Hz signal.

A counter has been chosen which allows the current value to be read as a digital word with a 12-bit resolution. The digital word represents the phase angle of the red phase supply voltage. This digital word is read into the DSP via the data bus and is used as an index when providing the required sine wave templates.

5.3.2.3 PI Controllers

Four PI controllers are used: one for the voltage loop and one for each of the d-axis, qaxis and n-axis current loops. Fig. 5.6 shows an op-amp that performs the task of the PI controller which also has an extra pole. The proportional constant, integral constant and pole of the controller in terms of component values are given as :-

$$K_p = \frac{R_2}{R_1} \tag{5.1}$$

$$K_i = \frac{1}{R_1 C_1}$$
 (5.2)

$$\omega_{p} = \frac{C_{1} + C_{2}}{C_{1}C_{2}R_{2}}$$
(5.3)

When a dc voltage component is sustained on the input of the op-amp problems, will

occur with integrator wind-up. The voltage on the integrator capacitor continues to rise even when the output hits the required limit. When the input voltage reverses polarity a time delay exists before the output starts to respond. This can impair the transient response of the system. To prevent integrator wind-up the integrator feedback capacitor is clamped. Zener diodes are used for this purpose and are connected across the feedback path of the op-amp (Fig. 5.6).

The reference for the voltage loop is obtained from a multi-turn potentiometer connected across +15V supply rail and ground, and similarly for the reference for the q-axis but is connected across +15V and -15V to allow for lead or lag reactive power flow.

5.3.2.4 Balancing Control Circuit

Although the balancing board is situated on a separate daughter board it still constitutes the control and so will be discussed in this section.

The circuit simply consists of two op-amps. One is used to find the difference between the two measured dc bus voltages and the other is configured as a low pass filter (LPF). The output of the filter forms the reference to the n-axis.

5.3.3 DSP Board

The DSP reads the phase of the supply and generates the 12-bit digital words for the sine templates for the a-b-c / d-q-n transformations. The DSP used is a Texas Instruments TMS320C50 and comes pre-mounted on a multi-layer printed circuit board (PCB) as part of a DSP starter kit (DSK). The kit allows direct connection of the DSK to a PC via an RS232 serial link and comes with PC software which includes a debugger program allowing the DSP to be rapidly programmed without the need to program an EPROM and

is therefore ideal for prototyping.

Some of the relevant features of the TMS320C50 and DSK are :-

- 16-bit fixed point processor
- 32-bit accumulator
- 16 x 16-bit parallel multiplier
- 50ns single-cycle instruction execution time
- 10K of on-chip RAM
- Timer interrupt with period registers
- 64K parallel input/output (I/O) ports, 16 of which are memory mapped
- Software-programmable wait-state generators

The DSP may be programmed using the software provided with the DSK. However, the capabilities are limited so an assembler and linker are used that produces object files that are executable by the TMS320 DSP's known as common object file format (COFF). Some of the main advantages include being able to write reusable code using macros, user defined variables and ease of programming the code in sections of memory.

5.3.3.1 Hardware

The DSP is used to provide the digital data word to each of the 12 MDAC's that represent the sine templates for the reference transformations and to read in the phase of the utility from the PLL counter.

The input/output pins required from the DSP are the data bus, the address bus, the read select (RD), the write enable (WE) and the I/O space select (IS) and are connected to the main control board using three ribbon cables. There are 16 memory mapped I/O ports. These ports may be accessed using more extensive addressing modes as well as the conventional IN and OUT instructions and as such are used to access the MDAC's and

PLL counter. Twelve ports are allocated to the MDAC's (address 4 - 15) and one port to the counter (address 0).

The MDAC chosen is the AD7845 with a maximum output settling time of 5µs and worst case write pulse width of 140ns. Fig. 5.7 shows how one of the MDAC's is connected to the DSP. As the MDAC has built in input buffers and latch it can be connected straight to the DSP data bus. A 4 - 16 decoder is used to decode the address bus and is connected to the chip select input (\overline{CS}) on the MDAC. The I/O space select pin is connected to the write input (\overline{WR}) on the MDAC.

The PLL counter consists of two cascaded 8-bit counters although only 12-bits are used. Fig. 5.8 shows how the counter is connected to the DSP. The counters require tri-state buffers to prevent a data bus contention. Two 8-bit buffers are employed, but only 12bits are used. As only one input is used no address decoder is required. The buffers are enabled by connecting their gate enable pins (\overline{GI} , $\overline{G2}$) to the I/O space select and read select pins on the DSP.

5.3.3.2 Software

The program for the DSP is written in TMS320C5x assembly language using the COFF format. This has the advantages of writing compact, fast code and allows direct control over the DSP hardware. The basic function of the program is quite simple. The phase angle is read in from the PLL counter. From this value the 6 sine template values are calculated and sent out to the 12 corresponding MDAC's.

The process is repeated in a continuous loop of a fixed time interval by using the DSP timer interrupt. The frequency of the timer interrupt is set to 150.376 kHz approximately 10 times the switching frequency and thus should have little effect on the overall response of the current loops. The period of the interrupt allows just enough time for the required

task to be executed and allows enough time for each of the MDACs to settle.

There are two methods of obtaining a sine wave function: calculate the function mathematically in real-time, or use a lookup table. Calculating the function takes up too much processor time so a lookup table is used which requires a large amount of memory to store the values. The lookup table is produced off-line by the DSP before the timer interrupt program is run by calculating each of the 4096 (12-bit) values. The function for calculating sin x is :-

$$\sin x \approx x - \frac{x^3}{3!} + \frac{x^5}{5!}$$
(5.4)

This is only valid for the first quadrant $(0 < x < \pi/2)$ [46]. As the other three quadrants are mirror images of the first it is relatively straight forward to obtain these values.

Fig. 5.11 shows the flow diagrams of the DSP program of the main program which initializes the DSP and the timer interrupt service routine (ISR).

Initially, all interrupts are disabled to prevent the DSP 'crashing' whilst it is being set up. The programmable I/O wait states are set to 2 so that the period the I/O space is accessed is increased from 50ns to 150ns for the MDACs and PLL counter. This allows MDACs with a relatively slower access time to work with the DSP. It also allows for additional propagation delays caused by controller board layout. The interrupt vector table is set up so that the DSP knows which address to jump to when a timer interrupt occurs.

The sine wave lookup table is then calculated for 4096 points and stored in the on-chip RAM. Next the timer interrupt is set to a frequency of 150.376kHz and all interrupts are enabled. The DSP is then left in an endless loop until a timer interrupt occurs. The DSP will enter the timer ISR every 6.65µs.

The timer ISR simply reads the PLL counter value and uses this as an index for looking

up the six sine waves. The six digital words are sent to the twelve MDACs. The DSP returns from the ISR back to the main program and re-enables all interrupts.

5.3.4 PWM Board

The PWM board converts three modulating waveforms from the main controller board to the required PWM pulses. A deadband is added to each pair of signals to prevent two IGBTs being on simultaneously thus preventing shoot through.

To generate the PWM pulses a triangular wave carrier is used. The triangular wave is generated digitally which has the advantages of having less problems with drift and offsets. Fig. 5.9 shows the basic circuit diagram of the carrier wave generator. It consists of an 8-bit up/down counter which is set up with additional logic to continually count up to 256 and then count back down to zero again and requires a counter with a terminal count (TC) pin which goes logic high when the maximum or minimum count is reached.

An 8-bit DAC is connected to the counter which will provide a triangular voltage output on the V_{out} pin and its logical complement on the $\overline{V_{out}}$ pin. Both the counter and DAC are clocked from a 8MHz TTL signal derived from a crystal oscillator. This gives a frequency of the triangular wave of 15,625Hz. By connecting the complementary outputs of the DAC to a differential amplifier, a triangular wave is obtained that has no dc component. The triangular wave is further amplified to give an amplitude of ±10volts and low pass filtered to help remove the steps in the output due to the DAC. A TTL signal is also obtained at the same frequency as the triangular wave.

Each modulating waveform is compared with the triangular wave using a comparator to produce a TTL signal. Fig. 5.10 shows the circuit diagram for one phase. A PWM latch is used to prevent multiple switching occurring due to noise during one switching period

160

using a D-type flip-flop. The output and complementary output of the flip-flop provides the upper and lower PWM signals for the switches in one leg.

A deadband is introduced to the rising edge of each signal. Each output of the D-type flip-flop is delayed using a 4-bit counter before it is allowed to set an S-R flip-flop. A clock signal derived from a crystal oscillator is used. A 4MHz clock is used which adds a deadband of approximately 2μ s. The S-R flip-flop is reset without any delay in the signal. The outputs of the two S-R flip-flops are the signals for the lower and upper switches. These signals are disabled using a gate-drive signal obtained from the protection board.

The modulating signals are clamped using Zener diodes to $\pm 9.7V$ to prevent over modulation occurring.

5.3.5 Protection Board

The protection board monitors the three phase inductor currents and the two dc bus voltages. The measured signals are compared with reference signals derived from potentiometers using comparators to produce TTL signals. This requires two comparators per measured signal to check that the signal has remained within its maximum and minimum limits.

If any signal has passed its limit then an S-R flip-flop is reset. The output of the flip-flop is used as the gate drive enable signal for the PWM board and thus the protection circuit can turn off all the IGBTs when necessary. The main three phase supply contactor is controlled by the protection circuit and so can remove the supply also.

5.3.6 Control Parameters

The control parameters for the four PI controllers are chosen to give a crossover frequency in the current loop of $f_{ci} = 2.5$ kHz and in the voltage loop of $f_{cv} = 30$ Hz. The voltage crossover frequency is chosen to reduce the effect of harmonics on the dc bus, caused by harmonics in the load and in the supply voltage, from distorting the supply currents.

Although the original rating of the prototype was 1.5kW the rectifier system suffers greatly from noise. Thus, a lower load power level of 200W was used for testing. The original filter components values are maintained. The dc bus voltage and nominal supply voltage are changed accordingly to give :-

 $V_{dc} = 110V \qquad \qquad V_{ph} = 30V$

The feedback constants remain the same as :-

$$G_i = 2$$
 $G_v = 1/100$

The resistor and capacitor components of the PI op-amps using standard value components are :-

<u>Voltage</u>
$R_1 = 12k\Omega$
$R_2 = 560 k \Omega$
$C_1 = 10,000 pF$
$C_2 = 220 pF$

These values give the following compensator PI constants and poles (Eqns. 5.1 - 5.3):-

Current	<u>Voltage</u>
$K_{p} = 8.18$	$K_{p} = 46.67$
$K_i = 66.85 \text{ krads}^{-1}$	$K_i = 8.33 \text{ krads}^{-1}$
$\omega_p = 89.87 \text{ krads}^{-1}$	$\omega_p = 8.29 \text{ krads}^{-1}$

The triangular carrier wave has an amplitude of 10V peak which allows the full output voltage range of the op-amps to be utilized. This has the effect of having an attenuation of 10 in the open current loop. Accordingly, the overall gain of the current loop PI controller is increased by a factor of 10. The pole in the current loop is placed near the switching frequency and is used to reduce the effects of noise.

A worse case ESR of the each of the dc bus capacitor is assumed to be $R_c = 90m\Omega$. This gives an ESR zero in the voltage loop of $\omega_{zesr} = 7.4$ krads⁻¹. The pole in the voltage loop compensator counters this. The phase margin of the voltage loop is approximately 47°.

5.4 Experimental Results

The performance of the experimental prototype is demonstrated by results obtained under steady-state and transient load conditions. A demonstration of reverse power flow is shown by the use of an active load. These results are compared to simulations using SABER employing the same power and control parameters as used in the practical case. The simulated circuit uses ideal switches and does not include deadband times for the switches.

Photographs of the four-wire prototype circuit are shown in Figs. 5.12 - 5.15. Fig. 5.12 shows the power circuit contained in a metallic case. On the left are the six gate drive circuits which are plugged into the gate drive mother board, to the right of these are the three IGBT modules and below them are the two dc bus capacitors. The circuit board to the right of the IBGT modules holds the current and voltage Hall effect transducers. At the top of the case are the boost and filter inductors and the filter capacitors. At the top right hand corner are the fuse holder where the power enters, the main contactor and the soft start contactor.

Fig. 5.13 shows the control circuit. At the top is the DSK board. The largest board is the
main control board and below that is the protection board. The PWM board is at the bottom right hand corner. The transformer for the supply to the DSK and the unregulated power supply board can also be seen.

Fig. 5.14 shows the control circuit and power circuit together. The ribbon cable provides the gate drive signals from the control board to the power circuit. The feedback signals from the power circuit to the control circuit are connected by multi-core coaxial cable. The bench power supply supplies 20V dc to the gate drive mother board. The rheostats can be seen to the right of the power circuit case which are used to load the power circuit. Fig. 5.15 shows the complete system with the PC which is used to download the assembly program to the DSP.

The input and output powers of the system were measured using a watt meter. The input power was 232.50W and the output power was 204.00W. This corresponds to an efficiency of about 88% and would likely be higher at greater power levels. The majority of the losses are due to conduction losses and switching losses in the IGBT modules. A power factor meter reading of the supply gave 0.998 per unit.

5.4.1 Harmonic Analysis

The first set of results are the harmonic analysis of the phase voltages, line currents and boost inductor current. The supply to the rectifier is from a three-phase variac connected to the 400V utility to give a nominal $30V_{ph}$ voltage. The measured quantities, using a true RMS meter give each phase voltage as :- $V_r = 26.50V$, $V_y = 27.74V$, $V_b = 29.96V$. An unbalance exists between the three phase voltages and will subsequently cause voltage harmonics on the dc bus and allow harmonics to occur in the line currents.

A harmonic analysis up to 1kHz was performed using a spectrum analyzer on the red phase voltage V_r at the time the practical results were taken and is shown in Fig. 5.17.

The harmonics are normalized to the fundamental 50Hz frequency (which is not shown). The dominant harmonics are the 5th, 7th, 11th, etc. as expected, but the triplen harmonics are also present due to in part a large number of PC's connected to the supply.

Harmonic analysis were performed on the red phase supply current and boost inductor current (Fig.5.18). The values have been normalized to their respective fundamental components. This is required to make a relative comparison between the two currents due to the fluctuating nature of the supply as the respective measurements were not taken at the exact same time. As such these measurements should be regarded as an approximate comparison.

The magnitude of the harmonics are less than 1.2% of the fundamental. The dominant harmonic is the 100Hz component. These harmonics occur in the boost inductor due the dc bus voltage containing small amount of harmonic components due to the unbalanced supply voltages and their harmonics. The harmonics are amplified by the voltage loop compensator resulting in a distorted current reference signal. The spectrum for the supply harmonics differs to that of the boost inductor as the harmonics in the utility voltage produce associated harmonic currents in the front-end L-C filter. The L-C filter of course lies outside of the current controller feedback loops.

Fig. 5.19 compares the normalized spectrum of the boost inductor current with the voltage loop closed and with the voltage loop open (the d-axis current reference is supplied from a dc source). The harmonics with the voltage loop open are much lower (less than 0.2%) and as such demonstrates that the current controllers perform extremely well.

The worst case boost inductor switching ripple current measured from an oscilloscope was approximately 300mA peak-peak and this compares well with the theoretical value of 293mA peak-peak from Eqn. 2.47. The worst case supply switching ripple current was measured as approximately 10mA peak-peak which again compares well with the

theoretical value of 12 mA peak-peak from Eqn. 2.50.

5.4.2 Steady-State and Transient Performance

To demonstrate the transient performance of the rectifier a resistive load of 60Ω corresponding to 200W full load is switched in and out. A storage oscilloscope was used to measure the experimental waveforms and an oscilloscope plotter used to plot the waveforms.

Fig. 5.20 and 5.21 show the experimental and simulated plots of a step-load change from no-load to full-load. As the load has a small amount of inductance the load current does not rise instantaneously. So that a more reliable comparison can be made between the simulated and actual results a non-ideal switch available as a template in the SABER simulator is used to connect/disconnect the load to the rectifier. The switch resistance exponentially changes with time over a period of 5ms. It can be seen that the output voltage waveform compares very well between the actual and simulated results. The voltage transient settles in about one period of the supply and the voltage control is well damped. The experimental output voltage shown settles higher than the required 110V. This error is introduced by the oscilloscope and plotter, the latter also causing an offset in some of the plots. The actual voltage was measured accurately as 109.78V. Fig. 5.22 and 5.23 shows similar results for a step-load change from full-load to no-load.

Figs. 5.24 and 5.25 show the experimental and simulated waveforms for a step-load change from no-load to full-load for the d-axis current reference. The two results compare well. However the experimental results show a slightly larger d-axis current reference waveform. The extra requirement of current is for the power losses in the circuit and because of a small short fall in supply phase voltage from the nominal value of 30V. Similar results are shown in Figs. 5.26 and 5.27 for a step-load change from full-load to no-load.

Figs. 5.28 and 5.29 show the waveforms for the boost inductor current in the red phase for the experimental and simulated circuits. The waveforms compare well. The amplitude of the boost current follows the d-axis current reference as the voltage loop settles. Figs. 5.30 and 5.31 show similar waveforms for a step-load change from full-load to no-load.

Figs. 5.32 and 5.33 show the voltage across the load resistor when this is switched in and out of the circuit and supply neutral current for the experimental and simulated circuits. At the transient ringing can be seen in the load voltage of the experimental results due to the load inductance and switch bounce. A small amount of 50Hz current can be seen in the supply neutral current of the experimental results which is due to the unbalanced supply voltage allowing a small amount of 50Hz current to circulate around the front-end L-C filter and supply neutral.

Figs. 5.34 and 5.35 show the phase voltage and current waveforms for the experimental and simulated circuits. The dc offset in the phase voltage waveform is due to the plotter. It can be seen that the current is in phase with the voltage. Again, it can also be seen that the amplitude of the experimental circuit supply current is slightly higher than in the simulation for reasons already mentioned.

5.4.3 Bidirectional Power Flow

To demonstrate the regenerative power flow capabilities of the rectifier, an active dc source is placed in the load as shown in Fig. 5.16. The rectifier is made to regulate the dc bus voltage at 60V. The voltage being lower than hitherto used in order to accommodate the limited output voltage of the available active dc source. The load consist of a 60 Ω resistor in parallel with a series connection of a 5 Ω resistor, a 70V dc bench power supply and a switch. When the switch is open the rectifier power flow is positive and when the switch is closed the rectifier power flow is negative and the dc bus

remains regulated at 60V.

Fig. 5.36 and 5.37 shows the total load current from the dc bus and red phase boost inductor current for the experimental and simulated circuits for a step-load change from positive to negative power flow. The power flow can be seen to reverse when the load current goes from positive to negative and the boost inductor current changes phase by 180°. During positive power flow the amplitude of the experimental boost inductor current is slightly higher than the simulated results due to the circuit losses in the practical system. During the negative power flow the amplitude of the boost inductor current is lower in the experimental results and again this is explained by losses in the practical system. Figs. 5.38 and 5.39 show similar waveforms for a step-load change from negative power flow to positive power flow.

Fig. 5.40 and 5.41 shows the red-phase phase voltage and phase current for the experimental and simulated circuits for a step-load change from positive to negative power flow. The reversal of phase current can be clearly seen. Figs. 5.42 and 5.43 shows similar waveforms for a step-load change from negative power flow to positive power flow.

5.5 Conclusions

This chapter has described a practical implementation of the four-wire rectifier. The prototype was designed for 1.5kW originally. A detailed description has been given of the power circuit design and the controller design. An analogue controller operating in the d-q-n reference frame was chosen as most was known about this at the time of the practical design, and a DSP was used to generate the required sine waves for the a-b-c - d-q-n transformations.

Due to problems with noise the rectifier was operated at a maximum load of 200W. The

most probable causes of noise were radiated noise from the switching power circuit picked up by the control circuit, and control circuit signals interfering with one another, in particular the high frequency digital signals interfering with the analogue signals. The use of wire-wrap for interconnections makes the controller very susceptible to noise particularly because of the large number of connections between IC's some of which require long connecting wires. A full PCB design would probably reduce the noise significantly especially if a multi-layer board is used. Noise problems were also encountered with the protection board.

A number of practical results were taken and comparisons made with simulation results. These included steady-state, transient and bidirectional power flow tests. The practical and simulation results compared very well and the only main differences being due to power losses in the practical circuit. Overall the prototype performed well and as expected for the 200W load test.

To obtain results at the 1.5kW level of the design would entail considerable expense and time in producing the necessary multilayer PCB's, and the results then obtained would add very little to the information already obtained at the lower operational power levels. It is thus considered that the results obtained at the 200W level fully demonstrate the feasibility of the four-wire power factor corrected boost rectifier and analogue d-q-n reference frame controller.







Fig. 5.3 Practical Implementation of ABC-DQN Transformation



Fig. 5.4 Practical Implementation of DQN-ABC Transformation



Fig. 5.5 Phase Locked Loop Block Diagram



Fig. 5.6 Op-amp Implementation of PI Controller



Fig. 5.7 Connection of MDAC to DSP



Fig. 5.8 Connection of PLL Counter to DSP



Fig. 5.9 Triangular Carrier Wave Generator



Fig. 5.10 PWM Comparator and Deadband Circuit





Practical Implementation



Fig. 5.12 Photograph of Prototype Four-Wire Rectfier Power Circuit



Fig. 5.13 Photograph of Prototype Four-Wire Rectifier Control Circuit

Practical Implementation



Fig. 5.14 Photograph of Complete Prototype Four-Wire Rectifier System



Fig. 5.15 Photograph of Complete Prototype Four-Wire Rectifier System with PC



Fig. 5.16 Bidirectional Power Flow Test Load



Fig. 5.17 Normalized Frequency Spectrum of Red Phase Supply Phase Voltage



Fig. 5.18 Normalized Frequency Spectrum of Red Phase Boost Inductor Current and Phase Current



Fig. 5.19 Normalized Frequency Spectrum of Red Phase Boost Inductor Current for Open and Closed Voltage Loop



Fig. 5.20 Experimental Load current and Output Voltage -Step-Load Change from No-Load to Full-Load











5ms/div

Fig. 5.23 Simulated Load Current and Output Voltage -Step-Load Change from Full-Load to No-Load



Fig. 5.24 Experimental Load Current and D-Axis Current Reference -Step-Load Change from No-Load to Full-Load







Fig. 5.26 Experimental Load Current and D-Axis Current Reference -Step-Load Change from Full-Load to No-Load



Fig. 5.27 Simulated Load Current and Daxis Current Reference -Step-Load Change from Full-Load to No-Load



Fig. 5.28 Experimental Load Current and Boost Inductor Current -Step-Load Change from No-Load to Full-Load



Fig. 5.29 Simulated Load Current and Boost Inductor Current -Step-Load Change from No-Load to Full-Load



Fig. 5.30 Experimental Load Current and Boost Inductor Current -Step-Load Change from Full-Load to No-Load



Fig. 2.31 Simulated Load Current and Boost Inductor Current -Step-Load Change from Full-Load to No-Load



Fig. 5.32 Experimental Load Voltage and Supply Neutral Current -Step-Load Change from No-Load to Full-Load



Fig. 5.33 Simulated Load Voltage and Supply Neutral Current -Step-Load Change from No-Load to Full-Load



Fig. 5.34 Experimental Phase Voltage and Phase Current on Full-Load



Fig. 5.35 Simulated Phase Voltage and Phase Current on Full-Load





Fig. 5.36 Experimental Load Current and Boost Inductor Current -Step-Load Change from Positive Power Flow to Negative Power Flow





Practical Implementation



Fig. 5.38 Experimental Load Current and Boost Inductor Current -Step-Load Change from Negative Power Flow to Positve Power Flow







Fig. 5.40 Experimental Phase Voltage and Phase Current -Step-Load Change from Positive Power Flow to Negative Power Flow



Fig. 5.41 Simulated Phase Voltage and Phase Current -Step-Load Change from Positive Power Flow to Negative Power Flow



Fig. 5.42 Experimental Phase Voltage and Phase Current -Step-Load Change from Negative Power Flow to Positive Power Flow





Proposals for Digital Control of the Four-Wire Rectifier

6.1 Introduction

Digital control can provide a number of benefits compared to that of an analogue controller. These include increased reliability and stability, reduced component count and allows for control techniques to be implemented that may otherwise be difficult to achieve.

Two proposals for digital control of the four-wire rectifier are discussed in this Chapter. These are a digitized version of the analogue d-q-n average current mode controller described in Chapter 2, and a predictive controller with average current control. Practical requirements are given for both systems. Simulation results are used to demonstrate the performance of the predictive controller. The basic topology of the four-wire rectifier without the front-end L-C filter is considered to simply the description.

The main component of the digital system is the processor. Typically this would be a digital signal processor (DSP), a microcontroller or a microcomputer. A DSP tends to have hardware mathematical functions such as a multiply, and can operate such instructions in one clock cycle, making it a very powerful processor in terms of numerical calculations. However, some microcontrollers now have similar functions available.

6.2 Digitized Average Current Mode Controller

The first of the two digital controls schemes is the digitized version of the average current mode controller discussed in Chapter 2. The use of the d-q-n rotating reference frame is

also included as this provides a smaller steady-state error of the 50Hz line current tracking under all-loads. The processor must perform the transformations from the stationary to rotating reference frames and as such requires some form of sine wave generation.

Fig. 2.24 shows the analogue four-wire rectifier average current mode controller for which a digital version is required.

6.2.1 Sampling and Data Acquisition

The digital system operates by quantizing all values, i.e. all of the inputs to the system (voltages and currents) and time (the sample period). The sample frequency is generally chosen as large as possible to maximize the bandwidth of the system. However, for a SMPS the maximum sample frequency is usually limited to that of the switching frequency as the duty cycle can only be changed once during a switching period. If the sample period is chosen as the switching period then it also simplifies the system, and as such shall be assumed for the rest of this chapter.

The input values required are the three boost inductor currents, the two dc bus voltages and the phase angle of the red-phase voltage. These values must be sampled at least once every switching period and converted to digital values using an analogue to digital converter (ADC). The resolution of the ADC's for use in SMPS control applications is usually in the range of 8-12 bits.

The effect of sampling results in a time delay of at least one sample period in the control loop.

6.2.2 Software and Variables

The controller program may be written in a high level language such as 'C' or a low level language such as assembly language. The advantage of a high level language is the ease of programming. However, the use of assembly can provide a much more compact and efficient code which will execute faster and provides direct access to the hardware. The use of macros in assembly programming can help structure the program and enable reusable code.

A floating-point or fixed-point number system is required for the variables of the controller. This usually depends on the DSP or microcontroller used, but a fixed-point processor can be made to emulate floating-point arithmetic operations through the software. If fixed-point arithmetic is used then a two's complement system is often used.

The number of bits used to represent a number determines the accuracy of the system. Overflow and underflow bits are required. Usually the requirement for underflow bits is greater and overflow is not too much of a problem. Eight-bit processors form the basic level of arithmetic accuracy, but 16-bit and 32-bit processors are becoming more common place. However, a 16-bit processor can be made to perform 32-bit arithmetic if necessary with the use of additional software such as macros, but is not as fast as an equivalent 32-bit processor.

To achieve an accurate sample period within the processor a timer interrupt (which is locked to the system clock) is often used and the digital control algorithm is executed on each interrupt. Many processors have a timer interrupt built in enabling the interrupt period to be adjusted via the software.

For a two loop system such as used here, i.e. an outer voltage loop and inner current loops, it is usual to use the same sample period for both due to simplicity of programming. However there is nothing wrong with having a slower outer loop sample frequency compared to the inner loop. In this case two interrupts may be used usually with the inner loop having precedence over the outer loop.

6.2.3 Digital Filters

The current loops for the d, q and n axes and the voltage loop all require a PI controller which may be implemented using digital filters. There are many publications on digital filters [47] and the basis is described here with emphasis on the practical implementation.

6.2.3.1 The z-Domain and the δ Function

The main form a function implemented discretely is using the z-domain. The relationship between the Laplace s-domain and z-domain is known as the bilinear transform :-

$$s = \frac{2}{T_s} \frac{1 - z^{-1}}{1 + z^{-1}}$$
(6.1)

where T_s is the sample period.

An extension to the z-domain is with the use of the δ function :-

$$\delta = z - 1 \tag{6.2}$$

The advantages of using a δ -filter compared to a z-filter arise in the practical implementation, the main ones being the significant reduction in wordlength for the coefficients, and the z-filter requires a larger wordlength with increased sample frequency whilst the δ -filter requirements are independent of sample frequency.

The filter can be represented in canonic form which has the main advantages of fewer stored variables and additions. A second order δ -filter in canonic form is shown in Fig. 6.1. The transfer function is :-

$$H(\delta) = \frac{c_o + c_1 \delta^{-1} + c_2 \delta^{-2}}{1 + r_1 \delta^{-1} + r_2 \delta^{-2}}$$
(6.3)

This can be compared to the s-domain equivalent :-

$$H(s) = \frac{n_0 + n_1 s + n_2 s^2}{1 + m_1 s + m_2 s^2}$$
(6.4)

The bilinear transform from the s-domain to δ enables the coefficients of the δ -filter to be obtained from the original s-domain filter and is given as :-

$$\delta = \frac{sT_s}{1 - sT_s/2} \quad or \quad s = \frac{2\delta}{T_s(2 + \delta)} \tag{6.5}$$

In terms of software implementation the operator δ^{-1} represents an accumulator. The pseudo-code for the δ -filter shown in Fig. 6.1 is given below :-

$$v = u - r_1^* w - r_2^* x$$
$$y = c_0^* v + c_1^* w + c_2^* x$$
$$x = x + w$$
$$w = w + v$$

6.2.3.2 A Digital PI Filter

The PI filter is represented in the s-domain as :-

$$H(s) = K_p + \frac{K_i}{s} \tag{6.6}$$

The function is first order. The bilinear transform of Eqn. 6.5 is used to obtain the δ function equivalent :-

$$H(\delta) = (K_n + K_j T_j 2) + K_j T_s \delta^{-1} = c_0 + c_1 \delta^{-1}$$
(6.7)

Form Eqn. 6.7 the coefficients c_0 and c_1 are found. The structure diagram is shown in Fig. 6.2 and it can be seen that there are no recursive elements present. This simplifies the equations as :-

$$y = c_0^* u + c_1^* w$$
$$w = w + u$$

The PI controller has an integrator element, i.e. there is a pole at the origin, and as such the output will continue to rise if the input is sustained without a change in polarity. This is known as integrator wind-up and is analogous to the problem of the operational amplifier implementation of the PI controller in Chapter 5. The solution in the digital implementation is to not to increase the variable w any further if the output y exceeds the required limit.

6.2.4 A-B-C, D-Q-N and α-β-o Reference Frames

The average current mode controller described in Chapter 2 uses a transformation of the boost inductor currents from the stationary a-b-c reference frame to the synchronously rotating d-q-n reference frame. An inverse transformation of the modulating waveforms from d-q-n to a-b-c is also used. The transformation matrix is given in Eqn. 2.40.

The transformations require quite a large amount of processing time and a method to reduce this is discussed as follows.

The α - β stationary reference frame converts the three phase stationary a-b-c values into two phase values. The d-q rotating reference frame is an extension to the α - β reference

frame in that it is rotating in synchronism with the utility frequency. The vector relationship is shown in Fig. 6.3. Four-wire systems require an extra axis to take into account the zero sequence or neutral quantities. The α - β reference frame is extended to α - β - σ and the d-q reference frame is extended d-q-n.

The mathematical relationship between the a-b-c and the α - β -o reference frames [48], and the a-b-c and the d-q-n reference frames is :-

$$\begin{bmatrix} V_{\alpha} \\ V_{\beta} \\ V_{\sigma} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} V_{\alpha} \\ V_{\delta} \\ V_{c} \end{bmatrix}$$
(6.8)

$$\begin{bmatrix} V_{a} \\ V_{q} \\ V_{s} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \sin\theta & \sin(\theta - 120^{\circ}) & \sin(\theta + 120^{\circ}) \\ \cos\theta & \cos(\theta - 120^{\circ}) & \cos(\theta + 120^{\circ}) \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} V_{a} \\ V_{b} \\ V_{c} \end{bmatrix}$$
(6.9)

where $\theta = \omega t$. It should be noted that in some publications the constant of the transformation matrices 2/3 is replaced by $\sqrt{2/3}$ or some other value. The transformation from the a-b-c to the d-q-n reference frame of Eqn. 6.9 may be achieved by first transforming to the α - β -o reference frame via Eqn. 6.8 and then Eqn. 6.10:-

$$\begin{bmatrix} V_{a} \\ V_{q} \\ V_{n} \end{bmatrix} = \begin{bmatrix} \sin\theta & -\cos\theta & 0 \\ \cos\theta & \sin\theta & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{a} \\ V_{\beta} \\ V_{o} \end{bmatrix}$$
(6.10)

From Eqn. 6.10 it can be seen that fewer sine functions are required in the matrix and two of the sine functions are the same, and that $V_n = V_0$. This method for calculating the d-q-n variables can be used with advantage.

The phase angle θ is read into the processor every sample period from a phase locked

loop circuit similar to that in Fig. 5.5 described in Chapter 5.

6.2.5 Average Current Control

A method is required to obtain the average boost inductor currents. There is a ripple current superimposed on the average boost inductor current and when an A/D conversion takes place the 50 Hz average current may not be measured accurately. This will lead to an error between the reference current and the actual average 50Hz current which will be larger for a smaller boost inductance.

Fig. 6.4 shows a typical boost inductor current with ripple current, the duty cycle and processor time allocation. This assumes a constant turn-on time and it can be seen that when the current is measured at the beginning of the sample period T_s the average current is not measured. One method to obtain the average current [49] is to take two measurements of each boost inductor current per sample period: $I_{min}(t_n)$ and $I_{max}(t_n)$. The third point is $I_{min}(t_{n+1})$ taken from the next sample and allows the average to be calculated as :-

$$I_{ave}(t_n) = \frac{[I_{\min}(t_n) + I_{\max}(t_n)]t_{on} + [I_{\max}(t_n) + I_{\min}(t_{n-1})]t_{off}}{2T_s}$$

=
$$\frac{[I_{\min}(t_n) + I_{\max}(t_n)]d(t_n) + [I_{\max}(t_n) + I_{\min}(t_{n-1})]d'(t_n)}{2}$$
(6.11)

where the duty cycle d is defined as :-

$$d = \frac{t_{on}}{T_s} \quad and \quad d' = 1 - d = \frac{t_{off}}{T_s} \tag{6.12}$$

and where,

 t_{on} is the time the switch is connected to V_{dc}^{-} t_{off} is the tine the switch is connected to V_{dc}^{+}
The samples taken in period t_n are used to set the duty cycle at the beginning of period t_{n+2} . This means that there is a two sample period delay in the current loops.

6.2.6 Stability

The choice of PI controller parameters for the current controllers of the rectifier was discussed in section 2.5.4.1 of Chapter 2. The analogue PWM system causes additional phase lag in the open current loop transfer function given by Eqn. 2.19. This is replaced in the digital system by the effects of a sampling delay z^{-1} . The relationship between the z-domain and s-domain is :-

$$z^{-1} = e^{-sT_z}$$
(6.13)

A two sample delay exists due to the method of averaging the current in Section 6.2.5. The function in Eqn. 6.13 when plotted against frequency f shows a constant magnitude of 0dB and a linear relationship in terms of phase lag. For a two sample delay the phase lag is :-

$$\theta = -f.2.T_s.360^\circ \tag{6.14}$$

The large additional phase lag means that the crossover frequency of the current loop f_{ci} now has to be much lower in frequency compared to the analogue counterpart to maintain stability.

If the example is taken from Section 2.7.2 with the analogue controller for a switching frequency of 15kHz, the current loop crossover frequency is chosen as $f_{ci} = 3$ kHz and by using Eqns. 2.17 -2.19 it was shown that the phase margin was 26°. Using the digital controller with two sample delays caused by averaging the current to achieve the same phase margin of 26°, the crossover frequency would have to be $f_{ci} \approx 770$ Hz, nearly four times lower. This means the gain-bandwidth product of the digital system is lower than for the analogue system and will have a worse transient response. As the controllers

operate in the d-q-n reference frame the steady-state response of the 50Hz component current should still track the reference well under all load conditions.

Choosing the open voltage loop crossover frequency f_{cv} to be 5-10 times lower than the current loop crossover frequency will maintain an adequate phase margin in the voltage loop. As f_{cv} is much lower than the sample frequency then the additional phase lag is quite small.

6.3 Predictive Average Current Controller

The second proposal for a digital control scheme is to use a predictive controller for the current loops. Transformations to the d-q-n reference frame are not required and as such should require less processing time. Also, due the nature of the predictive controller the dynamic performance of the converter should be maximized as a PI filter is not added to the current loop. A method of average current control is introduced.

6.3.1 The Basis of Predictive Control

The basis behind the predictive controller is relatively simple. The supply voltages, boost inductor currents and dc bus voltages form the inputs to the system. During each sample period the duty cycle is calculated from first principles that will force the required boost inductor current to match the reference current. Fig. 6.5 shows the four-wire rectifier. If one phase is considered then the required modulating voltage V^* to be set up at the centre-point of the switches is :-

$$V^{*} = E(t_{n}) - \frac{L(I_{L}^{*}(t_{n}) - I_{L}(t_{n}))}{T_{s}}$$
(6.15)

This assumes the supply voltage E remains constant over one sample period T_s.

6.3.2 Space Vector Modulation for Three-Wire Rectifiers

For three-wire rectifiers the three phase are coupled and so altering the duty cycle of one leg of switches will affect all three line currents. To overcome the difficulty space vector modulation (SVM) is used [50, 51, 52]. All the quantities are transformed into two phase quantities using either the α - β reference frame of the d-q reference frame. An equivalent vector equation is used for Eqn. 6.15. Eight distinct states exist for the six switches of the rectifier, two of which are the zero states corresponding to when all the upper switches are closed and when all the lower switches are closed.

The space vector diagram is shown in Fig. 6.6. The required modulating vector voltage $V^*_{\alpha\beta}$ lies in one of the six sectors. In one sample period the modulator moves between the two adjacent vectors V_k to V_{k+1} as shown in Fig. 6.7 where V_k is defined as :-

$$V_{k} = \begin{cases} \frac{2}{3} V_{de} e^{j(k-1)2\pi/3} & k = 1,...,6 \\ 0 & k = 0,7 \end{cases}$$
(6.16)

The time held in vector V_k is T_k and in the vector V_{k+1} is T_{k+1} to achieve the required modulating vector voltage :-

$$V_{\alpha\beta} = \frac{1}{T_s} (V_k T_k + V_{k-1} T_{k-1})$$
(6.17)

The remaining time of period T_s is spent on the zero states V_0 and V_7 for the periods T_0 and T_7 respectively in order to minimize the line ripple current [50] :-

$$T_0 = T_7 = (T_s - T_k - T_{k,1})/2 \tag{6.18}$$

The switching pattern in one sample period is shown in Fig. 6.8. Although each line currents changes twice per sample period there is only one switching transition per leg of switches.

6.3.3 Per-Phase Modulation

For four-wire converters the fourth wire has the effect of decoupling each phase. This means that SVM cannot be used. However, this simplifies the modulating process and no transformations to the α - β or d-q reference frames are required, although the advantage of introducing zero states is lost. A per-phase modulator is required to control each boost inductor current. The modulating voltage V^{*} in each case is realized by calculating the duty cycle required :-

$$V^{*} = \frac{V_{dc}^{*}(t_{n})t_{off} - V_{dc}^{*}(t_{n})t_{on}}{T_{s}}$$

$$= V_{dc}^{*}(t_{n})(1 - d) - V_{dc}^{*}(t_{n})d$$
(6.19)

rearranging this gives :-

$$d = \frac{V_{dc}^{*}(t_{n}) - V^{*}}{V_{dc}^{*}(t_{n}) + V_{dc}^{*}(t_{n})}$$
(6.20)

6.3.4 Average Current Control

A method was given in Section 6.2.5 to provide a calculation of the average boost inductor currents which required two measurements of each boost inductor current per sample period and leads to a two sample period delay in the current loops. An alternative method is provided here which takes advantage of the fact that the supply voltages are now made available as inputs to the system.

The proposed method is to predict the average current from first principles. Figure 6.9 shows a section of the ripple current in one of the boost inductors and its associated duty cycle. In this case single-edge modulation is assumed and the three boost inductor currents are sampled at the beginning of the on-time. As the duty cycle for period t_n was calculated in the previous sample period, the rise in inductor current Δi_{rise} , the fall in

inductor current Δi_{fall} and the average current may be predicted as :-

$$\Delta i_{rise} = \frac{[V_{de}(t_n) + E(t_n)]t_{on}}{L_{boost}}$$
(6.21)

$$\Delta i_{fall} = \frac{\left[V_{dc}^{*}(t_{n}) - E(t_{n})\right]t_{off}}{L_{boast}}$$
(6.22)

$$I_{ave}(t_n) = \frac{\Delta i_{rise} t_{on} + \Delta i_{fall} t_{off} + 2(\Delta i_{rise} - \Delta i_{fall}) t_{off}}{2T_s} + I_L(t_n)$$
(6.23)

Rearranging and substituting in d gives :-

$$I_{ave}(t_n) = \frac{T_s}{2L_{boost}} \cdot \left\{ V_{de}(t_n) \cdot E(t_n) \right] \left[d(t_n) (2 - d(t_n)) \right] - \left[V_{de}^*(t_n) - E(t_n) \right] \left[1 - d(t_n) \right]^2 \right\} + I_L(t_n)$$
(6.24)

The value of $I_{ave}(t_n)$ may be substituted for $I_L(t_n)$ in Eqn. 6.15 to enable the average 50Hz current to be tracked.

This system of average current calculation makes it possible to have only one sample delay in the current loop.

6.3.5 Practical Requirements

6.3.5.1 Hardware

The hardware requirements of the system are shown in Fig. 6.10. The system consist of the eight analogue inputs representing the boost inductor currents, the supply voltages

and the dc bus voltages. The inputs are simultaneously sampled using eight sample and hold (S/H) circuits and each one is converted in turn to a digital word using an analogue to digital converter ADC. The duty cycle is calculated within the processor and sent to the PWM circuit. Two methods of PWM are often used in digital systems :-

- The digital word representing the duty cycle is loaded into a down counter. For single-edge modulation a latch is set at the beginning of the on-time and the counter allowed to count down. When the count of zero is reached the latch is reset. The output of the latch is the PWM signal.
- The digital word representing the duty cycle is compared to a digitally generated ramp or triangular wave. The output of the comparator is either digitally high or low depending on whether the duty cycle is greater than or less than the ramp. The output of the comparator is the PWM signal.

A deadband must be added between switching in one leg of the rectifier to prevent shootthrough from occurring. This is either added in the software or in the PWM hardware circuit.

It is now possible to obtain commercially available microcontrollers that perform some or all of the data acquisition and PWM requirements on one integrated circuit (IC).

6.3.5.2 Software

The requirements of the software are :-

- read in the digital words representing the input signals
- calculate the average inductor current (Eqn. 6.24)
- calculate the modulating voltage (Eqn. 6.15)
- calculate the duty cycle (Eqn. 6.20) for each phase current

• write the duty cycle to the PWM circuit

The calculations require addition, subtraction and multiplication functions. A divide function is required for Eqn. 6.20, but occurs only once every sample period for all phases.

Fig. 6.11 shows the allocation of processor time in each sample period which is suitable for a one sample period delay. The 8 input values are converted before the calculations are performed in period t_n and the duty cycle is updated in period t_{n+1} . An alternative arrangement of processor time is shown in Fig. 6.12 which is suitable where a two sample period delay is acceptable. The A/D conversions are performed simultaneously to the calculations. The input signals converted in period t_{n-1} are used for the calculations in period t_n and the duty cycle is updated at the beginning of period t_{n+1} . A slower ADC may be used and more time is made available for calculations. However, the two cycle delay will introduce an additional phase shift (Eqn. 2.14) between the reference and the actual currents.

6.3.6 Voltage Loop

The voltage loop uses a PI filter implemented digitally. The output of the PI controller is multiplied by three sine wave templates locked to the respective utility supply phases to provide the three references to the inner current loops (Fig. 6.13).

To enable the current controllers to remain in a linear mode the slew rate of the boost inductor current (di/dt) should be high enough to track the sinusoidal references including transients. Thus the bandwidth of the voltage loop PI controller should be limited and the size of boost inductance kept as small as possible.

6.3.7 Front-End L-C Filter

A front-end L-C filter cannot be used easily on the rectifier to further attenuate the switching ripple current back to the supply. This is because the measurement of the boost inductor input voltage can no longer be assumed to be constant during one sample period and may change considerably due to the impedance of the filter. An attempt to measure the actual supply voltage rather than the boost inductor input voltage means that the dynamics of the system are completely different and Eqn. 6.15 is no longer valid.

Without the use of a front-end L-C filter a larger boost inductance must be used to minimize the ripple current fed back to the supply and reduces the available slew rate (di/dt).

6.4 Simulation Results using Predictive Control

To demonstrate the performance of a four-wire rectifier (without a front-end L-C filter) using a predictive controller with average current control, a SABER simulation has been run. The converter has the same 80kW rating switching at 15kHz as discussed in Chapter 2 and is supplied from a 400V 50Hz three phase four-wire supply. The dc bus voltage is chosen as 800V.

6.4.1 Filter Parameters and Control Parameters

The size of boost inductance is chosen using Eqn. 2.47. For a maximum ripple current of 4% $L_{boost} = 1$ mH. The per rail dc bus capacitance is chosen as $C_{dc} = 10$ mF per rail as in Chapter 2.

The PI parameters are required for the outer loop compensator. The feedback gain of the

voltage loop is chosen as $G_v = 1/100$. The inner predictive controller is set up to give a nominal closed loop gain of unity and as such simplifies the setting up of the simulation, i.e. the feedback gain of the inner current loop is $G_i = 1$. However, the current and voltage feedback signals to the predictive controller would be attenuated to realistic and safe values in practice.

Eqn. 2.36 and 2.37 are used to calculate the voltage loop PI constants. An open voltage loop crossover frequency of $f_{cv} = 40$ Hz is chosen and gives: $K_{pv} = 206$ and $K_{iv} = 26$ krads⁻¹. Setting $f_{cv} = 40$ Hz and $L_{boost} = 1$ mH enables the predictive controller to remain in a linear mode even during a step-load change on the rectifier.

The filter and control parameters are summarized below :-

 $L_{boost} = 1mH$ $C_{dc} = 10mF$ $f_{cv} = 40Hz$ $K_{pv} = 206$ $K_{iv} = 26krads^{-1}$

6.4.2 SABER Schematic

The schematic of the four-wire rectifier is shown in Fig. 6.14. The circuit consists of the six switches and antiparallel diodes, the boost inductors, the dc bus capacitors and supply. A resistive load may be switched in when required. The boost inductors are measured using $1m\Omega$ resistors. During each sample period T_s the boost inductor currents, supply voltages and dc bus voltages are sampled and held using the control block 'a2z'. A common clock pulse is used throughout.

A PI controller is implemented in the analogue domain for simplicity of simulation and the output sampled, but would have little difference compared to the PI controller implemented in the digital domain due to the relatively low voltage loop crossover frequency compared to the sample frequency. Three sine wave templates are sampled and multiplied by the output of the PI controller using the 'zmult' block to form the three current loop references.

Three predictive controllers subcircuits are used to control the boost inductor currents and the sampled voltages, currents and reference currents form the inputs to the controller. The output of the controller is the required duty cycle. The dc bus voltage is also passed through a nonlinear function to provide the inverse of the voltage which is sampled. This forms another input to the predictive controllers and simplifies the system as a divide function is not required by the sampled data system.

The predictive controller subcircuit is shown in Fig. 6.15. The equations to calculate the duty cycle and average current are implemented as a 'sampled data model' using readily available control type blocks which include addition, subtraction, multiply, sources, amplifiers and delay blocks. The upper part of the schematic calculates the required duty cycle (Eqn. 6.15 and 6.20). The lower part of the schematic calculates the average inductor current (Eqn. 6.24) and as the previous duty cycle is required to calculate the average current a delay block is required 'zdelay' which effectively holds the value from the previous clock period. The constants used in the amplifiers 'zamp' represent the sampling frequency of 15kHz and boost inductance of 1mH.

The duty cycle output of the predictive controllers are converted back to analogue values and compared to a ramp at a frequency of 15kHz synchronized to the clock frequency. A ramp is used to affect single-edge modulation and as the duty cycle is unipolar so is the ramp. The comparator could be implemented digitally in practice. The output of the comparator is used to control a switch driver, the output of which are two switch control signals, one the complement of the other for one leg of switches.

6.4.3 Steady-State and Transient Response

The transient response of the rectifier is demonstrated by using a step-load change from

no-load to full-load (8Ω resistor) at 25ms and from full-load back to no-load at 65ms. Fig. 6.16 shows the dc bus voltage and Fig. 6.17 shows the boost inductor currents and supply neutral current. Fig. 6.18 shows the supply voltage and boost inductor current on full-load.

6.5 Conclusions

Two proposals for digital control have been discussed in this Chapter. These are a digitized version of the average current mode control from Chapter 2, and a predictive average current controller.

An overview of the requirements for data acquisition and software has been given. The implementation of digital filters has been described with emphasis on practical requirements.

For the digitalized average current mode controller, a method of d-q-n transformation with reduced sine wave functions by transforming to the α - β -o reference frame first has been given to enable reduced processor computation time. Due to the method of average current measurement a two sample delay exists which can impair the bandwidth of the current loop.

The alternative method using predictive current control has the advantage of making full use of the inductor slew rate without the impeding effect of a PI filter in the current loop, thus providing good steady-state and transient response in the current loops. Transformation matrices are not required into the d-q or α - β reference frame due to the decoupling effect of the fourth wire in the rectifier and can further save on processor computation time. The principles of space vector modulation has been described as it is commonly used with three phase converter predictive controllers although it is not required here. A method of averaging the current for the predictive scheme has been

given which requires only one measurement of current per sample period and can lead to only one sample period delay.

The use of an L-C front-end filter on the rectifier can lead to the predictive scheme to fail as the input voltage to the boost inductor may not remain approximately constant during the sample period. This means that a larger size of boost inductance is required if an L-C front-end filter is not used to achieve the same switching ripple current returning to the supply. This can seriously impair the performance of the converter due to inductor current slew rate limitations.

The predictive scheme has a number of advantages over the digitized version of the scheme in Chapter 2. These include reduced computation time, a reduced number of boost inductor current measurements per sample period, and the possibility of only one sample period delay in the current loops. However the supply voltages must be measured and problems occur with the use of an L-C front-end filter.

This chapter has introduced some methods of digitizing the control of the four-wire rectifier and discussed the practical requirements and problems. Simulation results have demonstrated the performance of the rectifier with the proposed predictive controller.



Fig. 6.1 Canonic 2nd Order δ filter



Fig. 6.2 Canonic PI δ filter







Fig. 6.4 Processor Time Requirements for Average Current Measurements



Fig. 6.5 Four-Wire Boost Rectifier



Fig. 6.6 Space Vector for Three-Wire Rectifiers















Fig. 6.10 Practical Implmentation of Predictive Controller







Fig. 6.12 Processor Time Allocation for 2 Cycle Delay



Fig. 6.13 Overall Predictive Control Block Diagram



Fig. 6.14 Predictive Control Power Circuit SABER Schematic



Fig. 6.15 Predictive Control Circuit SABER Schematic



Fig. 6.16 DC Bus Voltage - Step-Load Change



Fig. 6.17 Boost Inductor Currents, Neutral Current - Step-Load Change



Fig. 6.18 Red Phase Supply Voltage and Boost Inductor Current

Chapter 7

Conclusions:

Summary, Further Work and Further Applications

7.1 Summary

This chapter concludes the research covered in this thesis; a summary is given in this section.

A topology for a three phase transformerless on-line UPS has been proposed. The topology consists of a new three phase four-wire power factor corrected reversible boost rectifier producing a balanced centre-tapped dc link, and a three phase four-wire reversible inverter. The fourth wire is the neutral of the three phase utility and is connected to the centre-point of two dc bus capacitors and to the inverter output or load neutral. The rectifier allows the removal of the conventional 50Hz transformer whilst still providing the main benefits of the transformer in applications where galvanic isolation is not required. The utility neutral and load neutral are connected together without any current flowing in the utility neutral. The four-wire rectifier is of a boost configuration and this allows a step-up facility to make up for the losses of the converter and allowing the nominal inverter output voltage to match that of the utility.

The utility neutral is maintained at zero current by balancing the three line currents equally. The control strategy used to achieve zero utility neutral current is an average current mode control scheme operating in the synchronously rotating d-q-n reference frame. This control scheme has the advantage of true average current tracking and provides zero steady-state error of the 50Hz line currents, and thus maintains accurately controlled currents under all load conditions. Power factor control is intrinsic with the

control used giving near unity power factor, or the displacement power factor may be adjusted if required.

The four-wire rectifier may also be used with an additional front-end L-C filter allowing the use of a smaller per phase boost inductance which also has the benefit of maximizing the dynamic response of the rectifier.

As the UPS is used to supply unbalanced loads a four-wire inverter is used and complements that of the four-wire rectifier. The main inverter control investigated was average current mode control to complement that of the rectifier. The use of load current feedforward was also investigated in an attempt to improve the dynamic response of the system particularly under nonlinear load conditions.

Connecting the four-wire rectifier to the four-wire inverter via the dc link provides an acdc-ac converter which can be used to form the basis of a transformerless three phase UPS. Even if a considerably large neutral current flows in the load this does not return to the utility. The utility neutral current remains zero apart from a small amount of switching frequency ripple. In an ideal sense the rectifier will not add any ripple to the dc bus voltage apart from switching ripple. The low frequency ripple components on the dc bus voltage are mainly caused by an unbalanced or nonlinear load on the inverter and as such, the dc capacitors are chosen to absorb the cyclic power from these loads. The dc bus ripple voltage will feedback to the current loop reference of the rectifier, thus causing a distortion to the utility line currents (although the utility neutral current will remain zero). A compromise between the transient performance of the rectifier voltage loop and the distortion of the line currents must be made.

The two dc bus voltages of the ac-dc-ac converter may drift apart due to unsymmetrical effects of the converters. Two methods are proposed to overcome this. The first method is a simple addition to the control, and the second method is to use an additional leg of switches and appropriate controller.

The four-wire rectifier, four-wire inverter and four-wire ac-dc-ac converter have been described in detail and include methods for determining the required filter components and controller parameters. Simulation results using SABER have demonstrated the performance of the converters under various supply and load conditions.

To demonstrate the performance of the four-wire rectifier practically, a prototype incorporating a L-C front-end filter was built as part of the research. The semiconductors devices used were IGBT's and fast recovery diodes in a modular package. The controller used was an analogue average current mode controller operating in the d-q-n reference frame. The original design of the four-wire rectifier circuit was for 1.5kW. However problems with noise occurred and as such results were taken at 200W for steady-state, transient and bidirectional power tests. The practical results compared very well to simulation results produced using SABER. Overall the prototype performed well, and notwithstanding the low power level, it nevertheless demonstrated the feasibility of the proposed rectifier.

Two proposals for digitizing the control of the rectifier have been investigated. These are a digitized version of the average current mode controller and a predictive controller. The proposed predictive controller was modelled using the SABER simulator and included a method of achieving true average current tracking. The possible advantages of the predictive controller over the digitized average current mode controller are reduced computation time, maximization of power circuit dynamics and reduced sampling delays in the current loop. However, the three phase supply voltages must be measured and problems exist when a front-end L-C filter is used on the rectifier.

Overall, the original objectives of the research have been achieved. A new four-wire acdc-ac converter provides the core to the realization of an on-line transformerless UPS and a thorough investigation has been given. The prototype rectifier built has demonstrated the practical performance of the four-wire rectifier. The proposed digital control methods provide a sound basis for future work.

7.2 Further Work

Although the overall objectives of the research have been fulfilled, the research could be extended to improve the current system and investigate alternative methods of control. Some suggestions are given in this section.

i) Controller Board Layout

General improvements to the practical prototype rectifier include a full multilayer PCB layout of the analogue control board. This would help to improve the noise immunity and allow a test to be performed at a higher power level. Further tests on the practical prototype would be to use a four-wire inverter as a load to the rectifier.

ii) Use of Realistic Models in the Simulation

The simulation results used in the thesis use ideal switching components and diodes. The practical implementation of Chapter 5 has compared the actual results with the simulation results from SABER. The two sets of results compare well and the main differences are due to power losses. A more accurate simulation would use IGBT/diode models and passive components that match the real components more closely, including the nonlinear effects of the power inductors.

Further improvements would be to model the controller with real operational amplifiers rather than control blocks. The robustness or tolerance of the system to parameter variations could also be simulated using techniques such as the 'Monte Carlo Analysis'.

iii) Digital Controllers

Two proposals for digitizing the control of the rectifier have been given in Chapter 6 and this forms the basis of the investigation of digital controllers. One of the mains areas to look at would be a method of allowing an L-C front-end filter to be used with the four-wire rectifier when using the proposed predictive digital controller. This would allow a smaller boost inductance to be used.

The predictive control relies on the use of a linear inductor to minimize the error between the reference and actual current. A method of calculating the inductance at each sample period from the measured values of voltages and currents could provide a more accurate tracking of the reference current in systems using nonlinear inductors.

The basic practical hardware and software requirements of the proposed digital controllers have been given in Chapter 6. A prototype could be used to test the principles in practice.

The use of a digital controller also would help reduce the noise problems as the control hardware is significantly reduced. The ultimate goal of the digital controller would be a one chip design including the A/D converters and PWM circuits.

iv) Alternative Inverter Control

The nonlinear loads connected to the UPS inverter requires a demanding inverter controller. The main method investigated in this thesis was average current mode control. However more robust methods could be investigated.

The use of the predictive control method proposed for the four-wire rectifier could be applied to the inverter.

v) Soft-Switching Converters

The converters used in the research are hard-switched. The use of soft-switched converter techniques could help to reduce power losses in the switching components.

vi) Improving the Voltage Loop Dynamics of the Rectifier

One of the main problems that limits the bandwidth of the voltage loop controller in the rectifier is the ripple voltage harmonics on the dc bus caused by cyclic power flows in the inverter load. These harmonics are fed back to the rectifier voltage loop and distort the current loop references. To reduce this effect the voltage loop bandwidth must be reduced considerably or a notch filter can be incorporated in the voltage loop feedback path of the rectifier. This seriously impairs the transient response of the rectifier. Thus a method of removing the harmonics from the rectifier voltage loop feedback signal without serious affect to the transient response of the rectifier is required.

7.3 Further Applications

The main purpose of the research was an investigation into the three phase transformerless on-line UPS. However, the four-wire rectifier and four-wire ac-dc-ac converter may be applied to other areas. Some suggestions are given in this section.

7.3.1 Single Converter Four-Wire UPS

The four-wire rectifier may be used as a single converter four-wire UPS. The configuration is shown in Fig. 7.1. This type of UPS has the advantages of requiring only one three-phase converter and having lower power losses compared to that of a double-

conversion UPS.

During normal supply conditions the load is connected to the utility and the rectifier operates in a rectifying mode drawing a small amount of current from the utility to charge the battery via a dc-dc converter if necessary. When the supply voltage falls out of permissible limits the load is isolated from the utility by the bypass switch and the rectifier operates in an inverting mode to supply the load from the battery via the dc-dc converter. This type of operation falls under the category of off-line UPS's.

During acceptable supply conditions the four-wire converter is used to charge the battery. However, the converter could also be used during this period as an active filter to absorb the low frequency harmonic currents that are injected into the supply by a typical UPS load. Thus the UPS configuration shown in Fig. 7.1 could allow the four-wire rectifier to have three uses: as an inverter to supply the load from the battery during a power failure, as a rectifier so the battery may be charged, and as an active filter when the utility supplies the load. The four-wire active filter is described in more detail in the next section.

7.3.2 Four-Wire Active Filter

The four-wire rectifier could be used solely as a four-wire active filter. There is much existing equipment connected to the utility, including three phase UPS's, which inject large low frequency harmonic currents into the supply. Recent European regulations have been introduced to limit the magnitude of these harmonics. Thus filtering of the mains to remove harmonic currents is becoming increasingly important. The use of active filters reduces the need for large passive component filters.

Fig. 7.2 shows a typical configuration of a four-wire active filter. The load is connected to the four-wire utility and the load line currents are measured. From the line currents

Chapter 7

feedback signals, signals proportional to the harmonic currents are extracted. The active filter is made to draw opposing harmonics to cancel the load harmonics. The four-wire active filter may also draw a neutral current to balance the supply due to a unbalanced load, and supply the required reactive power to the load.

The control of such a filter must be capable of tracking the harmonic currents accurately. One way to achieve this would be to have multiple rotating d-q-n transformations synchronized to each of the harmonic frequencies to be removed. However, such a scheme requires a large amount of hardware if done in analogue, or a large amount of processor time if the control is done digitally. A predictive controller may prove to be a more effective method.

7.2.3 Three Phase Induction Motor Drive

Three phase induction motor drives often only require three phase converters. However, using a four-wire ac-dc-ac converter for a three phase motor may prove to have certain advantages. The converter is shown in Fig. 7.3. One of the main advantages of the ac-dc-ac converter is that the star-point of the induction motor is closer to the utility neutral and earth depending on how well the currents in the motor are balanced. This can help in noise reduction, and also allows the connection of an L-C filter between the lines of the motor and neutral or earth. The ac-dc-ac converter allows regenerative braking of the motor due the converters allowing bidirectional power flow, and the rectifier is power factor corrected.











Fig. 7.3 Three Phase Induction Motor Drive

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Appendix

DSP Software Listings

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dix			DSP Listing
/* L	inker Command File */		
ORY			
/* P	rogram Memory */		
PAGE	0: VECTORS PROGRAM	:	origin = $0800h$, length = $0040h$ origin = $0980h$, length = $1280h$
/* E	Data Memory */		
PAGE	1: DATA VARIABLES CONSTANTS SINE	: : :	origin = 0100h , length = 0380h origin = 0480h , length = 0060h origin = 04e0h , length = 0020h origin = 1 c 00h , length = 1000h
	dix /* L DRY /* P PAGE /* E PAGE	dix /* Linker Command File */ DRY /* Program Memory */ PAGE 0: VECTORS PROGRAM /* Data Memory */ PAGE 1: DATA VARIABLES CONSTANTS SINE	dix /* Linker Command File */ DRY /* Program Memory */ PAGE 0: VECTORS : PROGRAM : /* Data Memory */ PAGE 1: DATA : VARIABLES : CONSTANTS : SINE :

SECTIONS

{

}

.

intvect :	{ }	> VECTORS	PAGE 0
program :	{ }	> PROGRAM	PAGE 0
.data :	{ }	> DATA	PAGE 1
.bss :	{ }	> VARIABLES	PAGE 1
constants :	{ }	> CONSTANTS	PAGE 1
sine :	{ }	> SINE	PAGE 1

DSP Listings

	title "PLL & MDAC Control	Program"	
******** ********	This program reads the index fro looks up the six sine waves and twelve MDAC's - sampling	om the phase locked loop, sends the data to the ng at 150.376kHz	******* ******** *****
*****	by Malcolm Fraser 1995		****
	.mmregs .include "math.asm" var_page: .set 9	; memory mapped re ; include mathematic ; variables at data pa	gisters macros ge 9
****	Variables .bss index,1 .bss s1,2 .bss s2,2 .bss s3,2 .bss c1,2 .bss c2,2 .bss c2,2 .bss c3,2	****	
****	Interrupt Vector Table .sect "intvect" NOP NOP NOP NOP NOP NOP NOP B tint	<pre>******* ; reset interrupt ; user interrupt 1 ; user interrupt 2 (user interrupt 3 ; timer interrupt</pre>	sed by DSK)
*****	Main Program .sect "program" LDP #0 SETC INTM splk #0aaaah,IOWSR LDP #var_page minit	******* ; disable interrupts ; i/o ports 0-15 set ; switch to variable ; maths macro initia	to 2 wait states s data page llization routine

Appendix

here:	timer CLRC INTM B here		; set up timer interrupt ; enable interrupts ; wait for interrupt
*****	Timer ISR		****
tint:	LAMM sacl index	PA0	; get index from PLL
	sacl s1 add #1365 sacl s3 add #1366		
	sacl s2 lacl index add #1024 sacl c1 add #1365 sacl c3 add #1366 sacl c2		
	lookup SAMM SAMM lookup SAMM lookup SAMM	s1 PA9 PA15 s2 PA8 PA14 s3 PA7	. .
	SAMM lookup SAMM lookup SAMM SAMM lookup SAMM SAMM	C1 PA6 PA12 c2 PA5 PA11 c3 PA4 PA10	
	RETE		

.

	.title	"Mathematic N	/lacros"		
****	Beginni	ing of sine tabl	e		****
	.sect	"sine"		0	the simulation of sing table (4006 16 bit
words)	table:		.long	U	; beginning of sine table (4090 10-bit
words)					
et e la cla cla cla cla cla cla	0	- 4 -			****
ጥ ጥ ጥ ጥ ጥ ጥ ጥ	.sect	"constants"			
			-		
• •	32-bit 2	2's complemen	t format	t 00032	43fb
	pi: pi ove	r. 2:	.long	00000	220h
	I —	-	-		
•	16-bit 2	2's complemen	t forma word	t 5555h	
		ver root two:	.word	5a82h	
	root_tv	vo_over_three:	.word	3c57h	
*****	Temno	orary variables	used in	macros	*****
	.bss	pointer.1			
	.bss	tempvar,2			
	.bss	SIGN,1			
	.bss	sa,2			
	.bss	sb,2			
	.bss	sc,2			
	.bss	sd,2			
	.bss	sx,2			
٤	.bss	scoeff,1			
	.bss	ssign,1			
	.bss	nx,2			
	.bss	st1,1			·. ·
	.bss	xt,2			
	.bss	xxt,2			
	.bss	yt,2			
	.bss	ayt,2			
	.bss	inct,2			
	.bss	index2,1			
	.bss	scoeff2,1			
	.bss	scoeff3,1			
	.bss	scoeff4,1			

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******	Macro initialization routine	*****
:	call before running macros	
,	minit: .macro	
	LDP #var_page	
	SPLK #1,st1	; set PM to 1, clear CNF
		; (B0 data space)
	LST #1,st1	; and clear SXM
	setc ovm	
•	load sine table	
	MAR AR0	
	LAR AR0,#table	; start of sine table
	LDP #0	
	SPLK #1000h,BRCR	; 4096 points
	LDP #var_page	
	stvar xt,12afh,9b78h	; initial value is -pi (*16384
	stvar inct,90feh,000ch	; to improve resolution)
	RPTB end_bk-1	
	loadacc xt	
	ABS	
	RPT #12	
	SFR	
	BIT xt+1,0	
	BCND jumpw?,NTC	
	NEG	
jumpw?:	stacc xxt	
	sin xxt,yt	
	loadacc yt	
	ABS	
	stacc ayt	use only low order hits
	conv yt,scoen4	, use only low order bits
	BII ayt+1,15	
	BCND Jumpx:,MTC	\cdot make sure answer is $< \pm 1$
		, make bare and the lot is the
	$\frac{D11}{PCND} = \frac{1}{10000000000000000000000000000000000$	•
	LACC #8001b	: make sure answer is > -1
	B jumpy?	,
	LACI scoeff4	
jumpx?:	ADD #8000h	; convert to offset binary
յսութչ։	SFR	; use only 12-bits
	SFR	· -
	SFR	
	SFR	

DSP Listings

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end_bk:	CMPL AND #0fffh SACL *+,0 loadacc xt addacc inct stacc xt NOP .endm	; correct sign
******* loadacc	Load acc with 32-bit variable .macro var lacl var add var+1,16 .endm	****
***** stacc	Store acc in 32-bit variable .macro var sacl var sach var+1 .endm	****
****** Stvar	Store value in 32-bit variable .macro var,numl,numh splk #numl,var splk #numh,var+1 .endm	******
****** addacc	acc=acc+var .macro var ADDS var ADD var+1,16 .endm	******
****** subacc	acc=acc-var .macro var subs var sub var+1,16 .endm	****
******* mult	acc=coeff*var (for +ve coeff) MACRO COEFF,VAR CLRC SXM LACL VAR+1	*****

J.

·	SACH SIGN LACC VAR ADDS VAR ABS SACH temp SACL temp LT COE	I,1 +1,16 var+1 var FF tempyar	• .
	PAC	tempvat	
	BSAR 16		
	MPY temp	var+1	
	BIT SIGN	1,15	
	APAC		
	BCND	B2?,NTC	
	ADD #1		
B22	NOP		
D2;	ENDM		
******	acc=coeff*v	ar (for +ve var and c	oeff) *******
multp	.macro COE	FF,VAR	
-	LT	COEFF	
t	MPYU	VAR	
	PAC		
	BSAR	16	
	MPY	VAR+1	
	APAC		
	.enam		
			·
*****	y=sin(x) (-p	i <x<pi)< td=""><td>****</td></x<pi)<>	****
sin	.macro x,y		
	loadacc	X	
	BCND	jump3?,GEQ	· · · · · · · · · · · · · · · · · · ·
	NEG		
Jump3?:	stacc nx		aload assumbtion with ni/2
	loadacc	pi_over_2	, load accumator with pb2
	SUDACC IIX	jumn12 GEO	
	DCIND	jumpr.,ODQ	load accumlator with pi
	subace ny	h	,ioad accommator with pr
	R iumi	n27	
jump1?	loadacc	nx	; load accumulator with x
1 L			· ·

iumo2?:	BSAR 1	
JF	stacc sa	: store x/2 in vara
	BSAR 1	,
	SACL scoeff	: store x/2 in coeff
	multp scoeff.sa	,
	stacc sb	; store $(x/2)^2$ in varb
	multp scoeff.sb	, , , , , , , , , , , , , , , , , , ,
	stacc sc	; store $(x/2)^3$ in varc
	BSAR 1	, , ,
	SACL scoeff	; store $(x/2)^3$ in coeff
	multp scoeff,sb	
	stacc sd	; store $(x/2)^5$ in vard
	SPLK #1111h,scoeff	; $coeff = 2/15$
	multp scoeff,sd	
	stacc sd	; vard = $x^{5}/(2*5!)$
	SPLK #5555h,scoeff	; $coeff = 2/3$
	multp scoeff,sc	; calculate x^3/(2*3!)
	neg	
	addacc sd	
	addacc sa	
	SFL	
	BIT x+1,0	
	BCND jump4?,NTC	
	neg	
jump4?:	stacc y	
	.endm	
****	convert variable v to coefficent form	nat *****
conv:	.macro y,coeff	- pr
	LACL y	; load low order bits
	BSAR 1	; shift them right 1 bit
	AND #7fffh	; remove top bit
	BIT y+1,0	; test sign bit of y variable
	BCND jump7?,NTC	
	OR #8000h	; set bit
jump7?:	SACL coeff	
	.endm	
*****	acc=coeff*var (no restrictions)	****
multn	.macro coeff,var	
	BIT coeff,0	
	LACL coeff	

DSP Listings

.

jump8?: jump9?:	BCND NEG SACL scoeff2 MULT BIT coeff,0 BCND NEG NOP .endm	jump8?,NTC scoeff2,var jump9?,NTC	· · ·
******* ******* lookup:	sine lookup tal 12-bit offset bi .macro index LACL index AND #0fffh ADD #table SACL pointer MAR *,AR0 LAR AR0,pu LACL *,AR0 .endm	ble 0<=index<=4095 re inary in accumulator	eturns ******* ******
****** ; timer:	Set up timer in Tout = 20MHz .macro LDP #0 SPLK #132,P OPL #8,IMH SPLK #20H,7 LDP #var_p .endm	nterrupt z/133 (set by PRD) RD R FCR age	****

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 $C_{\rm eff}$