Novel Manufacture of Out-of-Plane Optical Interconnects to Enable Low-Cost OECB Substrates

by

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Glossary

ACF	Anisotropic conducting films
ADM	Add Drop Module
AIT	Advanced Interconnection Technology Incorporated
AON	All Optical Network
ATM	Asynchronous Transfer Mode
BGA	Ball grid array
BERT	Bit-Error Rate Tester
BFA	Bare Fibre Adaptor
CCITT	Consultative Committee for International Telephone & Telegraph
CD	Chromatic Dispersion
CMOS	Complimentary Metal Oxide Semiconductor
CO	Central office
CSP	Chip-Scale Package
CWDM	Coarse Wavelength Division Multiplexing
CTE	Coefficient of Thermal Expansion
CVD	Chemical Vapour Deposition
DCA	Direct Chip Attach
DCA	Digital Communications Analyser
DBR	Distributed Bragg Reflector
DFB	Distributed Feed Back
DLL	Data Link Layer
DOE	Design of Experiments
DSF	Dispersion Shifted Fibre
DWDM	Dense Wavelength Division Multiplexing
ECOC	European Conference on Optical Communications
EDFA	Erbium Doped Fibre Amplifier
EDTFA	Erbium Doped Tellurite based Fibre Amplifier
EMS	Electronic Manufacturing Service
EOCB	Electro-Optical Circuit Board
EPO	European Patent Office
FBG	Fibre Bragg Grating
FC	Fibre Channel
FCA	Flip Chip Attach
FOA	Fibre Optical Amplifier
FOB	Fibre On Board
FP	Fabry-Perot
FSOI	Free Space Optical Interconnects
FTTC	Fibre To The Curb
FTTH	Fibre To The Home
GI	Graded Index
GRIN	Gradient Index
IC	Integrated Circuit
ICA	Isotropic Conducting Adhesive
IL	Insertion Loss

IO	In / Out
IP	Internet Protocol
IPA	IsoPropyl Alcohol
IR	Infra Red
ITU	International Telecommunication Union
IZM	Institut Zuverlässigkeit und Mikzointegration
LAN	Local Area Network
LD	Laser Diode
LED	Light Emitting Diode
LIGA	X-Ray Lithography
LP	Light Path
MAN	Metropolitan Area Network
MCM	Multi-Chip Module
MEMS	Micro-Electro Mechanical Systems
MFD	Mode Field Diameter
MM	Multi mode
MOEMS	Micro-Optical-Electro Mechanical Systems
MUX	Multiplex
NA	Numerical Aperture
NRZ	Non Return to Zero
NZDSF	Non Zero Dispersion Shifted Fibre
OADM	Optical Add Drop Module
OC	Optical Carrier
OE	Optical-Electrical / tronic
OEC	Optical Edge Connector
OECB	Opto-Electrical Circuit Board
OEM	Original Equipment Manufacturer
OIF	Optical Interconnecting Forum
OSA	Optical Spectrum Analyser
OSI	Open Systems Interconnection
OTMS	Optical Technology Manufacturing Service
OXC	Optical Cross Connect
PC	Patch Cord
PCA	Printed Circuit Assembly
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PD	Photo Diode
PDL	Polarisation Dependant Loss
PDU	Protocol Data Unit
PLC	Planar Lightwave Circuit
PM	Polarisation Maintained
PMD	Polarisation Mode Dispersion
POF	Plastic Optical Fibre
POP	Point Of Presence
POS	Packet Over SONET
PSU	Power Supply Unit
QoS	Quality of Service
RF	Radio Frequency
RIE	Reactive Ion Etching
RX	Receiver
RZ	Return to Zero
SAN	Storage Area Network
SBB	Stud Bumb Bonding
SDH	Synchronous Digital Hierarchy

SEM	Scanning Electron Microscope
SFP	Small Form Pluggable
SMF	Single Mode Fibre
SMT	Surface Mount Technology
SOA	Semiconductor Optical Amplifier
SONET	Synchronous Optical Network
SOP	State of Polarisation
STM	Synchronous Transfer Mode
SWS	Swept Wavelength System
TCP	Transmission Control Protocol
TDFA	Terrium Doped Fibre Amplifier
TDM	Time Domain Multiplexing
THT	Through Hole Technology
TIR	Total Internal Reflection
TM	Terminating Module
TRX	Transceiver
TV	Television
TX	Transmitter
UBM	Under Bump Metallisation
USF	Un-Shifted Fibre
USR	Ultra Short Reach
UV	Ultra Violet
VCSEL	Vertical Cavity Surface Emitting Laser
VSR	Very-Short Reach
WAN	Wide Area Network
WDM	Wavelength Division Multiplexing
WEEE	Waste from Electric and Electronic Equipment (Directive)
XC	Cross Connect

Abstract

Due to their bandwidth capacity, optical interconnects are beginning to replace bandwidth limited copper as bottlenecks appear on both inter-board, VSR interconnects and also inter-board, USR interconnects. Consequently, low-cost, optically enabled circuit boards are a key milestone on electronic roadmaps. Benefits exist in developing guided wave technologies, which have been classified into three generations. First and second generation technologies are based upon optical fibres and are both capable of providing a suitable platform for inter-board applications. However, to allow component assembly, an integral requirement for intra-board applications, low-cost 3rd generation OECBs containing embedded polymer waveguides are desirable.

The current barrier to the deployment of OECB architectures is the out-of-plane coupling between components and the waveguides. Integrated mirrors combine 90° deflecting mirrors into the OECB and provide an improved method compared to assembled mirrors. A novel two-step, integrated mirror fabrication process is presented in order to improve on IL results achieved by Intel of 1.5 – 3 dB.

The fabrication process comprises ablating an undercutting pocket, which is backfilled with electroplated copper in order to create a reflective interface at the undercutting polymer boundary. The mirrors are characterised using a prepared demonstrator. Sufficient results were achieved from initial trials to prove the process. Process issues that require addressing are: laser focus, mask alignment, copper overfilling, and fibre coupling to demonstrator. Characterisation of initial one-dimensional mirrors recorded an average IL of around –9dB. Mirrors with said IL are not suitable even for USR applications. The IL can be attributed to a large (200μm) reflected spot size on the top of the OECB substrate.

Accordingly, two-dimensional mirrors that are fabricated using the same process set-up as one-dimensional mirrors only with a shaped mask were fabricated and characterised. Analysis of the IL results concludes that two-dimensional mirrors are capable of averaging –2.9dB, which is sufficient to drive the further work necessary to deploy OECB architectures with integrated two-dimensional mirrors. Three-dimensional mirrors should also be investigated.

Chapter 1

Introduction

1.0 Telecommunication Networks

Driven by the demand for greater bandwidth across the telecommunications network, board level optical interconnects are important milestones on technology roadmaps. Architectures for providing both high-speed backplanes across telecommunication equipment and greater bandwidth between Integrated Circuits (IC) assembled onto Printed Circuit Boards (PCB) are required. Low-cost optically enabled PCBs, which include optical links driven by Vertical Cavity Surface Emitting Lasers (VCSEL), are therefore being developed in order to replace bottlenecks created by copper tracks.

The development of telecommunications, a combination of the Greek *tele*, "over a distance", and *communications*, "exchange of information", has greatly enhanced many areas of modern life, penetrating both the home and the workplace [1]. End users around the world interface with equipment, such as telephones, televisions (TV), and computers, exchanging three basic types of information: voice, video, and data [1-4]. The basic construction of telecommunication links consists of a transmitter, transmission medium, and receiver. The transmitter maps the data from the interfacing equipment, based on a given structure, and transmits it down the physical circuitry to the receiver, which decodes the data and displays the information back in to its original form.

Telecommunication links operate two principles of transmission: analogue and digital [5]. Analogue signals carry information through amplitude, frequency, and phase, which is error prone due to noise and other distortions resulting in the incorrect decoding at the receiver. Digital signals carry information in a data stream of binary code consisting of a series of logic high and low bits. Legacy analogue signals, such as voice, can be digitalised using the Pulse Code Modulation (PCM) technique, which samples the analogue signal at time periods and represents the values as digital numbers. Although this requires an increase in the amount of data transported over the link, the greater resilience to noise and distortions coupled with the ability to transmit data has established digital signals as the preferred transmission method.

1.1.1 Optical Interconnects

Whilst there are many important characteristics of telecommunication links such as security, speed, and reliability; in the wake of the digital era, the fundamental link property is unquestionably information carrying capacity. As demonstrated by the Shannon-Hartley theorem, capacity is proportional to the channel bandwidth, which in turn is proportional to the frequency of the carrier [1]. This formula, drawn from information theory, is true regardless of specific technology and highlights the issue that bandwidth capacity is ultimately limited, not by technological advances, but by carrier frequency: a physical property of the transmission signal. Defined by this theorem, the bandwidth capacity of a link can be incrementally increased by moving from copper, the foremost transmission medium, to twisted pairs, Radio Frequency (RF), and microwaves (satellite channels), through to light, which has the highest frequency and therefore the greatest bandwidth potential [1].

The vast bandwidth potential offered by optical links over traditional electrical links first became a commercial reality during the 1970s as technological advances, such as the development of edge-emitting Laser Diodes (LD) and Single Mode Fibres (SMF), enabled optical links to supersede copper in long distance telecommunications [6-8]. Through the subsequent decades, copper became redundant over reducing distances as it struggled to provide for the bandwidth explosion generated by three driving factors: the increasing base of global end-users, popularity of services such as the internet, and the emergence of data intensive applications such as video conferencing [6]. The modern telecommunications infrastructure is therefore a global mesh of optical networks able to offer a plethora of multimedia services (Figure 1.1).

To ensure global compatibility, various transmission standards have been adopted such as Synchronous Optical Network (SONET), Asynchronous Transfer Mode (ATM), and Ethernet. These standards, explored in references [9-13], govern link specifications from data protocol to loss budgets. Due to the varying function and link distance, protocols vary across the interconnecting networks, which are typically organised into three market-segments: long-haul, Metropolitan Access Networks (MAN), and Local Access Networks (LAN) (Figures 1.1 + 1.2) [14]. Although link

distances reduce, each market segment cannot simply be a scaled down version of the larger due to the varying traffic each network handles. The market segments have specific requirements on the cost and performance of the transmission equipment.

1.1.2 Transmission Equipment for Optical Interconnects

Long-haul networks span both regional and extended geographic distances, connecting MANs to extend global connectivity between regional domains [6, 15, 16]. Due to the long distances and the deployment of Dense Wavelength Division Multiplexing (DWDM), to provide for the huge bandwidth required at each link, high performance single-mode transmitters are required. For this reason, edge emitting Distributed Feedback (DFB) LDs transmitting around the 1550nm wavelength (c-band) have established themselves as the technology of choice for long-haul applications. DFB LDs give unrivalled performance in areas such as: single mode stability, power output, line-width, and wavelength selection [15]. In achieving such performance, components become dominated by performance rather than cost.

MANs operate over much reduced link distances, aggregating access traffic, generated by the user, through the regional MAN to corresponding MAN Central Offices (CO), also called the Point Of Presence (POP) [17, 18]. Each CO contains switches and routers that interconnect LAN or access networks both to each other and to the backbone for global communications between end users. Although DFB LDs exceed the performance requirements of the metro space, they are uneconomical due to cost. Consequently, cheaper Fabry-Perot (FP) lasers that transmit at the 1310nm wavelength are frequently used as link lengths decrease [9].

Access networks have predominantly the shortest link-lengths of the three-telecommunication network segments, between several hundred to several thousand metres. Since a high premium for optical channels would not persuade operators to switch from simpler and cheaper copper-based interconnects with proven reliability, access networks are the most sensitive to cost [1-3, 19]. From this standpoint the most important breakthrough in deploying optical interconnects across shorter links was the development of the VCSEL in the late '90s. Operating in the 850nm window, short-wavelength multimode VCSELs provide a cost effective solution with ample

performance density to operate over access network links. VCSELs have dominated the optical access market in recent years, their many inherent advantages include: low-cost due to high volume manufacture and in production testing at the wafer level; ultra-high modulation rates; low power consumption with threshold currents less than a milliamp; and lower coupling tolerances to fibre due to the circular beam output when compared to the oval output of edge emitting lasers.

DFB, FP, and VCSEL transmission lasers dominate their respective markets. However, a recent downturn in the telecommunications industry has prompted a rationalisation of the performance and packaging of the devices that has increased the competition in each market segment from both new technologies and also the spread of the developed sources. The most important issue that the rationalisation addressed was cost reduction. It is widely accepted that of the final module's cost, packaging constitutes between 85%, for LDs in butterfly packages [15], and 33%, for lower specification VCSELs [20]. Integrating the transmitter, receiver, and electronics into a standard transceiver package has proved successful at reducing costs [15, 21]. Small Form Factor Pluggable (SFP), VCSEL transceiver modules are offering an alternative to copper in Very Short Reach (VSR) interconnects, between 10m and 300m, as copper creates bottlenecks inside the telecommunication CO and POP.

The successful emergence of VCSELs in the VSR arena has renewed the long anticipated wait for optical solutions to Ultra Short Reach (USR) interconnects, distances less than 10m and predominantly based on circuit boards.

1.1.3 Very Short Reach Optical Interconnects

Network providers are required to connect co-located CO equipment with multiple, high-speed VSR optical interconnects to prevent bottlenecks developing [17, 18, 22]. As network providers exploit the increased bandwidth capacity provided by the installation of high-bandwidth fibre across the network and between telecommunications switches, capacity bottlenecks are occurring inside the CO. Interconnects inside the CO can be divided into several levels (Figure 1.2). The longest links inside the CO are VSR interconnects. VSR interconnects span between co-located equipment and cover distances between 10m and 300m. Traditionally, CO

equipment has been connected by copper based VSR interconnects, but the move toward data rates of 10 Gbps and beyond is pushing these links to their limits, so increasingly optical interconnects are being considered. Since the majority of CO equipment tends to be physically located within the same building, a significant proportion of these links are less than 300m, where it is uneconomical to deploy optical interconnects operating over standards optimised for longer distances. Subsequently, the Optical Internetworking Forum (OIF) has developed a set of VSR optical interconnection standards aimed at delivering low-cost interconnects between co-located equipment (<300m) [23]. VSR leverages technology developed for Gigabit-Ethernet, transporting OC-192 (10 Gbps) traffic. Parallel optical VCSEL channels are deployed except where SMF already exists.

The OIF set of VSR standards (Table 1.1), have enabled low-cost optical interconnects, based on VCSEL technology, to replace copper connections between co-located equipment inside the CO. However, this migration from long haul to VSR, despite repeated predictions [24, 25], has taken over two decades. The delay occurred due to problems in overcoming the technology challenges of manufacturing optical interconnects in large volumes and with sufficient performance but also at a lower cost than electrical interconnects. With optical interconnects being widely deployed across VSR links, the same technological hurdles are again being addressed as optical interconnects look to migrate onto USR interconnects within the CO equipment. USR interconnects are less than 10m and predominately based on PCBs (Figure 1.2).

It is expected that on-board optical interconnects will have an impact across a broad spectrum of the electronics market, with demand expected to increase significantly by 2010 (Figure 1.3). The drive to migrate optical interconnects into USR distances, less than 10m, is currently coming from two main directions. The first directly follows the implementation of VSR optical links inside the CO. To prevent bottlenecks forming on the backplanes of the equipment low-cost inter-board optical links to transport OC-192 traffic between daughter cards on a backplane are required. The second driving force toward board-level USR optical interconnects is concerned with intra-board applications, specifically; the increase in bandwidth capacity between ICs. Low-cost optically enabled circuit boards have therefore become a key milestone in electronic roadmaps (Figure 1.4) [26-28].

Table 1.1 ***OIF Implementation Agreements for VSR Interconnects:*** *four implementation agreements have been developed for transmitting OC-192 traffic (10 Gbps) across VSR interconnects. VCSELs are used for the MMF standards. FP lasers operate over the SMF standard.*

OIF agreements	Distance	Fibre characteristics			Wavelength
		Type	Number	Data rate	
OIF-VSR4-01	<300 m	MMF	12	1.25 Gbps	850 nm
OIF-VSR4-03	<300 m	MMF	4	2.5 Gbps	850 nm
OIF-VSR4-05	<600 m	SMF	1	10 Gbps (OC192)	1310 nm
OIF-VSR4-04	<85 m	MMF	1	10 Gbps (OC192)	850 nm

1.2 Celestica Limited

The author is an original member of Celestica's global Opto-Electronic (OE) development team and, funded through this industrially sponsored case award, pioneered the development of optically enabled circuit boards within the company.

Celestica Limited is a world leader in the delivery of innovative Electronic Manufacture Services (EMS). Original Equipment Manufacturers (OEM) have strategically outsourced electronics manufacture to EMS providers because of their specialised technology development and process capability, which enables OEMs to rapidly bring products to market without significant capital investment [29]. Operating from a global manufacturing network of more than 40 facilities and employing over 40,000 personnel, Celestica provides a broad range of services to leading OEMs, with products spanning a large number of industries. Although Celestica offers design, prototype, test, and repair, its services are based on a core competency of Printed Circuit Assembly (PCA). The trend towards miniaturisation of electronic products has encouraged the development and widespread use of Surface Mount Technology (SMT) throughout the PCA industry. Celestica has developed SMT processes capable of manufacturing electronic circuit boards in high volume and at low-cost.

1.2.1 Company Position on USR Optical Interconnects

OEMs producing optical components and equipment for the telecommunications networks are also strategically outsourcing manufacture. To satisfy this demand, Celestica introduced Optical Technology Manufacturing Services (OTMS) to its portfolio. To achieve global OTMSs, Celestica set up Opto-Electronic (OE) centres of competence, in order to introduce to each region the necessary OTMSs such as: fibre management, fibre splicing, fibre alignment, and optical test. The centres of competence also contain significant research capabilities.

Celestica is committed to developing the OTMS processes of the future in order to remain competitive in a fast changing environment. As such, it has identified the low-cost assembly of optically enabled PCBs as a key element in its research roadmap.

1.3 Details of Research

1.3.1 Problem Statement

Due to the bandwidth limitations of copper and in order to both relieve the bottlenecks appearing on CO telecommunications equipment and to provision for future clock speeds between ICs, optically enabled PCBs are required. To this end the aim of the research is to develop an optically enabled PCB architecture and to promote the architecture by producing a technology demonstrator.

It is necessary for the optically enabled PCB to provide optical links that meet the requirements for both intra- and inter-board USR interconnects. Therefore a major specification of the developed architecture is to allow the direct assembly of active SMT devices onto the substrate. In order for the developed architecture to be applied across many core areas of electronics and optics, the technology demonstrator should employ low-cost technologies and high-volume processes. To date no architectures meet these specifications. As an optical PCB architecture is a major milestone on electronic roadmaps and is also an enabling technology toward photonic computing, it is paramount that a suitable architecture is developed.

1.3.2 Research Objectives

In order to develop a technology demonstrator to showcase a low-cost architecture for integrating VCSEL driven optical interconnects into PCBs, the objectives of the research in this thesis are:

(i) To investigate optical approaches to resolve USR bottlenecks across copper traces on PCBs and to identify the candidate architecture most capable of providing both inter-board and intra-board aggregation of a VCSEL beam.

(ii) To ascertain which areas of research require further development in order to manufacture and assemble the optical PCBs, in particular in achieving the passive alignment of the active optical devices (e.g. VCSELs and PDs)

(iii) To develop a novel manufacturing process capable of integrating a light coupling mechanism into the PCB fabrication process, which enables SMT mounted devices to communicate across the optically enabled circuit board.

(iv) To investigate the effects of the main manufacturing processes and to characterise the optical performance of the formed structures.

1.3.3 Contribution to the Body of Knowledge

This thesis contains details of a novel manufacturing process for combing the optical coupling of a VCSEL and PD into the manufacture of an optically enabled PCB. The method improves on previous techniques as it enables the direct coupling of the active components without the need for ancillary equipment and their associated manufacturing costs and tolerance errors. The equipment necessary to complete the manufacturing process is detailed and the important process parameters are highlighted. The research characterises the optical coupling mechanism and identifies the coupling attenuation achieved at the junction. Prototypes have matched the 3dB attenuation at the junction achieved with alternative methods. At the present stage of development, the process is hand operated and the manufacturing is not optimised.

1.4 Structure of Thesis

Chapter 2 gives an overview of USR optical interconnects. FSOIs and guided wave technologies are identified in the literature review as the two methods for incorporating USR optical interconnects into the PCB. Guided wave technologies can be classified into three generations. First and second generation technologies are based upon optical fibres and although both are capable of providing a suitable platform for intra-board applications, to allow inter-board applications that require component assembly, 3rd generation OECBs containing emended waveguides are desirable.

Current OECB waveguide technologies are reviewed in Chapter 3, including: a study of waveguides and waveguide manufacturing technology; a review of VCSEL construction, assembly and packaging; identification of the current interconnection challenge to couple light out-of-plane to the OECB; a review of alternative approaches to achieve the change in direction, including a detailed patent search. Finally, a market gap is identified.

In order to resolve the interconnection challenge, a novel manufacturing process for integrating mirrors into OECB substrates is presented in Chapter 4. An OECB demonstrator is introduced with the aim of showcasing the integrated mirrors. Finally, the rationale behind the adopted research methodology is explained.

Chapter 5 introduces the laser ablation manufacturing process. The laser process parameters and also the results from the initial trials into the ablation of the angled pockets using a prototype jig are analysed. In order to achieve repeatable and desirable structures, specifications for an optical head to replace the jig are detailed. The results are evaluated and the key process parameters are identified.

Chapter 6 identifies the possible methods for coating the mirrors to improve upon the efficiency results achieved over TIR mirrors. The selection of electroforming is explained and details of the experimental activities and results given. The key process parameters are identified.

Chapter 7 details the experimental rig design that was assembled to enable the fabricated mirrors to be characterised. The results are analysed.

Methods for improving the optical coupling are suggested and the benefits of each method discussed in Chapter 8. Finally, the design set-up for manufacturing shaped off-axis parabolic mirrors is discussed and the initial results examined.

Conclusions on the research conducted are presented in Chapter 9 and Chapter 10 contains suggestions for further work.

1.5 Summary

An introduction to optical interconnects is given. Due to their bandwidth capacity, optical fibre interconnects rapidly replaced copper in telecommunications networks. VCSELs dominate short-link markets due to cost benefits. Optical interconnects are beginning to replace bandwidth limited copper as bottlenecks appear on VSR interconnects between co-located CO equipment. The limitations of copper are currently creating both inter-board bottlenecks on the backplanes of CO equipment and also inter-board issues between next generation ICs. Consequently; low-cost, optically enabled, circuit boards are a key milestone on electronic roadmaps. The sponsoring company, Celestica, is an EMS provider, which offers OTMS capabilities and has identified the development of an optically enabled PCB as a crucial research project. The research objectives are given in order to develop a technology demonstrator. Finally, an overview and structure of the thesis is given.

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Figure 1.1 ***Optical Network Hierarchy:*** *the three market segments, long-haul, MAN, and LANs interconnect at the CO to route traffic between global end users – Sorrento Networks [14].*

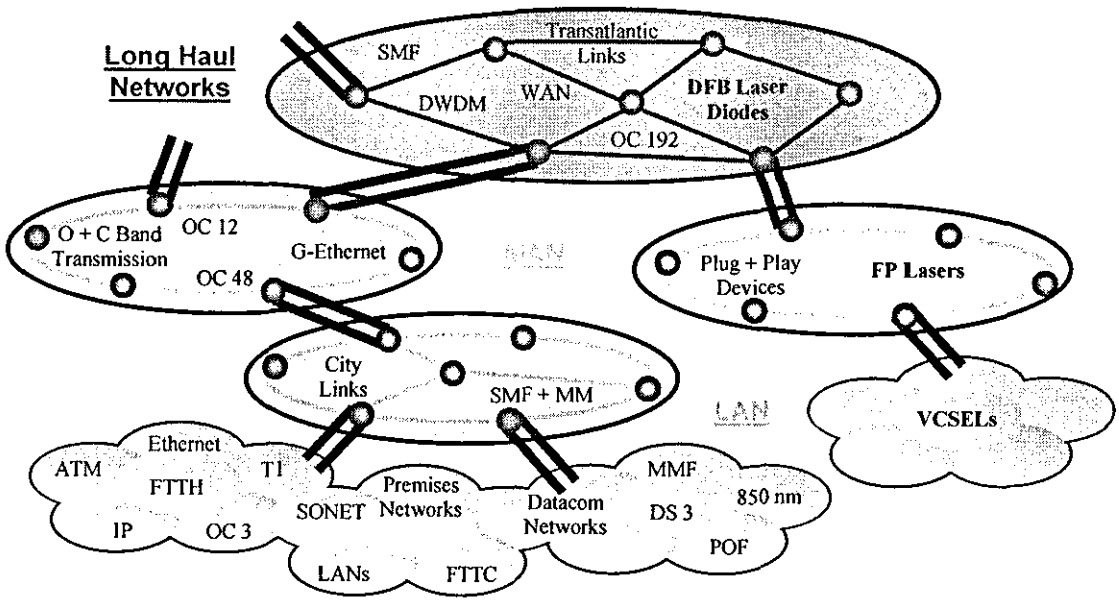


Figure 1.2 ***Interconnect Levels Inside CO Equipment:*** *VSR interconnects connect co-located CO equipment and are the longest inside the CO. USR interconnects (<10m) exist between backplanes and also include board level interconnects on the backplane and daughter cards.*

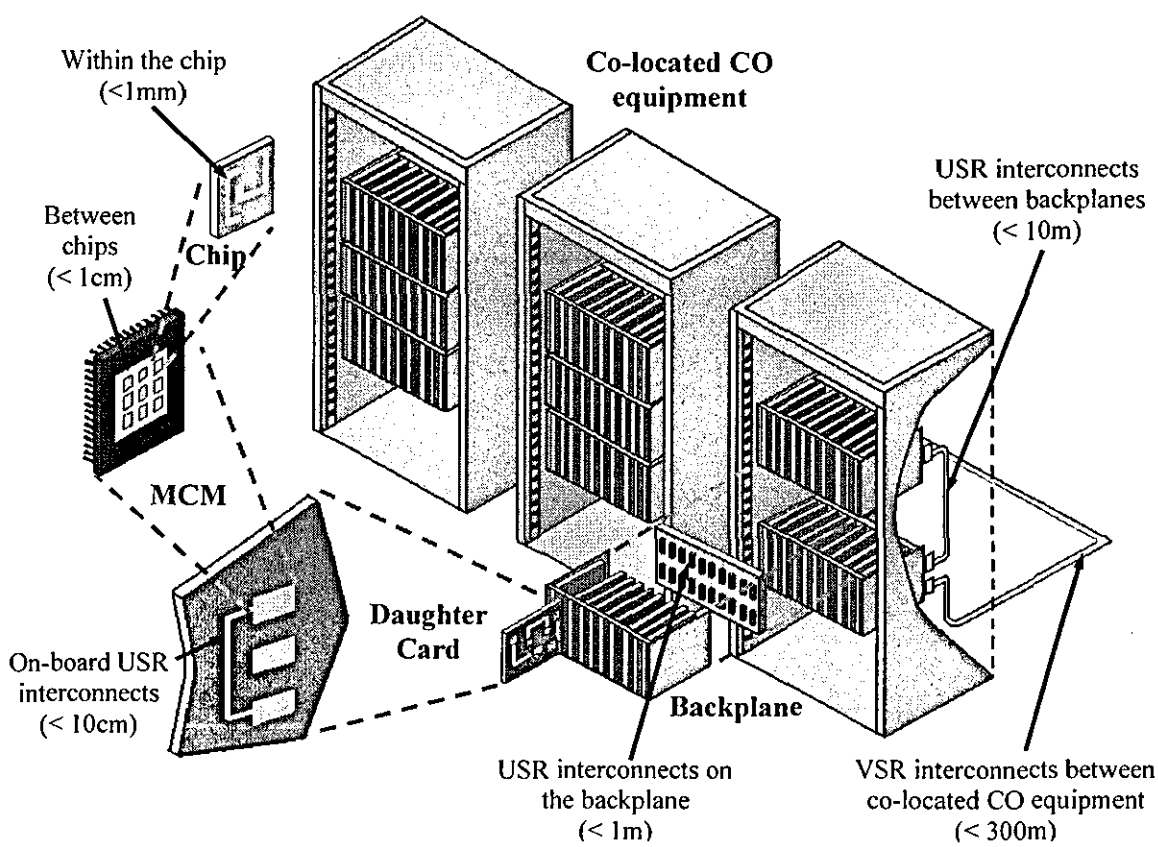


Figure 1.3 ***Predicted Growth of Optical Boards and Backplanes:*** *forecasted growth by ElectroniCast predicts a steady increase in optically enabled PCBs [30].*

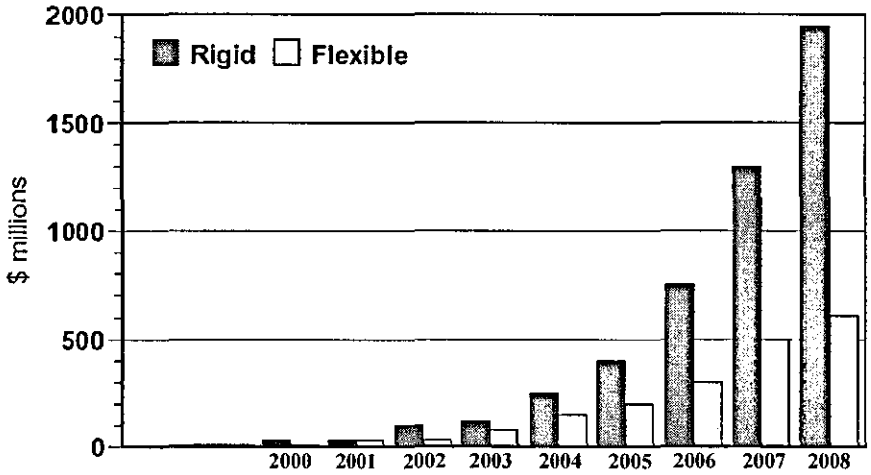
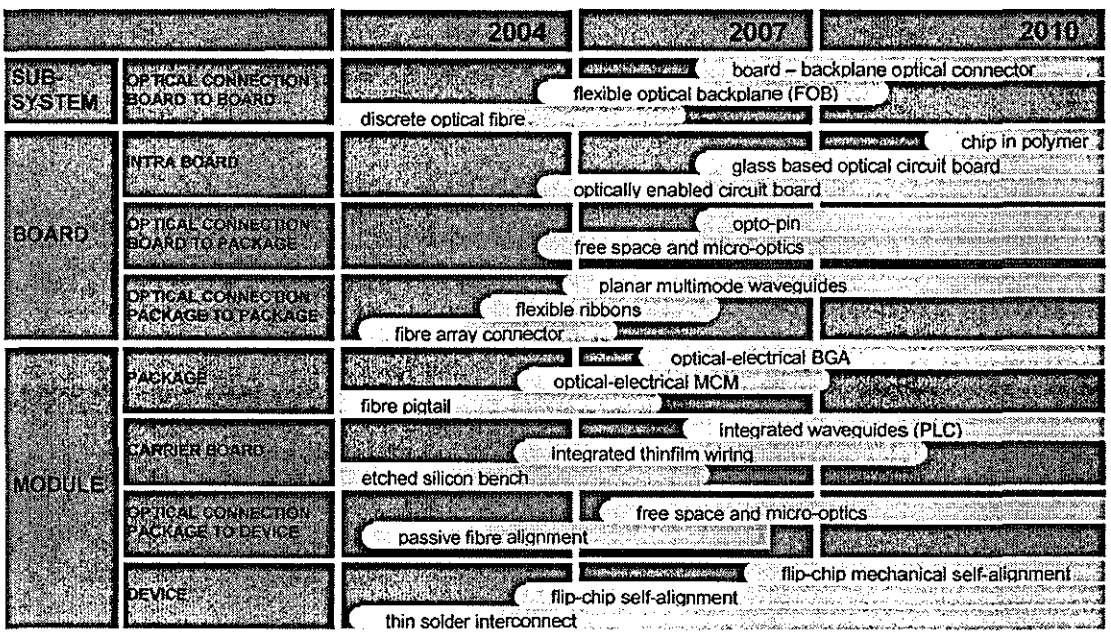


Figure 1.4 ***Photonic Packaging Roadmap:*** *packaging roadmap for OE and photonic integration at board, package, and device level - Fraunhofer IZM [26]*



Chapter 2

First and Second Generation Technologies

2.0 USR Optical Interconnects

Demand for greater bandwidth is continually increasing in both the telecommunications and consumer markets [1]. Driven by the need to increase the bandwidth capacity for both inter-board and intra-board interconnects, low-cost optically enabled PCBs are being sought to supersede USR copper interconnects.

USR interconnects span distances between a few centimetres and a few metres, connecting ICs that are mounted on to PCB substrates. Due to cost and performance benefits, FR-4 is the preferred substrate material. FR4 consists of a woven glass base laminate held together by an epoxy resin [2-4]. The woven glass layers provide the substrate with structural stability, whilst the resin provides ductility. Besides the base epoxy, the resin also contains chemicals such as curing agents, stabilising agents, flame-retardants, and adhesion promoters, all of which enhance the substrates performance. Conductive tracks are created on the FR-4 sheet by either an additive process, where copper is plated on to the surface, or by a subtractive process, where the tracks defined by selective etching of a copper layer coated on the FR-4.

For high-data applications the substrates are almost exclusively multi-layer PCBs, which are formed with layers of precisely aligned FR-4. The FR-4 layers are aligned to each other using mechanical fiducials and bonded together by applying heat and pressure [4-6]. A temperature of about 170°C at a pressure of about 1470 kPa is needed to laminate FR-4 material over the course of more than one hour [7]. The copper conducting tracks created on each of the FR4 sheets are connected by vias, formed by drilling holes and plating the sides with copper. To insure the integrity of the circuit, careful design of the board and traces are required. The outermost surface of the PCB contains pads to allow SMT component assembly.

The SMT process has been extensively researched and documented [8-10], and generally consists of first depositing solder paste onto the solder pads. Solder paste consists of solder particles suspended in a liquid carrier containing mainly flux,

activators, solvents, and rheology modifiers. Eutectic tin-lead solder alloys (63% Sn / 37% Pb by weight) are the most commonly used; however, legislation is coming into effect that requires lead-free solders to be used after January 1st 2006 [11]. After the solder is deposited, components are mounted on to the surface of the board and held in place by the tackiness of the paste. The populated PCB passes through a reflow process where the solder paste melts and solidifies to form the solder joint. Standard temperature profiles for reflowing tin-lead and lead-free solders are shown in Table 2.1 (page 17). Lead-free solders need higher temperatures to reflow. The solder joint provides both the electrical in/out (IO) and the mechanical attachment to the PCB.

One of the main driving forces in electronics is to create products with both greater functionality and also reduced footprint. This has directly affected SMT device packaging initiating a move toward area array devices, which have the interconnections positioned under the device to increase the capacity of connections per chip. Area array packages include: ball grid array (BGA), chip scale packages (CSP), and flip chip. The increasing IO density, created by the growing number of transistors per IC chip and allocated by the use of area array chips, has forced PCB manufacturers to pack the transmission lines as tightly as possible on the PCB.

To satisfy the demand for bandwidth, generated at the board level, traditional copper tracks are required to carry greater amounts of data. Increasing either the density of tracks or the data rate, the amount of data transmitted per second, can enlarge the bandwidth capacity of copper. However, due to both component packaging and electromagnetic interference, it is simply not possible in many cases to include more tracks onto the PCB. Also, although manufacturers have sought to extend the bandwidth by transmitting at higher data rates, the potential solutions based on copper traces, such as new board substrates and sophisticated end-coding techniques, tend to be expensive [13]. With copper tracks beginning to operate at their maximum bandwidth capacity and IC packaging struggling to increase the number of electrical IOs, optical solutions are being identified as a requirement to enable chip manufacturers to commit to the extension of Moore's law well into the future [14].

Table 2.1 ***Recommended Solder Reflow Parameters:*** *the table shows recommended solder reflow parameters for tin-lead and lead-free solders [12].*

	Duration above minimum temperature	Peak Temperature
Eutectic tin-lead	60 – 150 seconds above 183 °C	225 – 240 °C
Lead-free	60 – 150 seconds above 217 °C	230 – 260 °C

Based on Moore's law [15] – the doubling of transistor numbers on ICs every eighteen months – the trend predicts that by 2010 Complimentary Metal Oxide Semiconductor (CMOS) based transistors will be fast enough for transceivers to operate at clock speeds of around 14 GHz, with data-transfer rates in the region of 20 Gbs [14]. Since copper interconnects on FR4 based PCBs become bandwidth limited beyond 10 GHz [16], primarily due to frequency dependant losses such as the skin effect in conductors and substrate dielectric losses [17, 18], low-cost optically enabled PCBs are required.

History shows that the barrier to implementing optical links, over established copper-based interconnects, is overcoming the technical challenges to achieve higher performance for lower cost. These technology issues are similar for both inter and intra-board USR optical interconnects and can currently be divided into two research areas: free space optics, and guided waves.

2.1 Free Space USR Optical Interconnects

The most basic, although by no means the simplest method of applying optical interconnects at the board level is to use lenses and collimators to expand a VCSEL beam, suitably, so that it can be sent through the air to a corresponding configuration, for detection by Photo Detectors (PD) [19-22]. So-called Free Space Optical Interconnects (FSOI) can provide an increased bandwidth over copper due to the combination of both high data rates and the ability to densely pack FSOIs on the circuit board (Figure 2.1). Diffractive optics can be added to enable the FSOIs to be routed to different detectors and benefit from being reconfigurable [23-25].

Complications to this basic principle arise due to the requirement to maintain a precise line-of-sight rule. If the VCSELs and PDs become misaligned or blocked for

any reason the signal is lost. Although research is ongoing into ways of tracking and actively maintaining the links as the transmitter and detector arrays move relative to one another [26, 27], the occurrence of catastrophic signal loses due to environmental issues can not be eliminated without hermetically sealing the entire backplane. However, the increased complexity and additional hermetic requirement greatly increases the cost, so a low-cost architecture is still required.

Greater control of the signal between the transmitter and receiver is beneficial due to the reduced cost compared to FSOIs, which is achieved by eliminating strict line-of-sight rules and using fewer elements. Guiding the signal between geometric boundaries, such as fibre or waveguides, increases the routing control. Consequently; there is an increased interest in developing guided wave USR optical interconnects.

2.2 Guided Wave USR Interconnects

In order to develop a low-cost architecture for integrating optical interconnects onto PCBs, guided wave based systems are being developed. Optical fibre and planar waveguides are two examples of guided wave interconnect. As a core component in telecommunication networks, optical fibre is the most established technology.

2.2.1 Guided Wave Alternatives

Optical fibre is a thin, transparent, flexible strand that consists of a core with a circular cross-section that is surrounded by cladding [28-33]. The cladding material has a slightly lower refractive index compared to the core. The fibre material and manufacturing processes are responsible for determining the characteristics of the signal transmission. Limiting the signal degradation caused by attenuation is of primary importance. Attenuation is the loss of optical power and for transmission along guided wave structures is created by three attenuation mechanisms: Rayleigh scattering, micro-bending, and absorption.

Rayleigh scattering accounts for approximately 90% of the total attenuation and is generated by the microscopic non-uniformity of the refractive index, scattering the light into many directions. The loss created by this phenomenon is a function of

wavelength; hence, the overall tendency is for attenuation to decrease as wavelength increases. Micro-bending creates attenuation due to microscopic imperfections in the fibre geometry. Absorption is a characteristic of the selected fibre material and accounts for signal loss due to absorption of the optical power. The combined attenuation affects can be displayed as a spectral attenuation curve and can be used to explain the wavelength bands selected in telecommunication networks (Figure 2.2).

Silica-glass based fibre achieves the lowest attenuation levels [34]. Dopants can be added to change the characteristics of the fibres for application specific requirements, including: the removal of the 'water peak' around 1385nm (Figure 2.2), created due to absorption by the hydroxyl ion (OH-), a residual impurity from the fibre fabrication process; the reduction of dispersion effects; and to enable optical amplification of the signal for the manufacture of fibre amplifiers. Plastic Optical Fibre (POF) has increased attenuation but can be both fabricated and manufactured at lower cost.

Light is transmitted down fibre via two inherently different principals, which has led to two fibre types: Multi-Mode Fibre (MMF) and Single Mode Fibre (SMF). The fundamental physics of light propagation down optical fibres are explored in detail in references [30-33].

2.2.2 Multimode Guided Waves

The physical difference between SMF and MMF is the size of the core diameter. MMF has a much larger core diameter, typically 62.5 μm or 50 μm. The light is retained in the core due to Total Internal Reflection (TIR) at the core-cladding interface [28]. TIR is a physical principle of light based on refraction, the bending of light as it travels between two media with different indices of refraction. The selection of refractive index determines the Numerical Aperture (NA) of the fibre, which is a measure of the angle at which light will undergo TIR and propagate along the fibre. Light paths that are incident with the boundary at greater angles are lost.

MMF allows many paths or modes to propagate. Due to modes taking different times to travel their path down the fibre, pulse broadening occurs [35]. This form of pulse broadening is known as modal dispersion and causes inter-symbol interference

resulting in unacceptable bit errors as link distance and data rate increase (Figure 2.3). Graded Index (GI) fibres can reduce modal dispersion by gradually changing the index of refraction through the core radius. This slows light travelling through the centre of the core allowing modes to simultaneously reach the other end. SMF eliminates modal dispersion, by reducing the core size to allow only one mode to propagate (Figure 2.3).

2.2.3 Single Mode Guided Waves

SMF has a reduced core diameter compared to MMF. The core is approximately 8μm in diameter and allows only one fundamental mode to propagate down the fibre (Figure 2.3) [30-33]. The electromagnetic wave propagates down SMF in both the core and the cladding, with the difference in the refractive index causing the light to propagate along a plane wave front instead of a spherical waveform. The total waist diameter of the beam, including the portion that travels inside the cladding is known as the Mode Field Diameter (MFD), which is approximately 9.3 μm for SMF.

In MMF, modal effects are the greatest contributor to dispersion. Although SMF removes modal effects, two other dispersion mechanisms become evident: Chromatic Dispersion (CD) and Polarisation Mode Dispersion (PMD) (Figure 2.3) [29, 36, 37]. CD is wavelength dependant and consists of two components: material dispersion and waveguide dispersion. Material dispersion is the result of wavelengths travelling within the fibre at different velocities. Signal distortion arises because each pulse contains a small range of wavelengths, with each part of the pulse arriving at the fibres end at different times. Waveguide dispersion is generated because part of the light travels in the cladding. Since the cladding has a lower refractive index than the core, the light in the cladding arrives quicker than the light in the core, leading to pulse broadening. PMD is the least significant source of dispersion and occurs because the birefringence of optical fibre allows two perpendicularly aligned polarisation states to propagate. PMD cannot be easily compensated for as the effects fluctuate over time, temperature, stress and other non-controllable external environmental factors.

As link lengths and data rates increase, to ensure the integrity of the signal, it is necessary to decrease the level of dispersion. CD can be reduced using narrow line width transmitters and PMD can be tackled by introducing a high birefringent strip down the fibre to eliminate one of the polarisation modes. However, the reduced dispersion technology comes at a price premium, so is applied only when necessary.

2.2.4 Cost Advantage of Multi-Mode Guided Waves

The decision as to which guided wave transmission mechanism to use is based on the application of the given interconnects. USR interconnects are required to be low-cost and are limited in distance to a few metres.

The cheapest guided wave transmission medium is MMF. Although manufacturing SMF incurs slightly higher costs due to the small core diameter, both SMF and MMF are manufactured from large rods of material, using a drawing process, and are also joined and handled using the same methods. The main cost advantage of MMF when compared to SMF is achieved because of the reduced component coupling costs.

The reduced light coupling tolerances of MMF, caused by the large core diameter and NA, allow components to be aligned and packages pigtailed using less expensive manufacturing techniques [38-40]. MMFs can often be passively aligned to components using mechanical marks, such as v-grooves, or self-alignment techniques, such as solder tensions. SMFs require precise alignment to components and often require active alignment techniques that move the fibre, with respect to the component, whilst monitoring the optical signal that is transmitted through the junction. The fibre can be secured in place once an optimum signal strength has been located. MMF also requires lower specification transmitters and, in general, lower specification means lower cost. MM VCSEL transmitter components can be sourced at a greatly reduced cost to DFB LD devices, the preferred SMF transmitters [41].

The main advantage in deploying SMF is the reduced dispersion levels. However, signal dispersion is a function of distance so is not a major factor in USR interconnects. MM guided waves are the optimum solution for USR interconnects.

2.3 1st Generation Guided Wave USR Optical Interconnects

The demand for a low-cost architecture to increase the bandwidth across inter-board interconnects is leading to the development of guided wave USR optical interconnects; to date, the most successful uptake of these board-level interconnects has been on high-speed backplanes inside CO telecommunication equipment. As identified by market consultants BPA [42], the implementation of USR optical interconnects over backplanes can be classified into three generations of technology.

The 1st generation consists of discrete optical fibre interconnects, which are a direct descendant of the VSR links that are currently being deployed between co-located CO equipment (section 1.1.3). Each fibre is individually routed at the back of the switch to form point-to-point optical links. MMF is used due to the cost advantage (section 2.2.4). Discrete MMF interconnects have been successfully deployed across VSR links and also over USR links that interconnect between backplanes. However, with a typical optical switch containing 2048 optical fibre interconnects, attempts to extend 1st generation technology to address links across the backplane have been thwarted by fibre management problems generated by the resulting increase in the density of fibre terminations [43]. This greater density creates a 'rat's nest' of fibres at the backplane and also requires significant resources to manually route the fibres. Reducing the cost from the assembly and manufacture of discrete MMF interconnects was a key influence in the development of 2nd generation technologies.

2.4 2nd Generation Guided Wave USR Optical Interconnects

To enable greater integration of the USR optical interconnects into the board and to reduce some of the problems associated with discrete MMF interconnects, various institutions and companies [44-48] are developing 2nd generation technologies that combine MMF into a rigid board, termed fibre-on-board (FOB) (Figure 2.4).

The essence of FOB technology is to embed standard production MMF into a PCB harness. Although FOB technology reduces the fibre management problem when compared to 1st generation discrete fibre interconnects, fibre handling and its associated costs are clearly still involved in the manufacturing process. Fibre

management problems occur because of the requirement to maintain the minimum bend radius of the fibre, typically a few centimetres, which, if reduced, would result in unacceptable attenuation due to the conditions for TIR being negated. Ensuring the minimum bend radius is not breached is an important consideration when routing the fibres around the board and has two important consequences. Firstly, it prevents more than two fibres from crossing on the same plane and secondly, it inhibits the formation of tight bends in the fibre, which are necessary in order to connect with SMT components. To couple light to and from non-connectorised, SMT components, which are assembled onto the board surface, it is therefore necessary to use long sweeping bends and polished fibre terminations that are both costly to manufacture and also hard to precisely locate (Figure 2.5) [49]. Pig-tailed SMT devices can be coupled to the embedded fibres more easily, as the fibre end of the pig-tail can be joined to the fibre that exits the edge of the board. The fibres can be joined by either connectors or by splicing.

Connectors form temporary connections between fibres using male and female ferrules to physically mate the two ends together [35, 50]. Although connectors can minimise core misalignment, air gaps create Fresnel loses and back reflections, which can damage other networking equipment. Angled cleaves can alleviate the back reflections but connectors are easily damaged and have a finite insertion life. Splicing provides the connection method with the lowest loss, joining two bare fibres by stripping the protective layers to the cladding, cleaving both ends, aligning the cores, and fusing the glass together by sparking an electrical arc across the junction [50, 51].

Added to the complications of fibre management is the requirement to protect the fibres where they exit the harness and become vulnerable to damage. Removing the damaged section and splicing new fibre into the gap can repair damaged fibres. However, the splicing process requires a length of fibre to be accessible to enable the fibres to be loaded into the fusion-splicing machine. Fibres that are broken or damaged within close proximity to the edge of the PCB harness are therefore irreparable and result in the scrapping of the entire board.

Although FOB technologies offer benefits over discrete MMF interconnects, they fail to provide an adequate architecture for providing both inter-board and intra-board USR interconnects. Low-cost 3rd generation USR optical interconnects are required.

2.5 3rd Generation Guided Wave USR Optical Interconnects

Due to the associated costs and problems both with fibre management and component coupling, a significant cost advantage can be realised by eliminating fibres from the heart of the manufacturing process. This is the main advantage in 3rd generation technologies, which look to replace fibres with planar optical waveguides.

Planar waveguides have a similar construction to optical fibre, consisting of a core and cladding structure that retains the majority of the light within the boundaries of the core due to TIR at the core-cladding interface. Due to the similar construction, waveguides exhibit the same light guiding principals as fibres and are also affected by the same attenuation and dispersion mechanisms. Waveguides and fibre differ mainly in construction. Fibre has a circular cross-section and is manufactured in long free-form lengths; contrastingly, waveguides are manufactured in planar area layers.

Waveguides allow the optical links to be fully integrated into the PCB, with easier coupling routes for SMT devices, which allows the solution to address inter-board as well as intra-board interconnects. It is anticipated that most 3rd generation technologies will sandwich an optical layer, containing the waveguide, into a standard FR4-stack. The board will remain FR4 based since not all interconnects are required to be high speed so some copper tracks will be retained thus creating a hybrid Opto-Electrical Circuit Board (OECB) containing both electrical and optical interconnects. The importance placed on low-cost means OECB fabrication is required to employ manufacturing processes that closely align with current PCB methods.

2.5.1 OECB Based USR Optical Interconnects

OECB based architectures, fabricated using FR4-PCB technology for the electrical and mechanical support of the ICs and planar waveguides to route optical signals between chips, are increasingly emerging on technology roadmaps (Figure 1.2). The

USR optical links will be operated using VCSEL and PD pairs due to inherent advantages.

Although discussed in more detail in Chapter 3, OECB platforms consist of VCSEL devices, which are assembled onto the outer surface of the OECB using current SMT processes, transmitting light into the planar waveguides in the OECB structure. The waveguides can either be embedded under the surface of the OECB or over-laid on the outside surfaces. The waveguides route the light signal around the board where at the opposite end of the Light Path (LP) the signal is detected by a photo-detector. This configuration satisfies the requirements for intra-board aggregation.

The addition of optical edge connectors enables OECB based USR interconnects to extend between OECBs and also over extended distances via connection to MMF (Figure 2.6). This enables inter-board applications and positions OECB architectures as the technology most capable of providing both current and future USR interconnection requirements.

2.6 Summary

A literature review of USR optical interconnects is given. Methods for optically enabling PCBs can be divided into two research areas: FSOIs and guided waves. Whilst reconfigurable FSOIs provide a method for creating board level optical interconnects, they are complicated by precise line-of-sight alignment conditions; hence, benefits exist in developing guided wave technologies, which have been classified into three generations. First and second generation technologies are based upon optical fibres and are both capable of providing a suitable platform for inter-board applications. However, to allow component assembly, an integral requirement for intra-board applications, 3rd generation OECBs containing embedded waveguides are desirable.

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Figure 2.1 ***FSOI Based Backplanes:*** *VCSELs and PDs on separate daughter cards communicate across an optically enabled high-speed backplane via free space.*

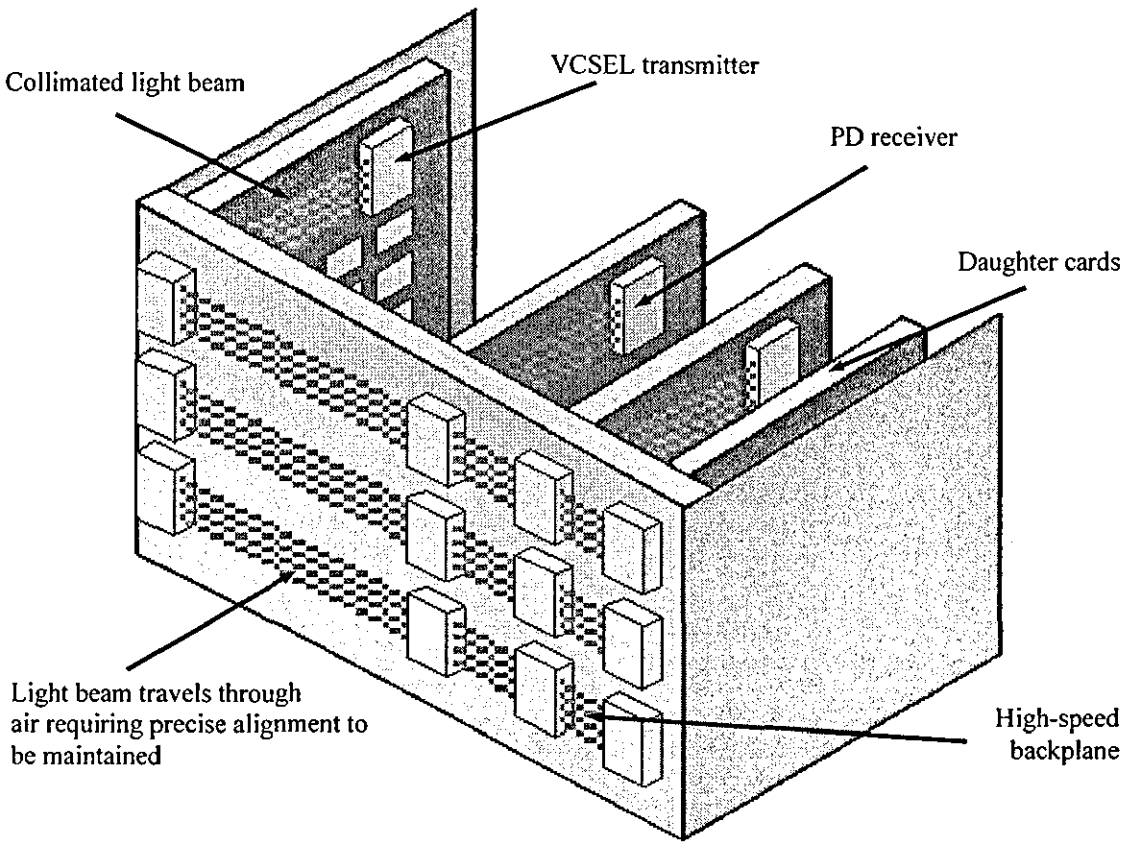


Figure 2.2 ***Spectral Attenuation Curve:*** *attenuation plotted against wavelength shows the transmission loss characteristics of standard silica SMF. Telecomm. network wavelengths have been separated into transmission bands [28, 29].*

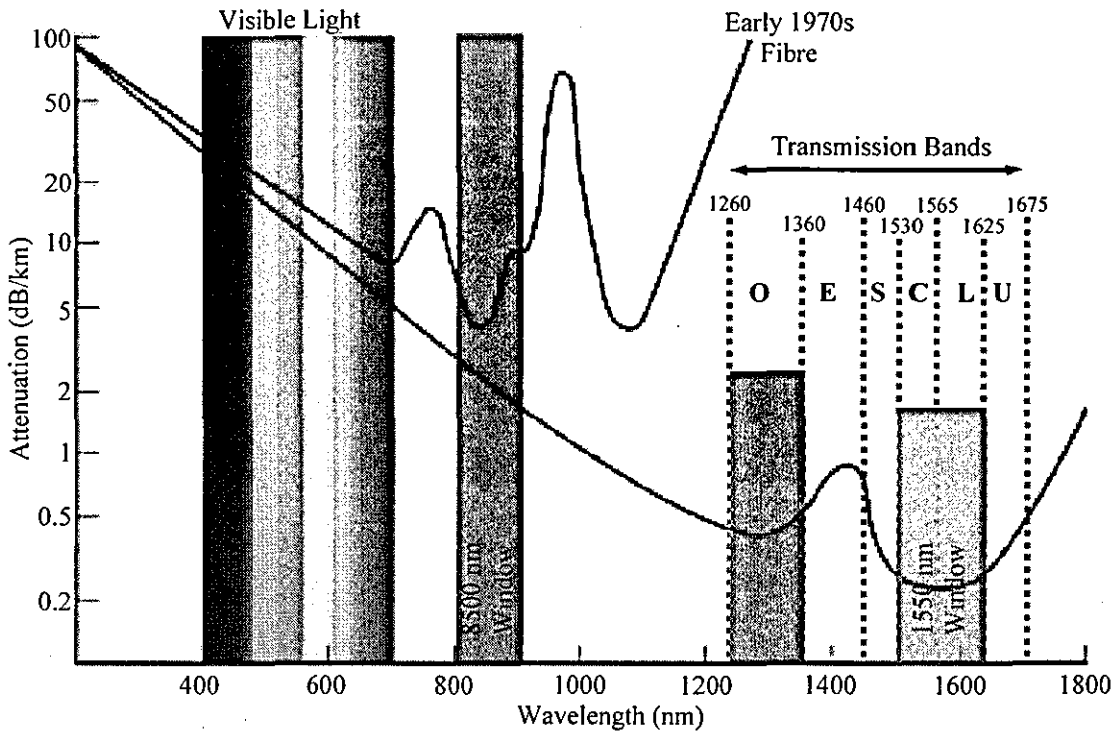


Figure 2.3 ***Optical Fibre Dispersion Mechanisms:*** *dispersion creates pulse broadening (a), which at high data rates leads to bit errors (b), and is generated by modal dispersion (c), CD (d), and PMD (e). Standard fibre geometry is detailed (f).*

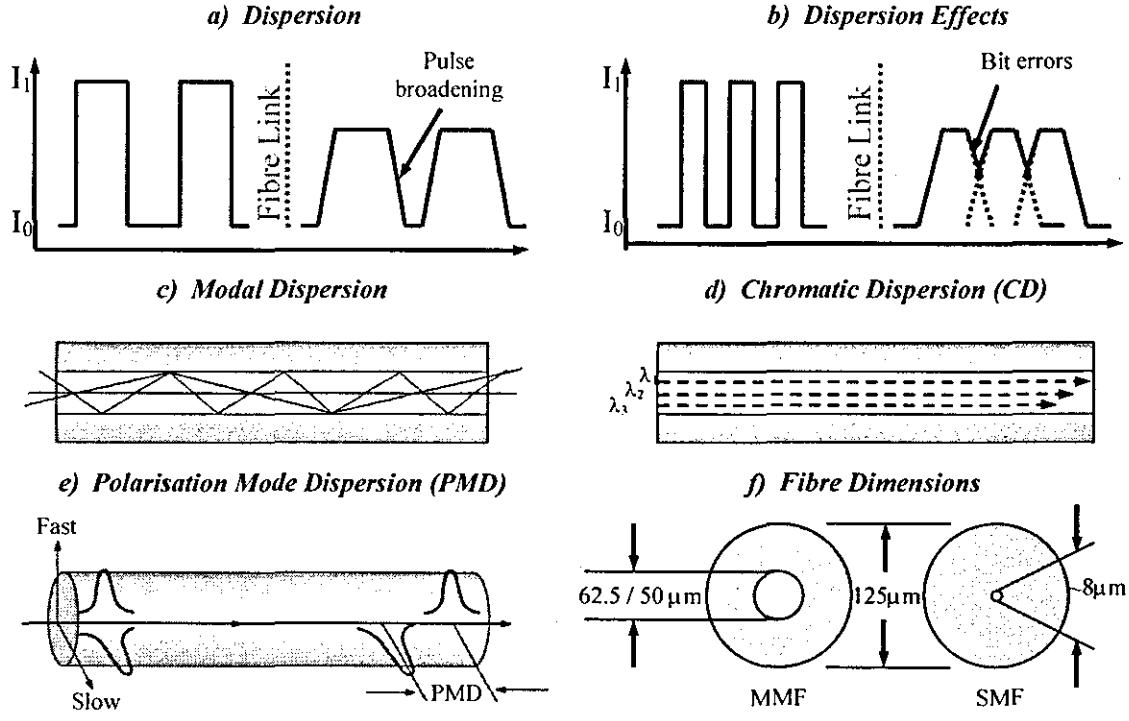


Figure 2.4 ***FOB USR Optical Interconnection Technology:*** *inter-board fibre management problems are reduced by combining the fibre into a flexible harness or PCB. Inset, an example of Molex's FlexPlane ™ [44]*

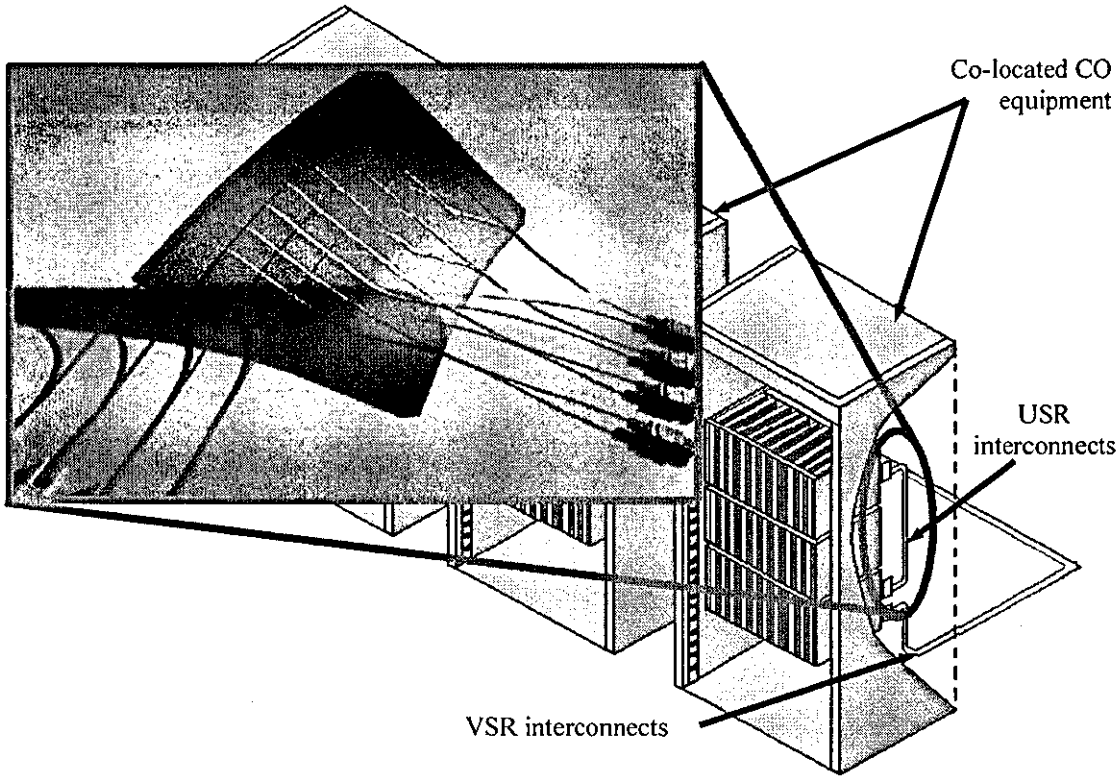


Figure 2.5 ***FOB Component Coupling Issues:*** *Maintaining the minimum bend radius inhibits the fibre from being bent upwards. The assembly also requires precise cleave and polish locations. Figure adapted from presentation slides [49].*

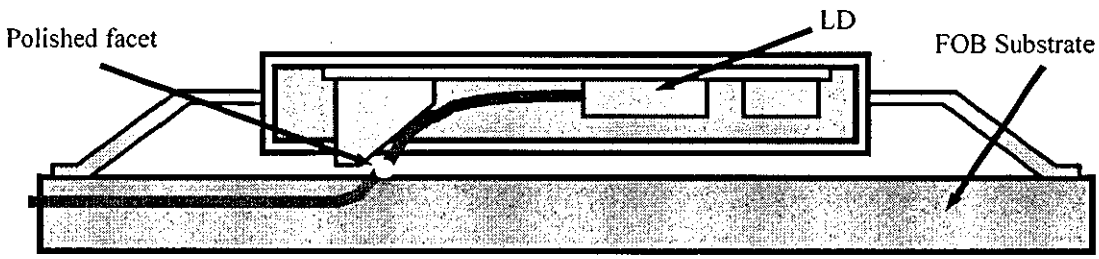
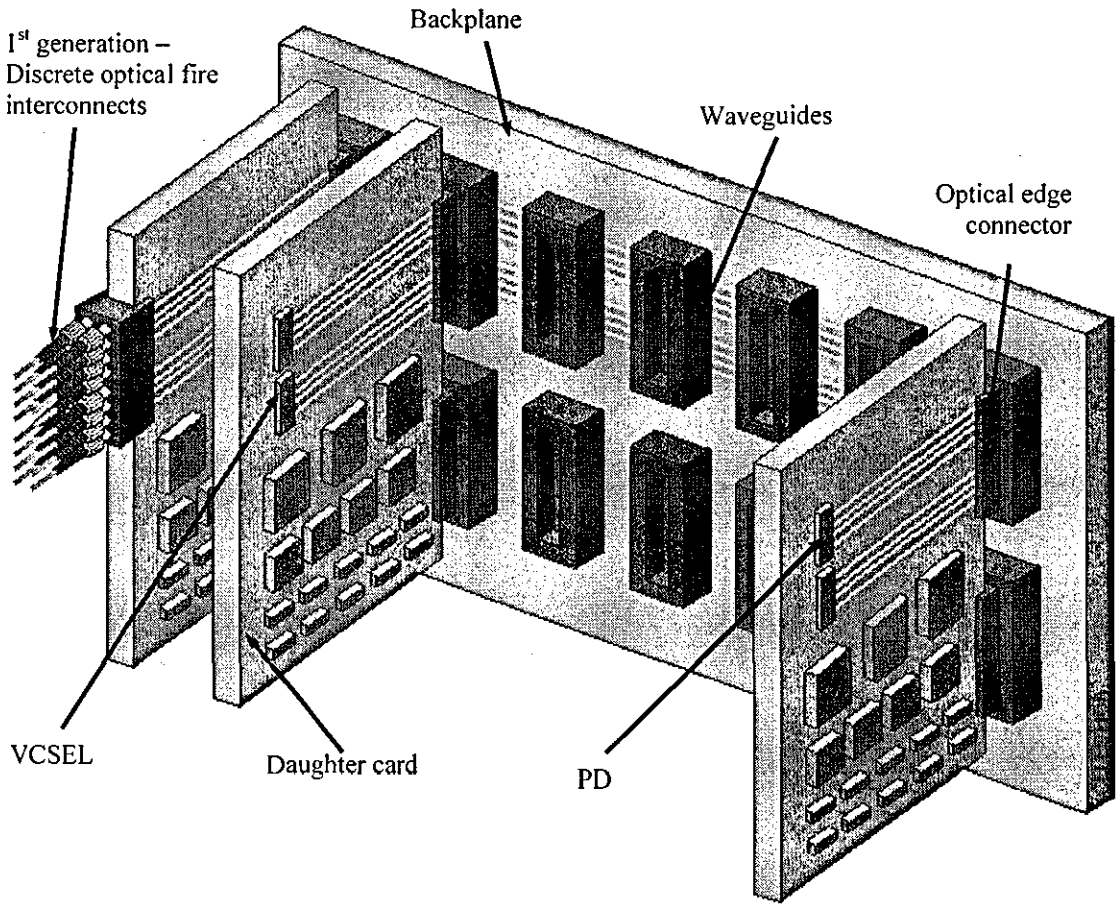


Figure 2.6 ***OECB Based Optical Backplane Architecture:*** *SMT assembled VCSELs emit light into embedded waveguides, which route onto the backplane to be distributed onto other daughter cards or in to fibre for aggregation over larger areas.*



Chapter 3

Third Generation OECB Technologies

3.0 OECB Technology

Optically enabled circuit boards with integrated optical layers are being developed. The OECB substrates combine optical layers containing optical waveguides into the PCB fabrication process. Active devices, such as VCSELs, are assembled onto the OECB substrate using SMT techniques and are optically coupled with the waveguides to produce board-level high-speed USR interconnects.

3.1 OECB Optical Layers

OECBs include an optical layer that contains defined waveguide paths. The optical layer can be overlaid on the outside surface of the substrate or embedded within the FR-4 stack. To ensure the thermal stability of the substrate and to avoid warping, a degree of symmetry is required in the arrangement of the optical layers through the substrate. If the optical layers are laminated with the FR-4, the materials used need to be compatible with existing PCB laminating processes, which require a temperature of 170°C at 1470kPa pressure [1]. The waveguide material must also match the mechanical and thermal properties of FR-4. Also, electrical properties such as dielectric strength and isolation resistance of the waveguide material must be considered. There are currently two main candidate materials being investigated to form the optical waveguide layers: glass, and polymer.

Attenuation determines the maximum waveguide length as well as the signal-noise ration, which affects the bit error rate, and is the predominant factor in the selection of the optical layer material. BPA's backplane market report [2] suggested that to achieve the necessary attenuation, less than 5dB/cm, glass materials would have to be adopted due to their much reduced intrinsic attenuation, a result of material absorption, when compared to polymers. However, against this prediction, glass manufacturing issues have prevented the production of high quality waveguides with low attenuation levels, whilst developments in the manufacture of polymer based layers have produced lower attenuation figures (< 0.03 dB/cm [3]).

3.1.1 Glass Waveguide Layers

Glass-based optical layers are integrated into PCBs by bonding thin glass sheets into a standard FR4 stack. Structures are formed in the glass sheets by etching channels, laser ablating channels, or by ion exchange [4-6]. Filling the channels with a glass material with an appropriate refractive index to enable light to propagate through TIR creates waveguides. Plating the etched or ablated channels with a thin metal coating can also form waveguides. The channels can again be filled with an optically transmissive glass material. A second metal coating completely encases the core. Light propagates down the surrounded core by reflecting off the mirrored sidewalls. Although glass has lower absorption properties when compared to polymers and also shows less degradation under high-temperature and high pressure conditions [7], the achieved attenuation is large. The high attenuation is predominately due to current manufacturing processes not being capable of generating smooth sidewalls. Sidewalls with high surface roughness scatter incident light, which leads to high attenuation.

PPC electronic, in conjunction with Isola and Ghent University, have developed an optical circuit board, termed Optoboard technology [8], which is based on thin glass sheets laminated into FR-4.

3.1.2 Polymer Waveguide Layers

Polymer waveguide layers are becoming the preferred technology for integrating optical waveguides into PCBs due to the reduced transmission attenuation compared to glass-based layers. There are many candidate polymer materials that can be patterned with waveguide circuitry, materials include: acrylates, halogenated acrylates, cyclobutenes, polyimides, and polysiloxane [9]. Table 3.1 shows a partial list of polymer waveguide technology manufacturers, including candidate polymers and manufacturing techniques. A variety of polymer waveguide manufacturing processes exist, including: laser ablation [10, 11], Reactive Ion Etching (RIE) [12], moulding [1, 13-15], and lithographic processes [3, 16-18]. Moulding processes, such as hot embossing and injection moulding, along with lithographic techniques are attracting the most research due to their lower manufacturing costs.

Table 3.1 ***Candidate Polymer Waveguide Technologies:*** *a partial list of candidate technologies for polymer waveguide based, optical PCBs. [9, 12]*

Manufacturer	Technology	Polymer	Manufacturing Technique	Attenuation @ 850nm
Corning (Allied Signal)		Halogenated Acrylate Acrylate	Lithographic, RIE, Laser	0.1 dB/cm
Dow Chemical		Benzocyclobutene (BCB)	RIE	0.8 dB/cm
DuPont (OXL) [16]	PolyGuide™ [19] (GuideLink ™)	Acrylate	Lithographic (Photo-fixing)	<0.08dB/cm
BF Goodrich	NIST – TOPCat	Polynorbornene	Moulding	0.24 dB/cm
Nippon Paint		Polysitare Photosensitive	Lithography, bleaching	0.1 dB/cm
NTT	OptoBump	Halogenated Acrylate Polysiloxane	RIE, Embossing	0.02 dB/cm
Epigem [20]		Acrylate	UV embossing	
Siemens / IZM	EOCB, OptoFoil	Polycarbonate	Hot embossing	<0.3 dB/cm
Terahertz [3]	Truemode	Fluorinated Acrylate	Lithographic	0.03 dB/cm

The Electrical-Optical Circuit Board (EOCB), developed at the Fraunhofer Institut Zuverlässigkeit und Mikrointegration (IZM) in conjunction with Siemens C-Labs, laminates a polymer-based optical layer into a standard PCB configuration [13]. The optical layer is fabricated separately by a hot embossing process and has been termed OptoFoil. The hot embossing process uses a positive mould of the waveguide cores to hot emboss a polycarbonate foil (Figure 3.1). The mould is removed and the embossed channels filled with a core material (Topas) with a higher refractive index when compared to the under cladding foil. Over cladding is created by coating the foil with a final layer of polymer. The OptoFoil is laminated to FR4 using standard PCB processes (60 minutes at 150°C and 1.47 MPa [6]).

TOPCat, the planar polymer waveguide developed as part of a NIST-sponsored ATP project, is manufactured using a process similar to injection moulding [9, 14]. Opposite to the hot embossing process, TOPCat is a "core first" microreplication. A polynorborene polymer is coated onto an embossing tool with a negative waveguide core pattern, with the polymer filling the channels in the embossing tool. The waveguide core is lifted from the embossing tool and overcladding applied. The optical layer is laminated into PCB substrates. The moulding processes employed in the manufacture of the OptoFoil and TOPCat polymer films both create optical layers

that can be laminated into FR4 PCBs; however, neither is directly compatible with current PCB fabrication methods.

Photo-lithographic processes are advantageous compared to moulding techniques as the processes are compatible with current PCB fabrication methods. Lithographic processes are widely used to develop photo-resists during the selective etching or plating of copper layers. The Truemode polymer waveguides manufactured by Terahertz [3] can be patterned using lithographic techniques and are fabricated in three steps (Figure 3.1). A thin undercladding layer is coated onto the substrate material, including FR4, using a variety of current PCB fabrication methods, including: spin coating, curtain coating, and screen-printing. The layer is cured via UV exposure. A second polymer layer is coated to the first with a thickness corresponding to the thickness of the desired waveguide cores. The core layer is selectively cured using lithographic techniques such as direct laser writing or masking. The remaining material is removed and over cladding coated. If direct laser writing is fast enough, it is beneficial over masking due to its ability to be reconfigured cheaply.

Photo-lithographic, polymer waveguide processing techniques are advantageous due to their close synergy with current PCB fabrication methods, which allows low-cost manufacture: an important specification for OECBs.

3.2 VCSEL Devices

VCSELs are the preferred transmission equipment for board level USR optical interconnects. The evolution of the telecommunications network infrastructure (Chapter 1) has led to 850nm VCSELs dominating the short link markets primarily due to their low-cost. The main factor that drives the cost out of VCSEL manufacture is the ability to test, characterise, and re-work each device at the wafer level, which results in much higher yields [21]. Wafer level re-work is enabled due to a fundamental difference between VCSELs and higher specification DFB LDs, which produce the optical power in the plane of the wafer and cannot be accessed until the wafer is diced into individual die. VCSELs generate the light in a vertical plane, emitting the beam from the surface of the wafer.

VCSEL construction has seen significant development [22-24] since their inception from the first design with the active area sandwiched between two Distributed Bragg Reflector (DBR) mirror stacks, fabricated predominately on Gallium Arsenide (GaAs) wafers (Figure 3.2). The light beam is created when electrical current is applied across the active layer, via intracavity contacts, generating photons that are then reflected by the DBR mirrors before being emitted from a circular aperture, about 14μm in diameter [25], on the surface of the wafer. Before the wafer is diced, a polyimide coating is applied between the VCSEL structures to protect the sides from oxidisation.

A single VCSEL die is typically 250μm square [25-27]. Wafers contain tens of thousands of devices and can be diced into either single devices or arrays with the individual VCSELs pitched at 250μm. Each VCSEL can be directly modulated so only requires a positive and negative electrical contact. The anode and cathode electrical contacts can be created on either side of the VCSEL to enable the die to be wire-bonded, die-bonded, or flipchip-bonded to the substrate. A passivation layer is applied to the wafer exposing only the metal contacts and aperture, which can be formed with the optical beam emitting from the top or bottom side of the chip when assembled. The electrical contacts, termed bond pads, provide an interface between the wafer and electrical interconnection. To achieve the electrical interface, an Under Bump Metalisation (UBM), consisting of layers of material, is deposited on to the contacts. The first layer is typically Cr, TiW or Ti and provides the adhesion to the wafer passivation. A final layer of typically Au or Cu with an Au protective layer provides the final bond pad surface. Presently, the bare VCSEL dies are assembled into packages. Chip Scale Package (CSP) interconnection technologies are employed to provide the electrical connections between the package and the VCSEL bond pads.

3.2.1 VCSEL Device Assembly

The bare VCSEL die require specific CSP assembly technology to ensure that the electrical connections and the optical output are both achieved without degrading the performance of the device. It is desirable to employ current CSP processes to achieve the electrical connections in order to drive low-cost assembly.

Conventional CSP electrical interconnects are formed by wire bonding. Wire bonding creates the electrical interconnects between the bond pads on the chip and substrate by creating thin wire loops (Figure 3.3). Wire bonds are created using a combination of heat, pressure, and / or ultrasonic-energy to form a solid phase weld between the wire and pad surface [28]. After the first wire bond has been performed, usually on the chip, the bonding head moves to the second bond pad location whilst feeding the wire to create the loop. The wire is bonded to the substrate bond pad and broken off. Three different techniques and bond properties are available: ball, wedge, and ribbon bonding. Wire bonding is not suitable for area array devices with a high number of interconnections. As an alternative, Direct Chip Attach (DCA) technologies offer a viable solution. Flip Chip Attach (FCA) methods are the most advanced form of chip level interconnects.

A well established FCA process is based on tin-lead solder. Tin-lead solder bumps are formed on the UBM using various technologies including: evaporated solder bump formation, where solder is evaporated onto the UBM and balled by reflowing the solder; electroplated solder bump formation, where the wafer is patterned with a photo resist and solder plated onto the UBM; and printed solder bump formation, where solder paste is printed through a stencil and balled by reflowing the paste [29-31]. Whilst balling wafers with tin-lead solder offers high yield and reliable connections, soldering requires complex processes and requires fluxes to remove oxides during assembly. Fluxes are hazardous in the assembly of VCSEL devices as they can coat the optics as they evaporate and condense during reflow. Due to wetting issues created by flux-less soldering, which are compounded when moving to Pb free alloys, VCSELs are often assembled using non-solder based FCA techniques.

Non-solder based, flux-less FCA techniques include Anisotropic Conducting Films (ACF) and Stud Bump Bonding (SBB). ACFs are designed to be conductive in the z-direction, between the chip and the substrate, and insulating in the horizontal direction to ensure short circuits do not form [32]. The ACF is placed on the substrate. The chip, which usually has bumps created proud of the UBM using an electroless nickel process, is aligned and placed. Pressure is applied to mould the film around the chip's profile. The ACF is cured, acting as an underfill. ACFs are not compatible with

bottom emitting VCSELs since the light cannot transmit through the conducting particles (Figure 3.3).

SBB forms gold solder bumps on the UBM [30, 33]. SBB uses wire bonders to create ball bonds on the VCSEL pads using Au wire. The wire is broken off close to the stud. The bonded stud bump is flattened (coined) to establish a uniform height. The SBB VCSEL die is flipped over and assembled to bond pads on the substrate either in conjunction with ACF or Isotropic Conducting Adhesives (ICA) or by directly bonding to gold plated bond pads on the substrate using thermocompression or thermosonic bonding processes [34]. Thermosonic bonding is a combination of ultrasonic and thermocompression welding and is preferred as it reduces the required interfacial temperature (Figure 3.3).

To improve the product life, FCA methods require underfill materials to: 1, protect the underside of the device from the environment; 2, increase the fatigue life of the joint by locking the substrate and chip together to stop stresses generated by movement between the materials as Coefficent of Thermal Expansion (CTE) mismatches are imposed; 3, reduce the junction temperature of the IC by acting as a thermal dissipater [35]. The underfill can be applied after the device has been bonded with capillary action pulling the underfill under the device. Alternatively, no-flow underfills can be applied to the bond site prior to the chip being placed. The chip is placed on top of the underfill. Pressure forces the stud bumps into contact with the bond pads. Most underfills contain curing agents that enable them to be spot cured using Ultra Violet (UV) light. Underfill that may be shadowed by the chip is cured by a secondary thermal bake.

In order to both cost-effectively integrate VCSELs onto PCB based telecommunications equipment and also to hermetically protect the device from the environment, it is currently necessary to first assemble the VCSELs into a package.

3.2.2 VCSEL Device Packaging

The bare VCSEL die require packaging methods that enable both the electrical connection of the intra-cavity contacts and also the optical coupling of the output into

a usable form. Currently; VCSEL device packaging for 1st and 2nd generation USR optical interconnections forms two identifiable package types [36, 37]. Both types of package route the electrical connections to the edge of the package to allow assembly to a standard PCB using either Through Hole Technology (THT) pins or Ball Grid Array (BGA) pads. The packages also couple the optical output of the VCSEL to the edge of the board. The signal is carried off the package either directly into an attached fibre pig-tail or through a fibre connector interface. Finally, the VCSEL packages provide a hermetic seal to isolate the laser die from environmental conditions, which can degrade the packages performance, for example, due to moisture condensing on the optics, or foreign bodies obstructing the light path. The two forms of package are TO-cans and Small Form-factor Pluggable (SFP) packages.

TO-can packages originate from a basic packaging trend [38]. A single top-side emitting VCSEL is die bonded onto a substrate. The substrate connects electrical pads on the top surface of the substrate to THT pins on the backside. The electrical pads are positioned to either enable the VCSEL to be wirebonded or flipchip bonded to the substrate. The substrate is housed in a package that enables a lens to be passively positioned in relation to the VCSEL die. A lid is attached to the package to hermetically seal the VCSEL device for environmental isolation. The lid generally contains a transparent section that allows a fibre pig-tail to be attached to the package. The VCSEL beam is coupled into the fibre via the lens. Some devices include a monitoring PD that enables a portion of the VCSEL beam to be monitored to ensure constant performance measures are met. Due to the temperature sensitive nature of some of the materials used, the TO-cans are attached to the PCB using standard selective soldering techniques such as: hand-soldering, hot bar soldering, and laser soldering [39].

SFP packages assemble arrayed VCSEL die into a BGA device [36]. The VCSEL die is assembled onto an internal substrate, which routes the electrical connections to BGA pads on the underside of the package. Internal waveguides or optics are used to couple the optical output of the VCSEL to an optical connector. The optical fibre is detached from the package to enable the package to be assembled using standard SMT high-volume reflow techniques.

TO-cans and SFP packages have proved successful in implementing 1st and 2nd generation USR optical interconnects. However, 3rd generation OECBs represent a significant change in the packaging of VCSEL devices, allowing the optical output from the VCSEL to be directly coupled with the waveguide without the need for the intermediate fibre (Figure 3.4). It is anticipated that moving towards the direct assembly of VCSEL die onto the OECB will decrease the cost of VCSEL packaging.

3.2.3 VCSEL Device Assembly to OECBs

3rd generation OECBs are required to enable intra-board USR interconnects (Chapter 2). A vital specification of OECBs is low-cost component assembly. VCSELs are therefore required to be assembled and optically coupled to OECBs with reduced intermediate packaging when compared to the packaging commonly used in 1st and 2nd generation USR optical interconnects. The simplest packaging method assembles the VCSEL die directly to the OECB. Hermetic requirements are met by encasing the sensitive areas of the VCSEL die with optical adhesive or underfill. The material is optically clear so the transmission path can be filled, which ensures foreign bodies can not disrupt the signal. Directly assembling the VCSELs to the OECBs may not be practical when the larger function of the board is considered.

As identified in Chapter 2, OECBs are hybrid PCB substrates containing a mix of electrical components as well as the high speed VCSEL interconnects. Problems arise when integrating DCA technologies onto the same substrates as larger SMT components due to the vast difference in feature sizes. It may therefore be necessary to include an interposer to disperse the range of feature sizes. The VCSEL die are assembled onto the interposer using CSP methods. The interposer is assembled to the OECB using SMT processes such as BGA solder balls. Optical adhesive / underfill is dispensed around the interposer and VSCEL to stop moisture, foreign bodies, and other environmental conditions from affecting the performance of the assembly.

The various architectures available for the assembly of the VCSEL devices provide the electrical interconnection through developed CSP and SMT methods. Although the architectures require the development of a new optical material for encasing the assemblies; currently, the major OECB technology challenge remaining, is the

coupling between the waveguides and SMT mounted VCSELs. The principal board fabrication issue is the 90° out of plane coupling, which enables light incident normal to the board surface to be coupled and transmitted along the waveguide. Subsequent research into assembly configurations, manufacturing tolerances, and hermetic requirements, will also be required before OECB systems can be commercially exploited.

3.3 VCSEL to Waveguide Optical Coupling Challenge

OECB architectures assemble VCSEL devices onto PCBs with integrated polymer waveguide layers. Bare VCSEL devices, suitable for OECB applications, are already available from a wide number of suppliers and polymer waveguide layers are gradually becoming commercially available. Currently; the remaining OECB issue under investigation is the 90° out-of-plane interconnection between SMT components and embedded waveguides. Research is proceeding into the possibility of creating pockets in the optical layers and sinking edge-emitting components into them. Thus, the edge emitting devices emit directly into the waveguide facet, which negates the requirement for the 90° change in direction. However, methods that couple signals to the waveguides without altering the direction of the light are limited in their application to other components, including low-cost VCSELs, and therefore do not provide the overriding advantage of deploying 3rd generation interconnects: the low-cost assembly of components. It is therefore essential to develop a low-cost architecture to change the direction of the light from being parallel with the board to projecting 90° out of plane to the top surface, thereby enabling compatibility with SMT devices and fibre ferrules.

Micro-mirrors, gratings, holographic elements, Micro Electro-Mechanical Systems (MEMS) based pop-up lenses, and photon band gap structures have all been proposed as methods for solving the out-of-plane coupling problem. The simplest approach is identified in US patent US2002/039475 and places a discrete bulk-optic prism or mirror in the waveguide end, which reduces the accuracy and complexity required in the manufacturing process. However, the manufacturing methods require additional components and process steps, which are not compatible with current PCB fabrication processes. Although the more advanced approaches offer additional functionality

such as wavelength selection and beam splitting, the most desirable approach is to form mirrors. Based on current literature and a detailed patent search, there are two distinguishable research strands for achieving the out-of-plane optical coupling between VCSELs and planar waveguides: assembled mirrors and integrated mirrors.

3.3.1 Patent Searching

Details of methods and architectures that are currently being investigated to achieve the 90° out-of-plane interconnection can be found by searching literature and by searching patent databases. Current literature contains sparse details of methods, since due to commercial interest, most institutions seek protection of their method by applying for a patent before releasing details of the research publicly [40, 41]. Several databases of patent documents exist [40-42]. One of the most comprehensive databases is Esp@cenet, which is provided by the European Patent Office (EPO). Esp@cenet can be searched using key words and also using International Patent Classification (IPC) codes and truncations thereof.

A comprehensive key word and IPC search of the Esp@cenet database identified numerous methods for achieving the 90° out-of-plane interconnection between planar waveguides and optical components. A detailed summary of the prior art can be found in Appendix A, with the key characteristics identified in sections 3.3.2 and 3.3.3.

3.3.2 Assembled Mirrors

Examples of assembled mirror techniques can be found in Appendix A, patents: 2, 3, 5, 8, 23, 27 and 29. Assembled techniques form the 90° optical interconnection by first creating a trench in the OECB to expose the vertical facet of the waveguides. An optical sub-assembly based on a BGA interposer is then placed onto the OECB with a carrier inserted into the trench. Light is then coupled to and from the waveguides either by direct alignment of a VCSEL or by using a mirror to direct the light upward to the surface, using either a free space or guided wave approach. Assembled techniques provide a simple process for coupling with the waveguides and have relatively few technological issues to resolve. However, the optical coupling relies on

manufacturing tolerances that are currently unable to provide sufficient repeatability. This is due to the reliance on the tension in the solder joints to self align the components to the waveguides: assuming that the bond pads are correctly positioned in the outset. Furthermore, the depth to which the carrier is inserted is also a critical alignment factor that cannot be guaranteed since the reference plane is FR4, which demonstrates large expansion in height due to a poor CTE value.

Integrated mirror techniques combine the 90° deflecting mirrors on the ends of the waveguides, allowing active devices to be flip-chip bonded directly on top of the OECB. This technology not only removes the need for additional assemblies and their associated part costs and manufacturing processes, but also enables the OECB to drive towards low-cost volume manufacture through SMT assembly. It is this move toward traditional EMS competencies, coupled with the perceived benefits in the re-work and test areas, which makes integrated mirrors the solution that is the most likely to break the significant USR market barriers of cost and performance.

3.3.3 Integrated Mirrors

Several of the patents found provide details of integrated mirror solutions that allow the direct coupling of components into the waveguides. For example, with reference to appendix A, patents: 1, 6-7, 12-15, 19-21, 24, 27-32; the majority of the patents found achieve the out-of-plane coupling by forming an integrated mirror structure that reflects the light from the second surface (Figure 3.5). Integrated mirrors that reflect light form the second surface remove material to form two surfaces; a vertical edge on the waveguides end and a second surface, which is opposite the waveguide end and openly slanted to form a 45° mirror. Light travels out of the waveguide and across the removed section to reflect upwards from the slanted surface. Although the gap can be filled to remove the signal degradation problems arising from the beam travelling through free-space, the light is not guided and so starts to disperse as soon as it leaves the waveguide. Index matching the filler material with the waveguide core can reduce Frenel losses although dispersion effects can not be removed; however, the dispersion can be reduced by limiting the distance the beam travels after exiting the waveguide.

A few of the patents disclose integrated mirrors that reflect the light out-of-plane using the first surface, which reduces the distance the beam travels unguided (Figure 3.5). First surface integrated mirror techniques form a slanted mirror surface, directly on the end of the waveguide, with prototype examples being published work from Intel [43] and Optical Cross-Connect (OXC) [16]. The two demonstrators are similar and are manufactured based on a standard core board containing electrical contacts for the components to which a section containing the waveguides is laminated (Figure 3.6). The waveguide section is pre-fabricated with 45° metalised IO mirrors on the ends. The section is then aligned on the core board using fiducial marks to ensure the precise position of the mirrors to the VCSEL pads and bonded using an UV curable epoxy. To enable SMT assembled devices to stand clear of the waveguide section it is necessary to sink the layer into a trench formed in the original board. This sits the top surface of the waveguide insert within a tolerance of the top surface of the core substrate. Using this approach, Intel have reported that when coupling VCSELs and PDs to the waveguides a misalignment in excess of ± 10μm still yielded 80% efficiency from the maximum coupling [43]. This tolerance range allows passive alignment, crucial in achieving the low cost manufacturing required for the systems.

With no set standards defining USR optical interconnect performance; the important characteristic of the link is to maintain the signal integrity over the distances involved; thereby ensuring that all the bits sent are correctly received. Although bit errors are generated by many factors, large link attenuation is a key contributor. Intel's demonstrator reported 1Gbts error free transmission over link distances of approximately 20cm with a loss budget of between 7-12 dB [43]. Of this loss budget the IO coupling between waveguide and component constituted signal attenuation of between 1.5 - 3dB. Despite demonstrating significant performance capability, the separate alignment and bonding steps required to attach the waveguide layer to the board contributes to additional tooling and process costs since the assembly methods are not aligned to that of current PCB fabrication. It is therefore necessary to further integrate the manufacture of the waveguides and IO mirrors into the substrate.

3.4 Market Gap

Current literature combined with the patent search has identified two possible routes for optically coupling SMT assembled VCSELs to waveguides in an OECB. Integrated mirrors improve on assembled mirrors by removing component parts and associated costs and tolerances. Despite significant research interest, fully integrated mirrors are still required. To that end, the research in this thesis contains details of a novel manufacturing approach, utilising current PCB fabrication techniques, to manufacture an OECB technology demonstrator with integrated mirrors for coupling waveguides to optical devices.

3.5 Summary

OECBs with integrated optical layers are being developed. Two optical layer materials exist: glass and polymer. Polymer layers are currently preferable because the manufacturing processes have achieved low attenuation levels and are also compatible with current PCB fabrication methods making them low-cost. VCSEL devices are assembled to the OECB. The electrical interconnects can be formed using current CSP techniques. Low-cost architectures are presently required to achieve the optical coupling between the VCSEL and waveguide. Based on current literature and a detailed patent search, there are two distinguishable research strands for achieving the out-of-plane optical coupling: assembled mirrors and integrated mirrors. Assembled mirrors place an optical sub-assembly, based on a BGA interposer, into a trench in the OECB. Integrated mirrors combine 90° deflecting mirrors into the OECB and provide an improved method compared to assembled mirrors due to the reduction of assembly parts reducing the cost and manufacturing tolerances. A gap in the current market for fully integrated mirrors is identified.

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Figure 3.1 ***Polymer Waveguide Manufacturing Processes:*** *moulding techniques, such as hot embossing (EOCB OptoFoil), create polymer films that are laminated into FR4 PCBs (a). Lithographic techniques develop polymer layers coated to PCBs (b).*

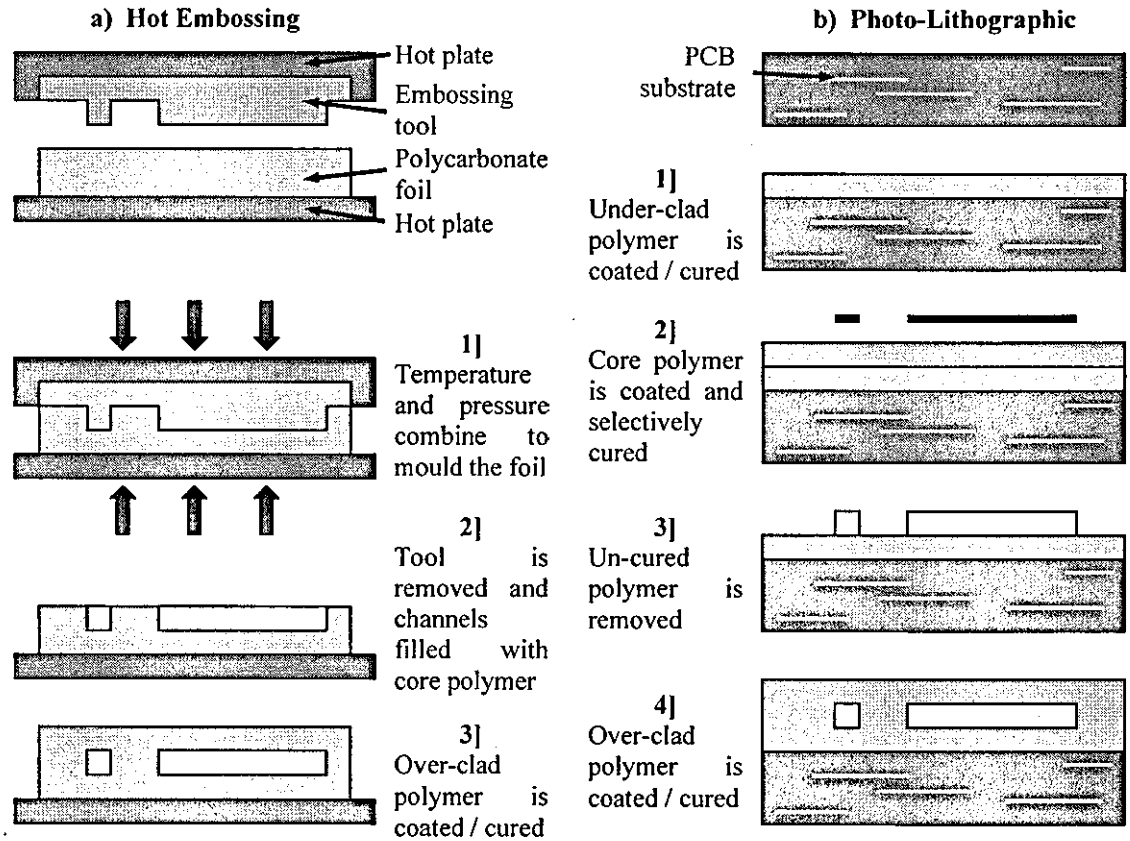


Figure 3.2 ***VCSEL Cross-Section:*** *layers of material are thinly deposited onto GaAs wafers to form DBR mirrors sandwiched either side of an active area. The quantum wells convert electrical energy into photons, emitting a light beam perpendicular to the surface of the substrate.*

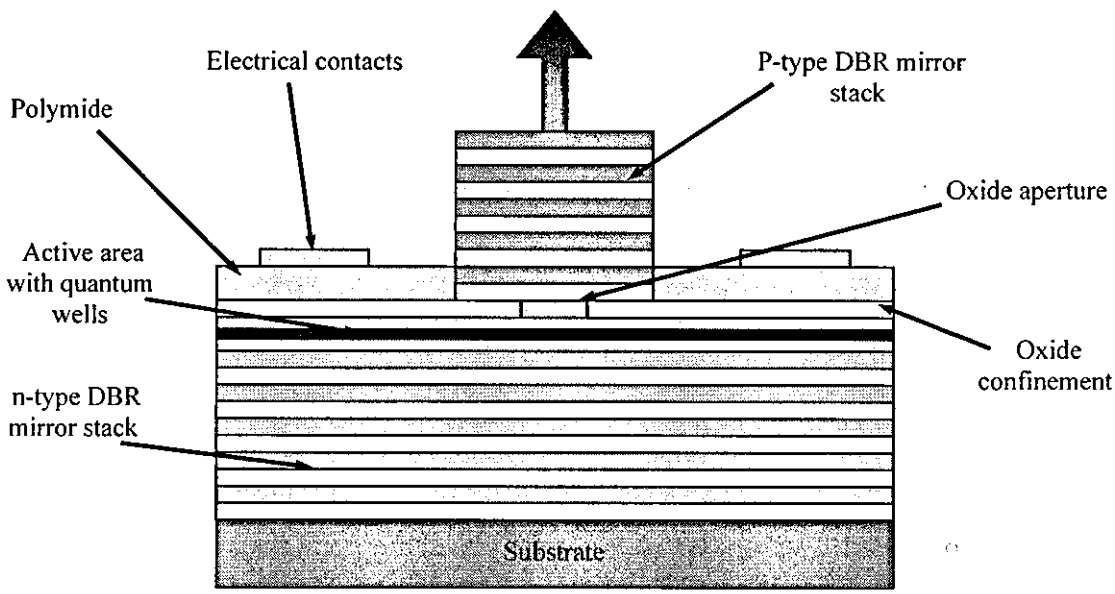


Figure 3.3 ***FCA Technologies:*** *VCSELs are assembled using non-solder based FCA technologies. Conventional wire-bonds form interconnects using thin wire loops (a). ACFs allow area array VCSEL IOs to be connected, although are not compatible with bottom emitting devices (b). SBBs are underfilled (c) or encapsulated (d).*

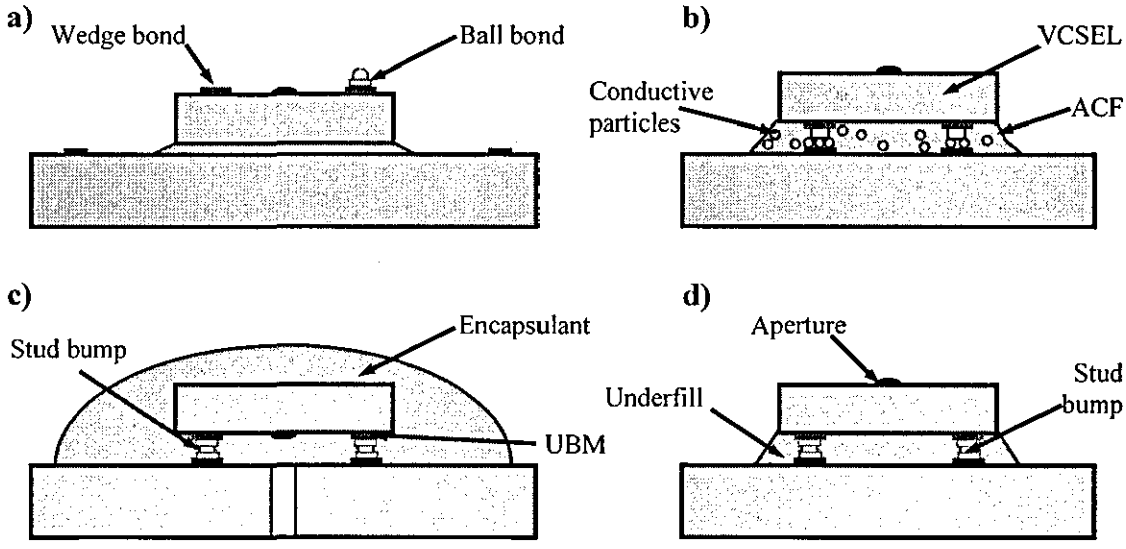


Figure 3.4 ***OECB Component Coupling Techniques:*** *typical configurations for coupling components to OECBs showing, on the top, two examples of assembled mirrors with the VCSEL mounted on an interposer allowing easier progression for other components such as fibre ferrules (a) and the VCSEL aligned to the waveguide supported by a carrier providing electrical contact (b). The bottom side of the OECB diagram shows examples of integrated mirrors with routes for connecting a wide variety of components (c) and a VCSEL assembled using an interposer (d)*

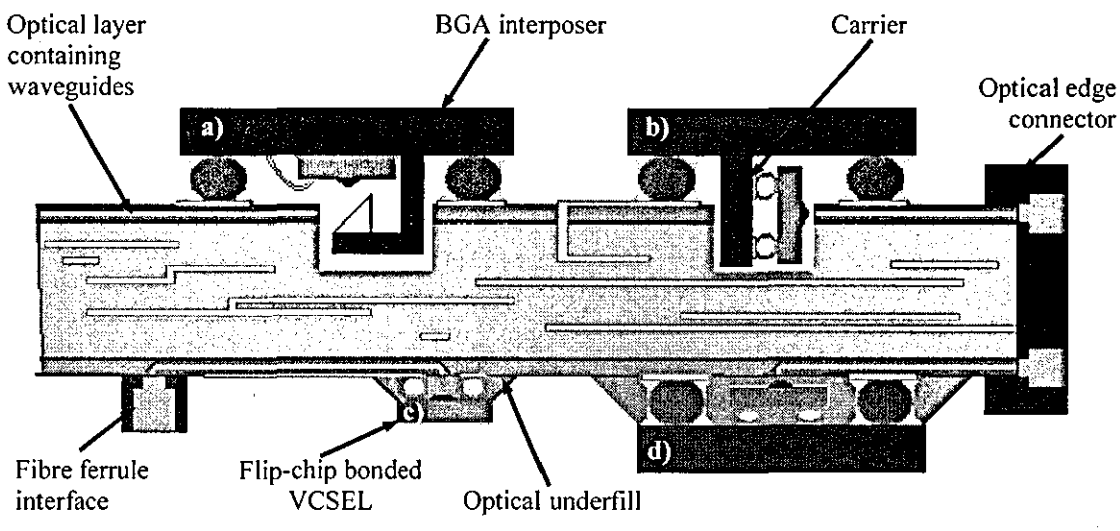


Figure 3.5 ***Integrated Mirror Techniques:*** *2nd surface integrated mirror (a) forms two surfaces and reflects the light from the openly slanted surface opposite to the waveguide end. 1st surface integrated mirror (b) forms a slanted mirror directly on the end of the waveguide.*

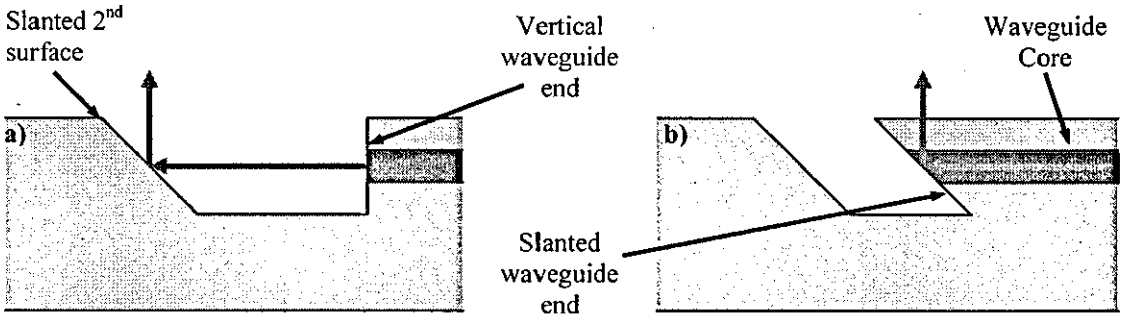
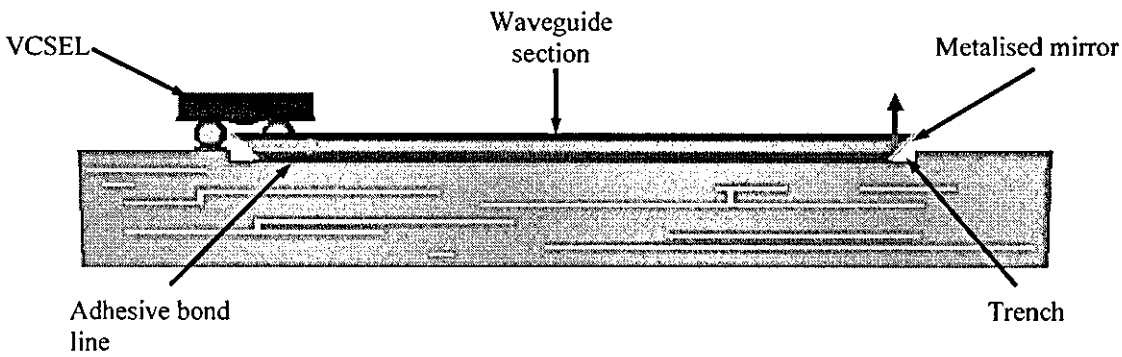


Figure 3.6 ***Intel Demonstrator:*** *a waveguide section is laminated into a trench in an FR-4 board to provide board integrated optical interconnects. 45° metalised mirrors on the ends of the waveguide section direct the light to travel out-of-plane.*



Chapter 4

The OECB Demonstrator

4.0 Integrated Mirror Manufacturing

To enable OECBs to become commercially viable, integrated mirrors are required. As identified in Chapter 3, OECBs are hybrid substrates consisting of FR-4 layers combined with an optical layer. Unlike assembled mirror methods that optically couple SMT assembled devices with the waveguides through sub assemblies that are inserted into trenches in the OECB, integrated mirrors are structures formed within the OECB substrate. As identified in the patent review (section 3.3), integrated mirrors can reflect light either from the 2nd or ideally the 1st surface. Intel [1] have demonstrated an operational board-level optical interconnect, which connects two surface mounted components over 20cm using 1st surface integrated mirrors. To improve on the Intel demonstrator, 1st surface integrated mirrors are required that demonstrate comparable performance and insertion losses (1.5 – 3 dB) but importantly at a lower cost and complexity. Removing the handling and precise bonding of the small waveguide sections from the OECB fabrication process can drive out the cost.

The costs associated with handling the small waveguide section can be removed by laminating full sized optical layer sections, such as in the EOCB [2, 3] and TOPCat [4] projects. Polymer optical layers that include pre-determined waveguide paths are included into the FR-4 stack and laminated into one substrate. The lamination process requires careful alignment of the optical layer to the FR-4 layers to ensure that SMT pads are correctly positioned with respect to the waveguides. The IO mirrors can be fabricated in the optical layer prior to the lamination process and the optical layers are often embedded under a top layer of FR-4. However, utilising current PCB manufacturing techniques, which are introduced in Chapter 2, is also an important factor in promoting low-cost. Presently, both projects (EOCB and TOPCat) use embossing processes, which are not compatible with PCB fabrication techniques.

Alternative methods of fabricating the optical layers, such as in Terahertz Truemode [5], allows the waveguides to be coated directly onto the FR-4 and, in doing so,

enables the careful positioning of the waveguide to SMT pads to be achieved through alignment of a mask or laser beam to fiducials. The optical layer can be treated like the final resin layer and have copper tracks defined directly on top. The coating and curing process is similar to current photo-imageable processes in the PCB fabrication and is therefore beneficial. Forming the copper circuitry directly on the top of the optical layer also reduces the distance between the chip and waveguide and eliminates the need for an optical via through layers of FR-4. Due to the low-cost manufacturing benefits, the OECB demonstrator uses Terahertz Truemode polymer to form the optical layer.

In order to couple with SMT devices, OECB substrates that have an optical layer coated onto the outside of the board, require integrated mirrors to be fabricated after the coating and waveguide formation step. Since the integrated mirrors are fabricated after the FR-4 bonding process, the structures are not required to be compatible with the high temperature and pressure generated during lamination. However, the mirrors are required to be compatible with PCA processes, which may consist of two reflow cycles, one wave profile and two rework heat cycles. The approximate temperature profiles for solder reflow are identified in table 2.1 and can be found in [6]. Because OECB assemblies are expected to be required long after the 2006 lead-free deadline [7] the OECB assemblies and mirror structures must be compatible with lead-free reflow profiles. To that end, a novel integrated mirror manufacturing process is presented.

4.1 Overview of Integrated Mirror Manufacturing

In order for the 1st surface mirror to deflect the light out of the top surface of the board, the physical geometry is defined such that the mirrored surface needs to be undercutting from the top perspective. Traditional methods of creating three-dimensional structures such as greyscale imaging and raster scanning would need to form the angled structure from the underside and are therefore not compatible as this would involve removing a large area of the board underneath the interconnection site [8]. A much more attractive solution is to machine the undercut surface from the topside of the board. The manufacturing method is required to produce smooth surfaces in order to avoid reflective losses that are generated by light being scattered

from surface imperfections. Manufacturing methods for creating undercutting surfaces include mechanical methods, Reactive Ion Etching (RIE), and laser ablation.

4.1.1 Undercutting Surface Manufacture

Mechanical methods for forming undercutting surfaces include using a wafer saw to make an incision: for example [9] shows the mirror being formed by tilting the blade at an angle to the board's surface and making a cut. The method is capable of providing a suitable undercutting surface and can be easily scaled to produce a trench capable of intersecting multiple waveguides. However, due to the geometry of the circular blade, either the centre of the cut is deeper than required or excess material is removed at the edges. Due to both the limited "real estate" space on PCBs and because mechanical methods are not currently used within the PCB fabrication process, it is not commercially viable to produce the undercutting surfaces using a wafer saw or similar mechanical methods.

RIE has been extensively used in the formation of three-dimensional structures such as waveguides and coupling elements. Although photolithographic techniques were preferred to RIE for the fabrication of the waveguides, due to the poor side-wall characteristics [10], RIE has been successfully used to form structures on the ends of the waveguides [11, 12]. The undercutting surface is achieved by presenting the board at an angle to the RIE beam. Although capable of producing suitable structures, RIE is not used in PCB manufacture and therefore, in order to meet the low-cost specification, a PCB compatible process for creating the undercutting surface is required.

Laser ablation techniques are both capable of producing the structures and are also currently used in the high-volume production of PCB vias. PCB fabrication plants generally employ three types of laser for via drilling: Nd:YAG, CO_2, and Excimer [13]. Both Nd:YAG and CO_2 lasers use focussed circular beams and machine work pieces by relative movement between the substrate and the beam. Such point machining would therefore form the structures required for the integrated mirrors by ablating an angled channel across the waveguide ends. Excimer lasers however, ablate using area machining. Shaping the laser using a mask forms intricate shapes.

Ablating an area at the end of the waveguide with a flat edge across the waveguide would form the undercutting surface. The excimer process is detailed in Section 5.1.

4.1.2 Mirror Formation Manufacturing

The System for Transparent Avionic Routing (STAR) project [14] investigated the use of undercut surfaces, which produced 45° mirrors on the end of waveguides but without any post processing to enhance the reflection of the light upward from the substrate. Results from the Star project suggest that TIR mirrors are not capable of producing sufficient reflective efficiency to act as OECB mirrors [15]. Core-to-air TIR mirrors can be improved by backfilling the pockets with cladding material. To stop voids from occurring beneath the undercutting portion of the pocket, some kind of forced flow would need to be induced.

An alternative to TIR mirrors is to coat the mirror surface with a reflective metal. Metal coatings are deposited using selective methods such as masking and evaporation coating. However, these methods are suitable only for surfaces that are accessible from the top and are therefore not applicable to the undercutting surface. To this end, a novel manufacturing process for backfilling the machined pockets with a metal to create a highly reflective surface at the polymer-metal interface is presented in section 4.2.

4.2 Novel Integrated Mirror Manufacturing Process

The novel integrated mirror manufacturing process presented is a two-stage process for forming mirrors in polymer optical layers in order to achieve the out-of-plane optical coupling between waveguides and surface mounted components such as VCSELs, PDs and fibre connectors.

The first stage is to create an undercutting surface that intersects the waveguide structure that is formed in the OECB substrate, which is fabricated prior to the mirror manufacturing process. Although there are various methods available for forming the undercutting surface (Section 4.1.1), laser ablation is preferred due to its close synergy with current PCB manufacturing processes. The geometry of the

undercutting surface should enable the maximum amount of light to couple between the waveguide and surface mounted devices. For the perceived applications this requires the mirror surface to intersect the waveguides at right-angles when viewed from the top of the board and to be angled at 45° when viewed from the side.

The second step is to backfill the pocket with a metal to create a reflective surface at the interface between the metal and undercutting surface. It is proposed that to achieve the backfilling an electroplating process is used. Electrolytic deposition is preferred over electroless plating due to the selective nature of the process. Electrolytic deposition is the process of producing a coating on a surface by the action of an electric current. Due to this, the coating is formed onto a conducting surface (cathode). For the integrated mirror application a copper pad, formed between the polymer optical layer and the top layer of FR-4, acts as the cathode. The copper pad can also be used as a beam stop in the excimer laser ablation process. A micro etch is required to prepare the surface of the copper prior to the plating process. The micro etch also acts to remove debris from the pocket and to smooth micro roughness on the angled surface. With the copper pad electrically connected in a plating bath, a current is applied and metal plated until the pocket is filled. The novel two-step process for producing integrated mirrors is detailed in Figure 4.1.

4.2.1 Benefits of Novel Integrated Mirror Fabrication

In terms of application and function, the novel integrated mirror manufacturing process is not expected to produce significant performance benefits over existing methods. The predominant performance characteristic of the mirrors is the coupling loss. Since methods have already reported losses of less than 3dB, the fabricated mirrors are required to match, if not better, this benchmark.

The potential benefit of the novel process over documented integrated mirror process is cost reduction. The cost reduction is achieved through various mechanisms.

- **Part reduction:** reducing the number of parts removes the costs associated with them during the manufacturing process. This includes costs from materials, part

handling, and process steps. Using fewer parts also reduces the compound adding of alignment tolerances, which enables less precise processes to be employed.

- **Process compatibility:** using processes that are compatible with existing PCB fabrication methods significantly reduces the initial capital outlay that often inhibits the uptake of new technologies and also removes process development costs that occur when proving new processes.
- **Board similarity:** removing the profile step and maintaining a similar surface design to electrical PCBs eliminates the chance of complications in the assembly process, such as poor stencil contact during solder printing.

4.3 OECB Integrated Mirror Demonstrator

The capability of the integrated mirror manufacturing process is showcased using a demonstrator board. OECB demonstrator substrates were manufactured and prepared to enable the investigation of the manufacturing process parameters.

4.3.1 OECB Demonstrator Substrate

The demonstrator, which was procured from Terahertz Photonics, is fabricated from a core single layer FR-4 sheet. The Terahertz TrueMode waveguide material is used to create an optical layer. Due to the polymer adhering better to FR-4 when compared to copper, the top copper layer of the FR-4 sheet is processed in order to remove the majority of the covering, but leaving areas of copper to act as the beam stop / cathode during the mirror fabrication process. The waveguide material is spun-coated on top of the FR-4 using wafer processing equipment.

Although large layers can be uniformly coated using other methods and equipment, Terahertz's process capability restricted the size of the substrate to a 7-inch wafer. A 20μm under-cladding layer is coated and cured. A 50μm core layer is coated and selectively cured to define multiple waveguide paths such that they travel over the top of the copper areas. A final 20μm over-cladding layer is deposited giving the total optical layer a thickness of 90μm. The relatively thin cladding thickness of 20μm was selected as an advantage was perceived in keeping the cladding layers minimal to reduce the distance between the mirrors and surface although sufficient cladding is

required to enable MM waveguides to propagate. The cladding thickness can be increased in future demonstrators should benefits be perceived. The waveguides are pitched at 250μm to correspond with the pitch of VCSEL arrays. The 50μm waveguide core size was selected because this is the most common core diameter of MMF.

Matching the waveguide core size, to that of fibre, ensures maximum coupling efficiency between fibre – waveguide and waveguide –fibre. Applications that do not require the waveguides to couple with fibre can benefit from using larger core sizes. This becomes apparent because the natural VCSEL beam divergence means the beam spot is much larger than the active aperture, which creates coupling losses when the beam spot is larger than the waveguide core size. Increasing the waveguide core size can therefore increase coupling efficiency between waveguides and VCSELs. Although the effects of core size need to be considered for the broader OECB applications, it is not possible to fabricate a substrate with more than one core size; therefore, the demonstrator contains waveguides with only 50μm cores.

The 7-inch wafer shape OECB substrate was diced into useable samples (Figure 4.2) using a wafer saw. A polymer bonded wafer saw blade was used to cut the substrate. Standard metal matrix bonded blades were not used because, when cutting polymer materials, they become clogged and liable to jamming. They are also reported to give a lower surface finish on the edge of the optical layer, which presumably occurs due to the metal particles scratching the sides of the material as it cuts.

4.3.2 OECB Demonstrator Substrate Preparation

The diced OECB samples contain straight waveguide arrays running from side-to-side and formed directly over copper pads on the top surface of the core FR-4 boards. Angled pockets can be laser ablated (Chapter 5) and, by electrically connecting the copper pads, the pockets can be backfilled using an electroplating process (Chapter 6). The mirrors can be characterised by taking a reference measurement prior to forming an integrated mirror in the demonstrator; the Insertion Loss (IL) and other coupling characteristics can be subsequently determined by comparing the light levels after the mirror has been formed with the reference recording.

The reference measurement requires a transmitter to be coupled with a fibre patch-cord. The opposite end of the patch-cord is butt coupled to the edge of the demonstrator substrate and aligned so as the maximum amount of light travels down the waveguide. At the opposite end of the waveguide a bare fibre end of a second patch-cord is aligned to the same waveguide and the connectorised end coupled to a receiver. After forming an integrated mirror close to one end of the sample, the IL can be calculated by comparing the reference to the light coupled when the fibre is re-aligned at 90° to the substrates surface (Figure 4.3).

After the reference measurement has been taken the fibre connections and configurations are required to be kept as constant as possible in order to eliminate errors, generated for example by poor or good alignment, and to therefore ensure the measurement is a true measure. To ensure this consistency the butt coupled fibre at the transmitter side of the demonstrator is required to be permanently fixed in position by optical adhesive. The fibre attachment process is detailed further in Chapter 7.

4.4 Experimental Design Methodology

Based on a structured approach to optimisation, Design of Experiments (DOE) methods are the best tools to separate important parameters from unimportant ones. [16] (World Class Quality – Using design of experiments to make it happen), identifies three DOE tools: Classical, Taguchi, and Shainin. The classical DOE approach is based on changing one factor at a time, which for a high number of factors produces unnecessarily large experiments that are often inconceivable. Taguchi reduces the number of experiments although still confounds the interaction effects with the main effects producing results which are statistically poor and are often unreliable. The Shainin DOE approach uses a collection of 10 tools each of which has a specific application in problem solving. The ten DOE tools can be linked in a sequence to systematically eliminate up to 1000 variables until only the top few are distilled for corrective action and preventative control. Reference [16] concludes that, of the three techniques, Shainin DOE methods provide the strongest tools for efficient process optimisation and, as such, has been adopted by Celestica Ltd. as a preferred DOE technique.

The ten tools used by Shainin and how they link together are detailed in Figure 4.4. Figure 4.5 details the Shainin DOE process through the use of a step-by-step flow chart. Following the flow chart in figure 4.5, the first step is to identify the factor that needs to be controlled or investigated, dubbed the Green Y by Shainin, which must be quantifiable and measurable. Every attempt should be made to locate an earlier Green Y in the process that may be easier to measure and that is likely to have a reasonable correlation with the final Green Y. Measurement accuracy or discrimination is defined in terms of part variation to measurement accuracy; it is recommended that a Green Y measurement accuracy of 5:1 is used to ensure the measured variations are coming from the process and not uncertainties introduced by the measuring instrument. The DOE tools are used in order to distil the parameters and interactions that most affect the Green Y. Details of each individual analysis tool can be found in reference [16]. The parameter or interaction that has the most impact is dubbed the red X. The red X can be optimised using the optimisation methods.

4.4.1 Experimental Design

Both steps in the novel two-stage process require development. The green Y for the completed mirrors is ultimately the IL, which can be determined by measuring the amount of light that can be coupled into a fibre that is aligned normal to the OECB substrate (Chapter 7). The surface roughness of the undercut mirror is a possible earlier green Y; however, although the results will correlate closely with the IL and can be used to analyse the laser ablation process parameters, the undercutting nature of the surface inhibits measurement of the surface roughness, for example using a Scanning Electron Microscope (SEM) or interferometer. IL is the only measurable green Y.

Air-cladding TIR mirrors are not expected to give sufficient performance to allow measurement of the IL. As such, the ablation and plating process parameters cannot be analysed individually because the IL green Y measurement requires both the process steps to be completed. Shainin DOE methodology is the preferred structure for identifying the important process variables and their effects on the mirror IL; however, the methodology requires that all the process variables are capable of being held constant. This was not the case for the experimental equipment configuration

setup and, as explained in Chapter 7, this coupled with other issues meant that it was not possible to follow the detailed Shainin approach. Therefore, although a structured approach was still followed, the Shainin DOE methodology is still preferred and, as such, should be followed for any further development suggested in Chapter 10.

4.5 Summary

Integrated mirrors are required to enable OECBs to cost-effectively couple with optical components. Intel has reported an integrated mirror with coupling losses in the region of 1.5-3 dB, although driving cost from the demonstrator is key conclusion. Forming the waveguides directly to substrates eliminates the costs and processes involved in forming and laminating thin waveguide sheets. Terahertz has developed a polymer which can be directly coated to the out side layers of PCBs and that can be patterned using standard lithographic techniques. A novel two stage process is presented for creating integrated mirrors into such polymer waveguides.

The first stage is to laser ablate an undercutting pocket to create a surface whose geometry is such that incident light is reflected into the waveguide. The pocket is backfilled using an electrolytic deposition process in order to create a reflective interface at the undercutting polymer boundary. The novel process promises benefits over existing methods such as: part reduction, process capability, and board similarity. The integrated mirrors can be characterised and through a prepared demonstrator. The Shainin experimental design methodology is the preferred method for investigating the effects of the process parameters.

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Figure 4.1 Novel *Two-Step Integrated Mirror Manufacturing Process:* *the manufacturing process consists of laser ablating an angled pocket in order to create an undercutting surface, followed by backfilling the pocket using an electroplating process that first requires a micro etch to prepare the copper surface (a). A copper pad, formed under the optical layer prior to the waveguide coating, acts as a beam stop for the ablation process (b). The copper pad is electrically connected to act as a cathode during the metal plating (c).*

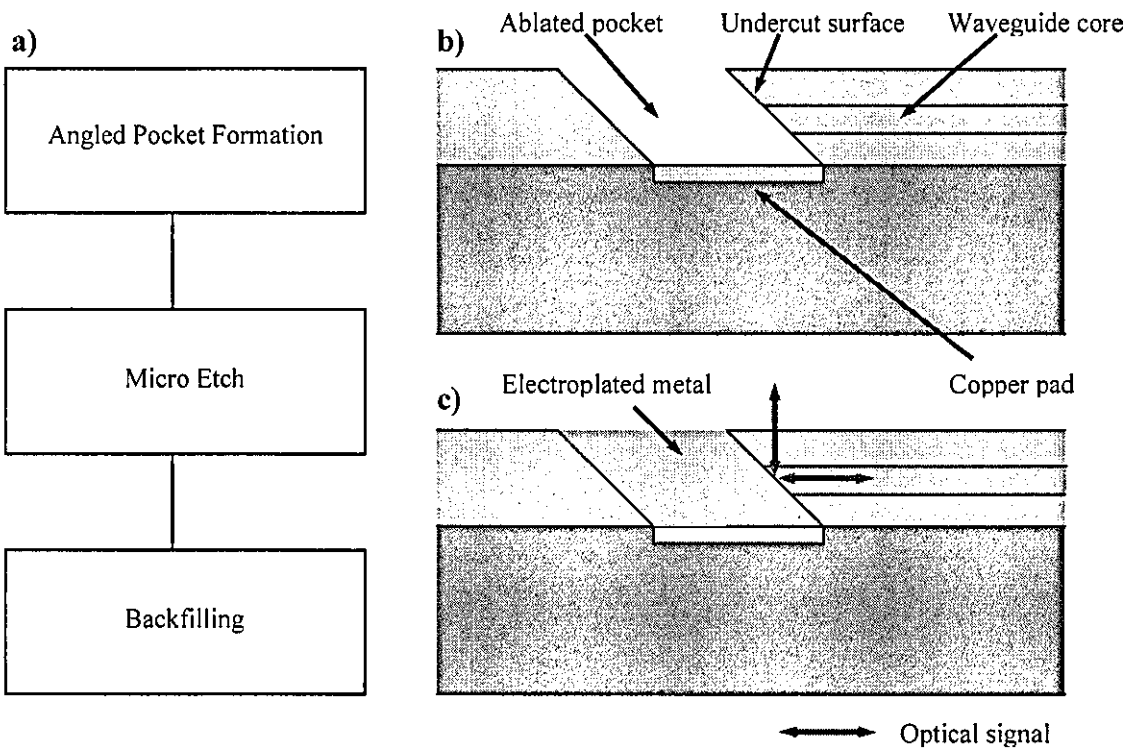


Figure 4.2 ***OECB Demonstrator Substrate:*** *wafer demonstrator is diced into useable substrates with positions for the formation of the integrated mirror structures.*

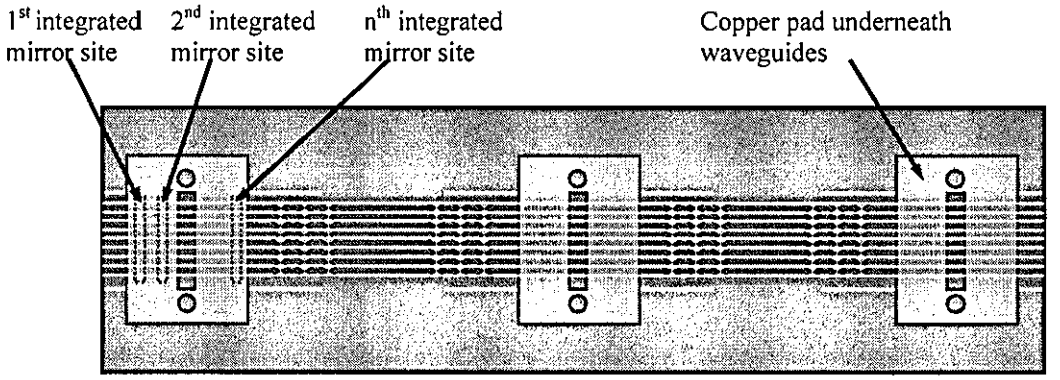


Figure 4.3 ***OECB Mirror Characterisation Set-Up:*** *a reference measurement is taken by butt coupling fibre to either end of the OECB demonstrator in order to connect a transmitter and receiver through the waveguide (Step 1). After an integrated mirror has been formed in the substrate, the demonstrator is re-positioned and the new light level compared to the reference (Step 2).*

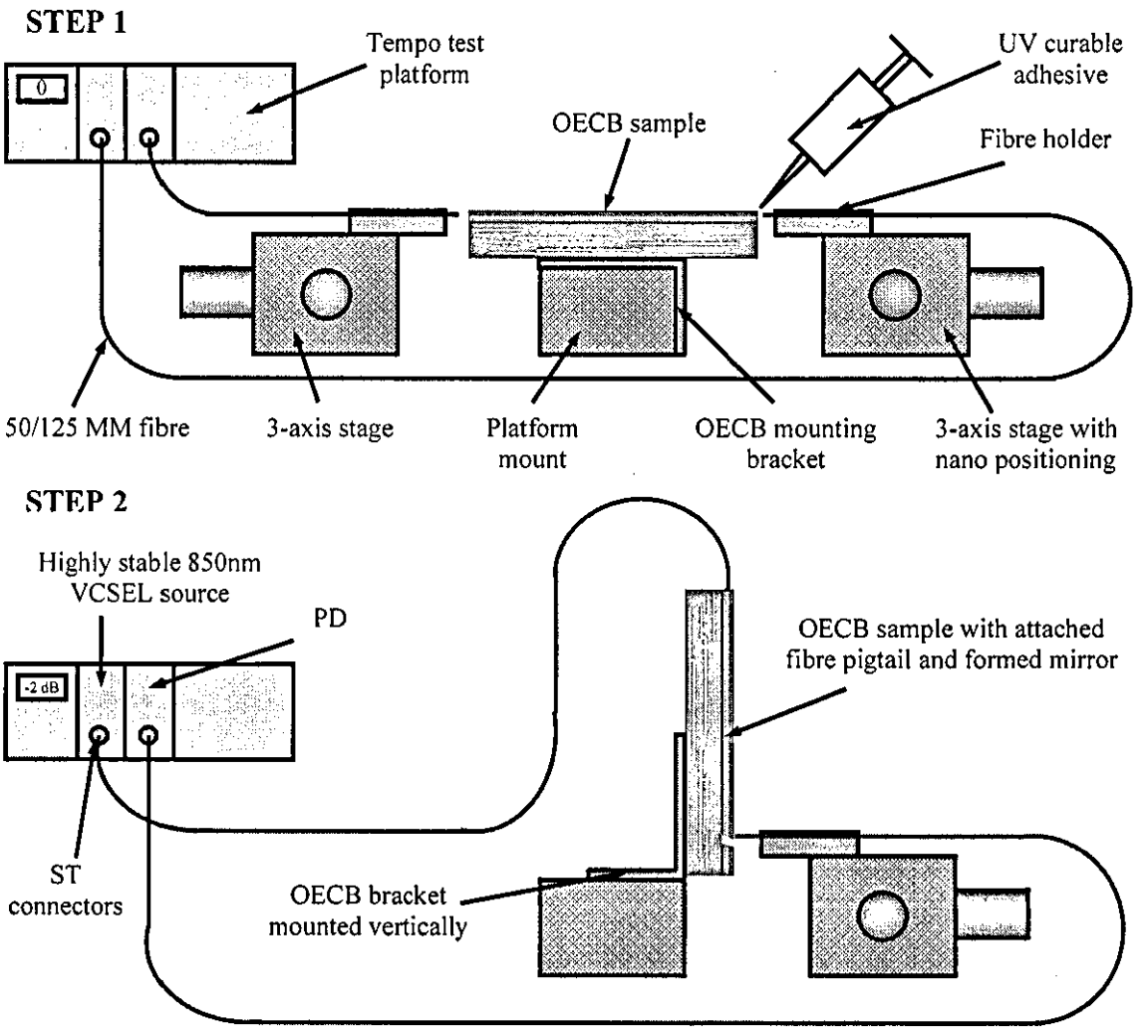


Figure 4.4 Systematic Flow of Shainin's 10 DOE Tools: *the 10 DOE tools (Multi-vari, component search, paired comparisons, product / process search, concentration chart, variables search, full factorials, B vs C, scatter plots, and response surface methodology) link in a sequenced manner.*

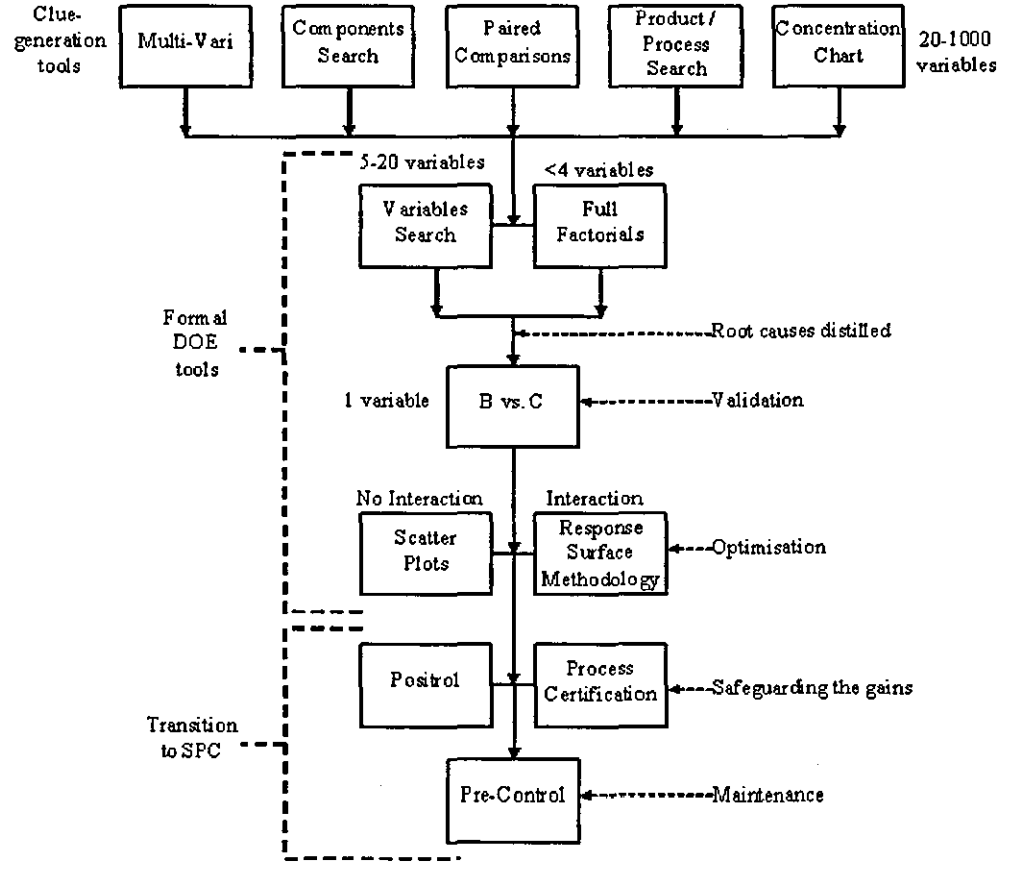
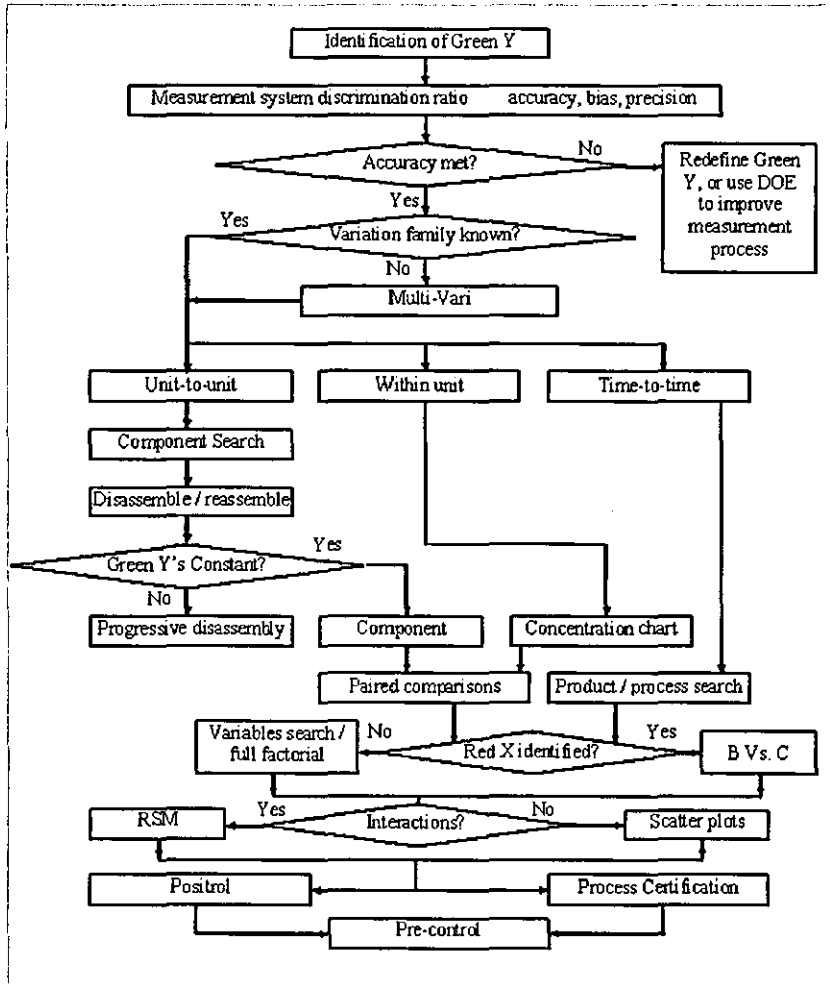


Figure 4.5 The Search for the Red X: A Problem-Solving Roadmap: *Shainin DOEs start with the identification of the green Y and proceed with the progressive use of each DOE tool to distil the red X.*



Chapter 5

Laser Ablation

5.0 Introduction

Within the PCB fabrication industry, the three laser technologies presently used for microvia formation are: CO_2, Nd-YAG, and excimer lasers [1]. CO_2 lasers are the most common for volume production due to the speed of drilling; however, the need for an additional process to penetrate copper layers has seen UV-YAG lasers used in conjunction or in place of the CO_2 laser. Excimers are not as widely used in volume via drilling as the ablation mechanism results in relatively slow drilling times. However, the excimer laser does produce excellent via properties due to machining characteristics such as ultra-small structures and high absorption rates. Excimer lasers are used predominately for applications where only a thin layer of dielectric is removed and microvia diameters are less than 150μm. As a consequence, Excimer lasers are the most suitable for the formation of the undercutting surface in order to produce the first surface integrated mirrors.

5.1 Excimer Lasers

A detailed evaluation of the laser process can be found in [2-6]. As with all lasers, excimers consist of an active medium, a pumping device, and a resonating cavity. For excimer lasers the active medium, which determines the laser beams wavelength, is a rare gas halide such as: Argon Fluoride (ArF) – 193nm, Krypton Fluoride (KrF) – 248nm, Xenon Chloride (XeCl) – 308nm, and Xenon Fluoride (XeF) – 350nm.
Lasing occurs by the stimulated emission of photons. Stimulated emission requires a population inversion from the ground state to the excited state. Excimer molecules cannot be excited directly from the ground state; therefore, various mechanisms of indirect excitation within the discharge are employed. Vigorous pumping is required to achieve the population inversion which invariably leads to the adoption of pulsed operation. Excimer lasers produce pulses of high energy photons, which exit the resonating cavity as a beam. The beam may be homogenised to produce a more uniform power distribution across the beam profile and is shaped by a mask prior to

being focussed. The focussed beam provides an area of high irradiance where the beam interacts with a substrate material.

The principle behind laser material processing is to bombard a substrate material with a beam of photons generated by the lasing process. Dependant on the wavelength of the beam, the surface atoms of the substrate can reflect, absorb, or transmit the photons. The suitability of a laser to machine a given substrate is determined by the absorption rate of the photons. As the photons are absorbed, dependant on the energy of the photons either ablation occurs or the area is heated. If the energy contained by the photons is greater than the energy in the bonds between the surface atoms then ablation occurs. Ablation is the term given to material removal and results from atoms absorbing high energy photons which break the atomic bonds between the surface atoms; the break down of the bonds generates a rapid rise in particle density and pressure resulting in a mini explosion which expels the broken particles as dust. If the energy of the photons is less than the force holding them together, the photons effectively shake the bonds and release the energy as heat.

Ablation is the mechanism used to create microstructures such as micro-vias and is a near non-thermal process. The beam shaping and manipulation, which occurs after the beam leaves the laser resonating cavity and is encompassed in the front end optics, ensures better uniform processing. The excimer laser situated in the Wolfson School of Mechanical and Manufacturing Engineering, Optical Engineering Group was used to investigate the laser ablation of Terahertz's fluorinated acrylate, TrueMode, waveguide material. The laser is a KrF excimer with a front end, which irradiates the beam at 90° to the substrate material.

5.1.1 Loughborough's Excimer Laser

The excimer uses KrF with a wavelength of 248nm. Feedback control equipment is capable of controlling the energy and the pulse rate of the laser output. Additionally, a rotational attenuator is housed on the aperture of the resonating cavity in order to manually adjust the beam power immediately prior to the front end optics. The front end optics generates additional attenuation due to the efficiency of the mirrors and beam manipulation elements.

Details of the original front end optics on the Loughborough excimer laser are given in Figure 5.1. The beam exits the resonating cavity through an adjustable attenuator and is folded before being reflected vertically down towards the substrate material. Cylindrical optics homogenise the beam to make it more uniform and square. The beam is collimated by a field lens immediately prior to the mask plane. A mask is used to shape the beam in order to give the desired final geometry. The final focus lens focuses the beam onto the work piece by a ratio of 15:1, machining a two-dimensional image of the mask into the work piece. Due to the beam being focussed onto the work piece, it is important that the surface is kept level at the focus point. Focus is maintained by a visible laser and PD arrangement that reflects off the surface of the substrate and is connected to the z-axis control of a positioning stage for feedback control. The positioning stage moves in the x- and y- planes in order to correctly position the substrate. The visible spot, produced by the visible HeNe focus laser, is used as a reference in order to correctly align the substrate and excimer beam.

In order to validate excimer ablation of the angled pocket as a feasible solution to creating the undercut surface for the integrated mirror application without significant expenditure, it is necessary to use the existing front end optics.

5.2 Initial Laser Ablation Trials

To quickly analyse the effectiveness of using an excimer laser to ablate the angled pockets, a jig was manufactured to present the OECB demonstrator samples at 45° to the focussed laser beam of the existing excimer laser at Loughborough University.

The jig enabled trial pockets to be ablated and cross sectioned in order to analyse the dimensions of the ablated structures.

5.2.1 Jig Manufacture

The jig is required to present the OECB samples at 45° to the beam and to facilitate the focussing of the sample using the existing front end optics and focussing system. Since the aim of the initial trials is only to give an indication as to the ability of the process to create smooth undercutting surfaces in the TrueMode polymer, it is not necessary for the OECB samples used during the initial trials to contain waveguides. As such, spare areas of the OECB wafer sample, that do not affect the main waveguide and copper pad areas, were used. Due to the varying dimensions of the samples, it is therefore a further requirement that the jig contains adjustable mounting fixtures in order to mount varying sizes of samples.

Figure 5.2 details the manufactured jig. The OECB samples are mounted to the jig using left and right mounting plates. The left mounting plate is adjustable in order to mount different sizes of samples. The mounting plates are located on two main rods which determine the angle that the sample is presented to the beam. Since the beam is vertical, the rods are mechanically fixed at 45° to the base plate. The base plate contains bolt holes to fix the jig to the positioning stages. Focus is achieved through the focussing table. The focussing table can be adjusted to position the top of the table directly adjacent to the ablation area. Focus can be achieved by using the positioning stages to locate the visible HeNe focussing laser spot on to the top of the focussing table, whilst using the z- axis of the positioning stages to find focus. Forming the pocket just over the edge of the table ensures the ablation occurs at the focus point.

5.2.2 Initial Trial Results and Discussion

During the ablation trials a standard rectangular mask, which was fabricated from a blank with a rectangular 15mm by 5mm aperture cut in the centre, was used to ablate a large pocket in the OECB samples. Due to the 15:1 reduction and also the trigonometric effects of the angled beam, the ablated pockets were rectangular and

approximately 1mm by 0.5mm. During the trials, various process parameters were used and each parameter set repeated in order to quickly identify any important parameters in the formation of the undercutting surface. As predicted, numerous non-destructive efforts to directly view and measure the undercutting surface were unsuccessful. The trial pockets were therefore analysed using cross-section methods and were also prepared and analysed using a Scanning Electron Microscope (SEM). The results were varied and inconsistent.

The initial trials demonstrated the ability of the laser ablation method to both create undercutting structures (Figure 5.3 and 5.4) and also the suitability of copper to act as a beam stop (Figure 5.4); however, many of the trial results failed to create any undercutting surfaces and instead created two openly angled sidewalls. DOE methodology concludes that because the poor results appeared randomly and with different results between repeated parameter sets, the critical factor in achieving undercutting surfaces is poorly controlled. Due to the set-up, the factor with the greatest inconsistency is focus. Despite the focussing table, focus is poorly controlled because it cannot be guaranteed that the top of the focussing table is the same as the substrate area being ablated. It was concluded by further trials that the first critical factor in achieving the undercutting surface was focus.

In order to characterise the undercutting surface, the structures need to be formed accurately along the path of the waveguides. During the initial trials it was observed that the existing alignment system, which uses the visible HeNe laser beam spot as a reference, would not be able to achieve sufficient alignment positioning. Since it is not possible both to add a vision system for alignment purposes and to adapt the focussing system within the existing set-up, a new front end optical set-up is required in order to conduct further trials.

The analysis of the initial results identifies a further issue with the process. Many of the ablated pockets exhibited similar ripple marks in the side walls (Figure 5.5). Since the excimer set-up is an imaging system, the ripples could be striation marks, which could be eliminated by using a better mask. A high quality mask is required for the further trials in order to remove the striation marks.

5.3 New Front End Optics

Although sufficient results were observed to show the excimer was capable of creating undercut surfaces, to proceed with the research a new front end to the laser was required to firstly enable the beam to be address a flat work piece and secondly to allow vision equipment to be added for alignment purposes.

The experimental front end optical set-up is designed to enable the substrate to be fixed flat to the positioning stages. This was achieved by adding an extra mirror into the excimer's optical path in order to direct the light at a 45° angle (Figure 5.6). The significant advantage in orientating the work piece such as to be flat to the positioning stages is that, once focus is found, the top of the sample can be easily, consistently and independently positioned at this reference plane regardless of the relation between measurement point and ablation area. Therefore in addition to presenting the OECB sample flat to the stages, it was also necessary to incorporate a reliable reference height system to position the top of the sample. The reference measurement is required to set the distance between the samples surface and the final focus optic. After consultation with industry experts the quickest and most cost effective apparatus fit for this purpose was a mechanical gauging probe, which was subsequently procured.

The new optical path allows vision equipment to be mounted directly above the ablation site. On-screen cross-hairs, which are aligned to the laser beam, are used in conjunction with the stages to position the substrate in order to precisely machine determined points. The vision system is also used to ensure that the mirror intersects the waveguides at 90°.

The set-up of the experimental front end is detailed in Figure 5.6. The arrangement is encased in a box for cleanliness and safety issues. The system is aligned to the excimer laser (Figures 5.7 and 5.8). After alignment to the laser, holding burn paper in the beam path aligns the beam turning mirrors. In order to start further trials into the characteristics and process parameters of the undercutting surface, it is required that a mask is manufactured, focus found, and the final mirror angle set.

5.3.1 Mask Manufacture

The ablation pattern machined into the substrate is defined by shaping the beam at the mask plane. Prior to the laser beam reaching the mask plane, two shaping optics are used to manipulate the beam to create a more uniform intensity distribution across the area illuminated at the mask. The optics not only homogenise the beam, by folding it through its axis, but also reshape the beam into a vertical rectangle. The beam exposes the mask plane with a vertical rectangle approximately 15mm x 5mm.

In order to machine, in one step, as many waveguides in the array (Section 4.3) as possible, the mask is required to ablate a rectangular pocket in the substrate that is longer in x- than the y- direction; therefore the current beam reshaping is not the optimum design for the integrated mirror application (Figure 5.9). Without reconfiguring the homogenising optics, the 10:1 magnification means the maximum useable pocket width is approximately 400μm. Although 400μm will only enable two waveguides, a fraction of the array, to be intersected by each mirror, stepping the ablated pocket across the waveguide array will enable all the waveguides to be intersected by a mirror and also produce more independent measurements.

The mask plane houses circular blanks, with a diameter of 29mm, into which apertures can be machined in order to give the ablation the desired geometry. The edge quality of the apertures is directly related to the quality of the mirror surface; therefore, the machining methods used to fabricate the apertures must ensure the edges are smooth. Masks can be manufactured using mechanical, laser or etching methods. In order to prototype masks quickly and efficiently, brass blanks were fabricated and apertures machined using mechanical methods. Rectangular mask were used for the further trials and in order to minimise the effects of striation masks, polished metal shim was adhered to the mask to give the undercutting wall defect free features (Figure 5.10a). The apertures are required to remain inside the area of the mask illuminated by the beam, which is approximately 15mm x 5mm. further trials were conducted using a large rectangular mask (4mm x 5mm) and a small rectangular mask (4mm x 2mm).

5.3.2 Determining Lens Focal Point

After the new front end is aligned to the excimer laser, the focal point of the final focus lens needs to be determined. Once determined, the gauge probe can be set to read zero at this point and used to consistently return the top surface of substrates to the focus point for machining.

In order to find the focal point, a focus mask was manufactured (Section 5.3.2). The mask consists of a brass blank with three circular apertures, of different diameters, machined in the centre. With the mask in the mask holder, the positional stages alter the lens to workpiece distance, firing the laser at each point to ablate a substrate. Focus is found when each of the three circular apertures appears clearly defined as ellipses in the incident substrate: the ablation pattern is a series of ellipses due to geometric effects. Since the focus point is independent of the incident material, 35mm photographic film was used due to its inherent machining properties. The film was blackened with marker pen for display purposes prior to ablation.

The effect of focus on the ablation structure is displayed in Figure 5.11. It is clearly visible that focus is required to be tightly controlled in order to maintain a crisp and defined structure. The gauge probe is therefore required to set the top surface of a substrate within ± 50μm of the determined focus point.

5.3.3 Final Mirror Angle

The final process step in setting up the front end is to set the angle of tilt of the final mirror to ensure the beam machines an undercutting surface at 45° to the substrate. The tilt of the final deflecting mirror can be set using a screw at the back of the mirror to change its angle. In trial and error fashion, the tilt of the mirror was set by ablating a pocket and measuring the angle of the undercutting surface. Encapsulating the OECB samples in a thermosetting resin and polishing to expose the pockets enabled the angle of the undercutting surface to be measured using a microscope. The measurement was taken using the centre section of the pocket to avoid spurious results from machining issues at the top and bottom of the pockets (Figure 5.12).

In between iterations of the trial and error process to set the angle of tilt of the final mirror, the undercutting surface angle was measured and the result analysed to determine if the tilt of the mirror required further adjustment. Altering the tilt of the mirror requires the focus point to be reset. After the trial and error process, the final mirror was set and the angle of the undercutting surface determined, using the mean measurement of repeated ablations, to be 46.09°. Although the angle of the undercutting surface is not exactly 45°, without developing a more precise method for altering the tilt of the final mirror, it is as close as can be reasonably expected.

The tolerance on the angle of the undercutting surface is of greater importance in consistently coupling SMT assembled components to the waveguides when compared to the angle itself. Using basic calculations it can be seen that a variance of ±5°, on the angle of the undercutting surface, can distort a mode travelling down the centre of the waveguide by approximately ±45μm at a standoff height of 250μm (Figure 5.13). In terms of passively coupling MM fibre with the waveguide, this large variance can result in the light becoming completely misaligned. The distribution of the measured angle of the undercutting surface is approximately 2°; however, this may improve as the ablation process is developed. Although the acceptable angle tolerance will be largely determined by the component assembly architecture, which will require further investigation during assembly trials, in the interim, a distribution of ± 1° is thought to be acceptable.

5.3.4 Vision Equipment

The vision equipment is required to monitor the ablation process and to align the excimer beam with the OECB sample. As such, the equipment added consists of a CCD camera, lighting, cross-hairs and monitor. The camera is installed in order to view the ablation site directly from the top perspective. The cross-hairs display permanent marks on the monitor to which the ablation mark of the excimer laser can be aligned. Ablating a substrate and aligning the cross-hairs with the mark viewed through the monitor enables subsequent substrates to be positioned to the cross-hairs and therefore predetermine the exact location of the ablated pocket.

Throughout the electronics industry the visual alignment of substrates to cross-hairs is completed using fiducials, which are reference marks in the substrate. The exact locations of all the features on a substrate are positioned relative to the fiducial marks. Subsequent assembly processes align to the reference marks in order to ensure the operation is completed at the correct position on the substrate. In the absence of an accurate fiducial on the demonstrator substrate, which could be used to determine the location of the waveguides, it is necessary to align the ablated pocket position directly with the waveguides. Since the waveguides are not clearly visible, they are required to be illuminated in order for their position to be viewed by the camera. During alignment with the cross-hairs a visible red HeNe laser, used for finding faults in optical fibre, was attached using a fibre ferrule to the end of the fibre that is aligned and adhered to the waveguide. With the waveguide illuminated the substrate is positioned on the stages using the cross-hairs to ensure the ablated pattern is formed in the desired position and at right angles to the waveguide.

5.4 Further Trials

Completing the commissioning of the front end optics enables further ablation trials to be completed in order to better investigate the ablation process parameters. It is desired that a structured DOE approach is employed to investigate the process parameters (Section 4.4). The further ablation trials consist of first taking a reference measurement, then ablating and back filling a pocket to create the integrated mirrors, and finally taking a new measurement and comparing it to the reference.

5.4.1 Ablation Parameters

When using DOE techniques the first step after identifying the green Y, which is IL for the integrated mirrors, is to define the measurement accuracy to ensure the variations in the measured IL are coming from the controlled parameters and not unidentified parameters or identified parameters being poorly controlled. A range of mirrors are required to be produced and characterised over a period of time in order to define the measurement accuracy. Due to uncertainties in the capabilities of the electroplating process, the two rectangular mask shapes (large and small) detailed in

Section 5.3.1, were used to create pockets for creating the integrated mirrors necessary to determine measurement accuracy.

The demonstrator samples were all machined within the 50μm tolerance of the set focus position. In order to determine the measurement accuracy, the pockets were all machined using the same laser parameters. Power and time are the two laser parameters that are controllable.

5.4.2 Laser Power and Time

The laser power is set at the laser head and manually adjusted using the rotational attenuator. Due to this manual attenuator setting, the laser system contains no built in way of monitoring the laser power reaching the substrates surface.

During the initial trials and the procedure for commissioning the new front end, two trends were observed during ablation; 1, at high laser powers blackening occurred around the ablated pocket and 2, it was clearly visible that the area under the undercutting surface was removed at a slower rate. The blackening was not observed at lower powers and could therefore be associated with a heat affected zone. In order to eliminate the possibility of the blackening affecting the light coupling from the mirrors, the ablation power was set below the levels at which the blackening occurred. The area under the undercutting surface could machine slower due to the hampered escape route for the removed material. A gas jet could be applied to aid the material removal; however, because the material is removed by extending the ablation time and that this does not affect the depth of the ablated pocket, since this is limited by the copper area under the ablation zone, a gas jet is not required. As areas of the copper become exposed at the bottom of the ablated pocket, it is important that reflections from these copper areas do not adversely affect the undercutting surface. In order to ensure that reflections do not ablate any more of the polymer material, the laser beam was set at a low level.

The laser power was set by attenuating the laser beam, using the rotational attenuator, to a power at which the waveguide material is not ablated. By incrementally adjusting the attenuator and observing the ablation result, a power level sufficient to

ablate the waveguide is set. The time of the ablation is determined by the time necessary to reveal copper completely across the bottom of the pocket. An ablation time of 20s ensures the complete material removal.

In the absence of a built-in monitoring device to ensure the consistent setting of the laser power, the laser power was kept consistent by repeating the attenuation procedure between ablation periods.

5.4.3 Further Trial Results

The main characterisation of the ablation process is completed after the formation of the integrated mirrors; however, to ensure the integrity of the pockets being formed, samples of the ablated pockets were cross-sectioned prior to the backfilling procedure.

The cross-section results showed that repeated undercutting structures were formed (Figure 5.14). Each of the results exhibited a reasonable undercutting angle at around 45° and also a reasonable depth to the pocket. The problem with the pockets being formed with two openly angled sidewalls that was observed in the initial trials was not observed. The new set-up changed the control over only one factor; focus. Accordingly, focus is likely to be the major factor in causing the open cut surface.

5.5 Summary

Laser processing is widely used in the PCB industry. Excimer lasers employ focussed beams, which are shaped using masks, to ablate substrates and such systems are particularly suited to creating microstructures. Polymers including the flurionated acrylic used to produce the OECB demonstrators keenly absorb the 248nm wavelength produced by KrF excimer lasers. A jig, manufactured to address substrates at 45° to an existing excimer laser set-up at Loughborough University, enabled initial trials to assess the validity of the ablation process to produce undercutting surfaces. Although undercutting surfaces were recorded, the results were varied and inconsistent.

The design, manufacture and assembly of a new front-end optics addressed the inconsistency problems identified by the initial trials. Focus was determined and limits set at ± 50μm, outside of which focus created detrimental effects. Further trial results using the new front end optics created consistent undercutting surfaces, which were measured to be 46° ± 1° when measured to the top surface of the OECB.

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Figure 5.1 **Existing** ***Excimer Laser Front End Set-Up:*** *the excimer beam exits the resonating cavity through a manual attenuator. Beam steering and homogenising mirrors manipulate the beam. The beam is shaped at the mask plane and focussed onto the substrate to machine a two-dimensional image of the mask shape.*

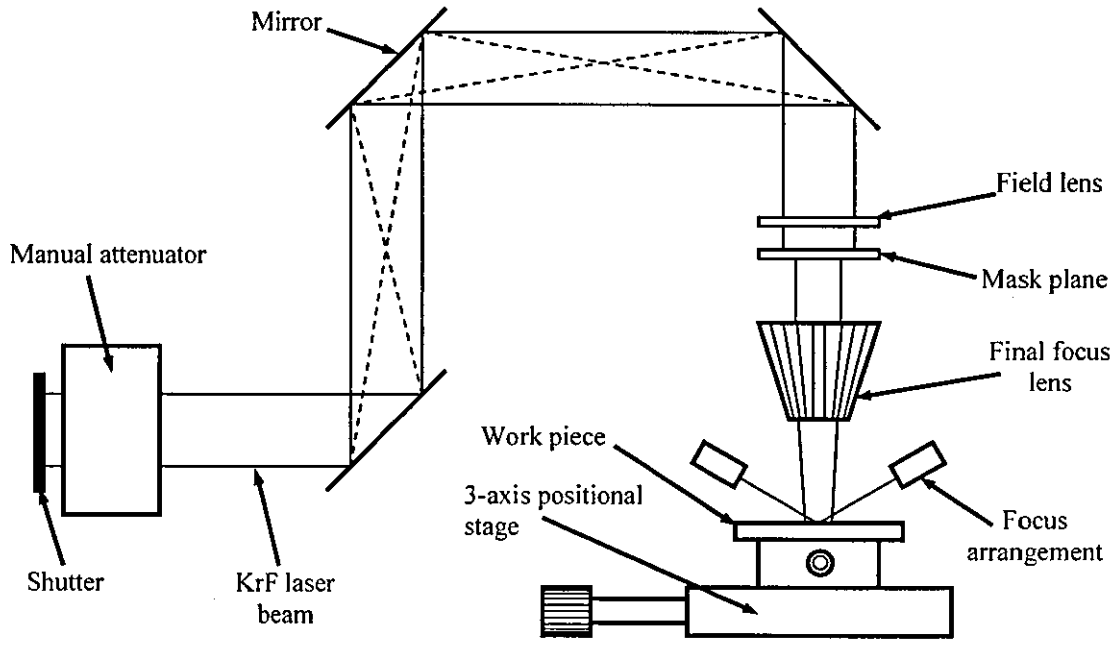


Figure 5.2 ***Initial Trials Jig Design:*** *in order to ablate trial pockets a jig was designed and manufactured with key features including: adjustable mounting fixtures to mount different sizes of samples; focussing table to enable the ablation to occur at the focus point; fixed angle to present the sample at 45° to the excimer beam.*

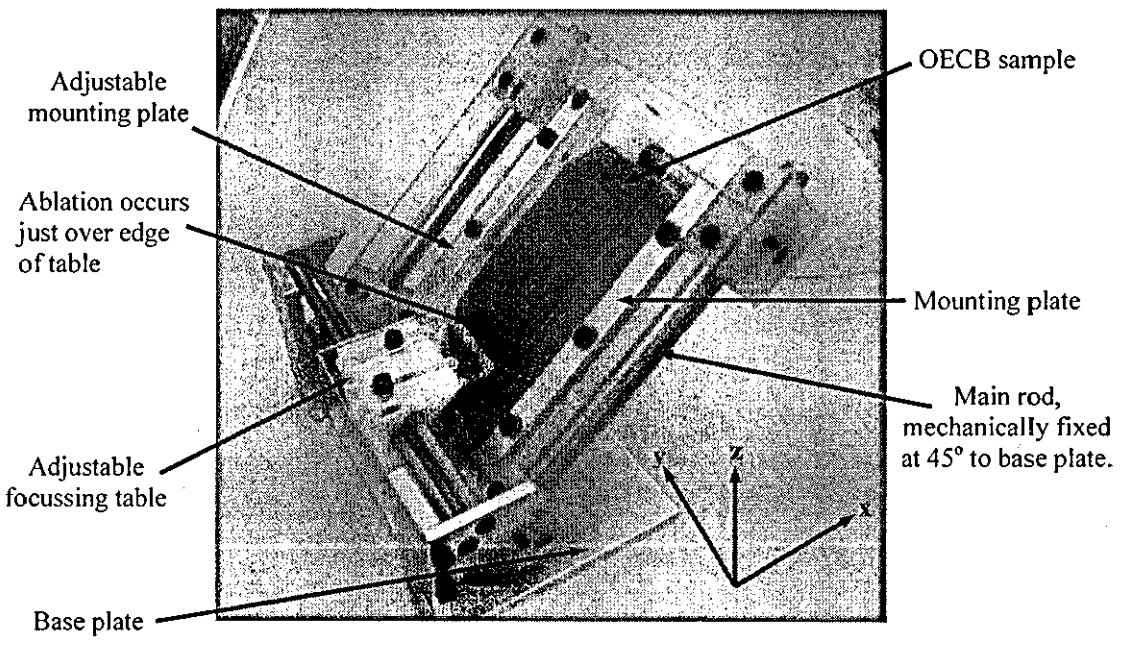


Figure 5.3 ***Initial Trial Results – Undercut Surface:*** *cross-section of a laser ablated pocket demonstrates the ability to create undercutting surfaces.*

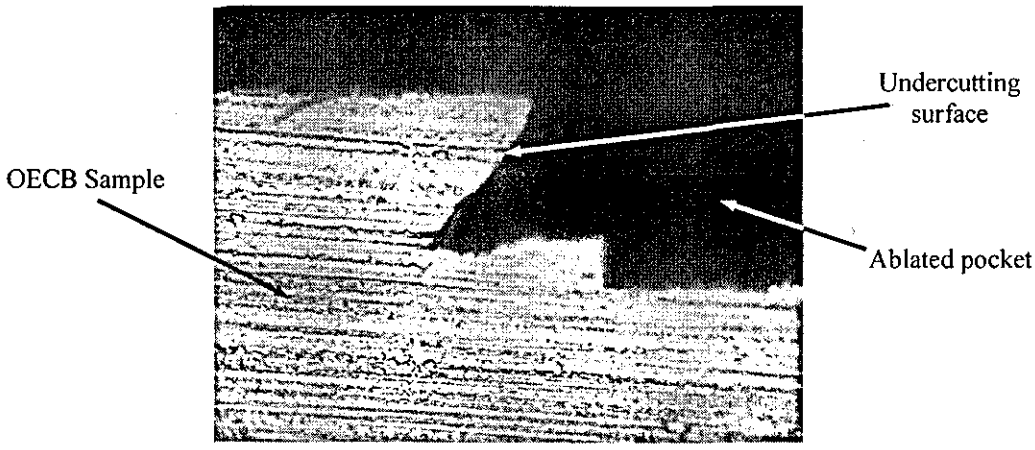


Figure 5.4 ***Initial Trial Results – SEM Analysis:*** *an ablated pocket through the optical layer demonstrates the undercutting surface and illustrates how copper act as a beam stop (right hand side) without which the ablation continues through the FR-4.*

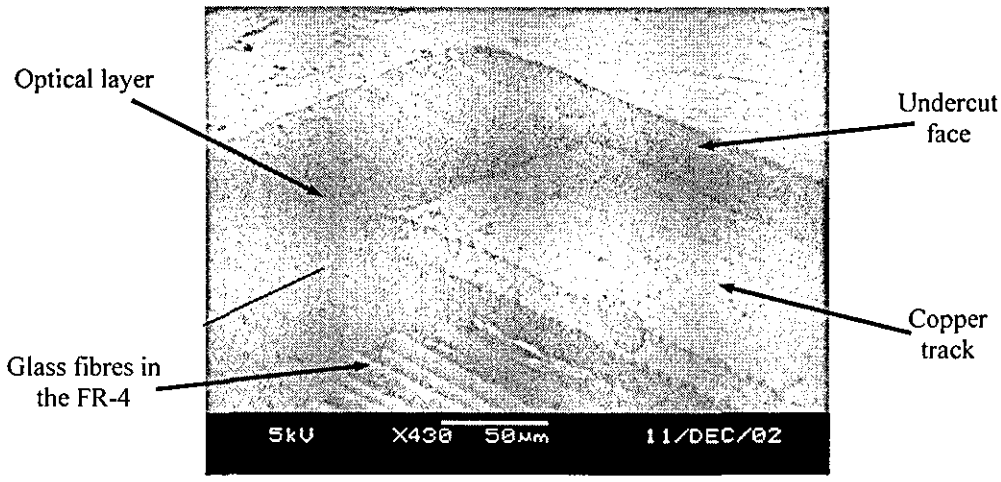


Figure 5.5 ***Initial Trial Results – Striation Marks:*** *the open angled face demonstrates the occurrence of striation marks.*

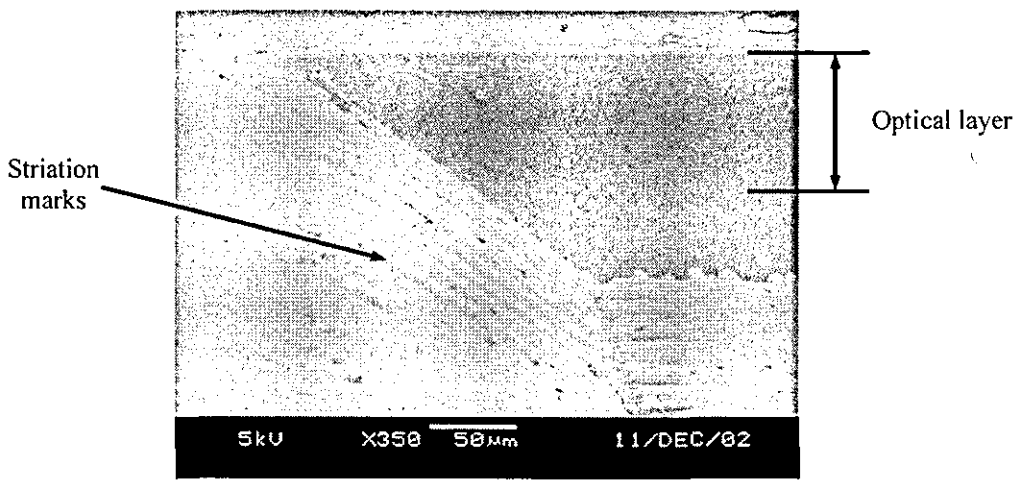


Figure 5.6 ***Experimental Front End – Set-Up:*** *new front end set-up manipulates the light to allow work pieces to sit flat on the positional stages; the design allows vision equipment to be added and focus set using a mechanical gauge probe.*

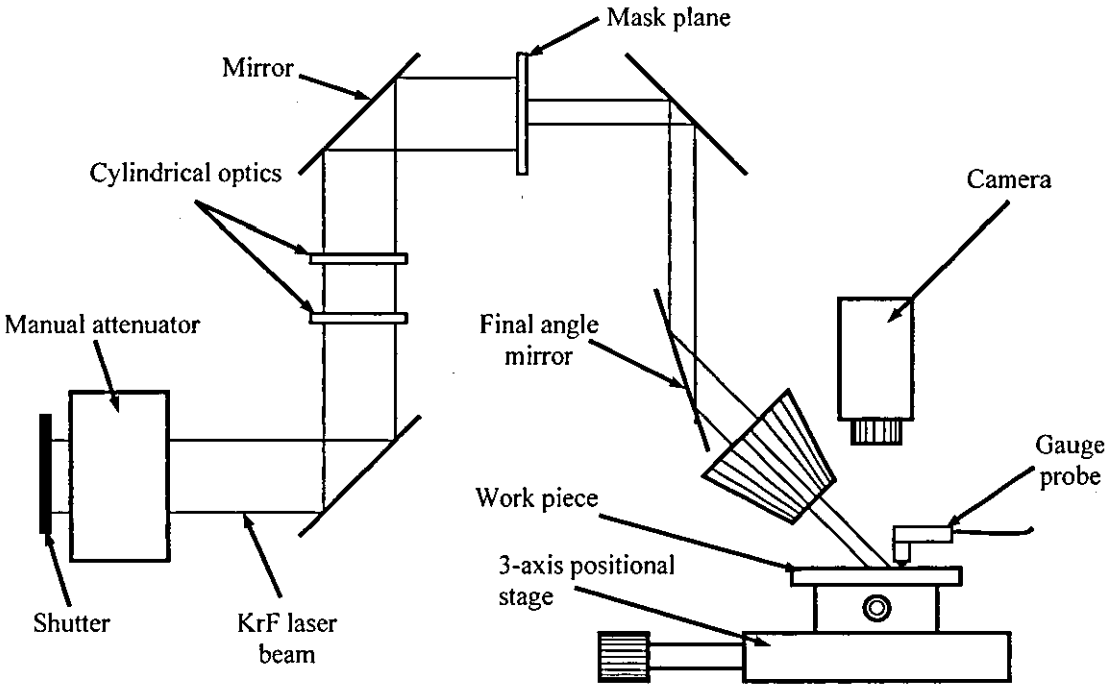


Figure 5.7 ***Experimental Front End – Optical Path:*** *the optical elements are housed within protective coverings and aligned to the aperture of the excimer laser.*

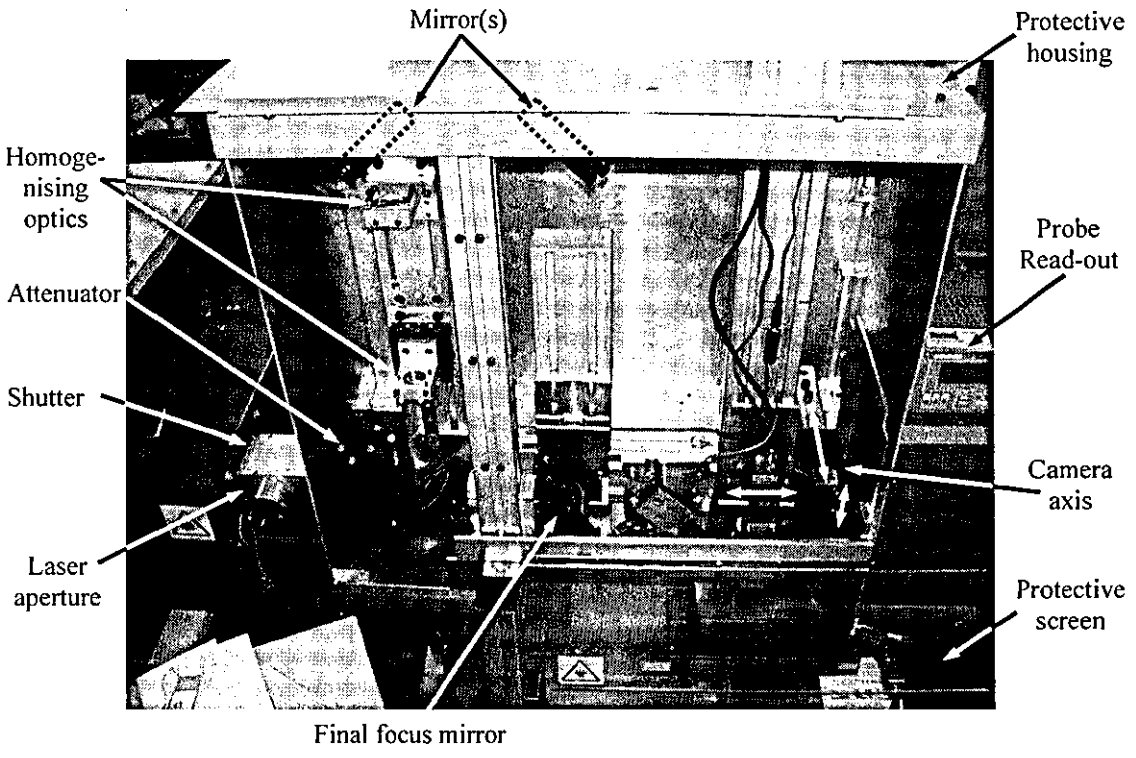


Figure 5.8 ***Experimental Front End – Work Area:*** *the OECB sample is fixed to the plate on the top of the positional stages. The gauge probe is used to position the top surface of the substrate at focus. Vision equipment aligns the substrate to the laser beam.*

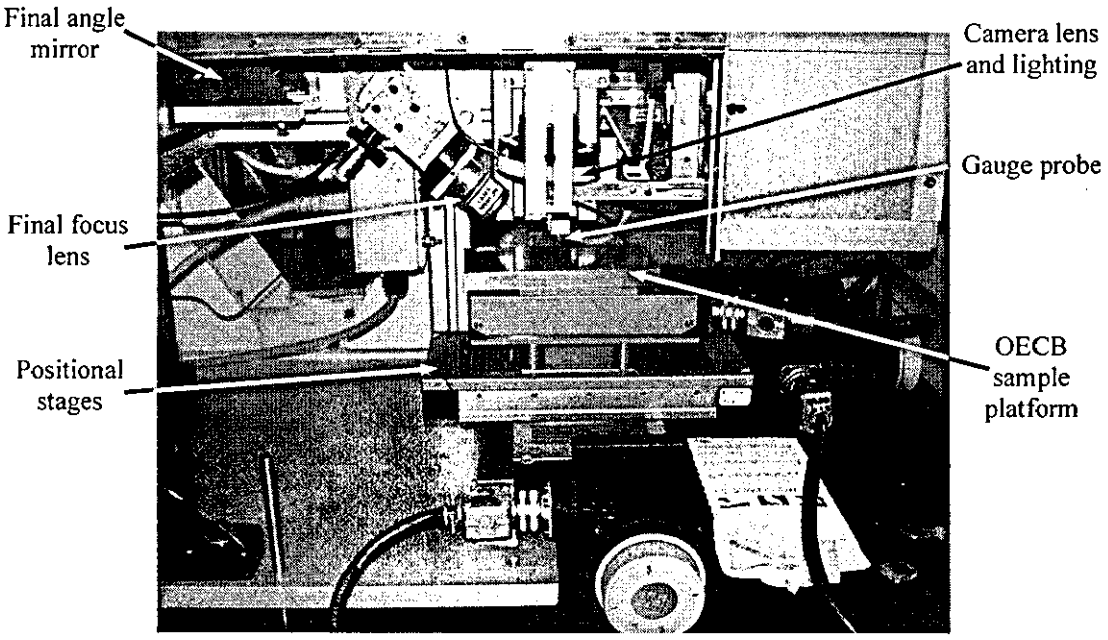


Figure 5.9 ***Mask Orientation:*** *current configuration of the homogenising optics leads to a reduced number of waveguides in the set from being intersected by each integrated mirror.*

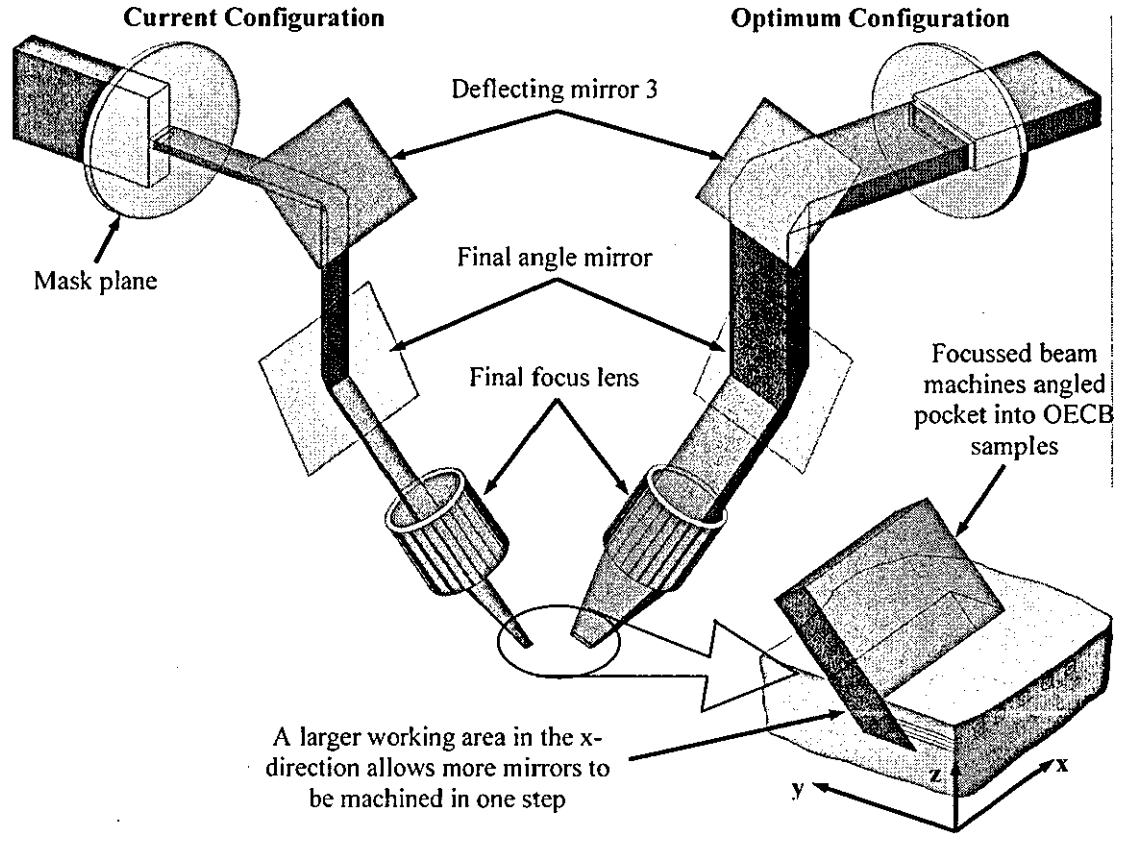


Figure 5.10 ***Mask Design and Manufacture:*** *a) rectangular mask consists of an aperture machined into the brass blank with polished metal shim to create a flat undercutting wall. b) The focus mask consists of three drilled circular apertures.*

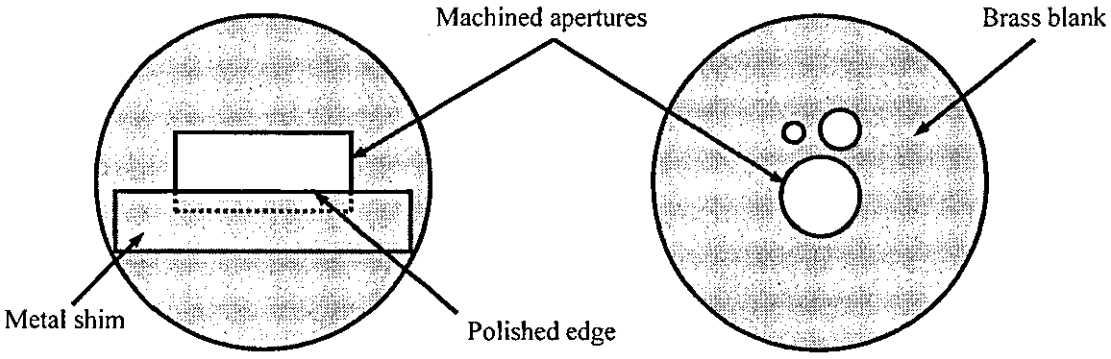
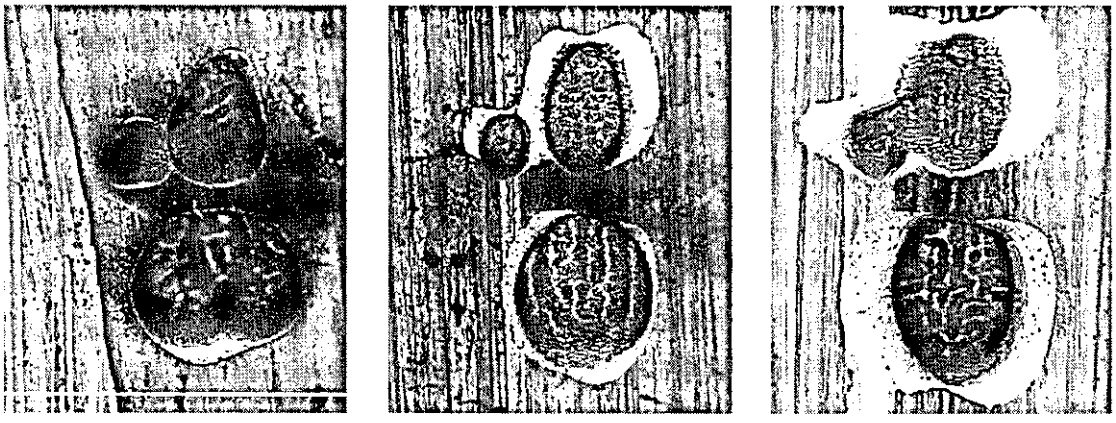
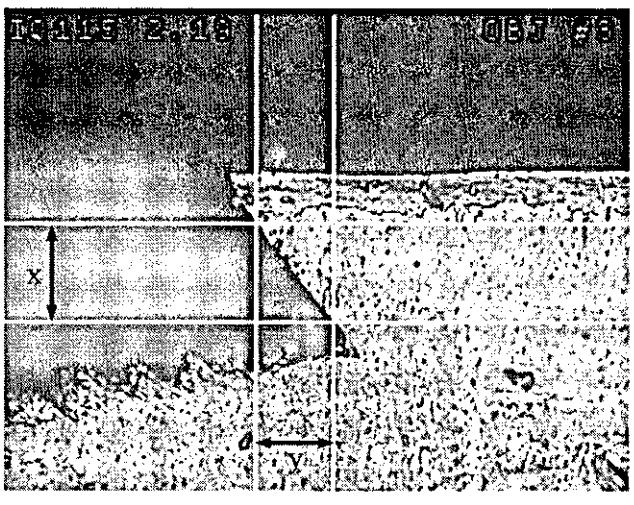


Figure 5.11 ***Focal Point Determination:*** *using the focus mask, ablated film demonstrates the effects of focus. At the focus point the ellipses appear defined. At 250μm above and below focus the ellipses become deformed and begin to merge.*



a) 250μm above focus **b)** Approximate focus **a)** 250μm below focus

Figure 5.12 ***Undercutting Angle Measurement:*** *after setting the tilt of the final mirror, repeated ablations were analysed to measure the undercutting surface angle.*



Measurement /mm x	y	Angle / °
0.071	0.068	46.24
0.044	0.042	46.33
0.051	0.048	46.74
0.08	0.079	45.36
0.055	0.054	45.53
0.051	0.049	46.15
0.073	0.071	45.80
0.088	0.081	47.37
0.064	0.06	46.85
0.065	0.066	44.56
	Mean Angle	46.09

Figure 5.13 ***Tolerance of the Undercutting Angle:*** *a variance of ±5° from the normal, leads to a mode travelling down the centre of the waveguide to vary by over 40μm at a 250μm standoff.*

$\mathbf{a} = 45 \times \tan 40 \approx 37.76\,\mu\text{m}$

$\mathbf{b} = 45 - a \approx 7.24\,\mu\text{m}$

$\mathbf{c} = (45 \times \tan 50) - (a + b) \approx 8.63\,\mu\text{m}$

$+\mathbf{x} = (295 \times \tan 10) - c \approx 43.38\,\mu\text{m}$

$-\mathbf{x} = (295 \times \tan 10) - b \approx 44.76\,\mu\text{m}$

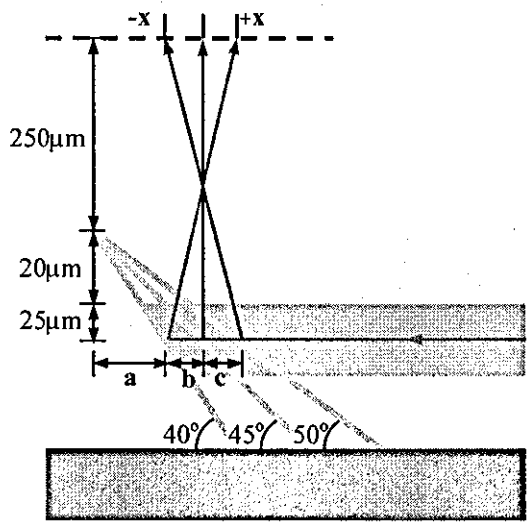
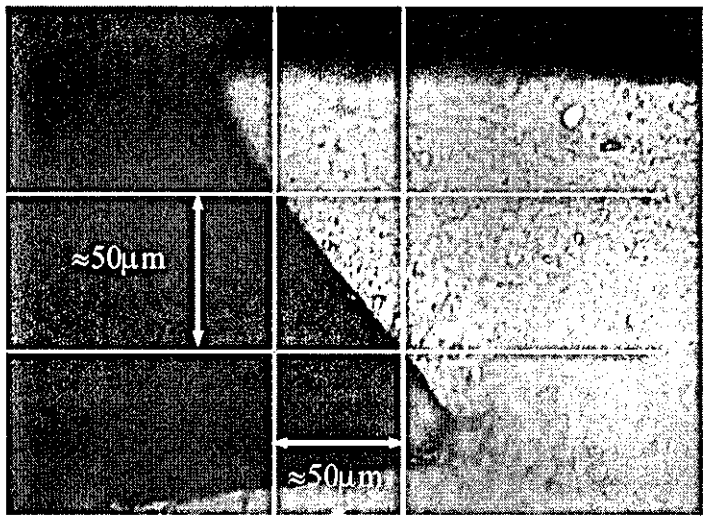


Figure 5.14 ***Ablation Cross-Sections:*** *repeated undercutting surface structures were formed in the demonstrator samples.*



Chapter 6

Electroforming Mirrors

6.0 Introduction

As herein referenced, TIR mirrors are not sufficiently reflective in order to be used in OECB architectures. It is therefore a requirement to establish a PCB compatible production process capable of creating a polymer-metallic interface on the undercutting surface of the ablated pockets (as formed in section 5). As previously discussed, it is not possible to employ conventional thin-metallic deposition processes, such as evaporation, sputtering, and chemical vapour deposition (CVD), due to the geometry of the ablated pockets. The problems with traditional methods arise from accessing the surface that requires coating. However, the characteristics of the pocket enable the metallic-polymer interface to be formed by backfilling the entire pocket. There are various possible methods for backfilling the pocket.

Flowing molten metal into the pocket may fill the pocket. Accordingly, in compatibility with current PCB processes, solder paste could be pasted over the board to fill the pockets and reflowed. The process would not require a mask since the blade could contact directly on the top surface of the OECB with the paste filling the pockets in a similar fashion to how it would traditionally fill the apertures of a stencil. During a reflow process the paste would form as solder on the copper pad at the bottom of the pocket under the action of the flux. The tensions in the solder would naturally force the solder to follow the undercutting surface.

Problems anticipated with this method include voids being formed under the undercutting surface, since the paste may not completely fill the pocket, especially if the relative movement of the blade to the OECB is not synonymous with the direction of the undercutting surface. Further anticipated problems include the probability of poor intimate contact between the undercutting polymer surface and the solder. It is possible that forcing the solder into the pocket during reflow using gasses may solve some of these concerns. However, this is not compatible with current PCB processes.

A variant of back-filling the pockets is to build up the metal deposit from thin layers, rather than attempting to flow the metal into the pocket, and as such it may be easier to avoid the formation of voids. Building up thin layers of metallic deposit may further improve the quality of the metallic-polymer interface at the undercutting surface, since it may be easier to control the abutment of the deposit to the undercutting surface.

The most widely used process within the PCB manufacturing industry of building up a deposit of thin metallic layers is plating. Accordingly, there is herein disclosed a process method comprising a plating process to backfill the ablated pockets.

6.1 Electroplating

Plating metal layers on a surface is termed electroplating and occurs due to the process of electro-deposition. Electro-deposition is the process of producing a surface under the action of an electric current [1]. Electro-deposition is a well-developed science [2-5] and can occur by an electrolytic or an electroless process. The advantage of an electrolytic process, which requires an electric current to be applied to the surface being plated, is that it does not require a masking process. Since the ablated pockets include a copper pad at the bottom, remnant from the laser ablation process, it is relatively straightforward to charge the pad with an electric current; therefore an electrolytic deposition process has been developed for the OECB application.

The electroplating process further comprises connecting the metal surface to be plated to a negative terminal of a DC power supply such that it acts as a negatively charged cathode. The cathode is submerged in a liquid solution called an electrolyte, which forms the plating bath. A positively charged anode comprising the metal to be plated is also submerged in the bath to complete the electric circuit. Positively charged cations in the bath solution are attracted to the negatively charged cathode where electrons flow from the cathode surface to neutralise the ions into metallic form and thereby creating a coating on the cathode. Meanwhile, negatively charged anions within the bath solution are attracted to the anode where electrons dissolve as replenishing ions into the solution.

6.1.1 Surface Preparation

Surface cleaning is a critical process in the success of forming an electrodeposited layer, since organic and non-metallic contaminants or films on the surface interfere with the bonding of the coating to the surface causing poor adhesion and even preventing deposition.

The surface contamination can be extrinsic or intrinsic. Extrinsic contamination comprises organic debris and / or mineral dust from the environment or proceeding process. The preceding process for the OECB application is the laser ablation, which may remove the organic material from the surface (the copper pad). However, it is possible that dust or other extrinsic contaminants may settle on the surface between the two process steps, thus cleaning is still required.

Intrinsic contaminants comprise organic films such as oxides, which form on the surface due to a reaction with environmental gasses and chemicals. Again it is possible that the laser ablation process removes the copper oxide film from the surface; however, the oxide begins to reform as soon as it is exposed to the air again and a cleaning process is therefore required to remove the oxide layer.

Cleaning processes are based on two approaches: physical cleaning, and chemical cleaning. Physical cleaning uses mechanical energy to release both extrinsic and intrinsic contaminants from the metal. This mechanical energy can comprise simply abrasion brushing the surface, or alternatively ultrasonic agitation can be employed for example by using an ultrasonic cleaning bath.

Chemical cleaning comprises removing the contaminants by dissolving or emulsifying them in a cleaning solution. Extrinsic contaminants can be removed with surface-active chemicals, which react with the anticipated contaminants. Intrinsic contaminants are removed with aggressive etching chemicals, such as acids, which often also react with the metal surface.

Once cleaned, the surface is washed and then ready for deposition of the coating. Dependant on the rate at which contaminants reform, the surface is inserted directly into the bath.

6.1.2 Material Deposition

One of the major factors in achieving a reliable electroplated thin layer deposit is the plating bath. The plating bath contains a liquid electrolyte, which is a specially designed chemical solution containing ions of the plating metal, for instance copper, dissolved in a form of sub microscopic metallic particles. The exact composition of the electrolyte is determined further by the characteristics of the desired plating finish and shape of the target object. For example, additives are introduced to obtain smooth and bright deposits.

As mentioned above, the object being plated forms the cathode and is generally placed in the centre of the bath. Banks of the sacrificial anode material are arranged on the outsides of the bath, thereby causing a deposit on both sides of the cathode.

The bath further comprises an agitation means in order to ensure that localised areas of the electrolyte, and in particular areas close to the cathode, do not become depleted of the positively charged ions. An aeration tube blowing air into the base of the bath generally supplies the agitation.

The current and duration of the plating determine the thickness of the electroplated layer on the cathode. The optimum plating potential for each metal is readily known and can be determined by a voltammogram of the current against electrode potential. Plating at voltages too high may lead to parasitic reactions. The thickness of the deposit can therefore be determined by the time the cathode remains in the operating plating bath.

6.2 Initial Electroformed Mirror Trials

In order to assess the ability of the electroplating process to successfully backfill the ablated pockets, initial trials were conducted by ablating a series of angled pockets into a waveguide sample using the initial jig assembly as detailed in section 5.2. The waveguide sample was specially selected to include an area where the polymer was directly coated on top of a large copper layer. Further to the angled pockets, the laser was also used to ablate large, approximately $1mm^2$, areas of polymer located in the corner of the copper area in order to electrically connect it. Although various metals and combination of metal layers can be and are electroplated onto a copper substrate in the PCB fabrication industry, it was chosen to plate copper directly onto the copper pad during the trials due to the availability of the electrolyte.

6.2.1 Process Configuration

Figure 6.1 shows the equipment set-up for the electroplating process. The plating bath comprises a container with an air hose inserted so as the aperture is arranged at the bottom of the container. The electrolytic solution fills the container. The ablated OECB sample is immersed in the plating bath with the Copper pad at the base of the angled pockets connected to be the negative terminal of the PSU. A Copper foil is attached to the positive terminal via a variable attenuator used to control the current.

In order to ensure a good plating adhesion and deposit, surface preparation of the OECB sample is required prior to immersing the sample into the bath. An ultrasonic cleaning bath was used to mechanically remove debris from the pocket such as dust particles. The exposed Copper at the bottom of the pockets was then etched using Ferric Chloride (2 parts deionised water 1 part $FeCl_3$) in order to remove the oxides. The sample was washed with de-ionised water before a wire was soldered onto the Copper pad and at the location of the large opening created by the laser.

The current was set at 5mA, in order to avoid any parasitic reactions. It was not possible to gauge the exact material deposit required, since the sample varied in thickness of the polymer deposit (due to the sample being cut from the edge of the demonstrator) and the exact shape of each pocket on the sample was not consistent

and could not therefore be guaranteed. The samples remained in the bath until the majority of the deposits had reached the top of the pocket, which was approximately ninety minutes. The height of the deposit was verified by viewing the sample under a microscope. Unfortunately, since the pockets on each sample varied in volume, whilst some of the pockets were filled some inherently remained under filled whilst others were overfilled.

6.2.2 Initial Trial Results and Discussion

To ensure the electroplating process is capable of filling the ablated pockets the samples were processed and cross-sectioned using traditional polishing techniques. The cross-section results enable the metal-polymer interface at the undercut surface to be explored to ensure no gaps or voids are created.

The cross-sectioned results were varied. Figure 6.2 shows some of the results. Figure 6.2 A – D clearly shows that the electroplated Copper deposit is capable of forming under the angled surface and in such a way as to follow the undercut. The cross-sections displaying unwanted properties can be split into two categories resulting from: 1, the laser ablation process and 2, the electroplating process.

1. The laser ablation issues include un-ablated polymer at the base of the undercutting surface (shown in figures 6.2 C, E and F), and re-deposited polymer (as shown in Figure 6.2 D). These issues are identified and addressed in section 5.4.2. The unwanted results associated with the electroplating process are limited to over-plating. Over-plating arises from leaving the sample in the bath for to long and results in a mushroom effect of the Copper deposit as it protrudes over the top plane of the pocket.

2. Over-plating is purely an issue of how long the sample remains in the plating bath. The issue arises however, due to a combination of the facts that on each sample the Copper pad at the bottom of the pockets is a common layer of Copper and the initial laser ablation process is not consistent, which creates pockets of varying shapes and volumes. Accordingly, material is deposited in the pockets at varying rates. As the laser process is improved with the implementation of the new front

end, the consistency of the pockets may also be improved, which may therefore also reduce the occurrence of over-plating.

Although the initial results show plenty of evidence of the integrated mirror structures being formed as anticipated; the only true test to prove whether the novel manufacturing process couples sufficient light between the waveguide and fibre, which is arranged at ninety degrees, is to form the structures in a waveguide and analyse the results of transmitted light.

6.3 Further Trials

Analysis of the initial trial results can only give an indication toward the ability of the electroplating process to effectively back-fill the angled pockets. Although few voids between the plated copper and polymer were observed in the cross-sections, the only real indication as to whether effective mirrors have been fabricated is to fabricate the mirror structures transverse a waveguide.

As detailed in Section 4 and according to Figure 4.2. (page 67), the further electroplating trials were conducted using a diced demonstrator substrate. Angled pockets were ablated using the new front end optics, which due to the available mask sizes (as detailed in section 5.4) resulted in each angled pocket intersecting multiple waveguides.

The further trials were conducted by ablating a series of angled pocket transverse the waveguides. Each series was then back-filled using the electroplated copper process. The mirrors were characterised according to Chapter 7. The first series of angled pockets were then diced from the end of the sample and a new series of angled pockets ablated transverse the waveguides and the process repeated. The diced sections were potted and prepared for cross-section analysis using microscopes.

The ablation process was also used to create a large (approximately 1mm x 2mm) pocket in the bottom right corner (when viewed as in Figure 4.2) of each Copper area. The large pocket was used to electrically connect each Copper area during the plating

process. The electrical connection comprises a wire soldered to the exposed Copper at the bottom of the large pocket.

6.3.1. Electroplating Parameters

The electroplating process was similar to that used during the initial results. Again 5mA was used as the plating current and the samples were plated until the deposit reached the top plane of the polymer as viewed visually using a microscope. Over-filling should be limited since fewer pockets are filled simultaneously. The pockets are also a more consistent volume due to the improved ablation process.

6.3.2.Further Trial Results

Optical characterisation of the fabricated integrated mirrors is discussed in Chapter 7. Although each series of the back-filled pockets were cross sectioned and analysed, to maximise the amount of optical characterisation only a thin slice of the samples containing the characterised mirrors were diced between each ablation series. Slicing large areas from the end of each demonstrator would limit the amount of mirrors that can be formed along each waveguide due to the finite areas of Copper. However, in reducing the width of the slice to a minimum, complications arose during the preparation of the cross-sections.

Preparing very small samples for cross-section is complicated due to the handling of the samples. Several samples were lost after being washed away with the cooling solution during the dicing process. The thin samples are also difficult to mount in the potting compound. Conventional mounting clips could not accommodate the small sizes. Mounting the samples on double-sided adhesive tabs enabled the samples to be orientated in the potting cup prior to the potting compound being added; however, the samples were often dislodged as the potting compound was added. The samples were therefore mounted in the potting cup using a clear adhesive. A globule of adhesive was placed on the bottom of the cup and the sample held in position until the adhesive cured. The potting compound was then added and the cross-sections prepared for analysis using conventional polishing methods. It was proposed to cross-section each of the mirrors in order to analyse if a certain defect in the mirrors tallied with

particularly bad optical results; however, the complications in preparing the cross-sections meant that no such correlation was possible.

The lost cross-sections were not critical due to the optical results. However, from the results analysed, it was clear that over-filling still occurred in some pockets whilst not appearing in others. The non-uniform plating of the pockets could be explained by poor bath conditions and monitoring/controlling. Occurrences of over-filling was limited during the further trials by observing the pockets being plated under a microscope after an hour of plating. The pockets were then examined at five minute intervals, and the plating terminated once all the pockets were above the minimum level identified in Figure 6.3.

Since the multimode nature of the light is retained within the core of the waveguide, the minimum filling depth is required to be above the core to ensure the mirror created by the polymer-metal interface reflects the light. The 20μm/50μm/20μm cladding/core/cladding minimum level is approximately 90% of the height of the pockets, although stopping plating once all the pockets were filled to 75% when viewed using a microscope enabled the amount of over-filled pockets to be reduced, over-filling still occurred due to the discrepancies in plating speed between the pockets.

It is anticipated that over-filling would be eliminated in a properly controlled bath, assuming the pocket volumes are consistent.

6.4 Summary

In order to achieve sufficient efficiency, the 45° angled surface, which is used to deflect the light propagating along the waveguide and comprises part of the angled pockets formed by the laser ablation process, is required to have a polymer-metallic interface. Traditional coating techniques are not applicable, instead an option is to back-fill the entire pocket. There are various options available, although the most attractive is to back-fill the pocket by building up a deposit of thinly plated layers through electrodeposition.

Electroplating is a well-developed science and is widely used in the PCB fabrication process for creating copper artwork. Initial trials using OECB samples with ablated sites showed that the process is suitable for back-filling the pockets. A critical factor of the process is the surface preparation of the material to be plated; accordingly the samples were prepared using a micro-etch and ultrasonic cleaning bath. The main issue with the process is controlling the depth of fill. Over-plating results in a 'mushroom' effect on the top of the OECB substrate that may block the light transmission from the mirror.

Ablated pockets formed orthogonal to waveguides in the OECB demonstrators were backfilled by electroplating copper in order to optically characterise the mirrors.

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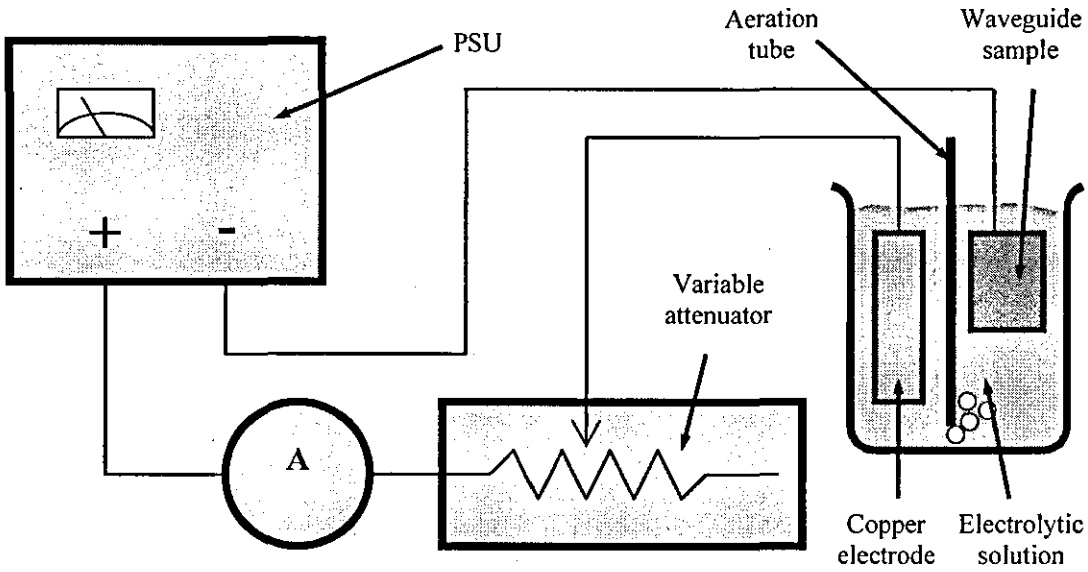
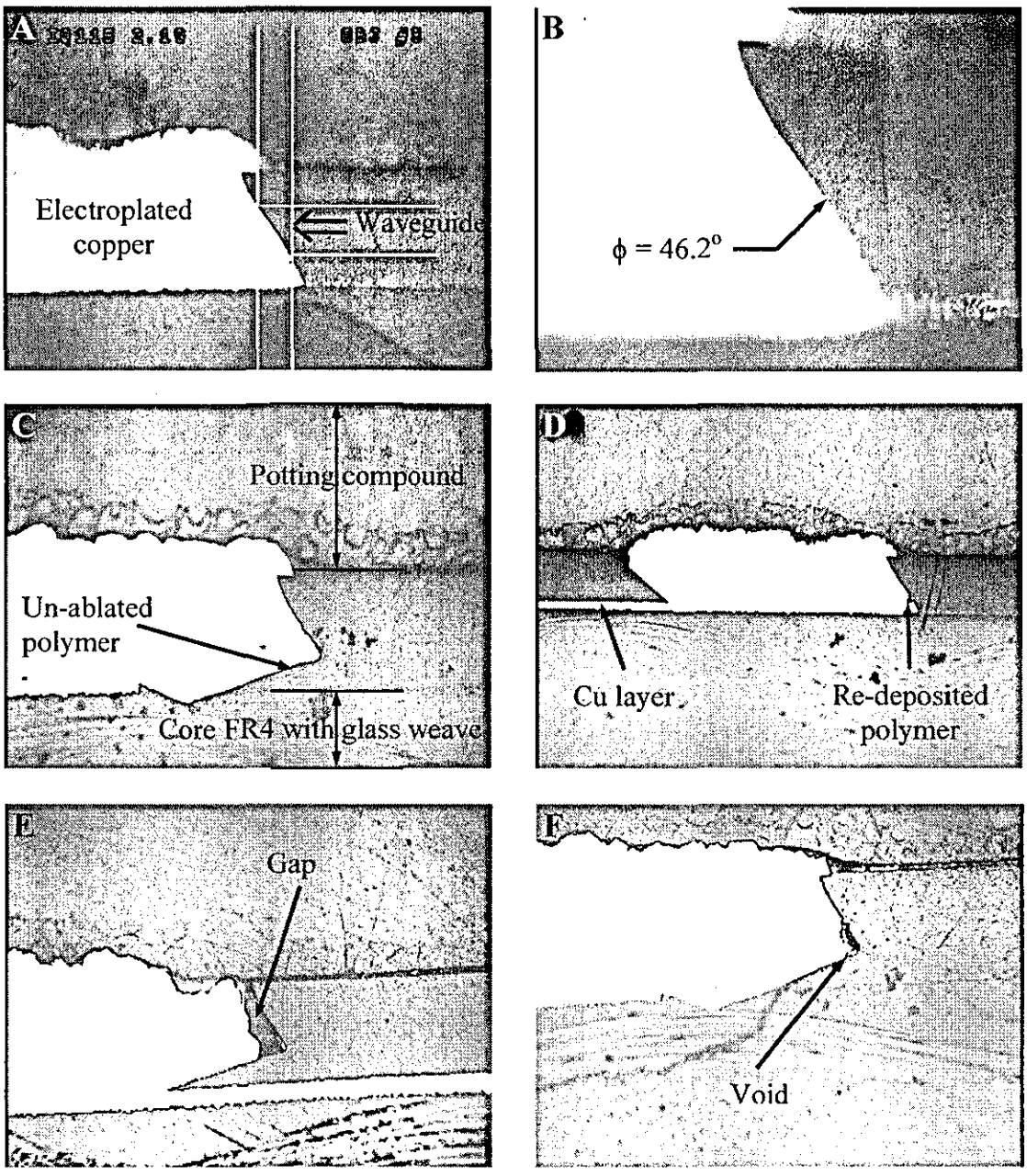
2. SCHLESINGER M. and PAUNOVIC, M. *Modern electroplating*. 4th ed. New York: Wiley; 2000.
3. DINI, J.W. *Electrodeposition: the materials science of coatings and substrates.* Noyes Publications; 1993.
4. TODD, R.H., ALLEN, D.K. and ALTING, L. *Manufacturing processes reference guide*. Industrial Press Inc.; 1994.
5. HOUSE, J.R. *Surface preparation and electroplating*. [Accessed on 14 Dec. 2004]. Available at: www.secfinishes.co.uk/articles/Article_Electroplating.htm.

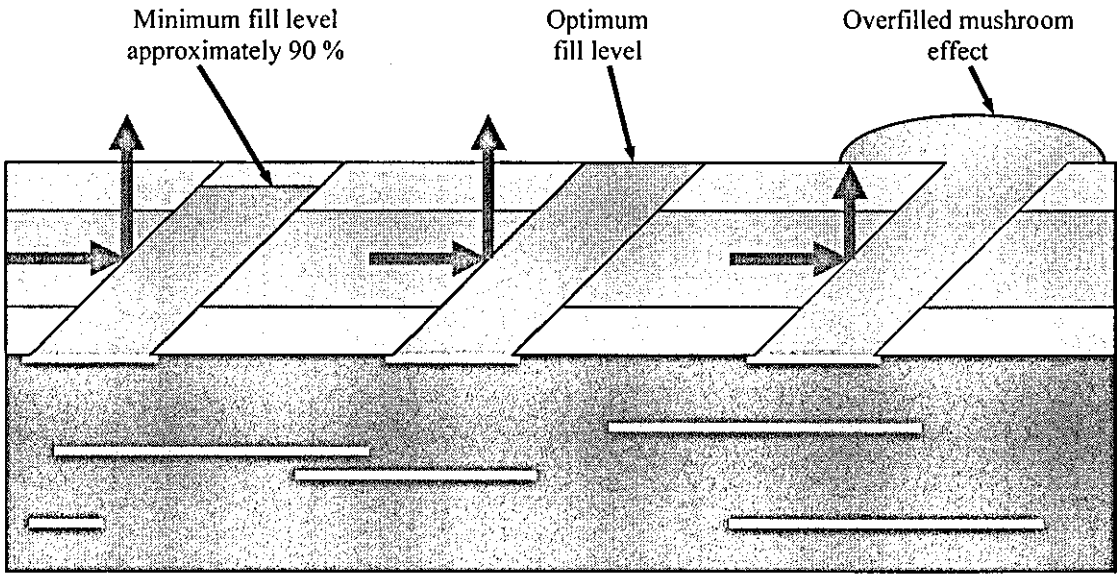
6.1 ***Electroplating Process Set-up:*** *the angled pockets were back-filled with copper using an electroplating process. As shown below the copper pad at the bottom of the angled pocket is connected to a PSU and immersed in a plating bath along with a copper anode.*



6.2 ***Electroplating Cross-section Results:*** *analysis of cross-sections through back-filled pockets. A & B) Cross-section images through a successfully back-filled pocket. Average measured angle is 46.2°. C & D) Examples of poor ablating with C showing a covering of waveguide material at the base of the undercut mirror, and D, a small portion of material which may have reformed after ablation. E & F) Examples of poor electroplating with E showing the copper not actually interfacing with the undercut polymer facet and F showing the presence of a void, although both cases are possibly due to the poor ablation of the pocket.*



6.3 ***Optimum Electroplating Fill Level:*** *the optical signal is maintained mainly within the core and immediately surrounding cladding. The pockets only therefore need to be filled to 90% of the depth of the pocket. Overfilling risks blocking the lights path to the surface of the OECB and also increases the risks of problems when butt coupling fibre to the OECB's surface.*



Chapter 7

Mirror Characterisation

7.0 Introduction

The characterisation of the integrated mirror structures involves measuring the coupling loss of the mirrors. In optical communications, coupling efficiency is measured as loss. Since the behaviour of optical structures can be wavelength dependent, i.e. they can generate different loss characteristics at varying wavelengths. It is therefore important that the optical efficiency of the mirrors is measured at the wavelength of the communication signal in the architecture that the structures are to be used. The integrated mirrors are formed in multimode waveguides for use in datacom architectures and will therefore predominantly transmit light at 850μm. The coupling loss of the mirrors can therefore be determined by detecting the transmission of light from a stable 850μm light source, which travels down the waveguide and is reflected by the mirror structures.

The detection unit could comprise a bare PD die assembled to a circuit board, which would be used to simulate a PD being assembled to the OECB according to one of the architectures identified in Figure 3.4. The active region of the PD being on the top side and being arranged off-set from the top of the OECB. The off-set corresponding to approximately 30μm, which is the height of a stud bump. However; such an architecture is prone to electrical losses due to, for example, the circuitry and assembly of the PD to the circuit board. It is also preferable to directly measure the optical signal, so characteristics other than power could be measured if required, rather than converting the signal back into an electrical form and monitoring that.

Accordingly, a better measurement is achieved by basing the measurement on a butt-coupled fibre architecture, which aligns a 50/125μm multimode fibre to the integrated mirror structure. The coupled light can then be measured by high-quality receivers and other optical characterisation equipment.

The power measured by the receivers could be directly compared to the power output of the transmitter. Although an uncomplicated measurement, the problem with this technique is that the coupling loss takes in to account the attenuation of the system, which results, for example, from waveguide-fibre coupling and transmission along the waveguide rather than purely attributed to the mirror.

In order to be certain of measuring only the loss generated by the mirror, it is necessary to take a reference, which isolates the loss of the mirror from the rest of the system. Such a measurement is termed Insertion Loss (IL) and is expressed in dBm as 10 x log10 P_1/P_0 where P_0 is the reference measurement in mW and P_1 is the measurement of coupled light subsequent to the fabrication of the integrated mirror.

IL is the predominant characteristic of the integrated mirror structures. However, if the 3dB yard-stick is matched or bettered, the measurement of further optical characteristics will be required. For example the mirrors will need to produce a bit rate error comparable to current datacom standards, and the alignment tolerances of fibres and active devices will need to be determined. The requirements of these further measurements were kept in mind whilst designing the mirror characterisation equipment and process detailed herein.

7.1. Experimental Mirror Characterisation Process

The mirror IL measurement is a two-step process as depicted by Figure 4.3 (page 67). The first step is to isolate the system attenuation from the measurement, which is done by taking a reference measurement. The reference measurement comprises butt-coupling fibre to either end of the straight waveguide sample. After taking the reference, an integrated mirror is formed in the respective waveguide and as near to the end as possible. The second step of the measurement process is to then replace the sample on the measuring equipment and re-align the butt-coupled fibre at the detection end, to the surface of the OECB. The IL is calculated by comparing the two measurements.

7.1.1. Process Equipment

An experimental test equipment platform was designed and commissioned in order to optically test the integrated mirrors. The test equipment was modelled on the requirements identified above. A Melles Griot optical table was used as the basis for the equipment. The optical table ensured that the optical measurements were isolated from vibrations, which could interfere with the results. All the process equipment was therefore required to be mounted on the optical table.

The test equipment comprises: alignment stages, vision equipment, and optical equipment. The specific requirement and design of each of these areas are identified below. The overall test platform is shown in Figure 7.1.

7.1.2. Alignment Stages

Two Melles Griot 3-axis positioning tables were assembled to the optical table. Nano positioning was available on one of the stages, which was positioned to the right of the test set up. The Nano positioning enabled table was mounted to a long axis stage to enable the 3-axis table to be moved easily across the width of the platform. This was necessary in order to reposition the stage as the demonstrator samples became shorter. The samples varying lengths are attributed to the mirrors being cleaved from the ends after each set of trials.

Each of the alignment stages required an attachment to hold fibre fast to the stages. The fibres are required to be cleaved in order to give a flat, clean termination to the fibre. Jagged fibre cleaves generate losses. The cleaving process comprises stripping the first and secondary cladding from the fibre. This is best done using a heated stripper as hand stripping the fibres can generate micro cracking in the fibre which leads to failure in use. After the fibres have been stripped Isopropyl Alcohol (IPA) is used to clean debris from the fibres cladding. The fibre is loaded in to the heat stripper using v-groove fibre holders. The holders are capable of being loaded directly into the cleaver without the need to re-load the fibres.

The cleaver uses an ultrasonic blade to initiate a crack in the fibre. The fibre is loaded in tension so that the crack propagates through the fibre as a clean cleave. Once the fibre has been cleaved any contact with the end could result in scratching, which produces high losses from the fibre end. Using the same fibre holder to mount the fibre on the alignment stages reduces the possibility of damaging the cleaved fibre end. The alignment stages were therefore fitted with attachments for fibre V-groove holders. The attachment comprises two precisely located dowels, which locate on the holders and secures the fibre fast to the alignment stages.

The alignment stages are arranged either side of a central platform. The design of the centre platform enables the OECB demonstrator samples to be orientated in both a horizontal and vertical position. This is achieved by mounting the OECB demonstrator to a bracket. Clips comprising metal shim trap the OECB demonstrator samples to the bracket. In the horizontal orientation of the OECB sample, the bracket is slide-able and assembled to the central mount on a vertical edge. The slide-able mounting enables the height of the OECB sample to be easily selected. In the vertical orientation of the OECB a second face of the bracket is slide-able and mounted on the top of the central mount. The slide-able mounting enables the OECB sample to be easily re-positioned with respect to the alignment stages.

In use, the alignment stages can be used to move the cleaved end of the fibres in x, y and z orientations relative to the OECB, which is held in a fixed position. The fibres can be aligned to the waveguides by finding first light: first light being defined as the initial transmission of light along the fibre. First light is found manually. The nano track feature of the Melles Griot positioning tables are used to run a logical search pattern to locate the optimum alignment position.

In order to find first light, it is necessary to include vision equipment, in order to visually determine the point at which first light is found.

7.1.3. Vision Equipment

Vision equipment is used to find first light of the coupling and also to ensure the offset of the fibre and demonstrator remains and that the cleaved fibre end does not

make contact with the demonstrator. Four cameras are used. Two are positioned at either end of the samples to view the ends of the demonstrator when in the horizontal position. These cameras check that first light is found. Although 850nm light is not detectable by the human eye, Charge Coupled Device (CCD) cameras can often view light well into the infra red spectrum and so display the 850nm signal as white. The first alignment stage can therefore be manoeuvred until first light is detected by the opposite camera. First light is easy to determine as an illuminated square at the end of the demonstrator.

Top and side cameras ensure that the second fibre is coupling to the correct waveguide. The top and side cameras are mounted onto a sliding bracket that enables them to be moved linearly, this allows for viewing of the coupling process at either end of the demonstrator.

7.1.4. Optical Equipment

IL measurement requires two pieces of optical equipment; a transmitter and a receiver. Due to the processing time required to manufacture the integrated mirrors, the time lapse in between the reference measurement and the second measurement is considerable (6-8 hours). This requires highly stable measuring equipment to ensure that the optical power and sensitivity of the receiver does not wander between reference and measurement.

Accordingly a highly stable Tempo platform with an 850nm VCSEL transmitter module and a PD receiver module was procured. The modules output was measured on an Optical Spectrum Analyser (OSA) and comprised a centre wavelength of 850.29nm (Figure 7.2). Aligning a fibre to either end of a waveguide of the OECB demonstrator and tracking the power level over a period of time measured the sensitivity of the system. A sensitivity of ± 0.1 dB was achieved as shown in Figure 7.3. Mode filters comprising three or four 2cm loops of fibre after connectors and sources ensured the stability was increased by eliminating spurious sources of light from propagating in the cladding material rather than the core.

7.1.5. Characterisation Process

The test equipment was used to take the reference measurement as described below:

- Prepare first fibre
  - Connectorise first end of first fibre by splicing on a patch cord (PC).
  - Load second end of first fibre into V-groove.
  - Strip fibre in heat stripper.
  - Clean fibre with IPA.
  - Load V-groove holder into cleaver and cleave end.
  - Load V-groove holder onto right hand side alignment stage.

- Prepare demonstrator
  - Dice ends off demonstrator.
  - Load horizontally on to central platform.
  - Raise central platform to approximate height of first fibre.

- Find first light
  - Plug the connectorised end of the first fibre into the transmitter (TX).
  - Use right hand side alignment stages and vision equipment to find first light.

- Prepare second fibre
  - Connectorise first end of second fibre using Bare Fibre Adaptor (BFA).
  - Strip and cleave second end of the second fibre.
  - Load second fibre onto left hand side alignment stage.
  - Plug the BFA connectorised end of the second fibre into receiver.

- Align second fibre
  - Use the left hand side alignment stage to manually align the second fibre with the first waveguide.
  - Upon achieving a transmitted signal, manually optimise the first fibre position using right hand side alignment stages.

- Run nano track on left hand side alignment stages in order to optimise the second fibres alignment with the waveguide.
- Fix the second fibre to waveguide (see section 7.2.).

- Take reference reading (see Figure 7.4)
  - Remove OECB from platform and replace in the horizontal position but with the first fibre now loaded on the left hand side stage.
  - Align the first fibre with the waveguide.
  - Use nano track to optimise alignment of first fibre.
  - Take reference reading. To increase the measurement accuracy, repeat the measurement three times and in-between each measurement remove the second fibre from the BFA and re-connectorise.

With the reference recorded the first fibre can be moved away from the OECB demonstrator sample allowing it to be removed from the central platform. The integrated mirrors can then be placed on the free end of the OECB sample and the sample returned to the first platform but this time in the vertical orientations. The top of the OECB facing the left hand side alignment stages. The efficiency measurement is taken as described below:

- Load the OECB sample
  - Load the OECB sample vertically on the central platform.
  - Re-connect the BFA connectorised end of the second fibre into the transmitter.

- Re-align the fibre
  - Re-align the first fibre to the top of the OECB.
  - Once light is transmitted into the first fibre optimise the alignment using nano track.
  - Take a measurement. Again repeat three times for accuracy.

The IL can be expressed in dB by fitting the reference measurement (P_o) and efficiency measurement (P_1) into the following equation $10 \times \text{Log}10\ P_1/P_o$.

7.2. OECB Demonstrator Preparation

In order to ensure that the coupling loss of the second fibre remains constant, the fibre is required to be glued permanently to the demonstrator end. Various optical adhesives are available for such a purpose. Ablestick, a global producer of adhesives for the electronics industry [1], produce various optical adhesives that exhibit low loss characteristics at the 800nm, datacom wavelength. These include A4043T, A4083T, OGFRI 146T, and A4035T. The adhesives were designed for a primary UV curing exposure to spot cure components in position, followed by a secondary thermal cure. A DSC analysis of the adhesives, Appendix B, shows that they will all cure completely via thermal initiators (120 – 125 °C for 17 – 20 minutes). However, some of the parts of the OECB assembly are not rated above temperatures of 80°C, namely the connectors. Accordingly, after consultation with Ablestick, OGFRI 146T was selected as it completely cures via UV exposure.

7.2.1. Initial Preparation Problems

Although a single fibre could successfully be aligned and glued using the adhesive. In doing so, the adhesive spread along the edge of the OECB demonstrator, which inhibits further fibres from being attached to the end of the demonstrator. In order to get sufficient results several fibres were required on each demonstrator. It was attempted to align multiple fibres at the same time by first gluing fibres into a silicone v-groove capable of holding twelve fibres pitched at 250nm – the same pitch as the waveguides. However, the manual process could not consistently get the fibres in the centre of the v-grooves and even when successful with the majority, the alignment stages require rotation about the fibres axis in order to ensure all the fibres are optically aligned.

7.2.2. Demonstrator Preparation Using Comb Structures

In order to align multiple fibres to the end of each demonstrator, a jig was manufactured. The jig comprises a base and an end angled at 90° to the base, both of which are made out of plastic. The angled end includes slots machined into it, to form a comb structure. The slots are machined into the plastic using a wafer saw. The saw

parameters of feed rate and speed were set using trial and error to get gaps approximately 150μm wide and comb structures of approximately 350μm wide. This enables at least half of the waveguides to be utilised as a waveguide is guaranteed to be positioned within the gap of each comb. The average structure widths are shown in Table 7.1 (page 110).

The demonstrator was secured to the jig by first aligning and gluing a single fibre to a first waveguide. The OECB sample was then replaced on the test equipment with the jig. The demonstrator was placed on the top of the jig with the free end spaced off-set from the comb structure. The off-set being approximately 250μm as viewed in the vision equipment. A visible light source was transmitted into the fibre and the demonstrator moved manually relative to the jig in order to ensure the waveguide is in the centre of a comb as viewed using the vision equipment. Once in place the demonstrator is screwed in place relative to the jig using adhesive.

The demonstrator is removed from the test platform and the fibre removed from the end. The sample, including the jig, is diced and replaced in the test platform. Fibres are aligned to the demonstrator by inserting the fibre through the comb structure. Once aligned adhesive can be applied in between the respective comb without the adhesive spreading between combs. The adhesive is added by wicking the adhesive down a needle positioned above the correct comb. The v-groove holder needs to be positioned relatively close to the comb structure to stop the fibre bending due to the tension within the adhesive. Whilst holding the fibre in position the adhesive can be optically cured by a UV lamp. No adhesive is applied to the end of the OECB so that it does not spread along its edge preventing subsequent fibre alignment.

Once a fibre is cured in place, subsequent fibres are aligned to the remaining waveguides and again through the comb structures. When all the possible waveguides are aligned with fibres, adhesives can be applied to the demonstrator end so that the gap between the end of the fibres and the demonstrator is filled with adhesive. Thus eliminating free space transmission and the risk of loss from contaminants (i.e. dust) getting between the fibre and the waveguide. A completed demonstrator with attached comb structure and fibres is shown in Figure 7.5.

Table 7.1 ***Average Comb Structure Measurements:*** *dimensions of the comb structures measured after fabrication using a wafer saw.*

Gap No.	Gap width / μm	Comb width / μm	Gap No.	Gap width / μm	Comb width / μm	Gap No.	Gap width / μm	Comb width / μm	Gap No.	Gap width / μm	Comb width / μm
1	358		7	379		13	341		19	371	
		121			116			127			153
2	362		8	368		14	377		20	377	
		116			155			145			114
3	372		9	371		15	366		21	364	
		114			126			110			152
4	360		10	373		16	357		22	349	
		108			112			142			
5	374		11	374		17	345		MAX	380	155
		129			119			110	MIN	341	110
6	380		12	375		18	379		Mean	367	126
		114			121			107			

7.2.3 Discussion of Preparation process

The comb structures would not be needed if fibre ribbons were provided with v-groove silicon blocks on one end and connectors on the other end. However, these are expensive and require a further rotation axis on the test equipment. In the absence of this equipment, the comb structures enable multiple fibres to be individually aligned and glued to the OECB. In practice however, operator error lead to adhesive occasionally wicking into adjacent combs: such wicking leads to a reduced number of waveguides being aligned to the demonstrators. Further complications occurred due to adhesive also wicking along the fibres. When cured this created a brittle section of fibre that was not supported by anything. The fibres thus becoming fragile and prone to breaking especially during transportation.

Handling the final demonstrator with attached fibres is also complicated due to the likelihood of the fibres becoming entangled and snagged on the equipment – the reason why it is so desirable to remove fibre from the manufacturing environment.

7.3 Mirror Characterisation Results

Using the OECB demonstrator substrates that were ablated and backfilled according to Chapters 5 and 6 respectively, the optical characterisation equipment and process described herein enabled IL to be measured. Table 7.2 (page 111) shows the IL characteristics of the integrated mirrors. An average IL of -9.17 dB was recorded. It should be noted however, that pockets that were overfilled such that no real light could be coupled were not characterised and were instead replaced by a repeated pocket immediately prior to the overfilled pocket.

Table 7.2 ***IL Measurements for One-Dimensional Mirrors:*** *integrated mirrors fabricated according to Chapters 5 and 6 were characterised using the process and equipment described in Chapter 7. The results show an average IL of -9.17 dB.*

No.		Power level / μW 1	2	3	Average / mW	Loss / dB	No.		Power level / μW 1	2	3	Average / mW	Loss / dB
3a1	P_0	74.13	86.82	90.64	83.86	-9.03	1b1	P_0	1.93	1.52	2.66	2.04	NA
	P_1	11.109	9.933	10.43	10.49			P_1	Broken Fibre			NA	
3b1	P_0	43.89	43.27	42.75	43.30	-8.79	1c1	P_0	9.21	10.27	9.2	9.56	-8.32
	P_1	5.86	5.712	5.6	5.72			P_1	1.74	1.4	1.081	1.41	
2a1	P_0	38.21	43.33	46.06	42.53	-7.66	1d1	P_0	30.08	30.16	27.78	29.34	-9.92
	P_1	7.224	7.415	7.221	7.29			P_1	3.12	2.97	2.87	2.99	
2b1	P_0	27.88	28.22	29.19	28.43	NA	1e1	P_0	46.22	44.82	47.94	46.33	-9.53
	P_1	Broken Fibre			NA			P_1	4.98	5.5	5.01	5.16	
2c1	P_0	72.6	73.6	76.8	74.33	NA	1f1	P_0	23.57	27.12	27.36	26.02	NA
	P_1	Broken Fibre			NA			P_1	Broken Fibre			NA	
2d1	P_0	71.4	72.35	75.09	72.95	NA						Max	-10.91
	P_1	Broken Fibre			NA							Min	-7.66
2e1	P_0	39.31	39.04	39.21	39.19	-10.91						**Average**	**-9.17**
	P_1	3.017	3.102	3.422	3.18								
1a1	P_0	11.73	11.65	11.41	11.60	NA							
	P_1	Broken Fibre			NA								

The mirrors were also analysed using a microscope. The reflected light from a visual fault finding laser diode module, which was connected to the end of the fibre attached to the waveguide, was viewed and the spot size measured. The spot size was measured by focussing on the top of the OECB and recording the spot size between cross-hairs. Figure 7.6 shows typical results. The results recorded a spot size of around 190μm.

7.3.1 Discussion of Results

The IL results proved that the experimental test set-up and process were capable of characterising the integrated mirrors. The process could be improved through the use of ribbon fibre and a further rotation axis, as this would eliminate the need for the comb structures. The fragility of the fibres also proved an issue. Even in controlled research conditions a large proportion of the fibres broke during handling of the demonstrator. Furthermore most of the fibres broke within a few centimetres of the OECB, which meant fibre could not be spliced on to the fibre terminations and therefore light could not be coupled into the respective waveguide. The fibre issues all reinforce the urgency in finding a solution to remove fibre from the manufacturing process.

The characterisation process could be further improved by permanently splicing patch cords to the ends of the fibre – it was not possible during the trials due to resources –

as this would reduce the uncertainty of the results. Said uncertainty emanates from discrepancies in the quality of the BFA connectorisation of the fibre between reference and reading.

An insertion loss of -9dB is a third of the power required to reach the 3dB benchmark, which in itself is optimistic as the mirrors will eventually require much lower losses. Consequently the excessive IL results for the mirrors are not suitable even for datacom applications. Whilst it is inevitable that the IL may be reduced through optimisation of the process parameters, the spot size will not dramatically change. Although VCSEL transmitters tend to overfill the fibres, the mode filters that are used to strip the cladding modes to increase the stability of the set-up also act to normalise the modes so that the power is more evenly spread through the core. Thus if the power distribution became equal across the waveguide core the 50μm core of a fibre would only be capable of coupling approximately a third of the light in the spot size of 190μm. Such simplicity would imply that by simply coupling all of the reflected light, the 3dB benchmark may already be breached.

7.3.2 Recommended Further trials

With many ablation sites still remaining on the prepared demonstrators, further trials need to be conducted into methods of coupling more of the reflected light into the butt-coupled fibre. Chapter 8 details the further research conducted.

7.4 Summary

An experimental test set-up was used to characterise the integrated mirrors. IL was measured for the mirrors fabricated according to Chapters 5 and 6. The results showed an IL of 9.17 dB and a spot size of 190μm. The IL is excessive and can be mainly attributed to the large spot size. The IL results could therefore be improved simply by coupling more of the reflected light into the fibre.

Recommend improvements to the characterisation process include: 1, adding an additional rotation axis to the alignment stages so that ribbon fibre may be aligned to the waveguides rather than individual fibre and thus eliminating the need for the comb

structures; 2, connectorising the fibres with patch cords rather than BFAs, in order to reduce the error uncertainty.

Further trials are required to asses the options for coupling increased amounts of light into the butt-coupled fibre.

References

1. Ablestick [home page on the internet]. [Accessed 15 Jan 2005]. Available at: www.ablestick.com.

Figures

Figure 7.1 ***Experimental, Optical Characterisation Equipment:*** *the centre mounting enables the OECB substrate to be mounted either horizontally or vertically. The optical table with nano-track capability is shown preparing to align a fibre to the OECBs surface. Vision equipment is also essential to enable first light to be found.*

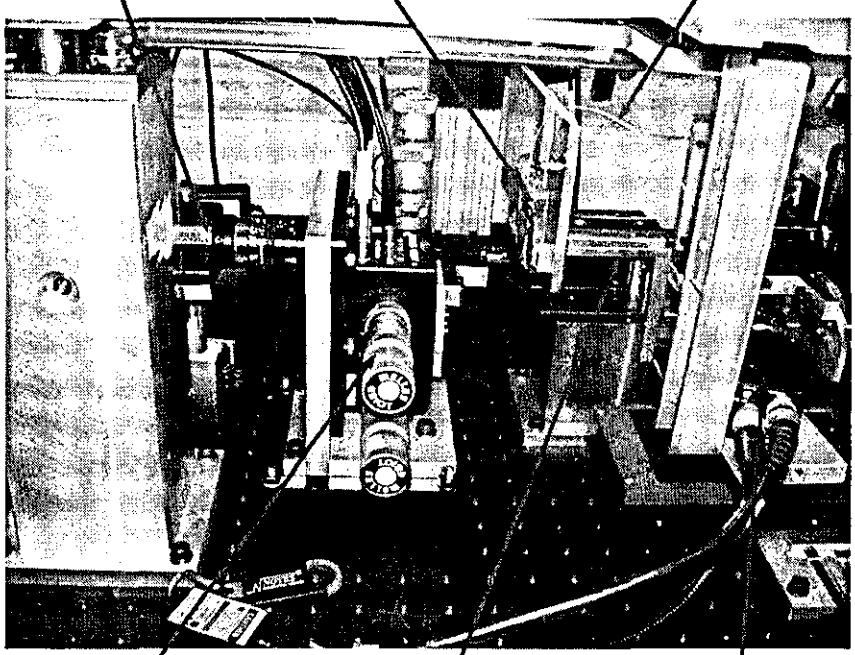


Figure 7.2 ***OSA Analysis of 850nm Source:*** *an OSA measured the central wavelength of the 850nm source used for the IL characterisation as 851.29nm.*

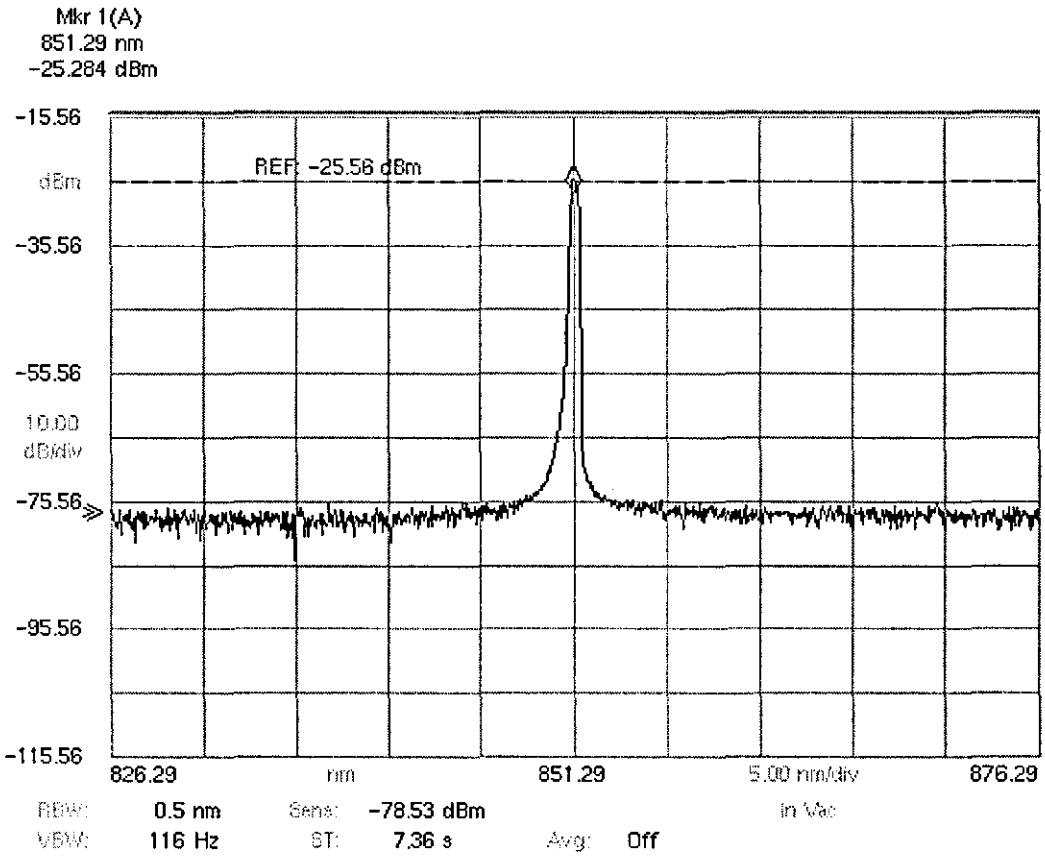


Figure 7.3 ***Stability Measurement of Test Set-up:*** *the stability of the source was recorded over a period of 5 hours, after an initial warm up period of two hours. The results show a stability of ± 0.1dB.*

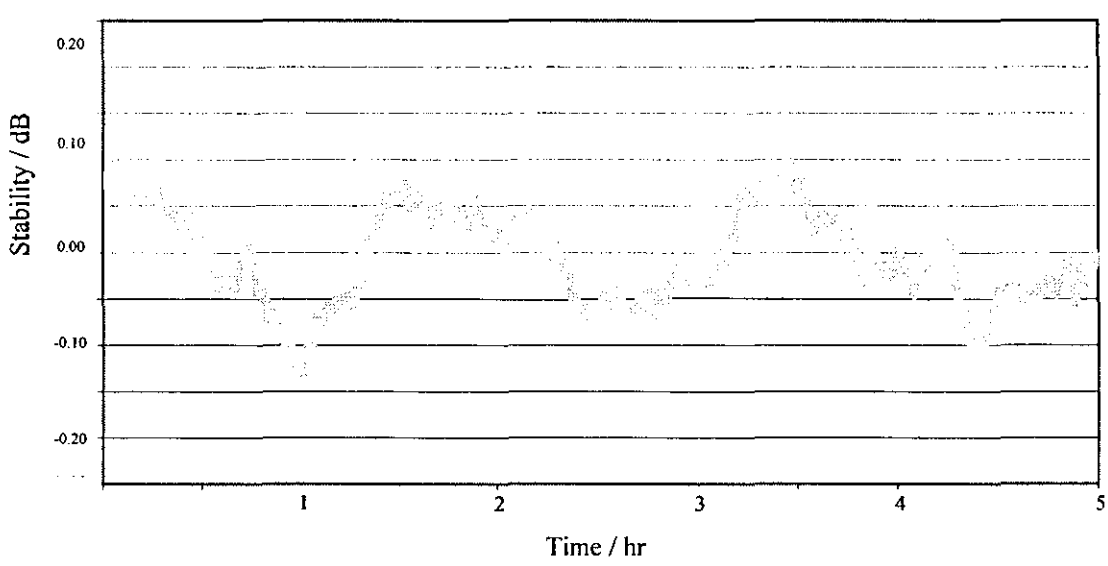


Figure 7.4 ***IL Measurement:*** *the IL measurement is taken with the OECB mounted vertically on the central platform. The fibre is initially aligned using the visible fault finder to detect first light.*

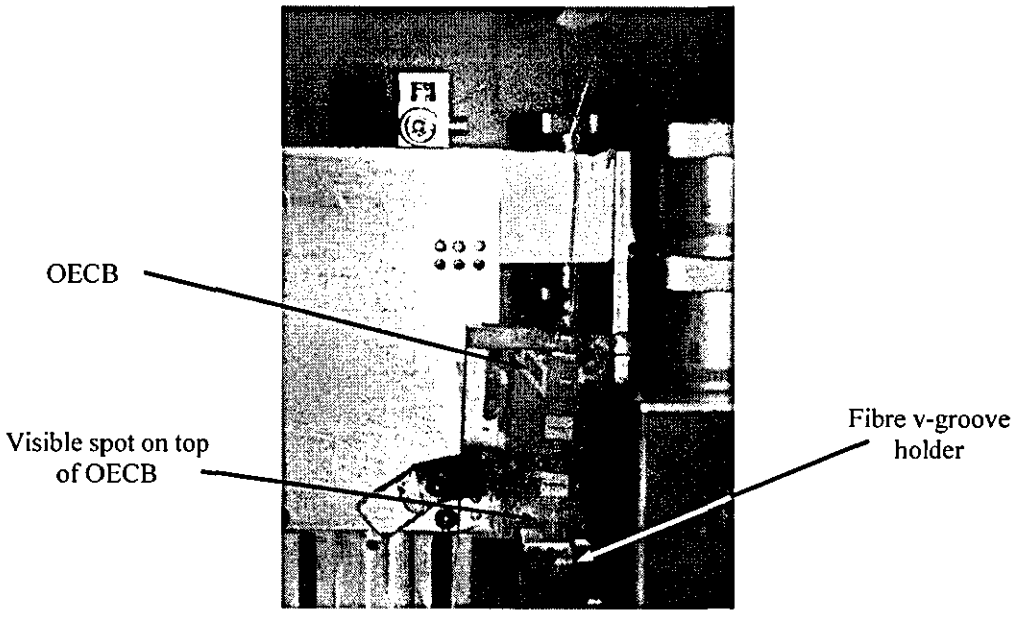


Figure 7.5 ***Demonstrator with Fibres Aligned Through the Comb Structure:*** *a comb structure is fabricated from plastic to enable multiple fibres to be aligned to a single demonstrator.*

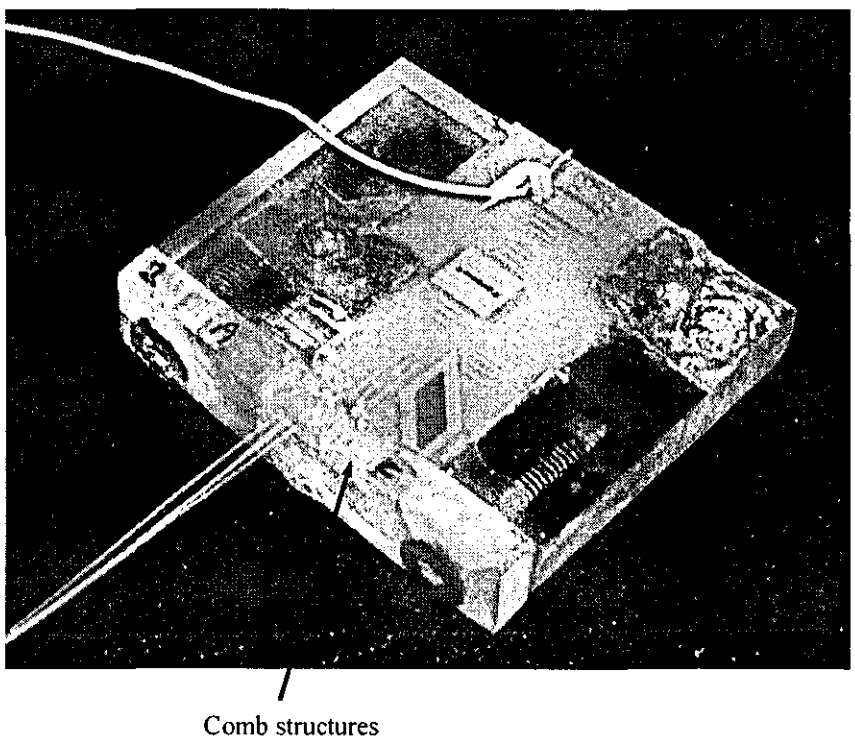
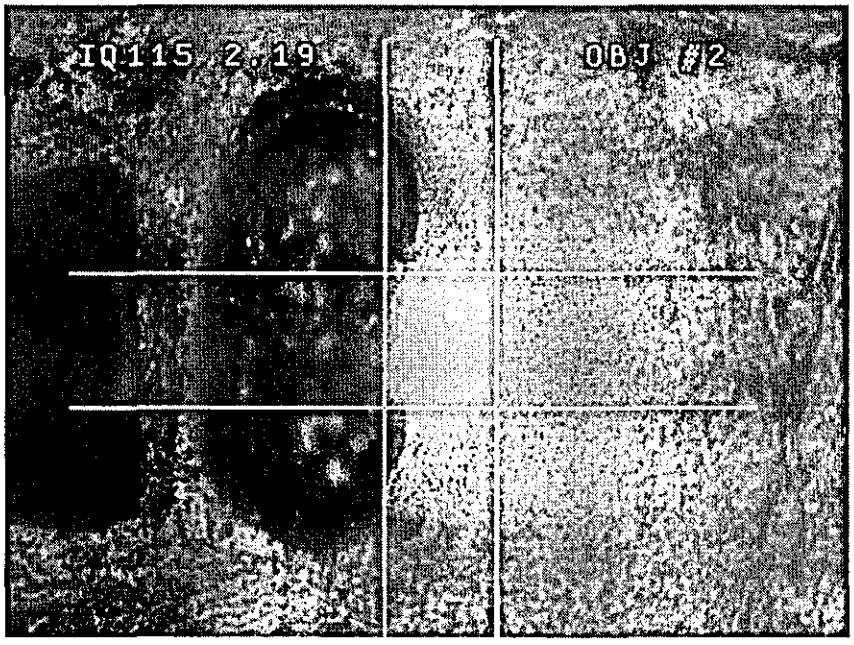
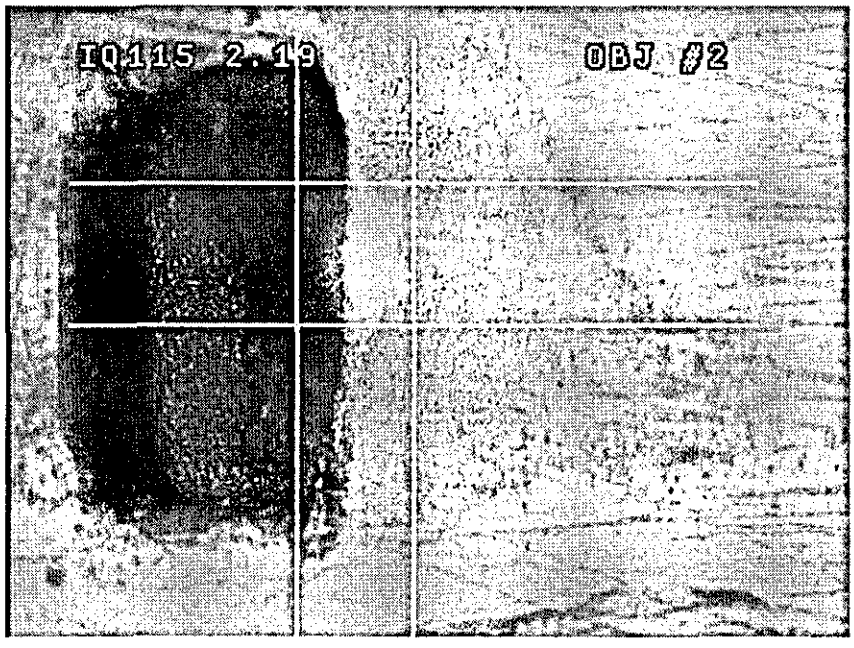


Figure 7.6 ***Spot Size Measurement for One-Dimensional Mirrors:*** *A, shows a typical result, with the spot size measured at 190μm between the cross hairs. B. emphasises the overfilling problem with the path of the light being blocked.*





Chapter 8

Improved Optical Coupling

8.0 Introduction

Although the results show partial success in achieving integrated mirrors, and optimising the process may well improve the reflection of light, the spot size on the surface of the OECB substrate is over fourteen times the area of the core of the fibre, the core being the only part that light can couple into. The reflective quality of the mirror is therefore insignificant since even with a 100% efficient mirror, only a proportion of the light can be coupled.

The only way to couple a large spot size into the fibre is to use optical elements such as lenses. Lenses are commonly formed in optics by creating droplets of adhesive and curing them [1-5]. The surface tension in the droplets creates a natural transmission lens. The properties of the adhesive and the volume of the droplet can control the focal length of the lens created in this manor. Applied to the OECB architecture, droplet lenses could improve the optical coupling by focussing the large spot into the fibre core. However the stand-off height of the lens may not be compatible with the architectures being considered. It also moves away from processing substantially flat circuit boards, which could generate problems with processes such as contact stencil printing and packaging.

An alternative to using lenses is to incorporate the focus mechanism into the electro formed mirrors. The mirrors produced and characterised in Sections 4-6 are flat mirrors inclined at 45° and can be referred to as one-dimensional integrated mirrors. Focus ability could be improved by using a curved mask to ablate the angled pocket, thereby creating a two-dimensional mirror that includes a degree of focussing.

8.1 Two-Dimensional Mirror Fabrication

Figure 8.1 shows an initial mask design that was produced to analyse the capability of the process to create two-dimensional integrated mirrors. The rough mask was fabricated using the same brass blanks that were used to manufacture the one-

dimensional mask (Section 5.3.1.). The two-dimensional mirrors are placed in the mask holder and the laser ablation process repeated, according to the process described in Section 5, and using spare waveguide samples not confusing waveguides. The two-dimensional pockets remain angled at 45° to the OECB and are back filled according to the same process described in Section 6.

Using the rough mask and machining spare waveguide samples enables a quick insight to be gained as to whether the two-dimensional mirrors are formed and specifically, whether the back filling process is capable of filling the intricate shape.

Figure 8.2 shows an example of a two-dimensional mirror structure formed using the rough mask and the two-step integrated mirror process. The SEM images show the copper deposit after the integrated mirror process and with the waveguide polymer removed for clarity. The polymer is removed using the laser. The excimer laser set-up is used to remove the polymer by orientating the sample though 180° and ablating without a mask in the mask plane.

The Figures clearly show that two-dimensional structures are capable of being formed by the ablation and back filling process. It was observed that the copper plating process did struggle to fill the corners of the pocket. However, as before, in order to achieve any meaningful results these structures need to be formed orthogonal to waveguides and tested and characterised as before and according to Chapter 7.

8.1.1 Two-Dimensional Mask Manufacture

The rough mask demonstrates that the two-dimensional structures can be made using the two step integrated mirror process. In order to get IL measurements it is necessary to form the two-dimensional mirrors in waveguides. The only difference in the set up to that described for producing one-dimensional mirrors is the mask design.

The ideal mirror shape for focusing light is parabolic [6]. The equation that defines the shape of the parabola can be equated such that the focus point of the lens can be set according to the architecture being used. Since the mask ablates a pocket with a profile taken at 45° to the mask, in order to ablate the desired parabola in the

substrate, the mask becomes a complex shape. The size of each mirror is also added to the equation since each waveguide will require its own parabolic region, whereas with the one-dimensional mirrors the mask could be stepped or large enough to intersect multiple waveguides. It is possible to produce a mask capable of ablating a pocket that intersects multiple waveguides, as shown in Figure 8.3. However, such masks require exceptional accuracy and would need to be fabricated possibly via laser cutting or plasma etching. For the trials, a single step mask design was used, the exact shape of which was approximated and cobbled together: the mask used is shown in Figure 8.4.

The mask includes a square region with a protruding ellipse area. The ellipse does not extend directly from the corners of the square area, which should relieve the problems found in the corners of the initial trials and aid the back filling of the pocket. The elliptical protrusion is responsible for creating the undercutting mirror surface. The undercutting surface remains inclined at 45° to the substrate.

8.1.2 Manufacturing Trials

The two-dimensional mask is arranged in the mask plane. The mask requires careful alignment within the maskplane, to ensure that the tip of the parallax is arranged orthogonal to the waveguide. If the mask is misaligned with the mask plane and relative to the waveguide, the mirror will not correctly focus the light. With the mask inserted correctly in the mask holder the pockets are ablated according to the process explained in Section 5 and using the same demonstrator samples.

The two-dimensional pockets are back filled using the plating process detailed in Section 6. The height of the copper deposits are controlled by viewing the deposit at periodical intervals in order to stop plating when at least 90% of the pockets depth is filled. The pockets are of similar volume to the one-dimensional mirrors and therefore also take approximately ninety minutes to plate.

8.2 Two-Dimensional Mirror Characterisation

The two-dimensional mirrors can be optically characterised using the same method described in Section 7. Some of the mirrors were also cross-sectioned in order to be sure that the copper completely filled the ablated pocket.

8.2.1 Trial Results and Discussion

Two-dimensional integrated mirrors were fabricated using the shaped mask and back-filled with electroplated copper. The mirrors were characterised for IL. The IL measurements are shown in Table 8.1. The results do not show a significant improvement in the average when compared to the one-dimensional mirrors. However, the range is a lot larger with results spaced between -19.36 dB and -2.00 dB.

The low ILs can be explained due to the reduced spot size, which, as shown in Figure 8.5, is reduced to around 50μm. The high ILs can be explained due to poor alignment between the ablation site and waveguide. The high IL mirrors all exhibited symptoms similar to that shown in Figure 8.6, wherein the mirrors are misaligned to the waveguides and the reflected light splits in to more than one beam, which remains within the cladding. The average IL for the mirrors that showed good alignment is -2.9 dB.

Table 8.1 ***IL Measurements for Two-Dimensional Mirrors:*** two-dimensional *integrated mirrors fabricated using the shaped mask and backfilled with electroplated copper where characterised for IL according to Chapter 7. The results show an average IL of -8.39 dB. However, the average IL for aligned mirrors is -2.9dB.*

No.		Power level / μW 1	2	3	Average / mW	Loss / dB	No.		Power level / μW 1	2	3	Average / mW	Loss / dB
1c5	P_0	20.7	20.83	22.09	21.21	-6.10	3a2	P_0	85.02	87.63	87.86	86.84	NA
	P_1	4.68	4.488	6.441	5.20			P_1	Broken Fibre			NA	
1d3	P_0	28.21	31.06	31.11	30.13	-19.36	3b2	P_0	45.39	49.66	45.09	46.71	NA
	P_1	0.324	0.361	0.362	0.35			P_1	Broken Fibre			NA	
1d4	P_0	30.65	30.92	31.64	31.07	-14.10	5c1	P_0	2.81	2.85	2.84	2.83	-2.00
	P_1	1.114	1.125	1.384	1.21			P_1	1.77	1.82	1.77	1.79	
1d5	P_0	32.83	31.59	33.12	32.51	-3.60	5c2	P_0	5.68	5.53	5.48	5.56	-10.54
	P_1	14.36	13.98	14.23	14.19			P_1	0.48	0.482	0.511	0.49	
2a3	P_0	47.83	50.01	51.33	49.72	NA	5c3	P_0	6.21	5.78	5.37	5.58	NA
	P_1	Broken Fibre			NA			P_1	Broken Fibre			NA	
2e2	P_0	38.45	38.25	37.2	37.97	-3.03						Max	-19.36
	P_1	19.00	18.93	18.78	18.90							Min	-2.00
2e3	P_0	40.76	42.30	46.01	43.02	NA						**Average**	**-8.39**
	P_1	Broken Fibre			NA								

A full DOE optimisation of the process parameters may further reduce the IL. However, in order to complete the optimisation process the alignment issues between the mask and waveguide need to be addressed. Thereby ensuring that sufficient results are achieved in which the mask is aligned to the waveguide. Further improvements may also be realised by designing and fabricating an improved mask.

8.3 Three Dimensional Mirrors

The spot size reduction from around 190μm to around 50μm, between one-dimensional and two-dimensional mirrors respectively, enabled IL measurements of around the 3dB benchmark to be achieved. However, this still corresponds with a 50% loss of light and with other components in the system having much lower losses, the IL of the mirrors needs to be a minimum. Whilst process optimisation and better made design and manufacture may yet further reduce the losses of the mirror, profiling the mirrors in the third dimension to produce spherical parabolic reflective surfaces may produce even smaller spot size and therefore even lower losses.

Three-dimensional integrated mirrors would have a curved undercutting surface, for example three-dimensional mirrors would have a cross-section similar to that shown in Figure 8.7. Whereas both one-dimensional and two-dimensional mirrors have a constant gradient optimally inclined at 45°.

Section 8.3.1 discusses the process modifications that would be required to enable the proposed two step integrated mirror manufacturing process to fabricate three-dimensional structures.

8.3.1 Recommended Process Modifications

Three-dimensional mirrors may be able to be fabricated using the same set-up as is described herein for producing one-dimensional and two-dimensional mirrors. A similar mask used for two-dimensional mirrors is required and should be designed and manufactured for producing a parabolic ablation on the surface of the substrate. The mask holder requires additional engineering to ensure that the parabolic mask is correctly aligned with the waveguides to avoid the poor reflectance noticed with two-

dimensional mirrors. The alignment tables may need a rotational axis added about the vertical axis in order to assist in resolving the misalignment issues.

Furthermore, in order to produce three-dimensional mirrors the laser ablation process needs to be modified to allow the position and angle of the ablation site to be manipulated. This would require adding a translational movement to the penultimate directional mirror and also adding a rotational axis to the final angle mirror. A computer would need to manipulate the two axes in order to choreograph the position and angle of the laser beam. Figure 8.8 shows a four-stage process for ablating three-dimensional mirrors with an arcuate cross-section. A first ablation step would produce a vertical pocket with the final angle mirror set at 0 degrees (i.e. out of the way). The angle of the final mirror would then be adjusted to 67.5° and the final downward mirror position adjusted to make a second ablation. The pocket would be finished by two further ablations at 45° and 22.5°. The example shown would give a faceted undercut surface. Increasing the iterations would smooth out the undercut edge or the movement could be made continuous to produce an optimum finish.

An alternative embodiment to direct the three-dimensional mirrors could be ablated by moving the work piece rather than the first downward mirror. Either process however, would require precisely controlled movement of the angle of the laser beam and the position of the work piece relative to the beam. Optimisation of the parameters of such a three-dimensional manufacturing process may be able to further improve the optical coupling. It may also prove an important capability for the future should lower losses throughout the link be required and as such the advantages of single mode technology be deployed across onboard USR interconnects. Wherein the integrated mirrors will be required to focus the beam into a 9μm core.

8.4 Summary

The flat, one-dimensional mirrors characterised in Chapter 7 do not achieve sufficient efficiency, which can be mainly attributed to the large spot size. Fabricating curved, two-dimensional mirrors that incorporate a degree of focus into the integrated mirror may reduce the spot size. Two-dimensional mirrors can be fabricated using the same process set-up as one-dimensional mirrors only with a shaped mask.

Two-dimensional mirrors fabricated and characterised generally in accordance with Chapters 5-7 but with a modified mask produced spot sizes of around 50μm. The IL measurements contained spurious results associated with mirrors that were not correctly aligned to the waveguide. The average IL of correctly aligned mirrors was 2.9dB.

Two-dimensional mirrors are capable of producing adequate mirrors. The process still requires optimisation, which may improve the results yet further. In order to optimise the process, a precise mask is required and the laser set-up requires improvements that will better facilitate the alignment of the mask and waveguide.

The optical coupling may be yet further improved by fabricating three-dimensional integrated mirrors, wherein the mirror comprises an arcuate cross-section as well as profile.

References

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Figure 8.1 ***Original Two-Dimensional Mask Design:*** *a two-dimensional mask was manufactured from a brass blank. The mask was used to fabricate the two-dimensional mirror structures shown in Figure 8.2.*

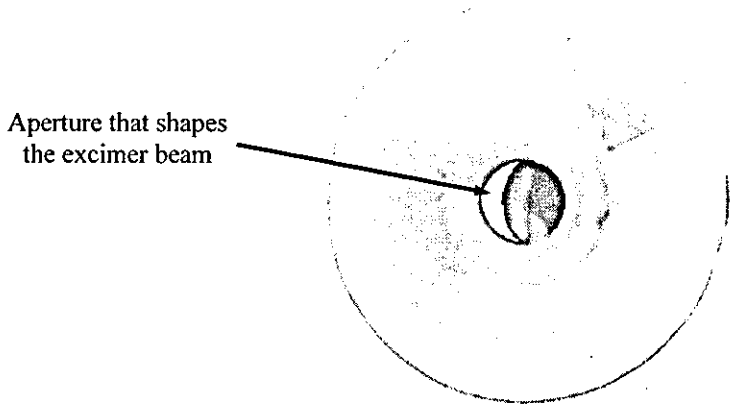


Figure 8.2 ***SEM Analysis of Two-Dimensional Mirror Structures:*** *the two-dimensional mirror structures are viewed using a SEM by first removing the polymer surrounding. A) Shows a formed structure. B) Shows a structure with the effects of copper overfilling still visible. C) Shows a magnified portion of the undercut surface.*

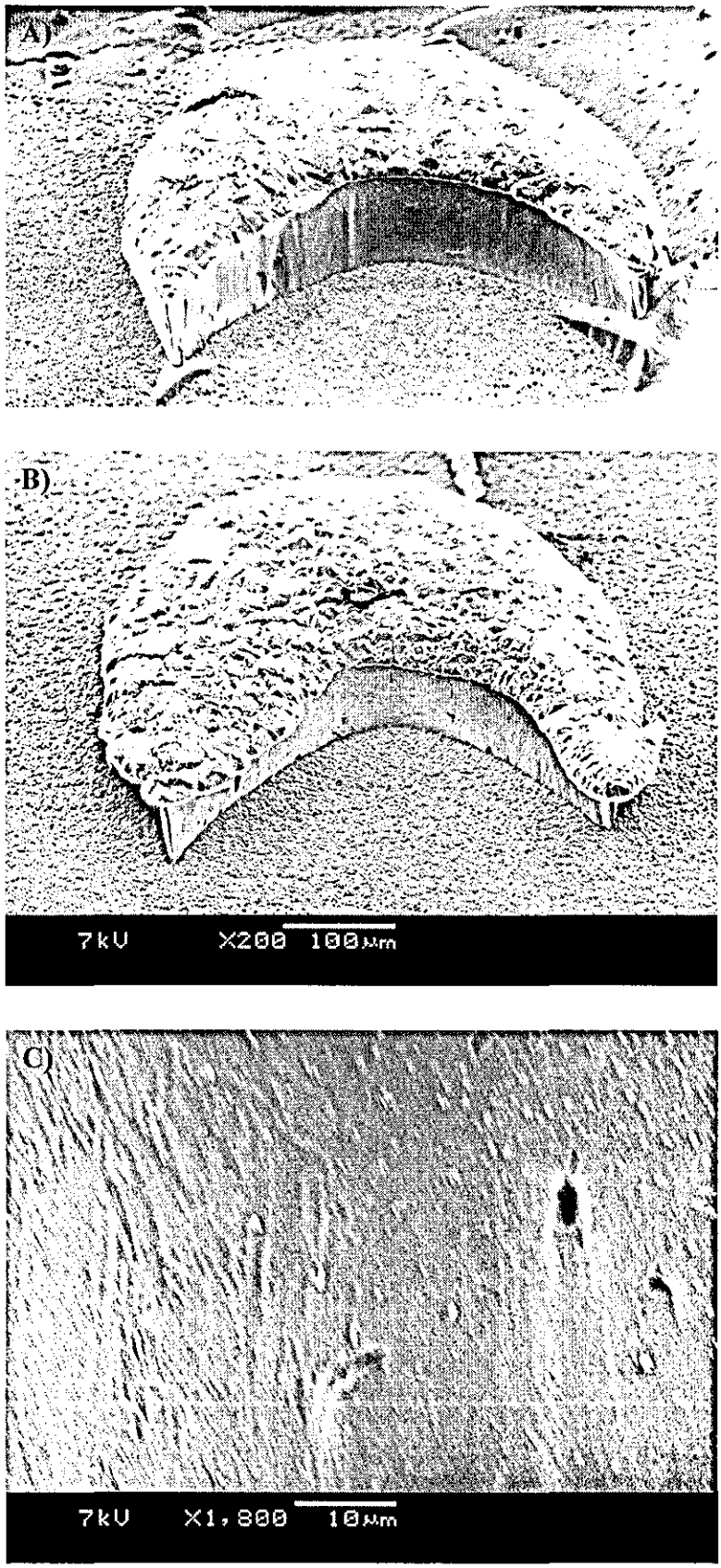


Figure 8.3 ***Mask Alignment for Multiple Two-Dimensional Mirrors:*** *whereas one-dimensional masks can intersect multiple waveguides, two-dimensional masks require careful alignment between the mask and waveguide.*

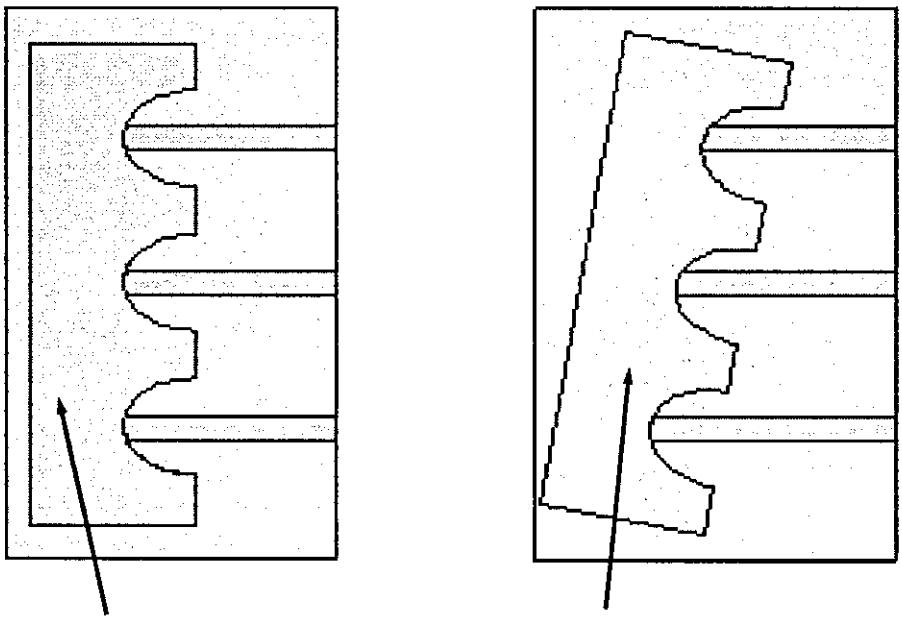


Figure 8.4 ***Two-Dimensional Integrated Mirror Mask and Ablation Pattern:*** *A) shows the mask design that was used to fabricate the two-dimensional mirrors characterised in table 8.1. B) Shows the ablation profile in the OECB substrate wherein the cross hairs denote a 50μm square.*

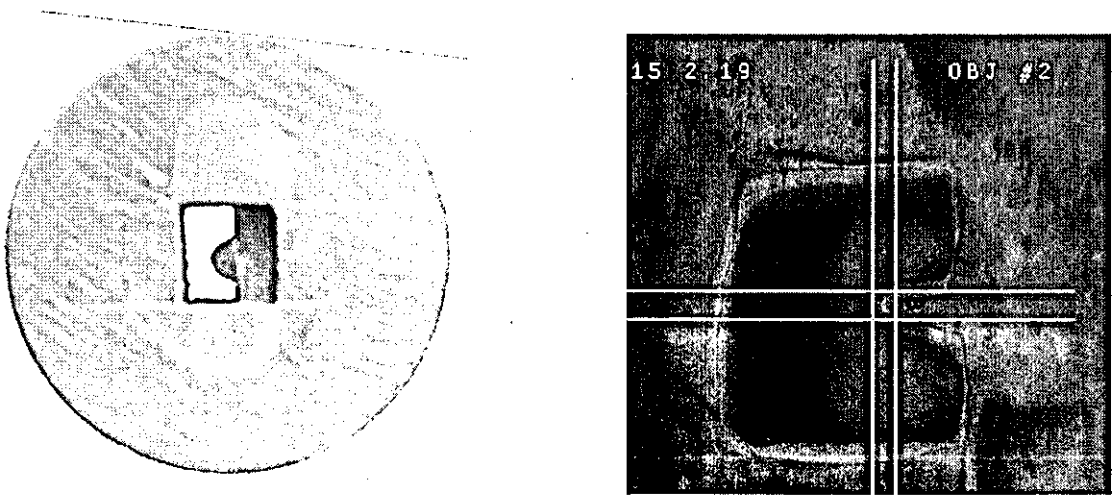


Figure 8.5 ***Two-Dimensional Integrated Mirror:*** *a backfilled two-dimensional mirror is shown. The cross hairs mark a 50μm square. The bottom figure depicts as a red dot and in the area circled the light that is reflected upwards.*

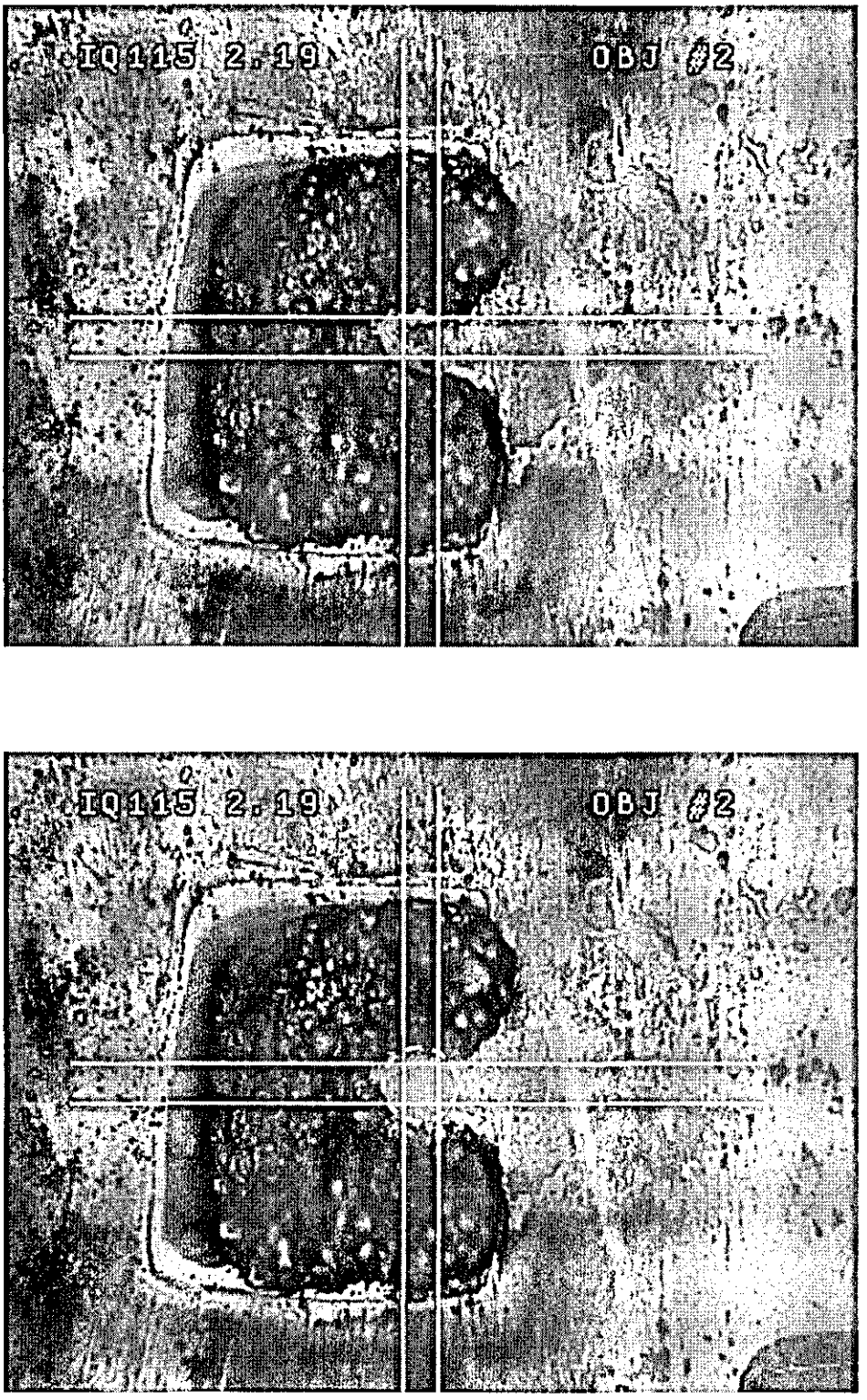


Figure 8.6 ***Misalignment of Two-Dimensional Masks****: poor alignment of the mask to waveguide creates erroneous IL readings, as the light tends to scatter in one or more major directions.*

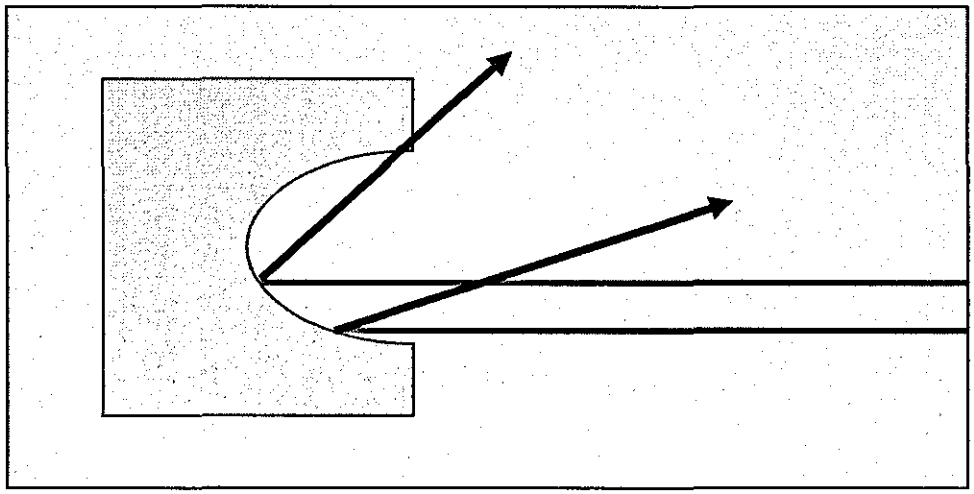


Figure 8.7 ***Three-Dimensional Integrated Mirrors****: a plan and cross-sectional view of a two-dimensional mirror and proposed three-dimensional mirror is given.*

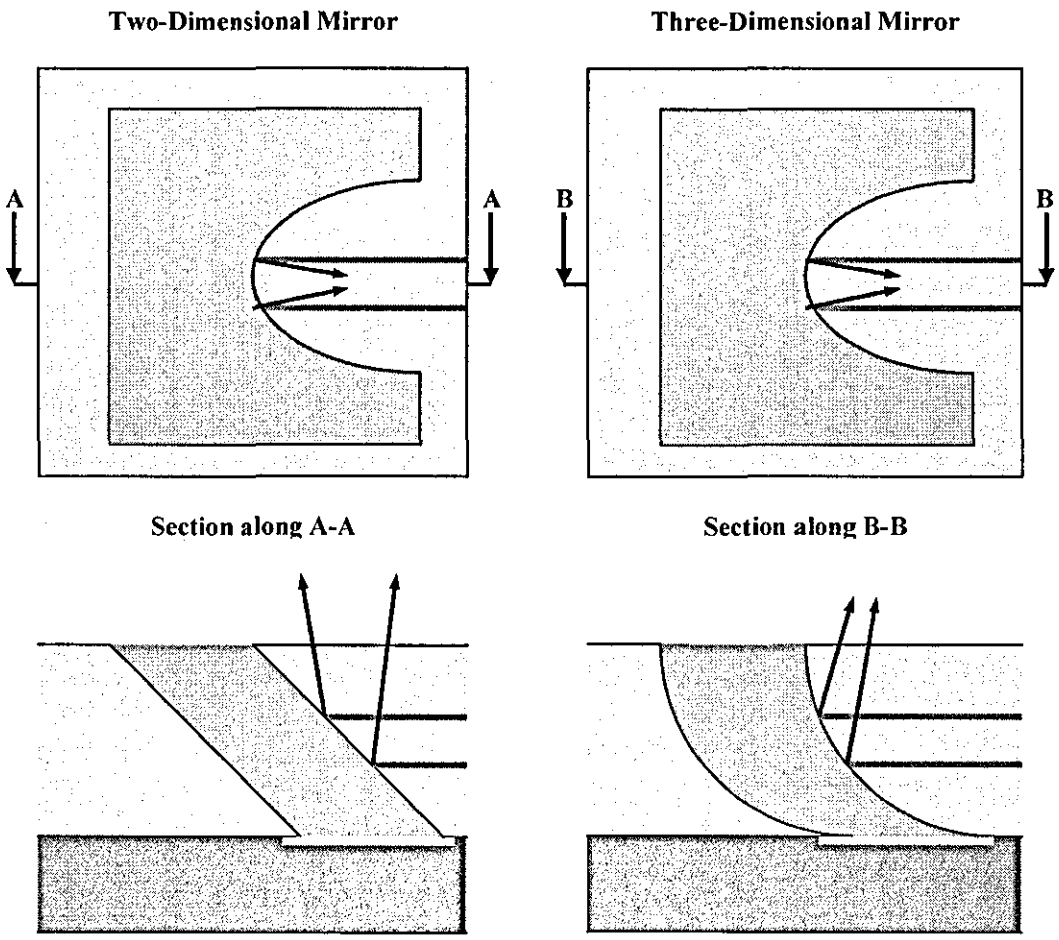
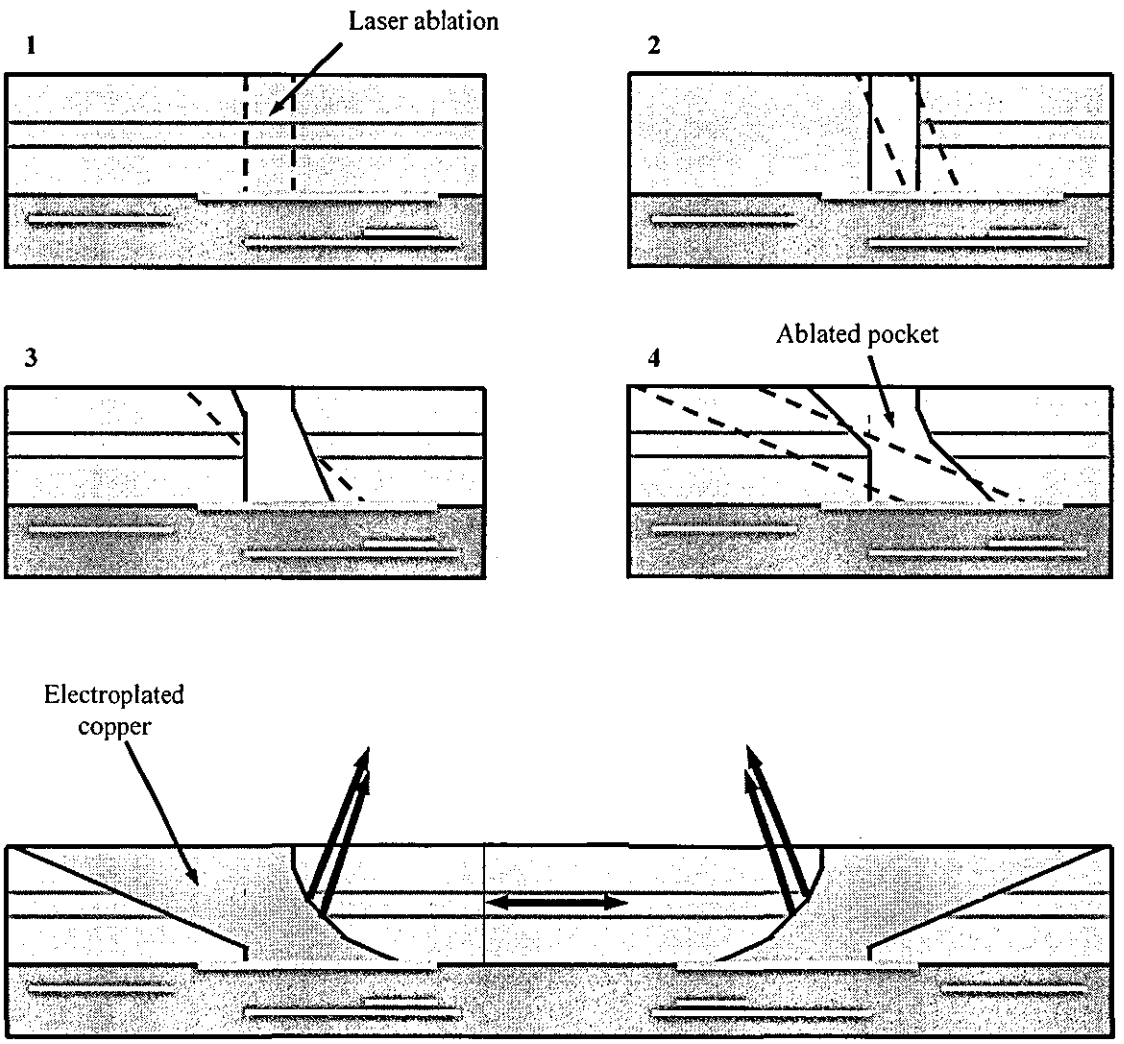


Figure 8.8 ***Fabrication of Three-Dimensional Mirrors****: the figure depicts a four-iteration laser ablation process for fabricating three-dimensional mirrors. Increasing the iterations, preferably infinitely, will create an undercutting surface with a smooth parabolic cross-section. The bottom figure shows the ablated three-dimensional pocket backfilled with electroplated copper.*



Chapter 9

Conclusions

9.0 Conclusion

This Chapter presents, in three sections, the conclusions from the work completed in this thesis. The first section concludes the development work conducted into one-dimensional integrated mirrors. The results from the experimental work allow the laser ablation set-up, electroplating process and characterisation equipment to be assessed. The capabilities of the three stages are documented. The IL results do not suggest that one-dimensional mirrors are capable of achieving sufficient efficiency for USR interconnects.

In the second section conclusions are presented on the research work conducted into two-dimensional integrated mirrors. Two-dimensional mirrors address the IL problems associated with a large spot size as identified during the characterisation of the one-dimensional mirrors. Alignment issues arise between the mask and waveguide, although IL results demonstrate that two-dimensional mirrors are capable of producing sufficient efficiency to be deployed across USR interconnects. Further work is required to gain a complete characterisation of the process and fabricated integrated mirrors.

In the third section, conclusions are presented ion the benefits and requirements of fabricating three-dimensional mirrors. Further research is required in to the production of three-dimensional mirrors.

The findings presented in this thesis provide a fundamental understanding of the ability to form integrated mirrors using a two-step process comprising ablating an angled pocket and backfilling the pocket with an electroplated metal. As identified in the thesis, the development of such integrated mirrors is the current barrier to the deployment of OECB based USR interconnects. The knowledge gained in this research can thus provide a basis from which both future process characterisation work of two-dimensional mirrors can begin and also as a basis to drive future development work of three-dimensional mirrors.

9.1 One-Dimensional Integrated Mirrors

The research work conducted into one-dimensional integrated mirrors allowed the process and equipment parameters to be evaluated. Excimer laser ablation of undercut pockets was proven. The polymer was cleanly ablated and the copper pad proved an effective beam stop. The ablation was reliable and repeatable. The material beneath the undercutting surface ablated at a reduced rate to the material not shadowed by the edge. However, the beam stop enabled all the material to be removed by increasing the ablation time. The main laser process parameter that requires controlling is focus. A contact measurement probe, as used in the experimental work, or preferably a non-contact measurement probe, which would enable the measurement to occur closer to the ablation site, can control focus. The laser power also requires controlling. For optimum results the power needs to be set at a level just above the ablation threshold of the polymer but beneath that at which heat induced blackening occurs.

Electroplating enables the pockets to be backfilled in order to create a polymer-metallic interface on the undercutting surface. Correct preparation of the substrate is required. Copper used in the trials showed the formation of good mirror like structures. Complications arise in controlling the amount of electroplated deposit. Overfilling the pockets leads to a mushroom effect on the top of the OECB, which interferes with the optical signal. The copper deposit can be better controlled through improved bath conditions and by connecting a single mirror to a single pad. In a properly controlled bath the deposit should be uniform and the deposit volume controlled precisely by the current and plating time.

Whilst the demonstrator preparation using the comb structures aligned fibres to the OECB samples and the losses generated should be referenced out of the IL, the process is not ideal. Preparing the demonstrator using ribbon fibre would enhance the reliability of the results. This would require a rotational axis to be added to the alignment stages. Furthermore, preparing the demonstrators with pig-tailed fibre rather than using BFAs would also improve the uncertainty of the IL measurements.

The characterisation equipment and process enabled IL measurements of the integrated mirrors to be recorded. Average IL measurements for one-dimensional mirrors were found to be around 9dB. This IL is high and is not suitable for use in OECB architectures, as it does not couple enough light between the components and waveguides. It is not recommended that any further research be conducted into one-dimensional mirrors.

9.2 Two-Dimensional Integrated Mirrors

Two-dimensional mirrors decreased the spot size of one-dimensional mirrors from around 190μm to around 50μm. The spot size reduction enables more light to be coupled into the core of the fibre and accounted for IL results of around –2.9dB, when correctly aligned. The results displayed a wide range of results, due to spurious results found when the mirrors were not correctly aligned to the waveguides. The mirror misalignment is generated by a misalignment of the mask and waveguide during the ablation process.

The IL results are sufficient to drive further research into the area of two-dimensional integrated mirrors within OECB based architectures. Recommendations for further work can be found in Section 10.1.

It is recommended that in order to achieve reliable, repeatable, sufficient results to complete the further work, the following modifications should be made to the process equipment used for the experimental work described herein:

1. Improved mask design and fabrication – the optimum parabolic curve for the mirror surface requires defining, which would allow the subsequent mask shape to be equated. Said mask design is required to be precisely fabricated. Preferably a mask that enables multiple waveguides to be intersected should be used, as this would allow more alignment references to be taken.

2. Improved mask alignment – the mask holder requires better alignment capabilities in order to align the mask with the waveguides, both laterally and rotationally.

3. Improved plating bath conditions – an improved plating bath should be used such that the deposit can be precisely controlled so that overfilling does not occur.

4. Improved demonstrator preparation – the demonstrators should be prepared using ribbon fibre with pig-tailed connectors, which would require an additional rotational axis to be added to the alignment stages of the characterisation equipment.

9.3 Three-Dimensional Integrated Mirrors

Improvements may be able to be made to the coupling efficiency of integrated mirrors by fabricating three-dimensional mirrors. Three-dimensional mirrors may become important when the inevitable drive for greater performance begins to strive for single-mode embedded waveguides on USR interconnects. In order to conduct the further work recommended in Section 10.2, the following process modifications are suggested to the equipment described herein and in addition to those outlined above:

1. Rotational and linear mirror axes – it is recommended that a rotational axis is added to the final angle mirror and linear axis to be incorporated into the final beam turning mirror of the optical train of the excimer laser equipment set-up.

2. Computer control of mirror axes – it is recommended that a computer control the additional rotational and linear mirror axes so that the arrangement of the laser beam can be precisely choreographed.

Chapter 10

Further Work

10.0 Recommendations for Further Work

From the results achieved by this thesis, it has been revealed that one-dimensional mirrors do not couple sufficient light between components and waveguides in order to encourage further research work. However, two- and three-dimensional mirrors are thought to provide sufficient promise to drive further work in these research areas. Recommendations for further work are presented for each mirror type in the respective following sections.

10.1 Two-Dimensional Integrated Mirrors

In order to complete further research work, it is suggested that the recommended changes to the process set-up identified in Section 9.2 are first made. This will allow reliable and repeatable experiments to be conducted. With the modifications made, it is desirable to complete a full DOE investigation into the process parameters of the manufacturing steps. It is recommended that a structured approach be used, such as that identified in Section 4.4, in order that the important parameters that affect IL can be distilled and optimised. The DOE should include an investigation of different electroplating materials, for example gold and silver.

A large experiment can then be run to measure the performance of the optimised two-dimensional integrated mirrors. The results can be used to set process parameters and tolerances. As well as characterising the optimised mirrors in terms of IL, the fabricated mirrors should also be characterised in terms of the following:

1. Digital Communications Analyser (DCA) – to allow the eye diagram to be analysed.

2. Bit Error-Rate Testing (BERT) – in order to determine the bit error rate of the interconnections.

3. Life Testing – accelerated thermal testing in order to characterise the performance of the mirrors after degradation simulating factors experienced during use.

Finally, depending on the results, a demonstrator should be manufactured to showcase the capability of the OECB architecture with integrated two-dimensional mirrors. The demonstrator should be similar to that depicted in Figure 2.6 and should include waveguides connected to edge connectors for backplane interconnection (e.g. daughter-card to backplane), waveguides coupled to surface mounted fibre, and waveguides coupled directly to active devices.

10.2 Three-Dimensional Integrated Mirrors

Simultaneously to the two-dimensional work, further research can also be initiated to investigate the potential of three-dimensional integrated mirrors, particularly with respect to use with single mode waveguides. Such work would need to investigate the formation of three-dimensional structures according to the two-step process identified herein and also characterise the IL of such mirrors in order to drive further research interest in this area.

Appendix A
Patent search

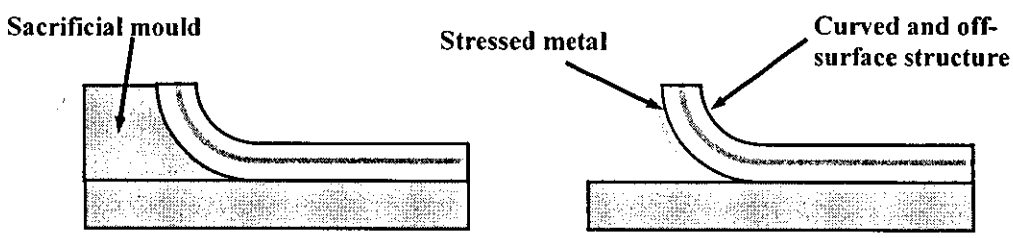
	Applicant	Pub. Date Patent No.
1] Curved metal-polymer dual-mode/function optical and electrical interconnects, methods of fabrication thereof, and uses thereof		2004-09-23 US2004184704
2] Optical circuit element and production method therefore, array-form optical circuit element, optical circuit device using it		2004-07-08 US2004131302
3] Multi-layer printed circuit board and the method for coupling optical signals between layers of multi-layer printed circuit board		2004-06-10 US2004109628
4] Optically connectable circuit board with optical components mounted thereon		2004-05-27 US2004100781
5] Circuit board e.g. for add-drop multiplexer in optical communications, has electro-optical and /or opto-electrical component coupled with electrical and optical conductor paths	Siemens AG (DE)	2004-03-25 DE10241203
6] Coupling to waveguides that are embedded in printed circuit boards	Siemens AG (DE)	2003-01-16 WO03005094
7] Electro-Optical Circuit Board Having Optical Transmit / Receive Module and Optical Waveguide		2004-02-26 US2004037512
8] Connection to optical backplane	Terahertz Photonics	2004-01-29 W02004010191
9] Optical high speed bus for a modular computer network	Raytheon Corp (US)	2003-11-18 US6650808
10] Passive alignment connection for fibre optical incorporating VCSEL emitters		2003-11-13 US2003210873
11] Integration and alignment of VCSELs with MEMS using micro-machining and flip-chip techniques	Xerox Corp (US)	2003-11-11 US6647036
12] Integrated optoelectrical circuit package with optical waveguide interconnects	Intel Corp (US)	2003-10-02 US2003185484
13] Optical clocking distribution using diffractive metal mirrors and metal via waveguides	Intel Corp. (US)	2002-02-26 US6351576
14] Integrated Platform for Passive Optical Alignment of Semiconductor Device with Optical Fibre	App. Science Tec. Centre	2003-09-18 WO03077001
15] Device for introducing light into a waveguide, device for emitting light from a waveguide and method for manufacturing such devices	Lionix B V (NL)	2003-07-10 WO03056374
16] Process for efficient light extraction from light emitting chips		2003-07-03 US2003124754
17] Optical coupling for optical fibres		2003-06-26 US2003118282
18] Passive alignment microstructures for electro-optical devices	CSEM (Switzerland)	2003-05-02 0118511.5
19] Optically Interconnecting Integrated Circuit Chips		2003-01-09 US2003007745
20] Flip-chip Package Integrating Optical and Electrical Devices and Coupling to a Waveguide on a Board		2003-01-02 US2003002770
21] Packaging and Assembly Method for Optical Coupling		2002-12-26 US2002196997
22] Optical device		2002-12-05 US2002181903
23] PCB embedded and surface mounted optical distribution systems		2002-10-03 US2002141163
24] Apparatus for coupling light into an optical waveguide	CIDRA Corporation (US)	2002-09-26 WO02075402

25] Active Optical Device	Zarlink Semiconductor	2002-08-29 US2002117679
26] Packaging system for two-dimensional optoelectronic arrays		2002-08-08 US2002104959
27] Optical interconnection circuit board and manufacturing method thereof		2002-04-04 US2002039475
28] Packaging enhanced board level opto-electronic interconnects	University of Texas (US)	2001-06-05 US6243509
29] Reflective coupling array for optical waveguide	Corning Inc. (US)	1998-07-16 WO9830925
30] Waveguide optical deflector, process for producing the same, and saw blade for use in this process		1998-02-04 EP0822430
31] Method for fabrication of mirrors in integrated optical waveguides	Bosch GMBH Robert (DE)	1998-01-07 EP0816878
32] Optical module having a reflective optical waveguide	Motorola Inc (US)	1995-05-10 EP0652454
33] Fabrication of cooled faceplate segmented aperture mirrors (SAM) by electroforming	US Airforce (US)	1988-04-26 US4740276

1] Curved metal-polymer dual-mode/function optical and electrical interconnects, methods of fabrication thereof, and uses thereof

Applicant			
Patent Number	US2004184704	**Publication Date**	2004-09-23
IPC Classification	GO2B6/12		

Summary of the Application



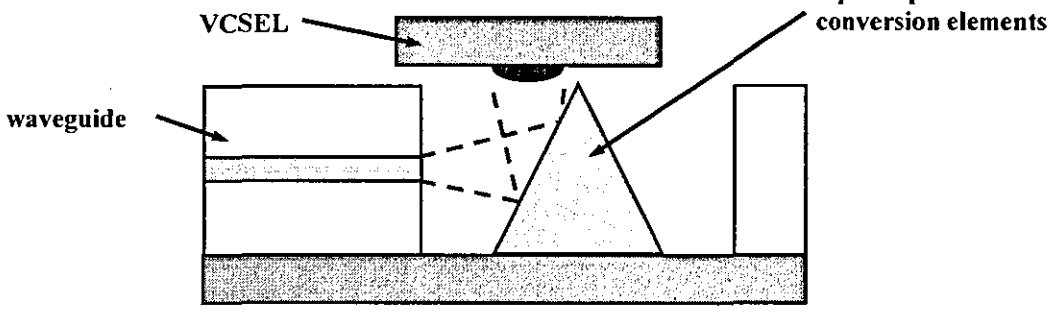
The patent details two methods for creating curved and off-surface structures, which can be used to couple waveguides out-of-plane without the need for gratings or mirrors. The structures can be fabricated by either coating the waveguides over a sacrificial mould and subsequently removing the mould, or by coating the waveguides over a stressed metal portion that when released curls upwards. The metal layer is used to create the curved structure rather than to reflect any light.

Comparison to OECB Invention

Field	Coupling waveguides out-of-plane without the need for gratings or mirrors
Related Art	none

2] Optical circuit element and production method therefore, array-form optical circuit element, optical circuit device using it			
Applicant			
Patent Number	US2004131302	**Publication Date**	2004-07-08
IPC Classification	G02B6/12; G02B6/26		

Summary of the Application



The invention relates to a device and method for monitoring light propagating down a waveguide by forming out-of-plane interconnections with PDs and other optical components. Cavities are formed in the ends of the waveguides and optical path conversion elements installed inside. The optical path conversion elements can be fabricated by inserting metal bumps into the cavities and then forming them with a mould, which can be flat or shaped to produce flat or curved mirrors. The cavity can be filled to reduce transmission losses. The optical path conversion elements deflect light travelling along the waveguide through 90° for coupling with optical components e.g. PDs.

Comparison to OECB Invention

Field	Coupling light out of an arrayed waveguide device.
Related Art	Similar to inserted component coupling techniques.

3] Multi-layer printed circuit board and the method for coupling optical signals between layers of multi-layer printed circuit board			
Applicant			
Patent Number	US2004109628	**Publication Date**	2004-06-10
IPC Classification	G02B6/12; Go2B6/26		

Summary of the Application

The patent describes a method for optically coupling between layers of a multi-layer PCB using optical signal coupling blocks. The optical coupling blocks are inserted into via holes formed in the PCB. Subsequently waveguide layers are laminated in a build up manner.

Comparison to OECB Invention

Field	90° out-of-plane optical coupling from board level waveguides.
Related Art	Patent comprises of methods for creating out-of-plane coupling using inserted components.

4] Optically connectable circuit board with optical components mounted thereon			
Applicant			
Patent Number	US2004100781	**Publication Date**	2004-05-27
IPC Classification	H05K1/18; H05K7/06		

Summary of the Application

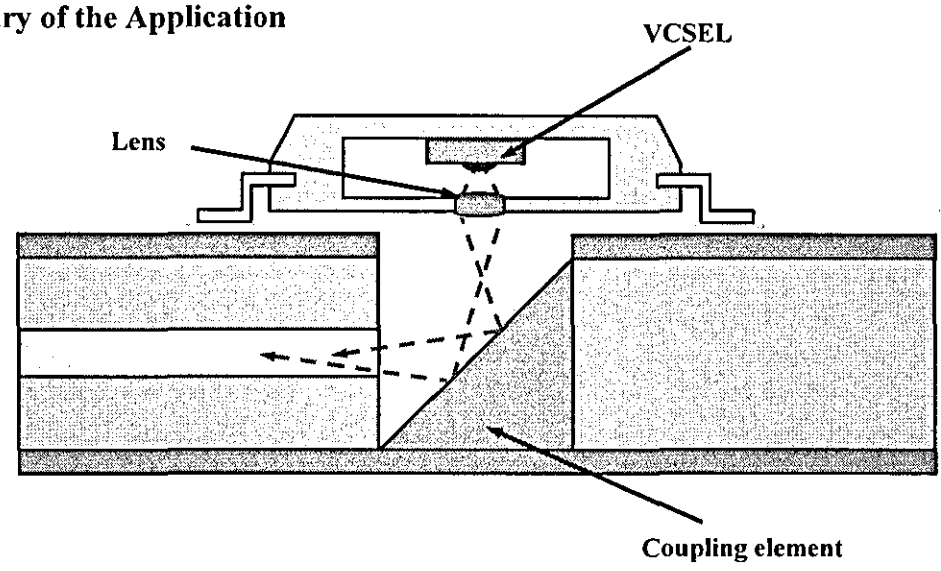
Surface mounted VCSELs and PDs are connected via waveguides. Optical coupling is achieved through gratings and mirrors, although there is no mention of how these structures are fabricated.

Comparison to OECB Invention

Field	Optical connection of components across PCBs.
Related Art	No definition of fabrication methods.

5] Circuit board e.g. for add-drop multiplexer in optical communications, has electro-optical and /or opto-electrical component coupled with electrical and optical conductor paths			
Applicant	Siemens AG (DE)		
Patent Number	DE10241203	**Publication Date**	2004-03-25
IPC Classification	H05K1/02; H05K3/46; G02B6/42		

Summary of the Application



VCSEL beam is coupled into the waveguide via a lens by reflecting of an integrated coupling element. The coupling element can be a mirror or MEMS element.

Comparison to OECB Invention

Field	Optically coupling VCSELS to optical PCBs
Related Art	Inserted component technology

6] Coupling to waveguides that are embedded in printed circuit boards			
Applicant	Siemens AG (DE)		
Patent Number	WO03005094	**Publication Date**	2003-01-16
IPC Classification	G02B6/43; G02B6/42; G02B6/12; G02B6/38		

Summary of the Application

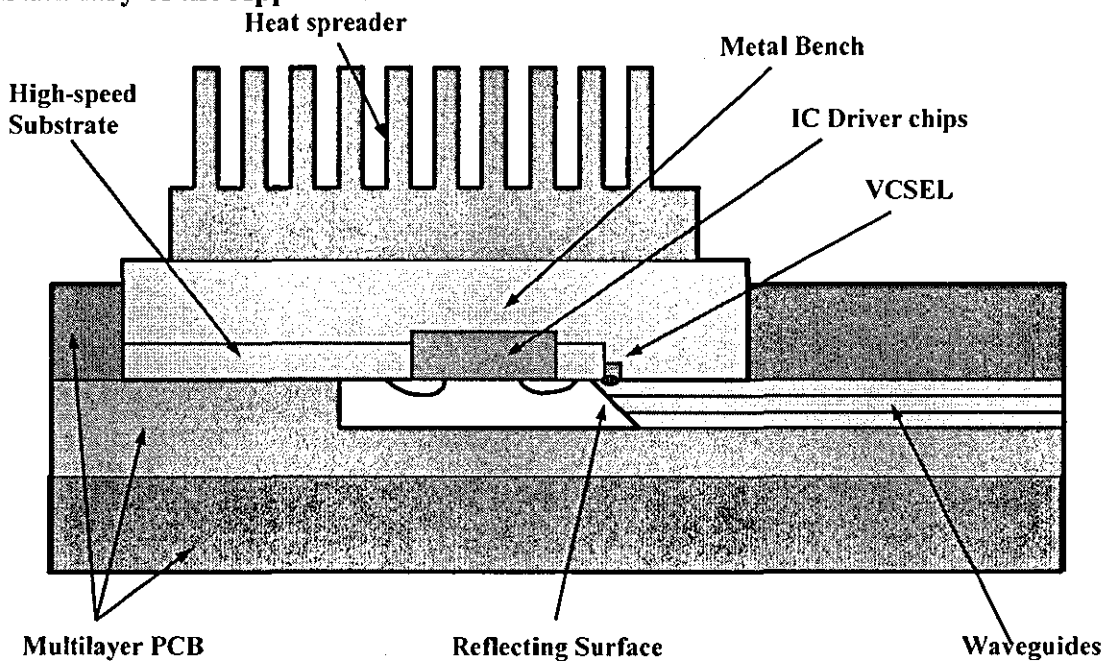
According to the invention; waveguides are contained in an optical layer of a printed circuit board. The waveguides are manufactured using an embossing process. The embossing process forms reflective ends that emit light in a perpendicular direction to the waveguides. The embossed substrate contains mechanical guide marks, such as guide holes for MT pins, for positioning optical components.

Comparison to OECB Invention

Field	Patent relates to OECB fabrication and coupling.
Related Art	Reflective ends are fabricated using an embossing process which is not compatible with all OECB fabrication methods.

7] Electro-Optical Circuit Board Having Optical Transmit / Receive Module and Optical Waveguide			
Applicant			
Patent Number	US2004037512	**Publication Date**	2004-02-26
IPC Classification	G02B6/42; G02B6/12		

Summary of the Application



The patent details embodiments of a design for creating optical interconnects between chips and daughter cards housed on a mother board by first forming an Electro-Optical Circuit Board (EOCB). The EOCB contains waveguides sandwiched between

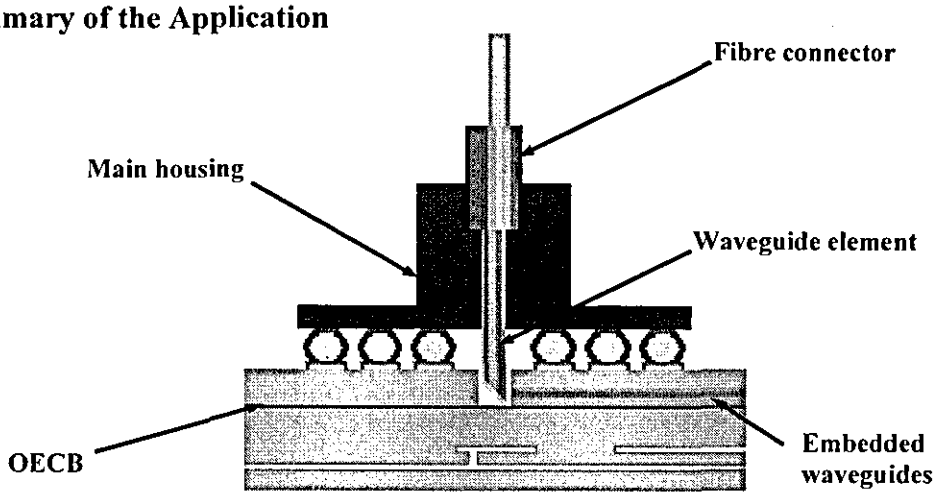
the layers of a PCB and operates by coupling the output light from a VCSEL into the waveguides. The patent improves on prior art in this area by simultaneously reducing the cost of the assembly by replacing the Silicon Optical Bench (SIOB) with a metal bench which contains alignment features which also solves some of the alignment issues. The metal bench contains a trench in which the VCSEL drivers are inserted. These ICs are then wire-bonded to connection pads on the bench and VCSEL. The housing is then assembled onto the EOCB facilitating the electrical connections between the PCB and driver ICs. The VCSEL outputs light downward, in a perpendicular direction to the waveguides, with the light coupling into the core of the waveguide by routing off a reflecting surface. The reflecting surface is angled at 45° and can be flat or curved; it is also plated with gold. The waveguides are formed using a hot-embossing process and are laminated between the layers of the PCB.

Comparison to OECB Invention

Field	Patent relates to manufacturing a method for optically interconnecting IC chips on boards and also between daughter cards across a backplane.
Related Art	Patent includes mention of a 45° metallised facet although there is no mention of how this is to be fabricated.

8] Connection to optical backplane			
Applicant	Terahertz Photonics		
Patent Number	W02004010191	**Publication Date**	2004-01-29
IPC Classification	G02b6/43; G02B6/42		

Summary of the Application



The patent describes a method for achieving the optical coupling between an optical connector and waveguides embedded within an optically enabled PCB. A trench is formed in the PCB substrate to expose the waveguide facets. An optical element comprised of a waveguide section with a polished and coated 45° angled reflector on one end. The waveguide element is held by a main body, which contains alignment marks and fixings for a fibre ferule. The main body of the connector is assembled onto the optically enabled substrate using standard PCB assembly methods. The positioning of the waveguide element and 45° mirrors is such that light couples between the waveguide cores on the inserted element and those embedded within the substrate.

Comparison to OECB Invention	
Field	Patent relates to coupling optical components to OECBs
Related Art	Patent details a method for achieving optical coupling through an integrated mirror approach.

9] Optical high speed bus for a modular computer network			
Applicant	Raytheon Cp (US)		
Patent Number	US6650808	**Publication Date**	2003-11-18
IPC Classification	G02B6/28		

Summary of the Application

The patent describes a method for providing a bus module capable of providing mechanical, electrical, optical, and power interface for individual circuit cards in a backplane architecture. The optical interface is comprised of paired VCSEL / PD arrays that pass data to each other over free space.

Comparison to OECB Invention	
Field	Optical backplanes (free space)
Related Art	None relevant

10] Passive alignment connection for fibre optical incorporating VCSEL emitters			
Applicant			
Patent Number	US2003210873	**Publication Date**	2003-11-13
IPC Classification	G02B6/43		

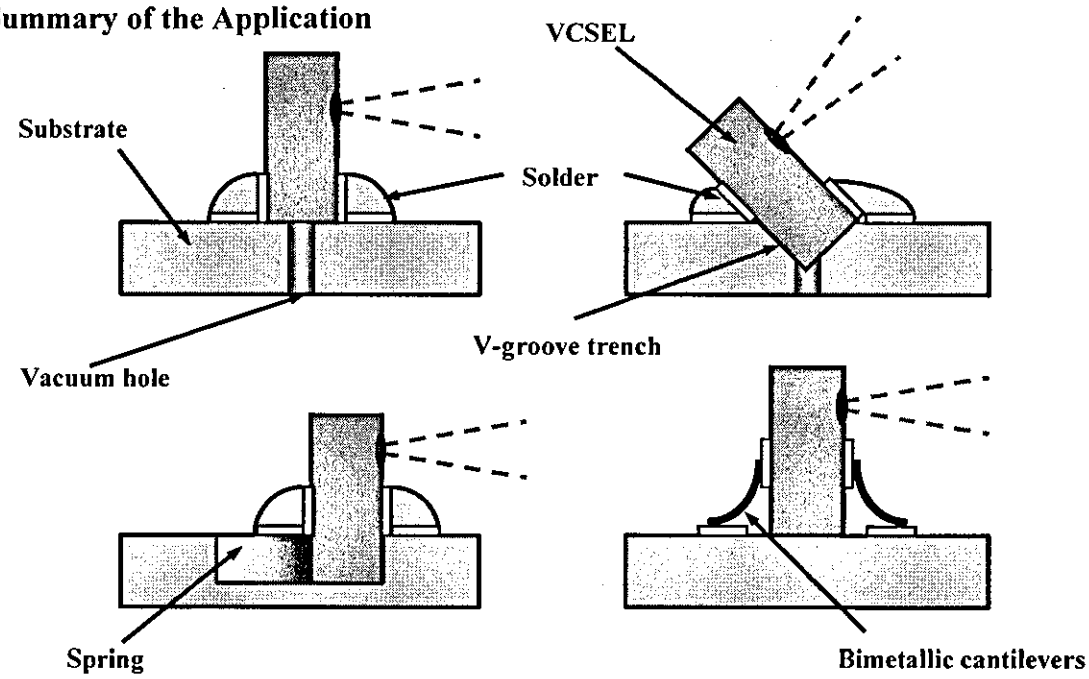
Summary of the Application

The patent details a method for achieving passive alignment between an optical fibre and a VCSEL array. In order to achieve the precise alignment between the ribbon fibre and VCSEL array, necessary to ensure there is minimum losses across all the connection locations, alignment pins are used. The alignment pins protrude from the mating connector ferrule housing the VCSEL array and insert into holes in the fibre connector ferrule. This improves on prior art such as: active alignment, which although reliable is expensive, time consuming, and complicated when aligning arrays, v-shaped grooves precisely etched in a substrate, which are not applicable to VCSELs that emit light perpendicular to the v-grooves, and fibres angled at 45°, polished, and gold plated to provide a mirror system to couple into the fibre when offered to the VCSEL in a v-groove.

Comparison to OECB Invention	
Field	Relates to manufacture of a component not a circuit board.
Related Art	None relevant, although may be applicable when coupling fibre to the surface of the OECB.

11] Integration and alignment of VCSELs with MEMS using micro-machining and flip-chip techniques			
Applicant	Xerox Corp (US)		
Patent Number	US6647036	**Publication Date**	2003-11-11
IPC Classification	H01S3/04; H01S3/00; H01L23/02; H01L29/40		

Summary of the Application



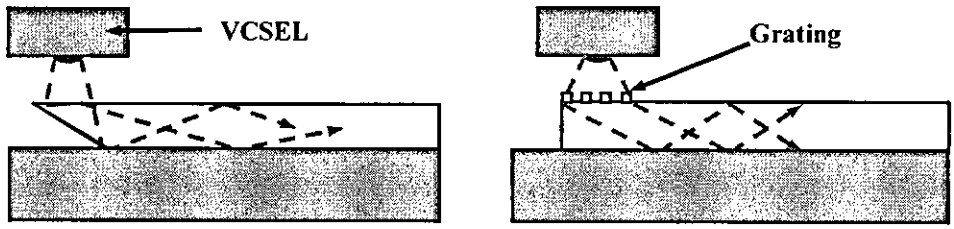
The patent describes various embodiments of a method for aligning a laser (e.g. VCSEL) onto a wafer substrate. The method allows the VCSEL to emit the beam non parallel to the substrate surface. This provides the advantage of being able to couple the beam to other components to scan the beam out-of-plane to the substrate. The first embodiment forms precisely located bond pads on the top surface of the wafer. A vacuum hole is etched so as when a VCSEL is placed upright on the wafer a vacuum can be applied to hold the VCSEL in place. During reflow, solder alignment forces refine the alignment of the VCSEL. The bond pads and solder joints can also form electrical connection to the VCSEL. The second embodiment alters slightly from the first, forming a v-groove trench in the substrate through standard lithographic etching techniques. A vacuum hole is still etched and a similar reflow process finely locates and permanently fixes the VCSEL at an angle to the substrate. A further embodiment removes the need for a vacuum hole and process steps by forming a spring mechanism by known lithographic techniques. The spring holds the VCSEL in place before reflow. A final embodiment forms coupled bimetallic cantilevers on the top of the substrate that curl up due to a natural stress gradient.

Comparison to OECB Invention

Field	Patent relates to assembling a VCSEL onto a substrate.
Related Art	Not relevant to OECB manufacture.

12]Integrated optoelectrical circuit package with optical waveguide interconnects			
Applicant	Intel Corp (US)		
Patent Number	US2003185484	**Publication Date**	2003-10-02
IPC Classification	G02B6/12; G02B6/43		

Summary of the Application



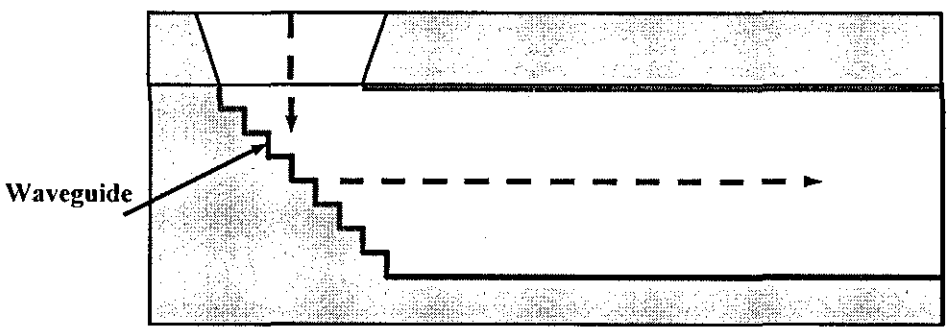
Two embodiments are disclosed for coupling between surface mounted components and waveguides. No specific manufacturing technology is discussed.

Comparison to OECB Invention

Field	Coupling between components and waveguides.
Related Art	Undercut mirror is evident although no details of the fabrication process are defined.

13] Optical clocking distribution using diffractive metal mirrors and metal via waveguides			
Applicant	Intel Corp. (US)		
Patent Number	US6351576	**Publication Date**	2002-02-26
IPC Classification	G02B6/12; G06F1/04		

Summary of the Application

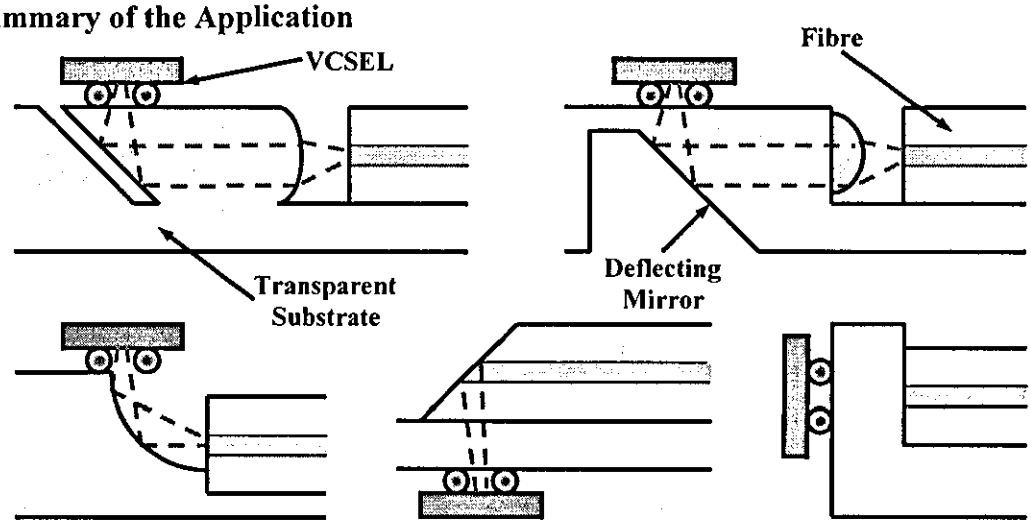


The patent describes a process for creating waveguide structures in substrates (typically wafers) and including a light reflecting structure at the ends of the waveguides. A through-substrate trench forms a light path through to the waveguides. A diffractive metal mirror is formed by a series of metalisations at the ends of the wageuides to deflect light through an angle of 90°. Light can be coupled between optical components and the waveguides defined within the substrate.

Comparison to OECB Invention	
Field	Patent relates to the optical coupling through 90o of optical components and surface planar waveguides.
Related Art	Invention is predominantly focussed on wafer substrates and fabrication processes and methods.

14] Integrated Platform for Passive Optical Alignment of Semiconductor Device with Optical Fibre			
Applicant	Hong Kong Applied Science Technology Centre		
Patent Number	WO03077001	**Publication Date**	2003-09-18
IPC Classification	G02B6/42		

Summary of the Application



The patent describes a method for manufacturing a component, which couples light from a transmitter (such as a VCSEL) into an optical fibre with reduced alignment tolerances through its integrated features. The main structure of the assembly is given by the transparent substrate, fabricated from glass or other high temperature polymer using process such as transfer moulding, injection moulding, or high precision grinding. The VCSELs are attached to the transparent substrate using flip chip processes, with the bond pads being coated on top, using various metallic deposition processes. The transparent substrate incorporates a reflective slanted sidewall to change the direction of the light. The slanted reflective sidewall would nominally be 45° although other angles are possible including a curved wall. The reflected light travels through the transparent substrate and is focussed into a fibre core through a lens array. The lens array can either be formed as part of the substrate or assembled separately. Fibres are fixed in place using v-grooves.

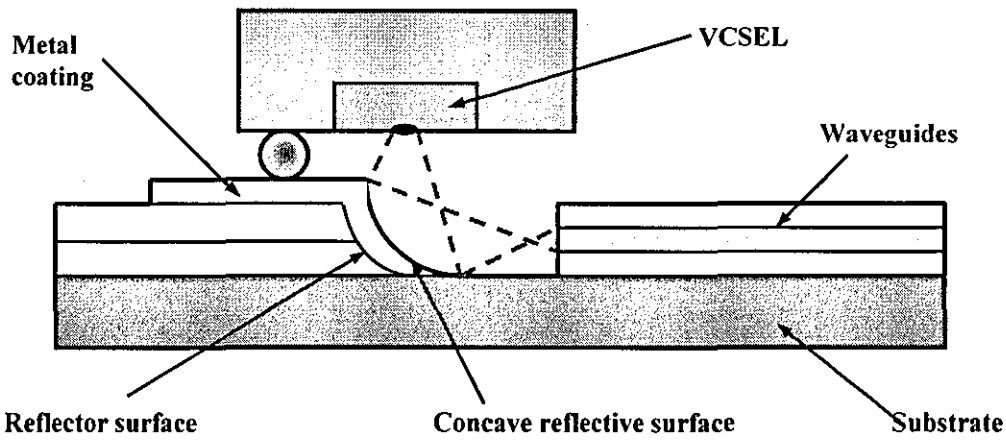
Comparison to OECB Invention	
Field	Patent relates to manufacturing a component, not a circuit board, and couples light into fibres not waveguides.
Related Art	Patent relates to light transmission through a substrate, no mention of waveguides or changing the direction of the light. Patent includes mention of a reflective slanting surface, although

no mention of how it is to be made reflective. Also contains no indication that the slanted wall is to be coated. Patent describes the manufacture of a reflective wall in a transparent substrate, which isn't applicable to the OECB.

15] Device for introducing light into a waveguide, device for emitting light from a waveguide and method for manufacturing such devices

Applicant	Lionix B V (NL)		
Patent Number	WO03056374	**Publication Date**	2003-07-10
IPC Classification	G02B6/42		

Summary of the Application



The invention relates to a device for coupling light between SMT assembled devices (e.g. VCSEL and PD) and planar waveguides. This is achieved by forming a reflector which is at least partially concave. This improves the coupling efficencey compared to prior art that employs flat mirrors since when flat mirrors are employed the divergent beam is diverged yet further during reflection, allowing only a portion of the energy to be coupled. The reflecting surface can be for instance be anisotropically etched at an angle to the main direction of the waveguide, or be built up for instance from a number of facets in an angular curved form. The formed reflecting surface is improved yet further by coating the surface with a metal layer, giving the reflecting surface a larger reflection coefficient. The metal layer can also form an electrode for the electrical connection to the active devices.

Comparison to OECB Invention

Field	The patent relates to a device for coupling SMT assembled active components to waveguides on the top surface of the substrate. Although nominally a wafer, it is within the scope of the claims to extend the substrate to PCBs.
Related Art	The patent describes the fabrication of a concave mirror on the second surface of a formed channel. The surface is coated with metal to form the reflective surface.

16] Process for efficient light extraction from light emitting chips			
Applicant			
Patent Number	US2003124754	**Publication Date**	2003-07-03
IPC Classification	H01L21/00		

Summary of the Application

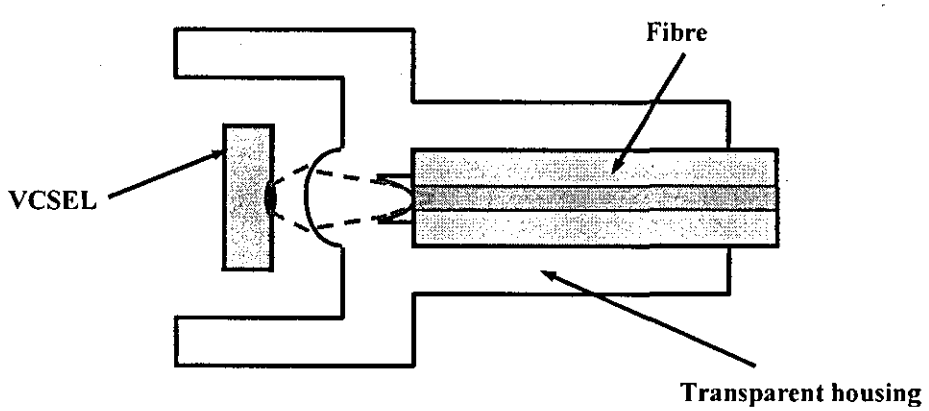
The patent relates to the fabrication of devices in order to more efficiently extract light from light emitting devices (e.g. VCSELs) contained on a suitable substrate (e.g. wafer). The patent describes a unique way to pattern an optical microstructure immediately on top of a mass produced wafer. The microstructure is built up on top of the active device by coating layers of spun-on-glass (SOG) onto the wafer to form a mirror shape. Metal is evaporated over the mirror. The addition of a microlens can increase the coupling efficiency to fibres or waveguides. This technique greatly improves the light-emission efficiency of active devices by reflecting any light lost out of the sides of the semiconductor material.

Comparison to OECB Invention

Field	Relates directly to VCSEL manufacture at wafer level.
Related Art	Metal evaporated coated to aid mirror fabrication.

17] Optical coupling for optical fibres			
Applicant			
Patent Number	US2003118282	**Publication Date**	2003-06-26
IPC Classification	G02B6/32; G02B6/26		

Summary of the Application

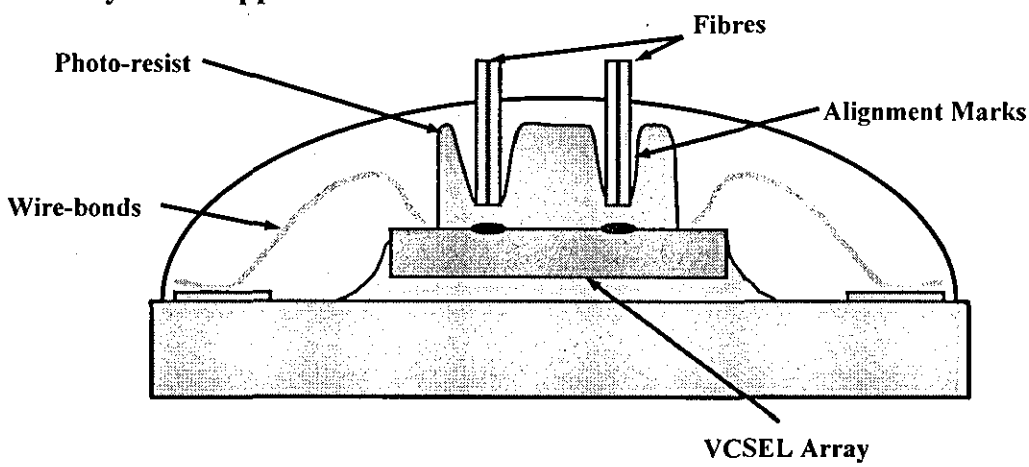


The patent describes a method and system for coupling a laser (e.g. VCSEL) to an optical fibre. The VCSEL beam is focussed on a fibre facet to improve coupling efficiency and repeatability. The optical models can be scrambled utilising an optical scattering surface. Two different approaches for the arrangement of concentrators and lens' are shown with the housing being moulded to contain all the components necessary to couple to the optical fibre. The housing therefore needs to be transparent.

Comparison to OECB Patent Application	
Field	Patent relates to assembling a VCSEL onto a substrate.
Related Art	Not relevant to OECB manufacture, although may be adaptable for creating edge connectors for connecting fibre to the edges of the OECB.

18] Passive alignment microstructures for electro-optical devices			
Applicant	CSEM (Switzerland)		
Patent Number	0118511.5	**Publication Date**	2003-05-02
IPC Classification	G02B 6/42		

Summary of the Application

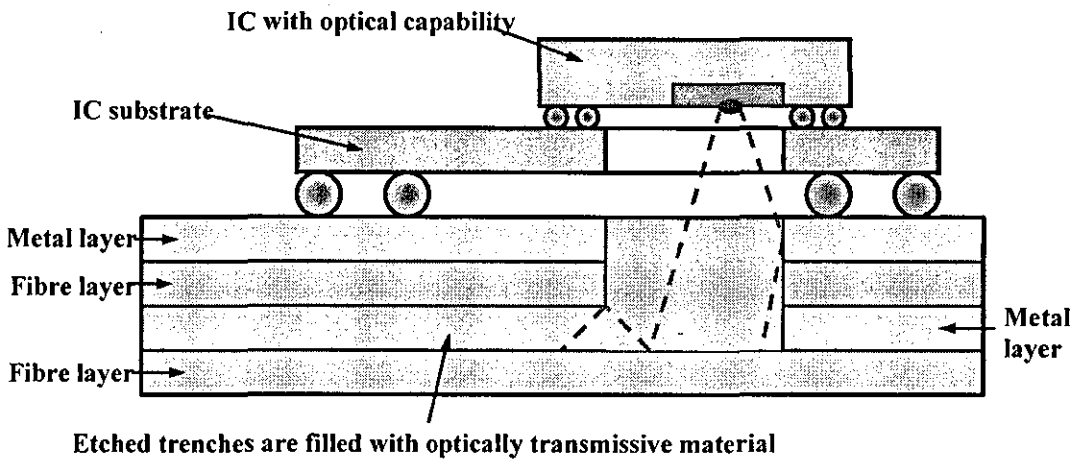


The patent relates to the integration and packaging of opto-electronic components and optical Microsystems. It describes the fabrication of continuous relief, round-edged micro-lithographic structures that act as alignment grooves and openings. They are formed by exposing and developing a photo-resist layer formed over a substrate. The edges of the alignment marks are rounded by subjecting the photo-resist layer to an extreme bake at elevated temperatures which cause the photo-resist to reflow. The method improves on prior art, such as etching v-grooves in glass or silicon substrates, by removing the time consuming and costly techniques associated. The design also allows the alignment of components orientated vertically to a wafer or device plane.

Comparison to OECB Invention	
Field	Patent relates to assembling a device onto a substrate and additionally aligning fibre to the top of the device.
Related Art	Not relevant to OECB manufacture.

19] Optically Interconnecting Integrated Circuit Chips			
Applicant			
Patent Number	US2003007745	**Publication Date**	2003-01-09
IPC Classification	G02B6/42; G02B6/12		

Summary of the Application



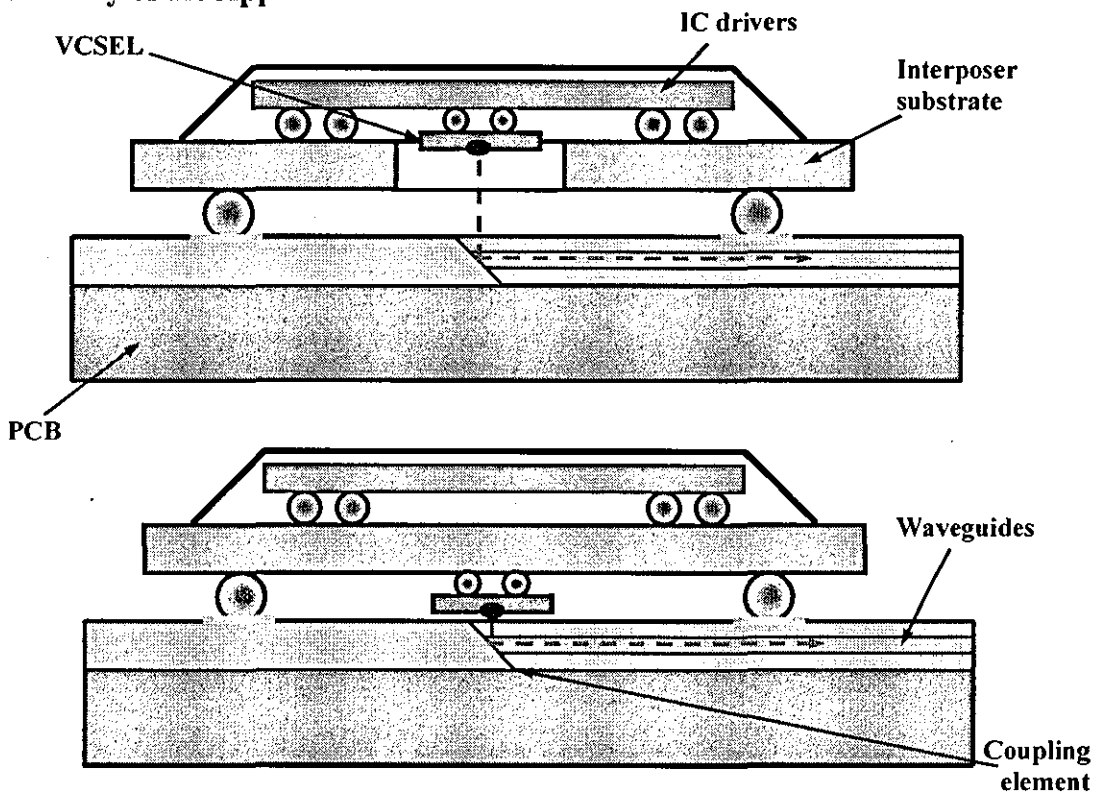
The patent describes embodiments of a method for optically coupling components (eg. VCSELs) mounted on PCBs. The components are assembled through standard techniques so as the active area is directed towards the board's surface. An optical waveguide path is formed by creating a path through the PCB to the ends of the waveguides and then filled with an optically transmissive material. The patent also describes a novel method for the fabrication of waveguides by etching 'waveguide circuitry' in copper layers. The channels are then filled with an optically transmissive material. The patent makes the statement that 'in some embodiments, the optical coupling is achieved without the need for components such as mirrors and other light directing components.

Comparison to OECB Invention

Field	Patent relates to the out-of-plane optical coupling between board level integrated waveguides and surface mounted components
Related Art	Out-of-plane coupling is achieved by creating and filling tracks and vias with optically transmissive materials. There is no mention of the use of mirrors in achieving the change in direction.

20] Flip-chip Package Integrating Optical and Electrical Devices and Coupling to a Waveguide on a Board			
Applicant			
Patent Number	US2003002770	**Publication Date**	2003-01-02
IPC Classification	G02B6/12		

Summary of the Application



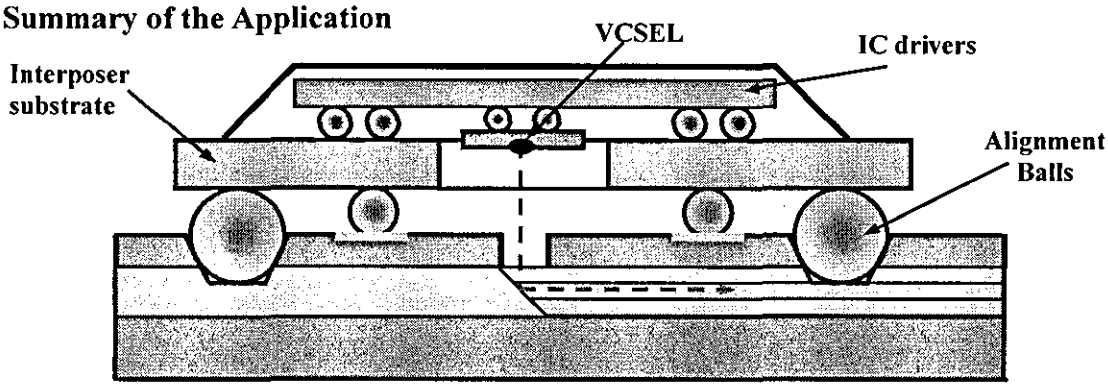
This patent is a continuation of previous patent, number US2002196997 (Packaging and assembly method for optical coupling). It improves on the prior art by removing the need for alignment to holographic elements in the PCB, thus reducing the alignment specification. All the embodiments of the design are concerned with the formation of an optical assembly where the active devices (eg. VCSELs) are flip-chip / wire-bonded to an interposer substrate in close proximity to the driver circuit ICs. The substrate is then balled to allow BGA assembly to the PCB. Optical coupling is enhanced by the addition of lenses in the assembly

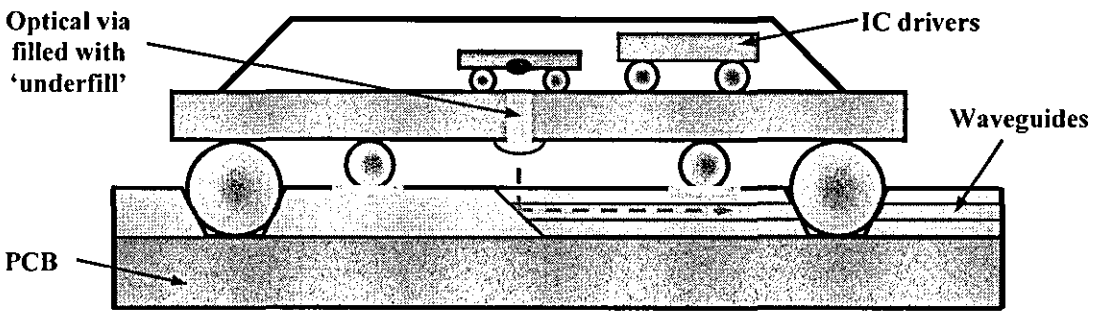
Comparison to OECB Invention

Field	Patent relates to manufacturing a component not a circuit board.
Related Art	Patent refers to 'coupling elements' that may be holographic elements or 45° facets incorporated in to the waveguides. However, there is no mention of how these are to be formed or fabricated.

21] Packaging and Assembly Method for Optical Coupling			
Applicant			
Patent Number	US2002196997	**Publication Date**	2002-12-26
IPC Classification	G02B6/12; G02B6/26; G02B6/30		

Summary of the Application





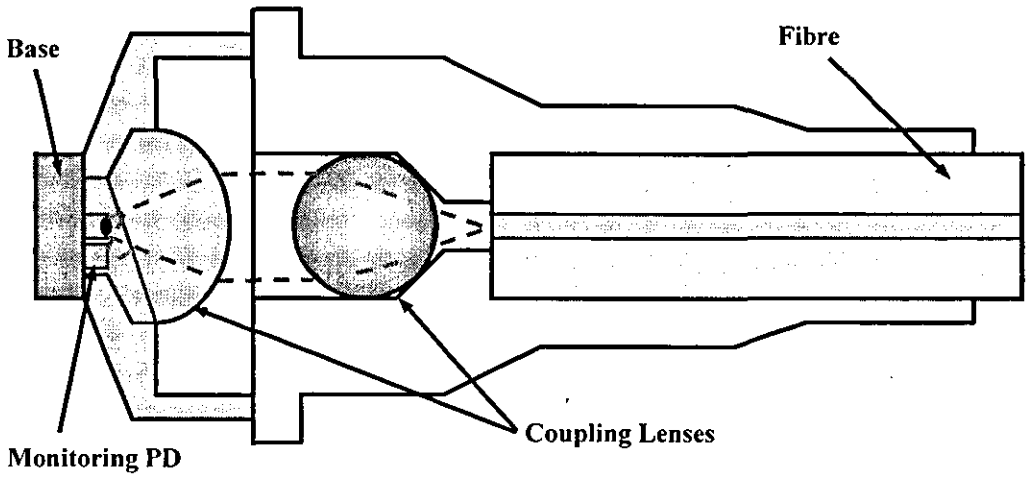
The patent describes embodiments of a method for both optically and electrically coupling between one or more integrated circuits and a PCB. The patent is concerned with manufacturing an interposer assembly to act as a re-distribution layer so as to remove the ultra-small pads from the PCB fabrication process. The interposer is typically a BGA assembly, aligned to the PCB using both mechanically positioned alignment balls or rails and also solder reflow technology. The basic embodiment consists of an active device (eg. VCSEL or PD) that is bonded to a substrate. To reduce the interference, the chips that form the driver circuitry are assembled in close proximity to the active devices, either side by side on the interposer substrate or by directly bonding the active device on top of the driver ICs. The active devices can either be surface or bottom side emitting / receiving and are flip-chip / wire-bonded to the substrate / top side of the IC. It is understood that the light coupling between the waveguides and components will be achieved by laminating 45° facetted waveguides to the PCB or by depositing waveguides directly over holographic elements.

Comparison to OECB Invention

Field	Patent relates to manufacturing a component not a circuit board.
	Patent includes mention of an interposer, optical underfill, and bottom emitting flip-chip VCSELs etc. Also contains claims for alignment of assembly to waveguides in PCBs.
Related Art	Claims are related to assembling components to PCBs which include waveguides with 45° facets although there is nothing specific to the actual manufacture of these waveguides or facets.

22] Optical device			
Applicant			
Patent Number	US2002181903	**Publication Date**	2002-12-05
IPC Classification	G02B6/42		

Summary of the Application



The patent describes a method for optically interconnecting a VCSEL element with an optical fibre. The assembly comprises a base member containing a VCSEL device situated in a recess and filled with a transparent filler. This is attached to a receptacle for receiving an optical fibre. A lens is included to improve the coupling efficiency and methods for tapping the output for monitoring purposes are also included.

Comparison to OECB Invention

Field	Patent relates to manufacturing a component not a circuit board.
Related Art	Not relevant to OECB manufacture, although may be applicable for creating edge connectors for optically connecting fibre to the edges of the OECB.

23] PCB embedded and surface mounted optical distribution systems			
Applicant			
Patent Number	US2002141163	**Publication Date**	2002-10-03
IPC Classification	H05K1/00; H05K1/18		

Summary of the Application

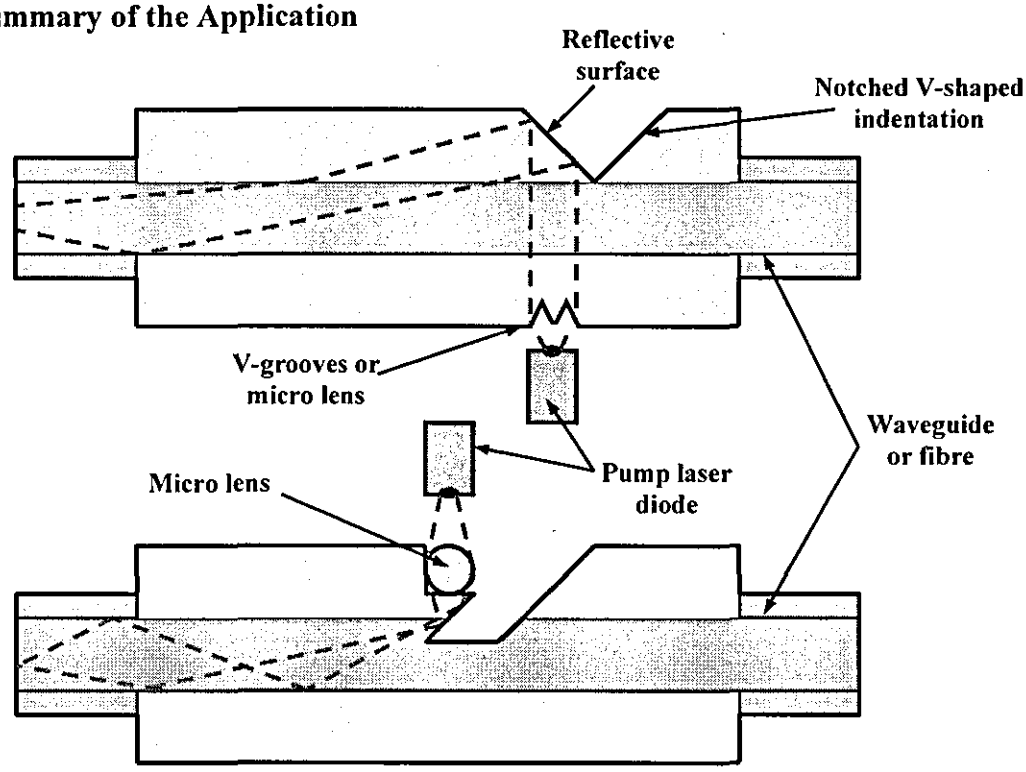
The patent protects a system of both embedding a pre fabricated one dimensional plane of optical fibres into a PCB and also a method of coupling the light between the ends of the PCB integrated fibres or waveguides into optical vias. The optical vias are at 90° to the waveguides or fibres. Static mirrors, MEMS mirrors (still and dynamic), or equivalent steering devices facilitate the 90° change in direction of the light.

Comparison to OECB Invention

Field	Coupling between SMT devices and planar waveguides.
Related Art	No mention of how the steering mirrors are to be fabricated.

24] Apparatus for coupling light into an optical waveguide			
Applicant	CIDRA Corporation (US)		
Patent Number	WO02075402	**Publication Date**	2002-09-26
IPC Classification	G02B6/28; G02B6/42; H01S3/094		

Summary of the Application



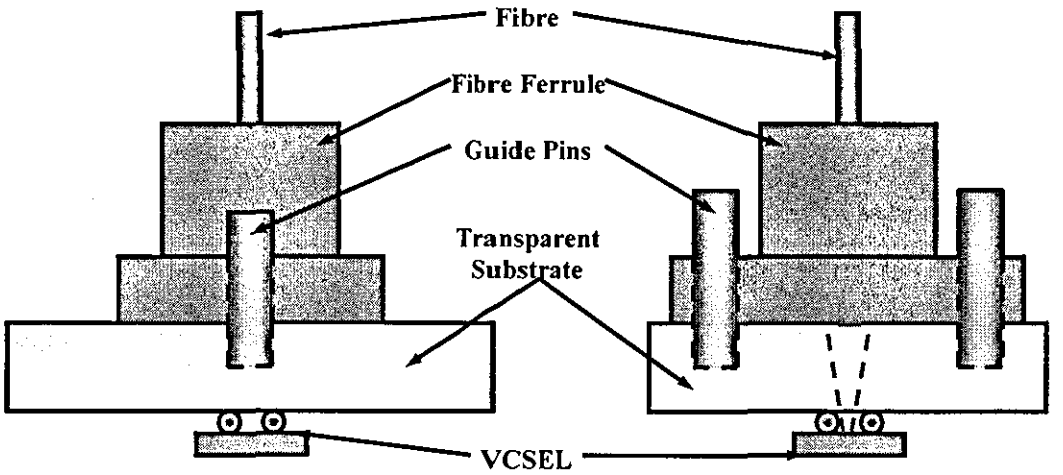
The patent contains various methods for providing an optical coupling device for coupling pump light into an optical waveguide or fibre. The aim of the invention is to improve the manufacturability and reliability of previous patents covering the manufacture of optical amplifiers, specifically to overcome both the need for the light to travel through the core of the waveguide before coupling into the cladding and the reliance on highly reflective surfaces, which are difficult to achieve on such small scales. The basis of the design has an optical source emitting light through a lens. The light is coupled into the waveguide cladding off a reflective surface. This surface may be either a notched surface of a V-shaped indentation or a cleaved end. The reflective surface may include a coated surface to enhance reflectivity.

Comparison to OECB Invention

Field	Although aimed at the manufacture of optical amplifiers the claims can easily be applied to the manufacture of board level optical interconnects.
Related Art	The patent relies on a reflective surface for coupling the light into the waveguide. Other than the mention that the surface is coated, there is no mention of how this structure is to be formed.

25] Active Optical Device			
Applicant	Zarlink Semiconductor		
Patent Number	US2002117679	**Publication Date**	2002-08-29
IPC Classification	H01L21/00; H01133/00; H01L29/40		

Summary of the Application



The patent describes a method for coupling VCSELs to fibre, with all the components mounted onto one substrate. VCSELs are mounted on one side of a glass substrate patterned using a conventional photolithographic technique to provide electrical connection to driver circuitry and fan out connections. Standard fibre ferrules (similar to MT types) are attached to the underside of the substrate, locating on guide pins that are precisely assembled to the substrate as part of the proposed manufacturing process. The bottom emitting VCSELs transmit light through the transparent substrate where the output is coupled into the attached fibre. The VCSELs are assembled using a flip chip process, which utilises solder alignment techniques to achieve the precise alignment.

Comparison to OECB Invention

Field	Patent relates to manufacturing a component not circuit board and also relates to coupling light into fibres not waveguides.
Related Art	Patent relates to light transmission through a substrate, no mention of waveguides or changing the direction of the light. Patent does include flip chip bonding of VCSELs (and similar devices) to a substrate with light emitting into the substrate, although this is not considered a protected technique as this is a widely used process. It is also not considered a problem as the flip chip bonding does not form part of the OECB patent.

26] Packaging system for two-dimensional optoelectronic arrays			
Applicant			
Patent Number	US2002104959	**Publication Date**	2002-08-08
IPC Classification	G01J1/04		

Summary of the Application

The patent describes a method for integrating active devices (e.g. VCSEL / PD) into a component, which allows opto-electronic connectivity to an optical fibre. In order to address the data capacity increase between ICs; from one chip to another, from one IC board to another, and from system to system. Prior art exists although does not address the interconnection to an industry standard connector. In embodiments of the patent, active devices couple light into flexible waveguide sheets that distribute the signal to the edge of the package for interconnection with MT style fibre connectors.

Comparison to OECB Invention

Field	Patent relates to manufacturing a component not a circuit board.
Related Art	None relevant.

27] Optical interconnection circuit board and manufacturing method thereof			
Applicant			
Patent Number	US2002039475	**Publication Date**	2002-04-04
IPC Classification	G02B6/10; G02B6/12; G02B6/26		

Summary of the Application

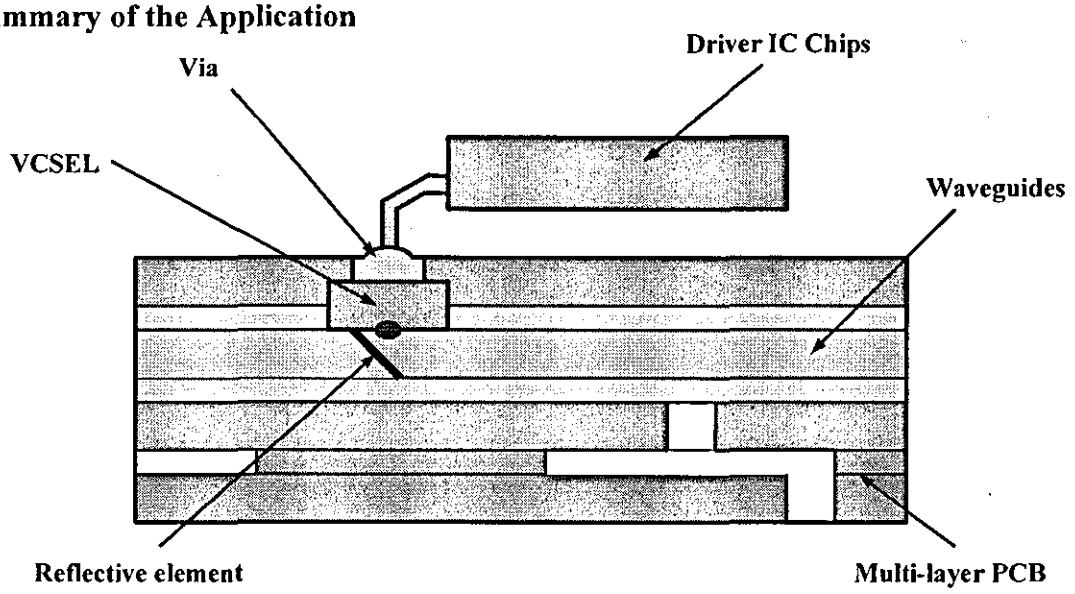
The patent describes the manufacture of a termination mirror which has a reflecting face and is buried in the cladding layer in order to reflect the optical signal guided in the core layer. The termination mirror is formed by one of two alternative methods. The first method buries either a reflecting material to form a mirror or a high refractive material to form a prim into the optical waveguide core. The second method forms a method by placing a spacer in the optical waveguide core and removed to form a cavity. The angled cavity can then be filled with air or an inert gas to form a reflecting surface.

Comparison to OECB Invention

Field	Out-of-plane optical coupling
Related Art	Patent describes a method for creating mirrors by backfilling a cavity with a gas.

28] Packaging enhanced board level opto-electronic interconnects			
Applicant	University of Texas (US)		
Patent Number	US6243509	**Publication Date**	2001-06-05
IPC Classification	G02B6/12		

Summary of the Application



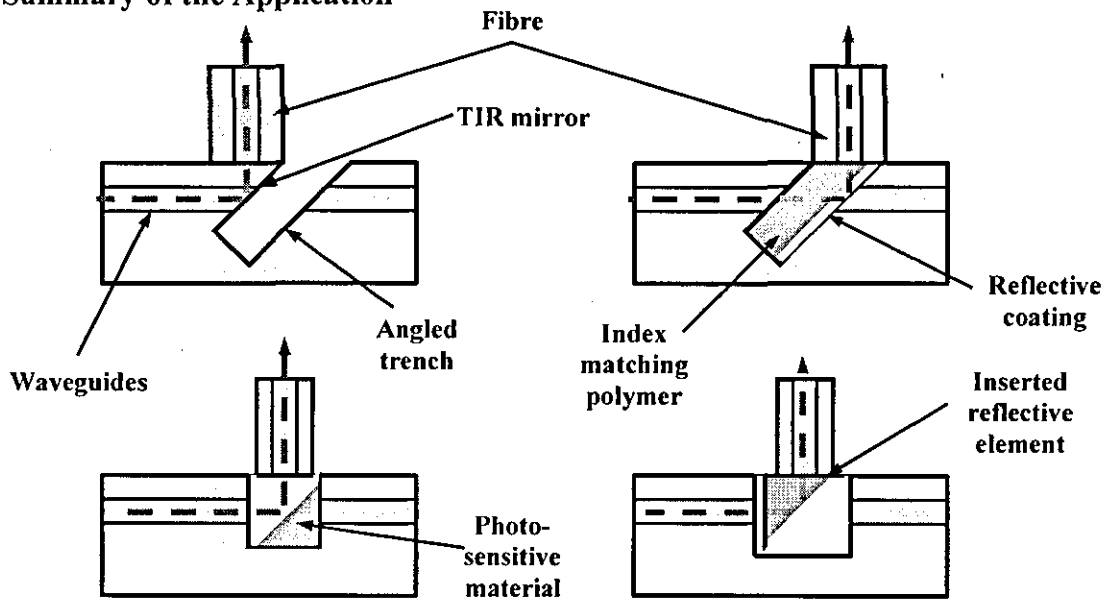
The patent details embodiments of a system which provides opto-electrical signal communications that are fully embedded within a PCB or MCM substrate. The system is aimed at relieving current speed, power distribution, packaging, and fan-out limits of electrical interconnect. The patent improves on prior art that has the active devices (e.g. VCSEL and PD) mounted on the top of the substrate transmitting optical energy through several dielectric materials, which inefficiently couple the energy into the waveguide. This improvement is achieved by forming the active devices within the PCB structure. Driver IC chips are still SMT mounted on the top of the board interfacing with the active devices through blind vias. By embedding the active devices so as they directly adjoin the waveguide channels it is hoped to achieve enhanced electro-optical coupling efficiency. The light signals are coupled into the core of the waveguide via reflective elements comprised of any suitable structure. Whilst mirror structures may be utilised the preferred method is to employ tilted waveguide gratings. Such gratings may be fabricated with known micro-fabrication processes; rendering them mass-producible with excellent accuracy and reproducibility. As an example, such a grating coupler may be fabricated by RIE.

Comparison to OECB Invention

Field	Patent relates to manufacturing a method for optically interconnecting IC chips on boards and also between daughter cards across a backplane.
Related Art	Patent includes the use of reflective elements. Although the preferred method is to employ gratings, mirror structures are included. However, there is no mention of how structures would be fabricated.

29] Reflective coupling array for optical waveguide			
Applicant	Corning Inc. (US)		
Patent Number	WO9830925	**Publication Date**	1998-07-16
IPC Classification	G02B6/26		

Summary of the Application



The patent makes a contribution to the field of optical communications and especially to coupling fibre with devices that separate the wavelengths. Whilst a significant proportion of the patent relates to achieving the functions necessary for the light de-multiplexing, a large area of the patent relates to the coupling of light from a fibre through 90° into a planar waveguide. As such, the patent describes various embodiments of a method for achieving this out-of-plane coupling. One design is based on forming an angled cavity by masking and RIE. Once formed the light can either reflect of the 1st surface using TIR, or of the 2nd, which would be coated with a reflective material. In this approach the cavity is filled with an index matching polymer, to prevent reflections from the side wall caused by index differences between the core layer and the cavity. An alternative design is centred on a conventional square cavity. This would then be filled either with a photo-curable material and cured so as to create an inclined surface that can then be coated or it can be filled with a photo-sensitive material and cured so as to create a holographic grating. Final embodiment is concerned with inserting reflective components into the cavity.

Comparison to OECB Invention

Field	Not specifically aimed at optical interconnects between boards and chips, but the out-of-plane coupling is relevant.
Related Art	The patent describes methods for creating TIR mirrors as well as coating the open surface and using this to create the mirror. Also contains methods for creating mirrors using photo-sensitive materials or inserting components.

30] Waveguide optical deflector, process for producing the same, and saw blade for use in this process			
Applicant			
Patent Number	EP0822430	**Publication Date**	1998-02-04
IPC Classification	G02B6/42; G02B6/12		

Summary of the Application

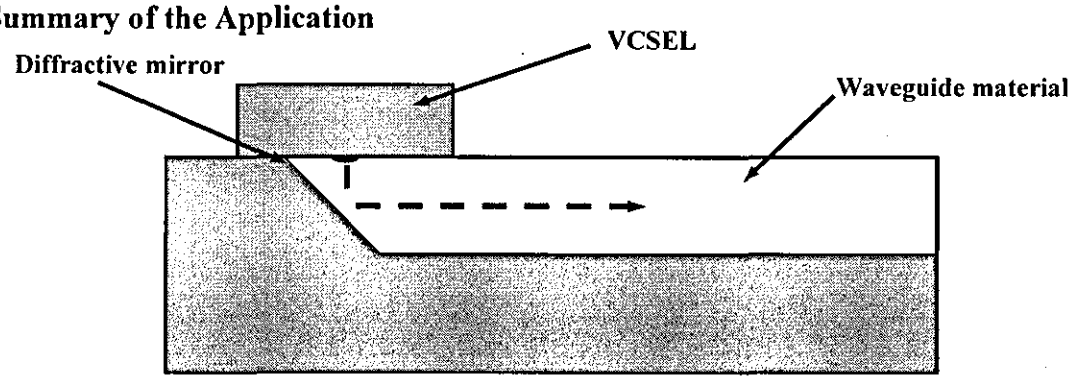
The patent details embodiments of a method to produce mirrors on the ends of waveguides using a circular saw and the required apparatus. Waveguides are formed on the top surface of a substrate. A bevelled saw makes a v cut in the waveguides down to the top of the substrate. The angled end face can be metallised for example by vacuum deposition. The waveguide is removed from the substrate for integration.

Comparison to OECB Invention

Field	Out-of-plane coupling from waveguides
Related Art	Technology uses wafer saw and produces the angled from the top.

31] Method for fabrication of mirrors in integrated optical waveguides			
Applicant	Bosch GMBH Robert (DE)		
Patent Number	EP0816878	**Publication Date**	1998-01-07
IPC Classification	G02B6/12		

Summary of the Application



The patent details a method for producing an optical waveguide with a reflector for coupling between surface mounted devices. The waveguides are manufactured by forming a trench in the substrate and filling the recess with a waveguide material. Reflectors are formed by creating an angled surface and coating a high-melting point metal layer prior to covering with the waveguide material.

Comparison to OECB Invention

Field	Relates to coupling between components and waveguides
Related Art	Mirrors are formed using similar methods to embossed mirrors and are not compatible with all OECB applications.

32] Optical module having a reflective optical waveguide			
Applicant	Motorola Inc (US)		
Patent Number	EP0652454	**Publication Date**	1995-05-10
IPC Classification	G02B6/42; B29D11/00		

Summary of the Application

The patent describes a method for creating optically enabled circuit board architectures by moulding waveguides and bonding them into a substrate. The waveguides have moulded termination surfaces that have an angle to reflect light at 90o to the waveguides. The termination surfaces can be coated with a reflective metal using deposition, evaporation, sputtering, or alike processes.

Comparison to OECB Invention

Field	Out-of-plane coupling from planar waveguides.
Related Art	None specific.

33] Fabrication of cooled faceplate segmented aperture mirrors (SAM) by electroforming			
Applicant	US Airforce (US)		
Patent Number	US4740276	**Publication Date**	1988-04-26
IPC Classification	C25D1/06		

Summary of the Application

An electroforming method is described for making a cooled SAM suitable for use with high energy laser irradiation. Electroforming is used to fabricate a continuous faceplate having a surface shape of the desired array. Electroforming is a variation of electroplating involving the formation of a removable layer of metal, which conforms exactly to the surface shape of the master. Electroforming of optical surfaces requires control of bath and plating parameters to limit the spring-back of the electroform. Electroformed optics are generally thin (less than 0.100") so require rigidisation but are capable of providing optical quality cooled surfaces. The method comprises steps of providing a master, electroforming a negative faceplate on the master, bonding a first substrate to the back of the negative faceplate, separating the faceplate from the master, electroforming a positive faceplate over the negative, forming coolant channels, electrodepositing further additional layers of material on the back to enclose channels and to connect manifolds in place for the surface cooling.

Comparison to OECB Invention

Field	Patent relates to manufacturing an electroformed mirror.
Related Art	None relevant.

Appendix B
DSC Analysis of Optical Adhesives

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Ablelux Adhesives

Evaluation of kinetics of curing (secondary thermal cure mechanism) by DSC

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Test methods

Instrument : DSC-7 Perkin Elmer
Sample holder : Al, 30 microliters , Atmosphere: nitrogen 99.99 % pure.
Sampling : liquid adhesive from syringes .
Sample size : around 10 – 20 mg

- **Determining the optimum curing Temperature :**

Scan from 40 to 180 °C
Scanning rate : 6 °C / minute
Record the curve and get the 1st derivative peak temperature of the heat-flow curve peak
(Estimated uncertainly of measurement : 2 °C)

- **Determining the optimum curing time :**

Ramp at 30 °C/minute, to reach the optimum temperature as mentioned above, than isothermal
Plot the % area curve and get the time (excluding ramp time) for 100 % curing
(Estimated uncertainly of measurement : 10 % of measured time)

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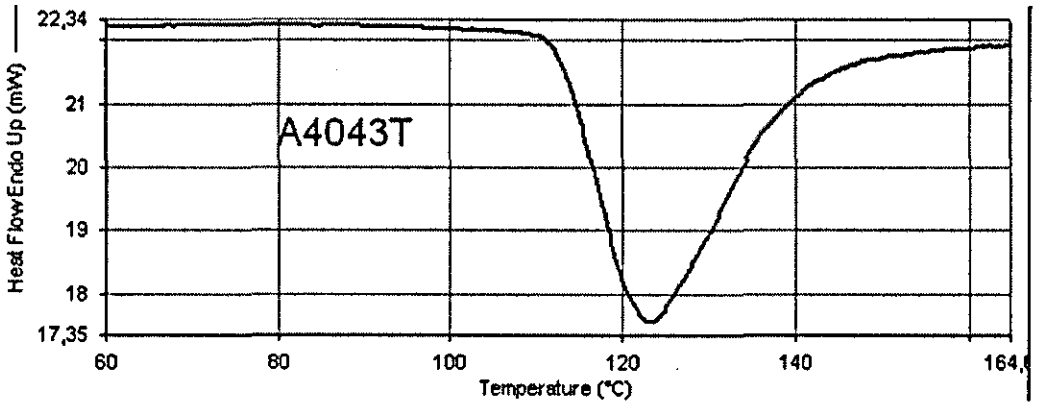
CELESTICA.

A4043T - DSC scan



Optimum curing Temperature : 120 °C

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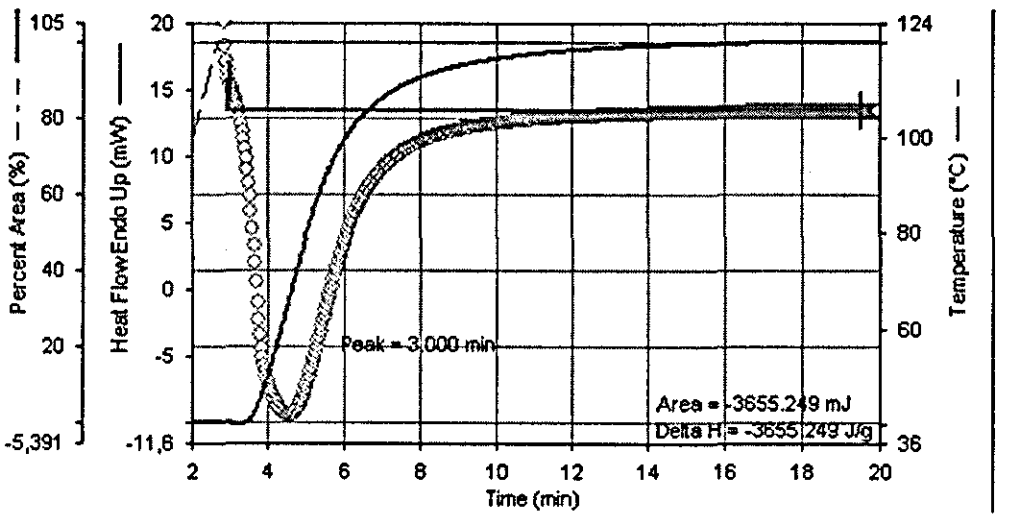
A 4043T - kinetics

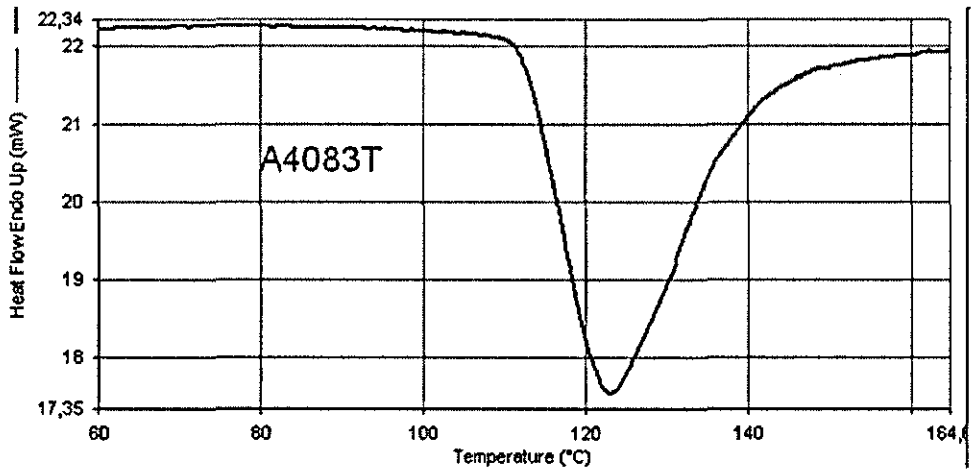


Blue solid line: % curing vs time (@ 120 °C)

- **100% curing : 17 minutes @ 120 °C**

CELESTICA.

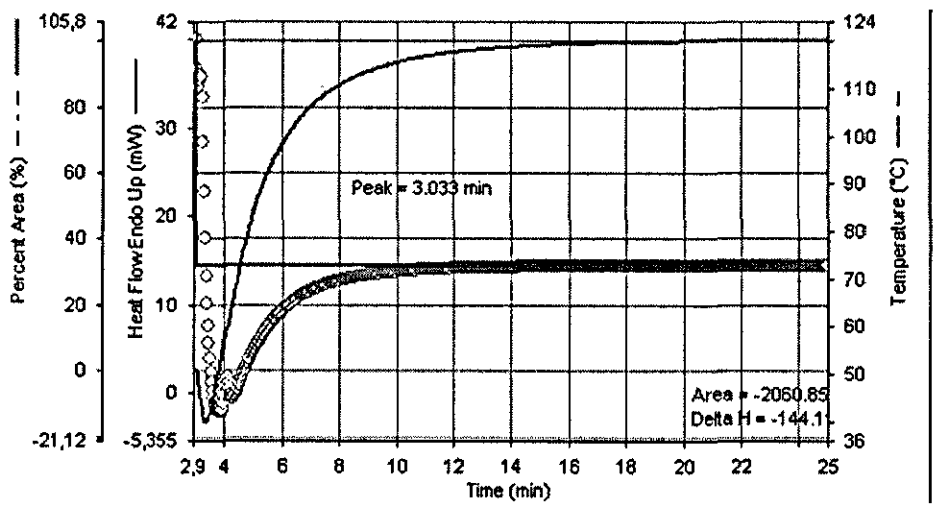
A4083T - DSC scan



Optimum curing Temperature : 120 °C

CELESTICA.

A 4083T – kinetics

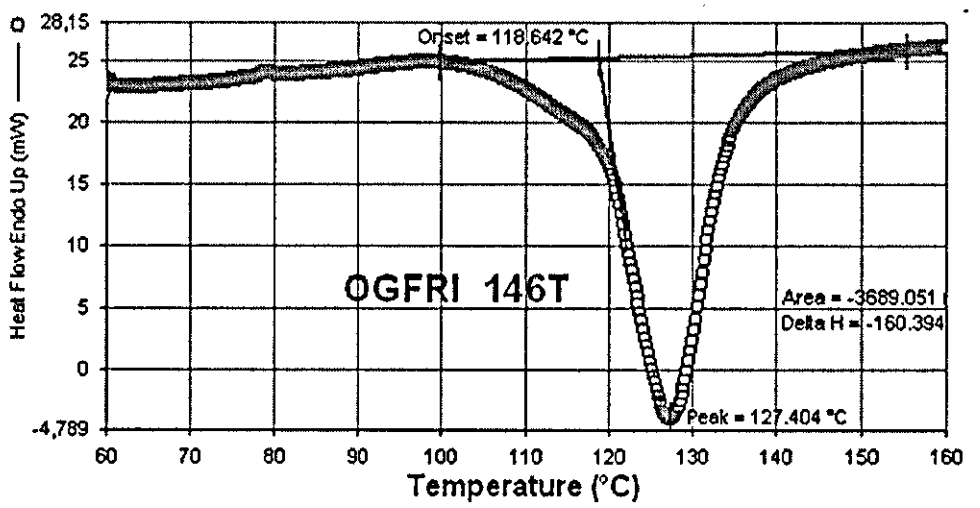


Red solid line: % curing vs time (@ 120 °C)

- **100% curing : 20 minutes @ 120 °C**

CELESTICA.

OGFRI 146T - DSC scan



Optimum curing Temperature : 122 °C

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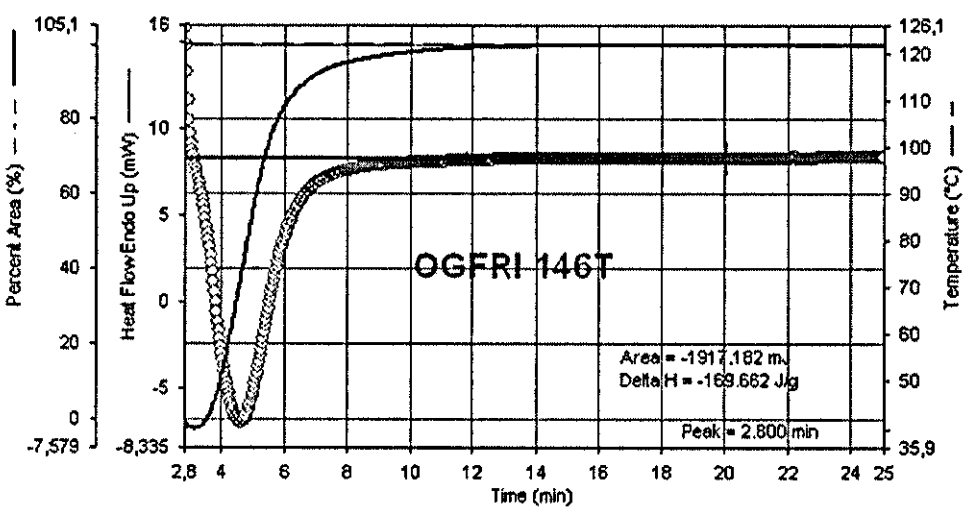
OGFRI 146T – kinetics

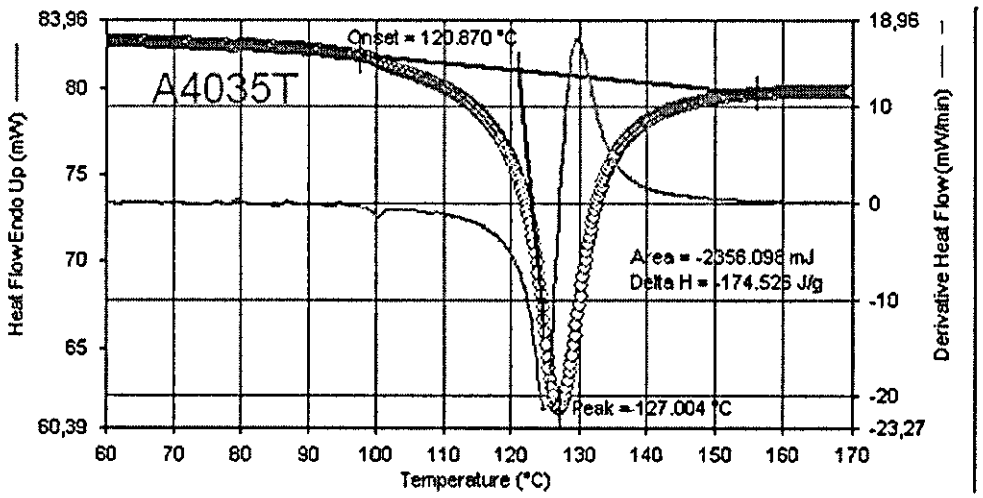


Blue solid line: % curing vs time (@ 122 °C)

- **100% curing : 17 minutes @ 122 °C**

CELESTICA.

A4035T - DSC scan



Optimum curing Temperature : 125 °C

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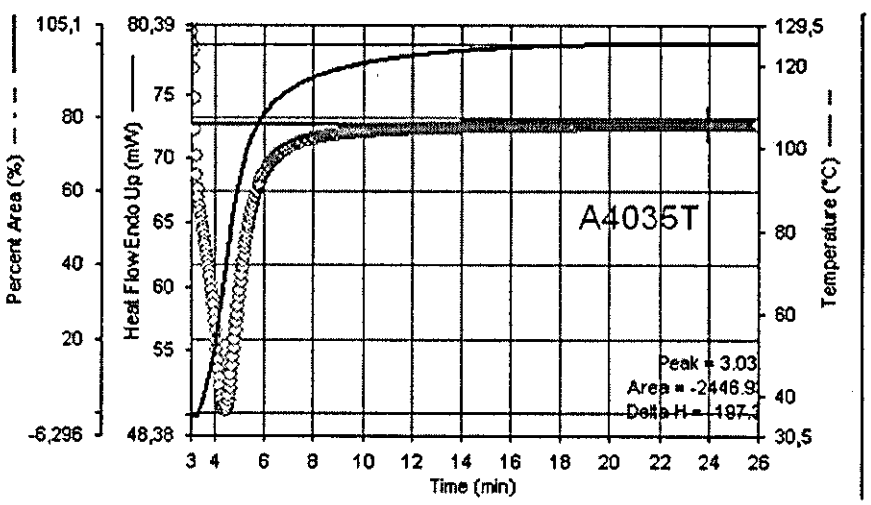
A4035T – kinetics



Blue solid line: % curing vs time (@ 125°C)

- **100% curing : 20 minutes @ 125 °C**

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Conclusion

The products under test are UV curable adhesives, with a secondary thermal curing mechanism. This last was evaluated by DSC .

According to the test results, the optimum curing cycles to reach a complete "chemical curing" , are listed in the following table :

Product	Time [minutes]	@ Temperature [°C]
A4043T	17	120
A4083T	20	120
OGFRI 146 T	17	122
A4035T	20	125