Materials and processes issues in fine pitch eutectic solder flip chip interconnection

Materials and Processes Issues in Fine Pitch Eutectic Solder Flip Chip Interconnection

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***Abstract*—New product designs within the electronics packaging industry continue to demand interconnects at shrinking geometry, both at the integrated circuit and supporting circuit board substrate level, thereby creating numerous manufacturing challenges. Flip chip on board (FCOB) applications are currently being driven by the need for reduced manufacturing costs and higher volume robust production capability. One of today's low cost FCOB solutions has emerged as an extension of the existing infrastructure for surface mount technology and combines an under bump metallization (UBM) with a stencil printing solder bumping process, to generate mechanically robust joint structures with low electrical resistance between chip and board. Although electroless Ni plating of the UBM, and stencil printing for solder paste deposition have been widely used in commercial industrial applications, there still exists a number of technical issues related to these materials and processes as the joint geometry is further reduced. This paper reports on trials with electroless Ni plating and stencil paste printing and the correlation between process variables in the formation of bumps and the shear strength of said bumps at different geometries. The effect of precise control of tolerances in squeegees, stencils and wafer fixtures was examined to enable the optimization of the materials, processes, and tooling for reduction of bumping defects.**

***Index Terms*—Flip-chip, shear Strength, stencil Printing, under bump metallization (UBM).**

I. Introduction

BALL grid array (BGA) and chip scale packaging (CSP) formats provide increased circuit density capability coupled with a reduction in real estate coverage on the supporting board. However, as the inexorable drive towards miniaturization and higher operating speeds continues, the need to completely eliminate even the minimum of chip packaging becomes evermore critical. Flip chip interconnection involves the assembly of naked, unpackaged chips directly to a supporting board, requiring products to be manufactured with solder joints at geometries similar to those of the semiconductor chips. Further reduction in the scale of flip chip geometries is expected, to ensure the technology keeps abreast of future product applications and integrated circuit (IC) designs [1], [2]. Such demands are also reflected at the board level, where microvia technology (sub 50 μm diameter) has been developed, that is capable of supporting flip chip on board (FCOB) interconnection [3].

Various hybrid processing techniques have been explored and adopted within the electronics manufacturing industry in order to provide FCOB solutions [4]–[7]. Electroplating, evaporation, solder jetting, stud bumping, stencil printing and "squeegee bumping" [7] have been employed, with each having its own merits, but their technological capability in terms of joint geometry, metallurgy, reliability, and processing cost (equipment, production yield) are critical factors to be considered. Extending surface mount technology (SMT) process capabilities, equipment, and soldering materials offers a cost-effective solution for flip chip interconnection. This can be achieved by coupling stencil printing with the UBM of electroless Ni–P for bumping chips (usually on a whole wafer), which are subsequently attached to a supporting board to form solder joints. The electroless Ni–P plating process, as a cost-effective approach to providing a barrier layer and wettable surface, has been investigated [8]–[11] to enable selective deposition onto the bond pads. Although this process is potentially commercialized, there still exist a number of issues regarding the plating quality and technical specifications with respect to the initial bondpad characteristics (e.g., Al alloy composition, microstructure, thickness, properties, passivation defects, etc.).

The materials and processing variables in stencil printing also critically affect the quality and yield of solder deposition to produce consistent, reproducible and uniform bumps for fine pitch flip-chip prior to final assembly [12]–[20]. The Ishikawa cause-and-effect diagram generated by Pan *et al.* [14] summarizes these variables. There are eight major categories identified (operator, environment, printing parameter, printer, stencil, wafer, squeegee and solder paste) that could influence the solder paste printing. Pan showed that, apart from the rigid control of the parameters related to the materials and systems used, the operator's skills and experience need to be included. In this paper, FCOB trials have been undertaken with flip chips having bond pad pitches in the range of 300 to 90 μm with both peripheral and full array bond pad layouts. The issues related to materials and processing variables are addressed to provide guidance in the further enhancement of FCOB for high volume production.

II. Experimental Details

A. Flip Chips For Trials

Two types of test chip, having different feature dimensions, were used to investigate the effects of size in relation to the materials and processes. Test chips were processed in a 4 in

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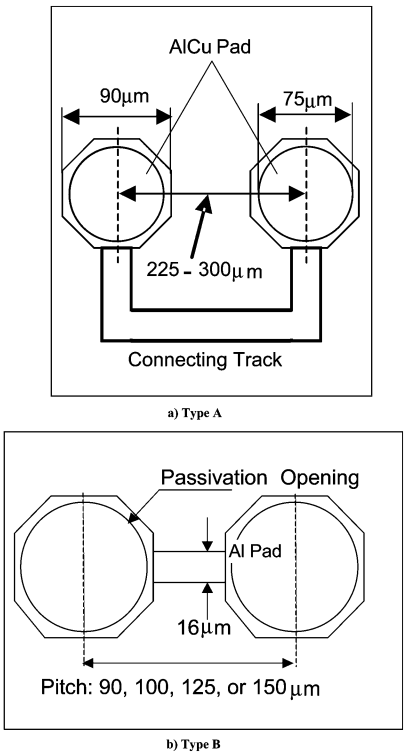


Fig. 1. Details of test chip designs: pad pitch, layout, materials, and opening.

(Ø100 mm) wafer format prior to dicing for bump analysis and assembly. Wafer type A [Fig. 1(a)] was a peripheral input/output (I/O) daisy chain design with 3-μm thick Al-1Wt%Cu alloy bondpads on pitches of 225 μm and 300 μm. The circular openings in the silicon nitride passivation over the bondpads had a diameter of 75 μm. The type A chips were 6 mm $\times$ 6 mm in size with a thickness of 500 μm.

Wafer type B [Fig. 1(b)] included chip designs with both peripheral and full area array patterns of 1-μm thick pure Al bondpads. For the purposes of this experimental evaluation, chips with an I/O pitch ranging from 90 to 150 μm, in a daisy chain format, were used. The bondpads had a circular passivation opening of 50 μm for the 90-μm pitch, but 60 μm for the other pitches. The type B wafer was laid out as an array of 12 mm square repeated patterns; where each 12 mm^2 die was subdivided into a further 16 smaller 3 mm^2 die areas. Fig. 1(b) shows the bondpads on the 3 mm^2 die laid out on four different pitches. Each pitch was laid out as a peripheral design, an array in a square pattern and a staggered on array hexagonal where the bumps were packed the closest that they could be for that pitch. Table I summarizes the details of the two types of wafer used for this work.

B. Under Bump Metallization (UBM) and Solder Bumping Trials

Both types of wafer were processed to generate an UBM layer on the bondpads for subsequent solder bump formation, using electroless nickel plating developed from previous experimental work [21], [22]. The process included activation of the Al bondpads by a single or double zincate treatment followed by plating

TABLE I
COMPARISON OF TWO TYPES OF WAFER USED FOR THE TRIALS

Wafer	Type A	Type B
Bondpad material	AlCu (1 wt % Cu)	Pure Al
Bondpad thickness	3μm	1μm
Passivation	Si_3N_4	SiO_2
Defects on passivation	None	Fine particles and pits
Die size	6x6mm	3x3mm
Pitch	225, 300μm	90, 100, 125, 150μm
Bondpad shape	Octagonal	Octagonal
Passivation opening	75μm circular	50, 60μm circular
Bondpad layout	Peripheral	Peripheral and full array

in an acidic hypophosphite bath that deposited a layer of Ni–P containing 4–5 Wt% P.

Following the electroless Ni UBM plating, solder paste deposits were created by stencil printing onto the bondpads to form eutectic SnPb bumps for subsequent reflow soldering. A recently developed paste that contained an 89 wt.% content of SnPb eutectic solder alloy particles (diameter 5–15 μm) and formulated with three different flux systems [rosin mildly activated (RMA), no-clean (NC) and water soluble (WS)] was used for the printing trials. Stencil aperture sizes in the range of 175 μm to a minimum of 75 μm in diameter were assessed with two electroformed Ni stencils that were 50 μm and 75 μm thick. Both metal and rubber squeegees were employed to compare their effects. Using a DEK 265 printing machine, stencil printing parameters such as squeegee speed and applied pressure were optimized to achieve suitable quality solder paste deposits for both the A and B type wafers. The parameters used in the printing trials were:

- printing speed: 10 mm s^{-1};
- snap off (separation gap between stencil and wafer surface): 0.00 mm;
- normal load on squeegee: 30–80 N;
- separation speed: 0.5–2.0 mm. s^{-1}.

Finally, reflow of the paste deposits in an N_2 inert atmosphere was carried out to form the solder bumps. A scanning electron microscope (SEM) with energy dispersive analysis of X-rays (EDX) was utilized to investigate the surface morphology and for materials analysis.

C. Laser Surface Profiling

Since the wafer was too fragile to be handled by the standard printed circuit board carrier, a wafer fixture (or 'holder') was needed to support the wafer during printing. Two wafer fixtures (I and II) were used for the trials, which had different tolerances for the recessed pocket where the wafer was held by vacuum. Fixture I was machined from an aluminium alloy with a recessed circular pad made from porous ceramic. Fixture II was machined from mild steel with a precision recessed pocket with minimum surface variation. The surface planarity of the wafer when held in the pocket using both fixtures was evaluated using a laser surface profiler, which utilitsed a Rodenstock RM600 laser stylus capable of non-contact measurement between 0.01 μm and 600 μm.

D. Bump Micro-Shear Testing

A micro-shear strength study of the mechanical integrity of the eutectic Sn/Pb bumps was conducted using a Dage Series

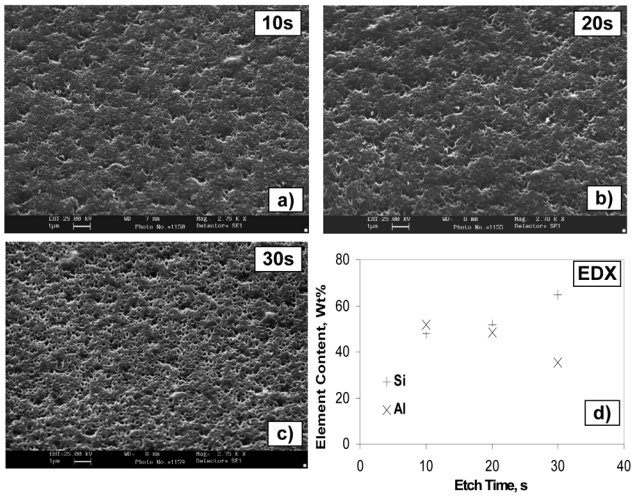


Fig. 2. Etching of Al pads on wafer B in 5% NaOH solution: SEM surface morphology after (a) 10 s, (b) 20 s, (c) 30 s, and (d) the EDAX elemental content analysis.

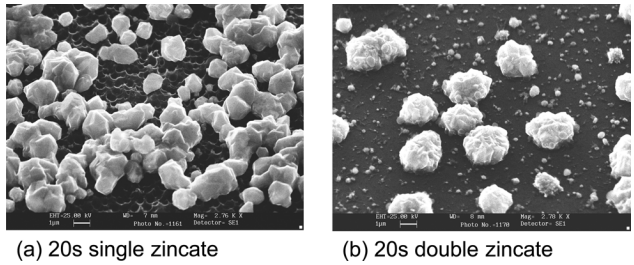


Fig. 3. Zincate treatment of Al pads on wafer B: (a) 20 s single zincate and (b) 20 s double zincate, following 20 s etch in 5% NaOH.

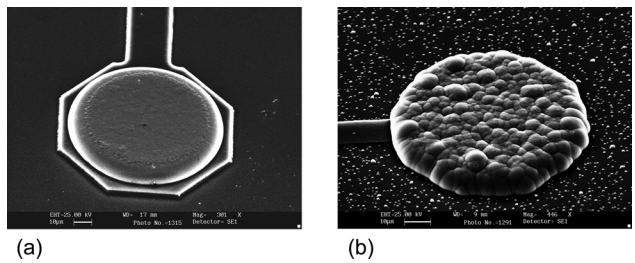


Fig. 4. Electroless Ni–P UBM bump formation: (a) Ni–P bump on pads of wafer type A and (b) Ni–P bump on pads of wafer type B.

4000 multipurpose bond tester with a BS250 Ball Shear cartridge. This low deflection cartridge enabled precision shearing at pre-set heights above the chip surface. The width of the shear tool was 100 μm, sufficiently wide to cover the bump diameter but not so wide as to interfere with adjacent bumps during the shear testing. A shear speed of 100–300 μm/s and shear height of 25%–50% of the bump height were employed. During each test, the peak shear force and the corresponding displacement of the shear tool through the bump structure were recorded. For each shear test protocol, 20 solder bumps were sheared from individual chips which were randomly chosen from each test wafer.

III. Results and Discussion

A. Under Bump Metallization

The under bump metallization (UBM) provides a solderable surface as well as protection for the Al pads from flux and solder dissolution during the solder reflow processes. A process that has received considerable interest as a maskless low cost wafer UBM technique is electroless nickel deposition, which is also suitable for large volume production [21], [22]. However, plating defects can occur when finer pitch chips are processed, which are related to the pad microstructure and plating process variables. Fig. 2(a)–(c) show the surface morphology of the Al pads on wafer type B after pre-etching in 5% NaOH solution for 10, 20, and 30 s, respectively. Clearly, due to the localized preferential etching, the Al pads became more porous after 30 s etching, which has led to poor Ni–P morphology in the subsequent plating. Fig. 2(d) shows an EDX analysis from these etched surfaces. A dramatic decrease in their Al content was seen for 30 s etching, indicating that damage to the pads had certainly occurred.

The zincation process, which is conventionally used to activate the Al pads prior to Ni deposition, may also cause thinning of the Al pads due to the highly alkaline characteristics of the zincate solution. This could substantially reduce the interfacial bonding strength (adhesion) of the deposited Ni layers [10]. Fig. 3(a) and (b) are SEM micrographs of the Al pads of wafer type B after 20 s single and double zincation, respectively. In comparison with the porous Al pads from single zincation [Fig. 3(a)], the Al pads after double zincation had been entirely removed [Fig. 3(b)]. This led to a radical reduction of the Ni layer adhesion [10]. Furthermore, the electrical resistance of the contact increased dramatically due to the thinning of the Al pads. For wafer type A, the thicker Al–Cu alloy pads allowed a wider processing window for etching and zincation to produce a finer and smoother zincate layer prior to Ni plating. Fig. 4(a) and (b) show the typical surface morphology of Ni–P coating on the bondpads of wafer A and B, respectively. A number of issues related to the type B wafer and process specifications were identified for finer pitch flip chips as shown in Fig. 5—illustrating an SEM image of a 5-μm Ni–P UBM for 100-μm pitch staggered full array chip. The defects observed in the passivation resulted in the deposition of Ni nodules over tracks and between pads. This may cause short-circuits between pads; therefore, caution must be taken to avoid such faults at wafer manufacture to eliminate defects in passivation and to ensure accurate registration of pad openings.

B. Stencil Solder Bumping of Flip Chips

1) Solder Paste Deposition By Stencil Printing: Production of consistent, reproducible and uniformly distributed paste deposits over an entire wafer by stencil printing presents numerous challenges in finer pitch flip-chip applications. The solder paste used is composed of solder alloy particles, flux, viscosity controlling agents and a solvent system. Modeling and experimental work has demonstrated that the minimum ratio of the aperture size to the solder particle diameter should be five [20]. Depending upon the pitch size of the flip chips, a solder paste containing fine particles (e.g., 5–15 μm) is therefore usually required to enable sufficient stencil aperture fill

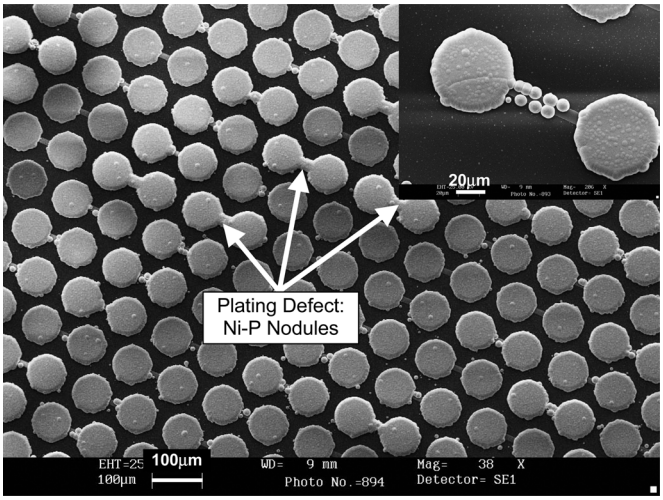


Fig. 5. Electroless Ni–P plating defect identification: 5-μm thick Ni–P layer on 100-μm pitch staggered full array chip.

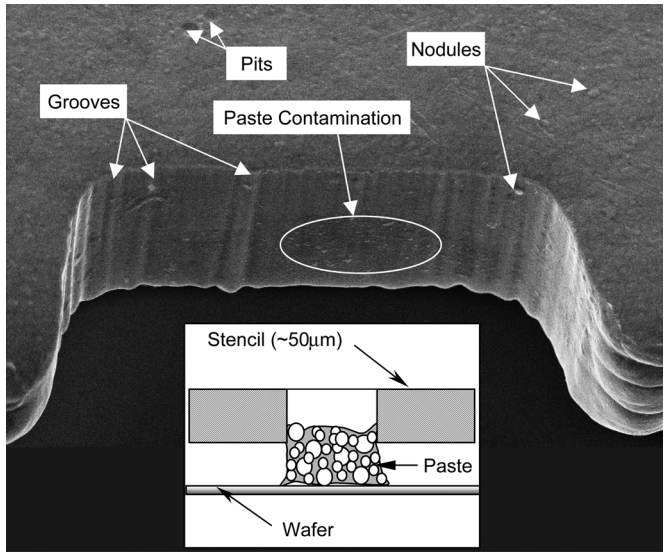


Fig. 6. SEM cross-sectional observation into aperture wall texture of a nickel electroformed stencil.

and acceptable release characteristics. In the printing process, solder paste sheared off by a squeegee blade rolls and subsequently fills the apertures in the stencil ahead of the squeegee as it moves over the stencil. On completion of the print stroke, the wafer is separated from the stencil, generating freestanding paste deposits on the bondpads beneath the stencil. Typical printing defects include bridging of adjacent pads, slumping, poor shape definition and skipping (insufficient or no solder deposited) [19]. Optimized printing needs to consider variables including: paste rheology; squeegee pressure and speed; stencil separation speed; print direction and environmental considerations such as temperature and humidity. According to Zou *et al.* [17], the print temperature and humidity could significantly affect the printing quality using the squeegee method; it is therefore advantageous to use an enclosed, environmentally controlled print system [17]. The printing trials in this work were however performed in uncontrolled ambient environment on two types of wafer (A and B) to investigate both the attributes and consistency of the paste deposits, without consideration of the external environment (e.g., temperature, humidity and air flow). The critical factors affecting paste flow during the printing were thought to be aspect and area ratio with paste transfer efficiency being improved if the aspect and area ratio were higher than 1.25 and 0.6, respectively [24]. There has been some experimental work combined with computational study (i.e., CFD approaches) to understand the printing process and the effects of relevant variables at macroscopic and microscopic scales [20], [23], [24].

Fig. 6 shows a SEM view of a 100 μm^2 aperture from the Ni electro-formed stencil. A number of features are apparent on the stencil surface (e.g., pits, nodules, and scratches), and along the wall of the apertures (e.g., grooves). As these features were equivalent to the size of particles in the paste, it is likely that filling of the aperture was affected by the interactions between paste and stencil. Macroscopic studies on bulk motion of paste ahead of a squeegee indicated non-Newtonian behavior during the rolling of the paste and numerous process parameters may therefore play important roles in determining the paste deposition [23]. Meanwhile, the microstructural dynamics of individual particles suspended in the carrier fluid could be critical to the printing consistency and quality [20]. In this study, the wave-like groove texture along the aperture wall (see Fig. 6) can affect the flow, filling and release behavior of the paste. In particular, adjacent to the corners of square apertures, the paste packing and subsequent release during the 'snap-off' (separation of stencil from wafer) can be substantially affected as indicated by microstructural modeling by He *et al.* [20]. The stencil surface texture that contained features (e.g., pits and inclusions) at the microscopic scale can also influence the rolling of the paste and the interaction of paste with the stencil, which also impacts on the print quality. The relationship between the motion of solder particles and the paste rheology, and the tendency for paste to adhere to the aperture walls during stencil withdrawal, requires further study into the microstructure of paste transfer dynamics. However, the behavior of a dense suspension at a plane wall boundary is different to that at the interior. At a solid wall, there tends to be a depletion of solid particles and hence a fluid rich region due to the packing arrangement of the particles and hydrodynamic effects. The fluid rich region acts as a lubricating layer and is responsible for "wall-slip" effects, where the suspension appears not to adhere to the solid surface from a macroscopic viewpoint [23]. The molecules of the suspending fluid do actually adhere to the walls but the lubricating layer is responsible for an apparent "slip velocity" of the solid particles. This mechanism plays an important role in the efficient release of solder paste from the stencil aperture, which is indicative for improving the print quality through altering the parameters such as print speed and squeegee pressure. However, at a microscopic scale, the properties of the "lubricating layer" can vary and relate more to the interaction between the aperture wall and the lubricating layer locally. This is determined by the localized properties of the solder paste and stencil wall texture.

2) Tolerance of Tooling (Stencil, Squeegees and Wafer Fixture) in Fine Pitch Solder Paste Printing: The stencil used for printing plays a significant role in the quality and yield of solder paste deposition. Currently, stencils for SMT assembly

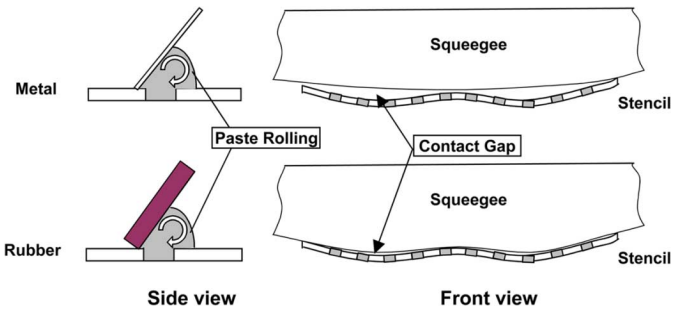


Fig. 7. Squeegees in action to roll the paste and fill the stencil aperture: the effect of the materials and design of the squeegees on the print quality and yield (a) rubber squeegee and (b) metal squeegee.

are usually fabricated by chemical etching, Ni electroforming, or laser cutting processes. The materials used to make a stencil should meet various requirements in terms of their processability, durability, plastic/elastic deformation properties, wear and corrosion resistance, and cost effectiveness. Electrochemical Ni formed stencils have often been used for fine pitch flip chip wafer bumping (e.g., for the $\sim$ 100 μm pitch on wafer type B) due to their high hardness, excellent creep and fracture resistance and rapid manufacturability. However, the challenge still remains to reduce the manufacturing costs and to optimize the microstructure of the surface finish and precision aperture definition [18]. In particular, for finer pitch chips, the relationship between the aperture shape and size, and the aspect and area ratio has to be considered to achieve the highest packing efficiency. The stencil surface friction and elastic and plastic characteristics are also important parameters to achieve high alignment accuracy and a suitable "snap-off" characteristic.

Squeegees are the blades used to shear and propel the solder paste to fill the apertures in the stencil. The contact between squeegees and the stencil surface, and paste rolling due to the shear process, were both found to significantly affect the final bumping quality (consistency and defect rates). The squeegee materials and properties (e.g., hardness, stiffness, and straightness) are of particular concern. Printing trials in this study showed that the quality and yield of paste deposits were dramatically improved with a rubber squeegee, in comparison to a metal squeegee. To explain this, Fig. 7(a) and (b) schematically illustrate the deformation of a squeegee with a stencil for two types of squeegees: rubber and stainless steel, respectively. The closer contact along the curved stencil surface that is attributed to the better elastic characteristics of rubber materials results in a narrower crevice between the squeegee and stencil, while the stainless steel squeegees were unable to co-locate the deformation with the stencil surface, so that larger contact gaps resulted. The larger the crevice, the lower the packing efficiency obtained, because of the localized lower levels of shearing and pressure. Therefore defects such as partial or incomplete deposits (skipping) and missing bumps were observed after the stencil was removed. Visual inspection confirmed that the distribution of the paste deposits when using metal squeegees was less uniform, and many missing or skipped bumps occurred.

The dimensional tolerance or accuracy of the wafer fixture (holder) is also critical to the printing quality (e.g., consistency)

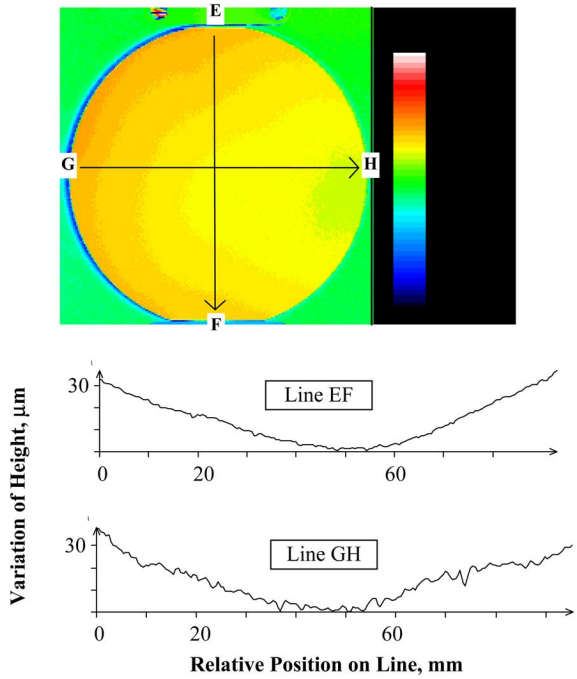


Fig. 8. Laser surface imaging profile of wafer fixture I: Surface variation of wafer in pocket drawn down by vacuum.

and yield. Two types of wafer fixtures (I and II) were used in this work to investigate the effect of their surface coplanarity tolerance. Fig. 8 provides the laser surface topography when the wafer was sucked into the pocket of fixture I by vacuum during the printing process. The line profiles EF and GH from the scans show a variation in height of $\sim$ 40 μm, measured from the edge to the centre of the wafer, owing to the poor planarity of the pocket surface. Zou *et al.* [17] proposed the estimation of substrate (e.g., wafer) distortion degree using $H/L\%$, where H is the maximum vertical variation due to bending, and L the substrate length or diameter. Accordingly, using fixture I the wafer distortion degree is estimated to be 0.04% for the 100 mm (4 in) wafers. This is well below the critical value of 0.1% proposed by Zou *et al.* to enable acceptable quality by squeegee printing in the case of PCBs with pitches greater than 300 μm. However, in this study, for printing on wafers with pitch size smaller than 300 μm, the trials have shown that squeegee printing was unable to cope with distortions as small as 0.04% using fixture I, resulting in a solder paste "smear" area appeared near the centre of the wafer after printing, and consequently, the occurrence of a number of print defects such as slumping, skipping, missing or displaced bumps where the paste "smear area" was observed. Fig. 9 shows a typical result of the evaluation selected from a number of trials on wafer type A. This indicates that the rigid wafer fixture is required to ensure the flatness of the wafer surface to be printed. Using wafer fixture II, the resulting variation on the wafer when it was drawn down in the pocket by vacuum was around 5 μm (see the line profiles of EF and GH in Fig. 10). This variation can be converted into a distortion degree of approximately 0.005%. Unsurprisingly, when using fixture II, there was no observable "smear" area after printing, printing trials showed an excellent quality and uniformity of paste deposit distributed throughout the entire wafer surface, with a dramatic reduction of the defects. Improvement of printing quality

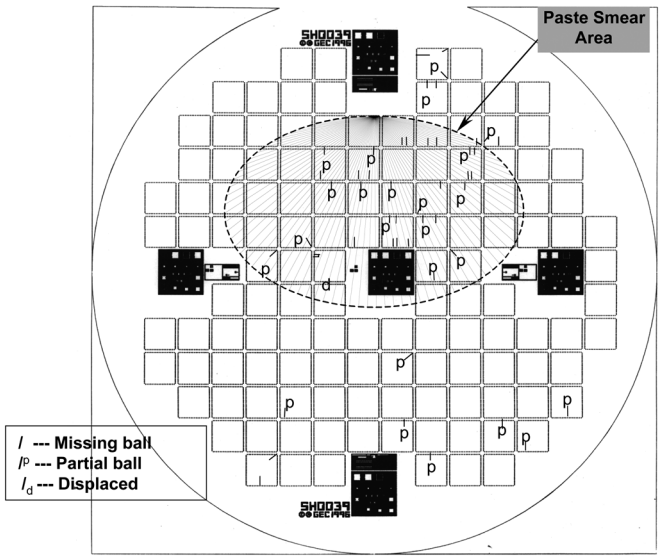


Fig. 9. Evaluation of bumping by stencil printing on wafers type A with wafer fixture I: A smear paste area was identified causing poor quality of paste deposition.

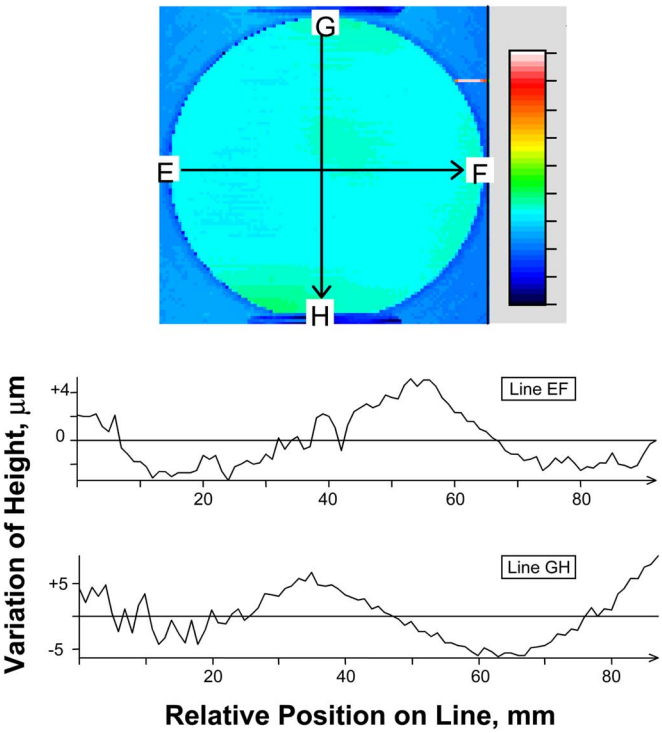


Fig. 10. Laser surface imaging profile of wafer fixture II: Surface variation of wafer in pocket drawn down by vacuum.

due to the smaller distortion of the wafer surfaces to be printed can be attributed to a significant increase of paste packing efficiency and a cleaner release motion of the paste from the apertures. When withdrawing the stencil from the wafer surface, the stencil conforming closely to the wafer surface resulted in uniform squeegee pressure and a controlled "snap-off" as the squeegee passes. In contrast, where there is poor stencil-wafer

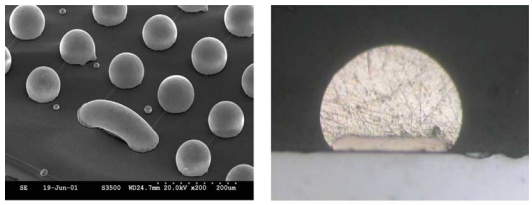


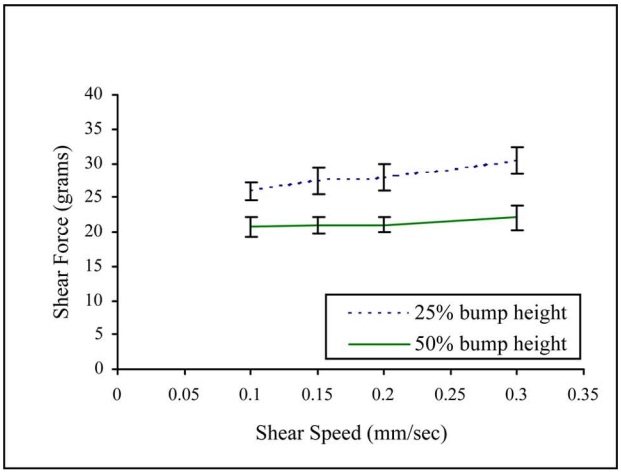
Fig. 11. Solder bump formation: (a) SEM micrograph of solder balls on Ni UBM of 150-μm pitch and (b) cross-sectional view of a 80-μm diameter bump.

conformation, the paste packing efficiency was significantly decreased due to less shear and squeegee pressure and solder paste tends to adhere to the aperture walls. The smeared paste area occurred where the squeegees cannot remove the paste from the depressed areas, such that the paste residues remained on the stencil surface. On withdrawal of the stencil, the paste in the apertures could be completely or partially lifted up along with the paste residues on the stencil, thereby causing slumping, skipping and missing or displaced bumps.

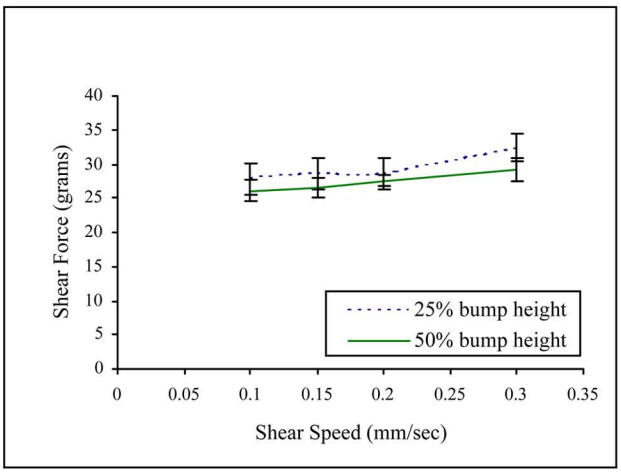
C. Formation and Shear Strength of Solder Bumps

After a reflow process in a nitrogen atmosphere the solder paste deposits formed solid solder bumps. Fig. 11(a) shows the solder bumps for a 150-μm pitch full array chip, which included a bridging defect. This type of failure was the result of adjacent oversized deposits merging together during reflow when the pitch was equivalent to the pad size (e.g., openings). The small balls formed between the bumps in Fig. 11(a) are thought to be formed at the defects on the passivation layer where the small Ni nodules were generated in the Ni UBM processes (Fig. 5) and could later have become the sites for solder attachment. The microsectional image [Fig. 11(b)] confirms the excellent wetting of solder to the Ni–P UBM and the formation of the intermetallics along the interface between the solder alloy and Ni–P layer, producing a typical bump with a height of 60 μm at 125-μm pitch.

Shear tests were carried out in this work to evaluate the mechanical strength of the final multilayer bumps, and to understand the failure modes. Fig. 12(a) and (b) show the effects of both shear speed and shear height at 80 μm and 100 μm bump diameters, respectively. The error bars around the data points, for all the graphs in this text, represent one standard deviation. The results, for the varying bump diameters, indicate two trends clearly visible from the shear study. First, increasing the shear speed yields apparently higher shear strengths for the bumps. Second, reducing the shear tool height also appears to increase the bump shear strength. The variation in shear height was investigated in light of the shear height tolerance specified within the JESD22-B117 standard, which states a maximum height of 25% of the bump height. These shear study trends reflect similar work reported by Huang *et al.* [25], albeit at BGA geometries. Further shear testing was conducted at a shear speed of 150 μm/s and corresponding height of 25%. The average shear strength was found to increase slightly from 27.5 g$\pm$ 1.8 g for the 80-μm bump to 28.6 g $\pm$ 2.3 g for the 100-μm bump size. This is attributed to an increase in the sheared cross-sectional area.



(a) 80μm bump diameter



(b) 100μm bump diameter

Fig. 12. Bump shear results: The effects of varying the bump diameter and shearing height.

IV. Conclusion

A number of technical issues related to the materials and process variables have been presented, in order to produce quality bumps and thus reliable solder joints for fine pitch FCOB interconnection. In electroless Ni plating for the UBM, the pretreatment steps including the etching (in NaOH) and zincation, are critical to ensure a Ni–P layer with adequate adhesion to the Al pads and low electrical resistance. The elimination of Ni nodules generated at the defects in passivation is crucial to prevent bridging and, as such, wafer manufactures should ensure a defect free passivation with accurate registration of the pad openings.

The stencil printing trials identified issues of stencil fabrication (e.g., the need for high quality aperture definition), and dimensional tolerances of squeegees and wafer fixtures used in printing. The filling, release and distribution characteristics of the paste material through the small aperture geometry determine the quality and consistency of the bump formation. Therefore, not only the print parameters, but all of the related mechanical components (e.g., stencil, squeegees, and wafer fixture etc.), and their dimensional tolerances, need to be carefully considered to achieve the maximum reduction of bumping defects. Significant reductions in solder bumping defects by stencil printing have been demonstrated by optimising the materials and processing variables in relation to the precise manufacture, definition, rigid design and control of the stencil apertures, wafer fixtures and squeegees. A Ni formed stencil with precisely defined aperture geometries, coupled with the use of rubber squeegees, a rigid wafer fixture and optimized printing parameters has been employed to produce consistent, reproducible and uniform paste deposits with high yields and quality for flip chip wafer bumping for pitches down to 100 μm.

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