The continuous measurement of arterial pulse wave velocity

THE CONTINUOUS MEASUREMENT OF ARTERIAL PULSE WAVE VELOCITY

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by

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ABSTRACT

This thesis describes a system which has been developed to continuously monitor the pulse wave velocity in the main systemic arteries in man, without surgical intervention. The production of the pulse wave and its mode of propagation are discussed and the possible applications of a device of this nature.

Pulse wave velocity is surveyed in terms of its analytical relationship to blood pressure, its clinical information and the measurement techniques used by previous experimenters.

The problem, as considered, is stated and a system based on a novel measuring technique is developed to enable a high resolution to be obtained. The pulse wave velocity is defined as the speed of propagation of the wave peak between two points on the artery, a short distance apart. The wave is monitored by transducers which are designed with a fluid sac to avoid mounting and centering difficulties.

The system functions by first controlling signal amplitude from the transducers to give a constant output, exponential amplification is then used to selectively amplify the peak value. From this signal the peak is defined by differentiation. The velocity is obtained by measuring the delay, and then computing it from this using an analogue system.

A Simulator is described which produces a signal, which has a waveform similar to that of the pulse wave.

The simulator provides two channels with a variable time delay between them.

The design of the constituent parts of both systems is discussed in some detail.

The report concludes by giving suggested modifications to the systems described, and also indicates fields in which future work should proceed.

CONTENTS

List of Symbols and Abbreviations

A_m	Amplitude
C_x	Capacitor X
D	Delay
Diff.	Differentiator
D_x	Diode X
E.F.	Emitter Follower
Exp.Amp.	Exponential Amplifier
f_k	Pulse Wave Ordinate (Fourier Analysis)
Gen.	Generator
h_{FE}	Transistor current gain at dc. Common Emitter.
Int.	Integrator
I_x	Current X
k	Boltzmann's Constant.
P.G.	Pulse Generator
q	Electron charge
RVX	Potentiometer X
R_x	Resistor X
S.C.	Shaping Circuit
SD	" " , Differential Control.
SI	" " , Integral Control.
S/D	Switch Delay
S/G	Switch Generator

T	Absolute Temperature
T_x	Time period X.
V_{BE}	Transistor, Base: Emitter Voltage.
V_{CE}	" , Collector: Emitter Voltage.
VTX	Transistor X
V_x	Voltage X
Z	Impedance Z
AGC	Automatic Gain Control
ECG	Electrocardiograph
PRF	Pulse repetition frequency
PWV	Pulse Wave Velocity
I/P	Input
O/P	Output

ACKNOWLEDGEMENTS

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Last, but not least, I wish to thank my wife Mrs. S.M. Wheaton, for converting my humble script into its present form.

SECTION 1

Introduction and Summary of Earlier Works

Before one can attempt to measure the velocity of the phenomenon known as the arterial pulse wave, one must consider the physiological 'mechanism' which produces this wave. In addition one must justify that the measurement of this parameter will be of some value.

Considering the latter point first, it is common, in an engineering environment, to express the 'performance' or 'reactions' of a device, circuit or system as a set of parameters. For example one can specify the performance of an amplifier circuit in terms of its bandwidth, gain, and input and output impedances.

However in dealing with a physiological system, the full data is generally complex and not easily measurable. Thus medical science has been built up on those parameters which lend themselves to being measured with comparative ease. Blood pressure can be included in this category, since its measurement can easily be effected with the aid of an occluding bandage or cuff, and a simple manometer. Blood pressure can be used, in conjunction with other information, to diagnose various illnesses and deficiencies occurring in the body. But is it necessarily the most useful parameter to measure? Would a knowledge of the "pulse wave velocity" be a more useful factor in determining the state of the arterial system? Questions

such as these do not as yet appear to have an answer, so only time and further work can give it. However, the parameter known as "Pulse Wave Velocity" may be of value, either alone or in conjunction with blood pressure, provided that it can be measured easily and accurately.

Before extending this argument, or considering any previous work in the field, an understanding of the circulatory system and the production of the pulse wave is required.

The circulation is divided into the three categories:- i) Pulmonary ii) Systemic iii) Portal.

The pulmonary circulation is for the reoxygenation of the blood, which is pumped to the lungs via the pulmonary artery from the right ventricle of the heart. The venous return from the lungs is fed into the left antrium via the pulmonary veins, this is the complete pulmonary circulation.

The systemic and portal circulations are both derived from the left ventricle, and are the circulation of the blood round the body. The systemic circulation feeds the body tissues, whereas the portal circulation feeds the digestive system and liver. Both are derived from the Aorta and the venous return is via the Venae Cavae into the right antrium.

Heart action is controlled by a small bunch of nerves and muscles located in the right atrium, to which the venous return from the body comes. The nerve cells act as a pacemaker for the heart and are called the sino-atral node. They also give rise to the electrical signal known as the electro-cardiograph. The normal rate of excitation is approximately 72 beats per minute, in an adult. Each period of contraction is followed by a period of rest of approximately the same duration.

The contracting period is known as the systole and the rest period as the diastole, each being approximately 400 msec long. The complete action is referred to as the cardiac cycle. The systole is subdivided into two parts, the atrial systole and the ventricular systole. The atrial systole is of a short duration and consists of a contraction wave sweeping over both atria and forcing the blood there into the ventricles, through the tricuspid and mitral valves. The ventricular systole commences as soon as the pressure in the ventria exceeds that in the atria. The valves shut and blood is forced into the aorta and pulmonary artery. The process ends when the pressures in the ventria are equal to those in the aorta and pulmonary artery.

The rest period or diastole now commences and blood pours into the ventria from the atria, and also into the atria from their own sources. This again continues until equal pressures are produced. The pacemaker then fires again and the

cardiac cycle is repeated.

The 'pulse' is created by the alteration in tension of the walls of the arteries due to blood being pumped through them in spasmodic bursts. Its propagation over the arterial system thus takes the form of a pressure wave, which travels along the arterial walls. Obviously like any other wave propagation, the pulse wave becomes attenuated, delayed and distorted by reflections.

To complete the definitions, the peak pressure reached during systole is referred to as the Systolic pressure and the value maintained during diastole is the diastolic pressure. The systolic pressure is produced by the pumping action of the heart, whereas the diastolic level is maintained by the contraction of the arteries, which is observed as the pulse wave.

In this work, the measurement of the pulse wave velocity will only be considered with reference to the principal systemic arteries; since these can be located easily and the pulse wave can be monitored with suitably designed transducers, through the relatively thin layers of surface tissue. Thus no surgical intervention, which could interfere with the physiological processes is necessary. The 'transducer pickups' and their design and performance are to be discussed in detail in Section 5.

A survey of previous work in the field follows.

Basically the work can be divided into three categories:

1) Analytical relationships between pulse wave velocity and blood pressure.

2) The clinical aspects of pulse wave velocity.

3) Methods of measuring pulse wave velocity and blood pressure.

Considering the category 1) it appears that the first consideration was by Moens in 1878, when he stated that the pulse wave velocity, v, could be expressed as:-

$$v = F \left[\frac{E\, e_o}{2\rho r}\right]^{\frac{1}{2}}$$

Where E = Young's Modulus

r = Internal Radius of the tube

e_o = Wall thickness

F = Constant found $\propto$ 0.8 in man.

ρ = Density of Blood $\propto$ 1.055

The expression as it stands has too many unknown factors and thus it was shown by Bramwell and Hill (1), that we can express the term $\left[\frac{2r}{E\, e_o}\right]$ in terms of a volume modulus as $\frac{1}{V} \cdot \frac{\partial V}{\partial p}$.

This simplifies the expression to the one given below:-

P.W.V. = v = 3.57/(% Increase in Volume per mm Hg increase in pressure)$^{\frac{1}{2}}$

The above expression was accepted as approximate, but usable by most authors until much later when King, (12), takes into account changing wall thickness and other factors and expresses

the pulse wave velocity as,

$$v^2 = \frac{A}{4\rho}\left[\left(\frac{2Br'}{r_o} - 1\right)\left\{\frac{\rho' - \rho_o}{A} + \left(\frac{r_o}{r'}\right)^{3/2}\right\} + 3\left(\frac{r_o}{r'}\right)^{3/2}\right]$$

Where $A = e_o \rho_o / 2r_o$

$$B = \beta u^1 \sinh^2 u^1 \Big/ \left(\sinh^2 u' - (u')^2\right)$$

and u' is defined by:-

$$\coth u' = \frac{1}{u'} + \frac{\beta r'}{r_o}$$

In these relationships β is an age dependant constant, characterising the elastomeric wall, which is the ratio of circumference of the tube to the maximal length of the molecular chain. The 'o' suffix refers to the dimensions considered when the pressure is zero, and ' symbols refer to the values when the pressure is p. He defined mean blood pressure as the mean value of the systolic and diastolic values. The above relationship gives increased velocity with increase in the pressure or age asfound in practice.

In his report he plots sets of curves given by the above expression, of pulse wave velocity to pressure and age. After this period certain texts have chapters devoted to the subject. (19), (26), (30). In the most recent of these the author is Hardung (30), whose treatment of the subject is thorough, but too long to condense into this report. He, like King, derives the Moens expression and extends the work to take into account factors not previously considered.

The true analytical relationship between pulse wave velocity and blood pressure is complex, and thus many of the early workers ignored this relationship and concentrated on a more clinical study.

Bramwell and Hill (2), studied the relationship of PWV to age on excised arteries and found that the velocity increased with age. Bramwell, Downing and Hill (3), noted that an S shaped curve was obtained for PWV with respect to pressure, which was fairly linear over the normal range of blood pressures. Also that the shape of this curve was related to age. Bramwell, McDowall and McSwiney (4), studied the effect of varying pressure on the PWV in living subjects by applying a syphygmomanometer bandage around the patient's arm, and varying the pressure in this manner. The PWV was measured, directly as a time delay. The results, they obtained, suggested a linear relationship with pressure. This work was verified by Hemingway, McSwiney and Allison (7).

Hickson and McSwiney, again working with living subjects measured the pulse wave velocity over approximately 50 cm. of brachial artery, by direct time measurement, and compared their results with the blood pressure.

The previous investigators accepted the modified Moens equation relating PWV to blood pressure and found that in certain circumstances it could be applied.

A good summary paper of work up to this stage is that by Hallock (8), who lists the findings of most of the previous authors.

Dow and Hamilton appear to be some of the earliest workers to attempt to verify Moens modified equation, and in their studies of PWV in dogs, found that the velocity varied with the distance from the aorta. They were however, able to account for the variations in terms of the change in elasticity of the arteries concerned. They also made a comparison between diastolic pressure and PWV.

Porjé's (11), is a later report (1946) which summarizes earlier papers in some detail. He, experimentally, has taken a sample of 58 healthy persons and examined their pulse waves with the aid of Fourier Analysis. The system he used was that of a piezo-electric pulse microphone coupled to an ECG amplifier/recorder. He takes his studies into some detail but a brief summary of his conclusions is given. The waveform itself is almost completely defined by the fundamental, second and third harmonies, of which the fundamental is the strongest. It consists of both initial and reflected components, and the reflected wave consists basically of the fundamental frequency. The higher harmonics present are transmitted, virtually without reflections, and the velocity of all components increases with the age of the artery. For interest, he also studied a number of pathological cases. In several cases he noted various differences in the waveforms. These included a more dominant fundamental component.

The reflected waves were increased, and the second harmonic was also reflected. The overall wave velocity was increased.

This report is of some value in that he gives typical pulse curves and also details of his pulse microphone, including a frequency response. He also appears to have been the first to analyse his waveforms by Fourier analysis.

However after this point little interest appears to be shown in PWV as a clinical parameter until Weltmann (21) produced what appears to be one of the first continuous pulse wave velocity monitoring devices. In his report he includes the action of the pulse wave under certain conditions, of stress etc. PWV measurement as a replacement for blood pressure is considered unsuitable at the moment by Webb Associates, (28),(31), due to the inaccuracies in the measuring systems, and hence this is sufficient licence for this work to be started.

The measurement of pulse wave velocity is a relatively simple process which consists of merely timing a pulse along a known length of artery. From these figures one can then easily compute the velocity. The early researchers, in general, used hot wire sphygmographs in conjunction with Einthoven galvanometers. The recordings were compared and the delay computed. However to obtain reasonable results large delays were required and hence the measurement of the arterial path became another problem. Porjé (11) used a similar method with his pulse microphone pickups. However for continuous recordings Weltmann, (and Sullivan), (21),(29),

and Salisbury and Wickham (27), appear to be the sole contributors to the field.

In the field of automatic blood pressure recording significantly more work appears to have been done, Gilson (10), Noble (13), Landsman (14), Green (16), Cooper and Richardson (22), Webb Associates (28),(31), ITT Federal Laboratories (33), Thompson (34), Van Bergen (35). The above is merely a selection of the references which are available. The basic technique is that described by Gilson (10), and uses an occluding cuff. However Van Bergen (35) estimates that this kind of measurement is subject to errors of 25%, or more. Thus production of a device which can measure pulse wave velocity, automatically, to a higher accuracy, could well have some useful applications.

Reviewing the measurement techniques adopted previously shows that Weltmann (21), computes the pulse wave velocity, by measuring the delay between the ECG and the pulse recorded at some peripheral artery. He defines this as:-

$$PWV = L/I^*$$

Where L = Arterial length between the aortic arch and the peripheral pulse transducer.

I^* = Time interval between pulse expulsion from the heart and pulse arrival at the peripheral transducer.

$I^* = I - 40$ msec.

Where I = Actual time period measured which he states is that intervening between detection of the 'R' wave of the ECG complex

and detection of the leading edge of the arteral pulse.

To present this information in terms of a velocity, he utilises the time interval to produce a proportionate analogue voltage, which is fed into an analogue, division circuit , with another analogue voltage representing the length of artery 'L'. The solution is then fed to a suitable recording device.

Consideration of his approach shows that the computation of the velocity from the time measurement is best achieved with an anlogue circuit, since this produces sufficiently accurate results (1%) with the minimum of components. However as to the actual quantities used, there is some doubt as to whether his figures for PWV are entirely relevant to the case being considered here. The actual length of artery can only be estimated, and in addition the dimensions and constants for the artery are continually changing along its length. Thus, even if one accepts that the method of measurement is justified, the value obtained for the PWV can only be a 'mean' figure.

The object of this work is to measure the velocity over a shorter piece of artery, and so correspondingly the time measured will be proportionately shorter, and hence must be measured more accurately.

One can assume a typical figure of 5 msec for PWV (Porjé) (11), and a period of 800 msec, thus in one pulse period the pulse will travel, 4 m, which is some considerable distance. A typical length of artery which we can measure to a suitable accuracy

(2%) would be 10 cm, from which a delay of 20 msec would be obtained. This is extremely small when compared with its 800 msec period, and thus the real crux of the measurement problem appears. Also one must bear in mind that one cannot rely upon the waveform to be propagated without changing its shape, nor upon its amplitude remaining constant over a period of time. Thus, despite these difficulties a suitable solution has to be found.

Salisbury and Wickmann (27) have designed a system which overcomes these troubles by superimposing a sharp edge on the trailing edge of the pulse wave, and then detecting this edge at a known distance away, with a suitable pick-up. The edge is superimposed on the pulse waveform by a small pneumatic device mounted above the artery. The delay time is taken as that from when the pulse is injected to its detection after propagation.

This method offers a solution to the measurement of the small delay involved, but in doing so interferes with the physiological system. And thus until proven,otherwise, it must be assumed that this will affect the velocity of propagation. Hence one cannot at present take the results as reliable, and so the problem still remains of how to measure a time, of the order of 20 msec, as a delay to an ill-defined waveform of period 800 msec, to an accuracy of say 1%

SECTION 2

The Proposed System

In the previous section the problem has been stated and previous work in the field has been surveyed. From this the conclusion is that the crux of the problem is to measure a delay of the order of 20 msec in an ill-shapen waveform of 800 msec period. The waveform, which presents itself as a pressure wave in the arterial walls, must also be monitored with suitably designed transducers.

Thus the first consideration is that of a suitable transducer to convert this pressure wave into an electrical signal. Such a device is described by Davies et al (32), in a recent paper. They indicate that faithful recordings of the pulse wave can be obtained with a device of the kind they are using. The transducer to be used here, is of a similar design to that used by Davies, and its development will be discussed in Section 5. It was considered that the scope of this project was already sufficient and the development of the transducer would be undertaken as a separate exercise. To enable the system to be developed without a transducer it was decided to make a 'Simulator', which would produce an electrical signal similar to that delivered by the transducers. The detailed requirements and design of this Simulator are discussed in Section 3.

The method of measurement of pulse wave velocity here will be to monitor the delay over a known length of artery, and from this compute the velocity at which the wave is travelling.

Thus for ease of description it will help to divide the work into various sub-sections.

The transducer will require some form of pre-amplifier to isolate it from the main system. The pre-amplifier design is governed by the characteristics of the transducer and will be considered in Section 5, with the transducer.

In addition a gain-controlled stage will be required to enable the signal obtained from the transducer to be of a constant output amplitude, and independent of the operating conditions.

Following these initial stages, the main system can be considered. The first function required is to measure the time delay between the two waveforms. This delay must also be presented in a suitable form to drive the division system which follows it. An analogue system can achieve the accuracy required (1%), with the minimum of expense. Here, as with previous authors, the delay is translated into an analogue voltage by the delay measuring system. Thus, the division system also becomes an analogue device. The two inputs to the division system are the time delay and the arterial length used. The arterial length can be supplied from a previously calibrated voltage source.

After obtaining the output from the division system, that is, the pulse wave velocity, it must be displayed in a suitable manner.

The salient features of the system are now discussed.

Section 2.1

Gain Control

The various methods of gain control, and the system selected are discussed in Section 4. The purpose of this stage is to enable a constant output signal to be provided from the transducers. This apparatus is intended for general application and the design of the system should allow for a maximum variation of the input signal.

A Gain control system, can, in general, be made to respond to either the mean or peak values, of the input signal. Here, for reasons that will become obvious, a system has been selected that responds to the peak value.

Section 2.2

Delay Measurement

Assuming that the signals supplied by the gain control amplifiers differ only in phase, and are of a constant amplitude, then a number of measuring techniques are available.

A possible method would be to define a point on each waveform by its dc level, and then use a level sensitive detector, such as a Schmitt trigger circuit, to produce a pulse edge at this instant in time. However, the resolution obtainable in this way is low, since the edges of the signal are extremely slow.

A technique based on the Lissajou figures, could be used to measure the phase difference of the fundamental components of the two signals. The frequency of this component may, however, change by a factor of 3 in a healthy subject and active filters would be required. This is a problem that could be solved, but still remains the problem of the high resolution required.

Here a novel approach has been considered, and a suitable system built round it. If one assumes that the length of artery is small and of a uniform nature, then apart from the phase shift the signal at either end will be the same. This being so the phase shift could be defined as the delay between the two peak values. (A typical pulse waveform is shown in fig. 2.2.1.). The peak value is a significant point which occurs in all pulse waves, and thus, this definition would be valid for all cases.

To measure the delay between the two pulse peaks the signal is 'processed' by amplifying it exponentially. That is with an amplifier with a characteristic of the form:-

$$V_o = A \exp(BV_1)$$

This kind of amplification selectively amplifies the peak value of the signal and in doing so 'sharpens' it. The effect on the waveform is shown in fig. 2.2.2. and obviously as many stages as required can be used. There is, however, the

requirement that the agc stage goes 'hand in hand' with this amplification since too large or small an input signal will result in an overloaded or zero output.

Exponential amplification does not remove any information from the signal since the original can be reconstituted by logarithmic re-amplification. Thus, providing the gain control is effective, then this system will perform the task required. In order to define the time at which the peak occurs, the signal is differentiated as shown in fig. 2.2.3. and gives a fast negative going edge coincident with the peak. This edge is used to trigger a pulse generator and produce a pulse of finite length, the leading edge of which defines the time at which the peak occurs.

To measure the delay this pulse is applied to a gating circuit together with the signal from the second channel. The output of the gate is a pulse, the length of which is the measured delay. This system is shown in fig. 2.2.4.

It is necessary to present the output in analogue form, which will require that the pulse is integrated. As continuous operation is required, a time period, and trigger signal, with which to reset the integrator are required. This period is produced by delaying the front edge of each of the pulses by the same amount. This delay period can

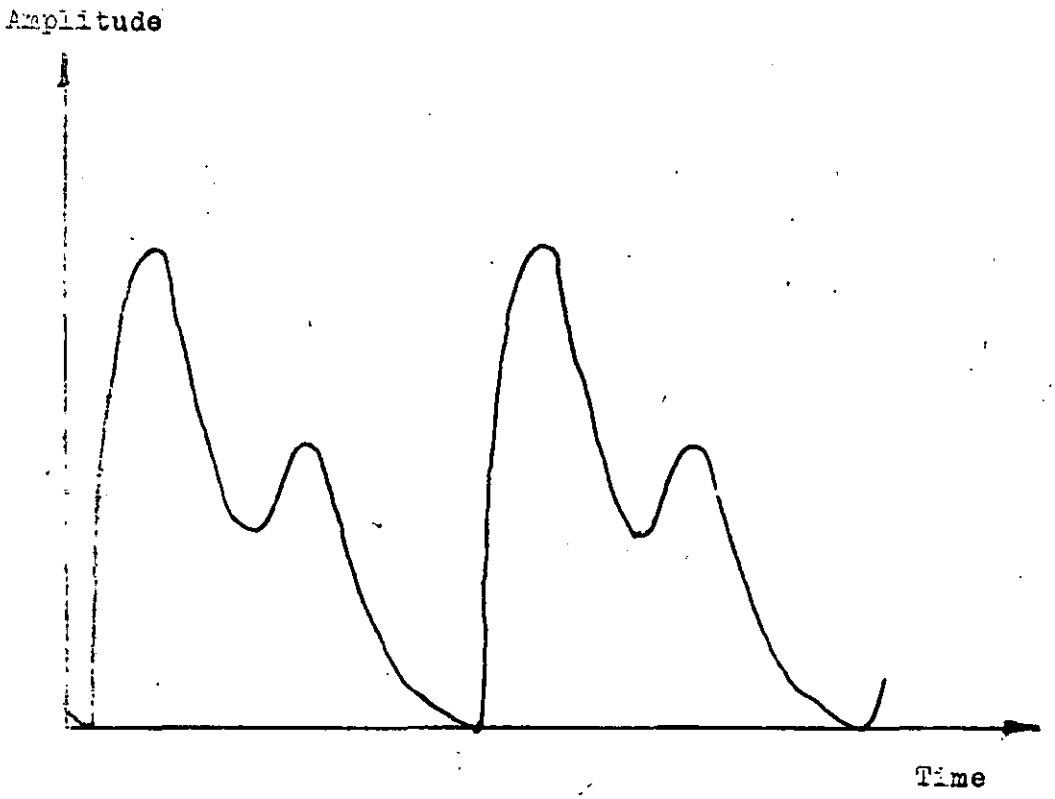


Fig. 2.2.1.

Typical Pulse Wave

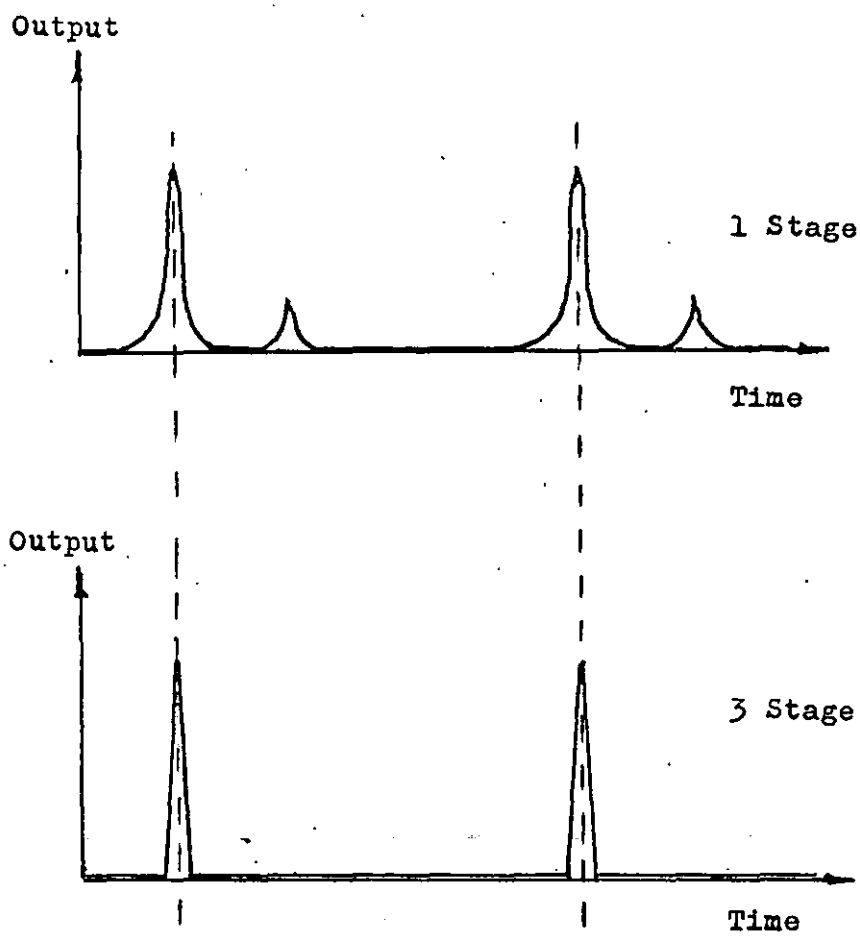


Fig. 2.2.2.

Exponentially Amplified Pulse Waves

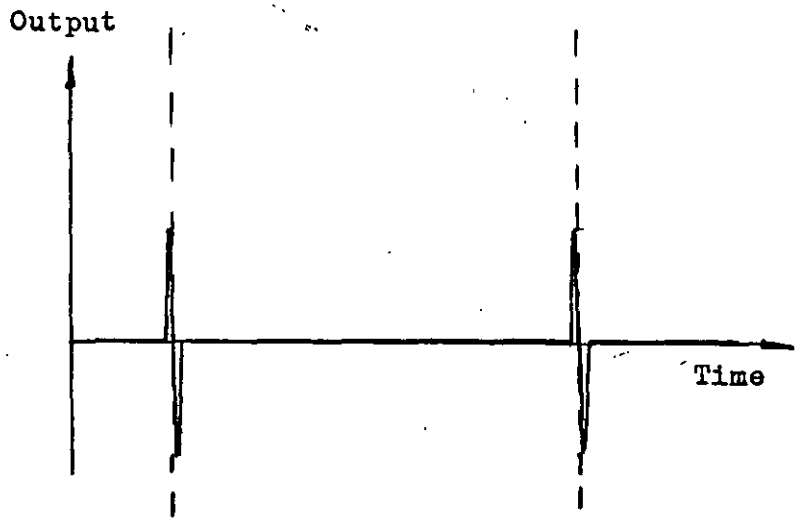


Fig. 2.2.3. Differential of Above Signal.

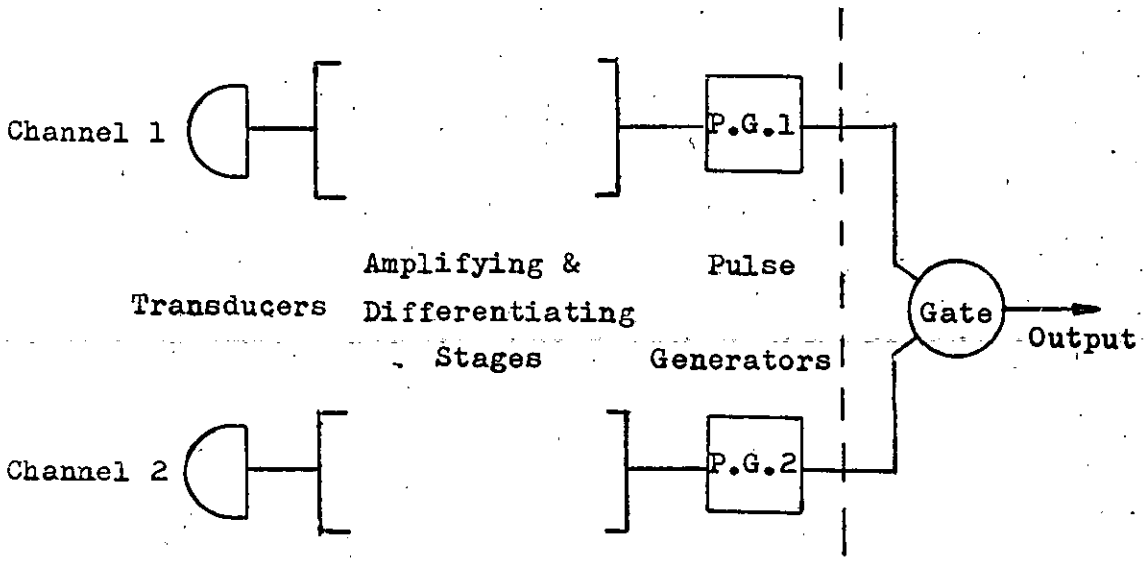


Fig. 2.2.4

Proposed System

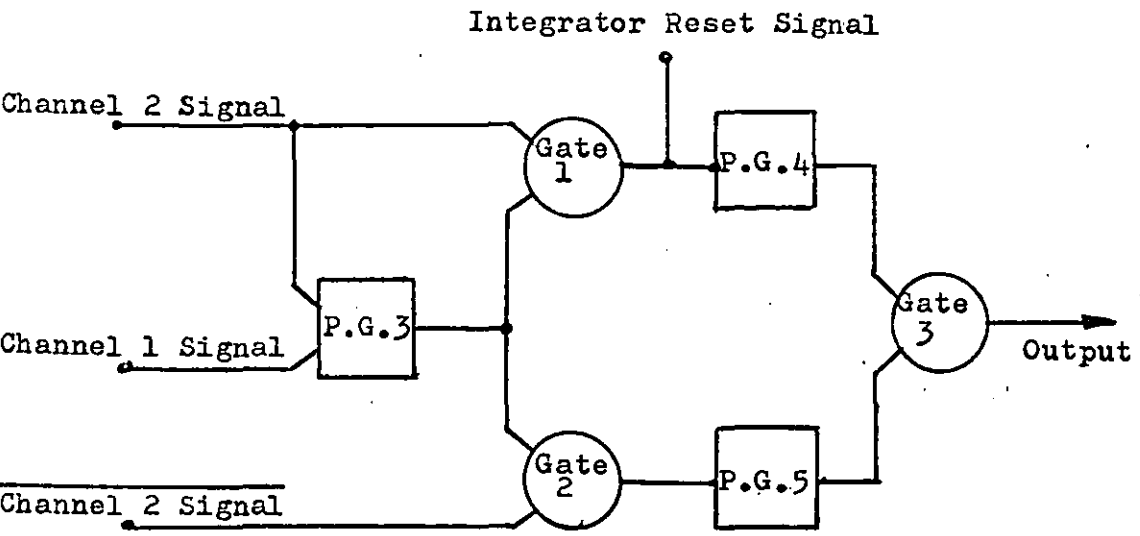


Fig. 2.2.5

Modification to Provide for an Integrator Resetting Signal

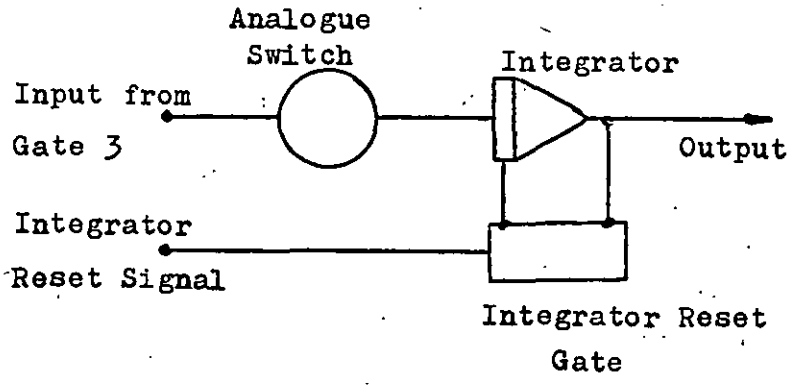


Fig. 2.2.6

Integrator Configuration

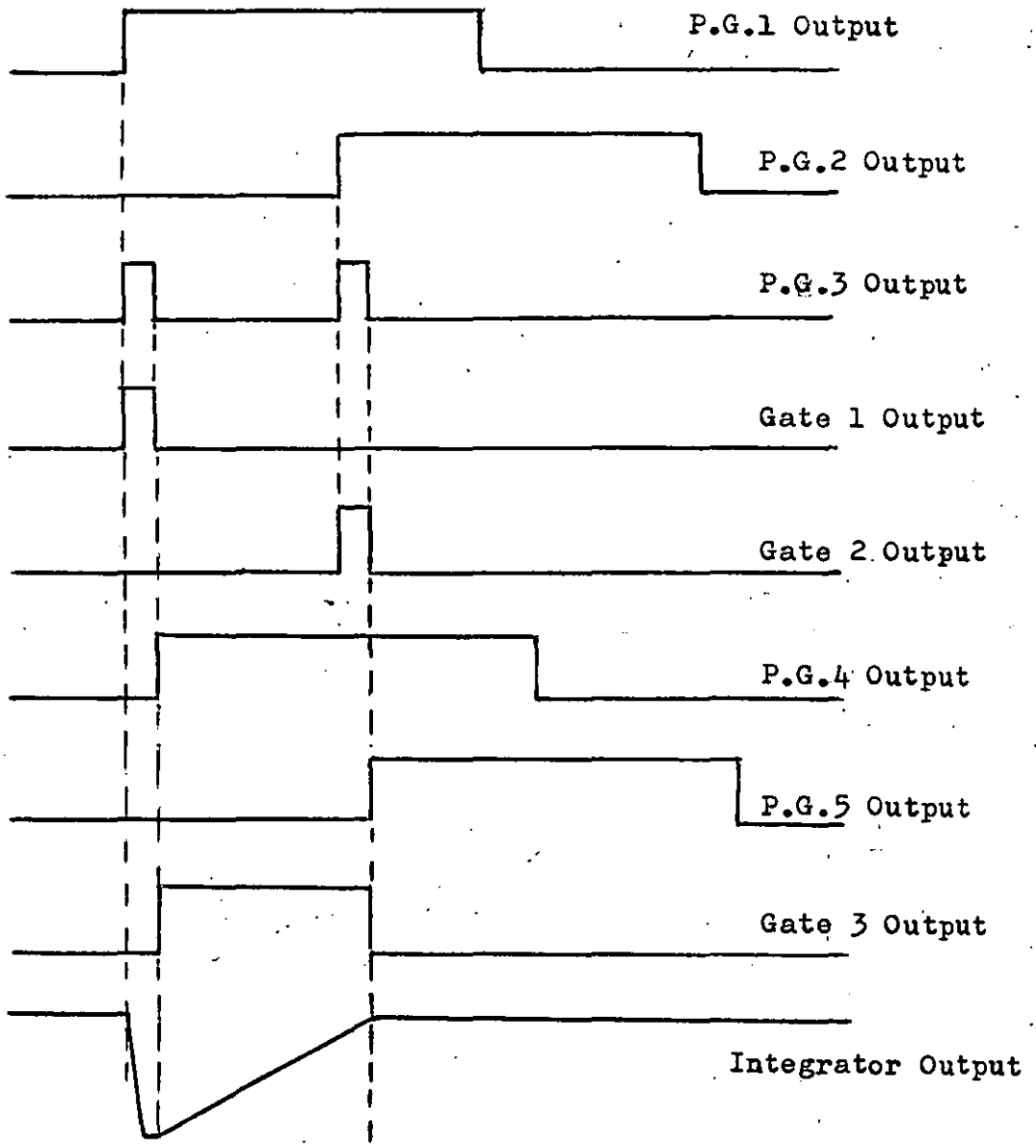


Fig. 2.2.7

Theoretical Waveforms Related to the Delay Measuring System
(as shown in fig. 2.2.4 - 2.2.6)

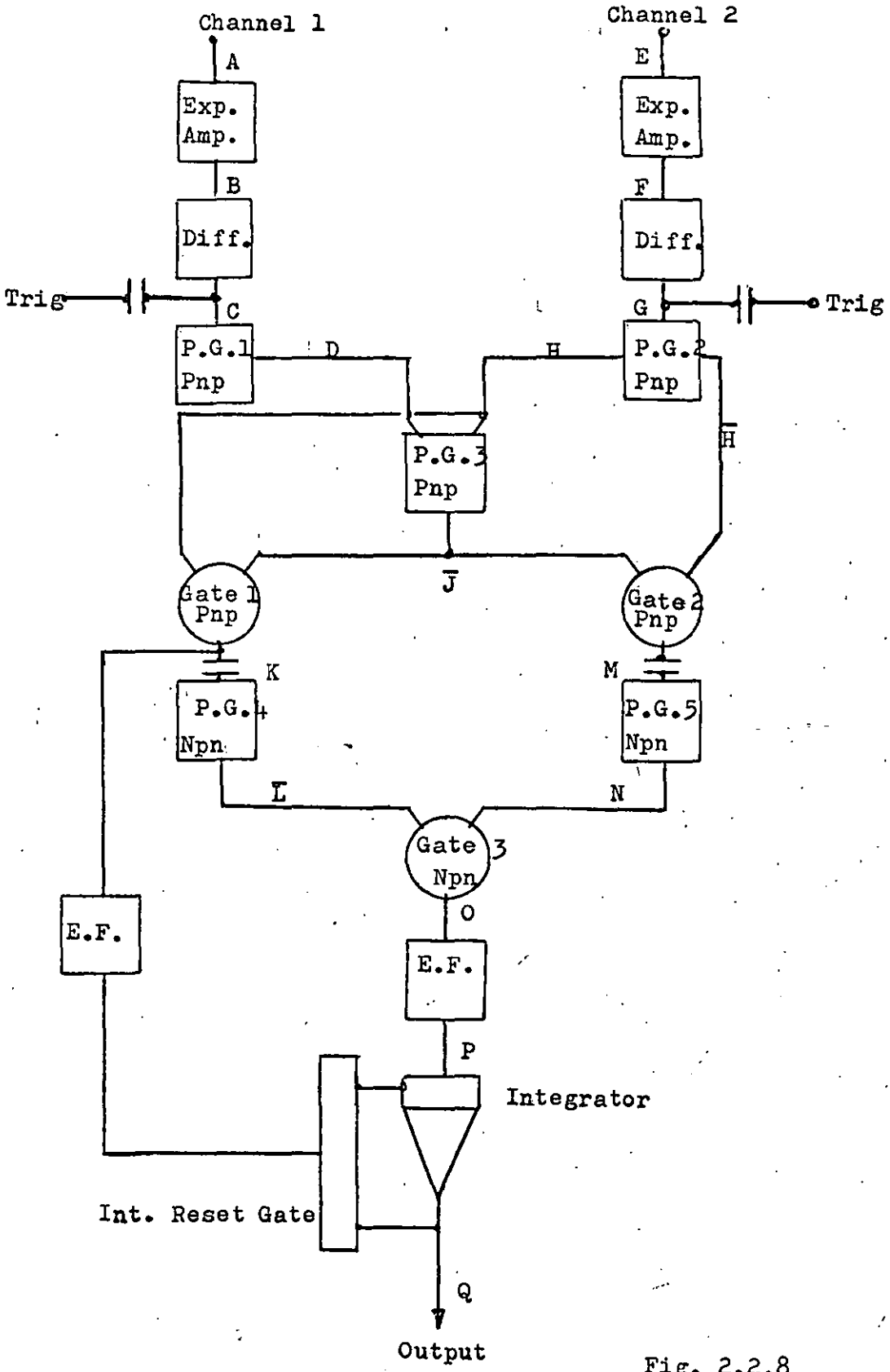


Fig. 2.2.8

Actual Delay Measuring System

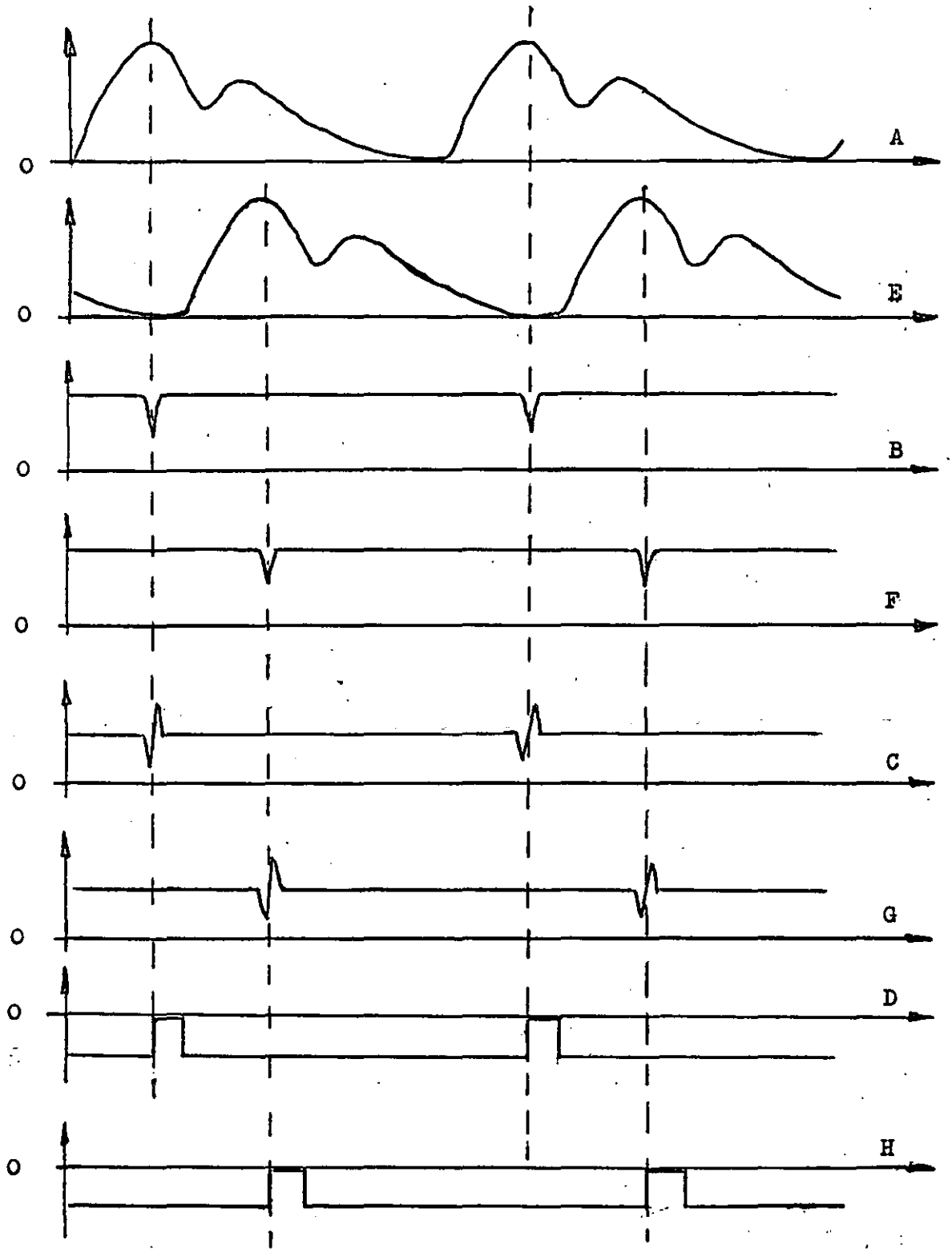


Fig. 2.2.9

Actual Waveforms for the Delay Measuring System

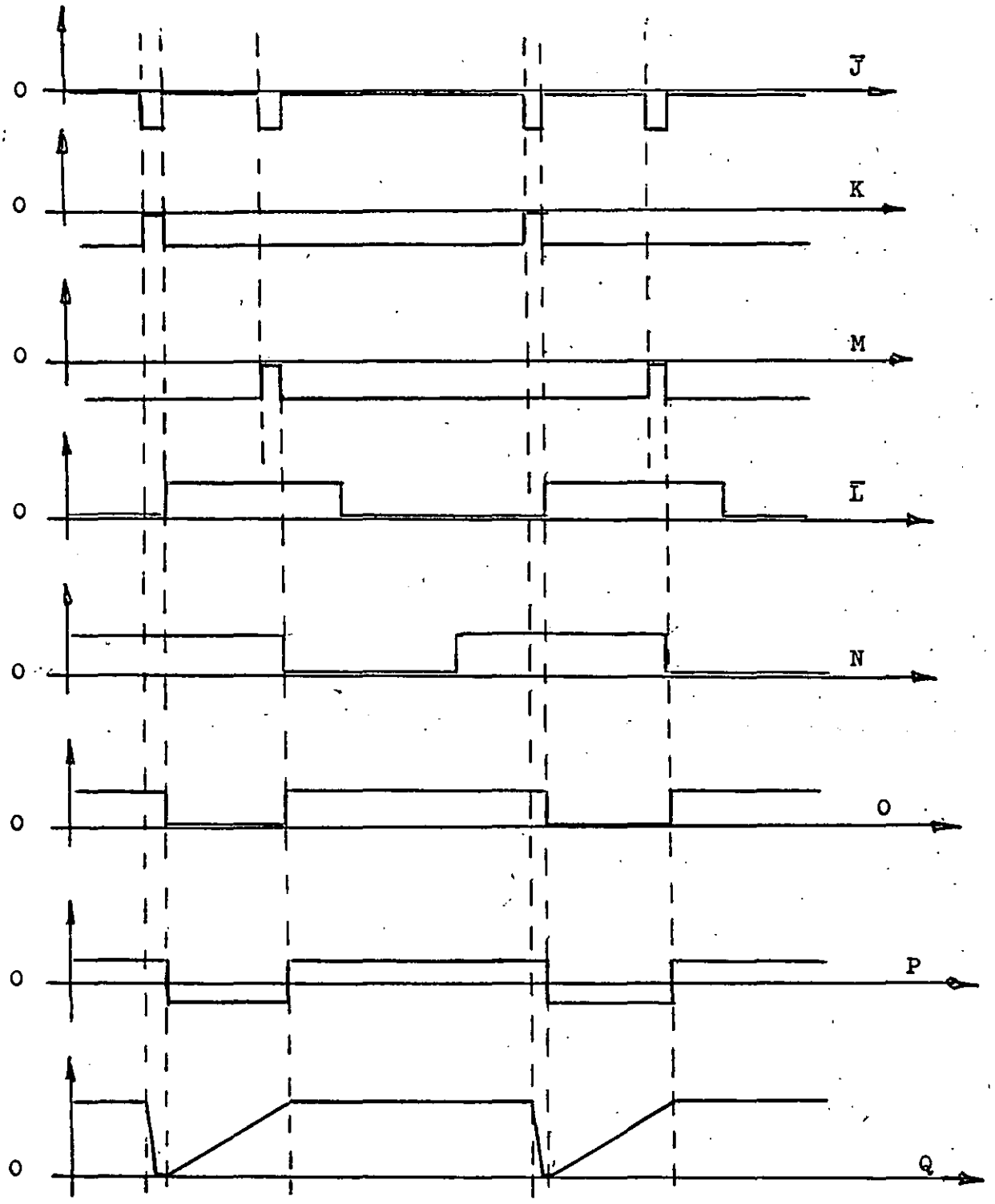


Fig. 2.2.9 (Contd.)

Actual Waveforms for the Delay Measuring System

then be used to reset the integrator. To perform this function the system as shown in fig. 2.2.5., is used. The original pulses are both fed into PG3 as shown. This generator produces a short delay pulse from each leading edge, these delay pulses are then routed back to their original channels by the logic shown. From the rear edge of these delay pulses further pulse generators are triggered to give the original signals in their delayed forms. The integrator reset drive is the channel 1 delay pulse, as shown. Waveforms relating to this figure, and to fig. 2.2.6, are shown in fig. 2.2.7. However, these waveforms may not apply directly to the real system since they are all assumed positive. The real system is discussed in Section 2.2.1.

The integrator is shown in fig. 2.2.6, and in addition to translating the pulse into an analogue signal, it serves as an analogue storage element for the system.

Section 2.2.1

The Actual Delay Measuring System

The actual system used for the delay measurement is shown in fig. 2.2.8, and the waveforms related to this system are shown in fig. 2.2.9. The input to both channels is required to be positive since simple exponential amplifiers have been used and they will only function for a single polarity input.

A three stage exponential amplifier is used to give the required definition to the system. The amplifier response

cam be found in Section 4.

The differentiator consists of a single stage performing the differentiation, ac coupled to a voltage amplifying stage which is needed to give sufficient output to drive the pulse generator following it.

The pulse generator produces a 2msec pulse which is a positive going pulse, between negative and earth. An additional input capacitor is provided to this stage to enable the system to be run without using the exponential stages if required. The pulse wave simulator will have a facility provided so that it can also drive the system at this point, if required.

From these outputs a 0.2 msec pulse is generated by PG3, for each pulse. Diodes have had to be included on the inputs to PG3 to avoid feedback. From this pulse generator the inverse output is taken, that is a negative going pulse between earth and negative. This signal is then fed into gates 1 and 2, as shown. For the channel 1 'delay pulse', it is necessary to gate this signal with the previous channel 2 output in its normal form, since this signal will inhibit the gate when a channel 2 output is present. Thus for the channel 2 output the gating is with the inverse original channel 2 signal. From these 'delay pulses', a pulse is produced from the rear edges by pulse generators 4 & 5, of 200 msec duration.

These pulses are then combined in gate 3 to give a pulse, the duration of which is the required delay. This is achieved by gating the inverse channel 1 signal and the normal channel 2

signal. The inverse channel 1 signal inhibits the gate until the pulse is present, the channel two signal closes the gate on the front edge of the pulse. Thus the gate output signal is of the required duration. This signal consists of a negative going pulse between positive and earth. This is then fed via a zener diode voltage shifting network into an emitter follower to provide a suitable low source impedance for the integrator.

The output is fed into the integrator via a silicon diode. The purpose of this diode is to avoid the necessity of setting the quiescent state of the output pulse to earth potential, since only that portion of the output negative with respect to earth will be transmitted. This facility is particularly important since the integrator also stores the delay as an analogue voltage, and slight discrepancies of the quiescent levels would cause the output to either continue rising slightly or to fall slightly, over the storage period. Using a diode, prevents this by ensuring that the diode is cut-off in the quiescent state; thus giving only its leakage current as an error input. For silicon devices the leakage is extremely small.

The integrator itself has been 'patched' to a gain of 20, as will be discussed later in this Section. The integrating capacitors are of a polystyrene type, which are suitable for this application, due to their low leakage characteristics.

Silicon transistors, which have low leakage characteristics, are used in the reset circuit. The drive to the reset gate

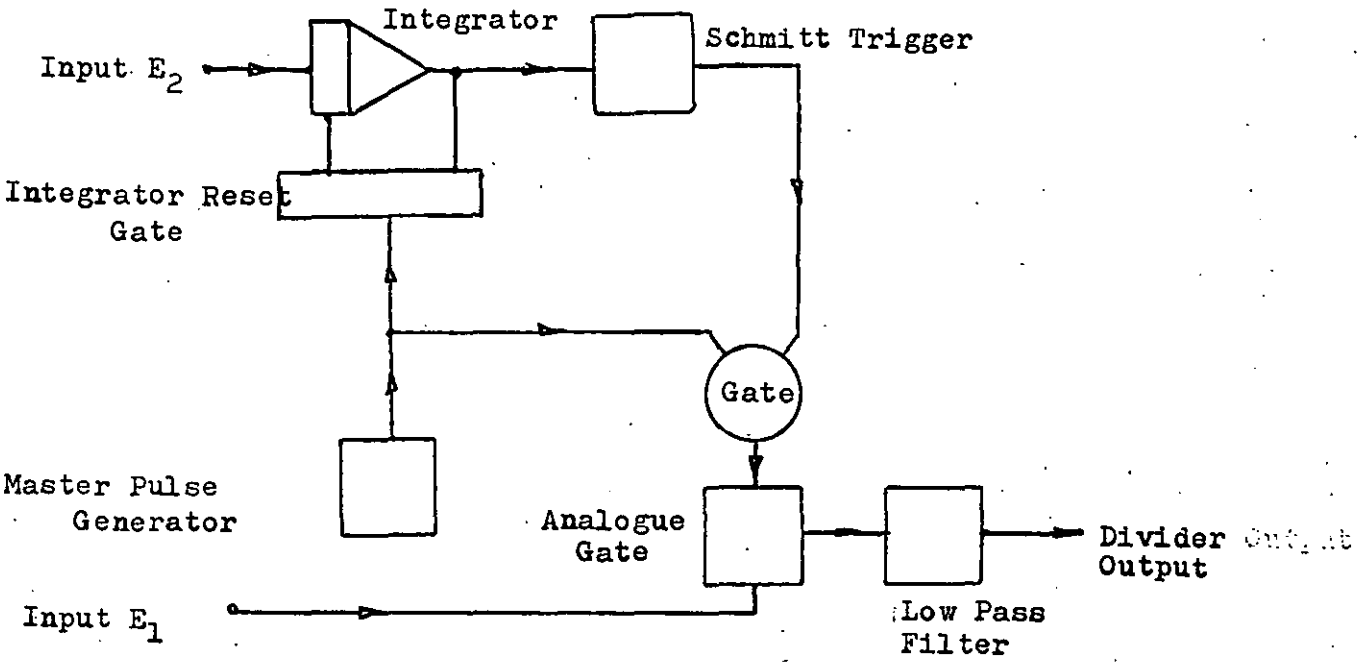


Fig. 2.3.1.

Pulse Width Analogue Division System

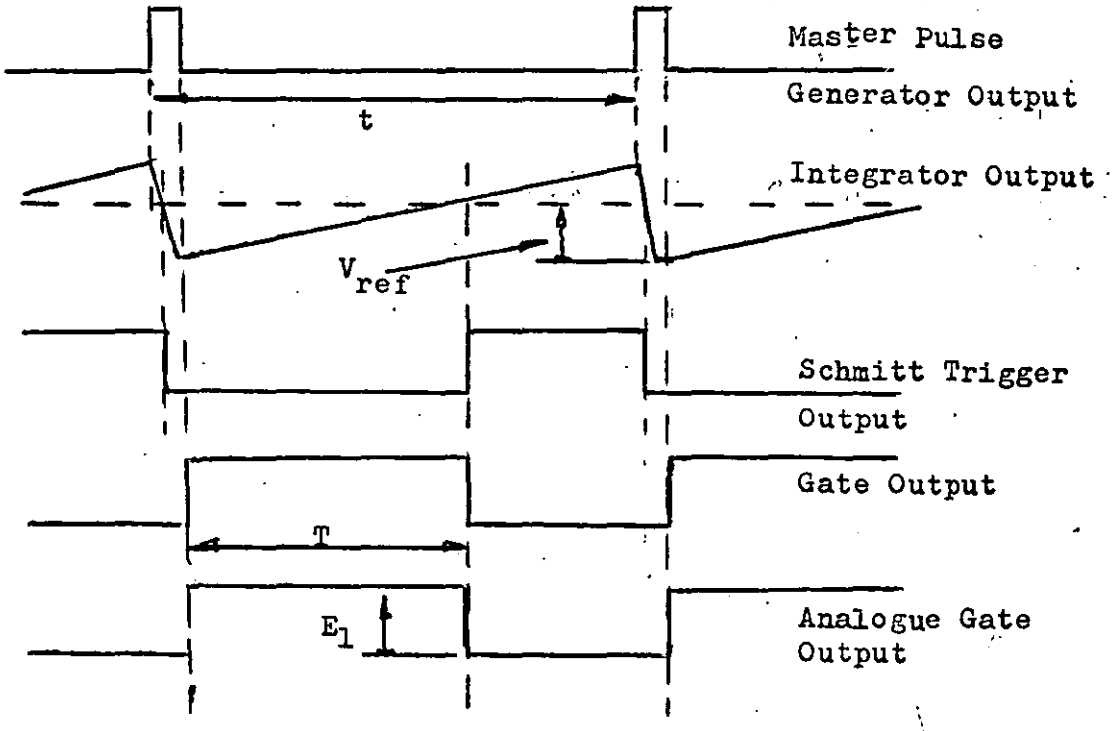


Fig. 2.3.2.

Waveforms Related to the System as shown in Fig. 2.3.1.

is fed via an emitter follower, to avoid loading the gate from which the signal is derived.

Section 2.3

Analogue Division

Analogue division can be accomplished by a number of standard techniques. However, in this case a single quadrant system will be sufficient. With this in mind a possible approach using logarithmic and exponential amplifiers was considered, similar to the system described by Cowell et al (48). This was rejected since the accuracy is solely dependent upon the manner in which the functions are generated. The simple approach using the non-linear characteristics of a junction diode has the disadvantage that the expression is dependent on temperature, (see Appendix C), and hence fluctuations in the temperature would affect the accuracy in a random manner. A second disadvantage is the large number of operational amplifiers that the system requires.

The system adopted, uses a pulse width technique, and the accuracy is dependent on the linearity of an integrator. The basic system is shown in fig. 2.3.1, and the related waveforms in fig. 2.3.2. Again all the waveforms are assumed positive.

The operation is as follows; an analogue voltage E_2, is fed into an integrator with an overall gain of A. After time period T, the integrator output will be given by, $V_o = E_2$ A.T.

When this integrator output exceeds a value of $V_o = V_{REF}$, which is set by the Schmitt trigger circuit, this circuit changes its state, as shown in fig. 2.3.2, and in doing so inhibits the gate, which had been previously opened at the initiation of the integration, by the master generator. Thus for this condition one obtains:-

$$V_o = V_{REF} = E_2 A.T.$$

$$\text{Thus} \quad T = V_{REF}/AE_2$$

To complete the cycle the master generator resets the integrator, via the resetting gate, and the reset integrator output resets the Schmitt trigger circuit. The master generator then inhibits the integrator's operation until the start of the next cycle. The process is then repeated at a high repetition rate.

The signal from the gate is used to switch an analogue gate on for period T, as shown. The dc component of the analogue gate output is given by:-

$$Vdc = \frac{E_1 T}{t} = \frac{E_1 V_{REF}}{t E_2 A} = k\left[\frac{E_1}{E_2}\right]$$

$$\text{Where } K = \left[\frac{V_{REF}}{A t}\right]$$

The dc component of this signal can be obtained by passing the signal through a low-pass filter as shown. As can be seen this dc voltage is directly proportional to the quotient (E_1/E_2), also the constant of proportionality is known = (V_{REF}/At)

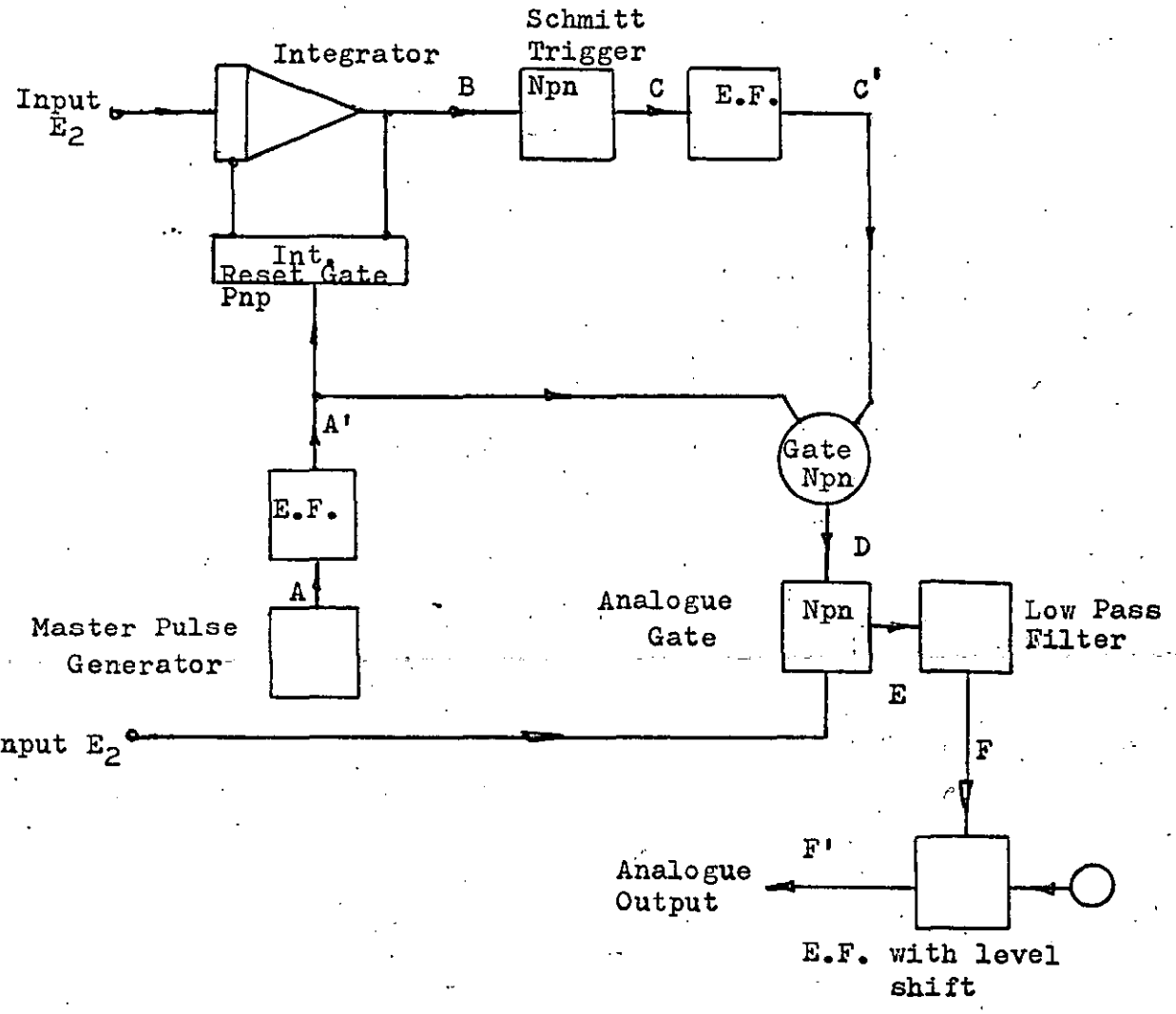


Fig. 2.3.3.

Actual Analogue Division System

Thus an analogue division has been performed, without using non-linear characteristics, upon which the accuracy is dependant.

The accuracy here is dependant upon linear operation of the integrator, stability of the reference voltage set by the Schmitt trigger circuit, and compensation for the saturation voltage of the analogue switch.

Section 2.3.1

The Analogue Division System

The system used for the analogue division is shown in fig. 2.3.3. As can be seen the system remains as before apart from the addition of several 'emitter follower' stages.

The input E_2 is from the delay measuring integrator and is a positive voltage. The inversion in the integrator produces a negative ramp. This ramp feeds into a Schmitt trigger circuit which consists of two npn transistors. The reference level of this circuit is set to approximately -4 volts, and when the ramp exceeds this level, in a negative sense, the device changes its state. The output is a negative going pulse edge from +10 volts to earth. This edge is used to close an npn gate, as shown, which was previously opened by the master generator. This generator is an astable pulse generator using two pnp transistors and operating between +10 volts and earth. The mark:space ratio is approximately 6:1 with an overall prf of 7 kc/sec.

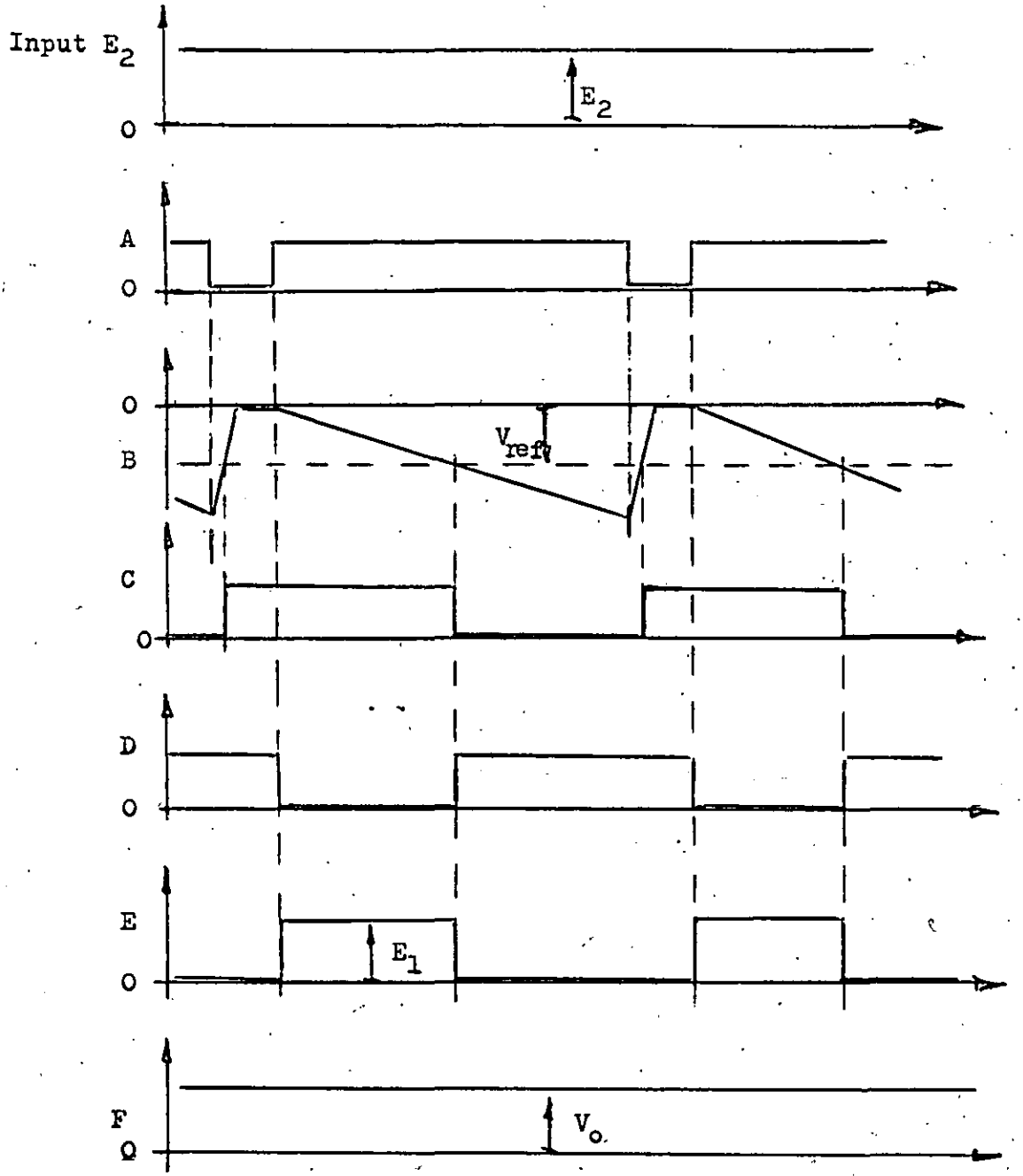


Fig. 2.3.4.

Waveforms Related to Fig. 2.3.3.

The large mark:space ratio is used for two reasons.

i) Only a short period is required in which to discharge the integrator.

ii) The accuracy of the system is directly related to this ratio.

The master generator also drives the integrator reset circuit, consisting of two pnp germanium transistors. The integrator has been 'patched' to a gain of approximately 50,000. This high gain is required for the system to function correctly at the high repetition frequency.

The npn gate is followed by a similar gate, used as an analogue switch, to which the E_1 input, representing the arterial length, is taken. The switched analogue output is then fed into a low pass RC filter with a 3dB cut-off frequency at approximately 5 c/sec. The output then appears as a dc voltage and is fed via a high input impedance emitter follower, to the output voltmeter. This circuit has variable biasing, to enable the output level to be set as required.

The waveforms relating to this system are shown in fig. 2.3.4.

The results of tests performed on the system are given in Section 6.

Section 2.4

Display facilities

With apparatus of this kind it is normal to display the results in analogue form on a roll of paper tape. In this case the display facilities are simple and consist of a moving

coil volt meter, mounted on the front of the apparatus which gives a direct reading of the divider output signal. To avoid loading the filter an emitter follower, with a variable bias facility is included as a buffer stage.

The voltmeter has two ranges so that the PWV can be read on a 0-10 m/sec or 0-50 m/sec scale.

A facility is provided for the addition of an external 100μA recording ammeter.

The calibration of the device, is described in the following section.

A circuit diagram is included in Appendix A.

Section 2.5

System Standardisation and Calibration

In order that the individual units will function correctly when combined they must be compatible. The range of transducer output signals must be determined, and the required range of operation of the device in terms of arterial length and velocity must also be considered.

The change in transducer output affects only the requirements of the gain control system and will be discussed in Section 4.

The standard pulse wave velocity appears to be of the order of 5 m/sec,, the delay can be measured in the range 10 msec to 100 msec. At 'standard' velocity this would give distances of 5 cm to 50 cm, arterial length, which would seem acceptable dimensions.

Let the gain of the Delay Measuring Integrator be, A, and that of the Division Integrator, G. The input pulse to the delay measuring amplifier is approximately 5 volts. Thus for a time period of length t, the output from the delay measuring integrator will be; $V_o = 5At$ volts.

With the division integrator, the minimum input voltage required is set by the timing period, the gain and the Schmitt reference level. In the complete integrating period the integrator output should be equal to V_{REF}, when the input voltage is a minimum. This time period is approximately 120 μsec (with 20 μsec off).

$$\text{Thus } V_{IN}(\text{Min}) = V_{REF}/G \; 120.10^{-6} \text{ volts.}$$

The minimum output from the delay measuring integrator is given by:-

$$V_o(\text{Min}) = 5A.10^{-2} \text{ volts.}$$

The maximum output from this integrator must not exceed 8 volts, otherwise the amplifier will saturate; thus

$$V_o(\text{Max}) = 8 = 5A.10^{-1} \text{ volts.}$$

The gain A is thus 16, in the actual circuit the gain is nominally 20, using preferred values.

This then gives a minimum output of

$$V_o(\text{Min}) = 1 \text{ volt.}$$

Now $V_{REF} \simeq 4$ volts, and hence G = 33,000.

In an attempt to improve on the 10 msec figure, stated earlier, the actual gain, on preferred values, has been set to 50,000.

The final task requires choosing suitable multipliers for the output meter. These were found experimentally and the values are given in Appendix A.

The calibration of the system requires that the component parts are functioning correctly and that the simulator has been standardised. Standardisation of the simulator infers that the position of the 50 msec delay is known accurately on the scale.

The 'Set L' arterial length control consists of a 10 turn helical potentiometer, the total output of which represents 50 cm.; the full scale reading is 100, this must be divided by 2 to obtain the arterial length in cm.

To calibrate the computer the unshaped simulator outputs are fed into the computer at the trigger points provided in the delay measuring system. The delay should be set to 50 msec, and the input to the delay-measuring integrator examined. This output should be set to a steady d.c. value by means of the 'Set Zero' control on the 'Set L' voltage generator.

This sets the zero level of the dc voltage from the 'Set L' control to $V_{CE}(SAT)$ to compensate for the saturation voltage of the switching transistor.

With the meter on the X1 range, the variable biasing of the emitter follower, which drives the meter, is used to set the zero position. This compensates for the offset voltage produced by the preceding circuits.

Set the 'Set L' scale to 25 cm (50 div), and with a 50 msec delay, set the meter to read 5 m/sec on the X1 range using the appropriate multiplier; then to 5 m/sec on the X5 range by adjusting the series multiplier.

This completes the calibration and the device is now ready for use. The above procedure has assumed that the integrators are functioning correctly and that the amplifiers are balanced. The balancing procedure for the amplifiers is given in Appendix A.

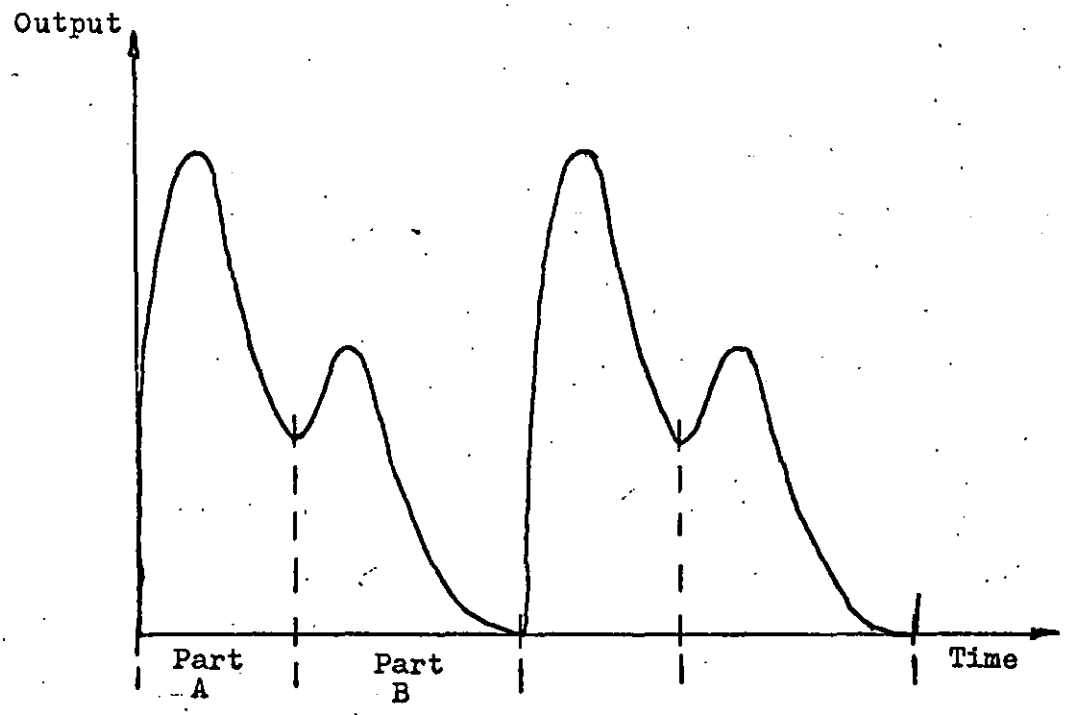


Fig. 3.1.

Typical Arterial Pulse Wave

SECTION 3

The Pulse Wave Simulator

As stated in section 2, a refinement that can be used for the development and testing of the system, is that of a signal source simulator. The body is not an ideal source of signals for the development of the 'electronics', since the shape, rate, and amplitude of the signal depend upon the conditions under which the body is functioning.

The simulator will be required to give an electrical signal, which represents the transducer output under typical conditions; but is sufficiently flexible, in its design, to enable the waveform to be modified if required.

The degree to which the simulated signal compares with the real one can be found by performing a harmonic analysis on each of the waveforms, and then comparing the results. The results from such harmonic analyses can be found in Section 6.

The basic shape of the arterial pulse wave is well established and equipment is now available on the consumer market to display pulse waves. A typical pulse wave is shown in fig. 3.1, and obviously there are many ways in which a waveform of this nature could be simulated. However, in addition to the requirements mentioned above, there are certain specific requirements here. These are that two outputs are required, one delayed by a variable amount from the other. The two channels should produce similar, or dissimilar, signals as required by the real system. The output amplitude should be

variable from zero, and independent on both channels. Also the signal should come from a low impedance source so that any kind of transducer output impedance can be simulated. For example for a piezo-electric transducer the signal would be fed via a capacitor, of the same value as the device.

A brief survey of the methods of simulation of such a signal, bearing these points in mind should justify the use of the final system.

Both mechanical and electrical techniques are available, in this instance, due to the low frequency nature of the signal. A possible mechanical method would be to cut a cam to the required profile, and this coupled to a motor could be used to drive the wiper of a potentiometer, thus giving the required signal output. This technique does not lend itself to a second channel, delayed by a variable quantity, or to a variably shaped waveform. It could be used to give a variable frequency signal, by altering the motor speed. But, the worst case frequency, that is the lowest frequency required would be sufficient, to test the system.

Of the electrical methods of simulation, the simplest, in theory, would be to sum the various harmonic components of the signal. Variable shape could be obtained by altering the amplitude and or the phase of these components. However to produce a second waveform, with a variable delay would be extremely difficult to achieve.

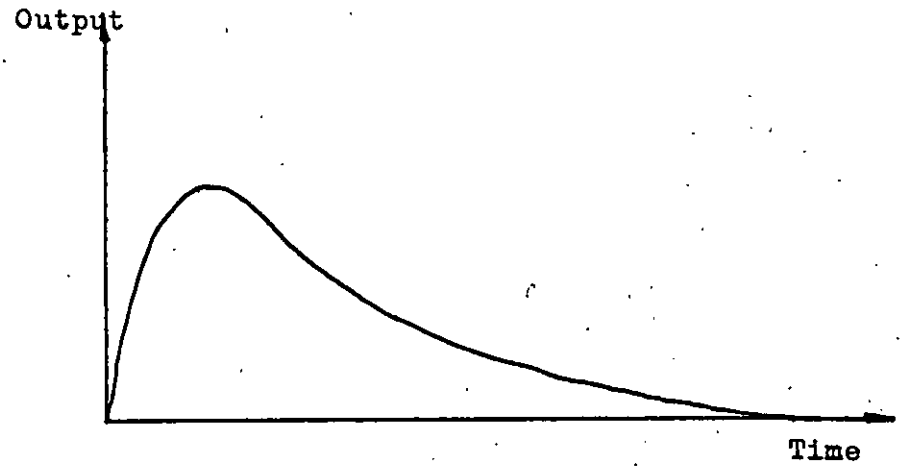


Fig. 3.2.

Exponentially Shaped Step Input

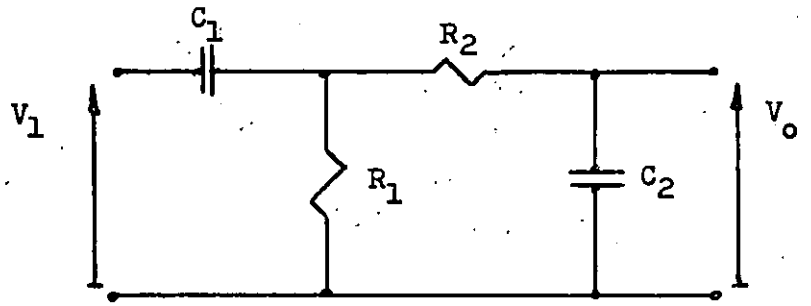


Fig. 3.3.

RC Shaping Network

A simple, yet practical solution is to produce the waveform by shaping one or more square waves, and then adding them together. Obviously, the technique has limitations in that continuous curves are forced to be exponentials. However careful consideration of the typical pulse wave as shown in fig. 3.1., shows that the wave consists, or could be considered to consist, of two parts, A and B in the diagram, each of which is similar in shape, there being a difference in phase and amplitude. Fig. 3.2 gives the double exponential shape produced when a step input is fed into an RC network as shown in fig. 3.3. This double exponential curve could be used to simulate part A of the pulse wave, and a similar, but delayed and attenuated signal, could be used to simulate part B.

The output could be produced by adding the signals algebraically, or by switching the output from one waveform to the other. The latter technique has been adopted since the two parts are then completely independent of each other. The circuit used to perform this switching is described in Section 4.6, and it is sufficient to say here that the 'Analogue Gate' requires switching signals, from low impedance sources, of both polarities. The analogue input is required to be of a small amplitude, less than 500mV, and appear from a source with a quiescent dc level that is negative by approximately 1 volt with respect to earth.

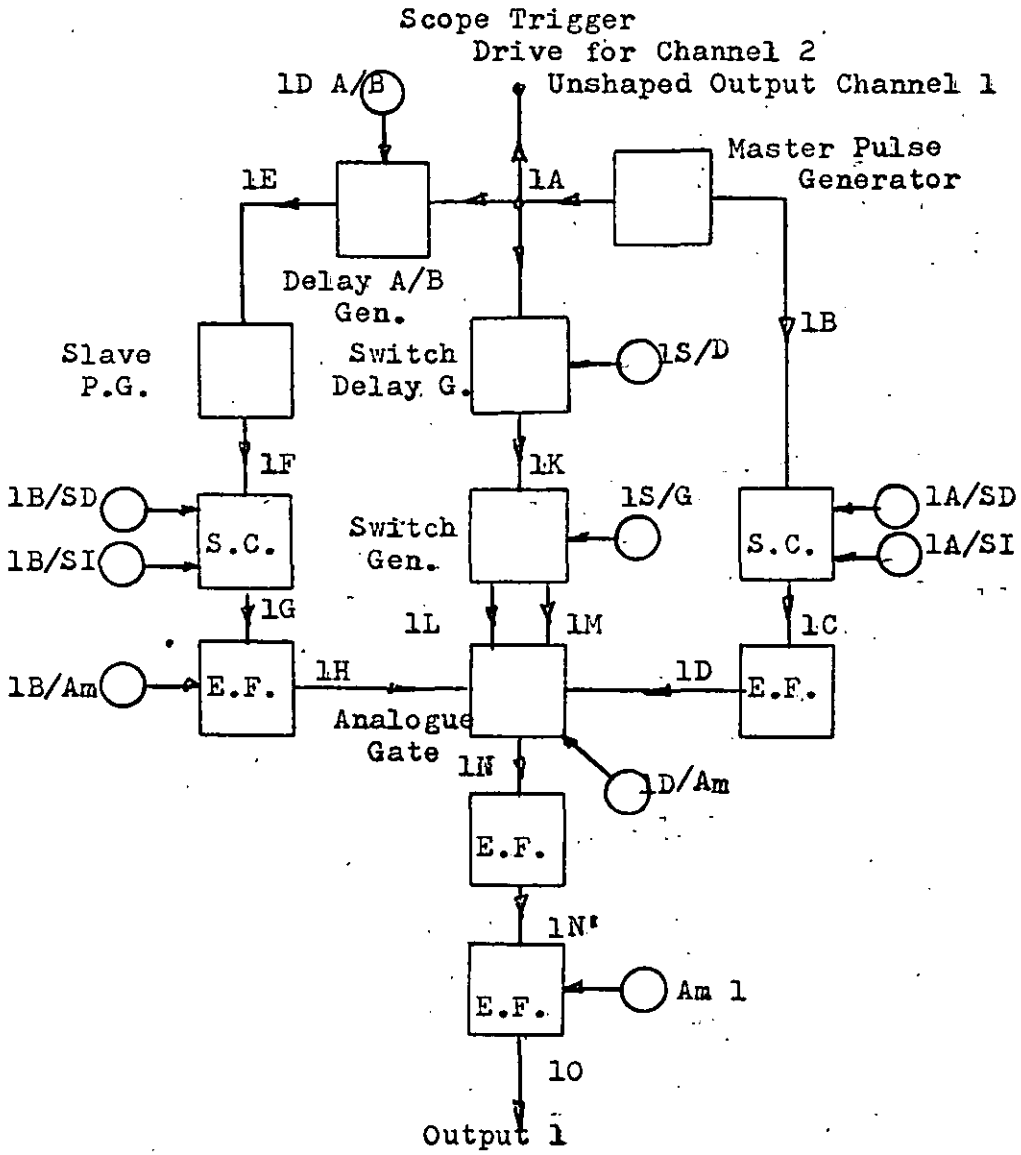


Fig. 3.4.

Pulse Wave Simulator Channel 1 Block Diagram

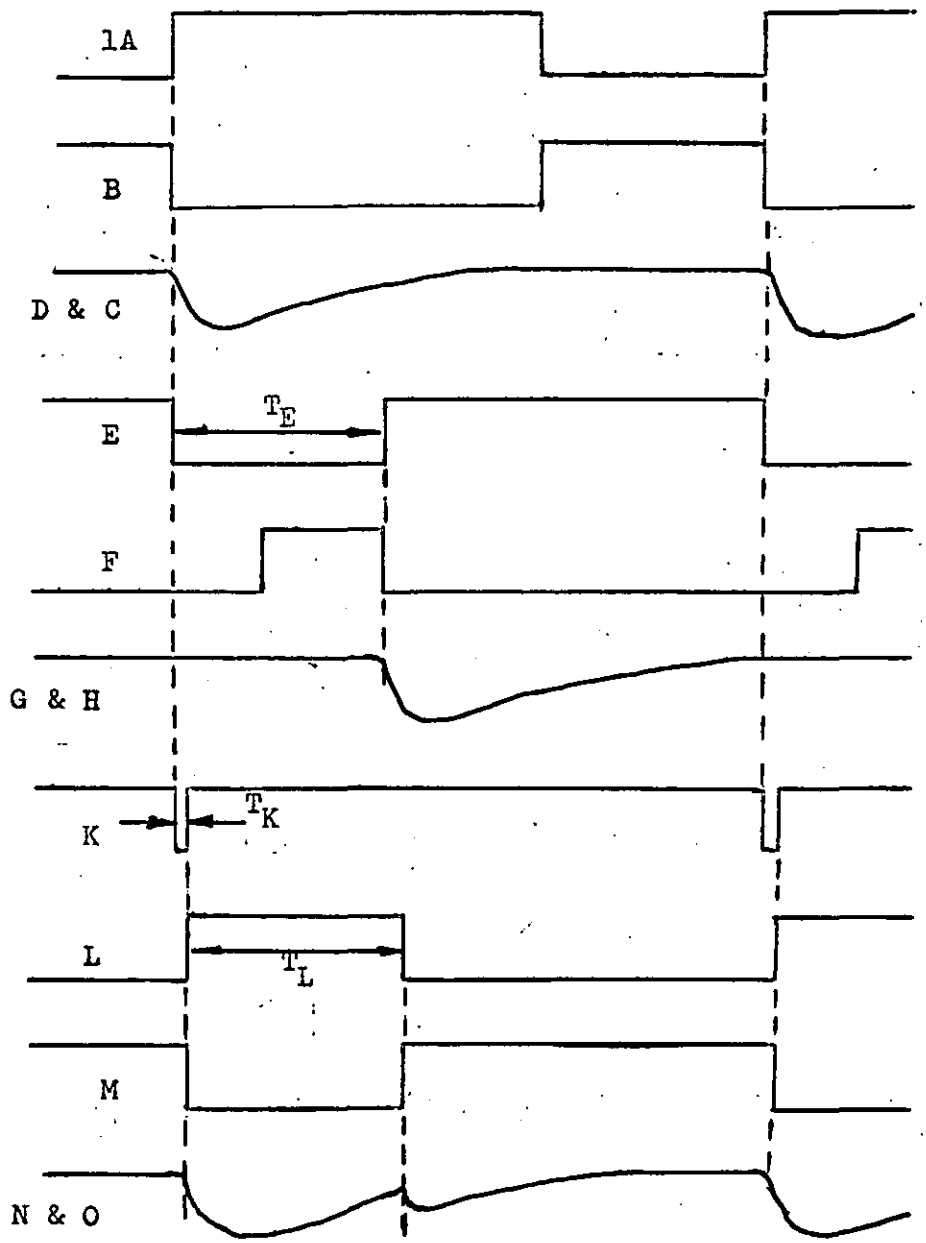


Fig. 3.6

Simulator Waveforms for Channels 1 and 2

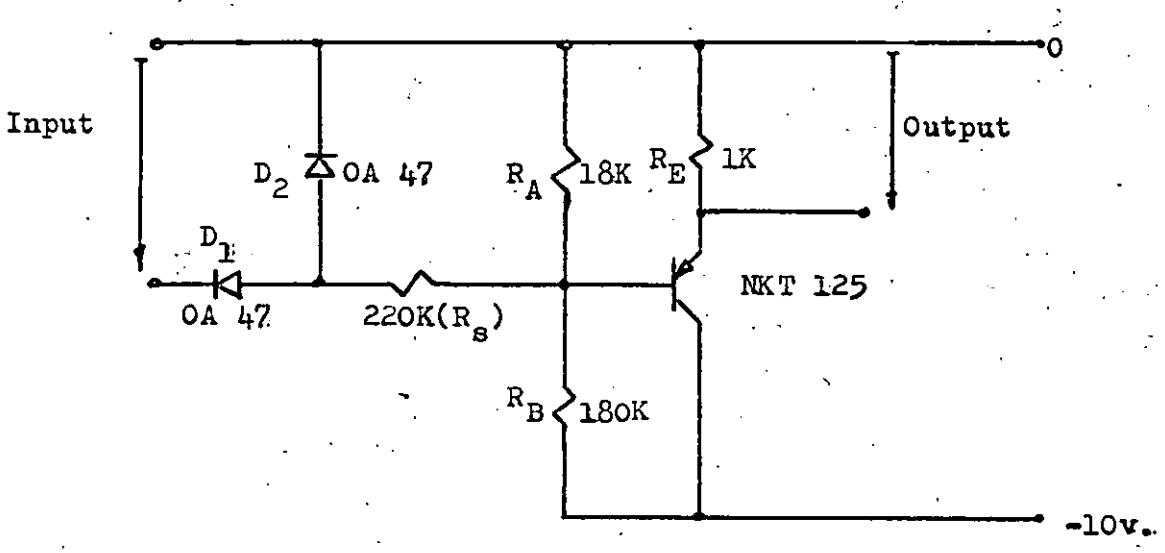


Fig. 3.7.

Attenuating Emitter Follower Circuit.

The simulator is timed by a master astable pulse generator, which is set to standard heart rate, and provides the step from which part A of the waveform is generated. In addition it triggers a delay generator from which a slave pulse generator is driven. This slave generator provides the signal from which part B of the waveform is produced. Note that the delay (A/B) generator cannot be used to produce part B of the waveform directly, since it has been found desirable to 'overlap' the waveform at both ends. The output from the master and slave generators are then fed into shaping circuits as discussed previously. Reference should be made to fig. 3.6, where the waveforms for the complete system, as shown in fig. 3.4, are given. The master generator output is given in its normal and inverted forms, as waveform A and B, and the shaped signal is produced from the B waveform and is shown as waveform C. The delay A/B generator produces waveform E, and from this the slave generator is triggered. The shaped output used to generate part B, of the waveform is shown on waveform G.

To make these shaped waveforms compatible with the input requirements of the Analogue Gate, requires that they are attenuated and biased to approximately -1volt. This is achieved by using the emitter follower circuit as shown in fig. 3.7, the diodes D_1 and D_2 accept only the negative going signal from the shaping circuit and clamp the quiescent dc level to earth. The signal is attenuated by the divider formed by the series resistor and the input impedance of the emitter follower stage.

The dc conditions are set up by the bias applied to the emitter follower.

For the B part of the waveform, a variable amplitude is obtained by replacing the emitterresistor by a potentiometer, and taking the output from the wiper.

The output is taken from the Analogue Gate by using a high input impedance emitter follower, to avoid loading the gate. This is then fed into a second emitter follower to give a low output impedance. A variableamplitude output is obtained as above. The first emitter follower has a large capacitor across the emitter resistor, which acts as a low pass filter and prevents any discontinuities in the waveform appearing on the output.

The switching signals for the analogue gate are shown as waveforms L and M in fig. 3.6. These are derived from the two sides of a pulse generator which is driven by the master generator via a delay stage as shown. To provide a low output impedance this generator has 680Ω collector loads.

This gives the basic single channel system, the location of the various variable controls are shown on the system diagram. The period T_E is a variable, controlled by the delay A/B generator. The shaping circuits have both their resistive components variable to enable the signal shape to be controlled (See Appendix D). The periods T_k and T_L are both variable so that any desired proportion of A to B can be selected.

The overall amplitude, and the amplitude of the B part of

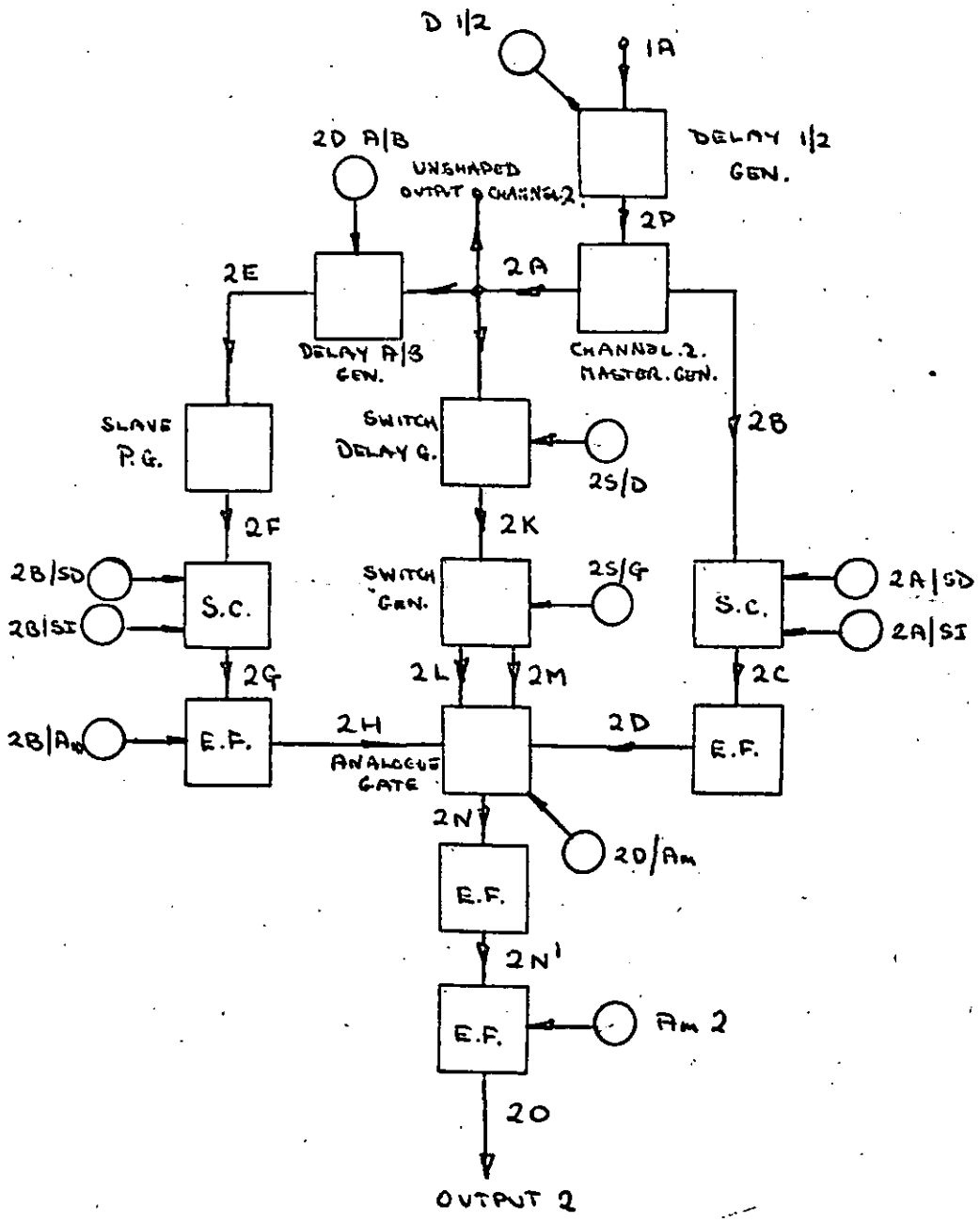


Fig. 3.5.

Pulse Wave Simulator Channel 2 Block Diagram

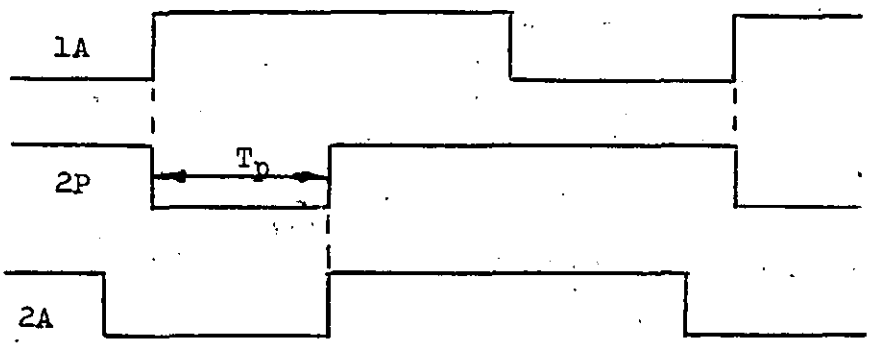


Fig. 3.8.

Simulator Waveforms for Channel Delay Production

the waveform are variable, and to facilitate balancing of the two parts of the waveform the Analogue gate incorporates a differential level shifting control.

For a second channel, which is delayed from the first by a variable quantity, it is only necessary to duplicate the original system and replace the astable master generator by a monostable master generator. This generator is then driven from the master generator via a variable delay stage. Thus a continuously variable delay is achieved, and the two output waveforms can be made similar, or dissimilar as required, by using the variable controls.

The system diagram for the second channel is shown in fig. 3.5, and in general the related waveforms are similar to those for Channel 1, those waveforms which are different, are given in fig. 3.8.

The Simulator provides the facilities which are listed below:-

(1) Both simulated outputs are available from a low impedance source and short circuit protection is provided.

(2) Waveform 1A is provided as a 'scope' trigger signal.

(3) Waveforms 1A and 2A are provided as 'unshaped' outputs, which can be used to drive the simulator via the inputs provided after the exponential amplifiers, for calibration purposes. Also these waveforms can be used as 'start' and 'stop' signals to a counter to enable the delay to be measured accurately for

standardisation.

The simulator construction incorporates its own power supplies and uses plug-in boards. The amplitude controls for both channels and the delay control are mounted on the front panel. All the other variable controls use skeleton potentiometers and are mounted on the rear edge of the plug-in boards. Full circuit diagrams, photographs and wiring details of the Simulator are given in Appendix B.

Copies of the waveforms produced by the simulator can be found in Section 6.

This simulator has been constructed using pnp transistors operatingbetween earth and -10 volts, and thus a negative going output is provided. The exponential amplifiers are however designed to operate from a positive going signal. Thus to invert the output a special phase correcting amplifier has been designed and it is described in Section 4, with the design of the various other components in this system.

SECTION 4

Design Considerations and Procedures

Introduction

In the following sub-sections of this section, the design of the various circuits discussed in the thesis, is given.

In all cases the circuits have been designed to operate from either + or - 10 volt rails, or both. The power supplies are described in sub-section 11.

In certain cases; for example gates, pulse generators etc, a pnp circuit is used in one instance, and an npn circuit is used in another. The design here considers only the npn case, since the pnp circuit can be obtained by inverting the polarity of any diodes in the circuit, and replacing the +10 volt rail by the -10, and vice versa.

Section 4.1

Operational Amplifier Design

For a dc amplifier to perform successfully as an operational device its performance must conform to the specification shown below:-

1. Very large internal voltage gain.
2. High input impedance.
3. Low output impedance.
4. Both input and output should have quiescent dc levels at earth potential.

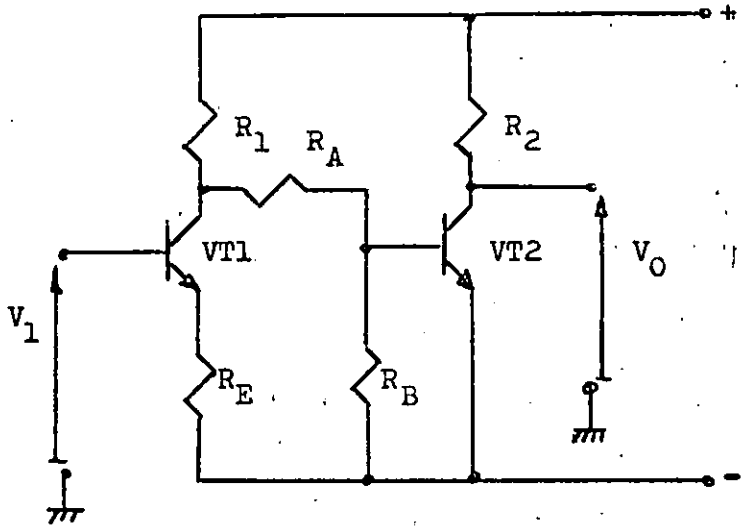


Fig.4.1.1

Dc Amplifier.

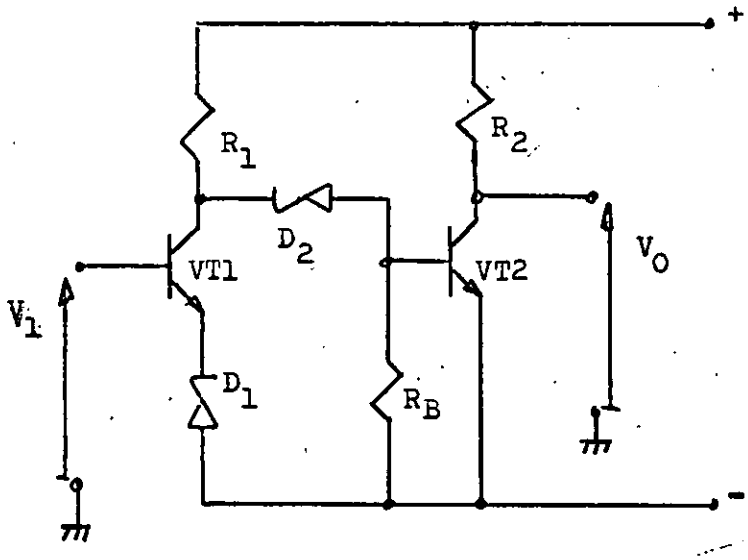


Fig. 4.1.2

DC Amplifier.

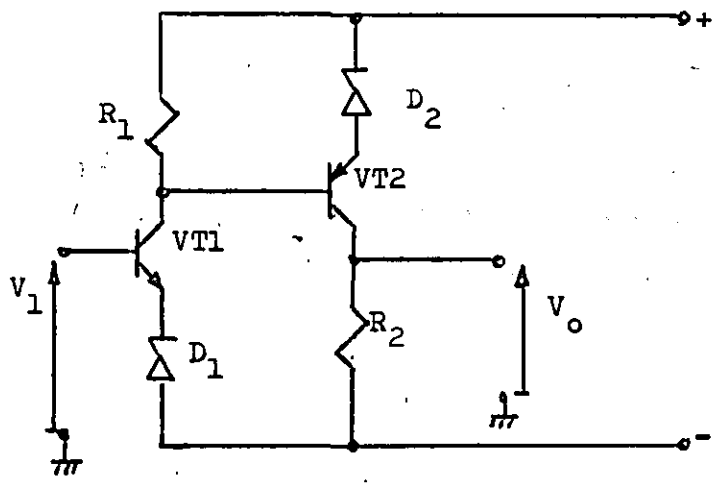


Fig. 4.1.3

DC Amplifier.

5. The dc operating points and gain should be stable with temperature.
6. The amplifier should have a bandwidth suitable to the application intended.

Experience shows that the above requirements are conflicting in nature, and that the final design must, as always, be a compromise.

The temperature sensitivity can be reduced to a minimum by using all silicon semiconductors. Obviously the circuit will require more than one stage of amplification and some form of dc coupling, between the stages, will be required.

The circuit given in fig. 4.1.1. gives a possible form of coupling, that will enable the zero input/output condition to be satisfied, but the undecoupled emitter resistor, and the resistive divider chain limit the gain. These components can be replaced by zener diodes as in fig. 4.1.2. which will give the required level shifting, without the degeneration, given by their resistive counterparts. Another modification is to replace the second transistor by its complement, that is pnp for npn, as shown in fig. 4.1.3., this eliminates the resistor R_B.

However the circuit now relies on the dc shift produced by the zener diodes for its operation. This voltage is temperature sensitive, and leads to poor temperature stability,

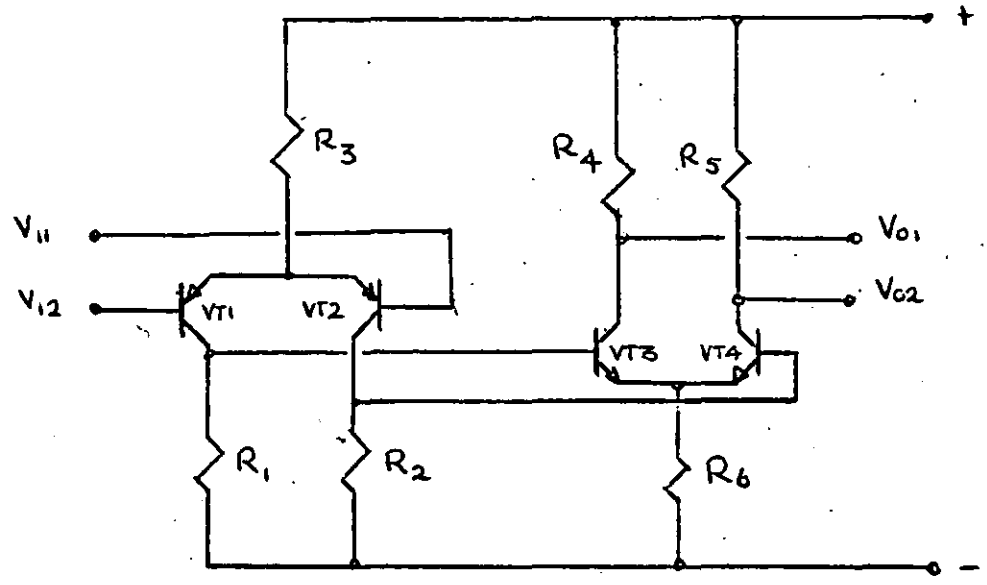


Fig. 4.1.4

DC Amplifier.

in a circuit where discrete circuit components are used. This would not necessarily be the case in an integrated circuit (57).

Thus an alternative approach must be adopted and there are two basic methods available. These being a chopper stabilised amplifier and a differential amplifier.

In the chopper stabilised amplifier (47), (58) the input signal is modulated, by using a chopping device, and the chopped signal is then amplified in an ac coupled amplifier. The amplified carrier signal is then demodulated to give the output. In this way an extremely large gain can be achieved with excellent temperature stability.

However in this work it was decided to use a differential amplifier (55), (56) since the gain with two differential stages can easily be made in excess of 1,000, which is considered to be large enough for this application.

The basic circuit diagram of a two stage differential amplifier is shown in fig. 4.1.4., and to achieve the zero input/zero output condition a pnp stage is followed directly by an npn stage, as in the manner of the single ended amplifier in fig. 4.1.3. The input is applied across the bases, and in true differential applications, the output is taken from the collectors of VT3 and VT4.

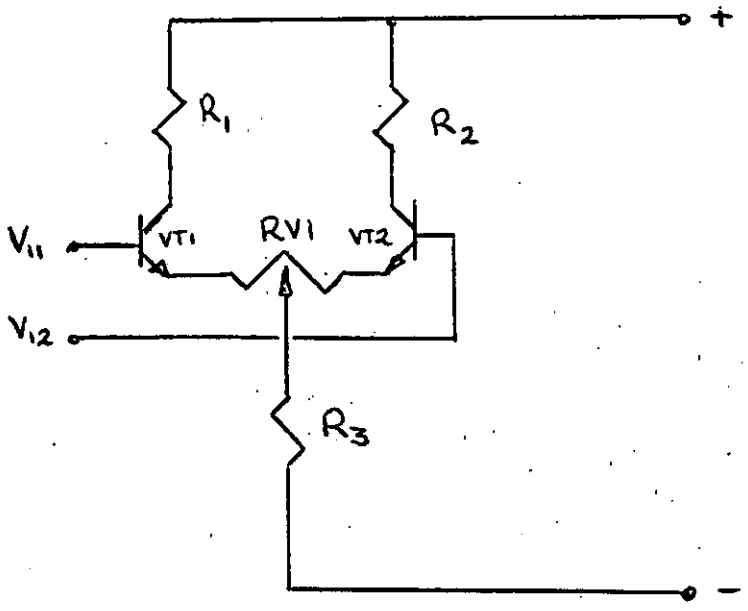


Fig. 4.1.5.

DC Amplifier.

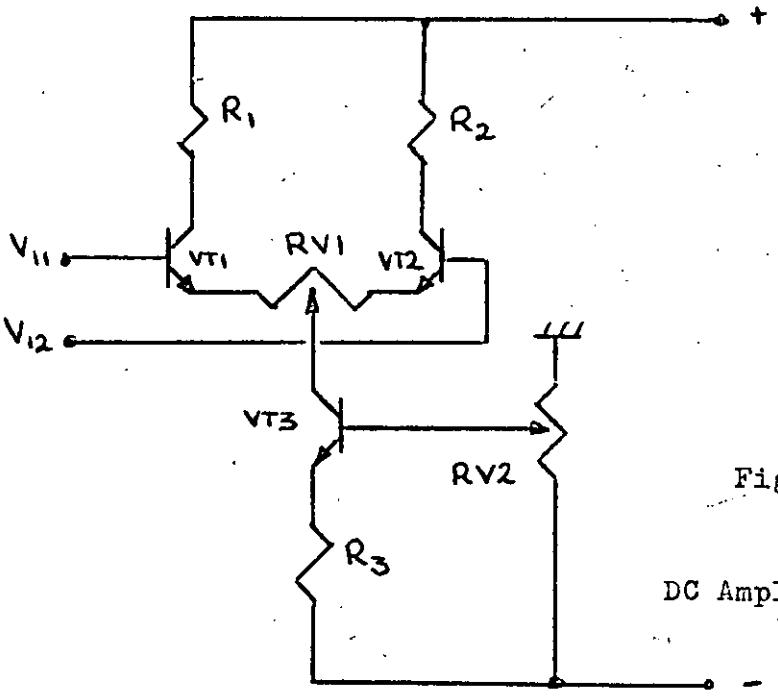


Fig. 4.1.6.

DC Amplifier.

If the differential pair are similar, both electrically and thermally, drift due to temperature variation will be equal on both sides and will not affect the relative states of the transistors. Also the drift produced by the pnp pair will tend to be compensated for by the drift of the npn pair.

In practice the transistors can be made similar thermally by clamping them in the same heat sink, but they must be matched, or compensated, to achieve similar electrical operation. The compensation normally takes the form of a small potentiometer inserted in series with the transistor emitters, as shown in fig. 4.1.5. This enables the two transistors to be balanced, provided that they are matched for gain. The resistance inserted also produces a small degree of feedback, which both stabilises the gain and increases the input impedance.

It can be shown to be desirable, (52) to make the tail resistor as large as possible, since this will then approximate to a constant current source, which is the optimum. As a rule of thumb, it can be said, that for stability, R_3 should be greater than, or equal to R_1 (or R_2). This is not always possible, due to the limitations set by the voltage rails, and in these cases, the tail resistor can be replaced by a transistor acting as a constant current source, as shown in fig. 4.1.6. For constant current operation the transistor must be biased into its linear region and supplied with a constant base current. This will produce a constant collector current set by the gain of the transistor. The biasing is produced by R_3 and potentiometer

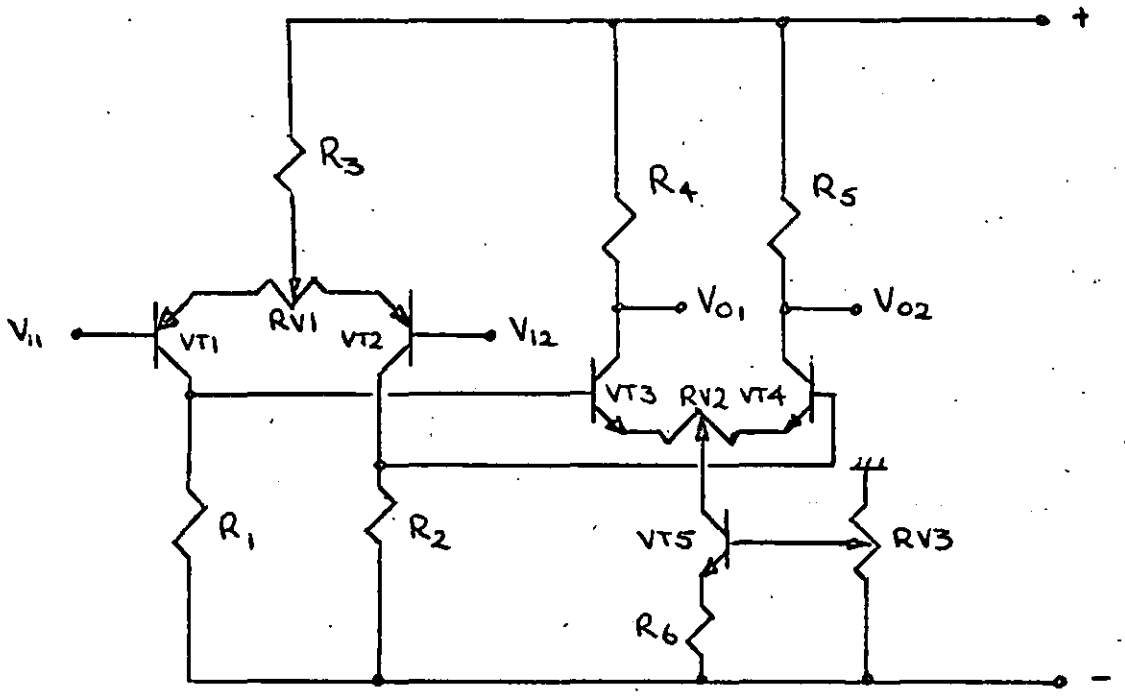


Fig. 4.1.7

DC Amplifier

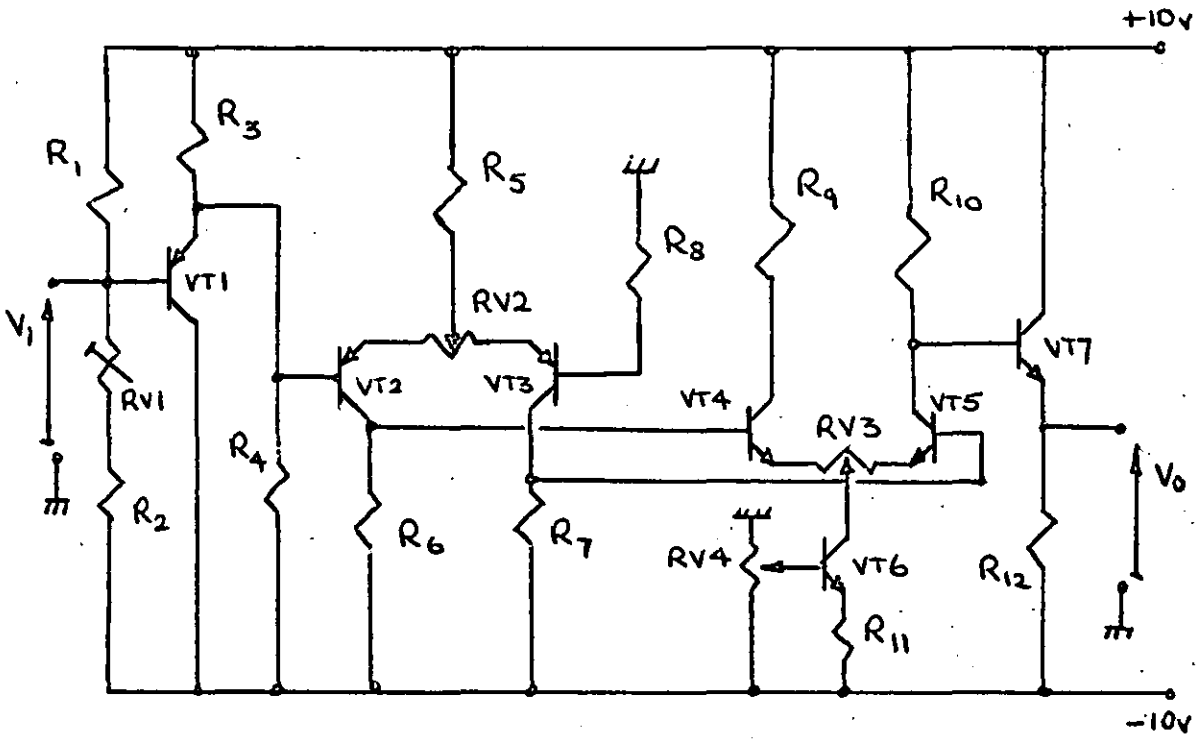


Fig. 4.1.8

DC Amplifier Final Circuit.

R_1	2·2M	R_9	10K	VT1	OC202
R_2	560K	R_{10}	10K	VT2	V405
R_3	22K	R_{11}	680	VT3	V405
R_4	560K	R_{12}	1K	VT4	BSY95A
R_5	10K	RV1	1M	VT5	BSY95A
R_6	10K	RV2	1K	VT6	BSY95A
R_7	10K	RV3	500	VT7	BSY95A
R_8	27K	RV4	10K		

Fig. 4.1.9

Component values in above fig.

RV_2, as shown.

Variation of the setting of RV2 will alter the base and collector currents, and can thus be used to set the dc operating conditions for VT1 and VT2.

A two stage differential amplifier with the refinements considered is shown in fig. 4.1.7., but as yet it does not conform to the specifications required for an operational device. Since the operational amplifier is basically single-ended, true differential operation cannot be applied. One of the input bases must be grounded and this is done via a suitable resistor. This gives a single ended input, with respect to earth, and an input impedance of approximately the grounding resistor. The amplifier is required to be inverting and thus this determines the output that is taken.

High input and low output impedances are provided by emitter followers at both ends of the basic circuit. The input circuit has variable biasing to enable the zero input condition to be set. The zero output is set, as described earlier, by the variable biasing in the constant current driver circuit.

The final circuit for the operational amplifier is shown in fig. 4.1.8., and a list of component values is given in fig. 4.1.9. The amplifier was designed to have a standing dc current in VT2 and VT3 of $\frac{1}{2}$ mA, with a collector-emitter

voltage of 6 volts. The standing current in VT4 and VT5 is 1 mA with a collector-emitter voltage of 8 volts.

The measured performance of the amplifier is given below:-

Voltage Gain > 1,000

Input Impedance > 600 kΩ

Output Impedance < 500Ω

Bandwidth > 400 kc/sec

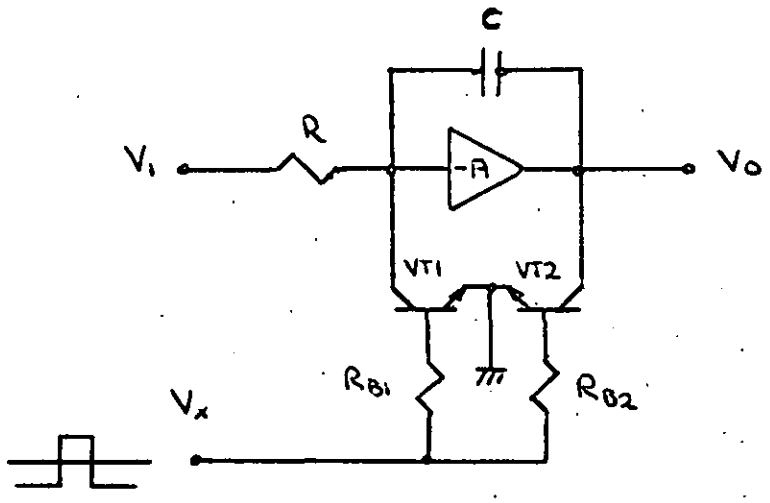


Fig. 4.2.1

Integrator Resetting Gate

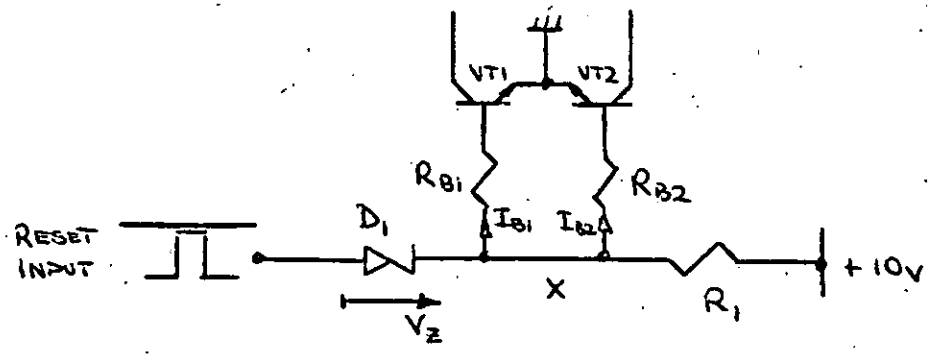


Fig. 4.2.2

Gate Drive for above fig.

Section 4.2

Integrator Resetting Gate Design

In the previous section a dc amplifier suitable for operational applications has been developed. However, for the applications intended, this amplifier will be operating as an integrator, which requires resetting to its initial conditions electrically. The method usually applied on analogue computers is to use electromechanical relays for resetting, but the analogue division system operates the integrator at a high repetition frequency, and conventional relays could not operate fast enough. A reed-relay would be a possibility, but another solution which appears to give satisfactory results has been used.

The initial condition required by both integrators is zero, that is a fully discharged capacitor. This simplifies the problem in that no initial charge has to be set on the capacitor. Consider the configuration as shown in fig. 4.2.1, with the transistors biased off the arrangement is a simple integrator, since the transistors will appear as a large, ideally infinite, impedance across the capacitor. If silicon transistors are used the leakage current will be very small.

When the transistors are turned on, the capacitor will discharge since both ends are tied to earth via a low impedance.

The time taken to discharge the capacitor is determined by the base current provided. Consider the circuit in fig. 4.2.2., this is the method used to provide the switching signal V_x,

since the integrator is an inverting device a positive output indicates a negative input and thus the derived reset pulse appears as a positive going pulse between -10 and earth, and thus requires level shifting which is achieved by the Zener diode.

If the source impedance of this pulse is R_S, then as far as the transistors are concerned the signal appears to be a pulse of approximate amplitude V_Z from a source impedance of R_1 and R_s in parallel.

Thus the total base current $2I_B$ will be given approximately by:-

$$2I_B = (V_Z - V_{BE}) / R_1 \| R_s + R_B/2$$

If this current flows for a time, t, then the charge removed from the capacitor by the resultant collector current will be approximately

$$Q = I_B h_{FE} t$$

But the initial charge on the capacitor is given by $Q = CV_C$

Thus equating these two figures gives:-

$$t = \frac{C V_c}{I_B h_{FE}}$$

$$\text{or } t = \frac{2C V_c \left[R_s \| R_1 + R_B/2\right]}{(V_Z - V_{BE}) h_{FE}}$$

A knowledge of the maximum voltage to which the capacitor will charge, its value, and the other circuit parameters can then be used to predict the discharge time for a given base resistor.

However the value taken for h_{FE} must be investigated, since at the end of this discharge this must fall from its normal value due to the transistor characteristics.

In practice the values have been found empirically, but the results fit reasonably with the above theory.

For example for the analogue divider system, typical values are:-

$C = 0.01$ mFd

$(R_s \| R_1 + R_B/2) \leq 3K\Omega$

$V_z - V_{BE} \geq 5$ volts

$V_c \leq 8$ volts

Thus assuming an h_{FE} of 50 gives a discharge time of approximately 2 μsec, which is of the order of the discharge times obtained experimentally.

The component values in the actual circuits can be found by reference to the full circuit diagrams for the computer, given in Appendix A.

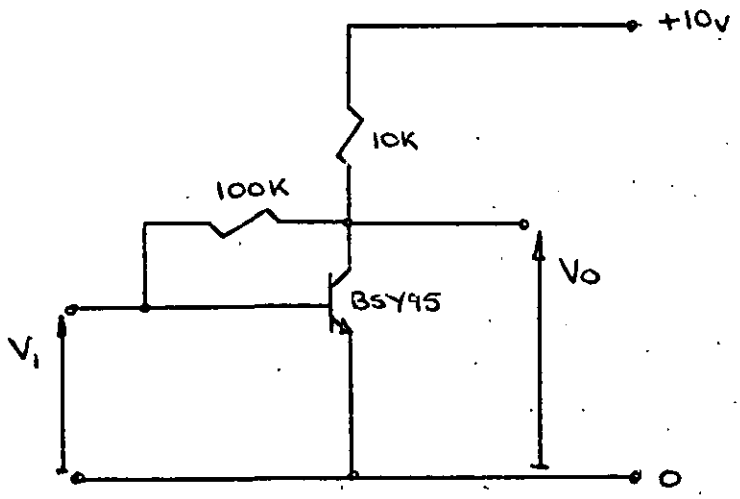


Fig. 4.3.1

Simple DC Amplifier

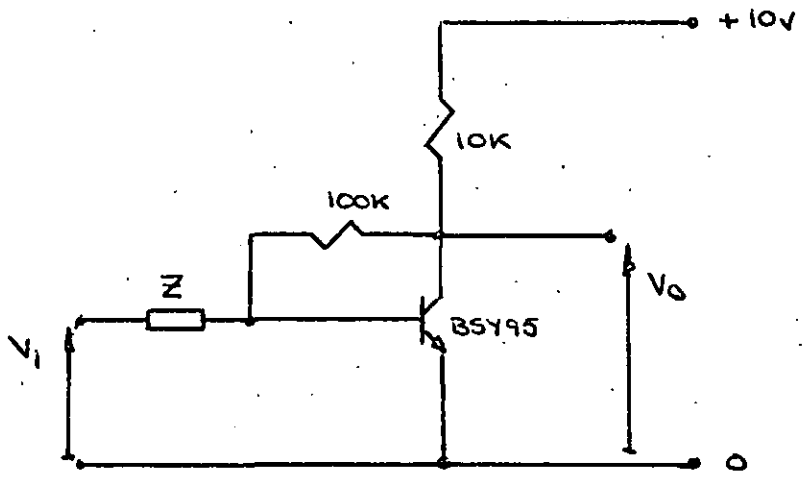


Fig. 4.3.2

Simple Operational Amplifier

Section 4.3

Simple Operational Amplifier Design

In certain applications it is necessary to perform an analogue function, to a minimal accuracy, over a limited range of input conditions. The use of the operational amplifier as described in Section 4.1, would be expensive and unnecessary. In this case a simple one transistor inverting amplifier has been designed to perform the function.

The basic circuit is shown in Fig. 4.3.1 and is extremely simple in design. The base resistor R_B, provides the dc biasing and also the required feedback. The nominal values of R_B and R_C, as shown give a typical amplifier performance as shown below:-

Voltage Gain	150
Input Impedance	1KΩ
Output Impedance	10KΩ
Quiescent dc output	+ 3 volts
Quiescent dc input	+0.5 volts

When patched as an operational amplifier as shown in fig 4.3.2, the theoretical tranfer function becomes:-

$$\frac{V_o}{V_1}(p) = \frac{R_B}{Z(p)}$$

However if a simple voltage amplifier is required, the gain is set by making $Z(p)$ purely resistive or zero.

Section 4.3.1

The Exponential Amplifier

In the exponential amplifier, the impedance Z (p) is that of a forward biased silicon junction diode. The diode has an exponential characteristic which is given, theoretically by:-

$$I = I_o(\exp(qV/nkT)-1) \quad \text{(See Appendix C)}$$

In practice silicon diodes obey this law over a limited operating range. However, if a small area junction device, such as the Mullard SX630, is used then the law is obeyed over an increased operating range.

The dc resistance of the device is given by:-

$$R_D = V/I = V \; I_o(\exp(qV/nkT)-1)$$

Hence the theoretical transfer function for the exponential amplifier becomes:-

$$V_o/V_1 = R_B/R_D = R_B I_o(\exp(qV_1/nkT)-1) \; V_1$$

Hence $V_o = R_B I_o(\exp(qV_1/nkT)-1)$ or $V_o = A(\exp(BV_1)-1)$

Where $A = R_B I_o$ and $B = q/nkT$

The diode manufacturer's quote typical figures for I_o and

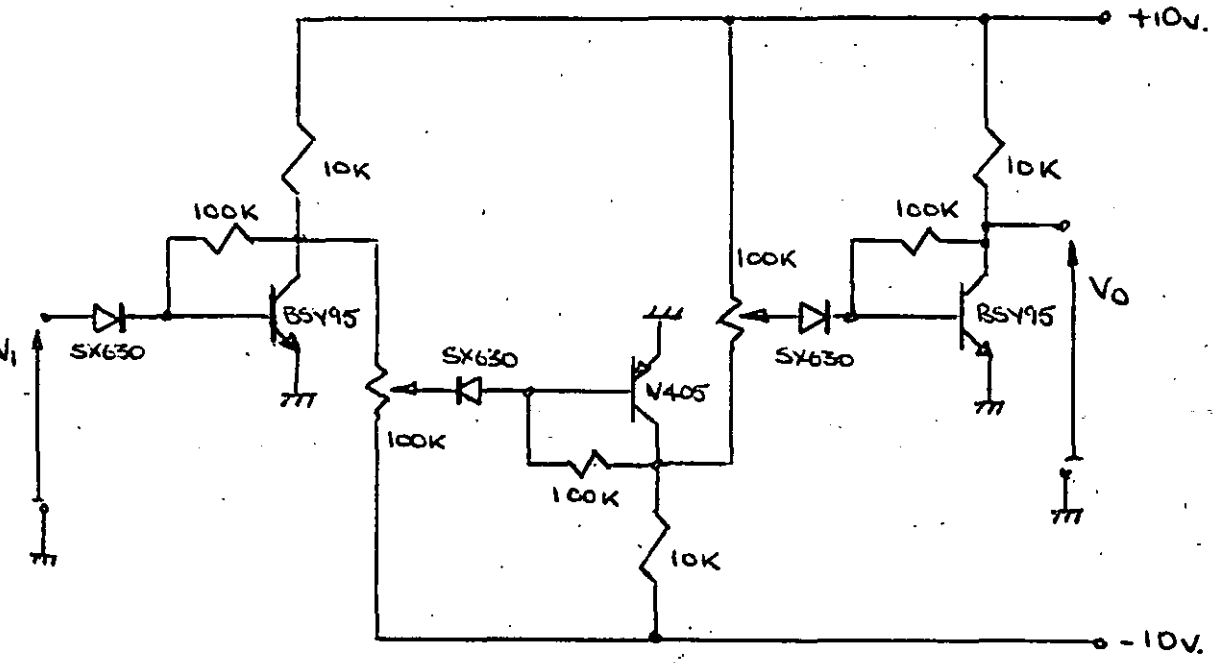


Fig. 4.3.3

3 Stage Exponential Amplifier

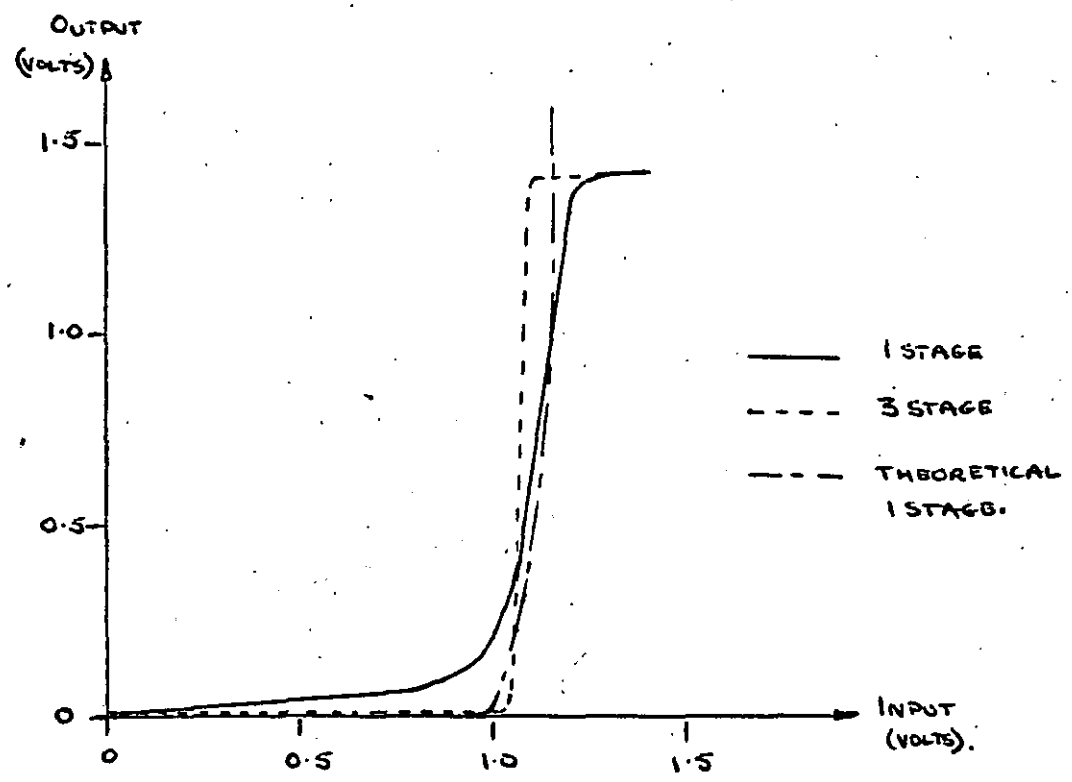


Fig. 4,3.4

Exponential Amplifier Characteristics

$\frac{q}{nkT}$ as 10^{-10} and 23 respectively. Also that the device will obey the theoretical law over an input voltage range of 0.2 to 0.7 volts. Thus this automatically limits the range over which the amplifier can function.

With V_1 = 0.2 volts, the quantity e^{BV_1} becomes approximately 100. Thus to accuracy better than 1% the -1 in the original expression can be ignored, thus giving a transfer function of:-

$$V_O = A\ e^{BV_1}$$

Where $A = 10^{-5}$ and B = 23

In practice it has been found that three stages of exponential amplification are required to give the desired accuracy.

To achieve this two npn stages are interposed by a pnp stage. The coupling between stages is via a 100K potentiometer which serves to attenuate the signal to the required amplitude and also provide the required dc level on the output. The complete circuit of the three stage amplifier is shown in fig 4.3.3.

Typical input/output characteristics for a single stage and a 3 stage amplifier are shown in fig. 4.3.4. In addition the theoretical transfer characteristic for the single stage is included. The curves have been drawn with a static dc output of zero, only for the purposes of comparison.

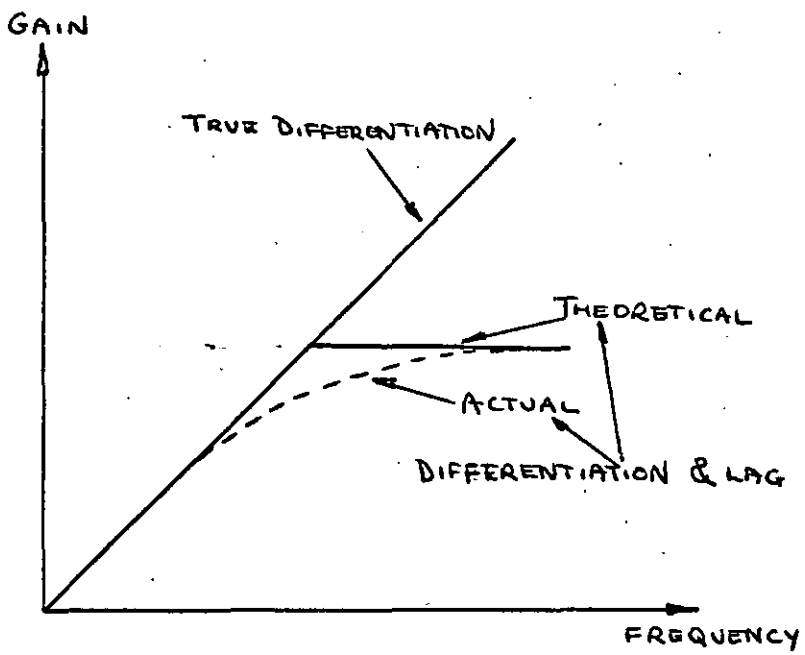


Fig. 4.3.5

Differentiator Characteristics

Section 4.3.2

The Differentiator

If the input impedance $Z(p)$ is a capacitor, of value C, then the function the amplifier performs is that of differentiation. The theoretical transfer function will become:-

$$\frac{V_o(p)}{V_1} = \frac{R_B}{1/pC} = pC\,R_B$$

where p is the Laplacian operator. Hence differentiation with a gain set to $C\,R_B$.

However when a typical analogue signal is differentiated in this manner it invariably becomes 'noisy' and the circuit tends to be unstable. This is because there is a linear relationship between gain and frequency in a differentiator, as shown in fig 4.3.5. Thus any high frequency noise present will be amplified many times and this has an adverse effect on the signal to noise ratio for the signal.

However if the function is modified, by the inclusion of a lag in the system, as shown in fig. 4.3.5, the gain above the breakpoint frequency is constant, and then any high frequency noise present will be amplified, but not to the same degree as in the pure differentiator.

The signal to noise ratio of the signal is affected but not as badly as previously. The lag can easily be introduced by placing a capacitor C_B in parallel with the resistor R_B, as

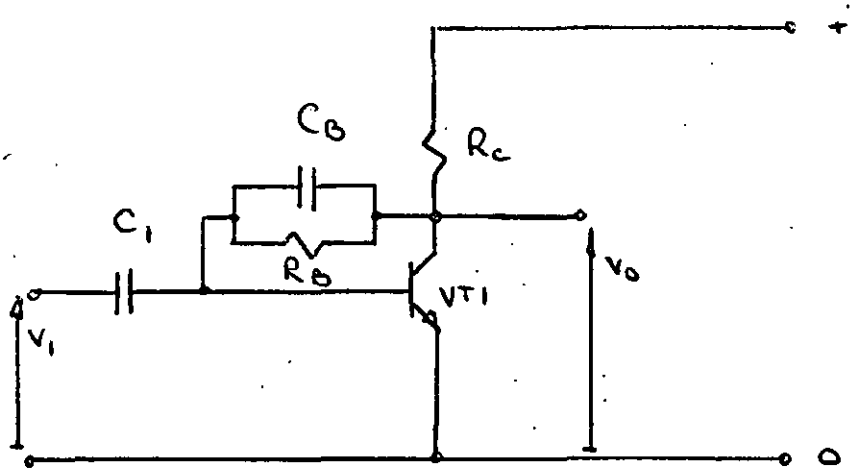


Fig. 4.3.6

Differentiator & Lag Circuit Diagram

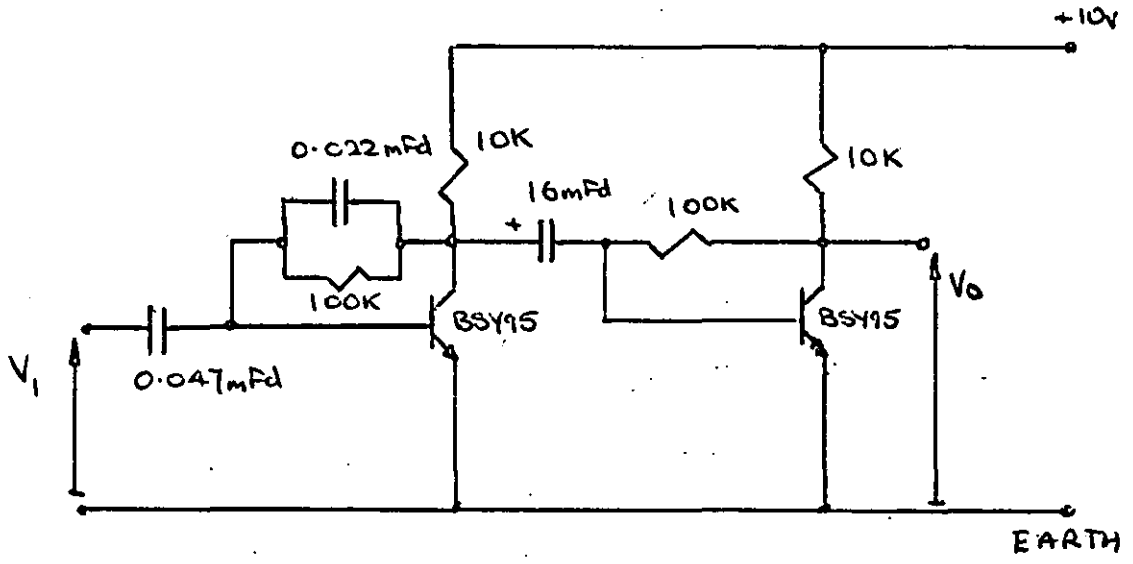


Fig. 4.3.7

Complete Circuit for Differentiator

shown in fig. 4.3.6. This arrangement has a theoretical transfer function of:-

$$V_o/V_1(\rho) = \rho CR_B/(1 + \rho C_B R_B).$$

The breakpoint frequency, f_1, is given by

$$f_1 = 1/2\pi C_B R_B$$

In the actual system it has been found that the 'high frequency' noise is at 100 c/s, and is thus from the power supplies. To remove this adequately a suitable cut-off frequency has been found to be 70 c/s, which, as a preferred value, makes $C_B = 0.022$ mFd.

For efficient differentiation a maximum value of input capacitor, C, was found to be 0.047 mFd. This, however, did not give sufficient gain for the output signal to drive the trigger circuit directly, and thus a voltage amplifier was added. This amplifier is of the same design as the basic operational amplifier, and is ac coupled to the output of the differentiation stage.

The final circuit of the differentiator stage is shown in fig. 4.3.7.

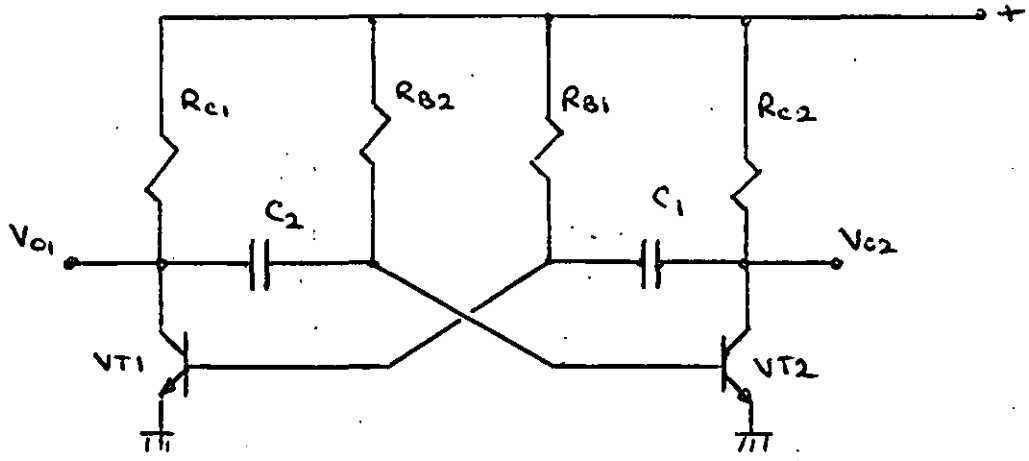


Fig. 4.4.1

Basic Astable Pulse Generator

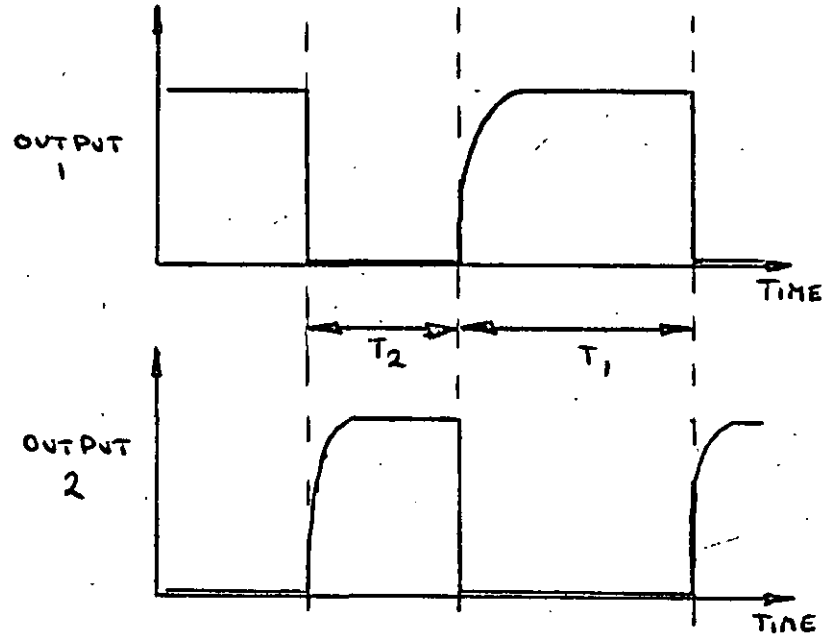


Fig. 4.4.2

Outputs from above Circuit

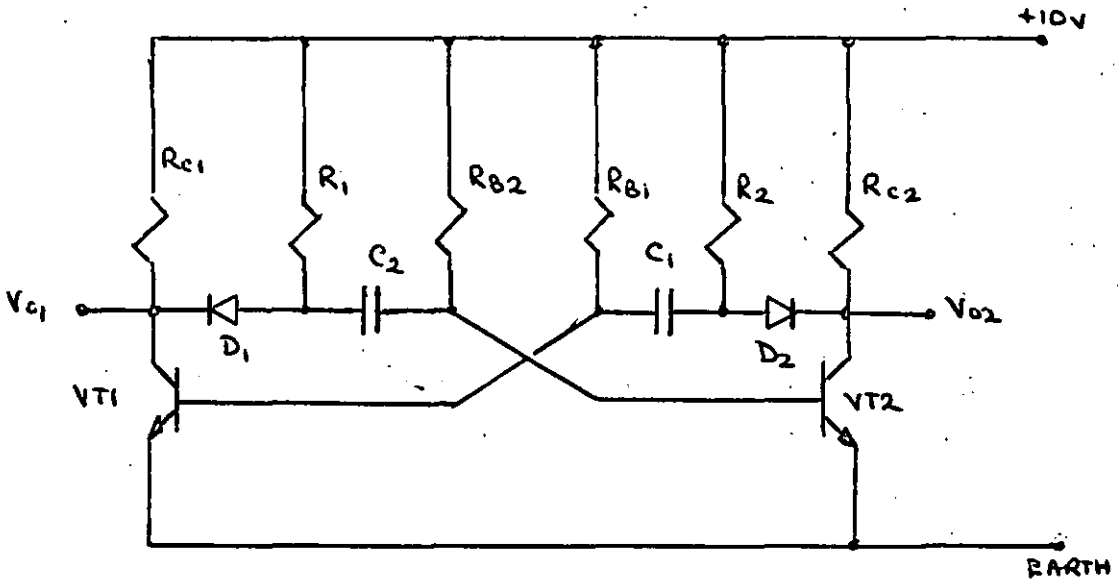


Fig. 4.4.3

Modified Astable Pulse Generator

Section 4.4

Astable and Monostable Pulse Generator Design

In both the computer and the simulator astable and monostable pulse generators are used. The circuitry is conventional, and of the collector/base coupled configuration, with RC timing circuits. The basic astable circuit is shown in fig. 4.4.1, either output is available and their polarities are shown in fig. 4.4.2.

The timing intervals T_1 and T_2 are given by $T_1 \simeq 0.7\ C_1 R_{B1}$ and $T_2 \simeq 0.7\ C_2 R_{B2}$. In a circuit of this type the capacitors discharge through the base resistors, and in doing so time the generator. They recharge through the collector resistors, and thus if the circuit is designed for low-frequency operation with large capacitors, as with the simulator, the edges of the output waveform are distinctly rounded in nature. To prevent this occurrence a separate charging path for the capacitor is provided, as shown in fig. 4.4.3. This resistor is coupled to the collector via a diode. Normally the diode is forward biased and the circuit is equivalent to that in fig. 4.4.1. However the difficulty is normally experienced when the transistor in question switches off. In this case the collector voltage rises quickly to the rail, and reverse biases the diode, thus isolating the collector from the timing capacitor. The capacitor then charges through the resistor provided. When the rail voltage is reached the diode is again

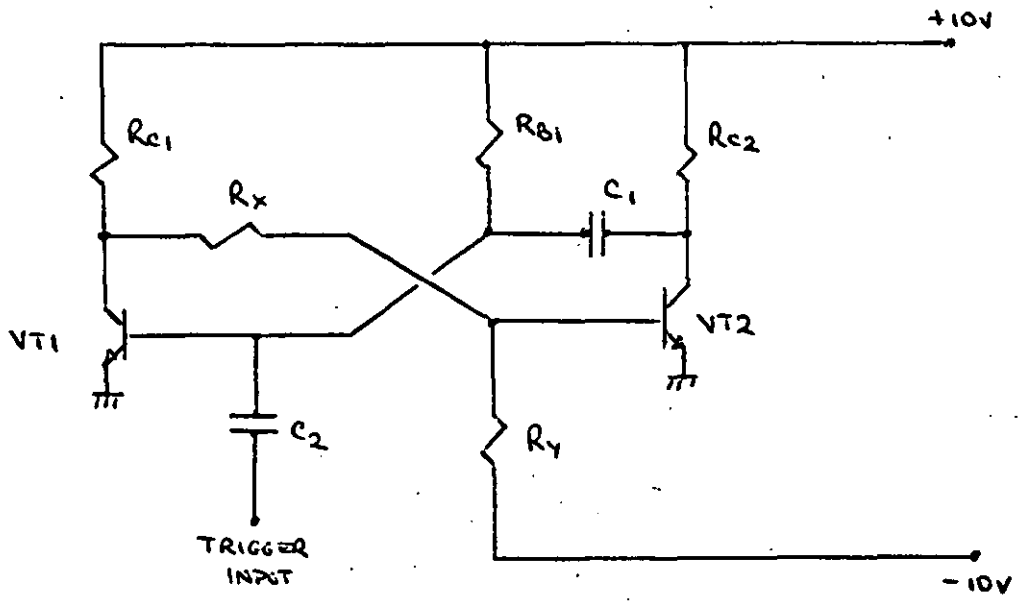


Fig. 4.4.4

Basic Monostable Pulse Generator

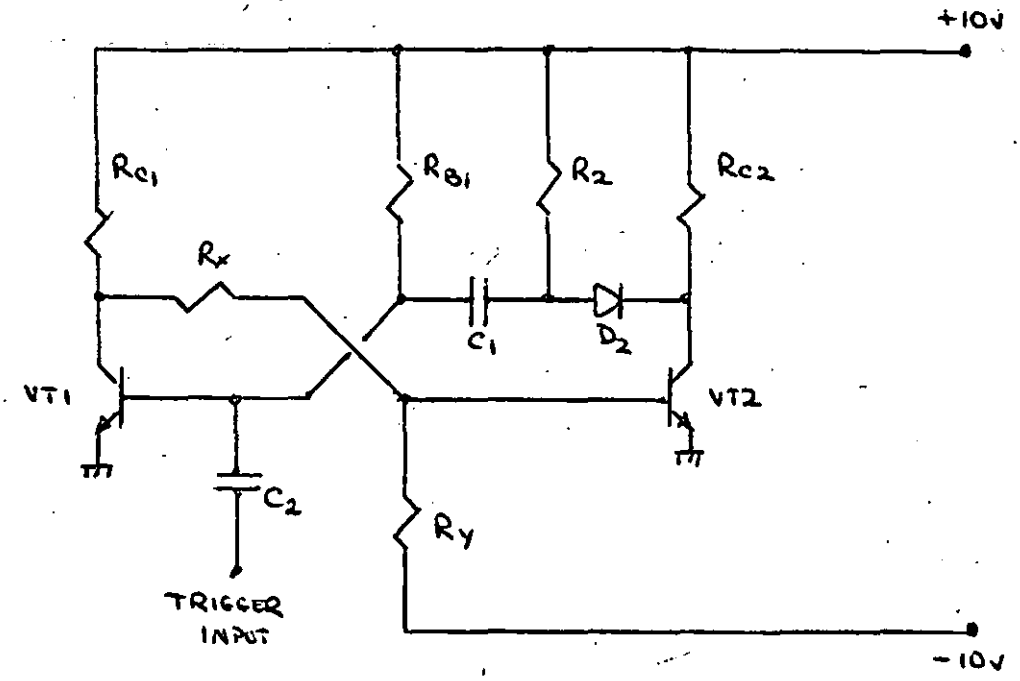


Fig. 4.4.5

Modified Monostable Pulse Generator

forward biased. Thus the capacitive loading of the collector is reduced to that of the stray capacities and the reverse capacity of the diode.

The time constant C_1R_2 must permit the capacitor C_1 to fully recharge in the time period T_2. It can be considered fully charged after a time period 3T, thus

$$3\ C_1R_2 \geq 0.7\ C_2R_{B2}$$

and $$3\ C_2R_1 \geq 0.7\ C_1R_{B1}$$

In the monostable circuit, one of the timing capacitors is replaced by a resistor chain as shown in fig. 4.4.4. This gives a stable state in which VT_2 is off and VT_1 is on and saturated. To produce an output pulse the circuit is triggered via a capacitor on the base of VT_1, with a negative going edge. This switches VT_1 off, and through the direct coupling to VT_2, switches VT_2 on and drives it into saturation. This condition is maintained while capacitor C_1 discharges and the circuit returns to its initial state after a time period, $T_1 \simeq 0.7\ C_1R_{B1}$

To ensure the trigger signal, is absent after this time interval, the input time constant C_2R_{B1}, is made considerably shorter than the required pulse length.

In general, $C_2 \simeq C_1/10$, is taken as an empirical law, but C_2 is not made larger than 0.1 mFd.

The circuit modification sharpen the edge of the waveform as shown in fig. 4.4.3 for the astable circuit, is also used on the monostable circuit, as shown in fig. 4.4.5.

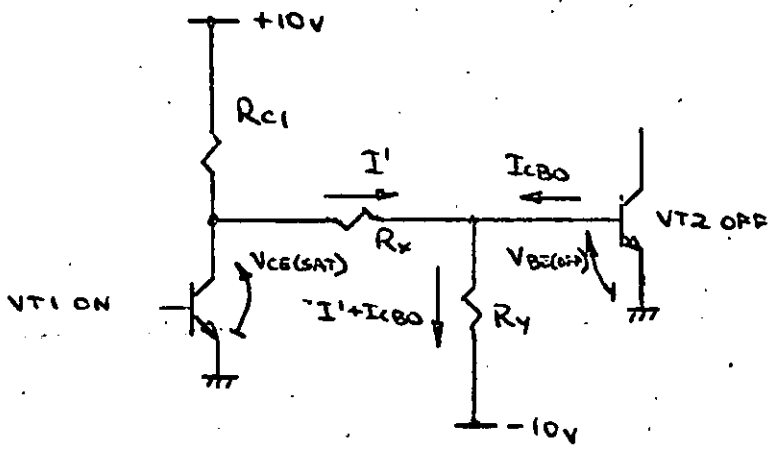


Fig. 4.4.6

Circuit Analysis

The main objective of the design is to ensure that the base biasing provides sufficient base current to hold the transistor saturated, and in the case of the monostable it holds the second transistor off, as required.

For the astable generator the maximum base current is given by:-

$$I_B = \frac{10 - V_{BE}(ON)}{R_B}$$

For a maximum collector current of 15 mA, and a minimum $h_{FE} = 50$, the base current required is 1/3 mA. This gives a maximum value for $R_B = 27k\Omega$.

The nominal collector load used is $1.5k\Omega$, which takes a current of 6mA, when the transistor is saturated. Thus 9mA of current is available to drive external circuits. The capacitor values can be calculated to give the required pulse lengths from the previous expressions.

In the monostable circuit the 'bias chain' comprising R_{C1}, R_x, R_y, must ensure that the base of VT_2 is biased that $V_{BE} \leq 0_V$, when VT_1 is on, and that it can supply the required base current to saturate VT_2 in the quasi-stable state.

Fig. 4.4.6. gives the 'bias chain' in the off state for VT_2.

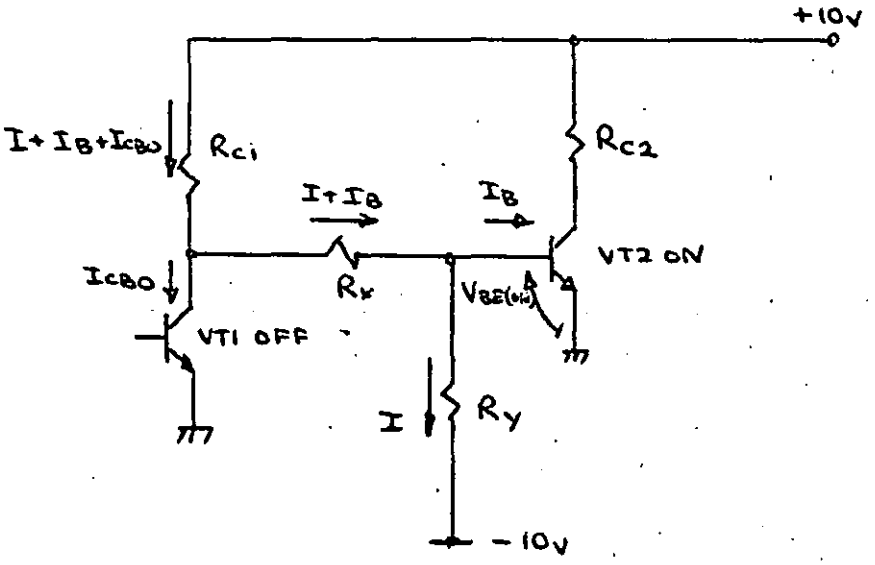


Fig. 4.4.7

Circuit Analysis

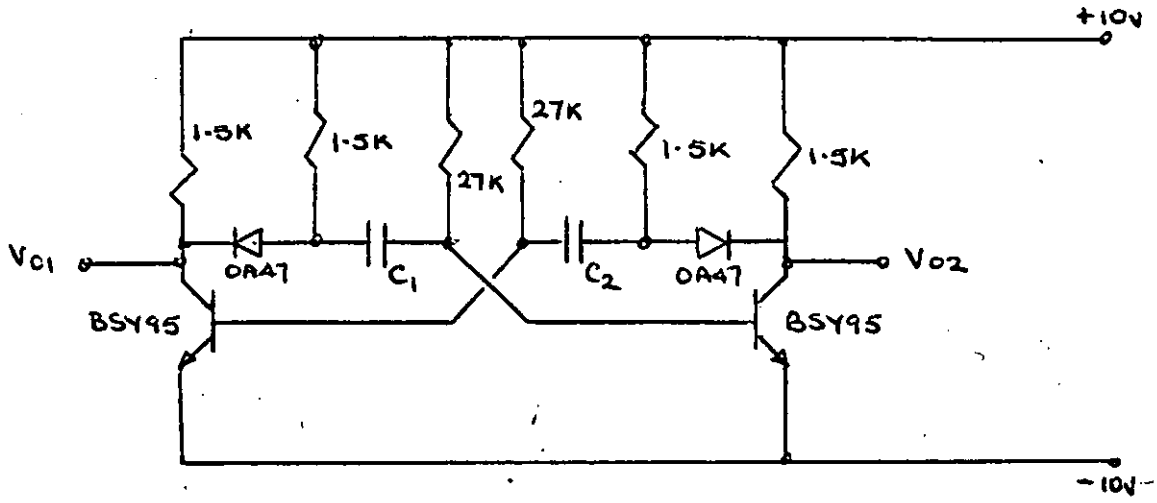


Fig. 4.4.8

Final Circuit Astable Pulse Generator

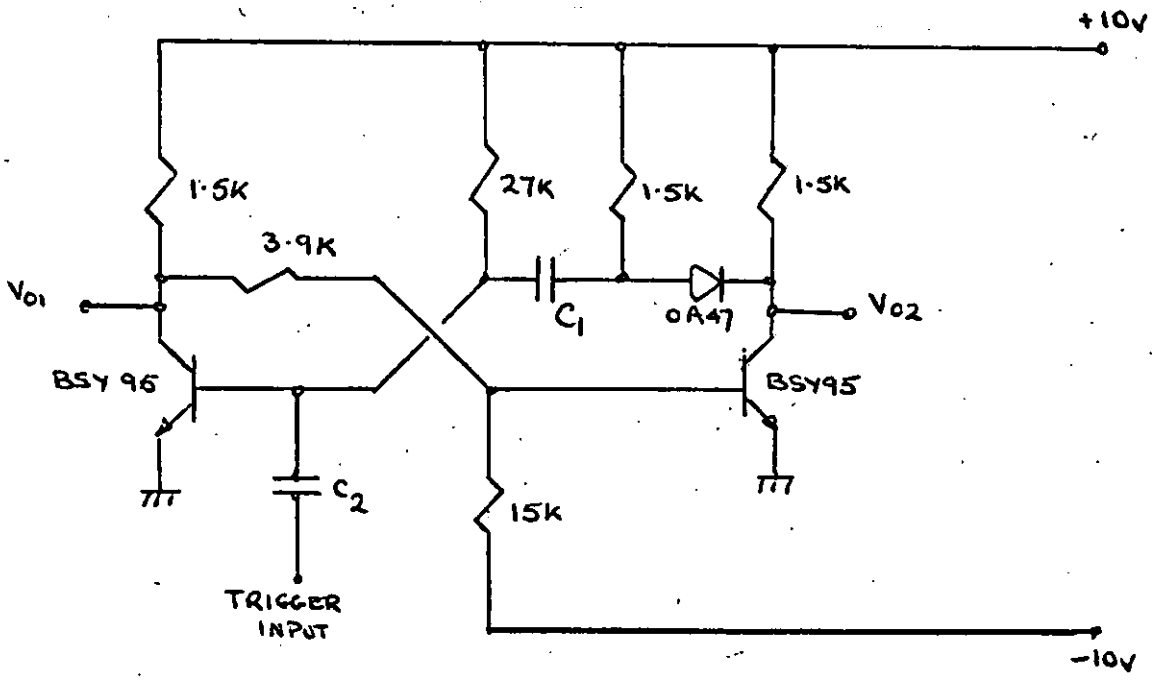


Fig. 4.4.9

Final Circuit Monostable Pulse Generator

Nodal Analysis gives:-

$$V_{CE}(SAT) - V_{BE}(OFF) = I' R_x \quad \text{----- (1)}$$

$$V_{BE}(OFF) + 10 = (I' + I_{CBo})Ry \quad \text{----- (2)}$$

Fig. 4.4.7 gives the bias chain in the on state for VT_2.

Nodal Analysis gives:-

$$10 - V_{BE}(ON) = (I + I_B)R_x + (I + I_B + I_{CBo})R_{C1} \quad \text{---- (3)}$$

$$V_{BE}(ON) + 10 = IR_y \quad \text{----- (4)}$$

A possible solution is found to be:-

$R_{C1} = 1.5k\Omega$ Rx = $3.9k\Omega$ Ry = $15k\Omega$.

Thus the final circuits for the astable and monostable pulse generators are shown in figs. 4.4.8 and 4.4.9.

In certain cases a variable delay or pulse length is required. To achieve this either, or both base resistors R_B, are replaced by a fixed resistor in series with a variable. By suitable arrangement of the capacitor and resistor values the required range of pulse widths can be covered.

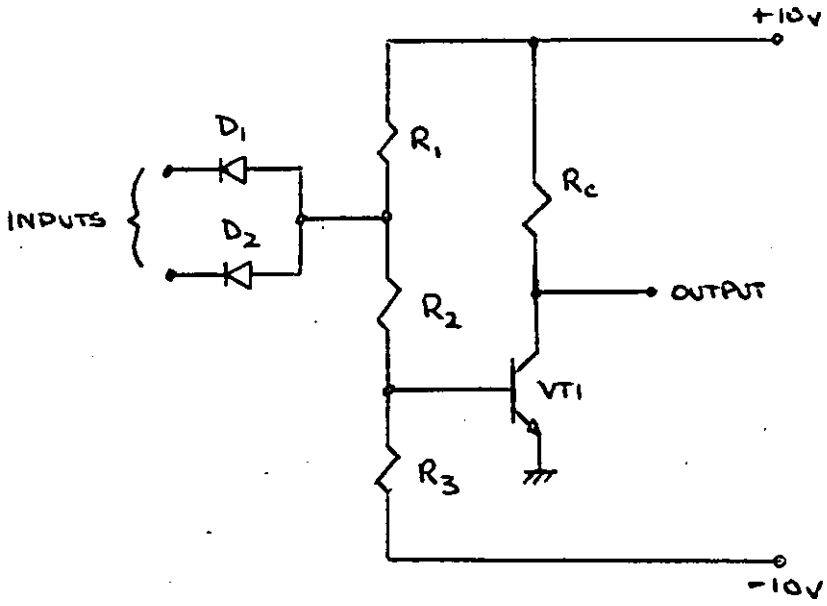


Fig. 4.5.1

Basic NOR Gate

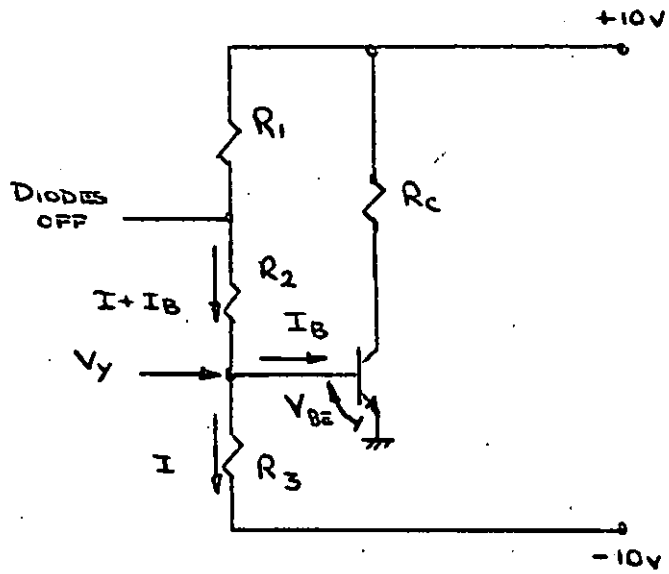


Fig. 4.5.2

Transistor On

Section 4.5

Gate Design

The gate circuits used here are generally referred to as Diode Transistor logic. The basic circuit is shown in fig. 4.5.1. The logical function performed is that of NAND or NOR, depending upon the polarity assigned to the 'I' input level. If we assume that the 'I' input is an earth level, then the function becomes NOR.

The design requires the consideration of the dc conditions applicable to both states, and the ac switching performance. However, since there is no requirement for particularly fast switching the ac design can be omitted.

The two sets of dc conditions under consideration are:-

1. A positive input, the diodes are biased off and the transistor is on and saturated. The output is therefore VCE(SAT) above earth, from the low impedance source of a bottomed transistor.
2. An earth input, the diodes are switched on and transistor is biased off. The output then becomes the positive voltage rail as seen through the collector resistor.

In case 1, the relevant circuit is shown in fig. 4.5.2. The diodes are cut off and it is only necessary to supply sufficient base current to bottom the transistor.

Nodal Analysis gives:

$$(10 - V_y) = (I + I_B)(R_1 + R_2) \qquad \text{------ (1)}$$

$$(V_y + 10) = I\,R_3 \qquad \text{------ (2)}$$

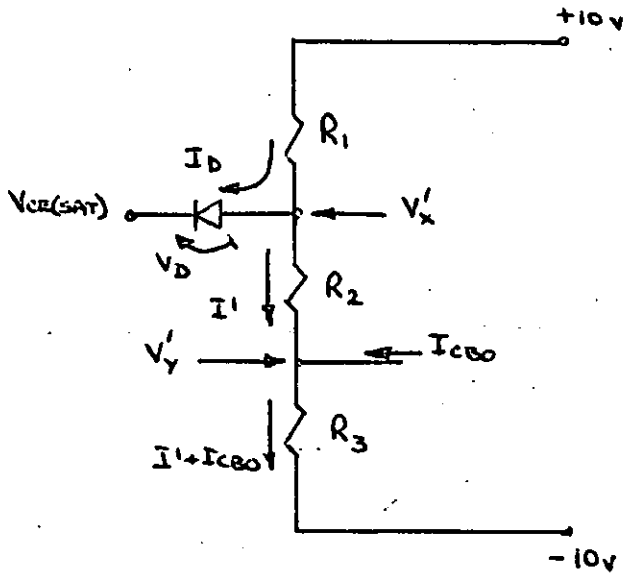


Fig. 4.5.3

Transistor Off

In the second case, the relevant circuit is shown in fig. 4.5.3. The input on the diode will be $V_{CE}(SAT)$ and thus the potential at point X will be given by:-

$$V'_x = V_{CE}(SAT) + V_D$$

Where V_D is the forward voltage of the diode.

Nodal Analysis gives:-

$$(Vx' - V'_y) = I' R_2 \qquad \text{------ (3)}$$

$$(V'_y + 10) = (I' + I_{CBO})R_3 \qquad \text{------ (4)}$$

For the constants, as usual in this type of design, worst case figures are used. These can be summarised as below:-

$V_{CE}(SAT) \leq 0.5$ volt

$V_D \leq 0.5$ volt (Germanium)

$V_{BE}(ON) \geq 0.7$ volt $\quad V_{BE}(ON) = 1.0$ volt say

$V_{BE}(OFF) \leq 0$ volt $\quad V_{BE}(OFF) = -1.0$ volt say.

For case 1.

$$V_y \doteq V_{BE}(ON) = 1.0 \text{ volts.}$$

Assuming that the maximum collector current is to be 25 mA, then for a worst case h_{FE} of 50, the maximum base current = $\frac{1}{2}$mA. Also on the grounds of stability it is desirable to make the current in the bias chain large, in comparison to the base current. Here we shall assume that the chain current, $I = 3\ I_B$

Then from (1), $9 = 2\ (R_1 + R_2)$

from (2), $11 = 3/2\ R_3$

$$R_3 = \frac{22}{3} = 7.34 \text{ K}\Omega$$

For case 2.

$$V_x' = V_{CE}(SAT) + V_D = 1.0 \text{ volts.}$$

$$V_y' = V_{BE}(OFF) = -1.0 \text{ volt.}$$

From (3) $2 = I' R_2$

Since the transistor is a silicon device the leakage current I_{CBO}, although present is sufficiently insignificant to ignore,

Thus from (4) $9 = I' R_3$.

Thus $\frac{2}{9} = \frac{R_2}{R_3}$

Hence $R_2 = \frac{2}{9}R_3 = 1.63K\Omega$

and since $(R_1 + R_2) = 4.5\ K\Omega$

Thus $R_1 = 2.87\ K\Omega$

The preferred values selected were:-

$$R_1 = 2.7K\Omega; \quad R_2 = 1.5K\Omega; \quad R_3 = 8.2\ K\Omega.$$

The collector load resistor can have any suitable value down to 400Ω, without causing a circuit malfunction. Nominally the load for logic operation is 1.8KΩ, this leaves approximately 20mA of current drive available.

The drive required by this gate is given by $I_D = \frac{10 - V'_x}{R_1}$

$$I_D \simeq 3.5mA.$$

This gives the gate a Fan-Out of 5, that is it will drive 5 similar gates.

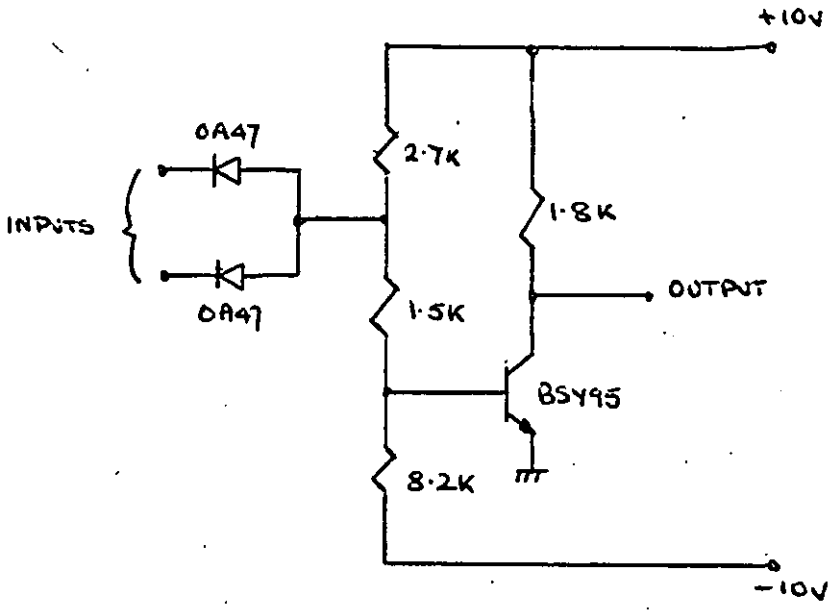


Fig. 4.5.4

Final Gate for Logic Applications

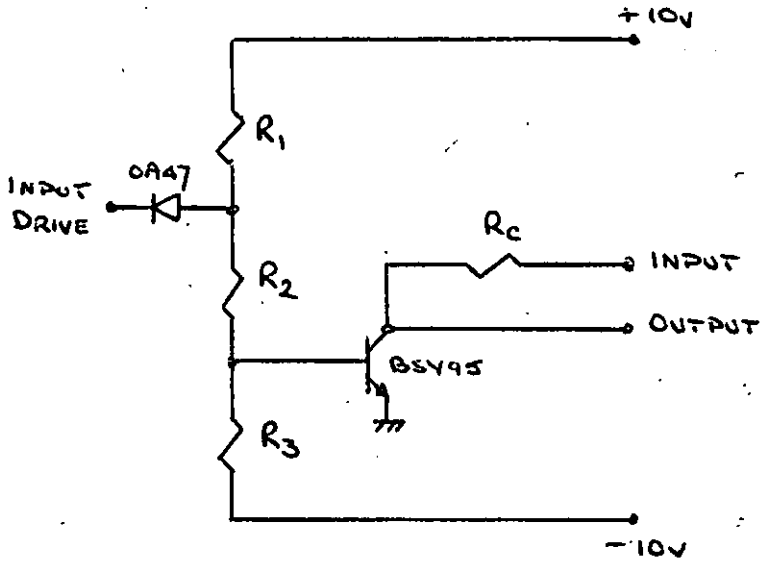


Fig. 4.5.5

Gate as an Analogue Switch

The final gate circuit is shown in fig. 4.5.4.

This type of gate can also be used as an analogue switch or chopper. The collector resistor is then returned to the signal which is to be chopped, and not the positive rail, as shown in fig. 4.5.5.

Normally with chopper circuits, the offset voltage is small, due to the small input voltage and currents. However in this case the offset, $V_{CE}(SAT)$, will be of a similar value to a saturating switch, since large signal levels are being handled. This can be compensated for, as will be discussed where this circuit finds its applications. The source impedance of the chopped signal is equal to that of the original signal in series with the collector resistor R_c.

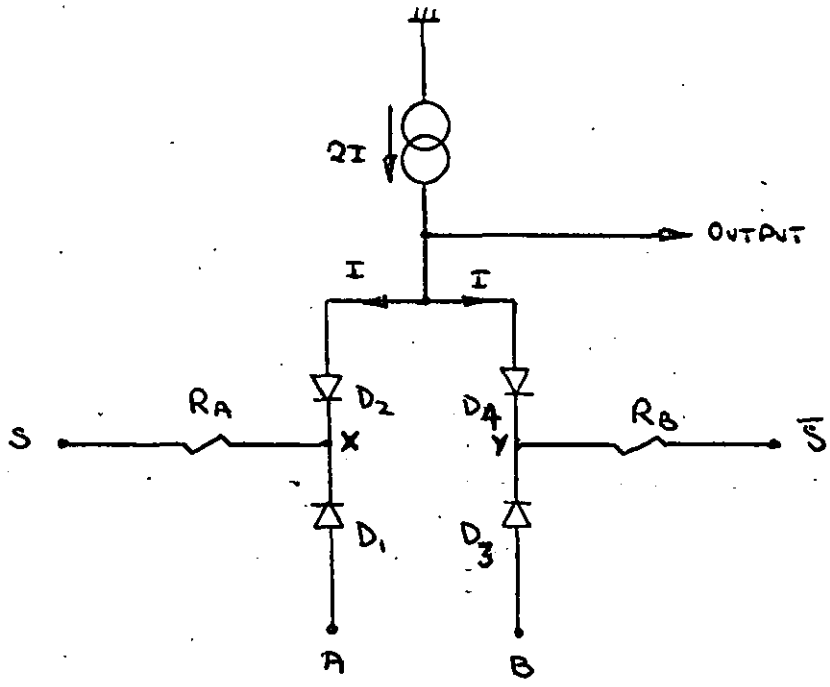


Fig. 4.6.1

Special Analogue Gate

Section 4.6

Analogue Gate, for Pulse Wave Simulator

The gate required in the simulator is a little more complex than its title would suggest since it is required to give an analogue output which can be switched to either of two analogue inputs. The basic gate configuration is shown in fig. 4.6.1, a switching signal and its inverse, are fed from low impedance sources to the points S and $\bar{S}$ as shown. The switching signal is of approximate amplitude 10 volts and is switched between -10 volts and earth. Considering the operation of the gate, the constant current generator gives a current 2I, which will split equally between diodes D_2 and D_4, provided that the resistors R_A and R_B are equal. This being so both D_2 and D_4 will be forward biased, and will form a low impedance path to an ac signal. The input signals at A and B are required to be small in amplitude and modulated onto a negative input level less than 10 volts. This being so consider the condition with S at -10 volts and $\bar{S}$ at earth. The diode D_1 will be forward biased, but D_3 will be reversed biased.

Thus the ac component on the A input will be transmitted to point X, and since D_2 is also forward biased, the output will also follow the signal at A. Reversal of the polarity

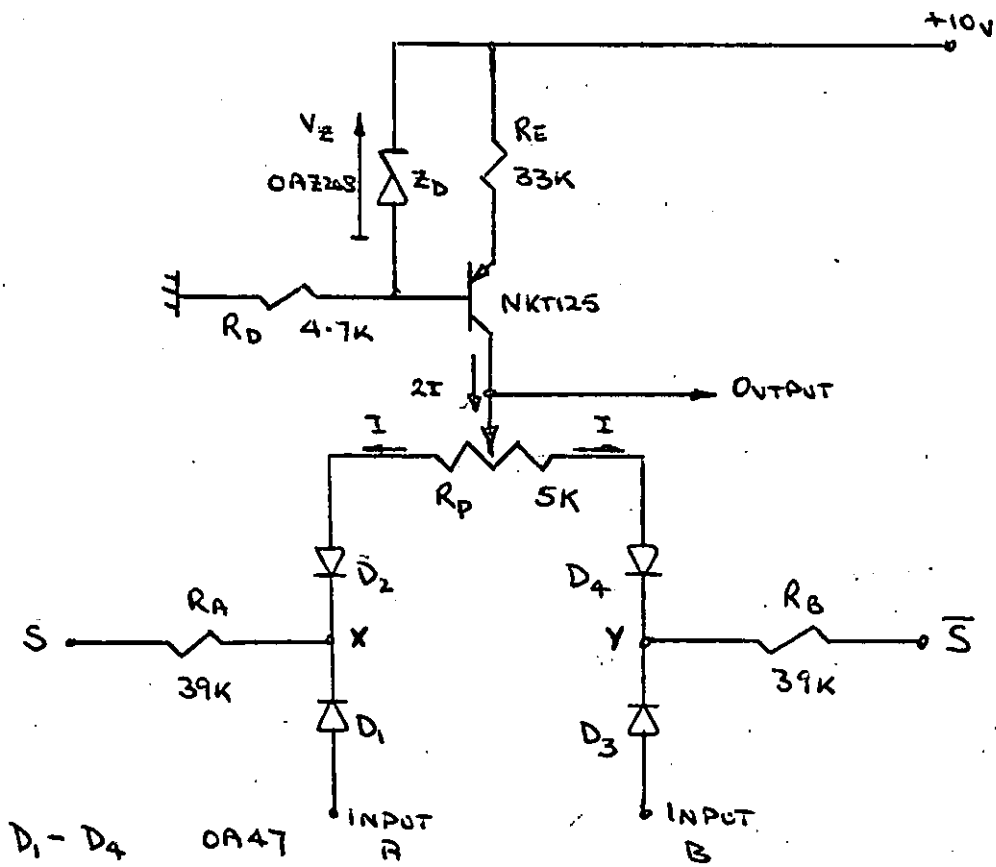


Fig. 4.6.2

Final Circuit Special Analogue Gate

of S and $\overline{S}$, would result in the input signal at B being transmitted to the output. Thus the basic objective has been achieved.

If D_1 and D_4 are similar diodes and the steady dc current through them is made equal, then the volt-drop from A to X will be equal and opposite to that from X to the output. Hence there will be no offset voltage between input and output.

The constant current generator can either be produced by a large resistor connected to a large positive voltage, or a transistor operating as such. The latter methods has been adopted here, the current is given by:-

$$I_C = (V_Z - V_{BE}) / R_E$$

Where V_Z is the zener voltage and R_E the emitter resistance as shown in fig. 4.6.2.

Another modification, which is of value here, is to place a potentiometer into the circuit, between the current source and the diodes, as shown in fig. 4.6.2. The current division will not be affected provided that R_p is small compared with R_A and R_B. This potentiometer will enable a variable offset voltage of either polarity to be generated. The maximum offset being IR_p. This can then be used as a differential level control between the two input signals, and avoids the necessity of using matched components.

The final circuit diagram, with component values is shown in 4.6.2.

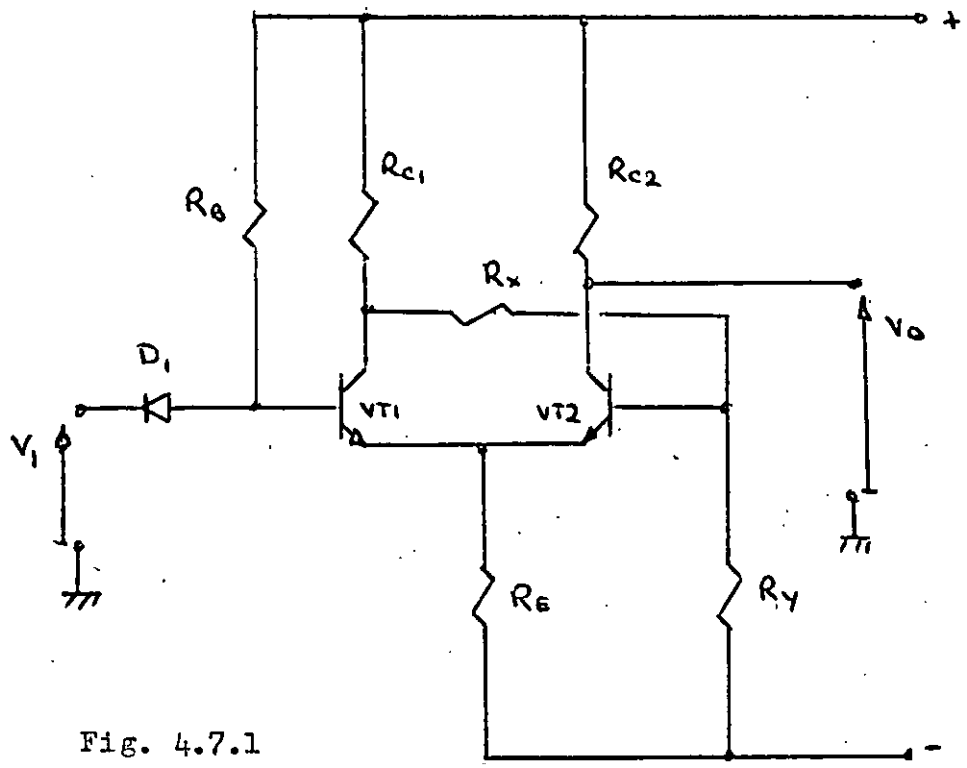


Fig. 4.7.1

Basic Schmitt Trigger Circuit

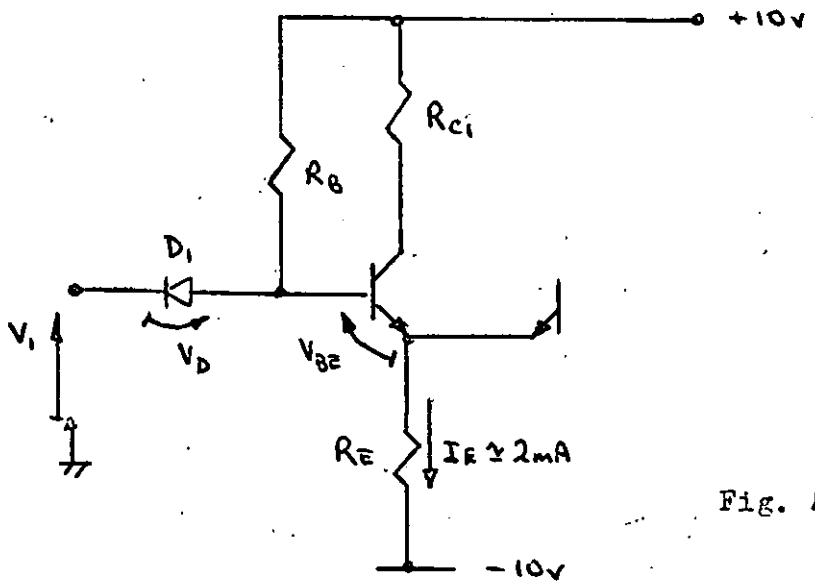


Fig. 4.7.2

Circuit analysis for above

Section 4.7.

Schmitt Trigger Design

The Schmitt trigger is a level sensitive switch, which changes state if the input should fall below, or rise above a set reference voltage. The circuit consists of an emitter coupled amplifier, with direct feedback from one collector to the other base. The basic circuit is shown in fig. 4.7.1, and is triggered by a negative input voltage.

The first transistor is biased on by R_B, and the direct coupling formed by R_x and R_y, holds the second transistor off. Application of a negative input voltage greater than the reference level, turns VT_1 off and in doing so switches VT_2 on.

The circuit is designed such that the voltage swing on the output collector is compatible with that in the conventional logic described earlier.

In designing the circuit it is assumed that the nominal collector current on either side, when on, is 2mA. This defines the collector load resistors , since for compatibility of the output swing with normal logic, requires the collector loads to be 5kΩ , or preferred value of 4.7kΩ. This does assume that the bias chain R_x, R_y does not significantly load the first collector. The reference voltage level is set by the emitter resistor, R_E, and is required to be approximately -4.5 volts. Fig. 4.7.2, gives the circuit in its normal state and from this it is possible to calculate the reference voltage level.

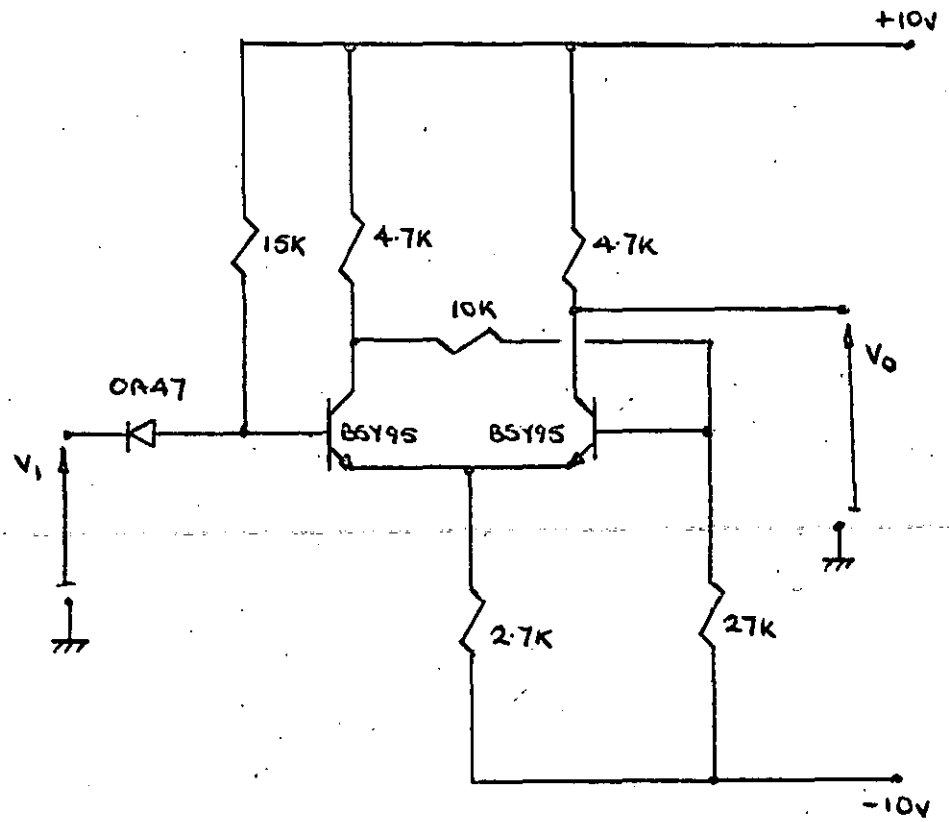


Fig. 4.7.3

Final Circuit, Schmitt Trigger

Analysis gives:-

$$V_1 = I_E R_E + V_{BE} - V_D - 10.$$

A typical value for V_D would be 0.5 volts, and the transistor would start to switch with $V_{BE} \simeq 0.5$ volts. This gives a preferred value of 2.7kΩ to resistor R_E.

The resistor R_x and R_y must be chosen so as to ensure VT2 is off when VT1 is on, and vice-versa. Suitable values have been found to be R_x = 10kΩ and R_y = 27kΩ.

The resistor R_B is required to supply sufficient base drive to hold transistor VT1 on, in the circuit's normal state. The value used here is 15kΩ. The final circuit of the Schmitt trigger is shown in fig. 4.7.3.

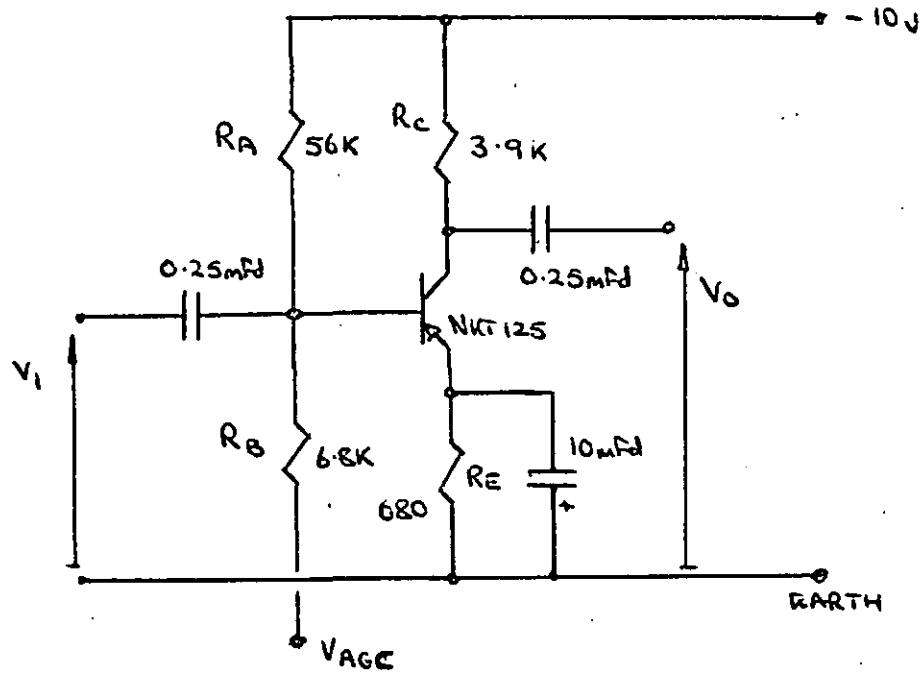


Fig. 4.8.1

Typical AGC Stage

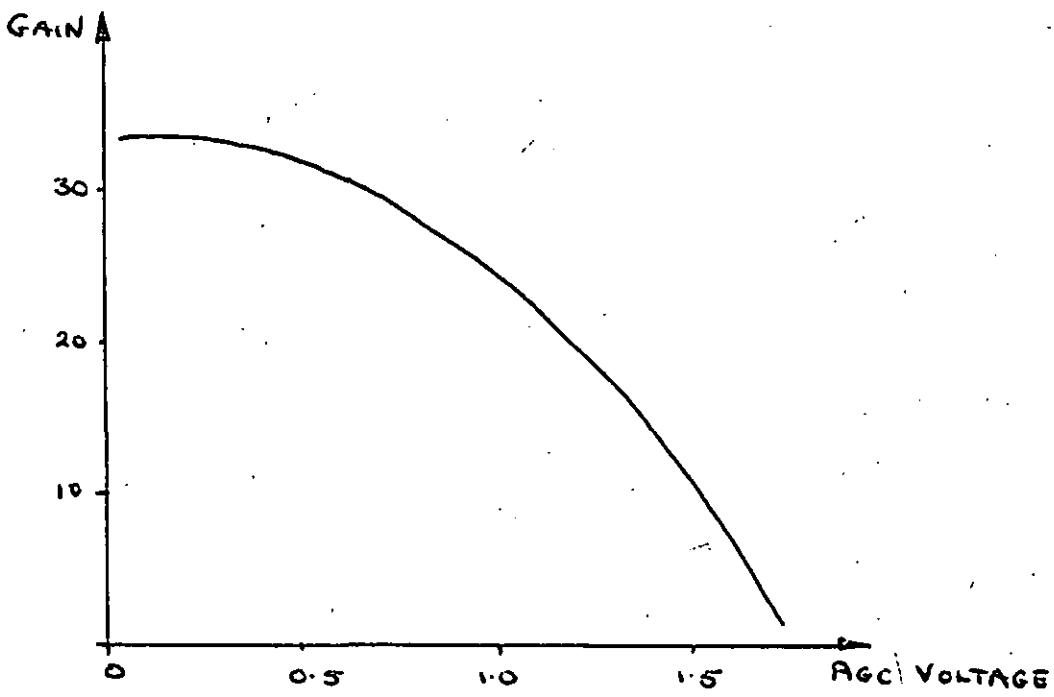


Fig.4.8.2 Gain:AGC Voltage for above fig.

Section 4.8

Automatic Gain Control Design

As discussed in Section 2, the system requires that the pulse-wave input, be of a given magnitude, irrespective of the frequency and amplitude of the signal output from the transducer preamplifier. In addition, the gain control device must operate using the peak vallue of the signal, as the controlling signal.

There are several methods, by which gain control cam be applied, (41), (42), (43), (44), however the most efficient is to use the non-linear impedance of a junction diode. In the junction diode the ac impedance is a function of the standing dc current. (See Appendix C).

To take full advantage of the transistor action the diode used is the base-emitter diode of the transistor stage producing the gain control. A typical AGC stage, with control on the dc base current is shown in fig. 4.8.1. The dc base current is controlled by applying a control voltage to resistor R_B, as shown.

The experimental results relating the stage gain to the applied AGC voltage are shown in fig. 4.8.2. and as can be seen the gain is a function of this voltage.

Over a limited operating range this characteristic can be specified as:-

$$A_V = a - b\, V_{AGC}$$

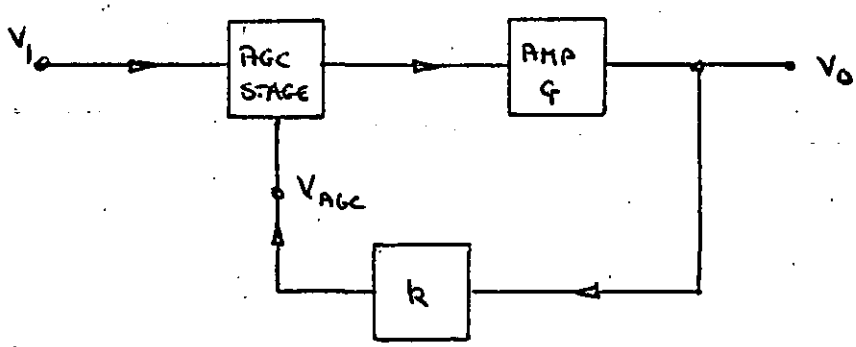


Fig.4.8.3

AGC System

Now consider the system as shown in fig. 4.8.3, the AGC stage is followed by an amplifier of gain G_1, so that the output is now given by:-

$$V_o = A_v.G.V_1$$
$$V_o = (a - b.V_{AGC})V_1$$

This output signal is now 'processed' in such a manner as to give a dc level given by kV_o, which is fed back as the AGC voltage. This gives:-

$$V_o = (a - bkV_o)\, G.V_1$$

$$\text{Thus} \quad V_o = \frac{1}{\left(\frac{1}{aGV_1}\right) + \left(\frac{bk}{a}\right)}$$

If the gain G is large, then $1/G \rightarrow 0$, and the output V_o becomes $\left(\frac{a}{bk}\right)$ which is constant and completely independant of the input voltage. Thus the principle of the gain control system has been established. Obviously the output is only constant to an order of magnitude; to obtain suitable values for the constants an error quantity, E, is defined as:-

$$E = \frac{\Delta V_o}{\Delta V_1} \simeq \frac{\partial V_o}{\partial V_1}$$

Thus differentiating the original expression with respect to V_1 gives:-

$$E \simeq \frac{1}{\left(\frac{1}{aGV_1} + \frac{bk}{a}\right)^2} \cdot \left(\frac{1}{aG\ V_1^2}\right)$$

However, $bk \gg \frac{1}{GV_1}$

Thus $E \simeq \frac{a}{b^2k^2V_1^2G}$

But the nominal output of the system is given by $\left[\frac{a}{bk}\right]$, and thus the expression for E can be rewritten as:-

$$E \simeq \left[\frac{V_0}{V_1}\right]^2 \frac{1}{a\,G} = \frac{A^2}{aG}$$

Where A is the 'steady state' gain of the AGC system.

Now relating the above to the physical system, the steady state gain will be given by the nominal output signal divided by the minimum input signal.

$$A = V_0/V_1(MIN)$$

The differential quantities ΔV_1 and ΔV_0, will be given by the maximum range of operable conditions at both input and output.

That is $\Delta V_1 = V_1(MAX) - V_1(MIN)$, and ΔV_0 is the permissable range of the input voltage to the exponential amplifier, and V_0 is the mean value of this range .

The range of output signals from the transducers preamplifier has been estimated as 0.2 to 20mV; and the nominal input for the exponential amplifier is 1.15 volts with a tolerance of ± 10mV, for a stable signal.

Thus in terms of the symbols used here, $V_1(MIN) = 0.2$ mV; $V_1(MAX) = 20$mV; $V_0 = 1.15$ volts; $\Delta V_0 = 20$mV

These figures require that the gain G, is approximately 10^6

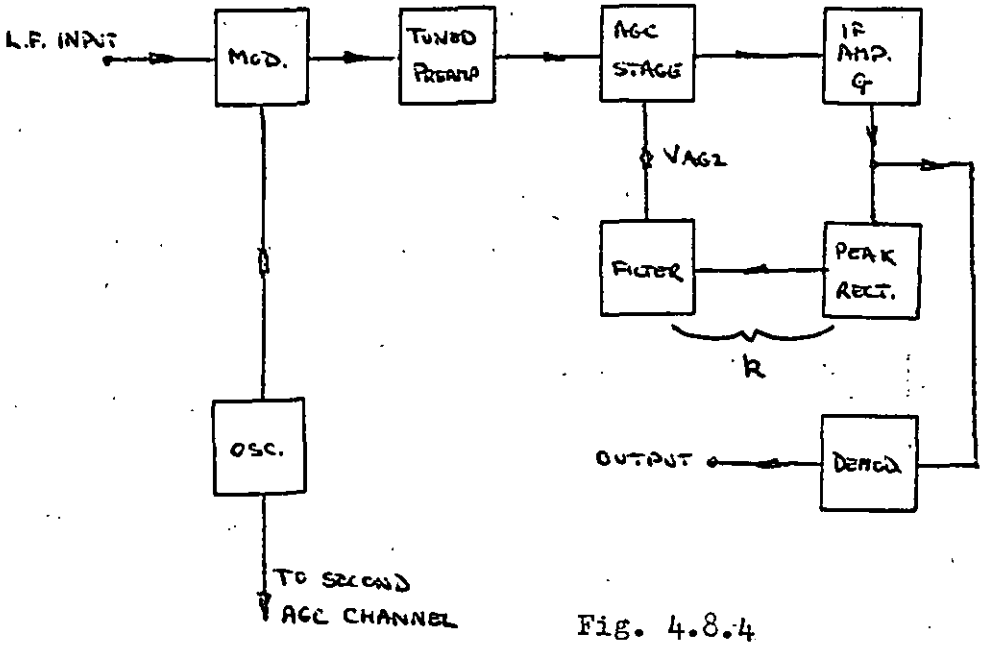


Fig. 4.8.4

Proposed AGC System for an LF Input Signal

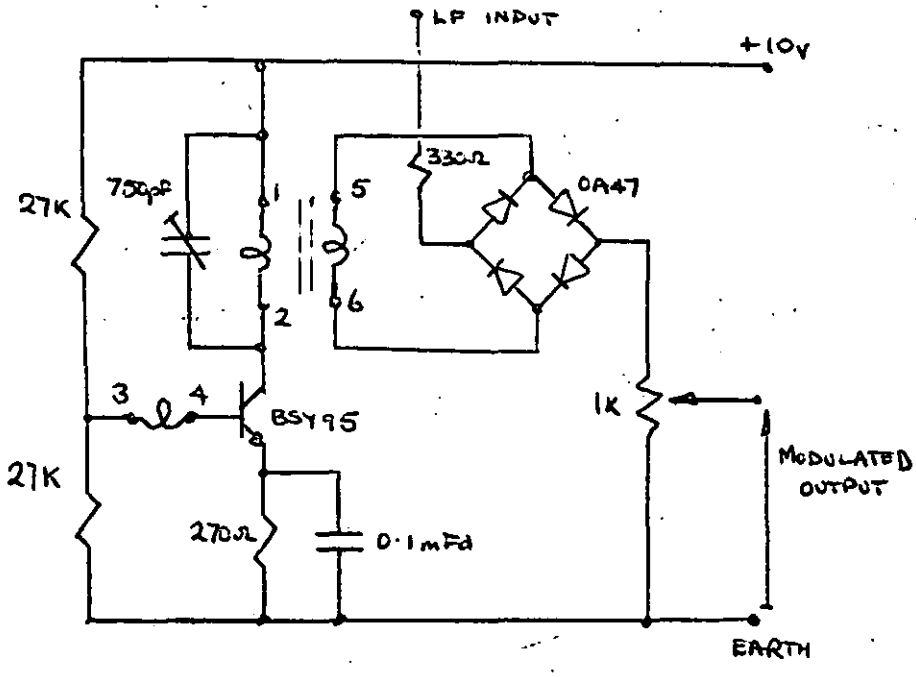
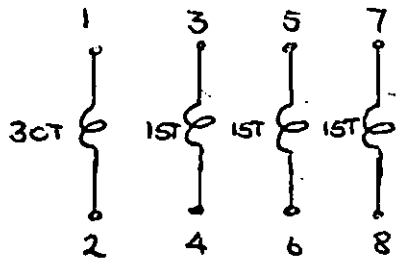


Fig. 4.8.5(a)

Oscillator and Modulator



Former, Mullard Vinkor (Medium Size)

Fig.4.8.5(b)

Coil Details

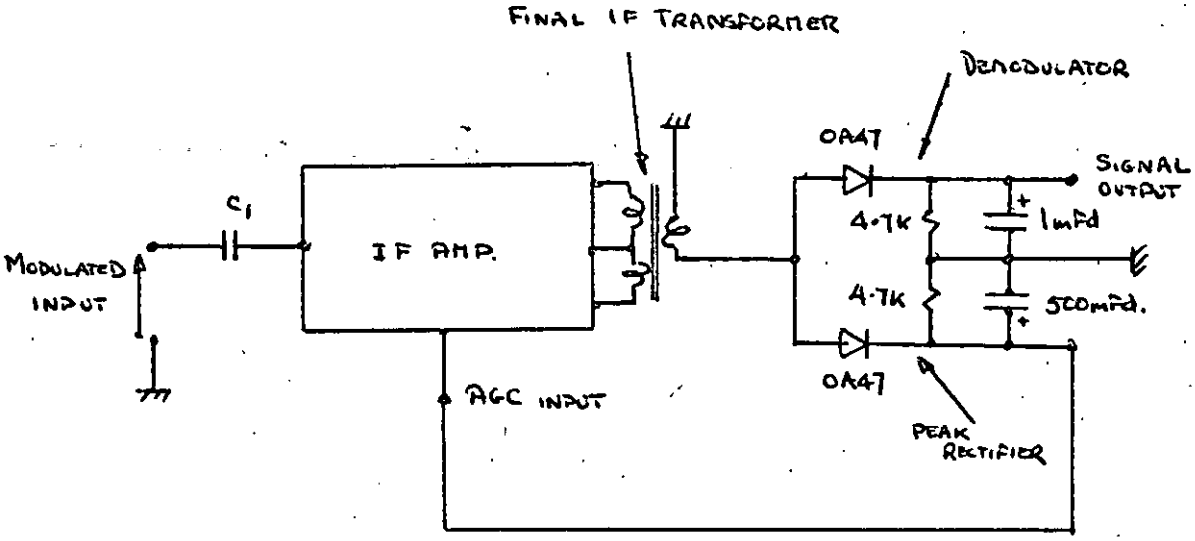


Fig. 4.8.6.

IF Amplifier with AGC Loop

which is an easily obtainable figure.

This method of gain control depends upon the change in the dc biasing of a transistor, for its functioning and this requires that the signal is ac coupled to the gain control stage. However with the low frequency nature of the pulse wave this would result in coupling time constants of the order of 2 secs. This would produce an excessive settling time to an input disturbance and prevent the system from functioning properly.

To overcome this the pulse wave is amplitude modulated onto a suitable carrier frequency, and for ease of design this is chosen to be 470kc/sec, that is the IF transformers from a domestic radio receiver can be used in a conventional IF strip to give the required gain.

This assumes that piezo-electric transducers are being used and the signal is initially free from a carrier. If a carrier modulated type of transducer is used then the carrier frequency will have to be modified to suit the transducer.

The proposed system is shown in fig. 4.8.4, the carrier oscillator has two outputs provided so that only one oscillator is required for the two channels. The oscillator and modulator are shown in fig. 4.8.5, whichisan LC tuned oscillator driving a diode bridge modulator. The IF amplifier used was modified such that the preamplifier was used merely as a filter, by removing the decoupling capacitor from the emitter of the first transistor. Also the AGC loop was modified as shown in fig. 4.8.6.

This system, although found operable experimentally, was not fully tested since its final form requires an accurate knowledge of the signal from the transducer preamplifier, but the theoretical treatment given earlier is quite rigorous.

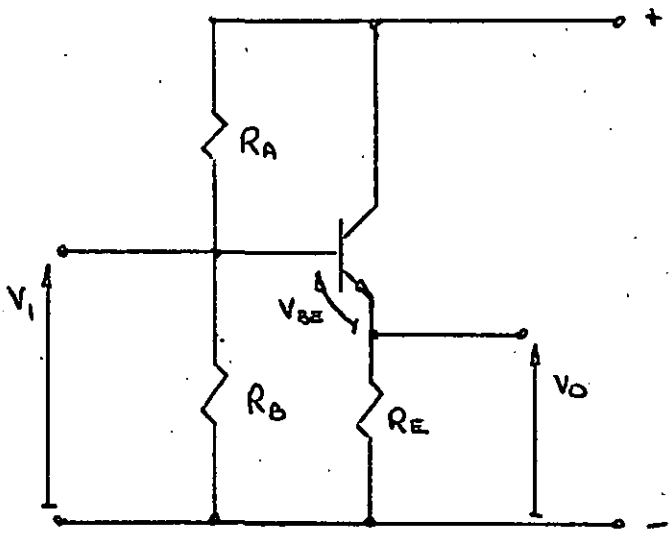


Fig. 4.9.1

Basic Emitter Follower

Section 4.9.

Emitter Follower Design. (Including 'Set L' Analogue Voltage Control)

In certain cases a power driver stage is required to distribute a signal within the system. The signal should not be attenuated or shifted from its dc level, but come from a low impedance source. In general an emitter follower is used for this purpose, since it is an amplifier with a voltage gain of unity and a current gain defined by the transistor used. The circuit can be considered as an impedance converter and can be used to provide a high input impedance, in addition to providing a low output impedance.

The basic circuit and method of biasing is shown in fig. 4.9.1, although in certain circumstances R_B or, R_A and R_B, can be omitted.

The output signal will be offset by the transistor V_{BE}, and the signal handling capacity is limited to the voltage rails to which the circuit is connected, and the maximum ratings of the transistor.

The input impedance is given approximately, by the parallel impedance of R_A, R_B and $h_{FE}R_E$; the output impedance is dependent on the source impedance of the signal, but must be less than R_E, in all cases.

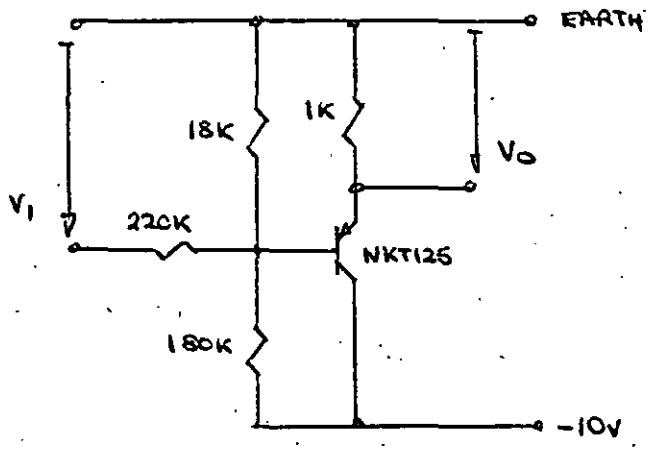


Fig. 4.9.2

Attenuating Emitter Follower

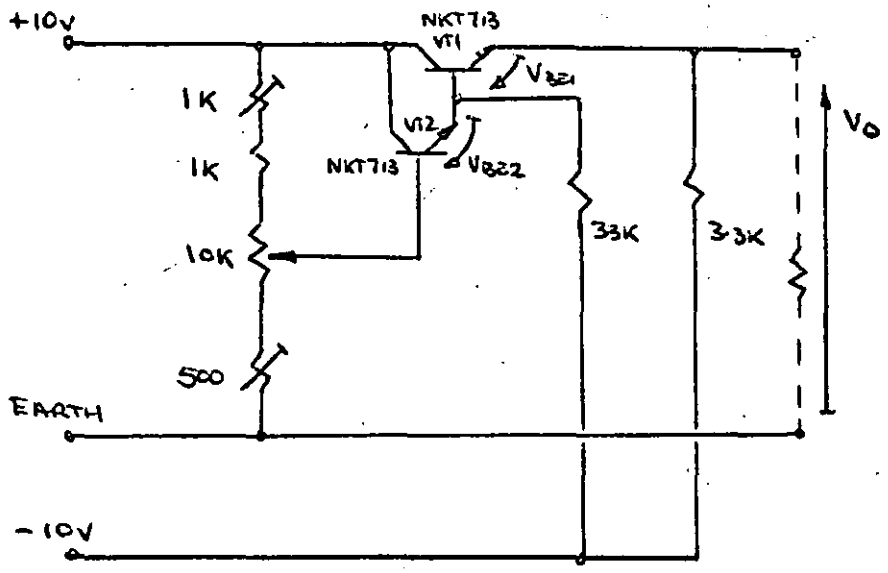


Fig 4.9.3

Set 'L' Analogue Voltage Generator

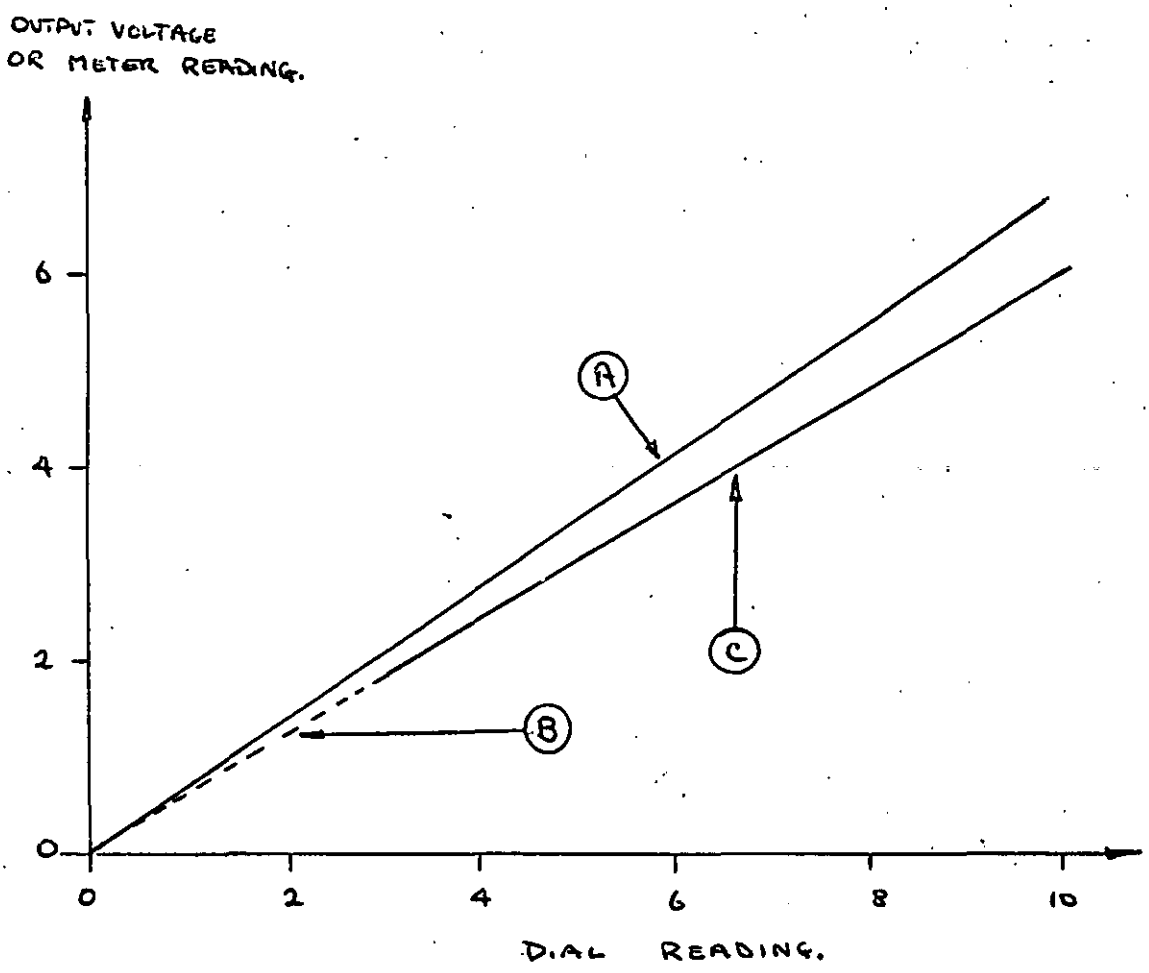
If the source impedance is low enough to provide the dc biasing for the transistor without the inclusion of both R_A and R_B, it is normal then to omit them.

In the Simulator a high i/p impedance emitter follower is used to buffer the shaping circuits from the analogue gate which follows them. In addition it attenuates the signal to a suitable amplitude for the gate to handle and sets the correct dc biasing for the gate on its output. The attenuation is produced by placing a resistor in series with the input as shown in fig. 4.9.2.

Another special application of an emitter follower is the device used to take the dc level, which is the divider output, from the RC filter producing it. The emitter follower is provided with variable biasing, and thus can be used to set initial conditions of charge on the capacitor to compensate for offset voltages.

Yet another specialised application is the method in which a variable dc voltage is produced, from a low impedance source to correspond to the arterial length. The basic circuit for this is shown in fig. 4.9.3.

The circuit is basically a high gain emitter follower circuit, produced by connecting two transistors as a Darlington pair. The input to this circuit is provided by the base chain as shown. The output will nominally be equal to $V_p - V_{BE2} - V_{BE1}$.



A Direct reading using a voltmeter.

B PWV meter reading x1 Range.

C PWV meter reading x5 Range.

Fig. 4.9.4

Set 'L' Analogue Voltage Generator Output

The base-emitter voltages of the two transistor are stabilised by drawing current from them to the -10v rail as shown. The 10k potentiometer is a precision 10 turn helical pot, and thus it provides an accurate potential divider, chain, provided that the current taken by the base of VT_2 is small.

The 500Ω and 1kΩ trimmers enable the calibration of the device to be carried out. At the zero end, the 500Ω trimmer enables the offset on the transistor chopper to be compensated for, and the 1k trimmer provides for amplitude calibration.

The results of a test relating the output voltage to the potentiometer reading is shown graphically in fig. 4.9.4, and as can be seen, the relationship is linear, with an offset produced by the 500Ω trimmer.

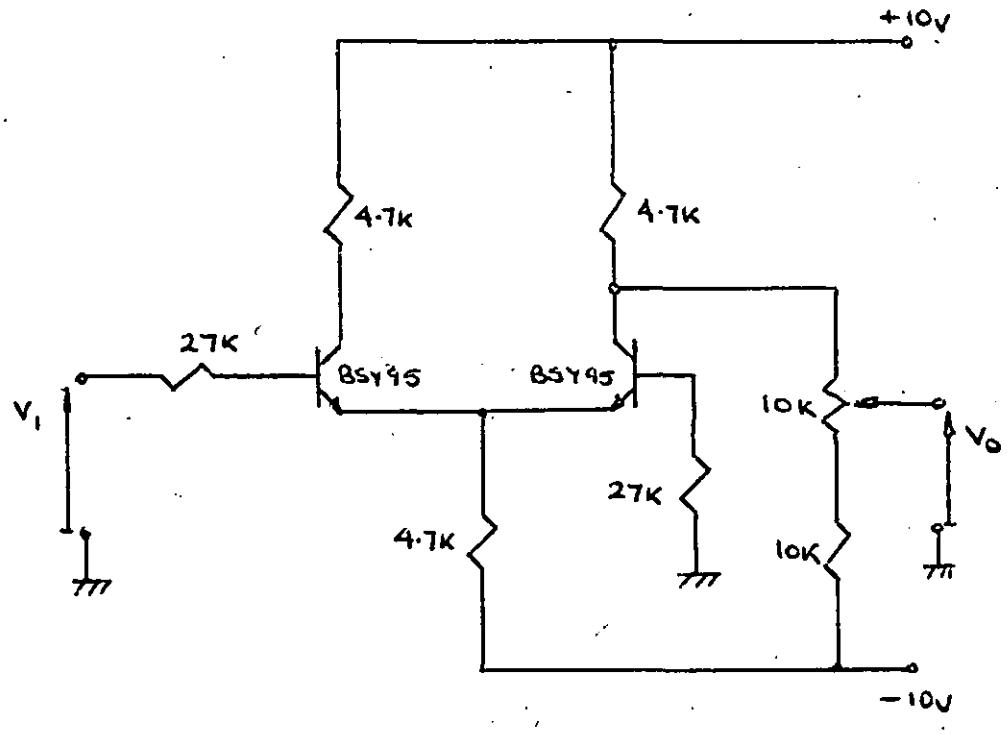


Fig. 4.10.1

Phase Correcting Amplifier

Section 4.10.

DC Phase Correcting Amplifier

The simulator provides a negative going output signal, below earth, and this amplifier is used to invert and amplify it slightly so that the signal can be used as intendad.

The circuit diagram is shown in fig. 4.10.1, and is basically a long tailed pair, which is current driven. The inverted output signal is taken from a potential divider chain, as shown, so that the quiescent dc level can be set to earth.

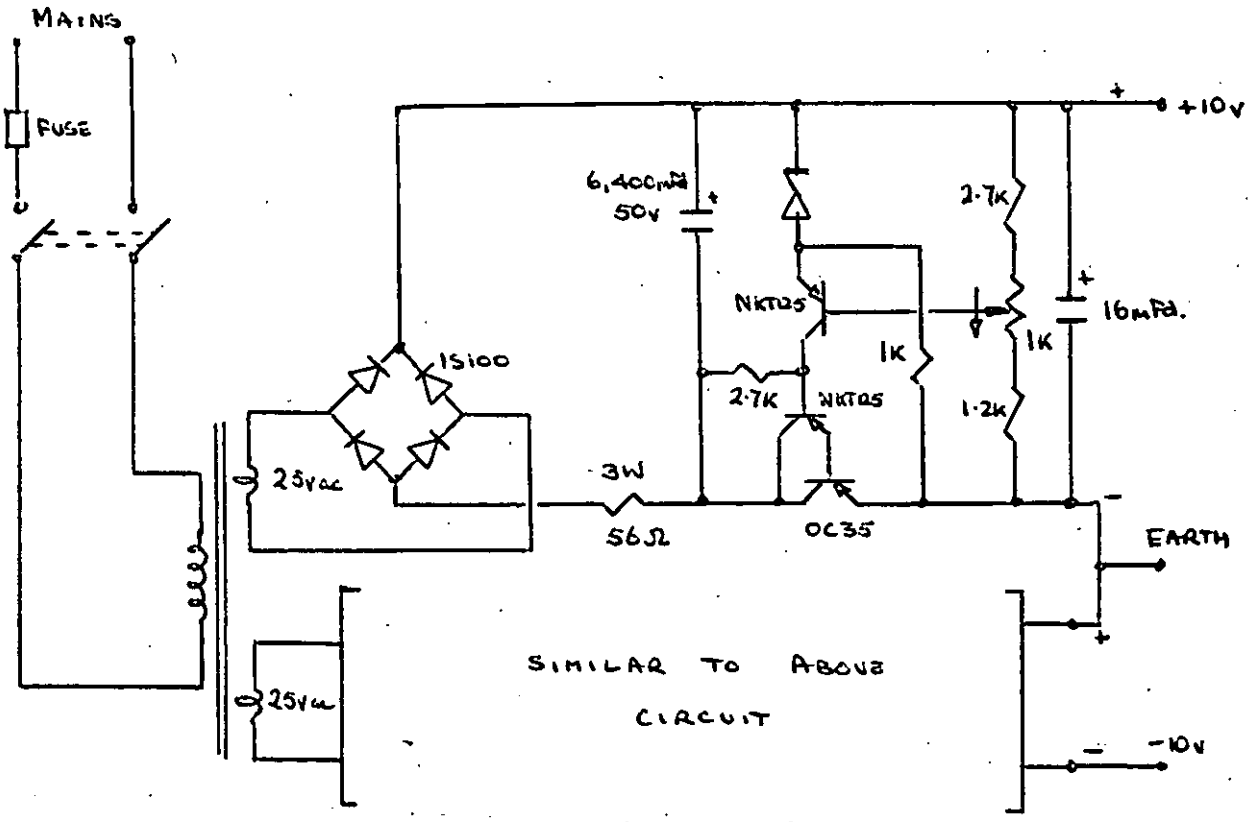


Fig. 4.11.1

Power Unit

Notes. 1) The OC35 transistors are mounted in heat sinks.

2) Transformer, Radiospares Rectifier Supply Transformer, 30v Type.

Section 4.11.

The Power Unit

As stated in the introduction to this section, all the equipment has been designed to operate from either + or -10 volts or both. Thus the power unit must supply + and -10 volts, with sufficient power to drive the system. The overall current rating on either voltage rail is considered to be less than ½ amp.

The unit is manufactured from two identical supplies each nominally 10 volts, the output of which is floating with respect to earth. These supplies are designed to give a full load current of ½ amp, and consist of a low voltage transformer, followed by a bridge rectifier and RC smoothing to give the raw dc supplies. The regulation is achieved by using a series stabilizer, which uses a zener diode as a reference element. The circuit is fitted with a potentiometer in the feedback loop to enable the output to be set accurately to 10 volts.

The complete circuit for the power unit is shown in fig. 4.11.1.

The typical supply performance has been measured experimentally and the results are shown below:-

Nominal Output Voltage	10 volts
Full Load Current	0.5 amps
DC Regulation at Full Load	1%
AC Ripple at Full Load	5 mV pk/pk

SECTION 5

The Transducer and its Preamplifier

As stated earlier, the actual transducer used has been designed by Dr. J.M. Ivison, but nevertheless a general discussion on its requirements will not be out of order.

The paper by Eckenrode and Kirshner (15), is a general one which describes the types of transducer which are available for measuring pressure transients. Various other references relate to the measurement of blood pressure directly, but are of interest in demonstrating how crude the science is at present. The paper by Davies et al (32), describes a device on which the design has been based. Thompson, (34) is experimenting with small transducers for measuring blood pressure directly in an artery, but the type of transducer, could have applications in monitoring the pulse wave as well.

The transducer must be sensitive enough to monitor the pulse waves, which at a pressure point are in the order of 2 psi, and be small enough to be positioned accurately.

The electrical and mechanical characteristics should give a flat frequency response from 1-20 c/sec, and provide a suitable method of mounting the transducer to a patient without causing discomfort; also the static contact pressure should not be too large since this could interfere with the physiological mechanism.

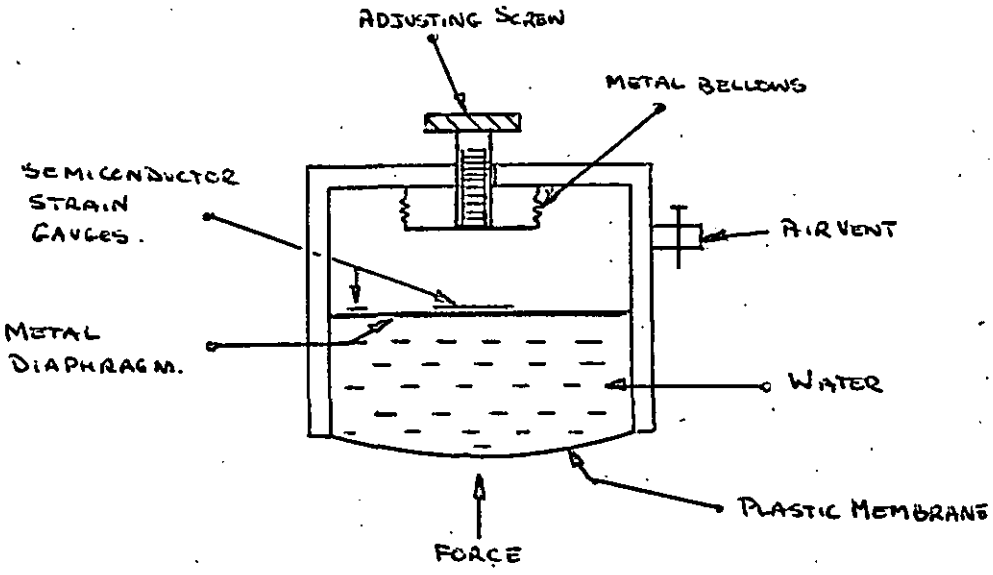


Fig. 5.1

Construction of Transducer used by Davies et al.

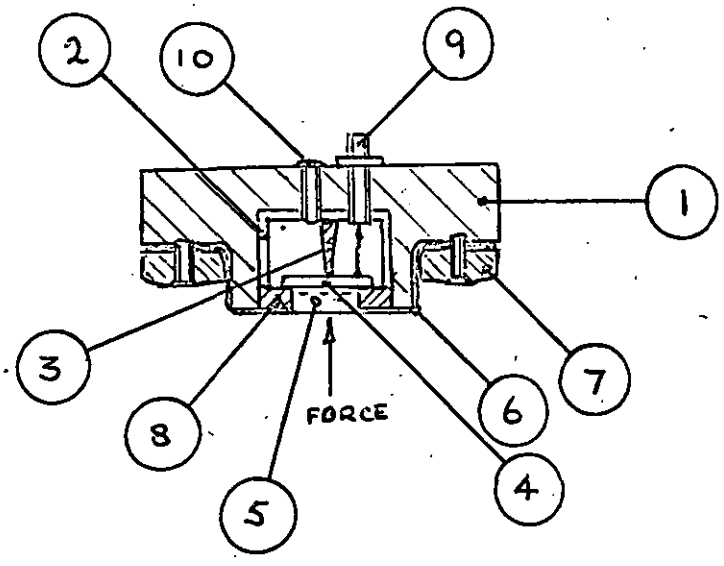


Fig. 5.1.1

Transducer Construction

Stiff metal diaphragms mounted above arteries can lead to trouble with the centring which results in an unequal stress distribution. To overcome this Davies et al, have used a fluid sac as shown in fig. 5.1. The force is then transmitted uniformly through the fluid to the diaphragm, and thus avoids the centring necessity. In addition they provide the facility of offsetting the static pressures set up in the diaphragms, as shown.

Section 5.1

Transducer Design

The transducer used here is a piezo-electric type and thus will only respond to a change in pressure. This avoids offsetting the static pressures set up in operation, provided they are not too large. The actual construction is shown in fig. 5.1.1. The aluminium alloy case (1) takes the PTFE housing (2) and support (3) for the piezo-electric ceramic disc (4). In front of the disc is an oil-filled space (5), sealed by membrane (6), which is held in position by a clamping ring (7). (8) is a PTFE spacer to provide the oil-filled space between the disc and the membrane.

The cavity behind the disc is filled with oil-filled plastic foam to damp out reflection from the rear of the casing. (9) is a coaxial ouput socket and (10) is a screw by which the device can be filled with oil.

The frequency response of the device has been found by mounting it on a mechanical vibrator.

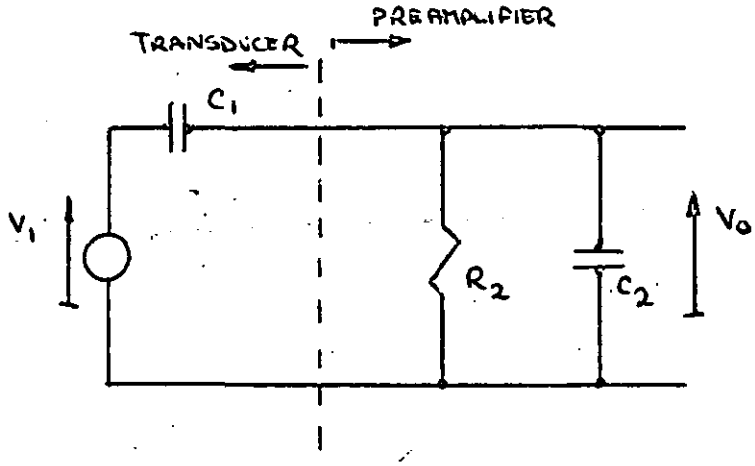


Fig. 5.2.1

Transducer:Preamplifier Input, Equivalent Circuit

These results are given in fig. 5.2.6. as a combined frequency response of the transducer with its preamplifier.

The device is mounted with its membrane above the required artery. As yet, the actual method of mounting has not been investigated.

Section 5.2

Transducer Pre-amplifier Design

With a piezo-electric transducer the signal is generated as a change in charge on a capacitor. Thus this has an equivalent circuit of a voltage generator in series with the device capacitance, the latter is generally quite small ($\simeq$ 1700 pf) and special input requirements are needed to avoid distortion at low frequencies.

If the output is fed into an amplifier, the input impedance of which is represented by the resistor R_2 in parallel with a capacitor C_2, as shown in fig. 5.2.1, then in terms of the Laplacian operator, the stage gain can be written as:-

$$V_o/V_1(p) = Z(p)/(Z(p)+1/pC_1)$$

Where $Z(p) = (R_2.1/pC_2)/(R_2 + 1/pC_2)$

$$\text{i.e. } V_o/V_1(p) = pC_1R_2/(1 + pR_2(C_1 + C_2)).$$

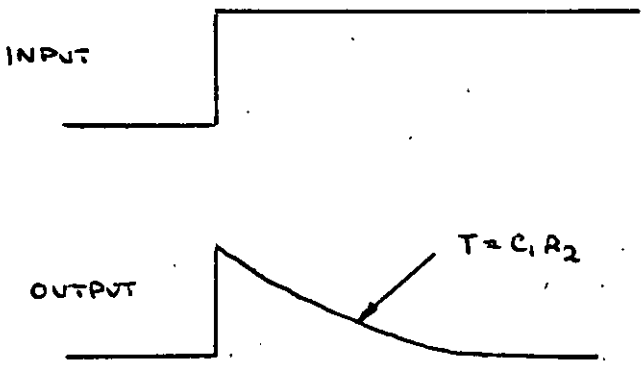


Fig. 5.2.2

Input:Output Relationship.

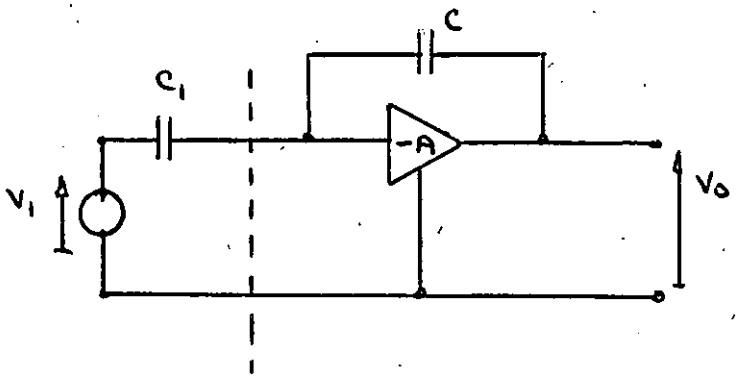


Fig. 5.2.3

Basic Charge Amplifier

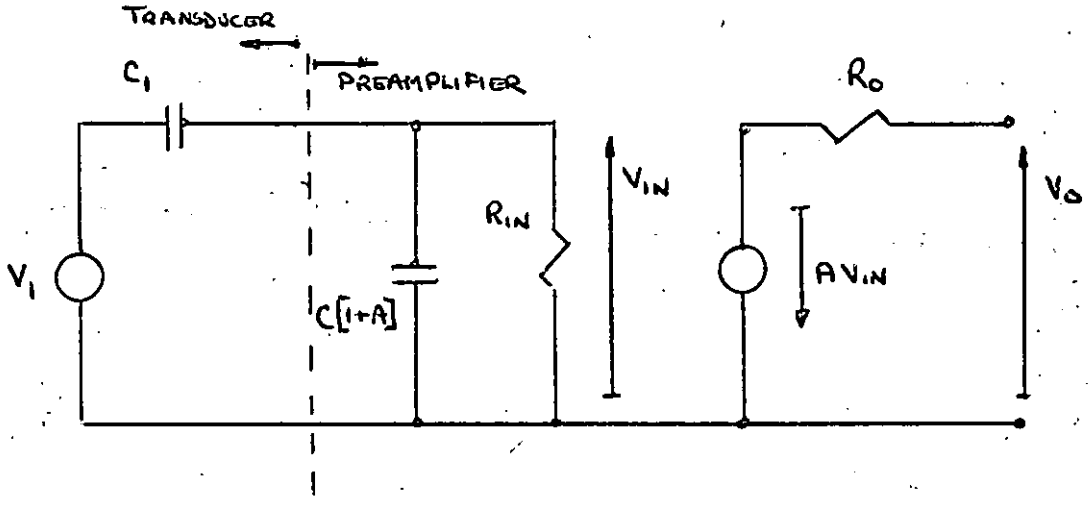


Fig. 5.2.4

Equivalent Circuit of fig. 5.2.3

Initially consider the system with $C_2 = 0$. If an input step of magnitude B is applied, the output becomes:-

$$V_o(p) = BC_1R_2/(1 + pC_1R_2)$$

i.e. $$V_o(t) = B \exp(-t/C_1R_2).$$

Thus the input step has been differentiated, and the discharge time constant is given by C_1R_2, as shown in fig. 5.2.2.

When C_2 is not zero, the output is given by:-

$$V_o(t) = \frac{BC_1 \exp(-t/(C_1 + C_2)R_2)}{(C_1 + C_2)}$$

Thus the signal has been attenuated by a factor $C_1/(C_1 + C_2)$, but the discharge time constant has been increased to $(C_1 + C_2)R_2$.

The criteria which dictates whether or not the signal is distorted is this coupling time constant, which Porje considers should be 2 to 3 seconds.

A practical method of producing a suitable input impedance is to patch an operational amplifier as a 'charge' amplifier as shown in fig. 5.2.3. To determine the input time constant the amplifier can be replaced by its equivalent circuit as shown in fig. 5.2.4, where R_{in}, R_o and A are the amplifier parameters. The final output V_o, on the application of the step input will be given by:-

$$V_o(t) = \frac{-ABC_1 \exp(-t/R_{IN}(C_1 + C(1 + A)))}{C_1 + C(1 + A)}$$

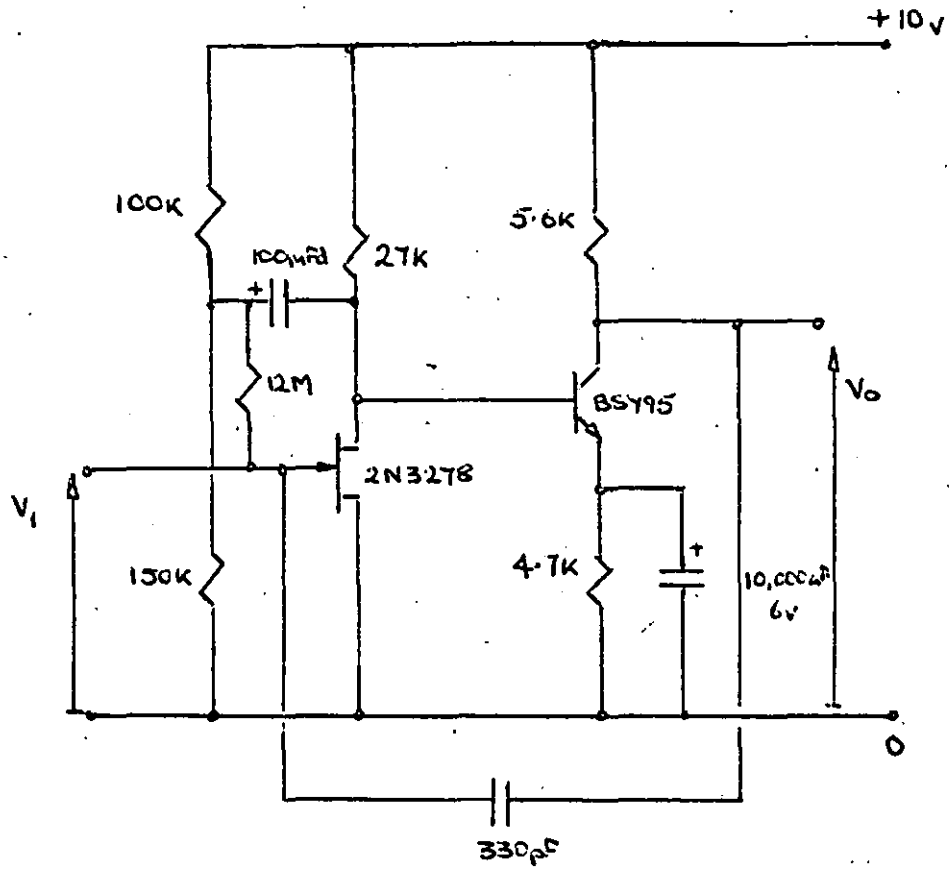


Fig. 5.2.5

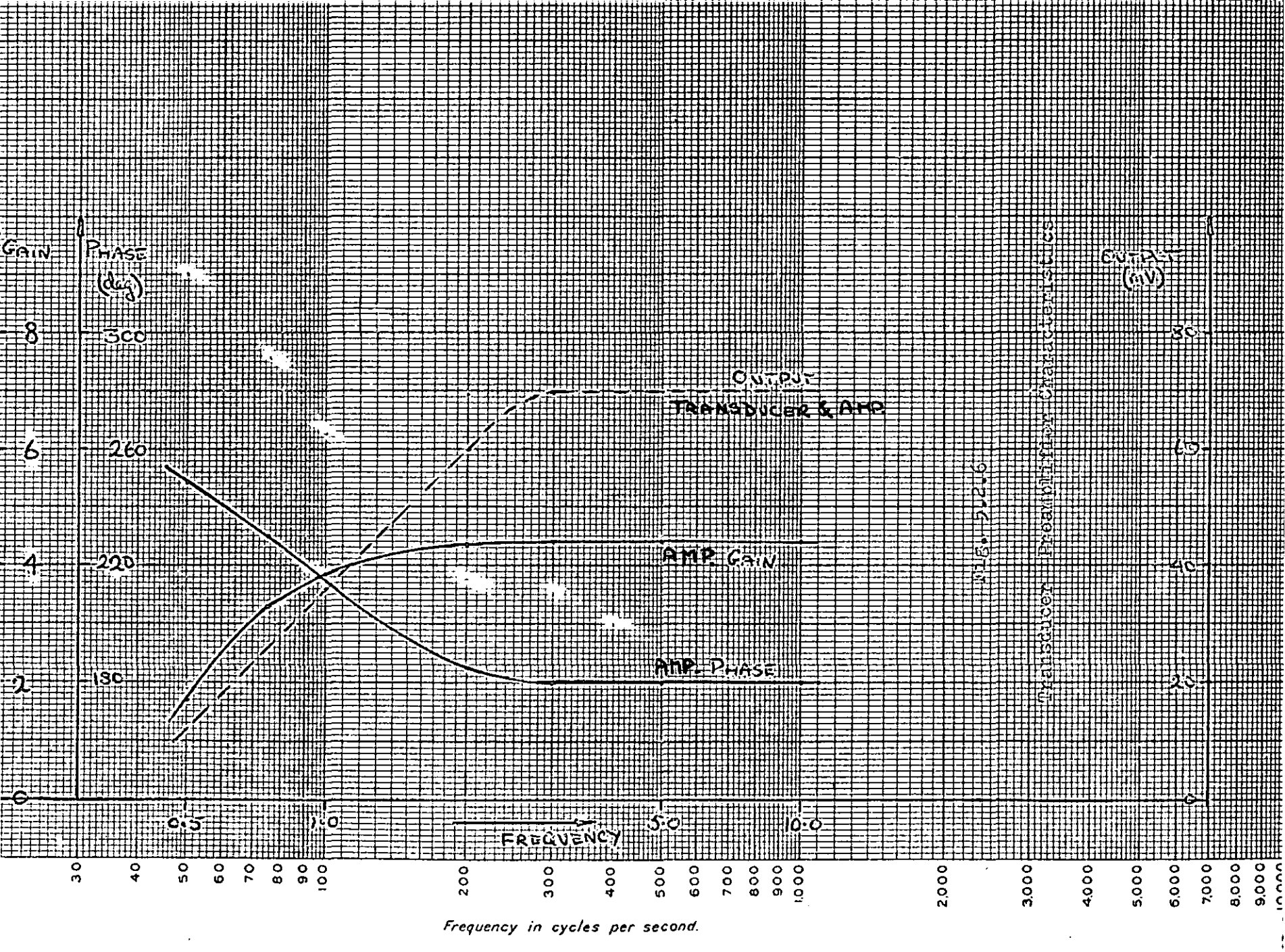
Actual Preamplifier Circuit.

Which is a gain of $-\left[\frac{C_1}{C_1/A + C}\right]$, and a coupling time constant of RIN $\left[C_1+C(1+A)\right]$.

If A is large $1/A \rightarrow 0$, and the gain becomes $-\frac{C_1}{C}$ with an infinite time constant.

In practice the amplifier used is shown in fig. 5.2.5, and consists of a bootstrapped field effect transistor acting as a source follower, followed by a high gain transistor amplifier. The feedback was applied via the 330 pF capacitor as shown.

Experimental results of the gain and phase relationships of the amplifier with frequency are shown in fig. 5.2.6.


GAIN
PHASE (deg)
8
6
4
2
0
350
260
220
180
OUTPUT TRANSDUCER & AMP
AMP. GAIN
AMP. PHASE
0.5
1.0
FREQUENCY
5.0
10.0
30
40
50
60
70
80
90
100
200
300
400
500
600
700
800
900
1000
2,000
3,000
4,000
5,000
6,000
7,000
8,000
9,000
10,000
OUTPUT (mV)
40
30
20
10
0
Frequency in cycles per second.

SECTION 6

Conclusions

This section concludes the work in this report. The performance of the system as described will be discussed and also any modifications which are now necessary will be included. Correspondingly the section will be divided into three parts, namely the computer, the simulator, and future work.

Section 6.1

The Computer

The computer itself consists of five main units:- the transducers and their preamplifiers; the gain control system; the delay measuring system; the division system and the output display facilities. It has been designed so that any one of the five units may be replaced by another unit, which performs the same task as the original , in any manner available, without preventing the overall system from functioning. This is because the transfer signal from one unit to the next is either an analogue signal representing the pulse wave or an analogue voltage.

For example, the delay measuring system receives an analogue signal of the pulse waves and translates this into an analogue voltage equivalent to the delay. The manner in which this task is performed, is immaterial to the rest of the computer provided that the accuracy is similar. The mechanical construction completes this theme, in that, each unit is self contained on

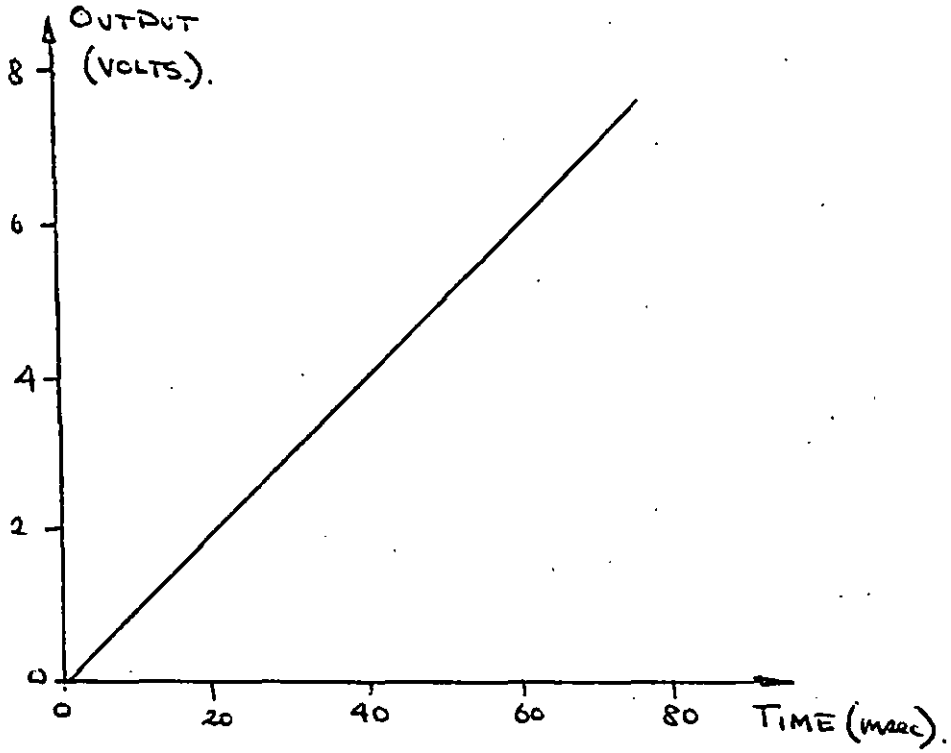


Fig. 6.1.1

Output:Delay, for the Delay Measuring System.

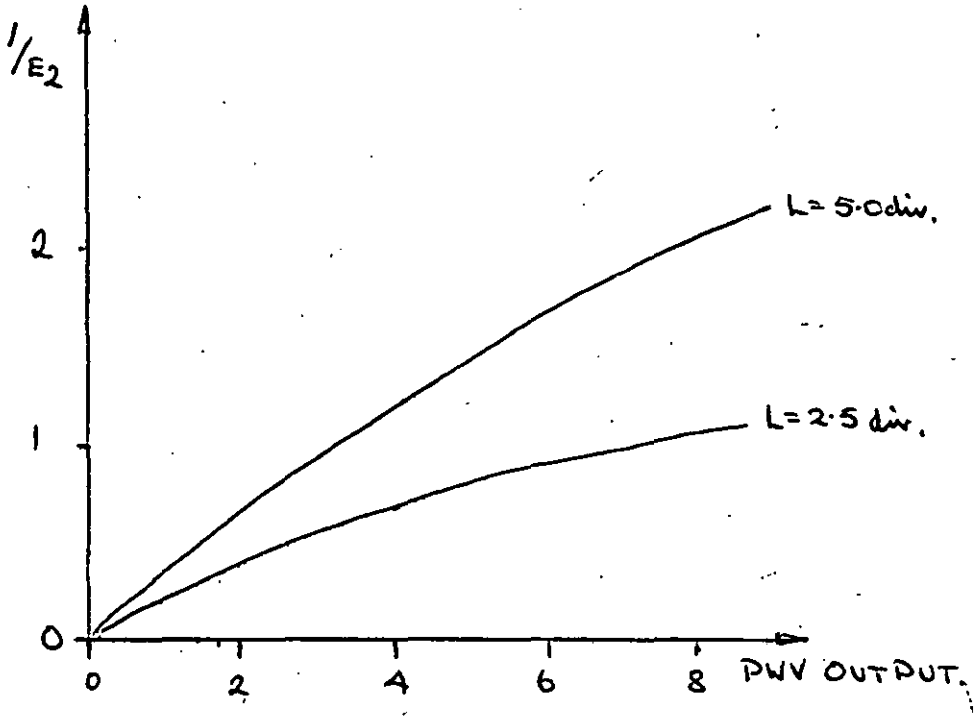


Fig. 6.1.2

Analogue Divider Response.

1-3 plug-in boards and thus if modifications to the system are intended, then they can be carried out by making a new plug-in board and merely exchanging it for the present one.

The completed system has been run successfully, using the simulator as a signal source, but without the gain control amplifiers. The operation in this form was reasonably stable, although from time to time it did tend to 'miss a beat', but this was due to the absence of the gain control system. Tests have been performed on the delay measuring system and also the analogue divider system.

For the delay measurement, the variable delay facility on the Simulator was calibrated using an oscilloscope. A graph relating the delay to the system output is shown in fig. 6.1.1., and as can be seen it is a reasonably linear function, as expected. Obviously, the function will not be purely linear due to the variable integrating time obtained by testing the system in this way. Compensation should actually be made for this factor. No attempt has been made to tie the accuracy down at present, since the measurement technique could have errors of ± 5%. For an accurate set of results the delay period must be measured on a digital frequency meter, and compensation for this period must be allowed for in the steady state dc output.

Two curves for the analogue division system appear in fig. 6.1.2, and they are not linear, as required. This is to be expected since the integrator in the system is patched to a gain

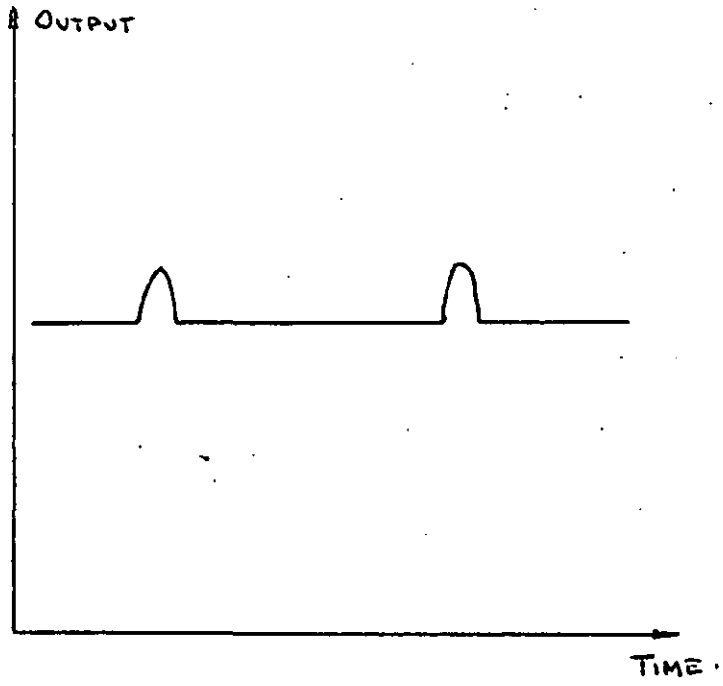


Fig. 6.1.3

Typical Output from Computer

of 50,000 but the specification of the open loop gain is only greater than 1,000. Thus the integrator obeys an exponential law, as indicated by the results. The large gain required, is due to the high repetition frequency, 7 kc/sec, necessary for the correct operation of a system of this kind.

The solution is to use a commercial operational amplifier with an open loop gain of greater than, 5.10^6, for a 1% accuracy. If this is intended it would be reasonable to replace also the operational amplifier in the delay measuring system.

The display system is a voltmeter and thus apart from possible zero errors, its operation is linear as demonstrated by fig. 4.9.4., in Section 4. A typical voltage output signal is shown in fig. 6.1.3, and as can be seen a small 'blip' occurs when the integrator in the delay measuring system is set to earth. The meter shows this clearly, due to the low frequency nature of the signal.

The transducer has been described briefly, but in sufficient detail to show that a piezo-electric device is not suited to measurements at low repetition frequencies. It has the advantage of responding only to transient pressure, but a special preamplifier is required.

The ideal type of transducer is one in which the output appears as the modulation on a carrier signal. In this form the low frequency signal can be handled easily.

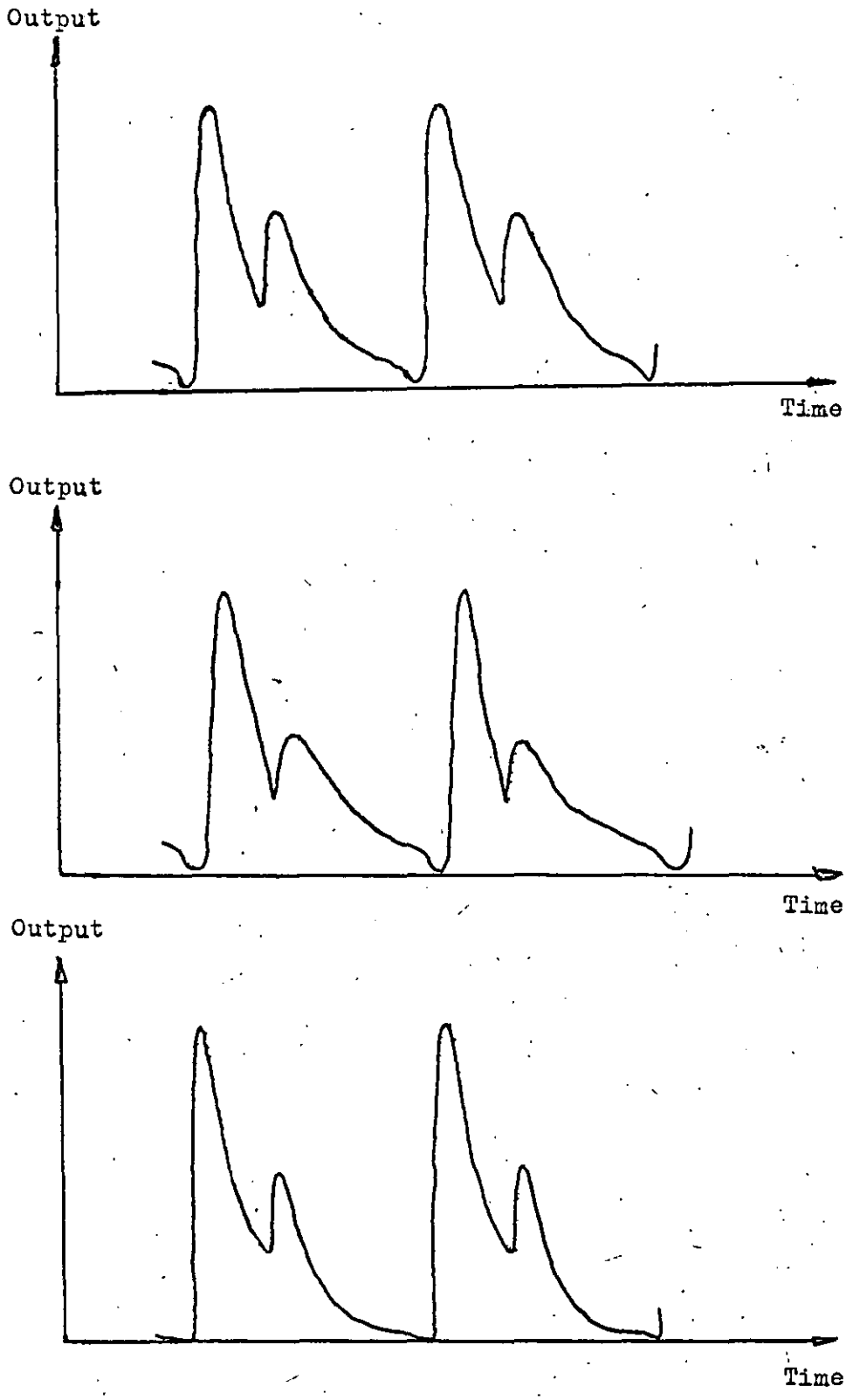
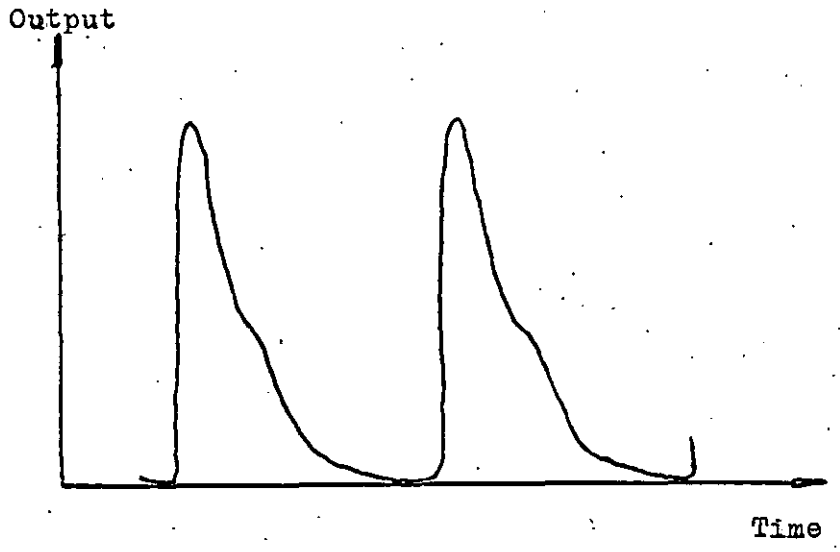


Fig. 6.2.1.

Typical Simulated Pulse Waves



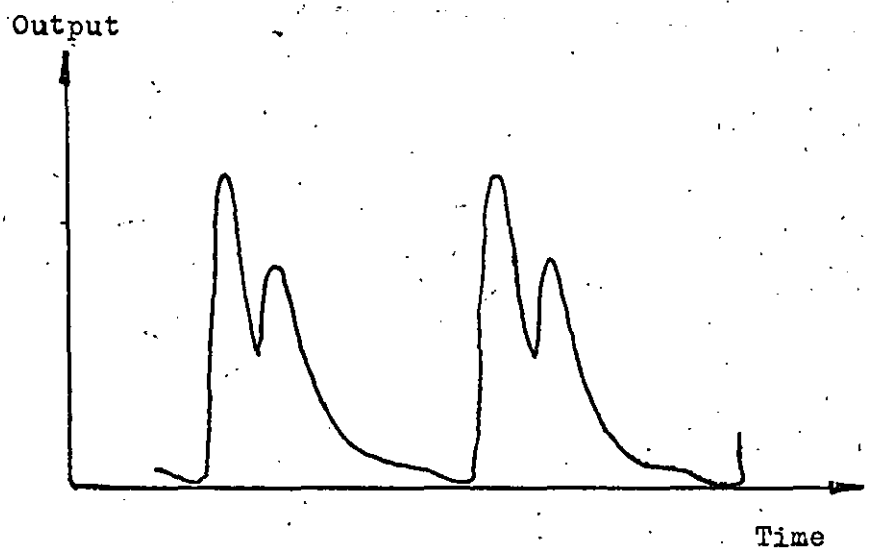
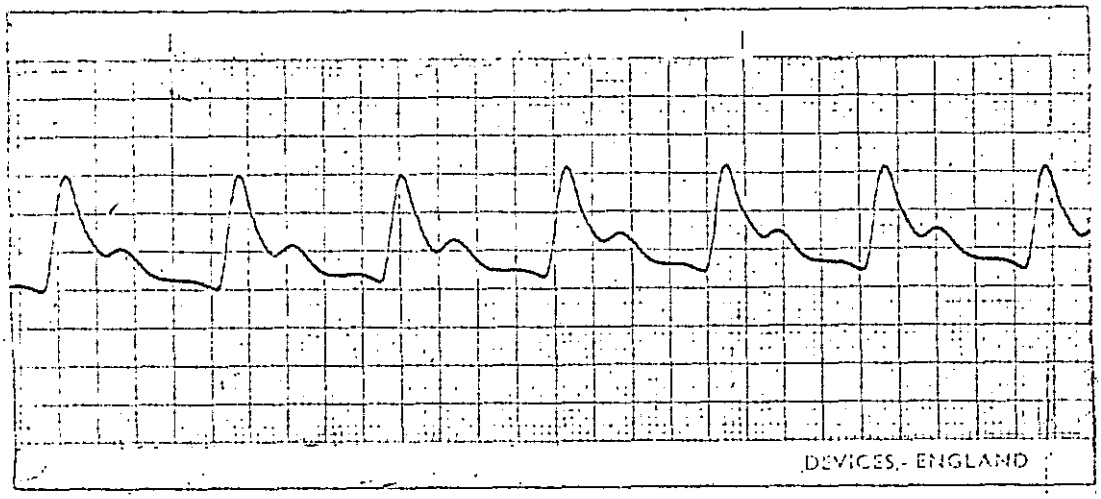
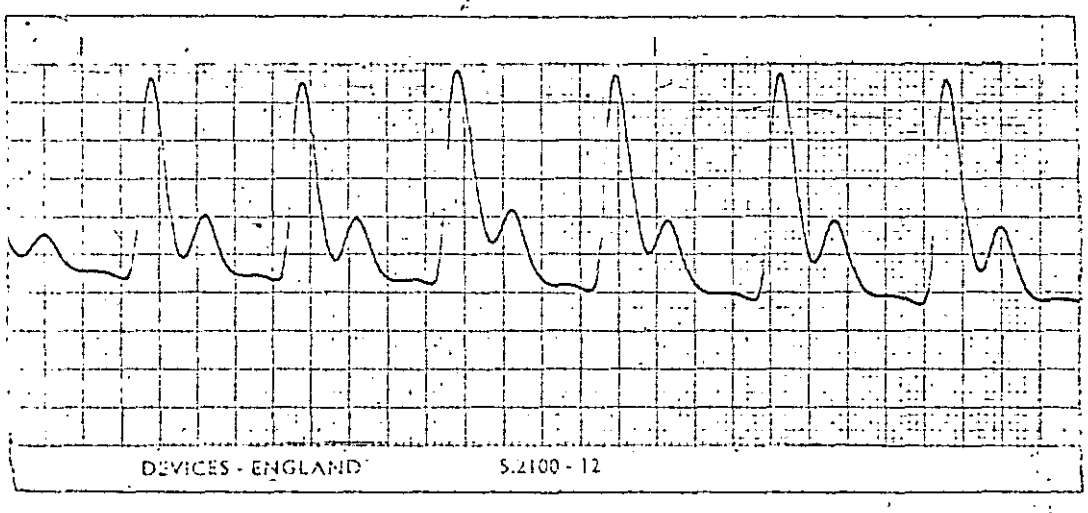


Fig. 6.2.1 (cont'd)

Typical Simulated Pulse Waves





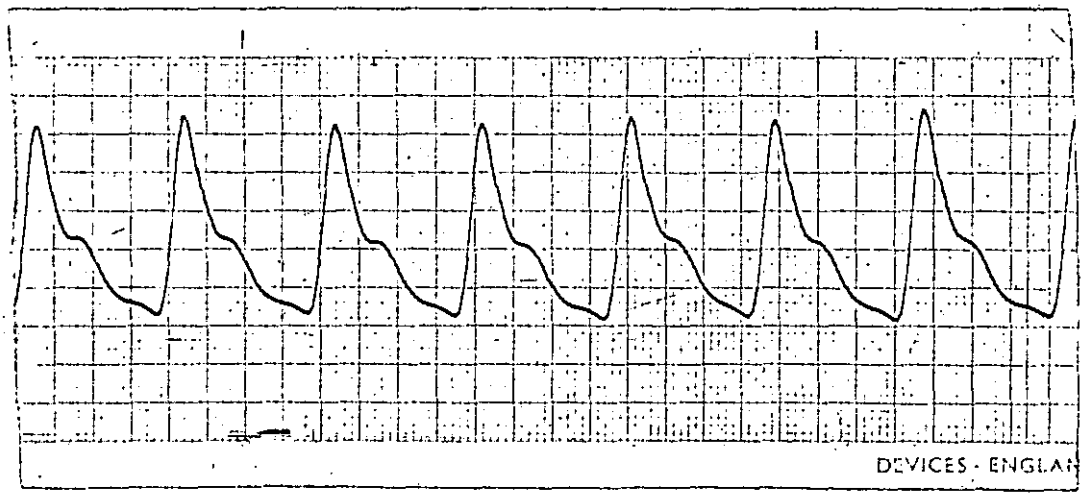


Fig. 6.2.2 Actual Pulse Waves

Also the 'noise immunity' can be improved by using a preamplifier with a differential input. Common mode noise, which is always present where a transducer is in contact with the body surface, can then be rejected.

A suitable transducer element is manufactured by Associated Electrical Engineering Ltd. type no. P.40. It is a variable reluctance device and is physically extremely small.

Section 6.2

The Simulator

The Simulator has been adequately described in Section 3, and its design has produced a versatile signal generator. Typical output waveforms are given in fig. 6.2.1, and some actual pulse wave recordings, supplied by H.S. Wolff (M.R.C.), are given in fig. 6.2.2, for comparison purposes. As can be see the simulated signals have a fair resemblance to their real counterparts.

In an attempt to test this more scientifically, certain real pulse waves were traced onto a piece of clear perspex. This was then mounted against the tube of an oscilloscope

No	1 A	1 S	2 A	2 S	3 A	3 S	4 A	4 S
MEAN	32	31	39	36	42	42	34	33
a_1	6	2	-11	-8	-11	-9	0	-1
b_1	35	38	26	26	30	26	29	29
a_2	-15	-13	-8	-7	-5	-6	-14	-13
b_2	19	13	15	14	20	19	22	20
a_3	-15	-13	-8	-7	-5	-6	-14	-13
b_3	-1	2	-4	-1	1	0	-3	-3

A= Actual Waveform.

S= Simulated Waveform.

Fig. 6.2.3.

Harmonic Analysis of the Pulse Waves.

displaying the simulated waveforms. With the aid of the variables provided, the two waveforms were matched, to a first order approximation. An Ultra Violet recording of the simulated signal was made and a Fourier analysis of the two waveforms was performed. (See Appendix E).

The results of such analyses appear in fig. 6.2.3. as can be seen the harmonic content of the real and simulated waveforms agree well; thus indicating that the simulated pulse waves have a similar harmonic content to the real signals.

In addition inspection of the figures show that the wave contains fundamental, second and third harmonics, of which the fundamental is the predominant oscillation. Also the second and third harmonics are of decreasing magnitudes. These conclusions are also given by Porjé (11), and he extends this by stating that the wave is composed, almost exclusively, of the fundamental, second and third harmonics.

Section 6.3.

Future Work

Dealing first with possible modifications to the present system. In the delay measuring system, the production of the integrator input signal is shown in fig. 6.3.1. the short pulses from gates 1 and 2 are used to trigger pulse generators 2 and 3, from their rear edges, The outputs of these pulse

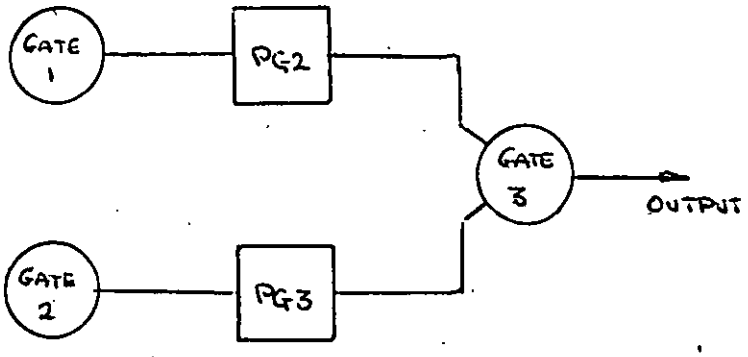


Fig.6.3.1

Present System

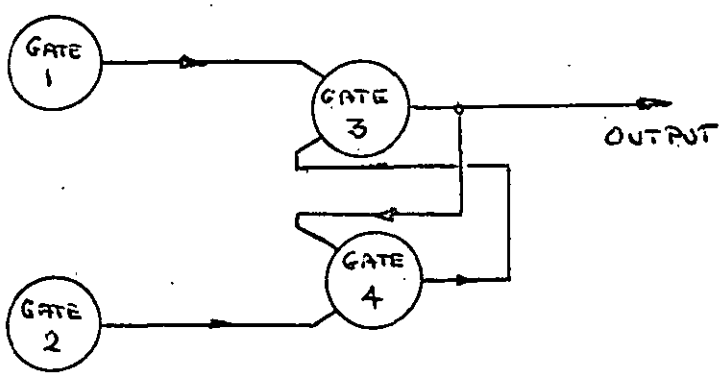


Fig. 6.3.2

Suggested Modification

generators are then passed into gate 3, used to generate the integrator input pulse.

This system has the physical limitation in that a delay, greater than (200 msec) the generator pulse length, cannot be measured, and also it is a rather clumsy method to use. The modified system, shown in fig. 6.3.2, replaces both pulse generators and gate 3, by a bistable composed of two gates connected back to back as shown. The rear edges of the pulses are now used to set, and reset the bistable, thus performing the desired task.

Additional modifications are the use of higher gain operational amplifiers as discussed previously.

Because of the task the system is required to perform, a rather unique method of delay measurement has been used. The definition of a system of this kind is limited, theoretically, to the regulation achieved by the gain control stages. This regulation is also found to be a direct function of the open loop gain of the agc system, and thus increased loop gain will give better regulation and a greater definition would then be possible. But there must be a practical limitation to the definition available, possible temperature fluctuations, and thus other methods of delay measurement should still be considered in parallel with the present technique.

A method that offers certain possibilities is that of a null-detector kind. Consider the system shown in fig. 6.3.3. A delayed version of the first channel signal is fed into a

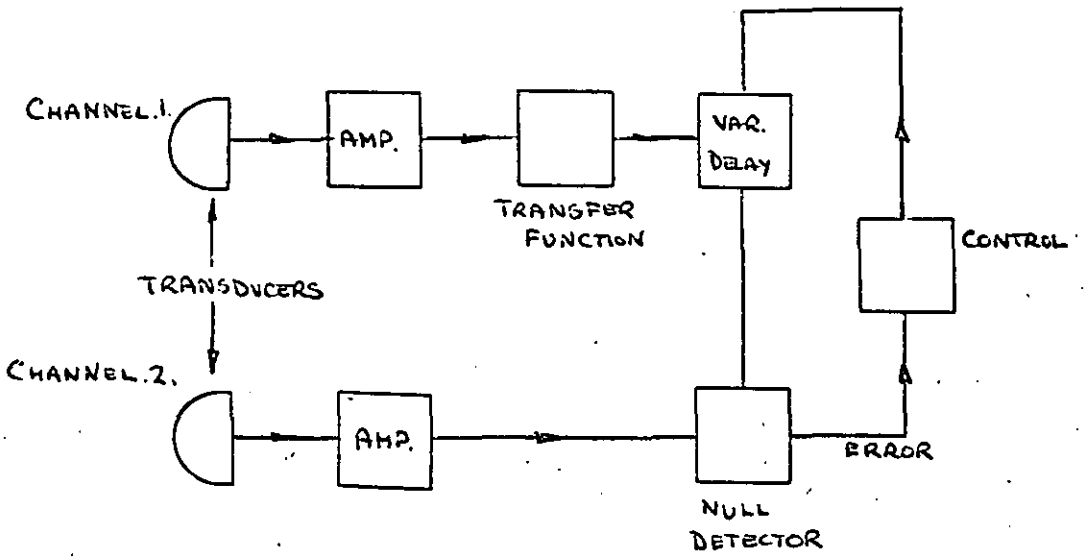


Fig. 6.3.3

Null Detector Method of Delay Measurement

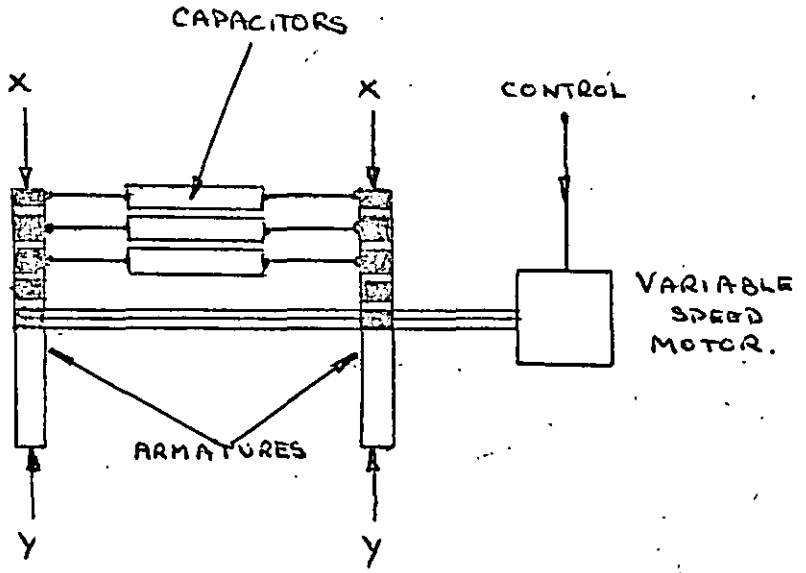


Fig. 6.3.4

Variable Delay Stage

null detector with that from the second channel. From this detector an error signal is derived, and fed back to the delay stage. Provided the null-condition is maintained the delay can be read directly, from the delay stage.

This system has a useful addition in that a longer length of artery can be considered. One need no longer assume that the transfer function is unity; for a true transfer function can be included in the first channel to compensate for that inherant in the second.

The null detector will be some form of a differential amplifier, and the variable delay stage could be manufactured in several ways. Two techniques used in analogue computing are the use of a magnetic recording loop coupled to a variable speed motor, or the use of a rotating bank of capacitors. That is two armatures with capacitors connected across them as shown in fig. 6.3.4. The signal is applied via the brushes at x-x, and the delayed output is taken from the brushes at Y-Y. Again the device is coupled to a variable speed motor, to which the control is applied. An interesting point to note, in this case, is that the motor speed will be directly proportional to the pulse wave velocity, and thus a tachometer could be used to display the output.

A purely electrical system performing the same function would be extremely complex in nature. However the difficulties in the above system would arise in the actual way in which the null detector functioned.

Other useful information could be generated by the computer. Heart rate is a function easily obtainable, it could be generated by using a diode pump with the input derived from the pulses on either channel. Also an audio monitor could be attached if required.

Finally when the transducers and gain control system are functioning, correctly, the computer should be used to record the PWV's of various subjects and the results obtained should be compared with those of previous authors.

SECTION 7

APPENDICES

Appendix A

Computer Construction & Circuit Diagrams

The computer (and simulator) construction is in a modular form using plug-in boards. The chassis and boards are standard Lektrokit components. The boards are fitted with a 10 way plug and the mating sockets are mounted in the chassis. This construction can be clearly seen in the photographs of the simulator and its plug-boards shown in fig. A.1. Note in particular the communal heat sink used with the operational amplifier, to obtain better thermal stability.

The board layout in the computer box, as viewed from the underside, is shown in fig. A.2. The circuit diagrams of the various boards are given in figures numbered A3 to A8, and a list of their tabulated pin connections appears at the end of this section.

The circuit diagram for the operational amplifier is given in fig. A.9, and the setting up procedure for the amplifier is as follows. Set the input approximately to earth using VR1. Then with VR2, balance the transistors in the first pair, by setting an equal dc level on both transistor collectors. Now with VR3, balance the transistors in the second pair in a similar manner, and set the output approximately to earth with VR4. Finally set the earth input and output accurately using VR1 and VR4.

The 'Set L' analogue voltage generator is shown in fig. A.10, and the output meter and its associated multiplier resistors is shown in fig. A.11.

Boards numbered 1 and 2, relating to the Agc system were not finalised and hence no data is given for these. All boards have pin 1 to +10 volts, pin 2 to -10 volts and pin 3 connected to earth.

Board No. 3.

4	Smoothing Capacitor Connection, +10v supply.
5	Smoothing Capacitor Connection, -10v supply.
7)	25v ac input to + 10v supply
8)	
9)	25 v acinput to -10v supply.
10)	

Board No. 4

4	Channel 1.	Input.
5	Channel 2.	Input
6	Channel 2.	Trigger point.
7	Channel 1.	Output
8	Channel 2.	Output
9	Channel 1.	Trigger point.
10	Channel 2.	Inverse output.

Board No. 5

4	Channel 1.	Input
5	Channel 2.	Input
6	Channel 2.	Inverse input

9	Integrator reset output.
10	Output to Integrator Input.

Board No. 6.

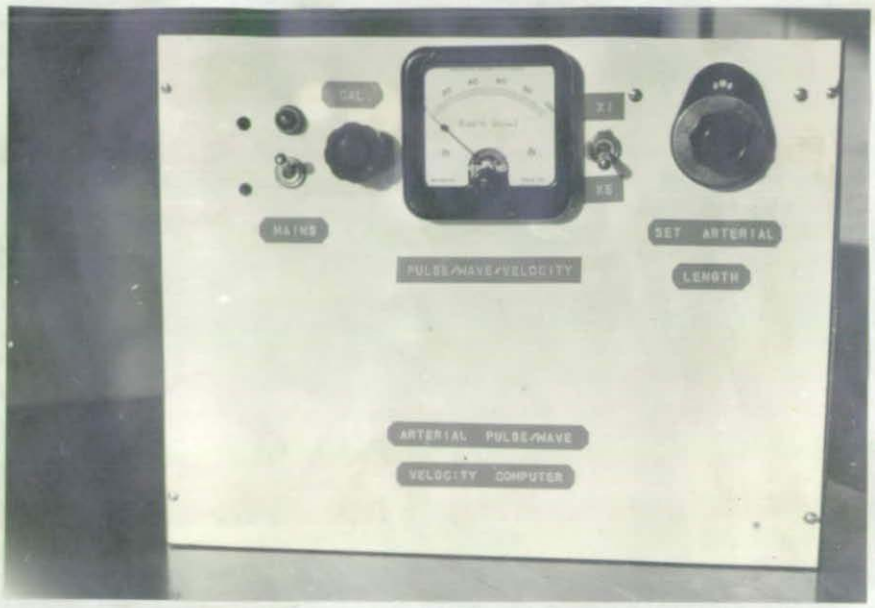
7	Integrator Output
9	Input to reset circuit.
10	Input to Integrator.

Board No. 7.

4	Input to Integrator
5	Integrator summing junction point.
6	Integrator output.
9	Input to Reset Circuit.

Board No. 8

4	'Set L' Analogue voltage input.
5	Input to Schmitt Trigger.
6	Analogue Output.
9	Integrator reset output.



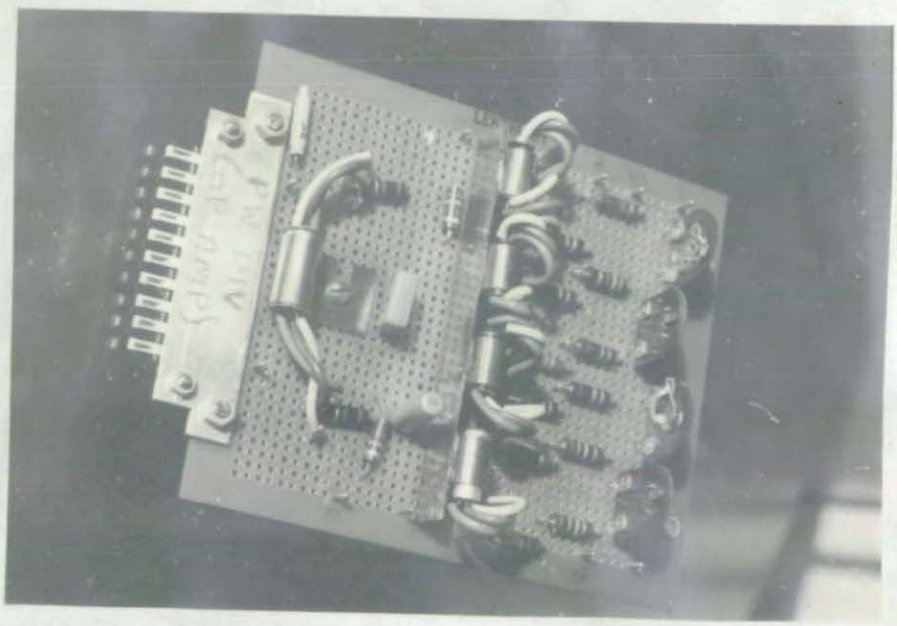


Fig. A.1.

Computer Construction.

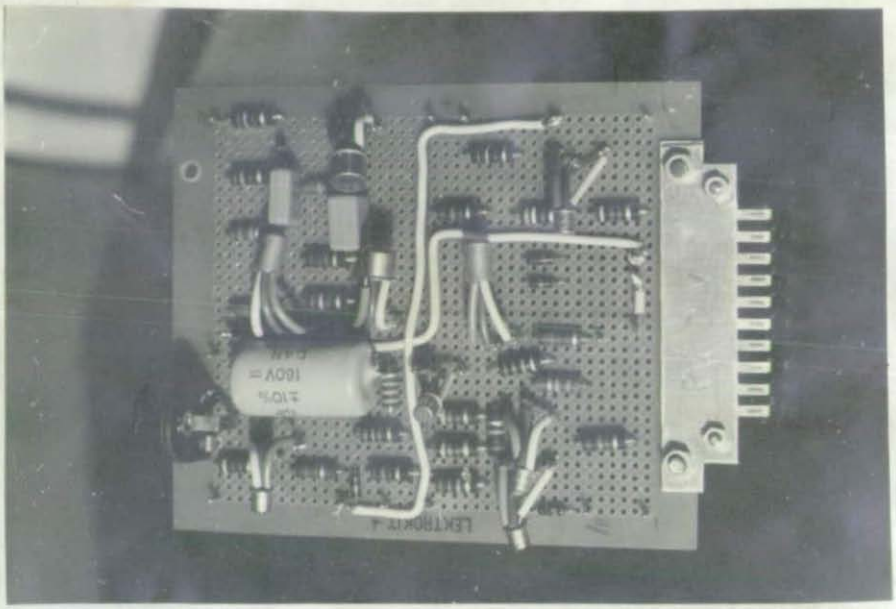
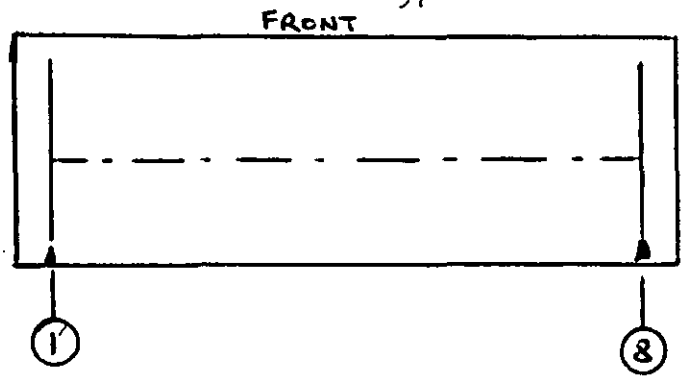


Fig. A.1. (cont'd)

Computer Construction.



Board No.	Function
1, 2	Age System and phase correcting amplifiers
3	Power Supplies
4	Delay Measurement. The exponential amplifiers, differentiators, and trigger circuits.
5	Delay Measurement. Various circuits to produce the Integrator reset and input signals.
6	Delay Measurement. Integrator and reset gate.
7	Analogue Division. Integrator and reset gate.
8	Analogue Division. The Schmitt trigger, master generator, filter and various gates.

Fig. A.2.

Computer Rack Schedule

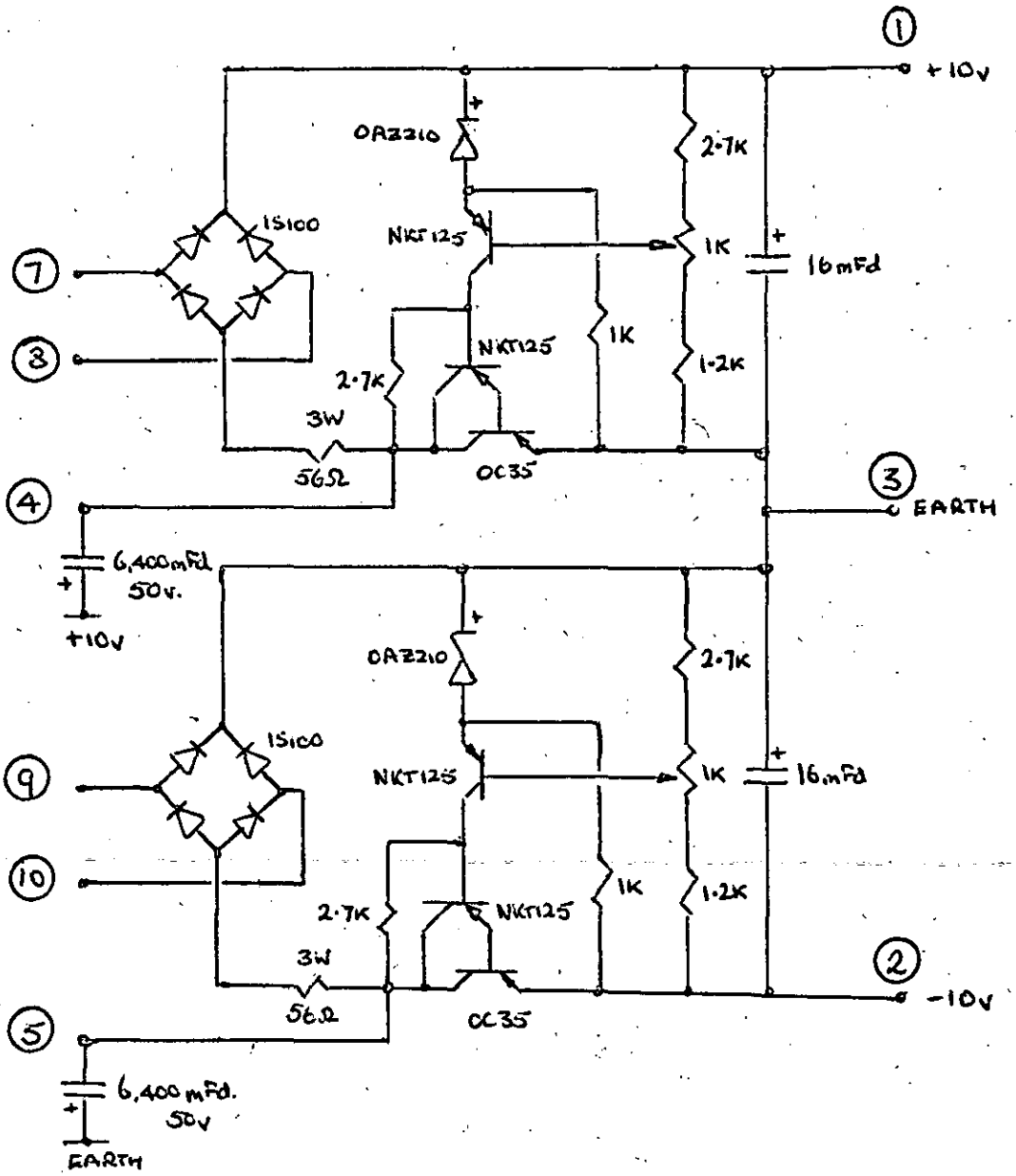
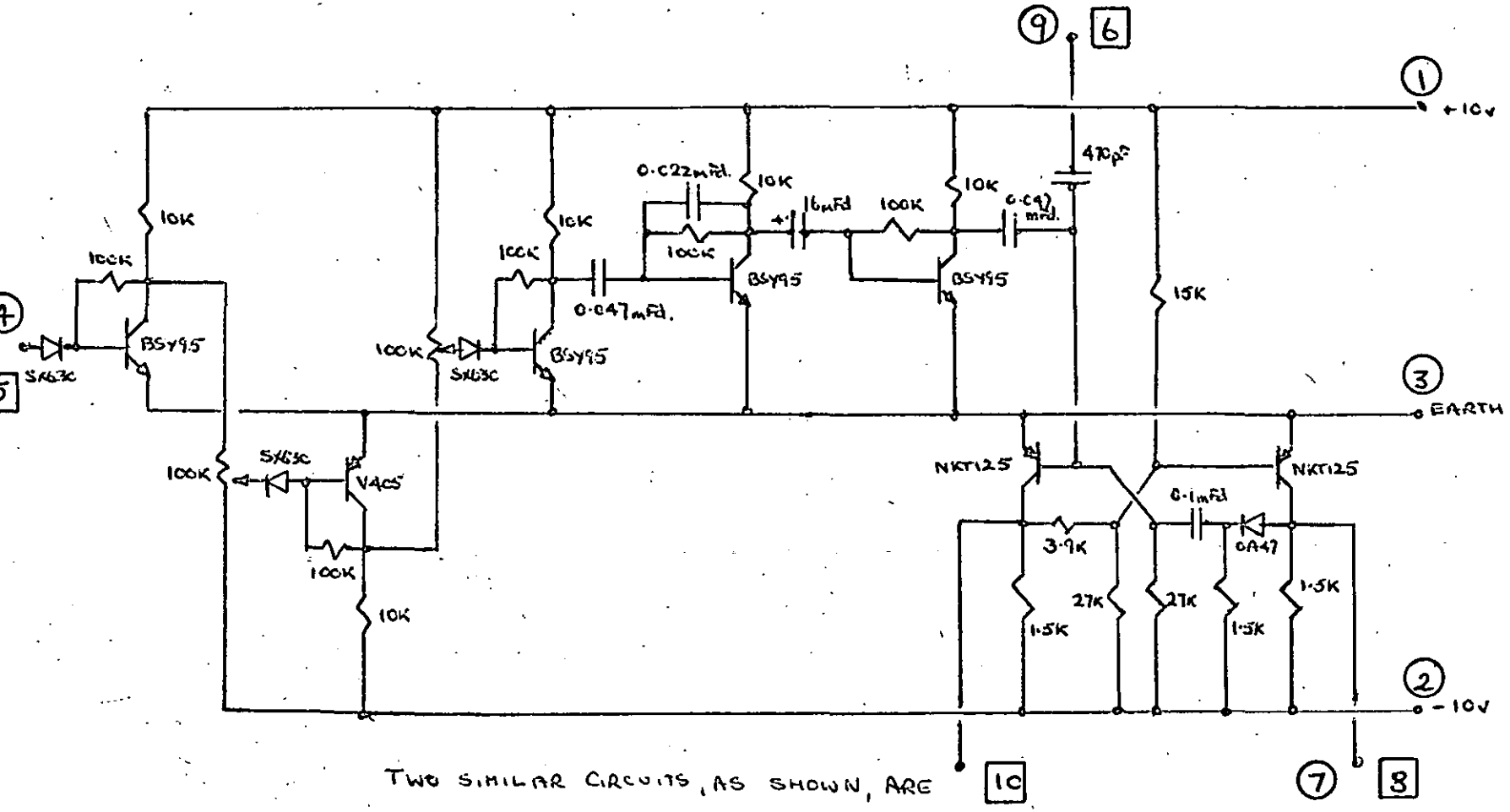


Fig. A.3.

Circuit Diagram, Board 3.



TWO SIMILAR CIRCUITS, AS SHOWN, ARE MOUNTED ON THIS BOARD.

FIG. A.4.

CIRCUIT DIAGRAM, BOARD 4.

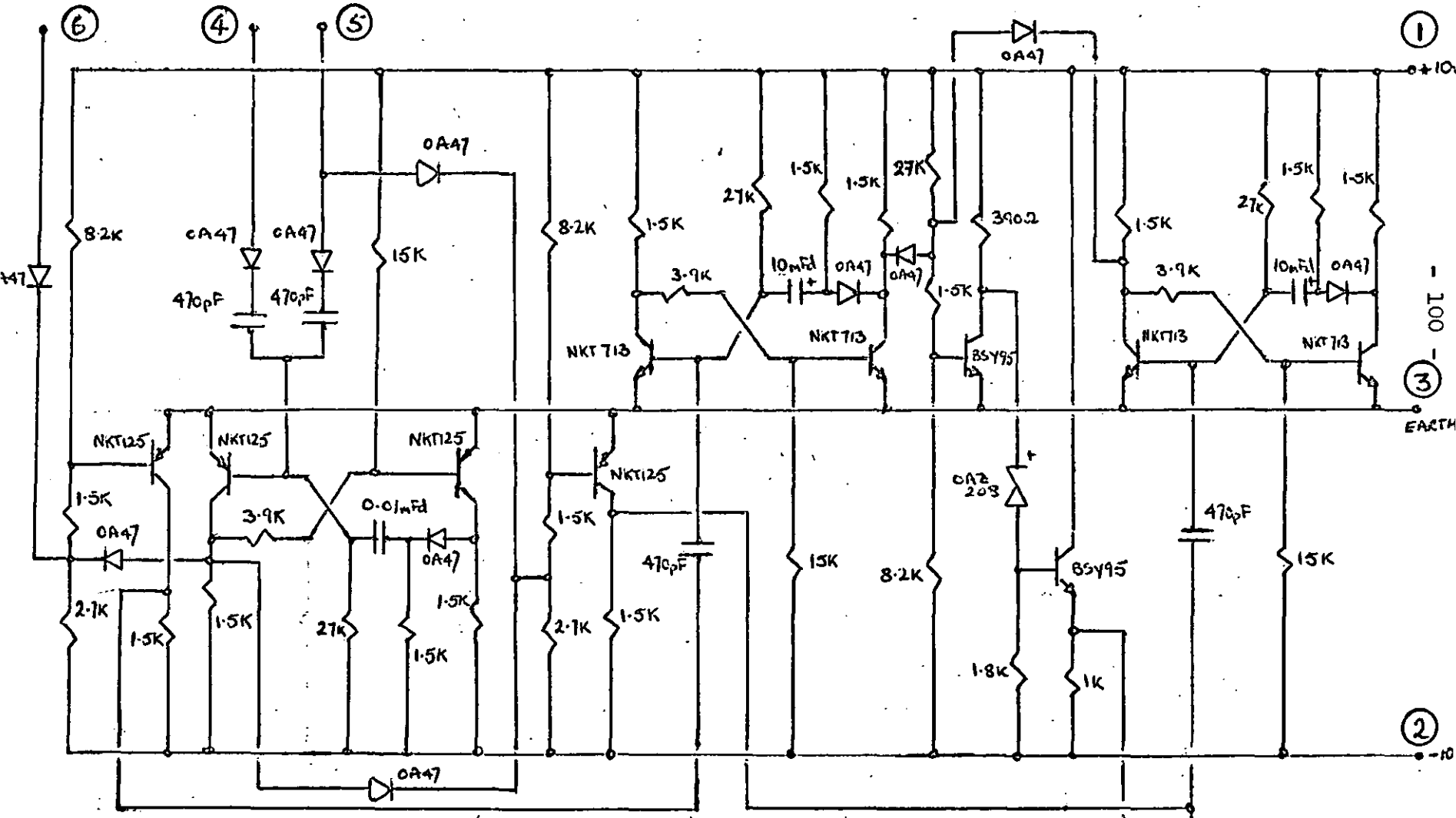


Fig. A.5.

Circuit Diagram, Board 5.

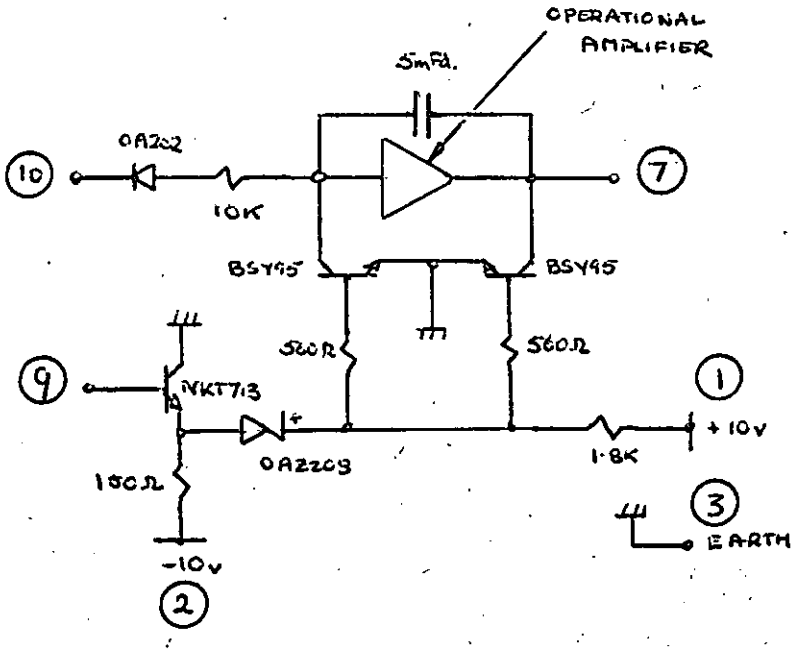


Fig. A.6

Circuit Diagram Board 6

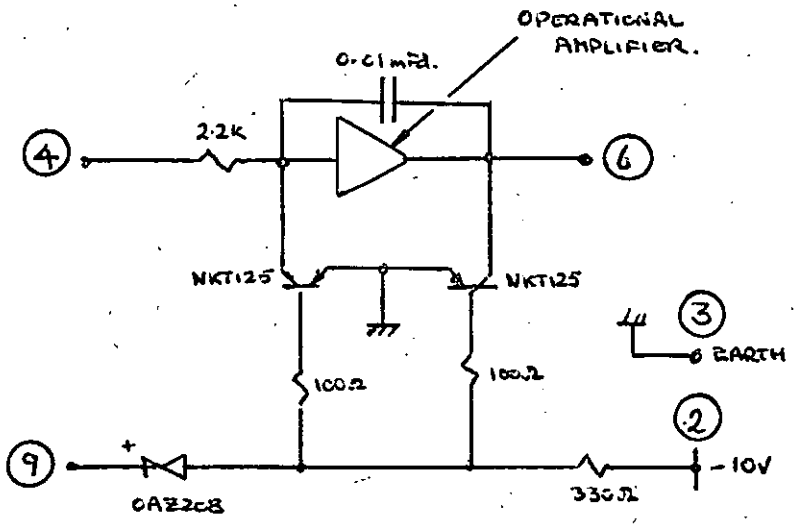


Fig. A.7

Circuit Diagram Board 7

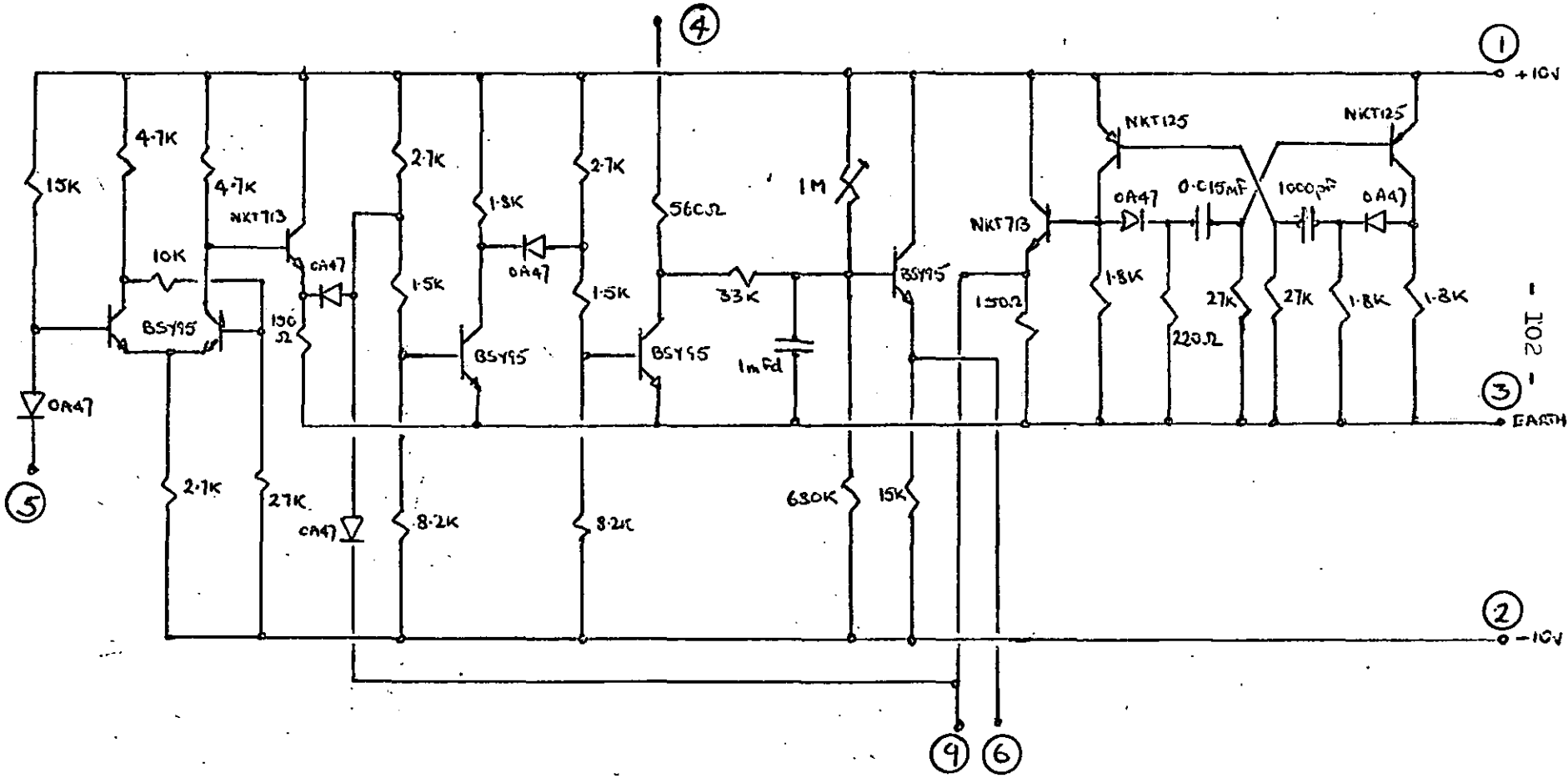


Fig. A.8.

Circuit Diagram, Board 8.

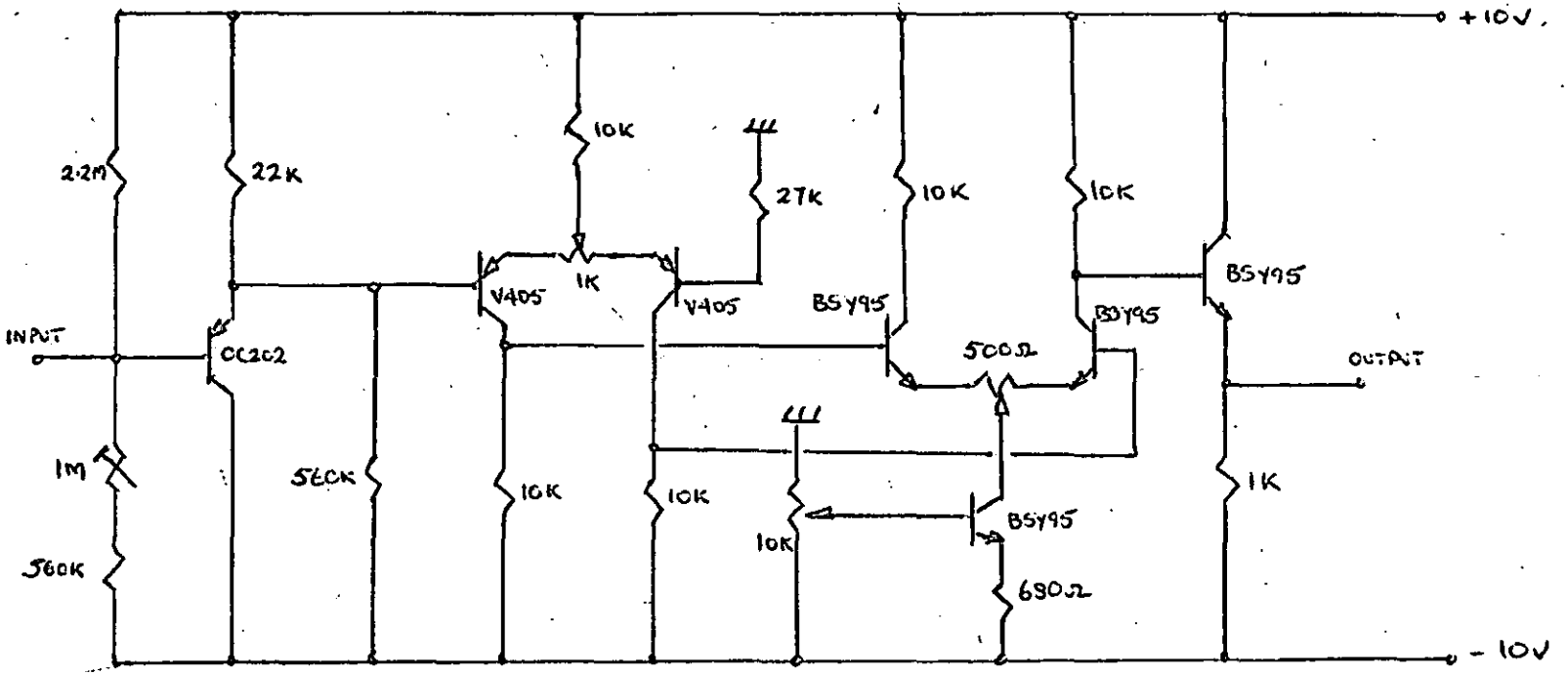


FIG. A.9.

OPERATIONAL AMPLIFIER.

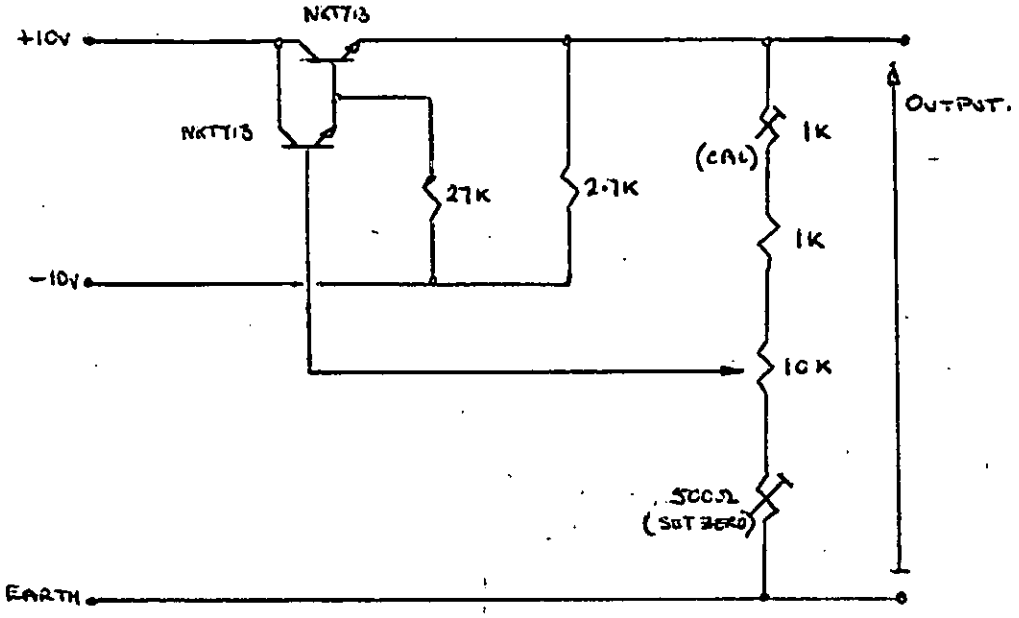


Fig. A.10.

Set 'L' Analogue Voltage Generator

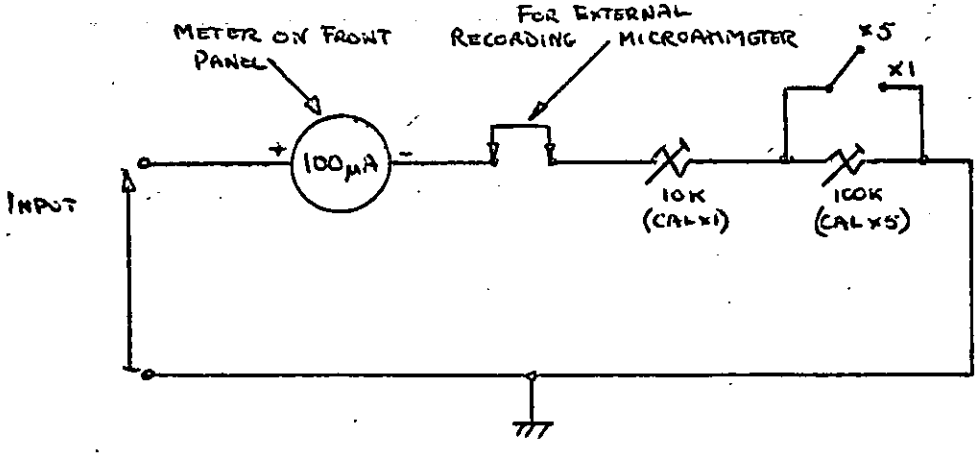


Fig. A.11.

Output Display System

Appendix B

Simulator Construction and Circuit Diagrams

The simulator construction is of a similar modular form to that of the computer, and is shown in the photographs in fig. B.1. The majority of the variables are skeleton potentiometers, which are mounted on the rear of the boards. Three variables, namely, the delay between the two channels and the amplitude controls for each channel are mounted on the front panel.

The board layout is shown in fig. B.2, as viewed from the rear. The circuit diagrams of the various boards are given in figures B3 to B5, and their various pin connections are listed at the end of this section. Note that the power supply board is identical to thatused in the computer, and its circuit can be found in Appendix A, also the boards numbered 2 and 4 are identical.

All boards have pin 1 +10 volts, pin 2 -10 volts and pin 3 earth.

Board No. 1

4 Shaped output (ID)

5 Switch drive (IL)

6 Switch drive (IM)

7 Master output (IA)

8 Oscilloscope trigger/Unshaped output channel 1 (1A)

Board No. 2

4	Trigger Input (1A)
5	Shaped Input (1D)
6	Connection to output amplitude potentiometer.
7	Switch drive input (IL)
8	Switch drive input (IM)

Board No. 3

4	Trigger Input (1A)
5	Shaped Output (2D)
6	Master output (2A)
7	Switch drive (2L)
8	Switch drive (2M)
9	Connection to delay 1/2 potentiometer.
10	Unshaped output, channel 2. (2A).

Board No. 4

4	Trigger Input (2A)
5	Shaped Input (2D)
6	Connection to output amplitude potentiometer.
7	Switch drive input (2L)
8	Switch drive input (2M).

Output Socket Connections

1	Unshaped output channel 2 (2A)
2	Oscilloscope Trigger output. (1A)
3	Channel 1. Output (10)
4	Unshaped output channel 1. (1A)
5	Channel 2. Output. (20)
6	Earth

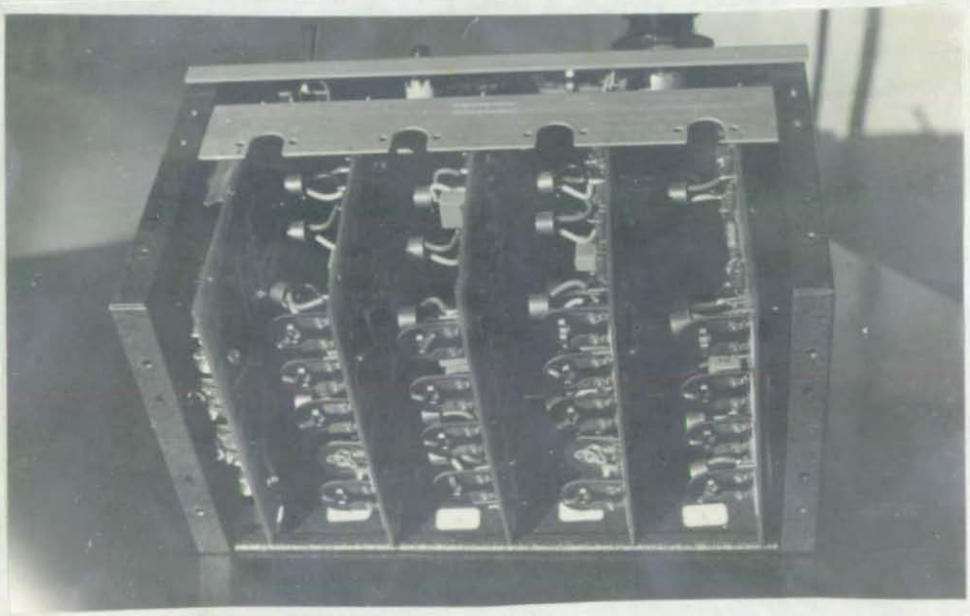
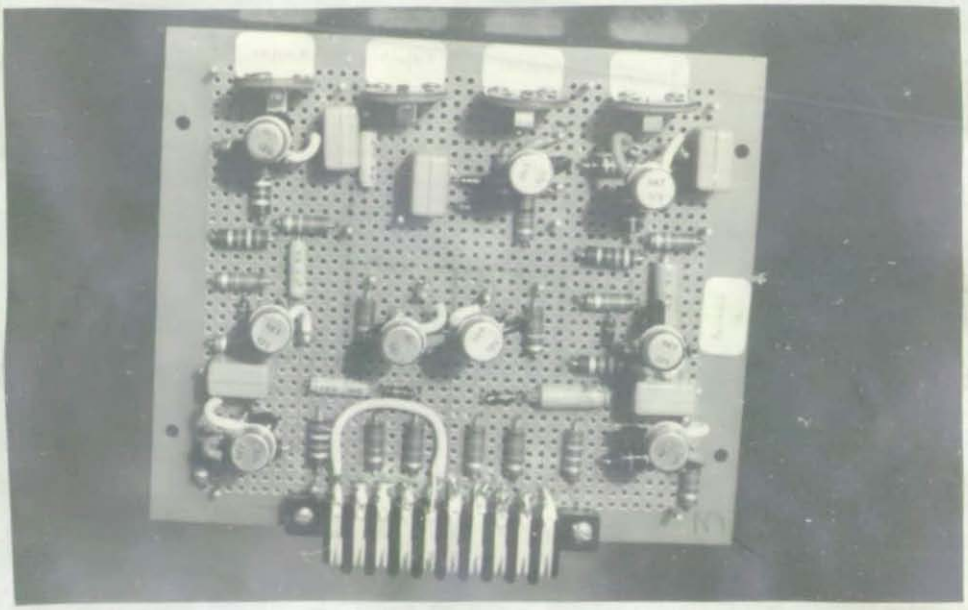


Fig. B.1.

Simulator Construction.



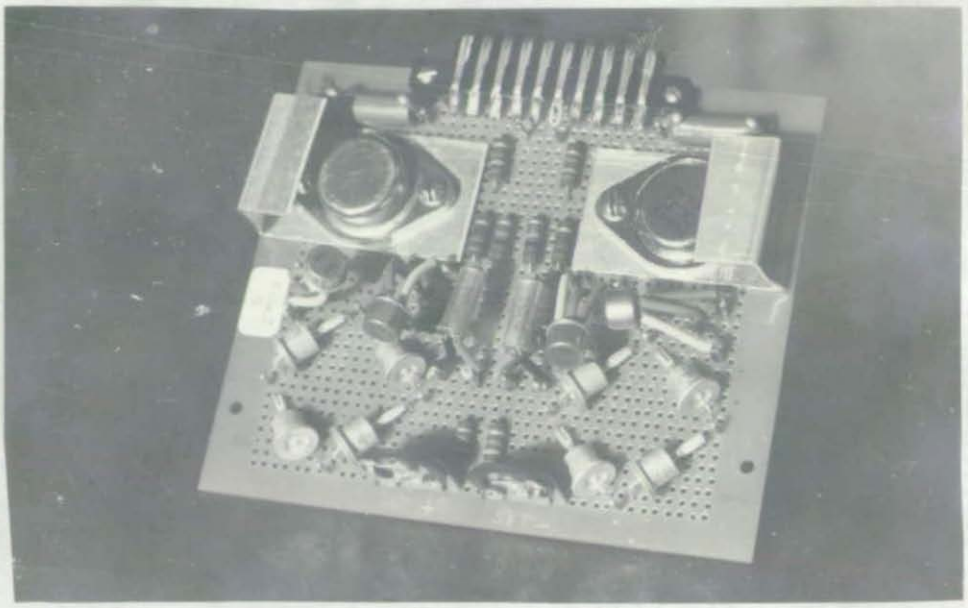
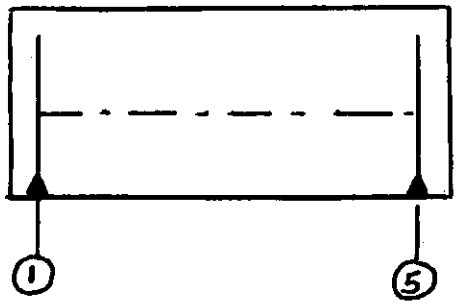


Fig. B.1. (cont'd)

Simulator Construction.



Board No.	Function
1	Channel 1. Master generator, switch delay generator, switch generator and shaping circuit for part A.
2	Channel 1. Delay A/B generator, slave generator, shaping circuit for Part B Analogue gate and output drive circuit.
3	Channel 2. As for channel 1 board No. 1 with the addition of the delay 1/2 generator.
4	Channel 2. As for channel 1, board No. 2.
5	Power Supplies

Fig. B.2.

Simulator Rack Schedule

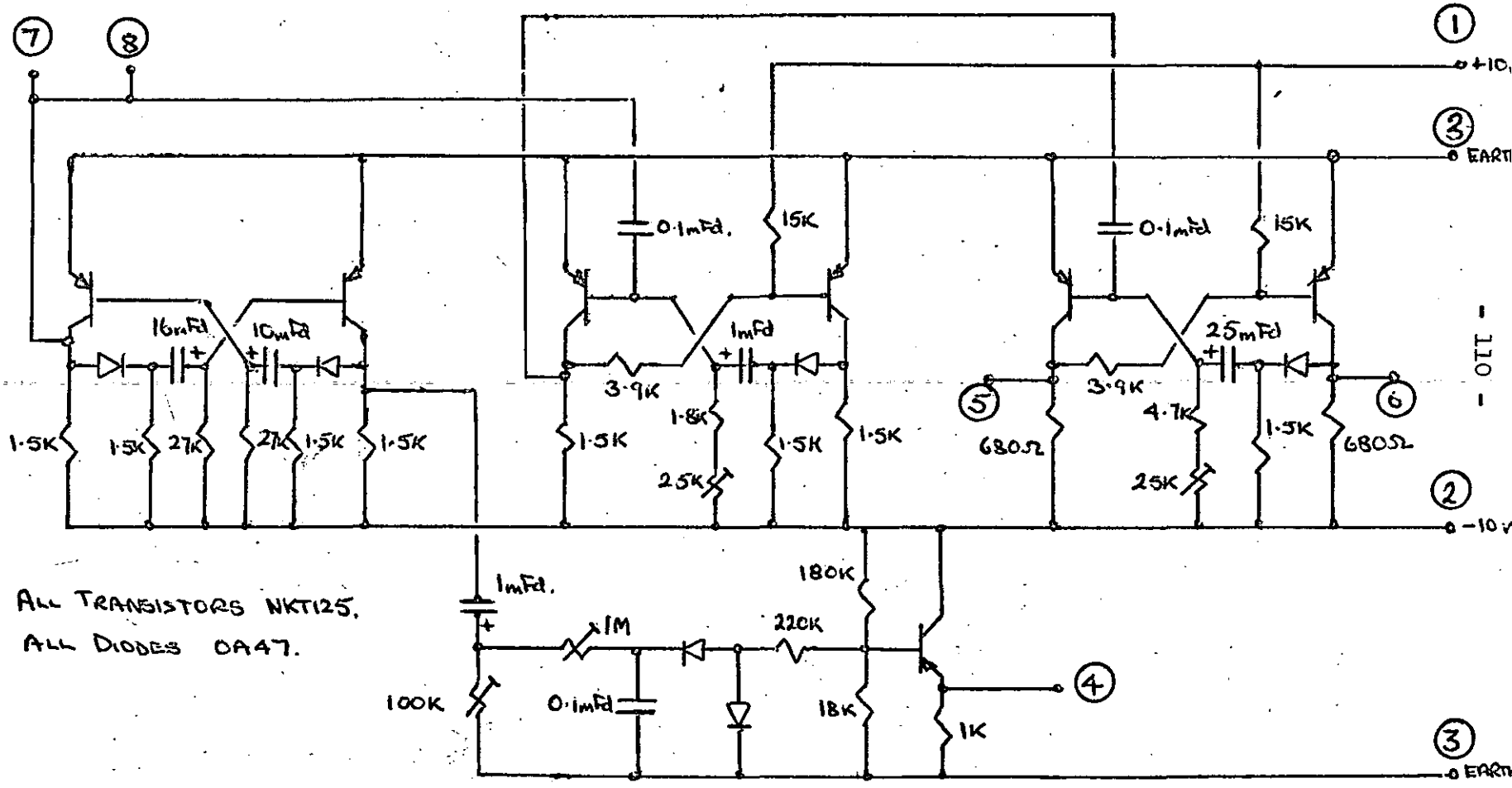
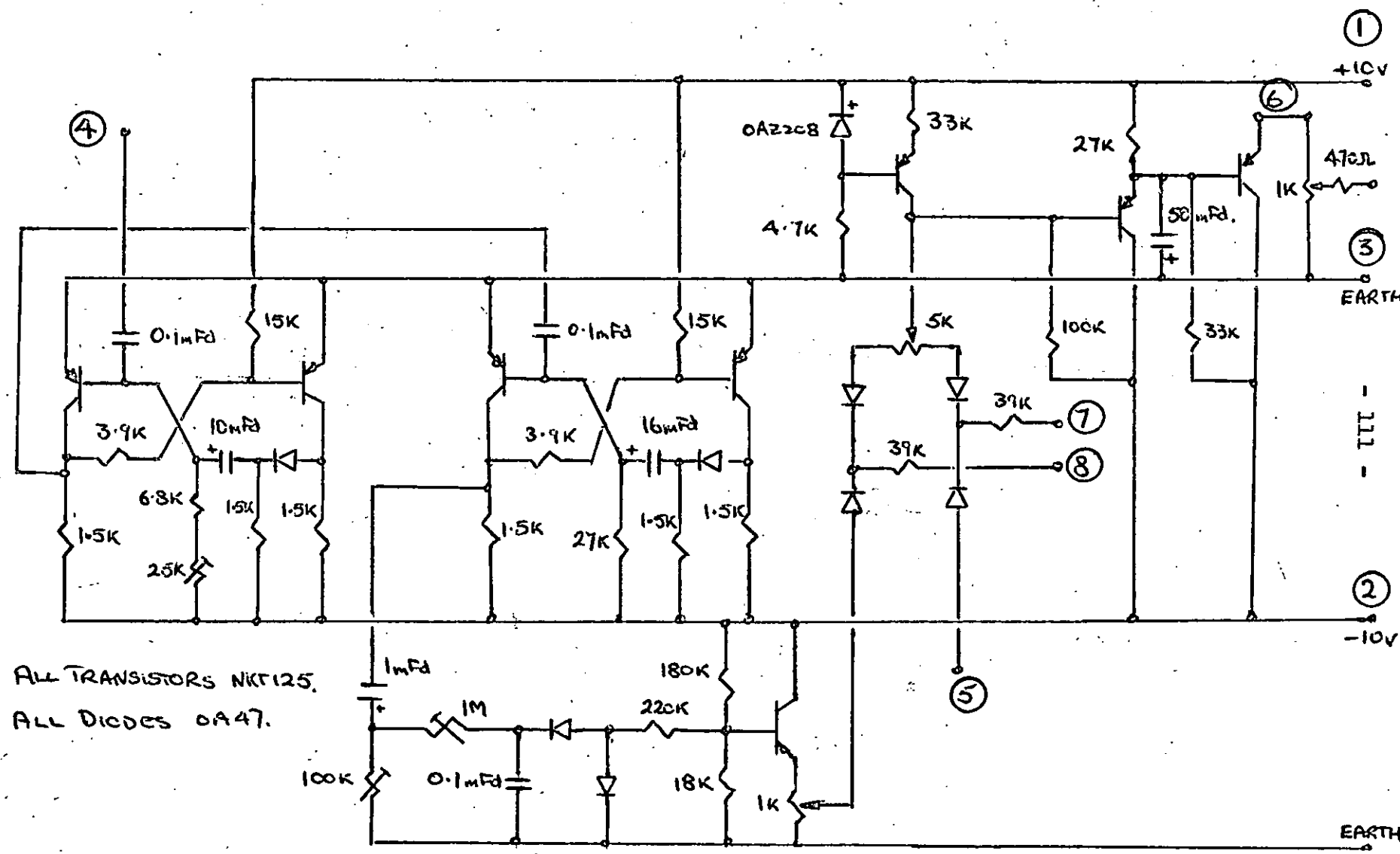


FIG. B.3.

CIRCUIT DIAGRAM, BOARD 1.



ALL TRANSISTORS NKT125.

ALL DIODES OA47.

FIG. B.4. CIRCUIT DIAGRAM, BOARDS 2 AND 4.

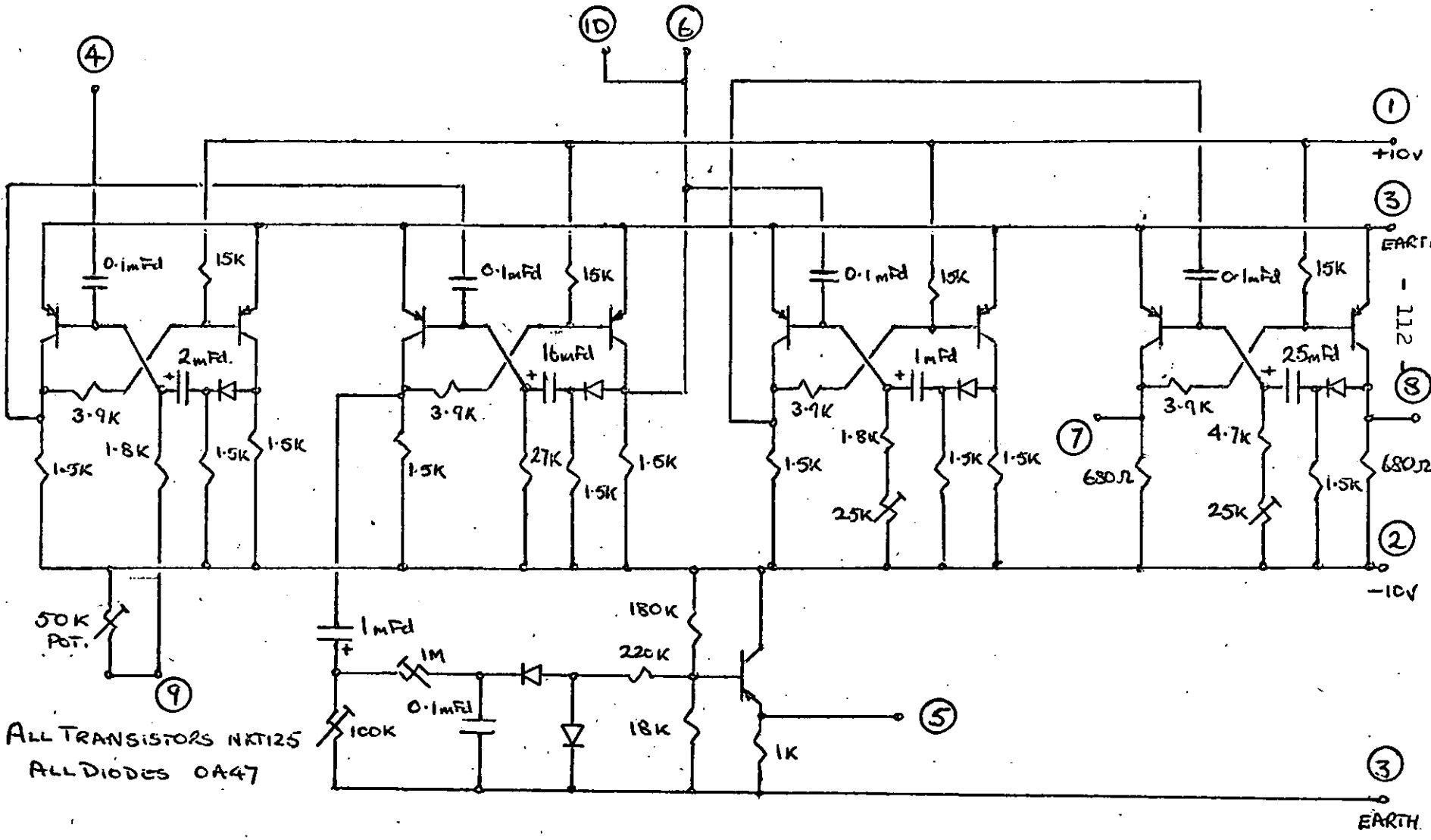


FIG. B.5. CIRCUIT DIAGRAM, BOARD 3.

Appendix C

Current/Voltage Relationship for a Semiconductor Diode

From the physical considerations of a semiconductor junction diode, it has been shown that the forward characteristic of the diode can be written as:-

$$I = I_o \left[e^{\frac{qV}{kT}} - 1 \right] \qquad \text{-------- (1)}$$

Where I_o is the reverse saturation current, and the other symbols have their normally accepted meanings.

Differentation of equation 1 gives:-

$$\frac{\delta I}{\delta V} = \frac{q}{kT} \cdot I_o e^{\frac{qV}{kT}} = \frac{qI}{kT} \qquad \text{-------- (2)}$$

This is an expression for the ac admittance of the diode, and expressing it more conventionally as an impedance gives:-

$$Z \text{ ac} = \frac{\delta V}{\delta I} = \frac{kT}{qI} \qquad \text{-------- (3)}$$

This equation is idealised and does not take into account the resistivity of the semiconducting material, but it can be shown in practice to apply to normal junction diodes provided that the expression (kT) is replaced by (nkT), where n is approximately 1 for germanium and approximately 2 for silicon devices, (51).

Thus the modified impedance term becomes,

$$Z \text{ ac} = \frac{nkT}{qI} \qquad \text{-------- (4)}$$

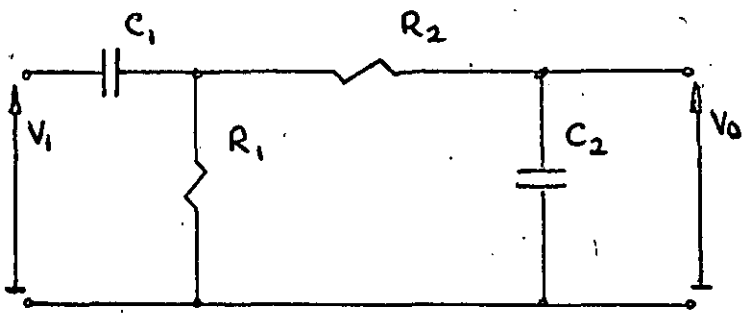


Fig. D.1

Basic Shaping Circuit

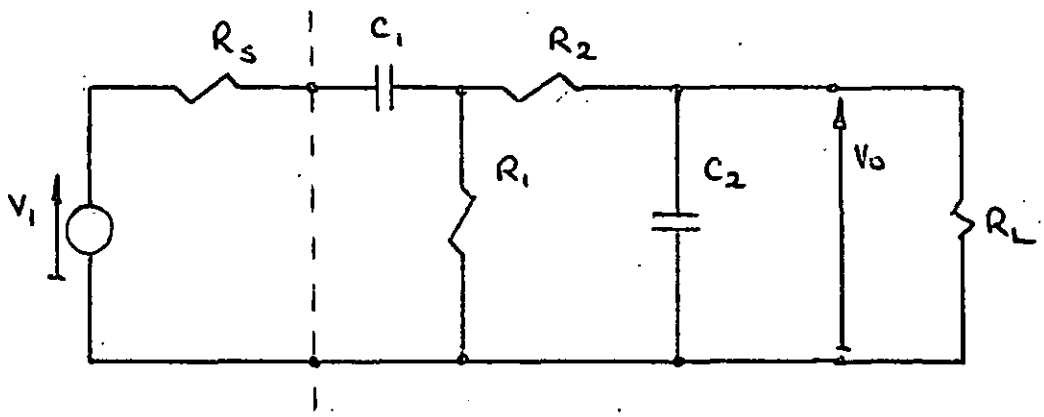


Fig. D.2.

Actual Shaping Circuit

Appendix D

The Shaping Network for the Simulator

As stated in Section 3, the basic shaping element in the Simulator consists of the RC filter shown in fig. D.1. The input is supplied from a source of resistance R_s and the network is terminated with a load resistor R_L, as shown in fig. D.2.

The transfer function, in terms of the Laplacian operator p can be written as:-

$$\frac{V_o}{V_1}(p) = \frac{pC_1R_1}{(pC_1R_1/k)(1 + kpC_2R_2) + \left[(1 + pC_1R_s)/L\right]\left[1 + LpC_2(R_1 + R_2)\right]}$$

Where $k = R_L/(R_2 + R_L)$

and $L = R_L/(R_1 + R_2 + R_L)$

If the assumption that $R_2 \gg R_1 \gg R_s$, is made then $k \simeq L$ and $p\,C_2(R_1 + R_2) \simeq pC_2R_2$

Which gives:-

$$\frac{V_o}{V_1}(p) \simeq \frac{p\,kC_1R_1}{\left[1 + p\,kC_2R_2\right]\left[1 + pC_1R_1\right]}$$

Let $C_1R_1 = T_1$ and $C_2R_2 = T_2$,

Then $$\frac{V_o}{V_1}(p) = \frac{pkT_1}{(1 + p\,kT_2)(1 + pT_1)}$$

Then the response produced by a step input of magnitude B is given by:-

$$V_o(t) = \frac{kBT_1}{(T_1 - kT_2)}\left[e^{-t/T_1} - e^{-t/kT_2}\right]$$

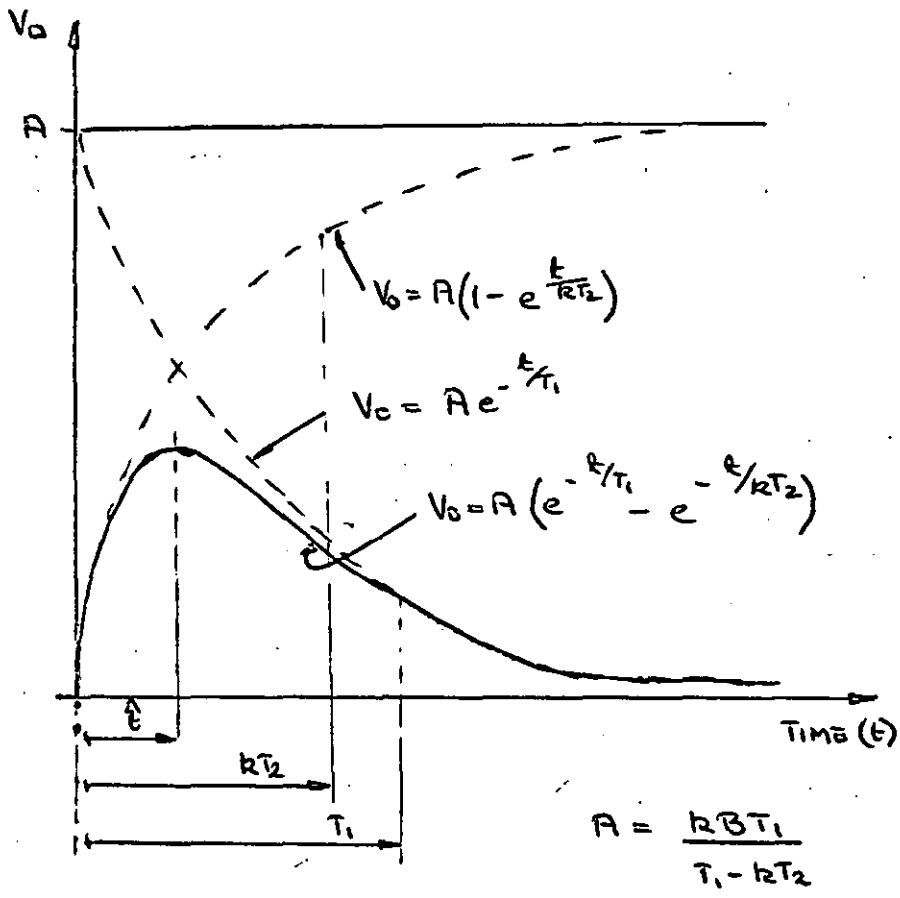


Fig. D.3

Design Diagram.

which is an analytic expression for the shaped waveform.

For design purposes the position of the peak value is required, this is found by the usual methods and gives:-

$$\hat{t} = \frac{kT_1T_2}{T_1-kT_2} \log_e\left[\frac{T_1}{kT_2}\right]$$

Also consider the waveform when $t \ll \hat{t}$, and assuming that $T_1 > kT_2$,

Then $e^{-t/T_1} \simeq 1$; since $\frac{t}{T_1} \simeq 0$.

Hence the waveform is given by:-

$$V_o = \frac{kBT_1}{T_1-kT_2}\left[1 - e^{-t/kT_2}\right]$$

Now when $t \gg \hat{t}$,

$e^{-\frac{t}{kT_2}} \simeq 0$; since $\frac{t}{kT_2} \gg 1$.

and the output becomes:-

$$V_o = \frac{kBT_1}{T_1-kT_2} \cdot e^{-t/T_1}$$

This gives the necessary design information, and its application is shown in fig. D.3. It can be clearly seen, which are the important factors for each part of the waveform.

The actual shaping network used has the various values listed below:-

C_1 = 1mFd $\qquad$ R_2 = 1MΩ Trimmer (500kΩ mean)

C_2 = 0.1mFd. $\qquad$ R_L = 300KΩ.

R_1 = 100KΩ Trimmer (50K mean) $\qquad$ $R_s < 1{\cdot}5$ KΩ.

The assumption that $R_2 \gg R_1 \gg R_s$ is more or less justified, and the various circuit constants becmme:-

$\therefore T_1 = 50\text{msec}; \quad T_2 = 50 \text{ msec}; \quad k = 3/8$

This gives a value of $\hat{t}$ as33 msec, which is a typical figure, for $\hat{t}$.

Appendix E

Fourier Analysis

Any periodic waveform can be analysed, with the aid of fourier analysis into its constituent components.

For a function which has a period, T,

i.e. $f(t + T) = f(t)$

it can be written as:-

$$f(t) = \tfrac{1}{2}a_o + \sum_{n=1}^{\infty}\left[a_n \cos\left[\frac{2\pi nt}{T}\right] + b_n \sin\left[\frac{2\pi nt}{T}\right]\right]$$

Where:-

$$a_n = \frac{2}{T}\int_o^T f(t)\cos\left[\frac{2\pi nt}{T}\right] dt; \quad n = 0 \rightarrow \infty$$

$$b_n = \frac{2}{T}\int_o^T f(t)\sin\left[\frac{2\pi nt}{T}\right] dt.$$

These expressions are useful where an analytic expression for the function exists, but in this case a numerical approximation is used.

The graphical representation of the waveform is divided into 12 equal intervals, such that ordinates are taken at t=0, t/12, ..., 11T/12

Let $\frac{2\pi t}{T} = \theta_k$ and $f(t) = f_k$

Then replacing the integral in the above expressions by a direct summation gives:-

$$a_n \simeq \frac{2}{T}.\left[\sum_{k=0}^{11} f_k \cos n\,\theta_k\right]\Delta T$$

and $$b_n \simeq \frac{2}{T}.\left[\sum_{k=0}^{11} f_k \sin n\,\theta_k\right]\Delta T.$$

Here $\Delta T = T/12$

Thus $\frac{2}{T}.\Delta T = \frac{1}{6}$

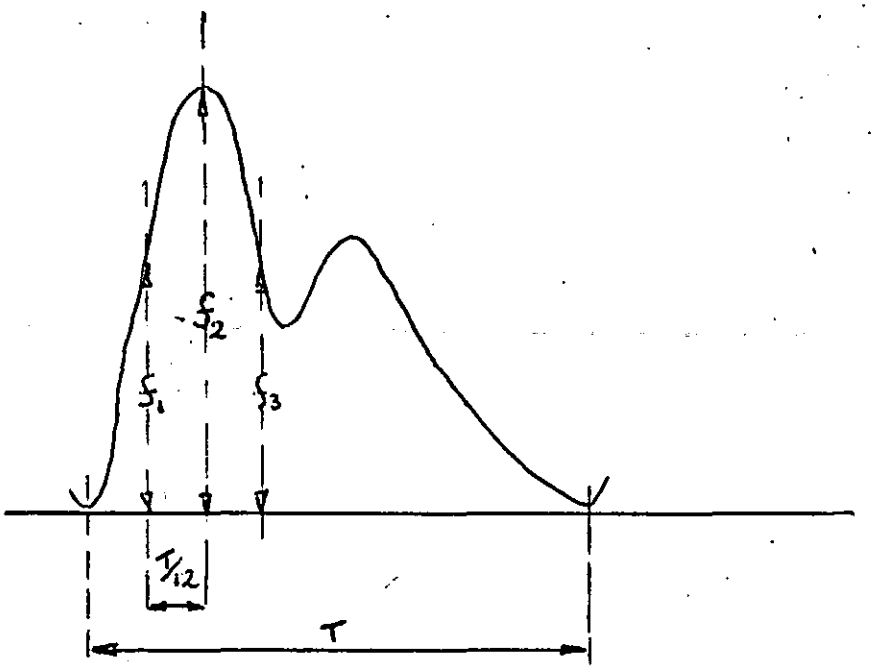


Fig. E.1

Division of Pulse Waveform into Ordinates

The values for $n\theta_k$ are all multiples of 30°, and hence the coefficients are all $0, \pm \frac{1}{2}$ or $\pm \sqrt{3}/2$

Considering the first 3 harmonics only gives that:-

$$a_0 = \frac{1}{6} \sum_{k=0}^{11} f_k$$

$$a_1 = \frac{1}{6}\left[(f_0-f_6) + \frac{\sqrt{3}}{2}\left[(f_1+f_{11}) - (f_5+f_7)\right] + \frac{1}{2}\left[(f_2+f_{10}) - (f_4+f_8)\right]\right]$$

$$b_1 = \frac{1}{6}\left[(f_3-f_9) + \frac{\sqrt{3}}{2}\left[(f_2+f_4) - (f_8+f_{10})\right] + \frac{1}{2}\left[(f_1+f_5) - (f_7+f_{11})\right]\right]$$

$$a_2 = \frac{1}{6}\left[(f_0+f_6) - (f_3+f_9) + \frac{1}{2}\left[(f_1+f_5+f_7+f_{11}) - (f_2+f_4+f_8+f_{10})\right]\right]$$

$$b_2 = \frac{\sqrt{3}}{12}\left[(f_1+f_2+f_7+f_8) - (f_4+f_5+f_{10}+f_{11})\right]$$

$$a_3 = \frac{1}{6}\left[(f_0+f_4+f_8) - (f_2+f_6+f_{10})\right]$$

$$b_3 = \frac{1}{6}\left[(f_1+f_5+f_9) - (f_3+f_7+f_{11})\right]$$

For comparison purposes the ordinates have been deliberately chosen such that the peak value is f_2, as shown in fig. E.1, also all the readings have been scaled such that f_2 is equal to 100 units for each waveform. The zero has been taken as the tangent to the waveform as shown.

SECTION 8

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