An investigation of environmental testing of surface-mounted components

AN INVESTIGATION OF ENVIRONMENTAL TESTING OF SURFACE MOUNTED COMPONENTS

by

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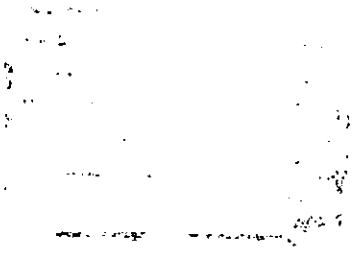
This is to certify that I am responsible for the work submitted in this thesis, that the original work is my own except as specified in acknowledgements or in footnotes, and that neither the thesis nor the original work contained therein has been submitted to this or any other institution for a higher degree.



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ABSTRACT

The increasing acceptance of surface mounting component technology by industry has prompted an examination of the attachment reliability of this technique. This has included a survey of the published literature, the design of suitable test vehicles and the development of test and measurement methods appropriate to this technology.

A comprehensive range of environmental tests have been applied to a variety of different surface mounted component types, including multilayer ceramic capacitors (1812), resistors (1206), and zero ohm jumpers (1206, 0805 and SOT-23). Also SOT-23 micropackaged resistors have been examined. These tests have included power cycling, temperature cycling, damp heat testing and board bending. In the later case cyclic board bending equipment has been developed.

Power cycle testing is the most representative of actual operating conditions, but is a very slow method of testing. The only failure that has been observed in over 14,000 power cycles occurred in a poorly soldered joint. Thermal imaging has allowed an examination of the temperature distributions occuring during power cycling and hence an estimate of the stresses occurring in components. Chip resistors may reach surface temperatures as high as 100°C and it has been shown that this heat flowing into adjacent thermally passive components may generate levels of stress in these passive components similar to those

observed in power dissipating components.

Temperature cycling of 1206 size and SOT-23 zero-ohm jumper chips from -55°C to +125°C has shown that the greatest increases in joint resistance occurs in cycling from -55°C to +95°C. No electrical solder joint failures have been observed in temperature cycling, but cracks have been observed after large numbers of cycles (>1000) on the larger 1812 chip capacitors.

The damp heat tests conducted were both steady state 85°C/8.5%RH and alternating 5 cycles -55 to +125°C and 500 hrs at 85°C/85%RH. A number of leakage current failures occurred in the capacitors tested.

The board bending tests have been conducted at three cycle speeds (1/hour, 30/hours and 600/hour) in order to assess the effects of creep on solder fatigue. Large numbers of failure occur rapidly during this type of testing, but measurements must be taken with the board under stress as the cracks close when the board is relaxed.

CONTENTS PAGE NO.

APPENDICES

ABBREVIATIONS

Ag - Silver

Au - Gold

C - Centigrade

Cu - Copper

DC - Direct Current

DIP - Dual in Parallel

DNP - Distance from Neutral Point

ESR - Equivalent Series Resistance

f - Frequency

F - Farads

Ge - Germanium

h - Height

Hz - Hertz

In - Indium

L - Length

LCD - Liquid Crystal Display

LUT - Loughborough University of Technology

MELF - Metal Electrode Face Bonded

Ni - Nickel

NPO - Negative Positive Zero

N_c - Number of Circuits

N_f - Number of Cycles to Failure

N_t - Number of Terminals

Pa - Pascals

Pb - Lead

Pd - Palladium

Pt - Platinum

PWB - Printed Wiring Board

RH - Relative Humidity

QC - Quality Control

Si - Silicon

SMD - Surface Mounted Devices

Sn - Tin

SO - Small Outline

SOT - Small Outline Transistor

T - Thickness

T_c - Component Temperature

T_{max} - Maximum Temperature

T_s - Substrate Temperature

TEC - Thermal Expansion Coefficient

THI - Third Harmonic Index

THM - Through Hole Mounting

V - Voltage

VLSI - Very Large Scale Integration

VSO - Very Small Outline

W - Width

α_c - Thermal Expansion Coefficient of Component

α_s - Thermal Expansion Coefficient of Substrate

ε_f - Fracture Strain (ductility)

ε_p - Plastic Strain

ε_t - Total Strain

tan δ - Dissipation Factor

Ω - Ohms

CHAPTER ONE - INTRODUCTION

1.1 Background

In modern electronics technology the systems and subsystems that are manufactured involve a wide range of electronic components. In the main, in modern electronics, the circuits are based on integrated circuit technology using MOS or bipolar devices. However, peripheral to these integrated circuits is the need for capacitors (generally tantalum, multilayer ceramic or plastic), resistors - often of a chip variety, inductors and quartz crystals. The whole system needs an interconnection technology to connect the various devices together and modern systems are usually made with either printed circuit boards (single or multilayer) or thick film technology, (either single or double sided conductor-resistor interconnectors or cofired multilayer ceramic). Additionally plugs and sockets are involved in connecting the printed boards or thick film hybrids together.

All the devices have various failure modes which limit their reliability. However it has been suggested that the majority of failures in subsystems are associated with the interconnection technology, including the attachment of the devices to the substrate involved. Therefore the essence of this project is to examine the problems of device attachments and suggest solutions.

The reliabililty of surface mounted devices (SMDs) is currently of particular interest. This is the technique of attaching components directly to a substrate without the through hole leads of more conventional technology (Figure 1(a) and (b)). The origins of this technique

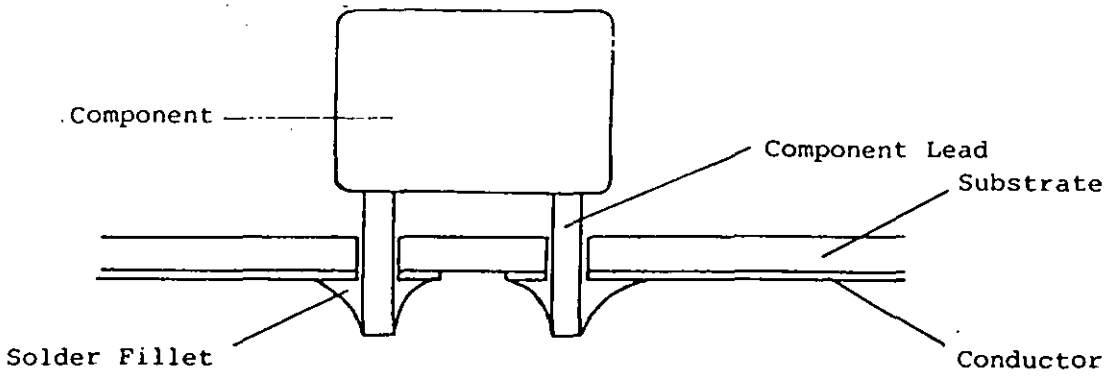

Figure 1(a) Through Lead Mounting

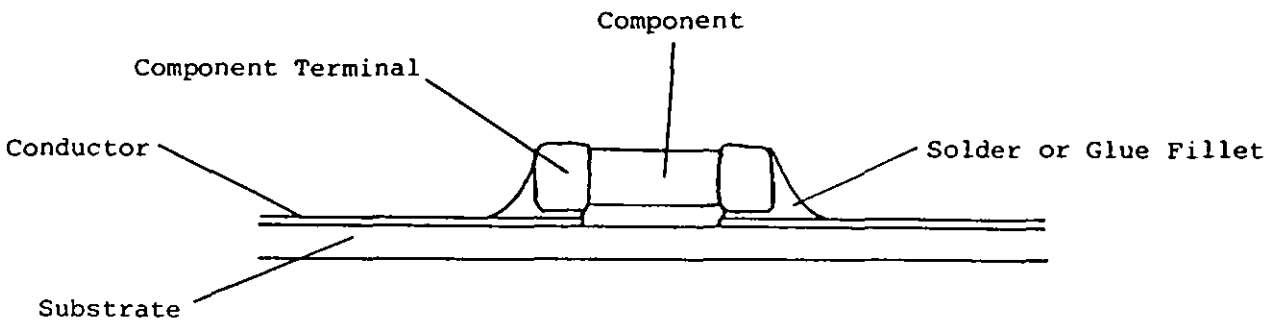

Figure 1(b) Surface Mounting

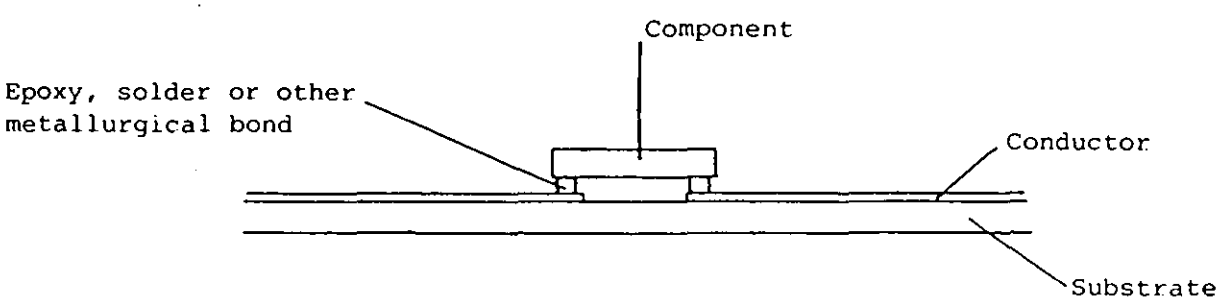

Figure 1(c) Flip Chip Mounting

Figure 1 Through Lead, Surface Mounted and Flip Chip Components

have been traced to 1952 [1], but it is only in recent years that advances in robotics have allowed mass production using this technique. A subset of surface mounted devices are flip-chips, which are components that when attached to a substrate have their terminations under the device (Figure 1(c)).

The growing importance of surface mounted devices is highlighted by tables 1, 2 and 3 (Ref. 2).

The 1983 worldwide consumption of major electronic components is shown in Table 1.

TABLE 1

1983 WORLD CONSUMPTION OF MAJOR ELECTRONIC COMPONENT TYPES

Resistors - 68×10^9 components
Capacitors - 47×10^9 components
Discrete semiconductors - 27×10^9 components
Integrated circuits - 11×10^9 components.

These figures can be further broken up into surface mounted devices (SMD) and those which are through hole mounted (THM).

TABLE 2 [2]

WORLD CONSUMPTION OF THROUGH HOLE MOUNTED COMPONENTS AND SURFACE MOUNTED DEVICES (SMD) ($x10^9$ COMPONENTS)

	THM	SMD	TOTAL
Resistors	57.0	11.0	68.0
Capacitors	34.0	13.0	47.0
Discrete semiconductors	24.6	2.4	27.0
Integrated circuits	10.4	0.6	11.0

A further interesting breakdown of the above figures into geographical areas is shown below.

TABLE 3 [2]

GEOGRAPHICAL BREAKDOWN OF THROUGH HOLE MOUNTED (THM) COMPONENTS AND SURFACE MOUNTED DEVICES (SMD) ($x10^9$ COMPONENTS)

	USA		JAPAN		EUROPE	
	THM	SMD	THM	SMD	THM	SMD
Resistors	8.6	0.6	40	10.0	8.0	0.5
Capacitors	6.1	0.9	23	10.0	5.0	2.0
Discrete semiconductors	12.8	0.2	7	2.0	4.0	0.8
Int.Ccts.	6.0	0.1	3	0.5	1.5	-
TOTALS	33.5	1.8	73	22.5	18.5	3.3
Percent by area	95%	5%	76%	24%	85%	15%

The projection for 1990 is that 13% of major components in the USA will be surface mounted whereas 48% will be surface mounted in Japan. By the year 2000 25% of all components will be surface mounted in the USA, whilst 75% of all major components in Japan will be surface mounted. No projected figures for Europe were available.

It must be remembered, however, that the Japanese are very much in the consumer market compared with the USA (Table 4), with a high usage of capacitors and resistors, the most commonly used surface mounted components.

TABLE 4

1984 VALUES OF EQUIPMENT MARKETS ($ x 10^9) [3]

	USA	%	W.EUROPE	%	JAPAN	%
Data Processing	79.0	61.5	25.6	42.4	17.3	41.3
Consumer	21.3	16.6	15.8	26.2	11.2	26.7
Communications	11.5	8.9	12.8	21.2	3.2	7.6
Industrial	7.4	5.8	2.8	4.6	4.8	11.4
Test	5.9	4.6	1.3	2.2	1.1	2.6
Medical	1.8	1.4	1.7	2.8	1.2	2.9
Automotive			1.7	4.1		
Others	1.5	1.2	0.4	0.7	1.4	3.3
TOTAL	128.4		60.4		41.9	

The bulk of the electronics industry in the USA is concerned with computer and industrial applications (including data processing) requiring reduced resistor and capacitor usage.

1.2 Programme

The technique of surface mounting components onto printed circuit type substrates is a rapidly expanding technology but in common with the adoption of any new technology, an assessment of any reliability hazards is required.

It is agreed that the principle reliability hazard in surface mounting technology is fatigue cracking of the solder fillet, caused by cyclic thermal stresses [4, 5, 6]. These stresses may be caused by both cyclic variations in power dissipation within equipment and by external environmental temperature changes.

The program has therefore had a strong emphasis on cyclic stress testing. The test program has included '0805', '1206' and '1812' chip devices and SOT-23 micropackages. All the devices wave soldered onto FR4 printed circuit board test coupons.

The cyclic stress tests are:-

(a) Power cycling - this test most accurately simulates actual working conditions.

(b) Thermal cycling - these tests are in common use, but are not representative of normal working conditions and consequently may provide misleading information.

(c) Mechanical cycling - mechanical or isothermal cycling tests have been investigated as a more meaningful accelerated test than thermal cycling.

In addition to these cyclic stress tests, damp heat tests (85°C/85% RH) and combined thermal cycling/damp heat tests (5 cycles -55 to +125°C/85°C/85% RH) were performed.

Thermal mapping work has also been conducted in order to assess the levels of strain that may occur during equipment operation.

1.3 References

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CHAPTER TWO - SURVEY

2.1 Introduction

The technology of surface mounting components is rapidly expanding from its origins in thick and thin film hybrid microcircuits and gaining acceptance for use with conventional printed wiring boards (PWBs). The market forces behind this trend are size, weight, cost and in complex systems, interconnection density. New component packages are also becoming available, both expanding the range of components available for use with this technology, and also taking advantage of the finer lines and spacing of conductors now available (for many years the industry standard for PWB layout has been a 0.1 inch grid; however component lead spacings down to 0.02 inches are now possible).

The problems and uses of SMDs in hybrid circuits have received much attention and are quite well understood. However the use of new components, substrates and soldering techniques involve continued attention to the problems associated with surface mounting technology.

2.2 A Hierarchy of Attachment Levels

Within any electronic system there exists several layers of interconnection/packaging. Figure 2 shows a hierarchy established by IBM [1] for their smaller computer systems, which, in general, may be applied to any electronic system. The hierarchy is as follows:-

(a) Individual component packaging - the components will normally be packaged singly. However in the case of hybrid circuits

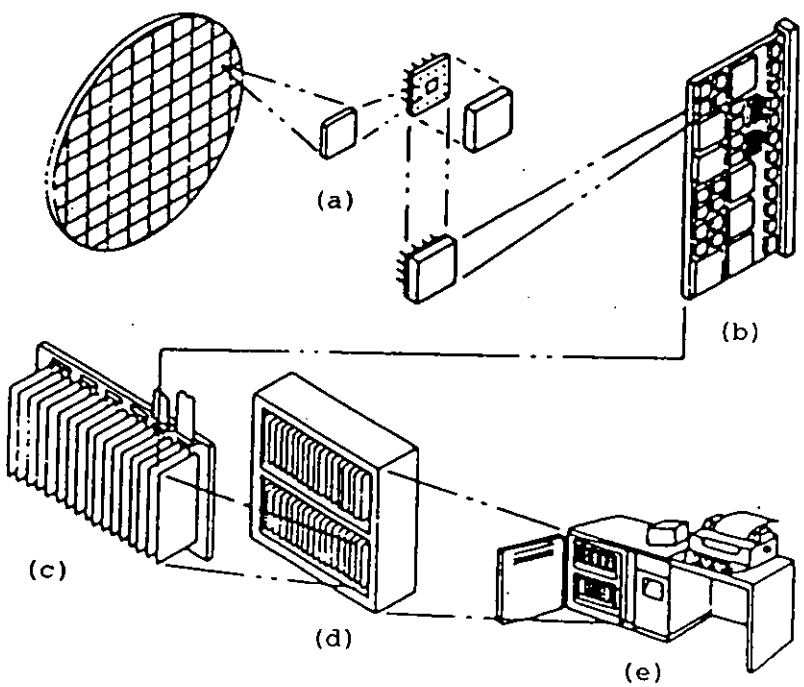


Figure 2 A Hierarchy of Interconnections (after Bonner et al, Ref. 1) from Silicon Wafer to Complete Computer System.

many components may be packaged simultaneously. In the case illustrated a silicon wafer is diced and the dice are assembled into chip carriers.

(b) The packaged components are assembled onto a daughter board.

(c) The daughter boards are connected to a mother board to form a module. At this and subsequent stages connectors are usually separable, as opposed to the normally permanent connections at earlier stages.

(d) Subsystems are assembled from modules.

(e) Subsystems are interconnected to give the final system configuration.

Some variation occurs between different systems, e.g. small systems may miss one or more of the intermediate levels. Hybrid circuits may contain a combination of both packaged and non-packaged components and components may be attached to daughter boards by separable connectors (e.g. DIP sockets).

As greater integration levels are achieved by semiconductor manufacturers, the demands upon the interconnection technology may be expected to decrease. However system complexity also grows so that often interconnections remain as important.

The interconnection density at any level of packaging may be estimated by Rent's relationship [2]:

$$N_T = N_C^{\beta}\alpha \qquad (1)$$

This empirical formula gives the number of terminals N_T for a package containing N_C circuits. The parameters α and β depend upon system size, and for large systems, values of 2.5 and 2/3 are typical [3]. This relationship is however not applicable to devices such as microprocessors and memory arrays which, being functional modules, require far fewer interconnections.

However, the number of connections has risen from 2-4 per component for discrete devices, to a hundred or more for today's VLSI components containing thousands of active devices.

These massive increases in circuit densities also make the testing of systems more complex, as access to fewer nodes of a system (in relation to the system size) becomes possible. This means that testability is rising in importance as a constraint upon design [4].

Care must also be taken to ensure that improvements in one area of packaging do not lead to unacceptable constraints on other packaging levels. For example, it has been claimed that with conventional (i.e. two layer) printed circuit technology, the pin grid array package using 0.1 inch pitch leads can use less printed board area than the smaller chip carrier which uses 0.05 inch pitch leads. This is because the closer pitch leads prevent the routing of tracks between pins,

resulting in a 'dead' space beneath the chip which is not entirely compensated for by the area released for use on the reverse side of the board.

2.3 Surface Mounting of Components

2.3.1 Advantages of Surface Mounting Components

The following advantages can be identified:-

(i) Size and weight - this can be reduced overall.

(ii) Interconnection density.

(a) DIP packages have a practical limit of about 64 pins which is insufficient for many VLSI devices. Chip carriers used for surface mount however offer up to 156 pins and IBM have produced flip chip devices with as many as 354 interconnections [5].

(b) The substrate pad area occupies only one side or conductor level of the board leaving room on the reverse side for either additional components or conductors (especiallly advantageous for multilayer boards).

(iii) Automatic Placement

Because leads do not have to be aligned with holes in the substrate, automatic component placement is very easy.

(iv) High frequency performance

The shorter signal paths have a lower impedance and thus superior high frequency performance (for leadless ceramic chip carriers track resistance and line to line capacitance are reduced by sixty to ninety percent over their DIP counterparts [6]).

(v) Component costs

Many surface mounting components have the potential to be cheaper than leaded devices. Two examples can be quoted. Ceramic chip capacitors follow an identical production path to their leaded counterparts, but do not receive the final lead attachment and encapsulation, both expensive processes. Ceramic chip carriers are basically the centre section of a DIP package without the leads - similar processes are used in manufacture but less materials are used.

2.3.2 Disadvantages

Some disadvantages can be recognised:-

(i) Some components are either unavailable or very expensive in surface mountable form, forcing the use of a mixed mounting technology (this situation is continuously improving however).

(ii) Surface mounted components are very much more sensitive to mechanical and thermal strains.

(iii) The solder fillet, i.e. the solder volume that attaches the devices to the substrate, is difficult to inspect. This is because of its small size and the fact that at least part of the fillet is hidden under the component.

(iv) The lower thermal impedance of components designed for surface mounting means that during soldering the safe operating region in terms of temperature and time is smaller and the thermal demand higher, making it much harder to achieve a solder joint without damaging the components.

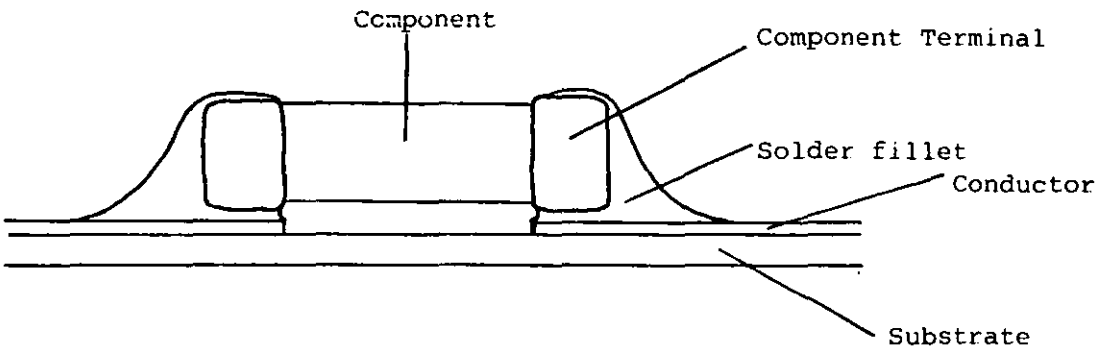
(v) Rework and field repairs are more difficult.

2.3.3 Methods of Attachment

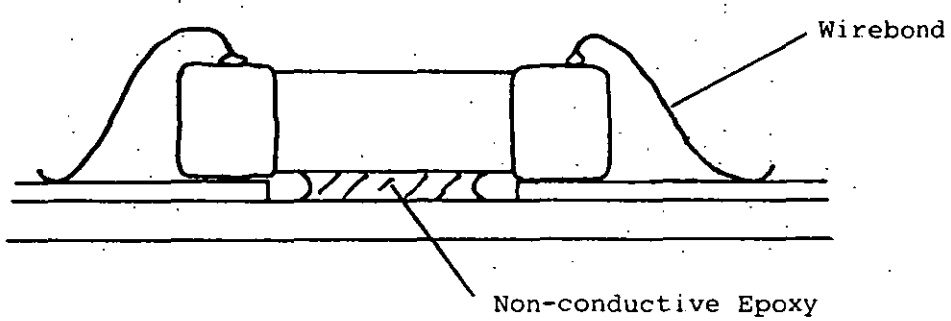
The most common methods for attachment of components (other than semiconductor dice) are listed below [7].

(a) Soldering - Figure 3(a) - a low melting point alloy - typically tin and lead, forms a metallurgical bond between component and conductors.

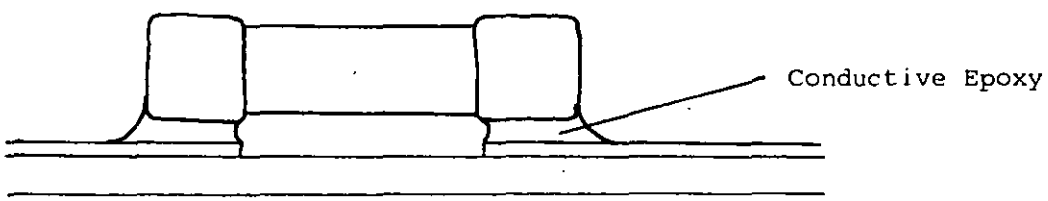
(b) Wire bonding - Figure 3(b) - components are glued to the substrate and subsequently connections are made by the same method of wire bonding used for semiconductor die. Thermal stresses only occur in the mechanical attachment and are low, but the wires



a) Soldering



b) Wirebonding



c) Conductive epoxy

Figure 3 Methods of Attachment

are fragile and difficult to handle. It is also a relatively slow and expensive process.

(c) Conductive epoxy - Figure 3(c) - this technique gives rise to higher stresses in components [8], due to the more rigid attachment. Thus fracture is more likely. However failures of this nature are likely to occur at the beginning of the component working life (infant mortality) and the long term hazard of solder fatigue is absent.

2.4 Substrates

2.4.1 Functions of the Substrate

Virtually all electronic assemblies consist of components or sub-assemblies mounted on a support plate or substrate. There are two primary functions of the substrate:

(a) To provide mechanical support for the components.

(b) To support a conductor pattern for interconnecting the components.

Secondary functions of the substrate are to assist in dissipation of heat from the assembly and sometimes to provide electromagnetic shielding.

2.4.2 Properties of Substrates

Various properties of substrates affect their suitability in any particular application:-

(a) Mechanical strength - seldom a problem unless there are some heavy components or, as sometimes, the substrate is designed to form part of the final packaging of the system. However, large, brittle (i.e. ceramic/glass) substrates may be difficult to handle and subject to fracture in mechanically harsh environments.

(b) Ability to support a conductor system - there are four main methods for producing the electrical interconnections.

(i) Chemical etching of a conductive foil laminated to or deposited on the substrate (referred to as a printed wiring board);

(ii) Screen printing of a conductive paste onto alumina and subsequent firing (the thick film circuit). The development of polymer thick film pastes with their much lower firing temperatures (under 260°C as opposed to 800°C for conventional glass frit pastes) allows the use of this technique with a much greater range of substrates than previously;

(iii) Deposition, usually onto glass, by evaporation, sputtering or chemical reduction plating of a conducting layer which is then chemically etched (the thin film circuit);

(iv) Discrete wiring systems such as wirewrap, speedwire, etc.;

These techniques may be combined on one substrate. An example is the chemical plating of 'vias', i.e. connections between conductor layers, in printed wiring boards. It is also possible to add polymer thick film components/conductors to previously etched printed wiring boards.

(c) Insulation resistance - substrates must obviously have a high surface resistivity. Where the primary substrate material is conductive an insulating layer must be applied, e.g. the insulated metal substrate.

(d) Thermal conductivity - important in circuits where either heat cannot escape directly from components into the environment (e.g. where encapsulation prevents air cooling), or where high power densities require additional conductive cooling.

(e) Thermal expansion coefficient - this has a profound effect on the reliability of circuits using leadless surface mounted devices. This is because differential thermal expansion creates large strains in both components and the interconnect system. This may also affect the reliability of vias or through hole plating in printed circuit boards.

(f) Modulus of elasticity - this affects the ability of the substrate to absorb both mechanical and thermal strains.

(g) Dielectric constant - very important in high frequency applications or where it is required to integrate capacitors into the substrate.

(h) Surface flatness - important for the production of screen printed conductors and also for the use of wave soldering.

(i) Electromagnetic shielding - insulated metal substrates (IMST) may have to be used and these have the advantage of providing shielding of electromagnetic interference [9].

Table 5 shows some properties of substrate materials as reported in the literature. Table 5 also shows the not inconsiderable variations between data from different sources. These variations may be due to either differences in the materials tested or the test being carried out at different temperatures.

2.4.3 Substrates for Surface Mounting Components

Surface mounting technology originated with thick and thin film circuits, using glass (alumino-silicate or borosilicate) for thin film substrates and alumina for thick films. However, not only do various other substrate materials have advantages for use with these technologies, but also PWB technology is increasingly being used with surface mounting components.

The main reasons for the use of alternative substrates for thick film products are matching of thermal expansion coefficient,

TABLE 5 PROPERTIES OF SUBSTRATE MATERIALS

	THERMAL EXPANSION COEFFICIENT ($X10^{-6}$)	YOUNGS MODULUS (GPa)	THERMAL CONDUCTIVITY (W/m °C)	DIELECTRIC CONSTANT
GaAs	5.73		55	12.85
SILICON	2.15 - 4.0		160	11.7 → 12
SILICON CARBIDE	2.6 - 3.3	400	270	40
ALUMINIUM NITRIDE	2.65		140 - 170	10
BOROSILICATE GLASS	3.2	69	121	4.6
ALUMINOSILICATE GLASS	4.2	89	50	6.3
BERYLLIA (BeO)	5.4 - 8	320	240	6.5
ALUMINA (Al_2O_3)	6 - 7.9	250 - 380	10 - 35	8.5
STEELS	12	200	60	DEPEND ON
COPPER	16.7	13	385	INSULATING
ALUMINIUM	23	70	238	MATERIAL
POLYMERIC* SUBSTRATES	3 - 30	LOW	GENERALLY LOW	2 - 5

*The properties of fibre reinforced plastics vary enormously depending on the fibre type, the resin and the lay-up technique.

improved thermal conductivity and lower cost. Beryllia has a high thermal conductivity, as have aluminium nitride and silicon carbide. These last two also have thermal expansion coefficients close to that of silicon [10, 11], and have dielectric constants somewhat higher than that of alumina. All are however more expensive and beryllia is highly toxic.

Insulated metal substrate technology has a number of potential advantages - lower cost for large areas, increased toughness and good heat conductivities. However technical difficulties have slowed its acceptance by industry.

Organic substrates have several advantages for surface mounting. These are:-

(a) Coefficient of thermal expansion may be tailored to the application, e.g. the use of kevlar fibres allows the thermal expansion coefficient (TEC) to be reduced to that of silicon allowing low stress attachment of flip chip devices [12], and metal (invar) cored boards are available with their TEC values closely matched to that of ceramic chip carriers [13].

(b) Low dielectric constant.

(c) Generally cheap.

(d) Readily available in large sizes.

(e) Generally compatible with conventional mass production equipment.

When leaded surface mounted components are used, for example the tantalum capacitor in Figure 6(d), the lead acts as the compliant member to allow for differences in expansion of the device and the substrate. These differences in expansion may be caused by differences in material co-efficients of thermal expansion, temperature differences due to power dissipation within the device, or both of these effects acting at once.

When leadless components are surface mounted the solder becomes the compliant member in the structure and the solder joint will be stressed.

Three approaches to solving the compatability problem between the substrate and surface mounted component have been used. These are [48]:-

(i) Constraining Dielectric - a low expansion inorganic or organic system with an inherently low CTE matching the components.

(ii) Unconstrained approach - This accommodates the differences in CTE by flexibility in a lead, a thick solder joint or a resilient layer on the top surface of the PWB.

(iii) Constrained approach - This approach uses a low expansion substrate with a restraining core (e.g. copper-invar-copper within fibreglass) to restrain the X-Y expansion of the inter-connection structure. The system is rigidly bonded together.

2.5 Components for Surface Mounting

2.5.1 Multilayer Ceramic Capacitors

These are one of the best established surface mountable components. They have excellent resistance to soldering heat, but unless their silver palladium terminations are given a barrier layer, e.g. nickel, they are susceptible to solder leaching, particularly during wave soldering (Figure 4).

The very high rigidity (Young's modulus) of the ceramic body means thermal strains must be absorbed by the solder fillet or substrate.

The thermal expansion coefficient of these devices may be substantially different to that of the bulk dielectric material, and appears to have a substantial spread between capacitors of the same dielectric type. Hence thermal strains are not entirely predictable. Table 6 gives figures obtained for four dielectric types, two high permittivity (K1200) and two low permittivity, low temperature coefficient of capacitance (NPO) dielectrics. Table 6 shows both the difference in expansion coefficient between these different dielectric materials and the spread of expansion coefficient for capacitors made with the same dielectric material.

TABLE 6

THERMAL EXPANSION COEFFICIENT OF CHIP CAPACITORS [14] (10^{-6}/°C

Component	R11-K1200	R13-K1200	R11-NPO	R13-NPO
1	12.0	14.0	21.8	12.6
2	20.4	11.5	17.5	14.7
3	24.2	14.6	17.7	14.7
4	19.0	13.6	18.3	14.8
5	20.6	14.7	20.5	13.8
AV. VALUES	19.2	13.8	21.2	14.2

2.5.2 Chip Resistors

These are made by thick or thin film technology usually on alumina or glass substrates respectively. Figure 5 shows a cross section through such a device. The resistive film is usually protected by a glass coating. Like ceramic capacitors, these have a high rigidity and may produce large strains in the solder connection due to differential thermal expansion. This may occur even on alumina substrates because power dissipation may result in the resistor body being substantially hotter than the substrate.

2.5.3 Solid Tantalum Capacitors

These have been produced in three basic forms (Figure 6a, b, and c) for surface mounting [15]: the T-bar, the hybrid and the moulded. The T-bar is difficult to use and very susceptible to mechanic-

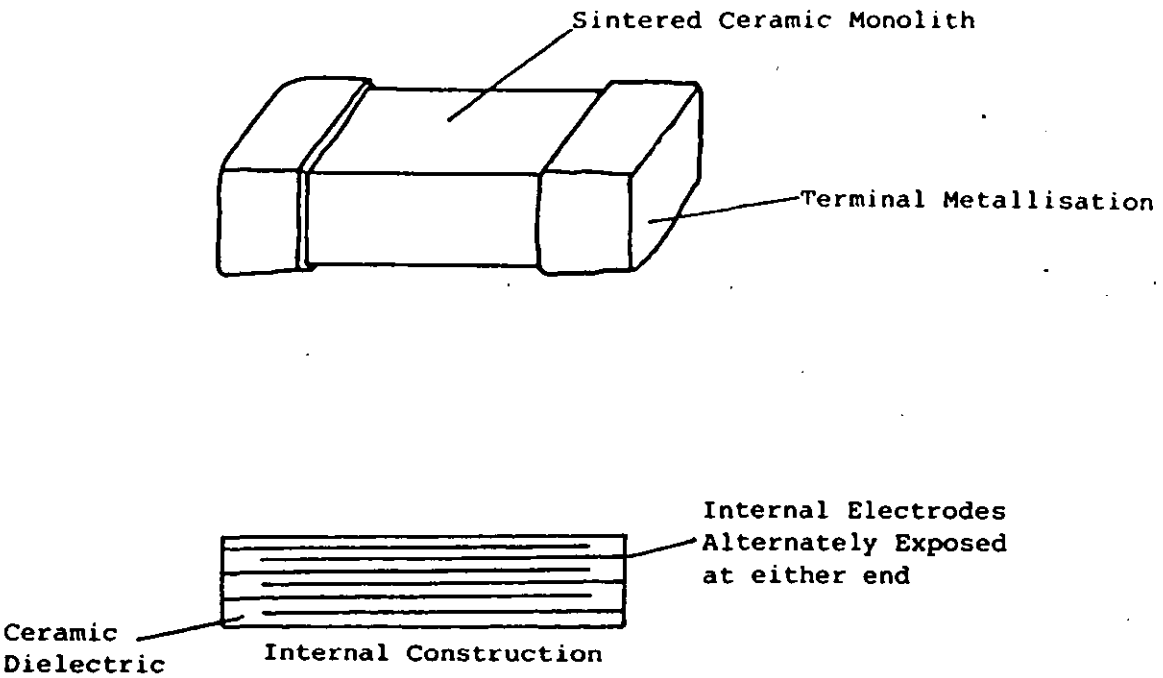


Figure 4 Multilayer Ceramic Capacitors

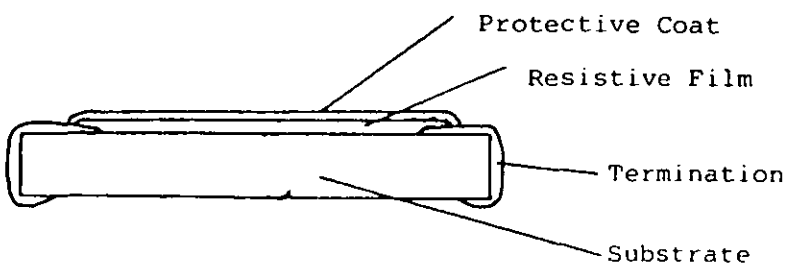


Figure 5 Chip Resistors

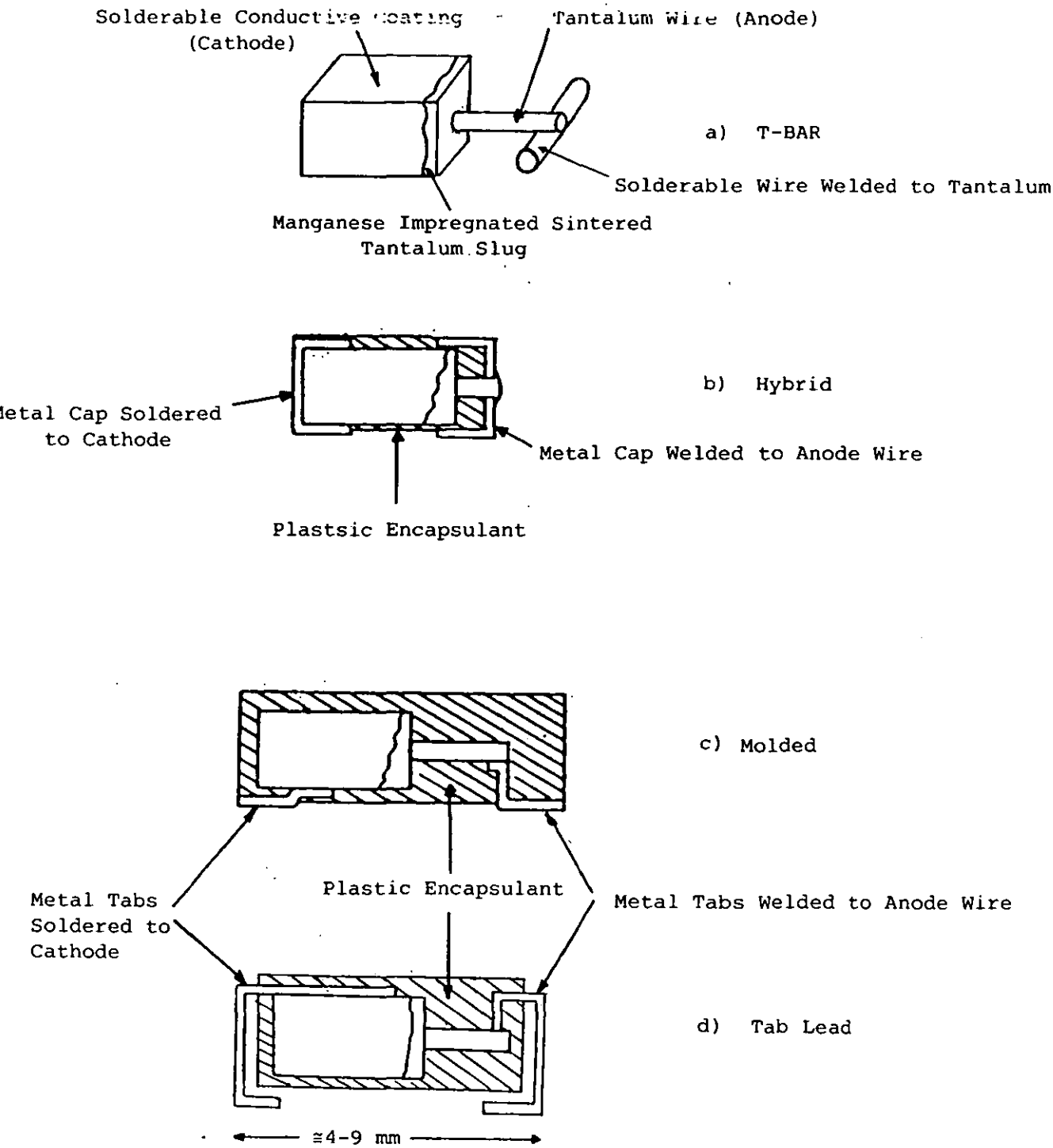


Figure 6 Solid Tantalum Capacitors (after Bell and Hyland, Ref. 15).

al and thermal damage. The hybrid has the highest volumetric efficiency, but is both susceptible to thermal damage to the silver coating of the anode and thermal fatigue similar to that experienced with ceramic capacitors [16]. The molded device has a slightly lower volumetric efficiency, but the possibility of incorporating tab leads (Figure 6d) allows stress relief and gives a longer thermal path from the connecting pads to the anode.

2.5.4 Soldered on Transistors (SOT)

These devices have short leads, giving good stress relief provided the solder fillet size is not excessive [17]. Figure 7 shows a SOT from various angles.

2.5.5 Metal Electrode Face Bonded Devices (MELF)

Cylindrical components such as resistors and diodes may be supplied with metallic caps in place of their normal leads. These are rigid devices and when attached to a substrate the solder fillet can also be subject to solder fatigue (Figure 8).

2.5.6 Small Outline Packages (SO)

These packages for integrated circuits and such things as resistor networks have small leads on a 1.27mm pitch giving substantial size reductions over their DIP counterparts (Figure 9). An extension of this family of packages is the VSO (very small outline package) with terminations on a pitch of 0.762mm. As with the soldered on

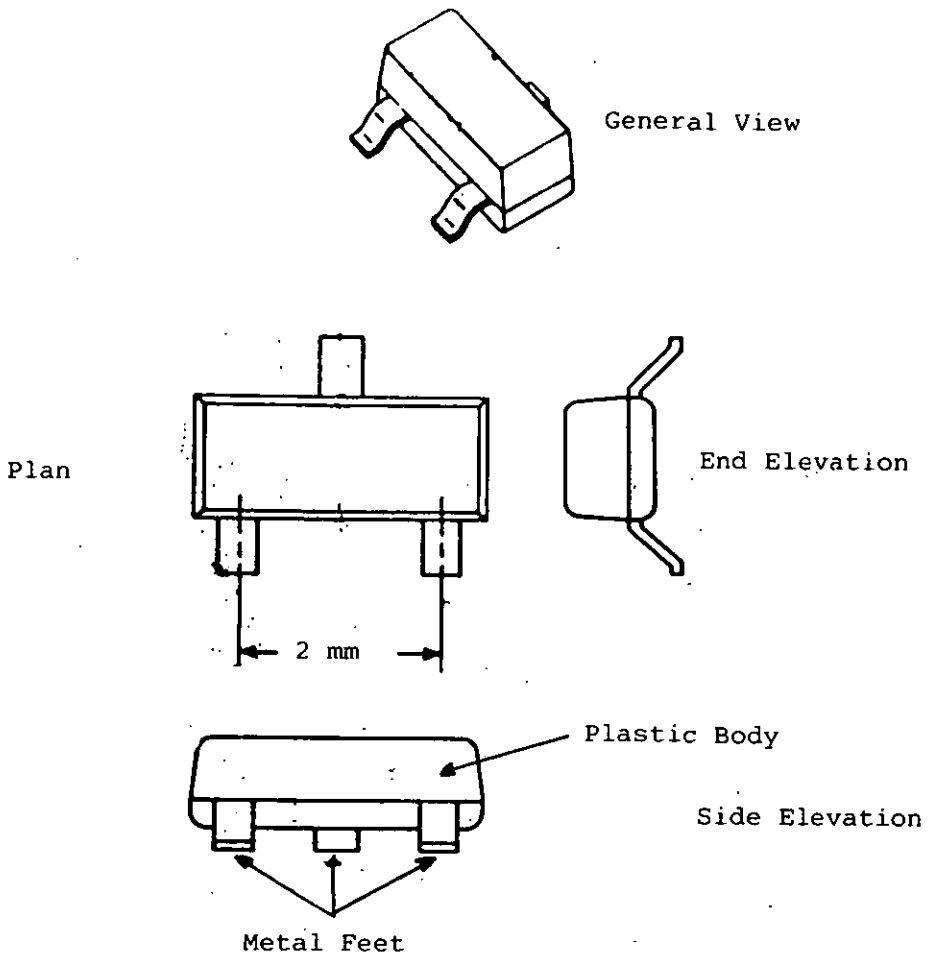


Figure 7 Soldered on Transistors

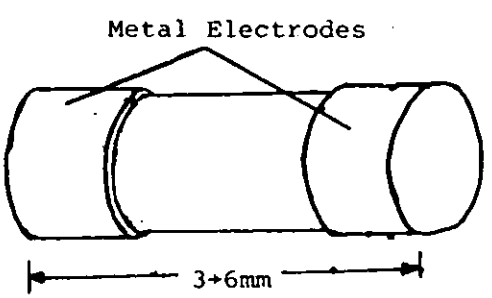


Figure 8 Metal Electrode Face Bonded Device

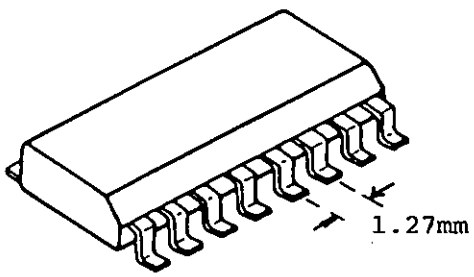


Figure 9 Small Outline Package

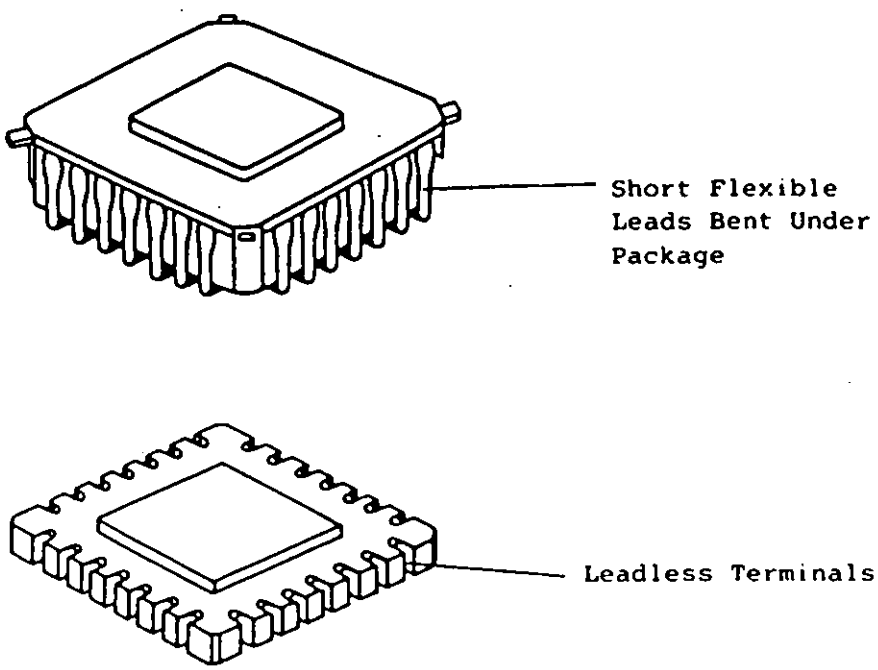


Figure 10 Leaded and Leadless Chip Carriers

transistor the leads will normally give sufficient stress relief. These packages however can be incompatible with the large die sizes of modern VLSI devices.

2.5.7 Chip Carriers

Various types of chip carrier are in use, both plastic and ceramic, with or without leads (Figure 10). Virtually all conform to Joint Electron Devices Engineering Council standards and are thus interchangeable by way of pad geometry [18]. The chip carrier has terminations on all four edges giving small size and short signal paths. However their size is large compared with most surface mountable components and therefore thermal expansion mismatch is critical in the leadless types [19]. British Telecom has greatly reduced this problem for PWB mounted devices by manufacturing their 'Epic' chip carrier from FR4 - a fibreglass material commonly used in PCB manufacture.

2.5.8 Other Surface Mountable Components

The range of components in surface mountable form is increasing rapidly with switches [20], connectors [21], inductors, relays, etc. now available.

2.6 Semiconductor Die Attachment

2.6.1 Attachment Techniques

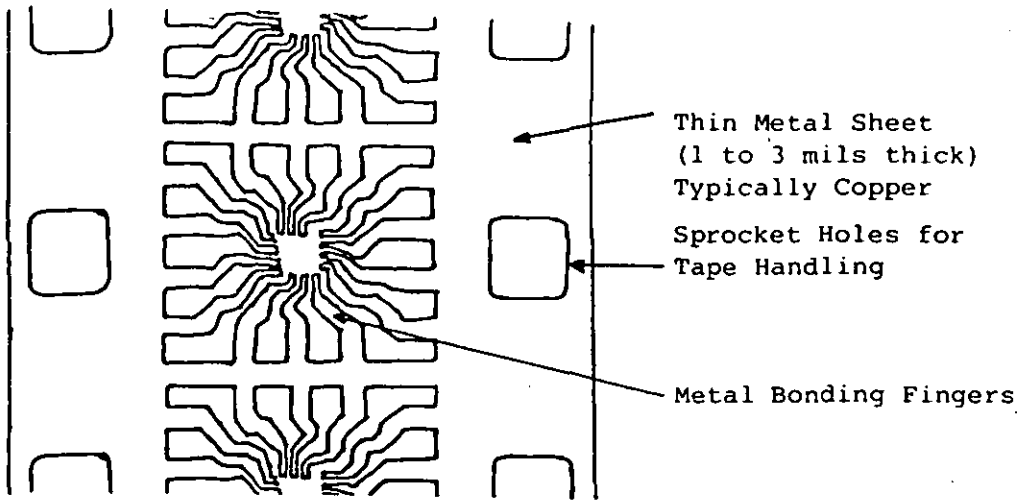
Many mass bonding techniques have been proposed as replacements for wire bonding in circuit fabrication [22], but none have gained

universal acceptance. All have their advantages, but many suffer from the need for specially processed/metallized dice or other problems [23].

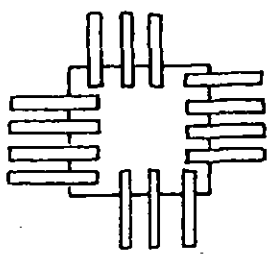
The main limitations of wire bonding are the handling problems of delicate chips and wires, and the difficulty of pretesting devices prior to assembly. These give rise to poor yields in large modules. Assembly into chip carriers as the first level of packaging helps to overcome these limitations, but where system design requirements preclude this there is a need for a better bonding technique. The most promising alternatives are:

(a) Tape automated bonding (TAB) [24] - this technique uses a tape, etched with a conductor pattern, which may be bonded in one operation to the die before it is back-bonded (Figure 11). Back-bonding is the process of joining the back or non active side of the die to the substrate. This allows full device characterisation prior to assembly and, with the development of bumped tape [25], does not require special device metallization, (i.e. gold bumping is done to the tape, not the bonding pads of the device). Lead impedances are also greatly improved over wire bonding.

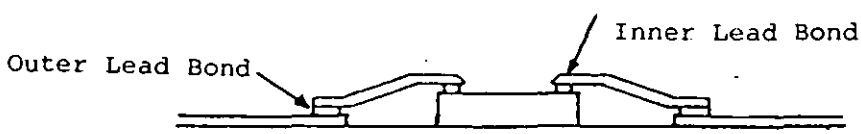
(b) Flip chip bonding (Figure 12) - Early techniques using ultrasonic welding, thermocompression bonding, or soldered copper balls required very accurate chip alignment. This was very difficult because the terminals are hidden beneath the chip. The technique also suffered from planarity problems for devices with more



Bonding Tape
Metal Bonding Tape

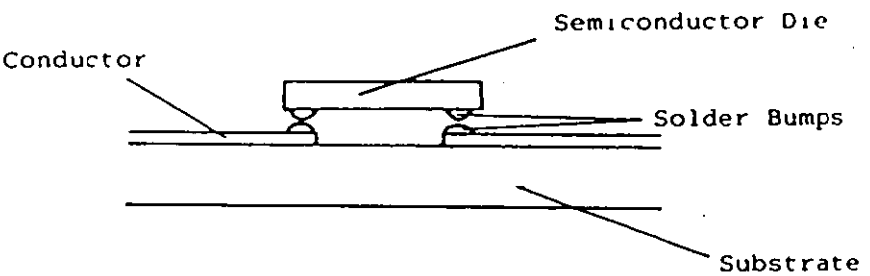


Chip Inner Lead Bonded and Excised from Tape

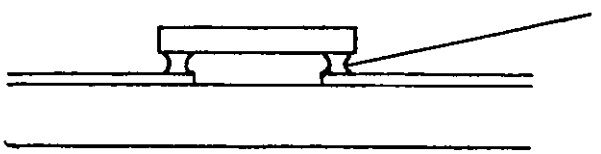


Chip Attached to Substrate and Outer Lead Bonded

Figure 11 Tape Automated Bonding



a) Before soldering



b) After soldering

Figure 12 Controlled Collapse Flip Chip (a) before and (b) after Reflow Soldering.

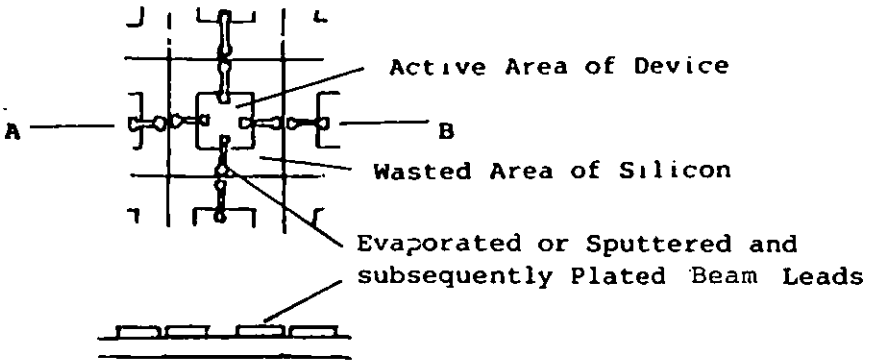
than a few terminals. The controlled collapse connection overcomes these problems by relying on surface tension during the solder reflow process to align the chip [26]. Much work has been done on this technique at IBM and it is a well understood process offering high yields. Though pretesting of die is still a problem, rework is much simpler than for other methods of attachment.

(c) Beam leading [27] - though this technique gives good results, it is very expensive. This is because the leads are formed with the device, consuming valuable wafer area and making subsequent dicing operations difficult (Figure 13(a)). Beam leaded devices may be attached using a back bond or may be flipped (Figure 13(b)).

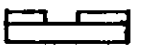
All semiconductor attachment techniques are susceptible to thermal fatigue [28, 29, 33] of the back bond where present, and of the connections if large strains are present without sufficient compliance in the connections. This is a particular problem for flip-chips, or for devices where encapsulation creates stresses, (i.e. plastic packages).

2.6.2 Heat Dissipation

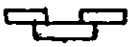
The heat dissipation properties of back bonded devices are quite similar, the primary conduction path being through the material used to bond the device to the substrate. In the case of flip-chips however the primary conduction path is generally through the term-



(i) Cross Section AB Before Dicing Operation

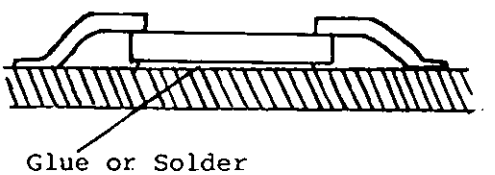


(ii) Cross Section AB After Dicing

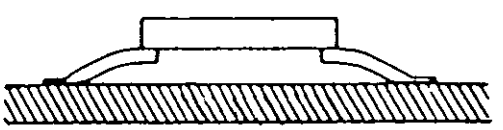


(iii) Cross Section AB After Etching

Figure 13(a) Fabrication of Beam Leads.



(i) Back bonding.



(ii) Flip Chip

Figure 13(b) Back Bonded and Flip Chip attachment of beam lead devices.

Figure 13 Beam Lead Devices - Preparation and Attachment

inations, which means that the thermal conductance is proportional to the number of terminals. Hence power dissipation is severly limited for devices with few terminals, but for large numbers of terminals the conductance approaches that of a continuous bond, with the advantage of conducting heat from the front (i.e. active area) of the die. The flip chip also has the added advantage that the back of the die is available for additional cooling systems e.g. the IBM thermal conduction module [30]. This employs a spring to press a thermally conductive plunger onto the die (Figure 14). This allows significantly higher power dissipations than is possible with back bonded devices because heat is removed from both sides of the die.

2.7 Thermal Strain in SMDs

2.7.1 Modelling Solder Fatigue

It has been shown [31] that if multilayer ceramic chip capacitors were rigidly mounted to ceramic substrates, even moderate temperature excursions would cause fracture of the capacitors. From this it is clear that strain in the solder joint does, and must, occur. If any of this strain is plastic, it will inevitably cause fatigue and ultimate failure of the joint.

In fact, wherever leadless surface mounted components are used solder fatigue is likely to occur as a result of strain caused by differential thermal expansion. This may be either as a result of the difference between the thermal expansion coefficient of the components and that of the substrate, or because of temperature gradients within the system, (i.e. matching expansion coefficients will not always

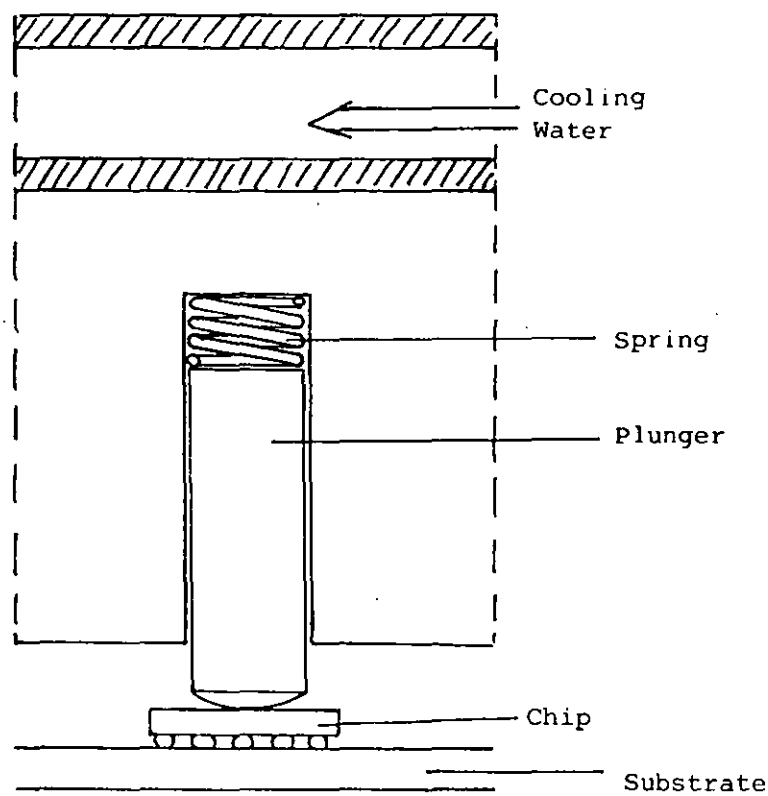


Figure 14 The IBM Thermal Conduction Module.

prevent strain in the system [32].

This situation also arises in the back bond between semiconductor dice and their substrates [33] - hard soldered devices are subject to very high stresses and may crack, but soft soldered bonds are subject to thermal fatigue. Soft soldering is generally taken to mean a process involving temperatures below about 400°C. Hard soldering involves temperatures higher than this. The higher melting point solders are generally much harder at room temperatures than the lower melting point types, giving rise to the above terminology.

Unfortunately most metallurgical research on thermal fatigue is based on tensile or compressive constraint of the material, but in surface mounted components the primary stress/strain is shear. Figure 15 shows a settled (i.e. after several cycles have allowed the curve to stabilise) stress/strain relationship for a metal which does not significantly change its properties over the temperature range of interest. The strain is proportional to temperature, but the origin is arbitrary.

The simplest model for determining the plastic strain ε_p in a solder joint assumes the following:-

(i) Total rigidity of component and substrate. The high Young's Modulus of ceramic materials and silicon dice make this a good approximation for traditional hybrids.

(ii) All thermal strain is absorbed in the solder fillet by plastic deformation, that is that $\varepsilon_p = \varepsilon_t$.

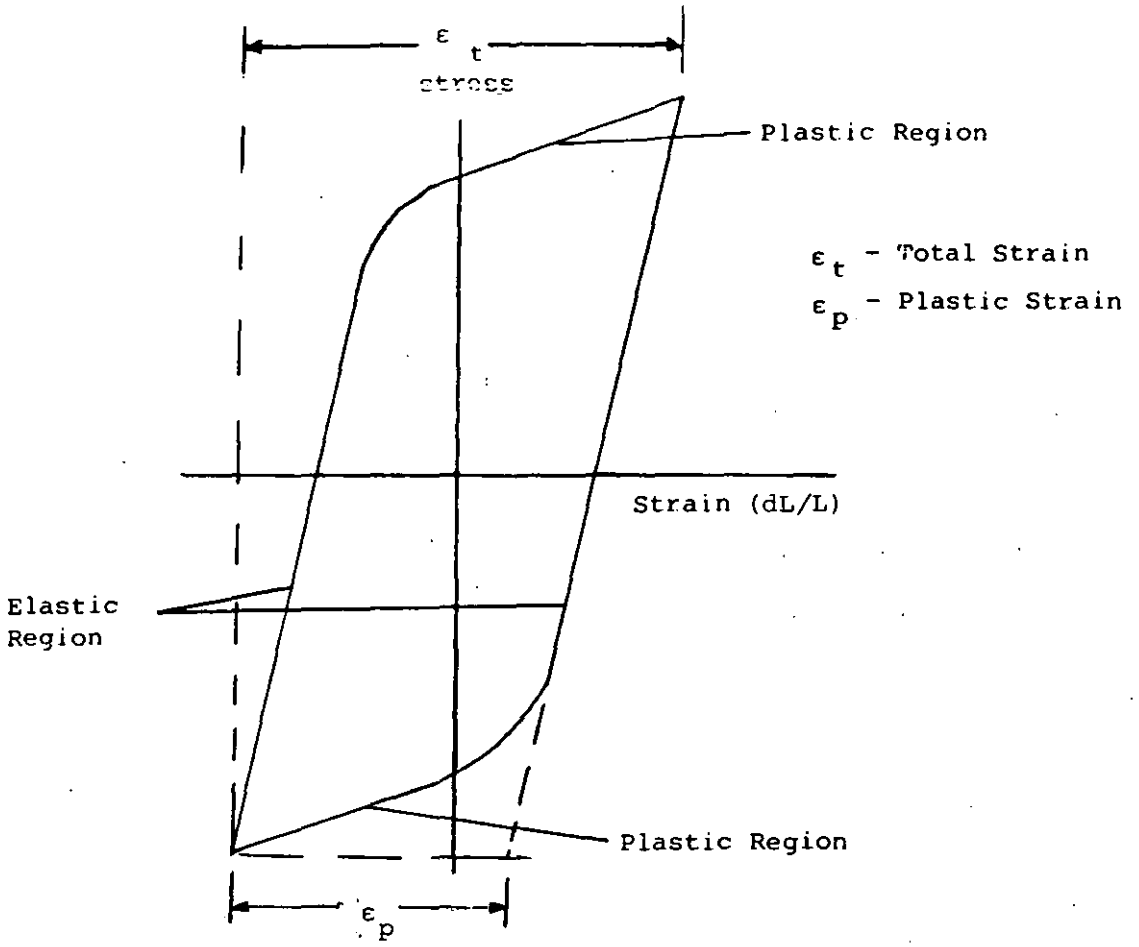


Figure 15 Settled Stress/Strain Cycle.

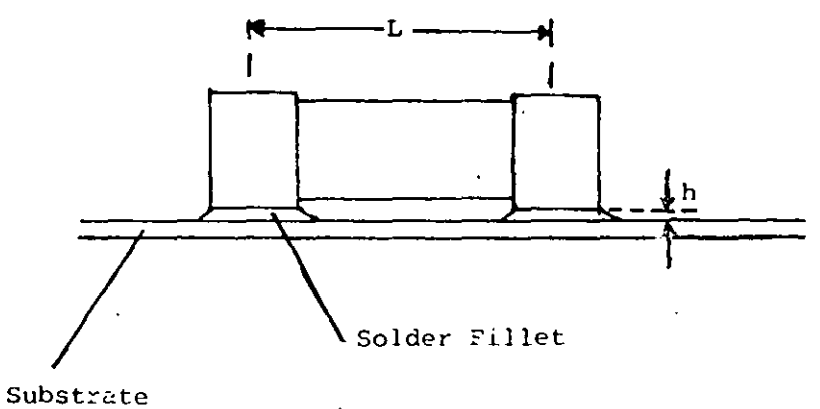


Figure 16 Strain in Solder Fillet

The change in length ΔL between component termination and substrate for a temperature change ΔT is taken to be (Figure 16):-

$$\Delta L = \Delta T \ (\alpha_c - \alpha_s) L/2 \qquad (2)$$

where α_c and α_s are the thermal expansion coefficients of component and substrate respectively.

L/2 is often referred to as the 'distance from the neutral point' (D.N.P.), i.e. that part of the component which remains stationary with respect to the substrate. The idea of a neutral point is only valid for devices with three or more terminals. This is because for two termianl devices the weakest terminal will absorb all the strain.

From equation (1) we obtain the shear strains in the solder fillet as:

$$\varepsilon_p = L\Delta T(\alpha_c - \alpha_s)/2h \qquad (3)$$

where h is the height of the solder joint.

A more general form of equation 2 where temperature gradients exist in the system is:-

$$\Delta L = (\alpha_c \Delta T_c - \alpha_s \Delta T_s) L/2 \qquad (4)$$

where T_c and T_s are component and substrate temperatures.

For well behaved metallurgical systems, i.e. where creep and grain growth do not occur and where the temperature range is sufficiently small for changes in the materials properties to be insignificant, the Coffin-Manson equation is a good model for the fatigue process. This empirical model states that:-

$$\varepsilon_p = mN_f^{-n} \quad \text{or} \quad N_f = (m/\varepsilon_p)^{1/n} \tag{5}$$

where N_f is the number of cycles to failure for a plastic strain per cycle ε_p and m and n are constants. The constant, n, has been found empirically to be 0.5. In a tensile test taken to breakage, $\varepsilon_p = \varepsilon_f$, where ε_f is the fracture strain or ductility and $N_f = 1/4$. This gives:-

$$m = \varepsilon_f,/2 \tag{6}$$

Hence one can write:-

$$N_f = (\varepsilon_f,/2\varepsilon_p)^2 \tag{7}$$

Combining equations 2 and 7 we get:-

$$N_f = [2\varepsilon_f h/L\Delta T(\alpha_c - \alpha_s)]^2 \tag{8}$$

This model, whilst useful for making relative calculations, is inadequate for direct prediction of the life of solder joints because:-

(a) Creep and corrosion fatigue effects mean that the rate of cycling is important (corrosion fatigue is also very dependent upon the

partial pressure of oxygen [34] - hermetic packaging may extend lifetimes in some instances by a factor of ten or more).

(b) The mechanical properties of solder vary between temperature extremes as is illustrated in Figure 17 [35].

(c) The far lower modulus values of composite materials such as fibreglass mean not all strain is absorbed plastically. It has been shown that below room temperature thermal stress in PCB mounted ceramic chip carriers is almost entirely absorbed by bimetallic type bending of the circuit board [36]. This is caused by the rapid increase in the yield stress of the solder as the temperature is reduced.

These factors mean that modifications to the Coffin-Manson relation are necessary. Workers at IBM [37] have empirically produced a model to include these effects:

$$N_f = (f/f_o)^{0.33} (\Delta T/\Delta T_o) (T_{max}) N_o \qquad (9)$$

where (T_{max}) is a temperature factor based on the maximum temperature and N_o is the experimentally determined number of cycles to failure for a cycling frequency f_o and temperature range ΔT_o. This model however is specific to a particular metallurgy of the joints. It has been successfully applied to relative calculations of lifetimes for IBMs flip-chips.

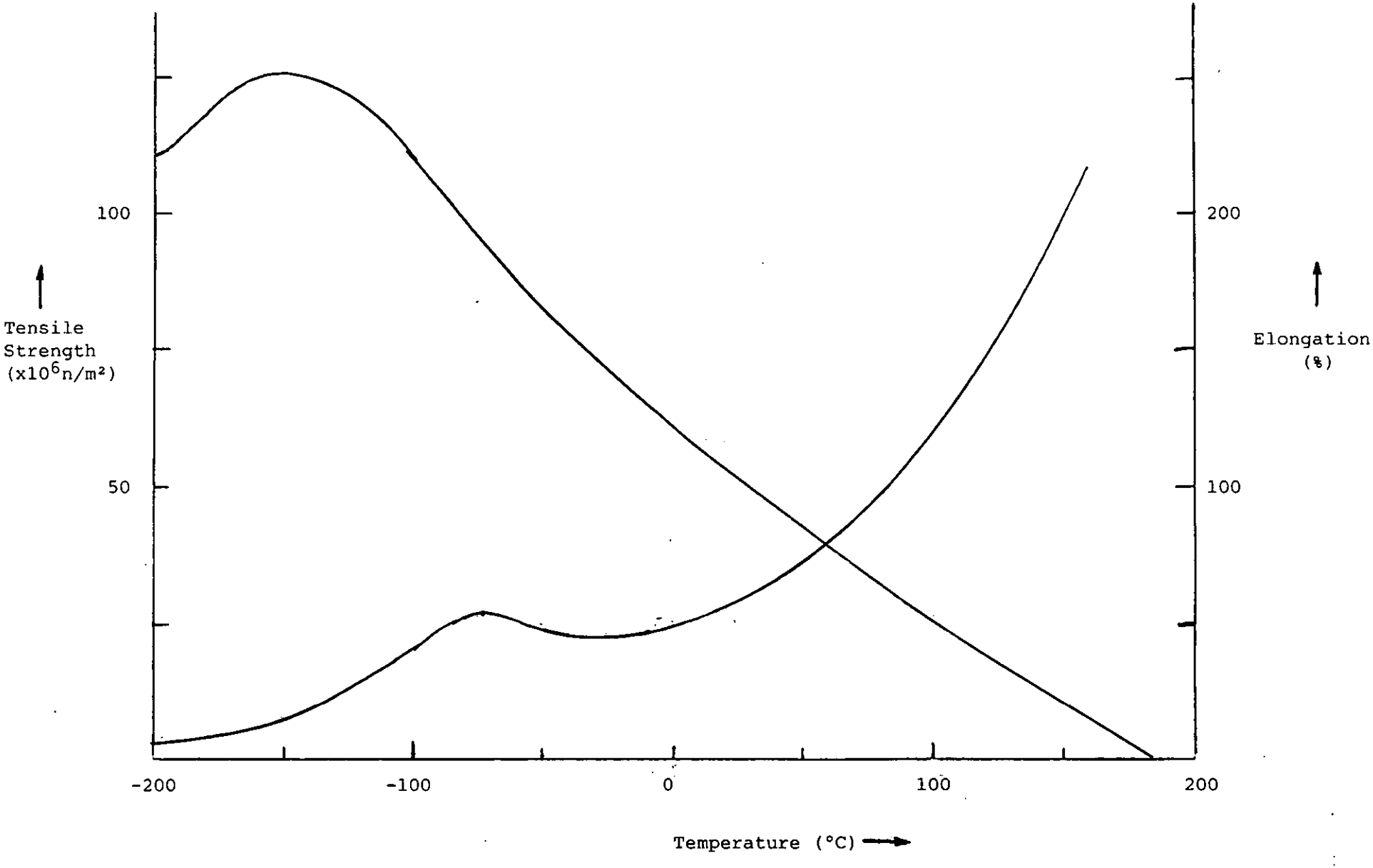


Figure 17 Influence of Tempeature on the Mechanical Properties of 60Sn/40pB Solder.

2.7.2 Minimisation of Thermal Strain

From the above it is seen that strain in the solder joint may be reduced by three methods:

(a) Reduction of L/2 by careful component design/choice.

Where a choice of components exists it is best to choose the shorter fatter design [38]. When designing components it may be possible to bring terminations out on one face rather than at the ends. This may make joint inspection more difficult but is likely to have substantial benefit in long term reliability. Figure 18 shows some possible ways of reducing the DNP for multilayer ceramic capacitors.

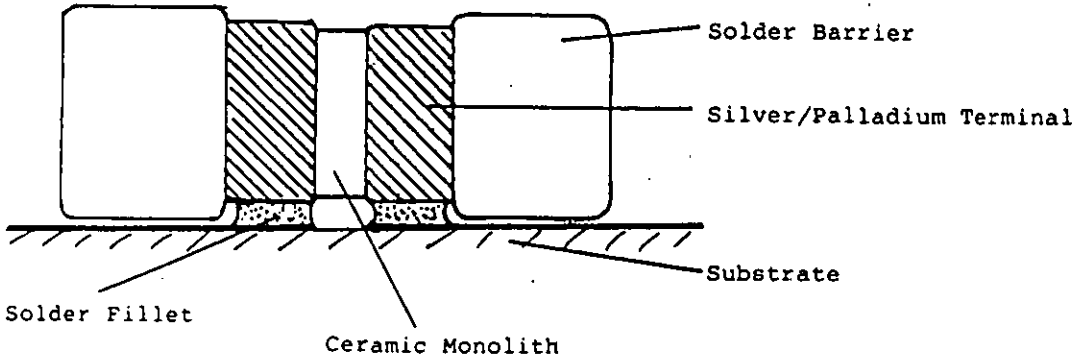
IBM have reduced the DNP for their flip-chip devices by placing the connection pads in an array in the centre of the chip with the active regions of the chip surrounding them [5] (Figure 19). It is possible that this technique also allows easier chip design and shorter on-chip signal paths.

(b) Increasing the height of the solder joint.

The joint height may depend on one of three factors:

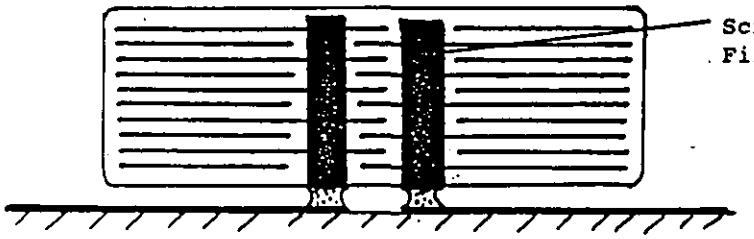
(i) Standoffs on either component or substrate - this gives a consistent and probably sufficient joint height (Figure 20(a)).

Solder Barrier (39)



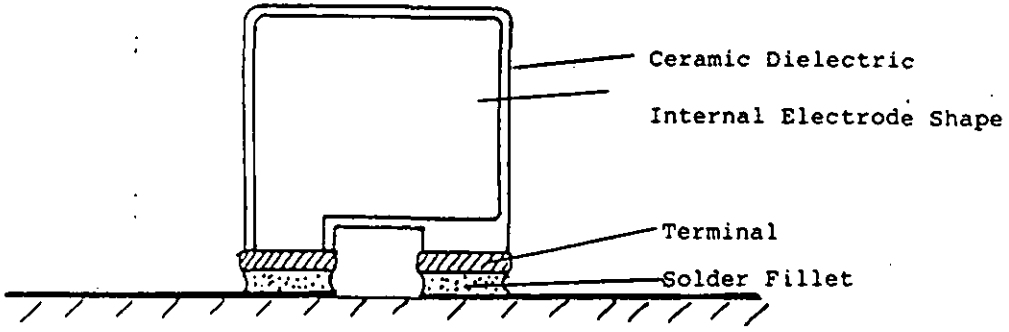
Advantages	Disadvantages
Barrier provides standoff	Joint inspection difficult Increased use of termination material

Vias (40)



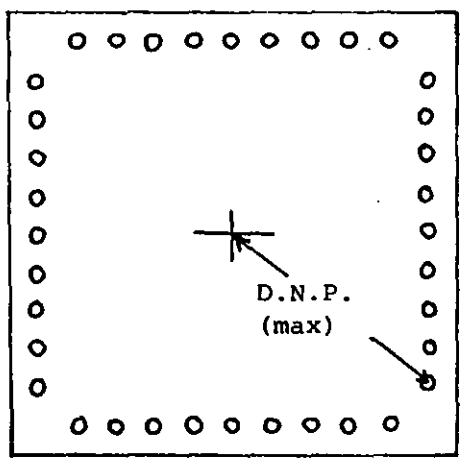
Very effective May improve overall capacitor performance	Requires expensive retooling for manufacture and attachment Alignment and inspection very difficult

Chip Geometry (41)

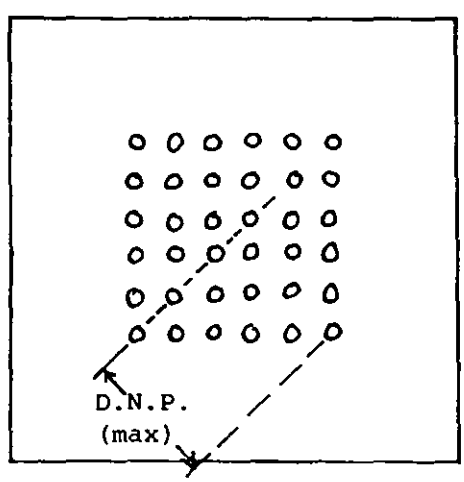


Easy alignment and inspection Reduced use of termination material	Requires expensive manufacturing changes

Figure 18 Methods of Reducing the Distance from the Neutral Position (DNP) for Multilayer Ceramic Capacitors



Conventional Edge Connection



Area Array Connection Sites. The benefits of this technique increase rapidly for higher numbers of connections.

Figure 19 Area Array Connections to Semiconductor Die

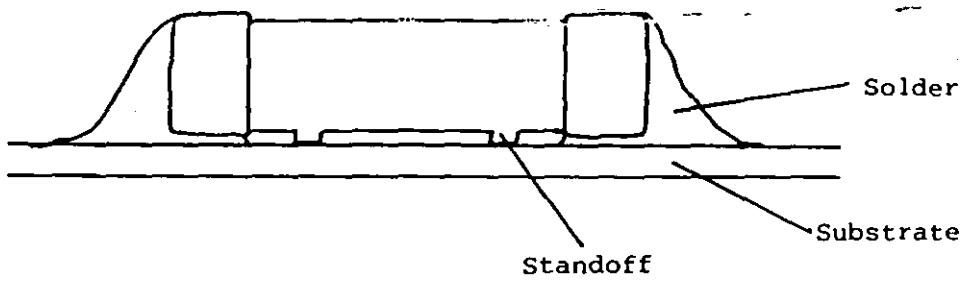
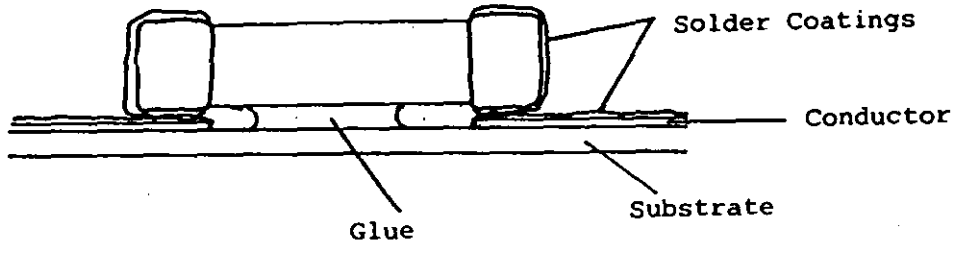
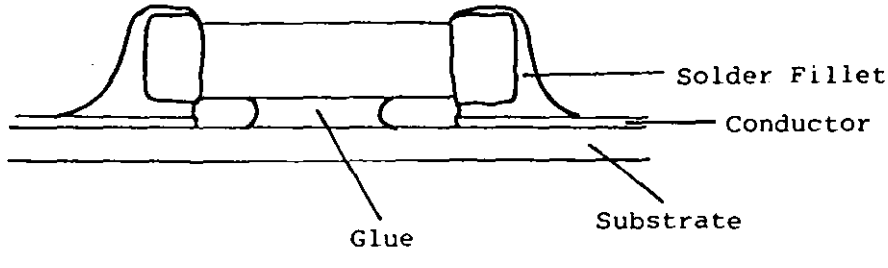


Figure 20(a) Use of Standoffs to Fix Joint Thickness



Before Soldering



After Soldering

Figure 20(b) Use of Glue as a Standoff

Figure 20 Solder Joint Heights Thickness

(ii) Where components are glued to the substrate prior to soldering the joint height is likely to be small and dependant upon the thickness of the solder coating on both the component and the substrate metallisation (Figure 20(b). The joint height may, therefore, be increased by either adding standoffs or increasing the solder coat thickness.

(iii) If the previous two factors are not present then the joint height will be determined by surface tensions within the solder whilst forming the joint. The height is usually adequate for small light chips, but becomes smaller for large heavy chips. Standoffs are likely to be the only way to increase joint height.

(c) Introducing greater compliance to the system.

There are several methods for increasing compliance:

(i) Attachment of short flexible leads to the components [38, 42].

(ii) Using a substrate of greater compliance or with a more compliant surface layer. Two methods used (in STC Exacta) are those of adjoining a thicker resin rich area to composite boards, or adding a special flexible coating to composite boards or other substrates [43] (Figure 21).

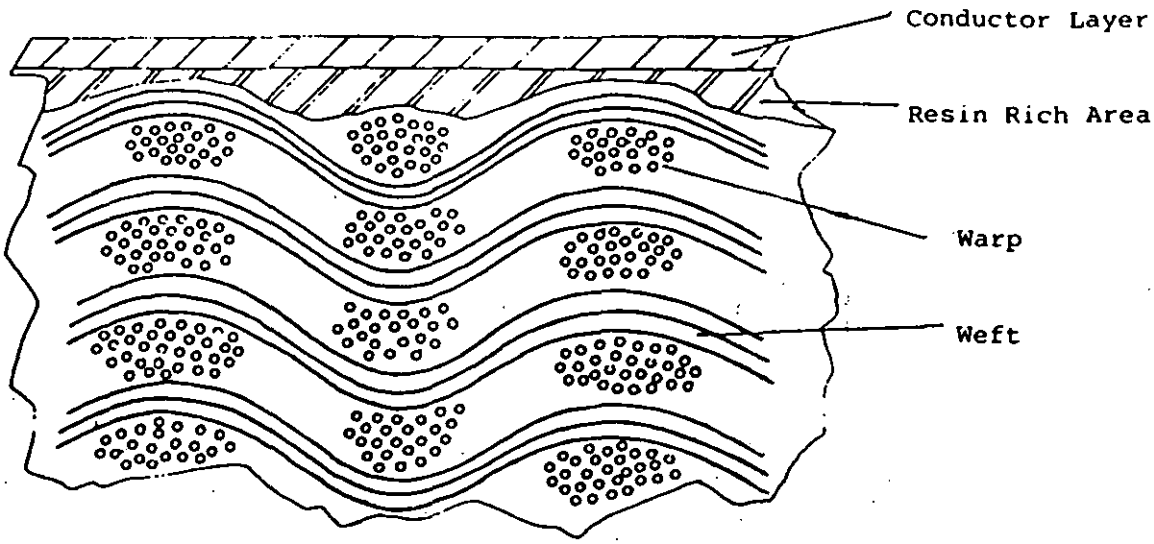


Figure 21(a) Typical Substrate Construction[43]

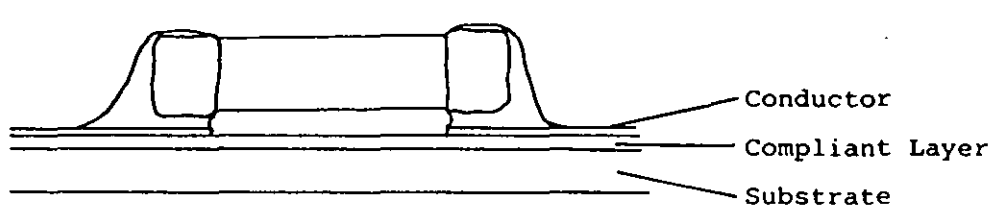


Figure 21(b) Addition of a Compliant Layer

Figure 21 Compliant Substrate

(iii) One suggestion that has been made is to mount larger components using the type of elastomeric conductor often used for LCD displays. This also has the advantage of allowing much higher interconnection densities than conventional chip carrier sockets, whilst retaining the ability to easily change components [44].

The fatigue life may also be improved by careful choice of solder material, e.g. IBM have found benefits in using indium alloys [45].

2.7.3 Methods of Solder Fatigue

So far it has been assumed that all strain occurs parallel to the substrate and is caused by thermal expansion mismatch. However other factors may be present such as:-

(i) Mechanical strain:- Solder fatigue may also be caused mechanically, e.g. by bending of the substrate. This is much easier to model because the properties of the materials involved remain constant. Mechanical fatigue tests (either by twisting components relative to the substrate, or by bending of the substrate) have been used as a technique for predicting relative thermal fatigue lifes, e.g. between different fillet sizes/ geometries [45].

(ii) Where components are glued to a substrate before soldering, the solder joint will be partially constrained perpendicular to the substrate, possibly giving rise to additional thermal fatigue.

2.8 Soldering

2.8.1 Types of Solder

The most commonly used solder electronic production is a eutectic or near eutectic alloy of tin (Sn) and lead (Pb), i.e. 62%Sn/38%Pb. In a eutectic alloy the ratios of the constituent metals are such that, on melting, the solder passes directly from solid to fully liquid, without a 'pasty' range of temperatures (Figure 22). Table 7 lists some other solders and their uses/advantages.

2.8.2 Soldering Techniques

Production soldering falls into two primary categories, wave soldering and reflow soldering. In the former, molten solder is supplied to the joint area whilst the joint is being made. In the latter solder is supplied prior to joint formation and is subsequently heated, often along with the whole assembly, to the soldering temperature. Other techniques such as hand or dip soldering are generally unsuitable for production soldering.

The two most important criteria for the selection of the solder are the melting point and the strength, as these cannot be compensated for. A soft solder (Sn/Pb) does not allow high levels of mechanical stress to build up, so there is less choice of a catastrophic failure due to the fracturing of a component. However, since soft solders undergo a plastic deformation as opposed to elastic deformation, their life is shorter especially if the thermal expansion coefficient mismatch is large.

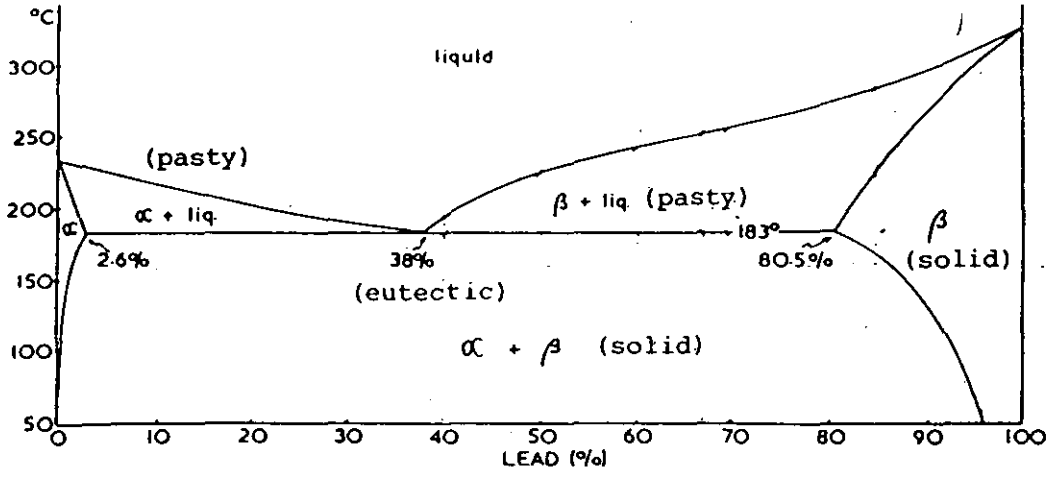


Figure 22 Tin/Lead Thermal Equilibrium Diagram [47]

TABLE 7

SOME SOLDER ALLOYS

ALLOY CONSTITUENTS	MELTING RANGE (C)	ADVANTAGES	COMMENTS
62.5%Sn, 36.1%Pb, 1.4%Ag.	179° Eutectic	Better wetting and higher ductility than Sn/Pb eutectic. Lower leaching of silver containing conductors.	Often referred to as low melting point (LMP) solder.
50%In, 50%Pb	180°-209°	High ductility, good fatigue resistance and low leaching rates.	Prone to corrosion and rapid oxidation.
42%Sn, 58%B	138° eutectic	Very high ductility and fatigue resistance. Low melting point reduces stresses generated by soldering.	Prone to rapid oxidation.
98%Au, 2%Si	698°-1472°	Good wetting of silicon and other semiconductor materials.	Used extensively in semiconductor die attachment.
88%Au, 12%Ge	356° eutectic	Good wetting of gallium arsenide/ phosphide. Low melting point.	Used for gallium arsenide/ phosphide die attach.
80%Au, 20%Sn	280° eutectic	Low melting point.	Used for low temperature semiconductor die attachment.

A major problem with chip components has been the leach resistance of end terminations and the consequent formation of poor solder joints. Soldering with solder paste is also especially prone to intermetallic formation. The importance of attenuating this problem by using more leach resistant palladium-silver material, either by using a nickel barrier layer or end termination or by modifying the solder process can be seen from the dissolution rates given below in Table 8.

TABLE 8 [48]

APPROXIMATE METAL DISSOLUTION RATES IN SOLDER (μm/second)

	200°C	250°C	300°C
Au	5.8	26	-
Ag	3.2	10.3	26
Cu	0.05	1.03	2.6
Pd	0.03	0.03	0.26
Pt,Ni	0	0	0

Au and Ag diffuse rapidly into solder so control of reflow time and temperature is important. A gold concentration of approximately 4% in 60 Sn/40 Pb solder causes a large decrease in joint strength. Intermetallics are brittle and, having a TEC significantly different from that of the solder alloy and metals being joined, they create high stress regions.

Intermetallic formation can be recognised by a rough or frosty appearance to the joints which is due to the altered structure of the

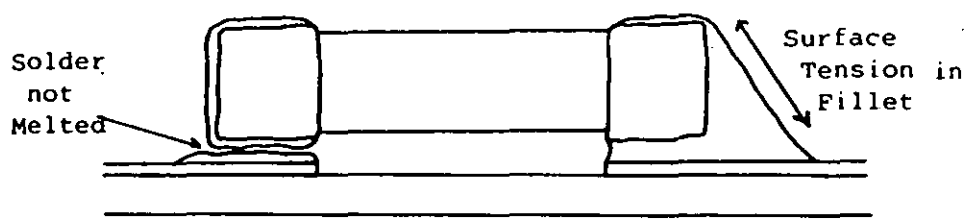
solder. A lack of wetting can also indicate excessive intermetallic formation. Intermetallic formation can be minimised by:-

(a) Minimizing reflow time and soldering temperature by using an intensive preheat at about 150°C.

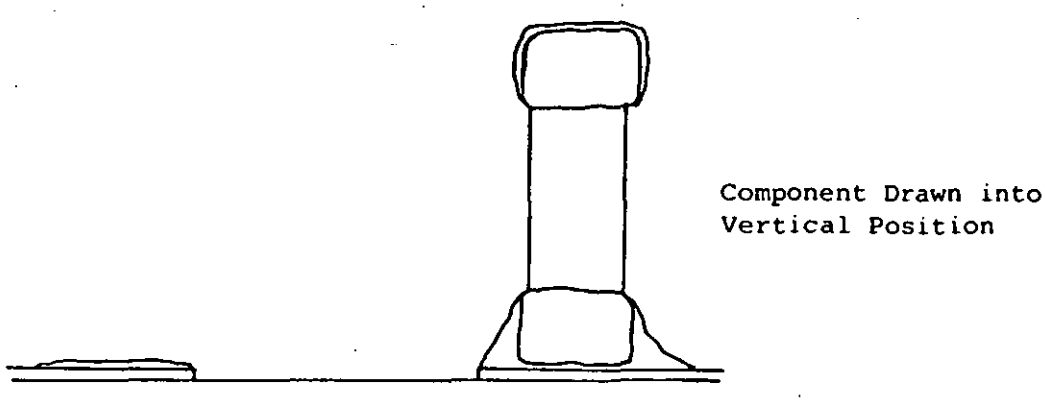
(b) Pretinning components to ensure an adequate tin reserve - otherwise the tin content can be depleted to the point where lead-rich dendrites will precipitate out early in the solidification process, giving the joint a rough appearance.

(c) Modify the reflow profile to include an intensive preheat around 150°C, to minimize reflow time, and use a rapid cooldown to minimize the time spent at elevated temperatures. Make sure the surfaces being joined are solderable and that the correct flux activity is being used.

(d) Use large volumes of solder to reduce the concentration of intermetallics. This may however cause components to float or drift from position if not glued to the substrate before reflow soldering. Another related problem which may occur (variously referred to as tombstoning, drawbridging, wheeling, the Manhatten effect and the Stonehenge effect) is that of surface tensions in the solder tipping a component onto its end. This happens if the solder paste at one end melts and forms a fillet before that at the other (Figure 23).



(a) Intermediate situation.



(b) Final situation.

Figure 23 Tombstoning During Reflow Soldering

To ensure good joints:-

(a) Eliminate sources of precious metals and other contaminants in solder joints, since contaminants reduce fatigue ductility.

(b) Use solder barrier plated parts where appropriate, to prevent precious metals from entering the solder joints.

(c) Limit intermetallic formation by limiting heat exposure.

(d) Provide rapid cooling to minimize grain size. This will enhance fatigue ductility.

(e) Ensure that solderable components and boards are brought to the assembly process.

2.8.3 Wave Soldering

This is the standard production technique for PCBs (Figure 24a), hence its adoption for surface mounting components requires low capital outlay. It is also often the only feasible choice for mixed technology circuits because presupplying solder (for reflow) to conventional leaded components is difficult.

Because the components dip quite deep into the wave, shadowing of trailing components may be a problem. Though careful board design will often avoid this [49], dual wave machines have been developed to overcome this problem. Another development of wave soldering is the immersed wave, (Figure 24(b)), where the soldering operation takes

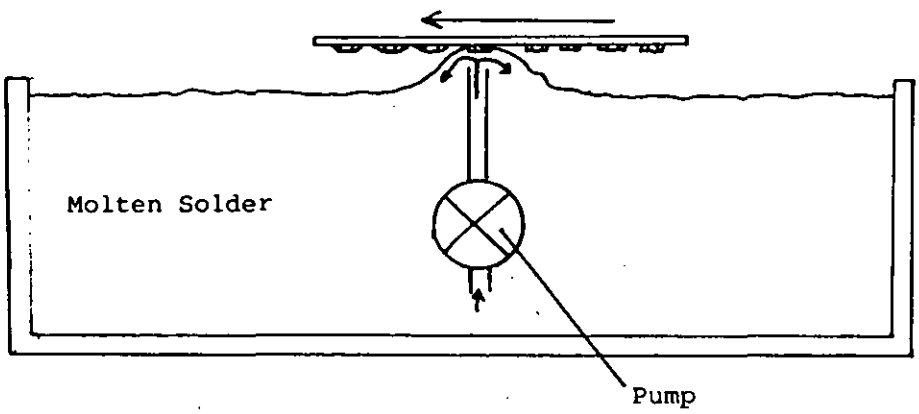


Figure 24(a) Basic Wave Soldering

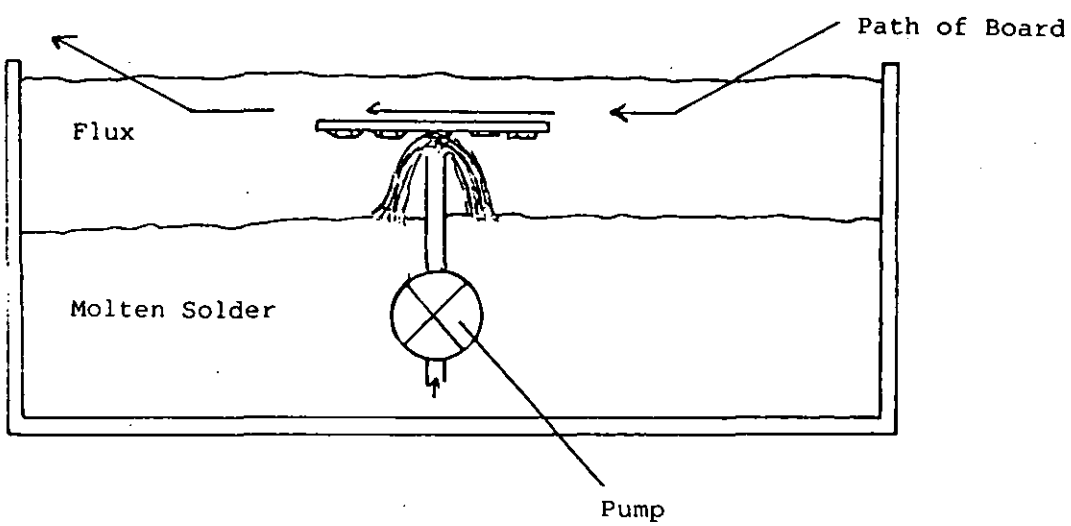


Figure 24(b) Immersed Wave Soldering

Figure 24 Wave Soldering Machines

place under the surface of a flux bath. This gives lower dross formation and allows the easier use of more 'exotic' alloys such as those containing bismuth.

Because of the large quantity of solder within a wave soldering machine it may however be uneconomic to use special solders to improve fatigue life. Another disadvantage of wave soldering is that components must be glued to the substrate prior to soldering.

2.8.4 Reflow Soldering

Solder is normally supplied in one of three ways - by preforms, by screen printing of solder paste, or by syringe placement of solder paste. Understanding solder paste and the soldering process has become very important because increasing board complexity increases the cost of the rejects due to poor soldering; rework and QC can account for up to 50% of the assembly operation cost because of its very labour intensive nature. Solder paste for attaching surface mount components must be consistent with the users processing conditions and the performance and reliability specifications of the product. Other methods of supplying solder to the joint area include dip or electro tinning, or, as in the IBM flip chip, by evaporation.

The solder is subsequently melted by one of several methods:

(a) Hot plate reflow - the substrate is placed on a plate heated to well above the soldering temperature. Since conduction is relied upon for the heat to get to the joint area, this technique is

unsuitable for organic substrates because of their low thermal conductivity. It is also only useable for single sided assemblies.

(b) Oven reflow - heat reaches the joint primarily by convection. This is a slow technique, exposing components to high temperatures for an extended time.

(c) Infra-red heating - this is a rapid technique, but often the components themselves shield their terminations from the heat source, increasing soldering time, the risk of thermal damage to the components, or possibly causing incomplete soldering.

(d) Laser heating - the heat may be precisely aimed where required, reducing the risk of overheating components, but it is a slow (200 to 400ms per joint) and expensive process.

(e) Hot gas - a jet of hot gas can provide rapid localised heating - very useful for reworking.

(f) Vapour phase or condensation soldering - this technique, which relies on the condensation of a saturated vapour upon the workpiece, provides rapid heating to the soldering temperature without the possibility of overheating. All components are however exposed to the full soldering temperature.

(g) Liquid phase soldering - heat is supplied rapidly by conduction from a liquid stable at the soldering temperature, e.g. a

perfluoropolyether. Two ways of applying the liquid to the joint exist - either immersion in a tank, or the use of a conventional wave soldering machine filled with the liquid.

(h) Induction heating - eddy currents induced by a HF field can rapidly heat metallic objects, but components are easily heated and damaged as well.

(i) Resistance heating - a high electric current is passed through the parts to be soldered giving rapid resistive heating. However this is also a slow process due to the limited number of joints that can be simultaneously soldered. Variation in contact resistance may also affect the heat input, making the process unpredictable.

2.9 Summary

It has been seen that there are considerable advantages to be gained from the adoption of surface mounting technology. Further, the necessary component packages and substrates are available and techniques exist for soldering these assemblies.

There are, however, some disadvantages associated with this technique. Principally these are the hazard of thermal stress fatigue failure of the solder joints in this type of assembly. Methods are available for reducing the thermal stresses but will not entirely eliminate them and may further add to the cost of an assembled circuit. It is, therefore, important that a detailed understanding of the behaviour of solder joints is obtained.

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CHAPTER THREE - TEST PROGRAMME

The program was chosen so that the most relevant tests are applied to each component type and to gain the maximum amount of information without unnecessary duplication of tests. For example, because the thick film resistor chips and zero ohm jumper chips are structurally identical, each test is applied to one or other of these component types, but not to both. The program is shown in Table 9 and the numbers in the table indicate the number of components in each test group.

Table 9. Tests on surface mounted components.

Component type	Size	Power cycle	Temperature cycle (°C)					Mechanical cycle			Damp heat	
			−55 to +5	−55 to +65	−55 to +85	−55 to +110	−55 to +125	600/hour	30/hour	1/hour	Steady state	Cyclic
Thick−film on alumina resistor	1206	128						128	128	64	128	128
Thick−film on alumina 'Zero−ohm' jumper chip	1206		128	128	128	128	128					
	0805				120							
Multilayer ceramic capacitor	1812				128		128		128	128	128	128
	1206						128				256	128
Thin−film potential divider	SOT−23	80										
Jumper	SOT−23			120	120		120					

CHAPTER FOUR - TESTING TECHNIQUES

4.1 Power Cycling

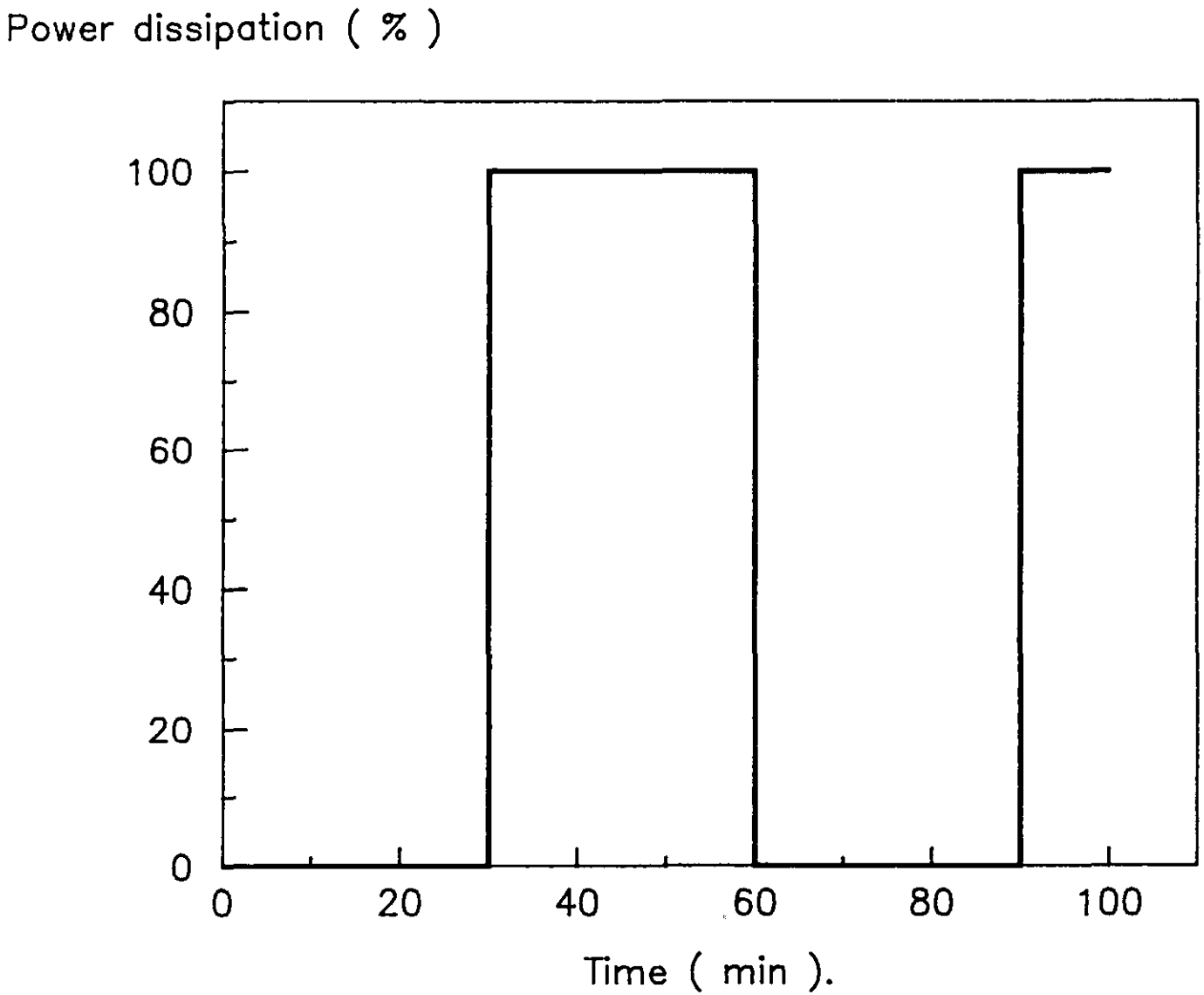
Power Cycling tests are most representative of the stresses encountered in normal working conditions and are therefore considered the best method for predicting solder joint fatigue life. The test cycle is 30 mins. at full power, followed by 30 mins. at zero power (Figure 25). These dwell periods are chosen to allow most of the thermal stress (>90%) to be relieved by creep in the solder fillet.

4.2 Thermal Cycling

Temperature cycling tests are often used in component test schedules, but the applicability of common cycle profiles (e.g. -55 to +125, -40 to +110 etc.) for surface mounted components required investigation.

An examination of the effect of peak cycle temperature (T_{max}) has therefore been undertaken. This has involved temperature cycling of coupons of components over the five ranges -55°C to T_{max} where T_{max} is +5°C, +65°C, +95°C, +110°C and +125°C. The temperature cycles were all of 120 mins. duration (12 cycles per day), with a rate of change of temperature of 3.5°C/min. (Figure 26). Most of these tests were conducted using a LEC CL10HB. This was interfaced to a PET microcomputer to allow full control of test profiles (Appendix 1). Some testing was also carried out at STC Leeds and STL Harlow.

Figure 25. Power cycle test profile.



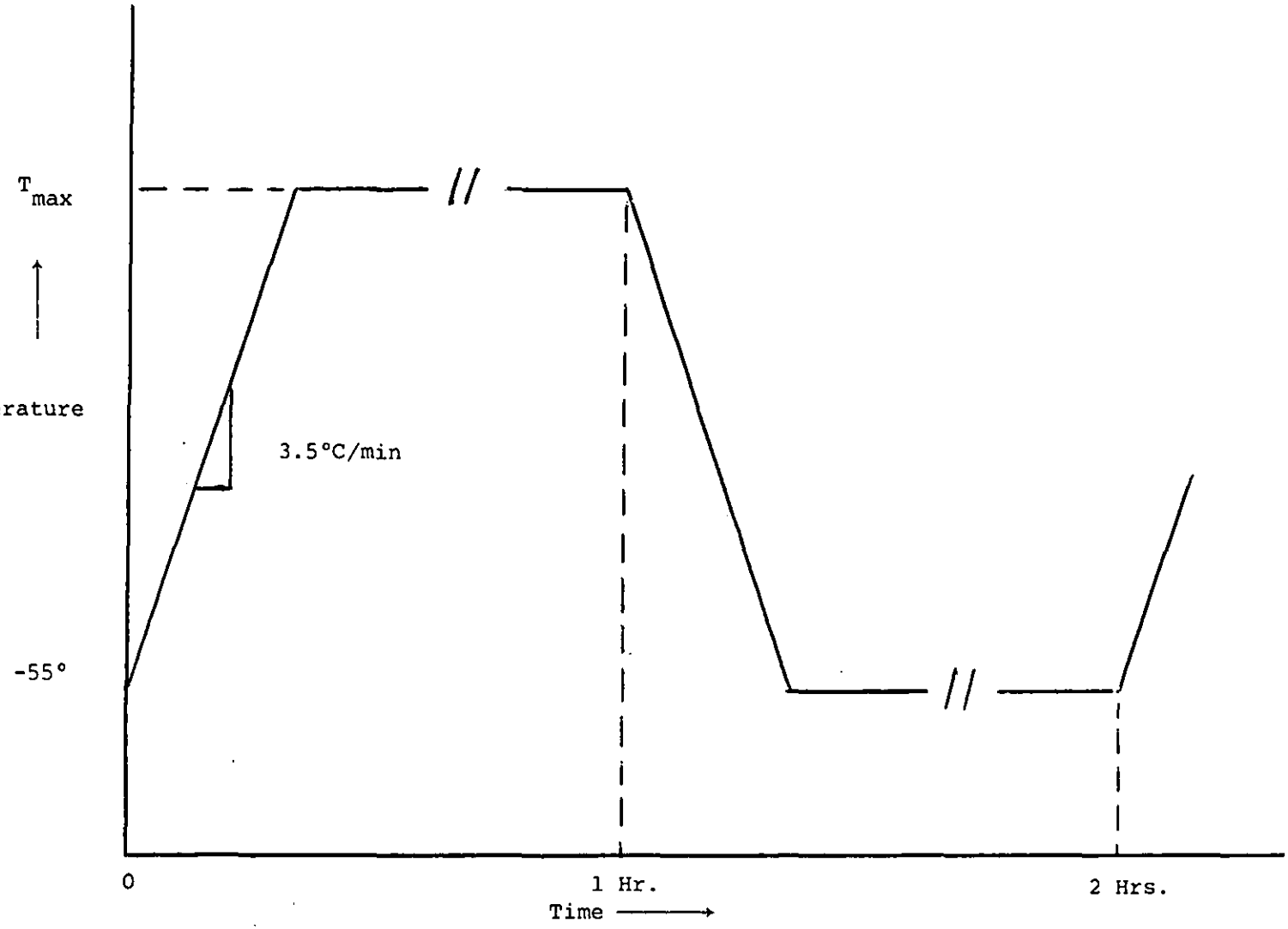


Figure 26 Temperature cycle test profile

4.3 Mechanical Cycling

Mechanical cycling allows the application of relatively large levels of strain isothermally, i.e. without changing the properties of the materials tested. Mechanical cycling therefore offers a technique for consistent, highly accelerated, fatigue testing.

The following calculations of the strain caused by board bending make two assumptions:-

(i) that the board is bent to a uniform radius;

(ii) the cross-section of the board is unaltered by bending.

The strain at the surface of the board may be calculated as follows:-

$$r_1 = (1 + \varepsilon)r_0 \text{ or } \varepsilon = r_1/r_0 - 1 \qquad (11)$$

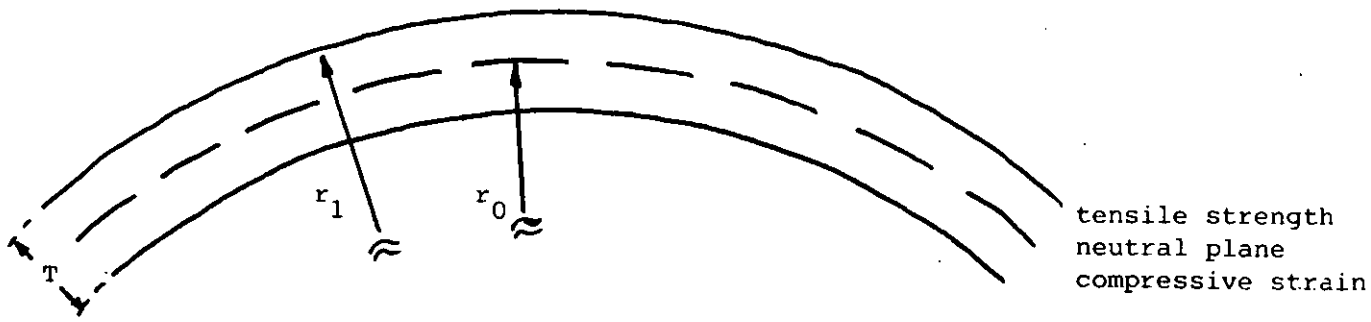
Where ε is the surface strain and r_1 and r_0 are the radii of curvature of the surface and the neutral plane respectively (Figure 27(a)). One also knows that:-

$$r_1 = r_0 + \tfrac{1}{2}T \qquad (12)$$

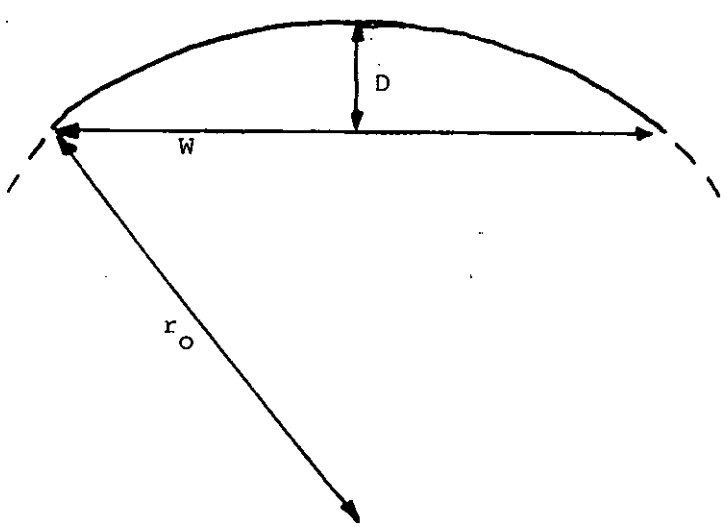
Where T is the thickness of board.

Substituting (12) into (11) one obtains:-

$$\varepsilon = (r_0 + T/2)/r_0 - 1 = T/2r_0 \qquad (13)$$



(a) Strains in a board



(b) Deflection of a board.

Figure 27 Board Bending Diagrams.

The deflection D for a board length L to give radius of curvature r_0 may be calculated by (Figure 27(b)):-

$$D = r_0 - \sqrt{r_0^2 - (L/2)^2} \qquad (14)$$

From this one may obtain the deflection for a required strain:-

$$D = T/2\varepsilon - \sqrt{(T/2\varepsilon)^2 - (L/2)^2} \qquad (15)$$

The strain versus deflection values from equation (15) have been calculated and plotted in Figure 28 for a 1.6 mm thick board with a width of 150 mm. The levels of strain indicated are typical of those occurring during temperature cycling, and a machine has been designed and built to apply these levels of strain to printed circuit boards. A photograph of the machine is shown in Figure 29.

Three designs were considered for the board bending machine:-

(i) Using three bending bars

(ii) Using four bending bars

(iii) Using a curved block of the required radius.

Method (iii) guarantees that the board is accurately bent to the required radius but lacks flexibililty. Method (ii) was therefore chosen as the best compromise between accuracy and flexibility. Figure 30 shows the more uniform bending moment generated by four point bending compared with three point bending. Tests with strain gauges have confirmed the levels of strain obtained agree with those calculated..

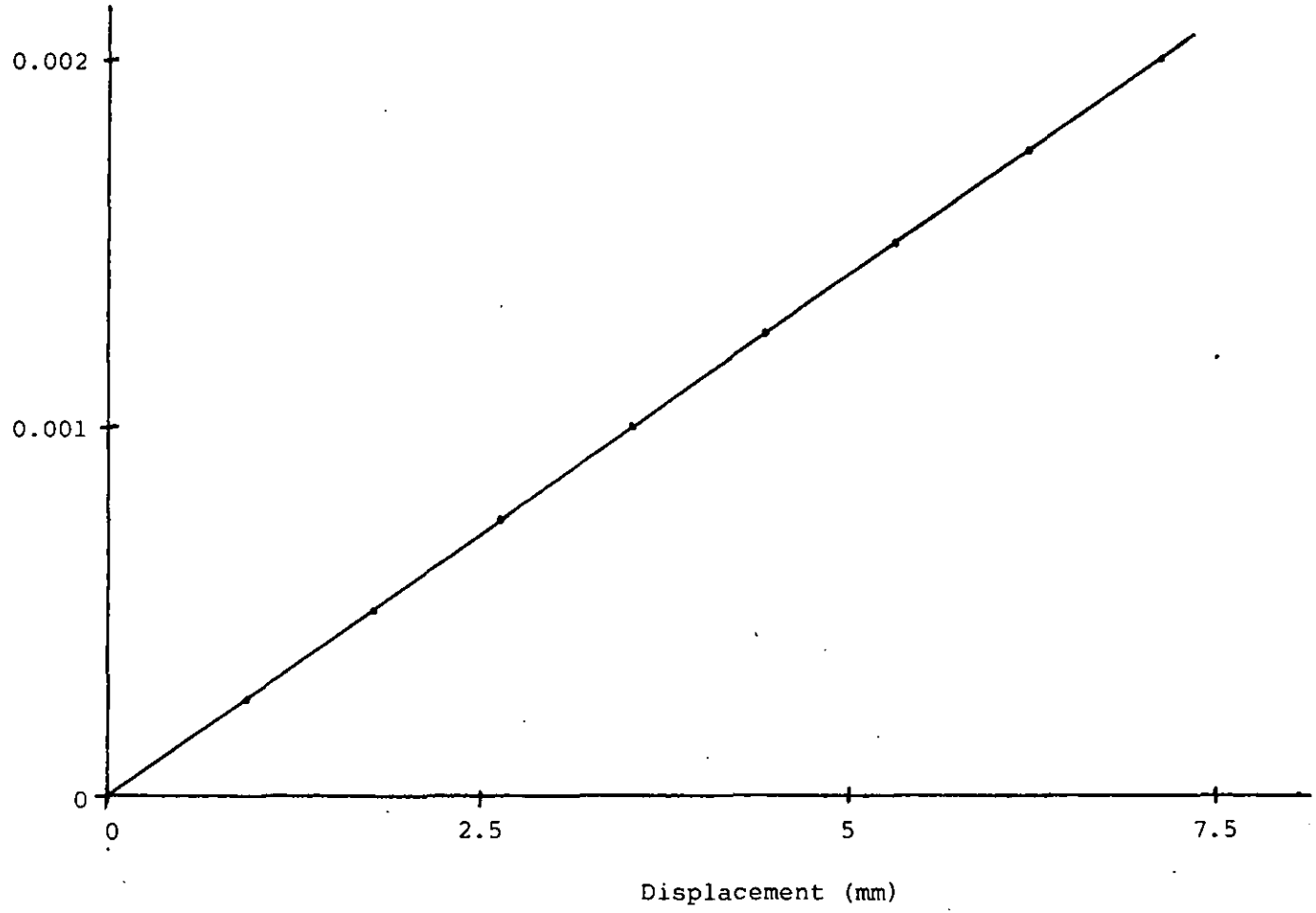


Figure 28 Strain/Displacement for 1.6 mm thick board 150 mm wide.

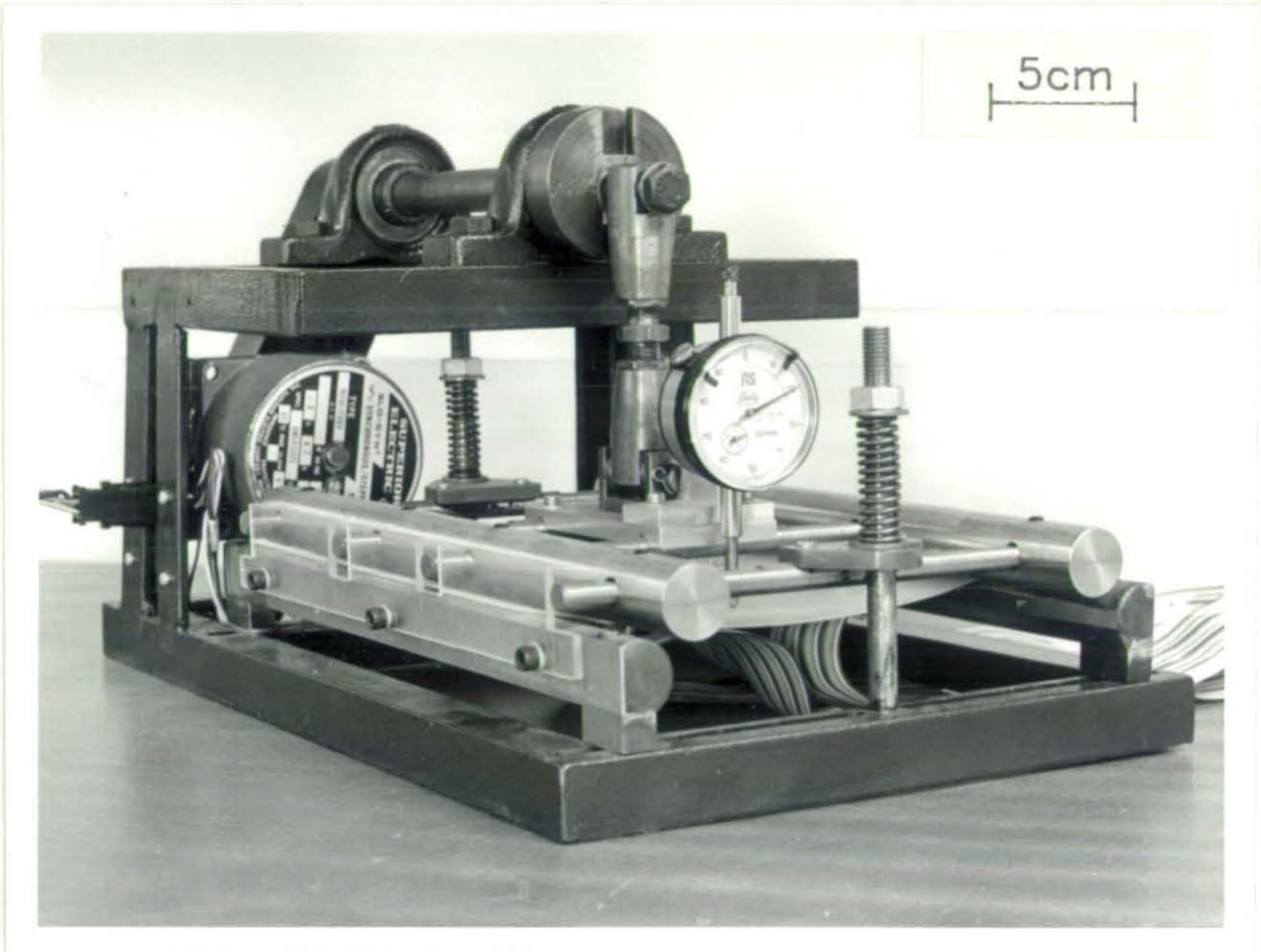
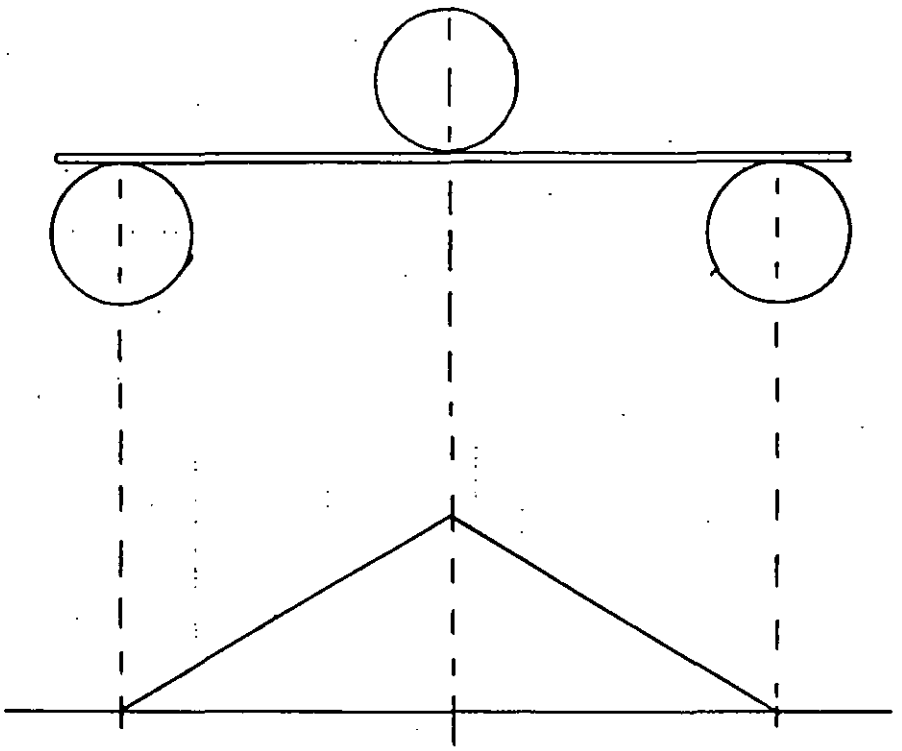
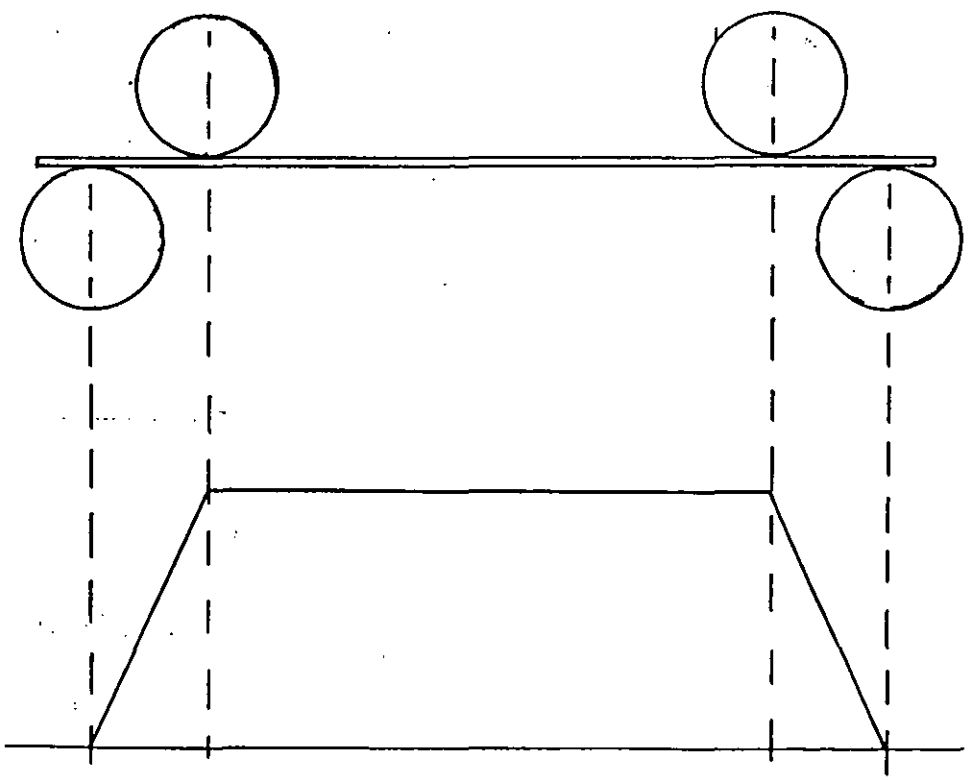


Figure 29 Board Bending Machine



3 POINT BEND TEST AND BENDING MOMENT



4 POINT BEND TEST AND BENDING MOMENT

Figure 30 Comparison of Bending Moments in 3 Point and 4 Point Bending Tests.

The machine is controlled by a PET microcomputer allowing a choice of any test waveform up to 600 cycles/hour (Appendix 1).

4.4 Damp Heat

Two types of damp heat test have been undertaken:-

(a) Steady state (85°C/85%RH)

(b) Combined temperature cycling and damp heat test (5 cycles -55 to +125°C +21 days 85°C/85% RH).

The steady state tests were undertaken because it is known that high levels of humidity may cause component degradation through the mechanisms of corrosion, migration and ionic conduction. It was therefore felt that an investigation of whether these presented any particular problems with the technology of surface mounting was necessary.

The combined tests were undertaken in order to investigate any synergistic effects between the two types of test.

The equipment used for the damp heat tests was a Fisons model 090 cabinet and the temperature cycling tests were conducted with the equipment described in Section 4.2.

4.5 Sectioning

Sectioning is an important technique for identifying the cause and severity of cracks in the solder fillet. The method used

for preparing specimens is as follows:-

(a) An area of PWB is sawn from the test coupon with the specimen attached.

(b) The specimen is mounted in Struers Epofix cold curing epoxy resin. Vacuum impregnation is used to ensure penetration of the resin into any cracks.

(c) The specimen is wet ground using successively finer grades of silicon carbide grinding paper and then diamond polished.

CHAPTER FIVE - TEST COUPONS

5.1 Introduction

A series of test coupons have been designed for the placement of four package styles in different configurations - the small outline transistor (SOT-23) and chip components in sizes 0805, 1206 and 1812 (Figure 31).

In all cases pad geometry, solder mask windows and component spacings have been designed to comply with STC design rules (Figure 32) [1,2].

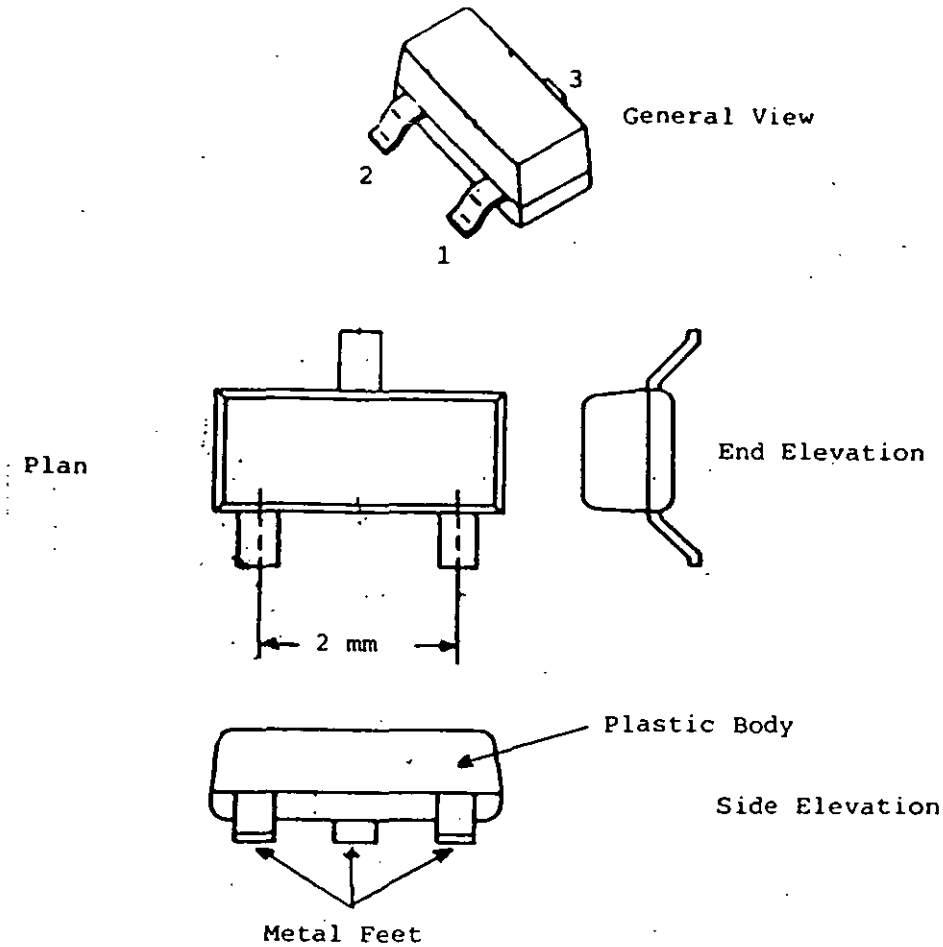
All coupons, except the thermal mapping coupon are designed to allow connection to the automatic measuring systems with 40 way ribbon cables and B.S. 9525-F0023 style connectors.

The coupons were assembled at STC Leeds. The assembly process is hand placement onto dispensed glue dots (Epotek H70E/4 or Amicon D-124F) followed by double wave soldering using Frys 63Sn/37Pb solder.

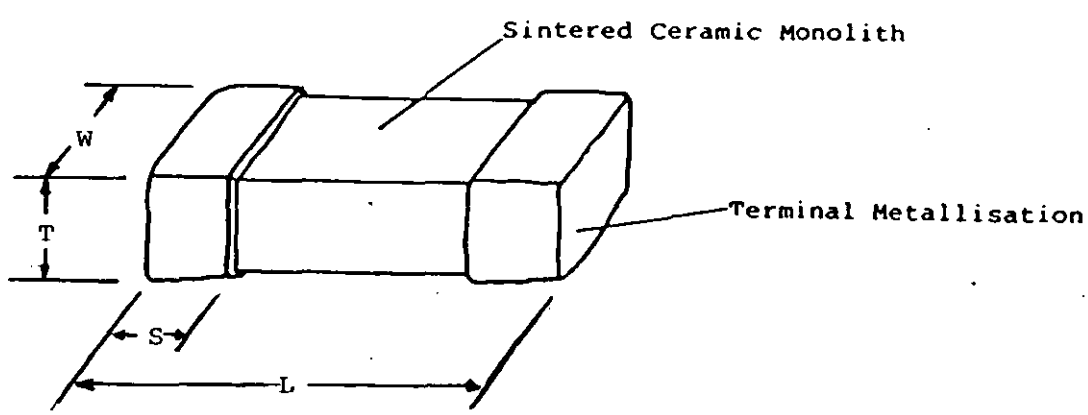
5.2 Components

The eight component types used in the tests are listed in Table 10. All chip components have nickel barrier layers to prevent solder leaching problems.

The 0805 and 1206 jumper chips and the 1206 resistor chips are fabricated using thick film techniques on an alumina substrate and the



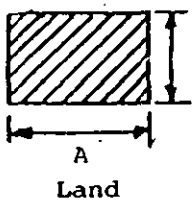
a) SOT-23



	L	W	T	S
0805	2	1.25	0.45	0.25
1206	3.2	1.6	1.25	0.5
1812	4.57	3.2	2.03	0.5

b) Chip

Figure 31 Component Packages



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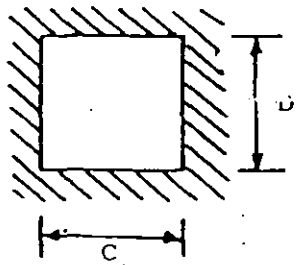
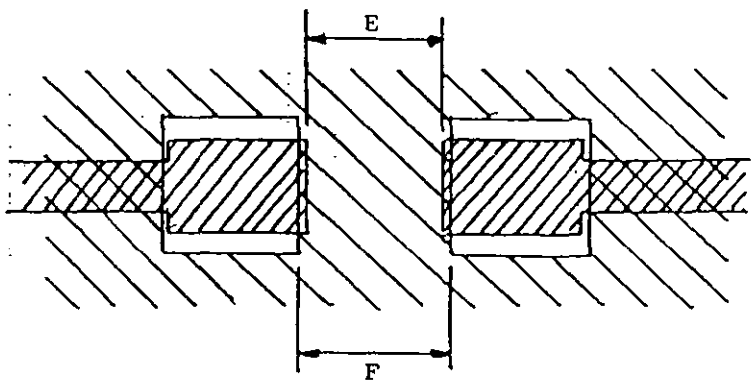
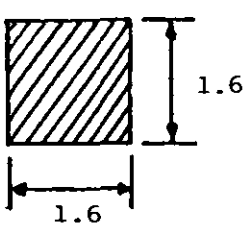


Solder Resist Aperture

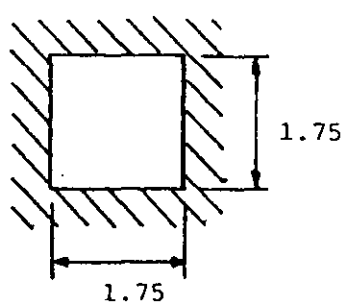


	A	B	C	D	E	F
0805	1.6	0.9	1.5	1.6	0.7	1.1
1206	1.8	1.2	1.8	1.8	1.8	1.9
1812	1.9	2.4	2.0	3.3	3.0	3.0

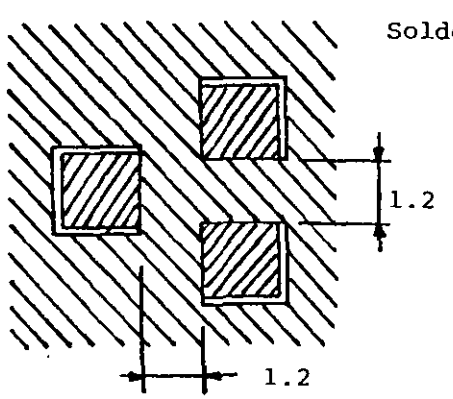
a) Chip



Land



Solder Resist Aperture



b) SOT-23

Figure 32 P.C.B. Conductor Layout Patterns (dims. in mm.)

Package Style	Component Type	Component Value	Tolerance	Manufacturer	Part No.
0805	JUMPER	< 50 mΩ	-	ROHM	MCR10JPW
1206	JUMPER	< 50 mΩ	-	ROHM	MCR18PJW
1206	RESISTOR	200 Ω	± 5%	DALE	CRCW1206-201J
1206	CAPACITOR	4.7 nF	± 5%	STC	X1206J-50-472J
1206	CAPACITOR	0.68 > 39 nF	± 10%	CORNING	CC1206X7R
1812	CAPACITOR	100 nF	± 20%	CORNING	CC1812X7R104M50LB
SOT23	JUMPER	< 50 mΩ	-	MICRODEVICES	HC659
SOT23	POTENTIAL DIVIDER	2 x 100 Ω		MICRODEVICES	HC661

Table10 Components for Tests

capacitors are multilayer, ceramic dielectric types. The 1206 size (STC) capacitors are of conventional co-fired construction using a noble electrode material (silver/palladium), whereas the 1206 and 1812 size Corning capacitors are fabricated by the technique of creating hollow electrode sites in the ceramic dielectric which, after firing, are filled with a non-noble (lead) electrode material (Appendix 2). The absence of silver in the Corning capacitor's electrodes is expected to improve reliability, particularly under humid conditions. This is because silver tends to migrate in the presence of moisture and electric fields.

5.3 1206 Resistor/Capacitor Coupons

This coupon (Figure 33) is designed to accept 128 chip components and was designed to allow machine assembly by STC Leeds, but programming the machine was uneconomical for such a small production run.

5.4 1206 Jumper Coupons

The series connection of components gives a more sensitive test for overall resistance changes. The very low resistance of individual jumpers (< 50 mΩ) combined with the resolution of the instrument used (1 mΩ) prevent highly accurate measurement of individual jumpers. The coupons allow both measurement of chain resistances and also individual jumper resistances.

The original coupon design (Figure 34) allows the placement of 128 jumper chips connected in 8 series chains of 16 and was designed for machine placement. The overall size is 152 mm x 298 mm.

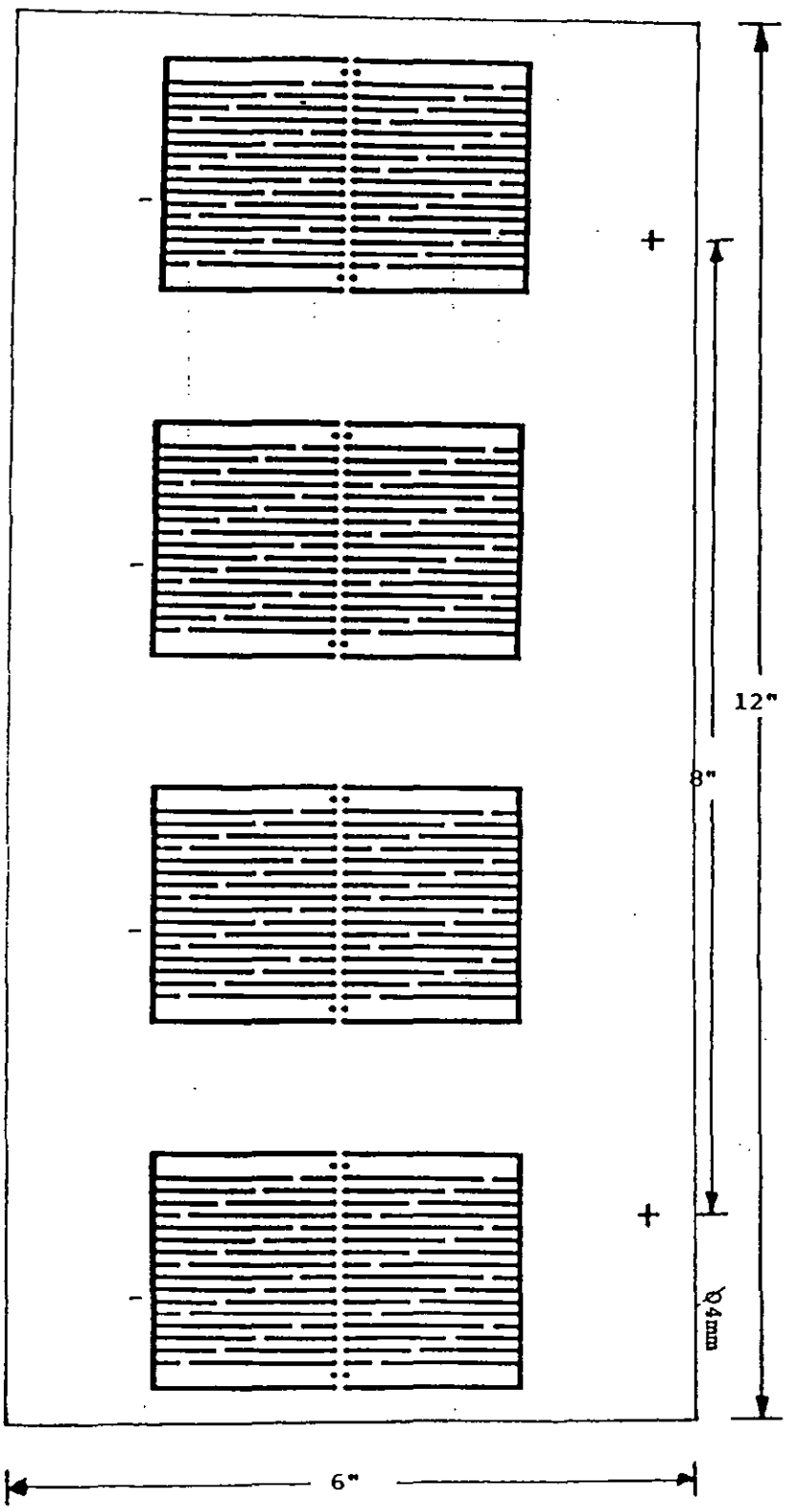


Figure 33 1206 Resistor/Capacitor Coupon

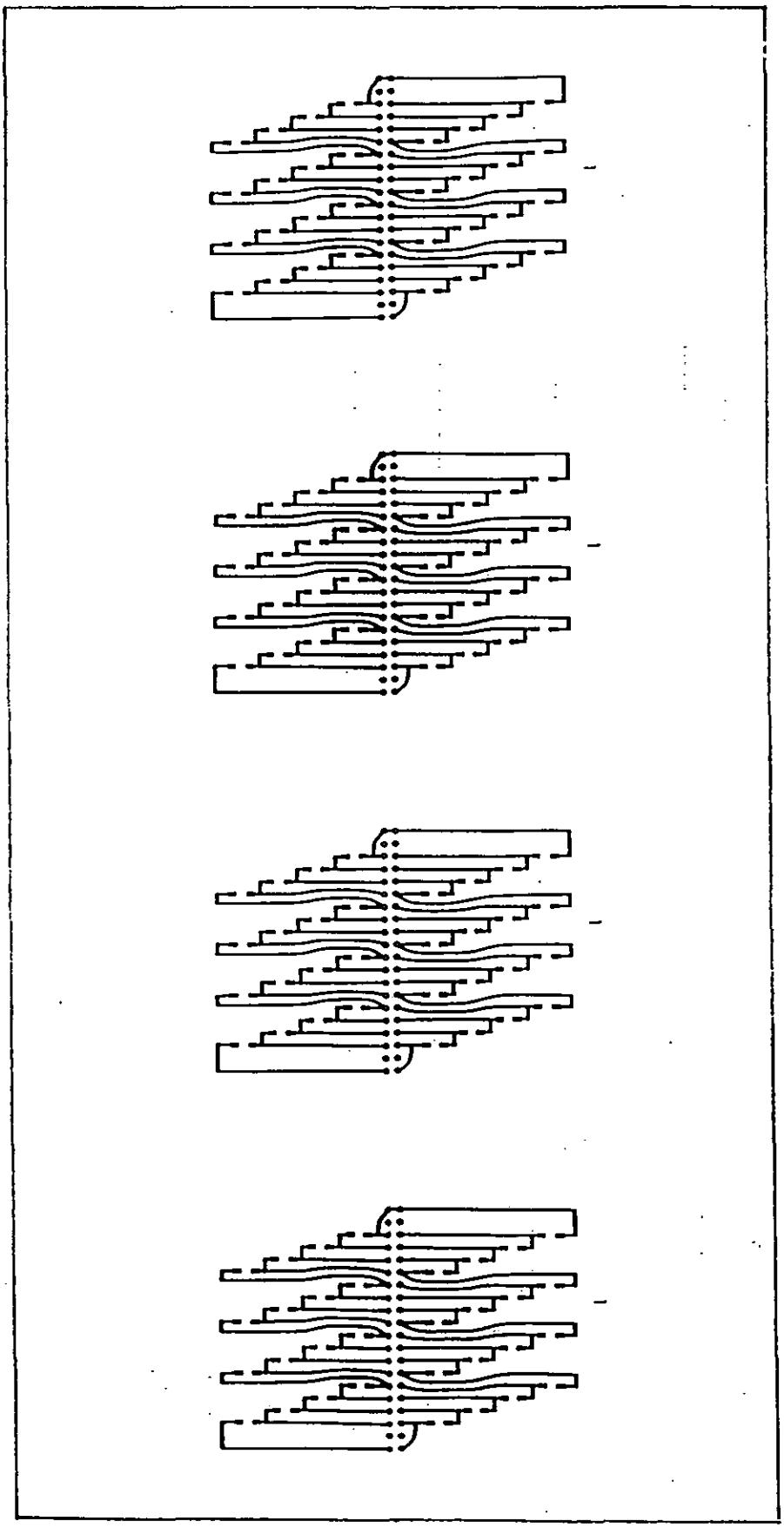


Figure 34 1206 Jumper Coupon

The coupon has been redesigned (Figure 35) to allow easier connection to the measuring system and allows the placement of 120 chips connected in 6 series chains of 20. The size has also been reduced to 152 mm x 165 mm.

5.5 0805 Jumper Coupons

This coupon (Figure 36) is very similar to the revised 1206 jumper coupon. That is, it contains 6 series chains of 20 jumpers. This coupon however is larger (152 mm x 216 mm) than the 1206 coupon to allow bend testing.

5.6 1812 Capacitor Coupons

This coupon (Figure 37) is based on the 1206 resistor/capacitor coupon, but uses the TEP-1E 8U card size (222 mm x 195 mm).

5.7 SOT-23 Jumper Coupons

Two coupons have been designed for SOT-23 jumper chips (Figures 38 and 39) allowing placement of the chips both along the board length, and across the board length. This is to allow board bending tests on components in both orientations.

The coupons each contain 6 chains of ten jumpers, connected in series alternately using pins 1 and 3 and pins 3 and 2 (see Figure 31). Both designs use an 8U card size (222 mm x 195 mm).

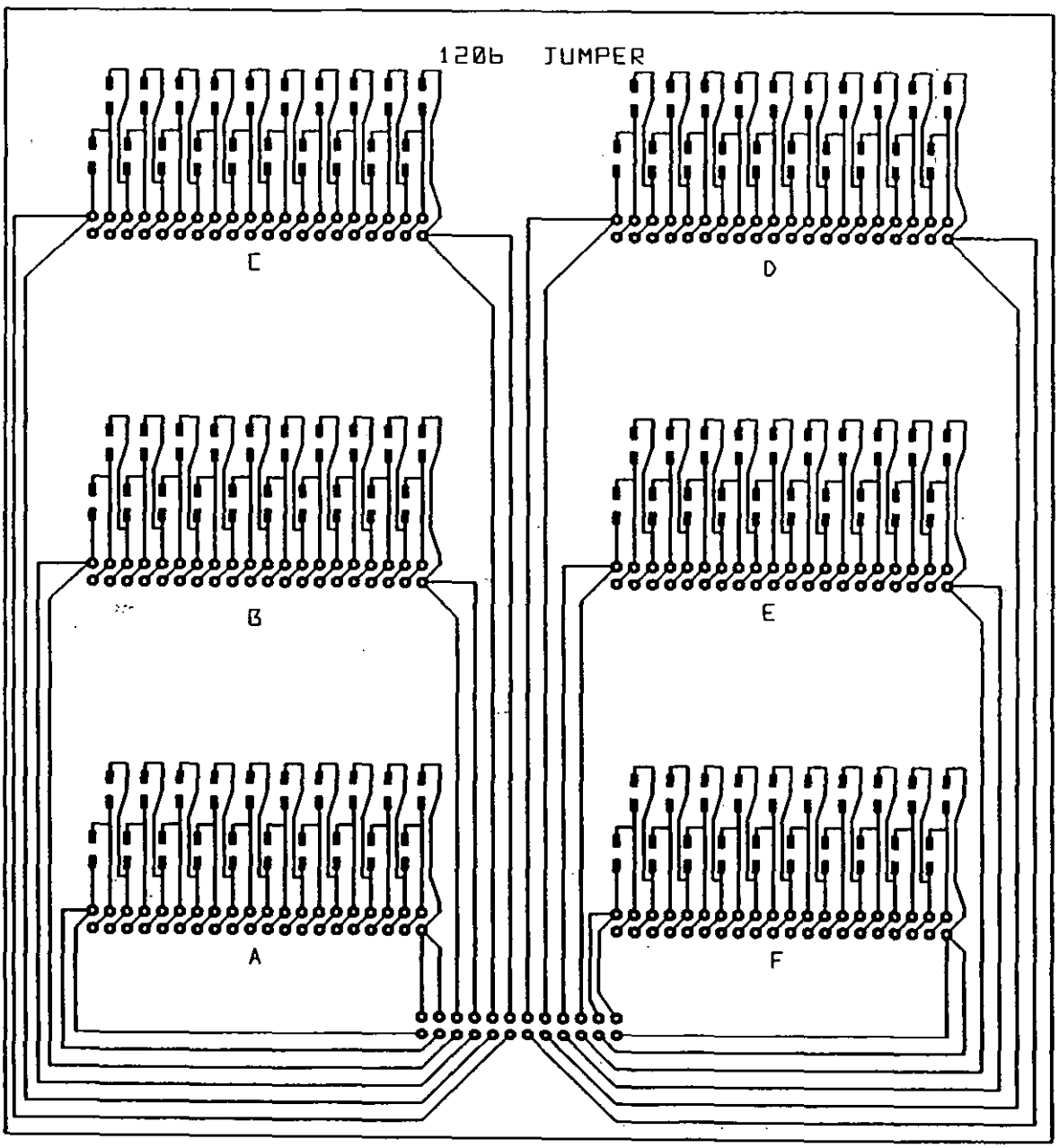


Figure 35 Revised 1206 Jumper Coupon

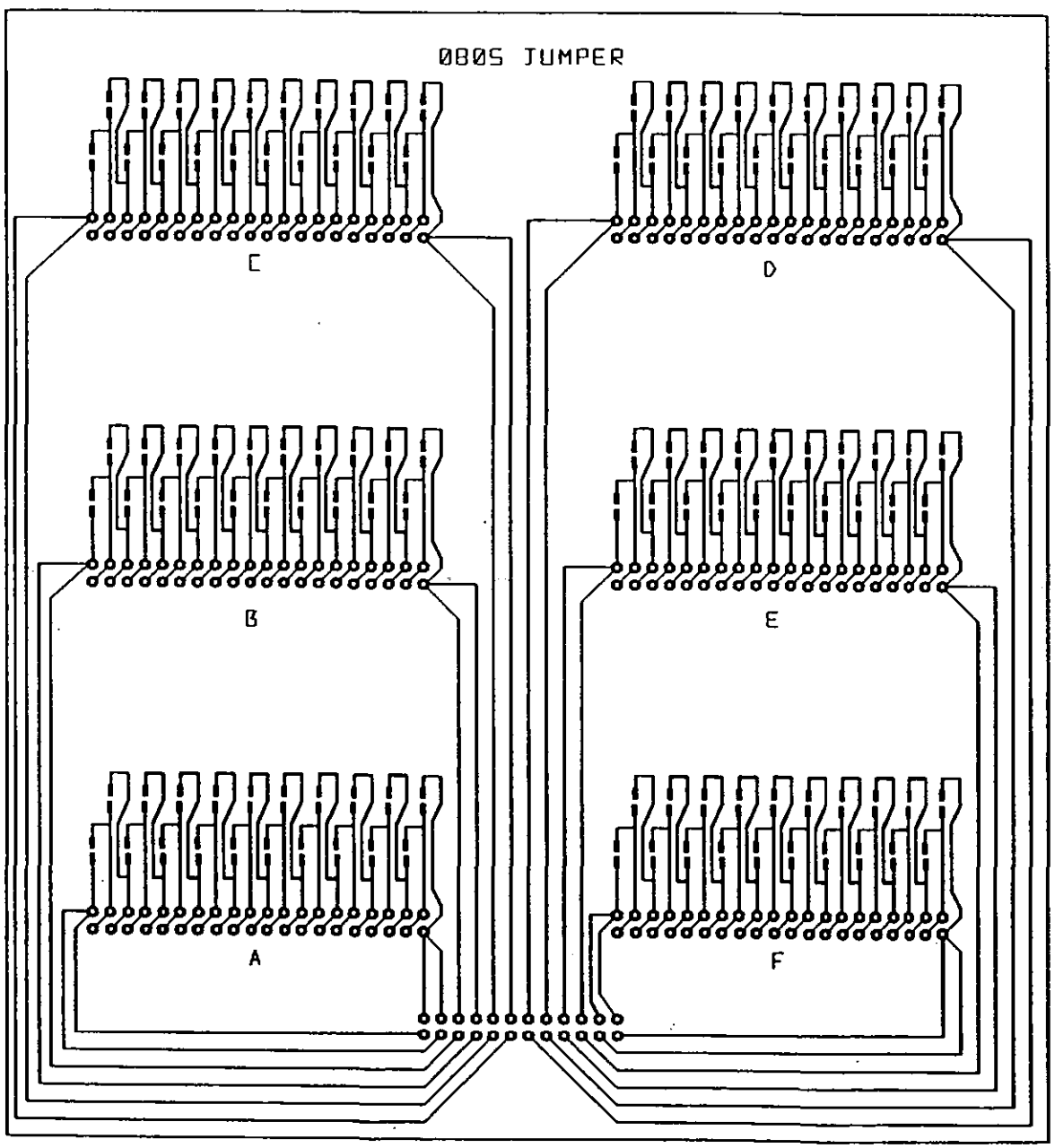


Figure 36 0805 Jumper Coupon

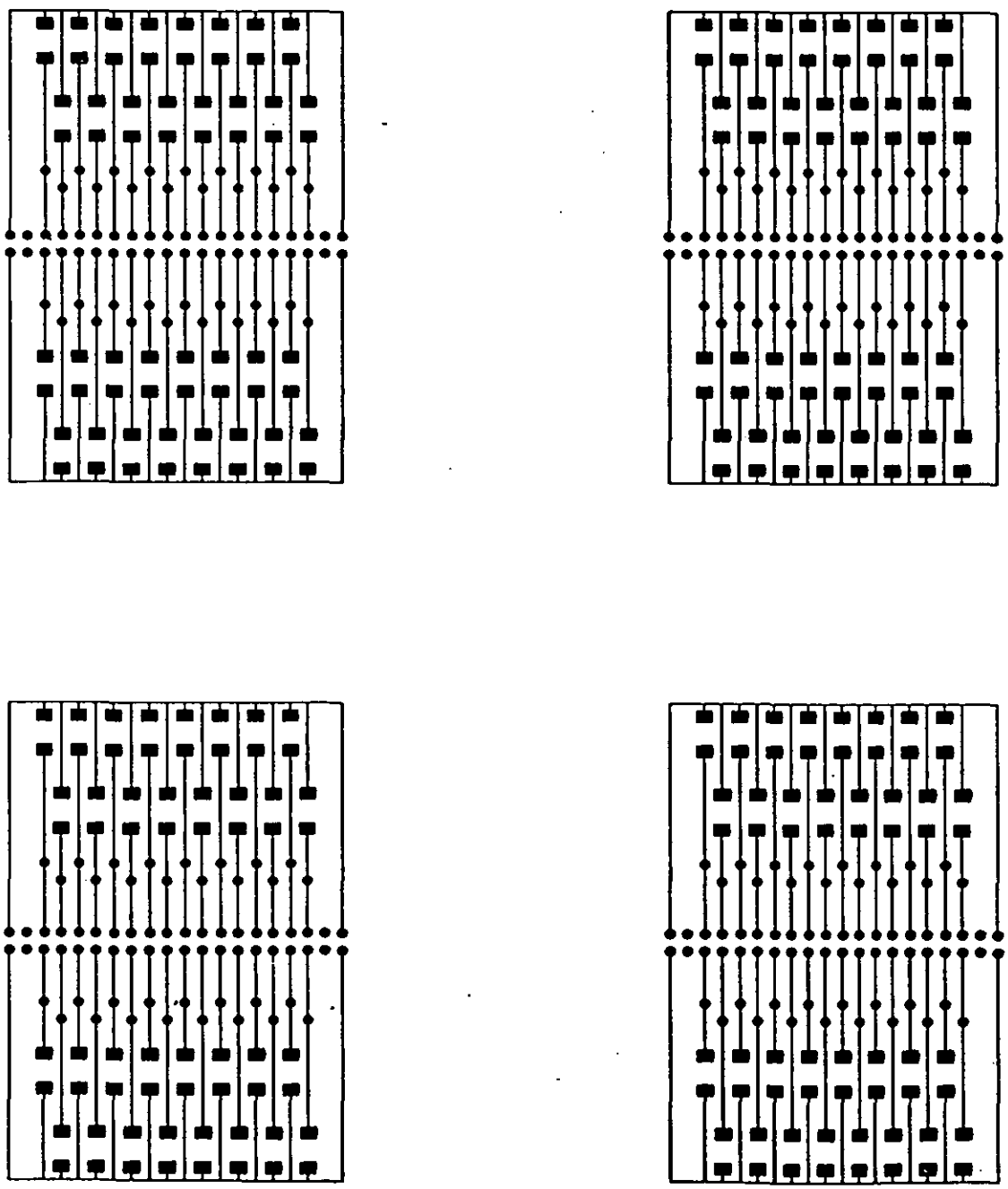


Figure 37 1812 Capacitor Coupon

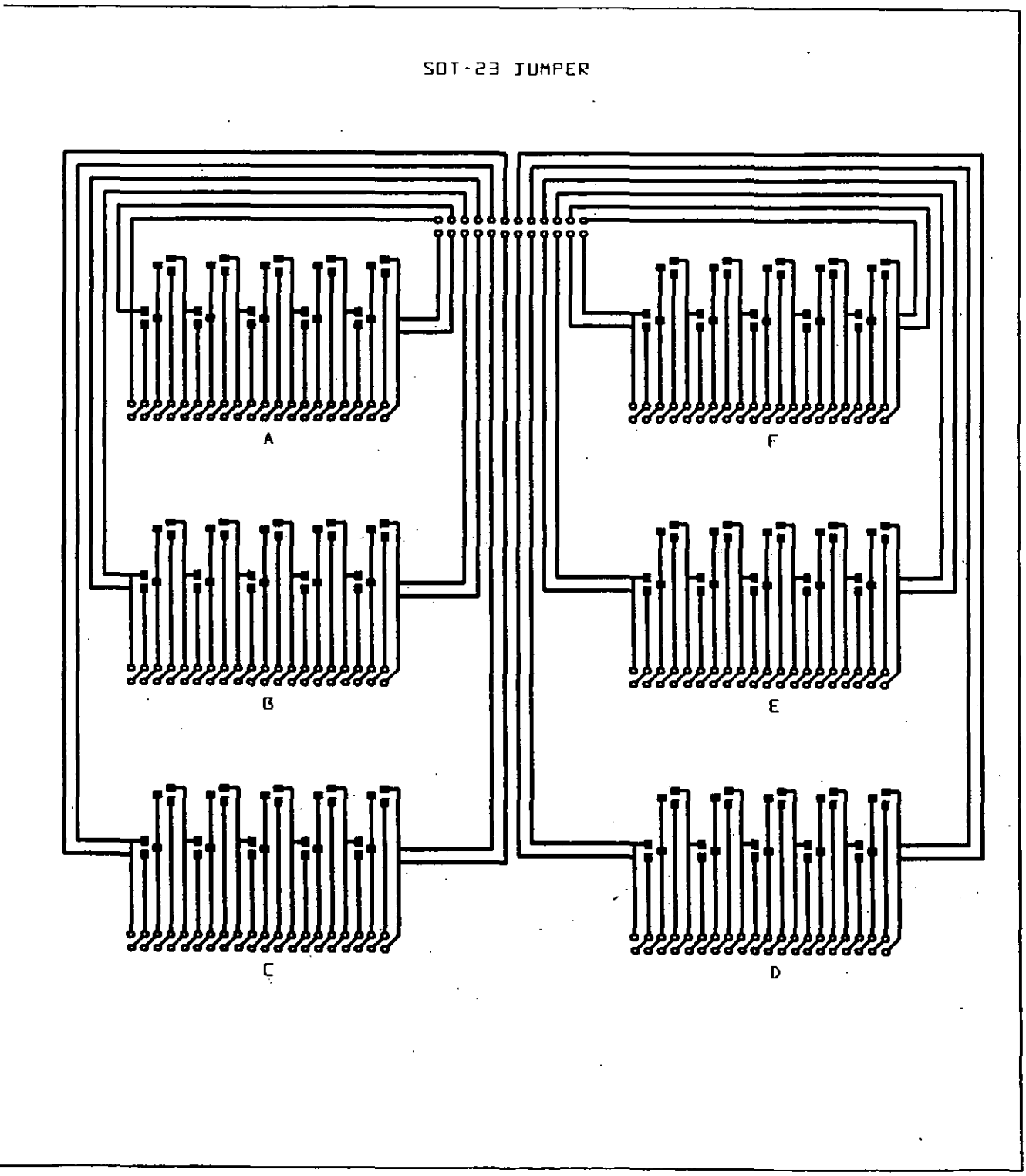


Figure 38 SOT-23 Jumper Coupon A

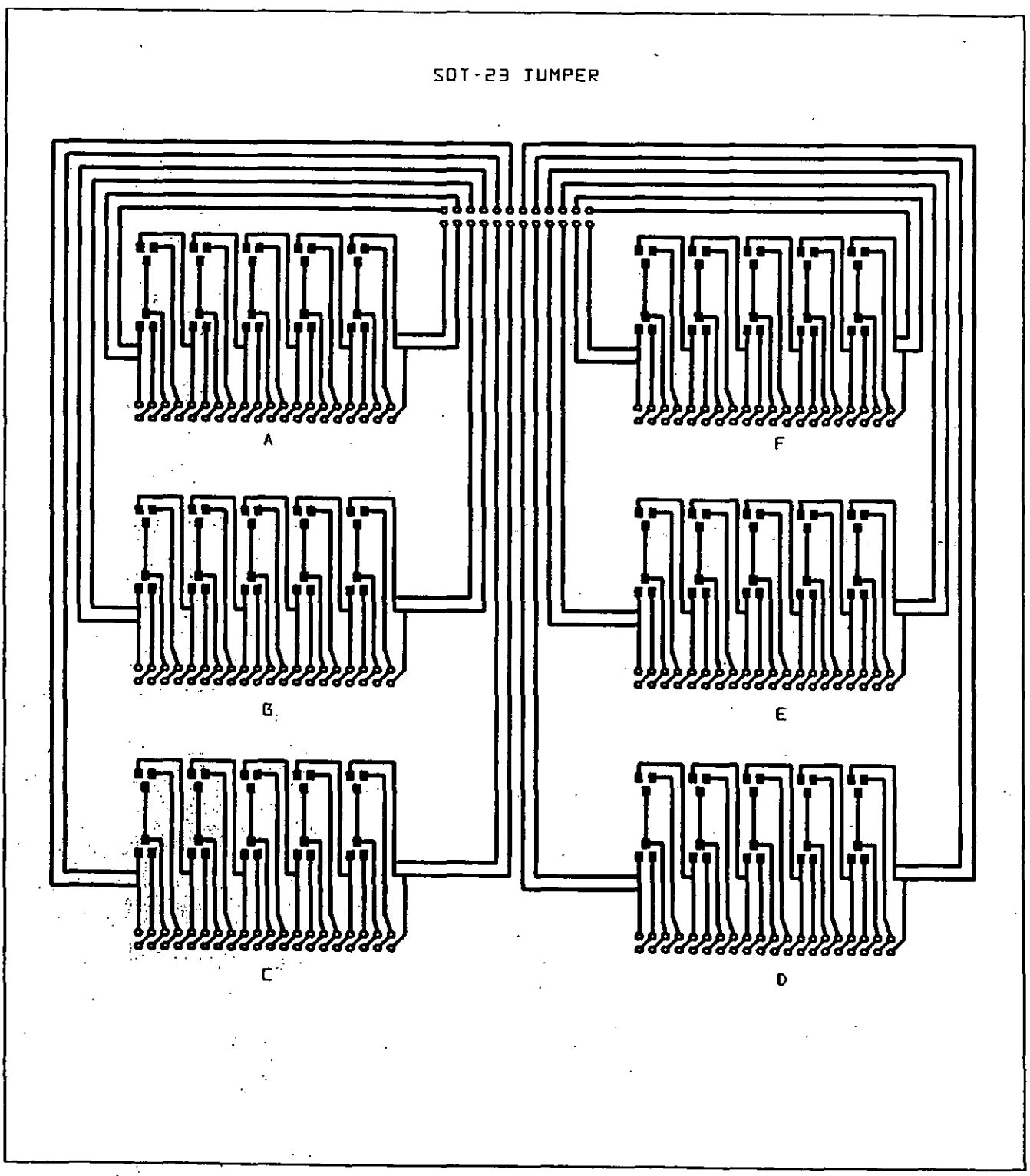


Figure 39 SOT-23 Jumper Coupon B

5.8 SOT-23 Resistor Coupon

This coupon (Figure 40) allows the placement of 80 SOT-23 packaged potential divider chips (2 x 100Ω) on an 8U size circuit board (222 mm x 195 mm).

5.9 Thermal Mapping Coupon

This coupon (Figure 41) contains five groups of nine 1206 chip mounting sites. The court area establishes an area around the component for placement, inspection, test and rework access. This area must not be encroached on by the court area of any other component. The spacing between component court areas within the groups on the test coupon are 0, 2, 3.5, 6.5 and 10 mm. This board design allows the effect of component spacing on temperature rise and distribution to be examined.

5.10 References

1. STC Company Standard CS50, Printed boards (ITT Engineering and Manufacturing Standards) 001-ITT 4050 0006, p 1, December 1984.

2. STC Company Standard CS60, Surface Mounted Components User Guide, Part 2, Page 7, Issue 1, February 1984.

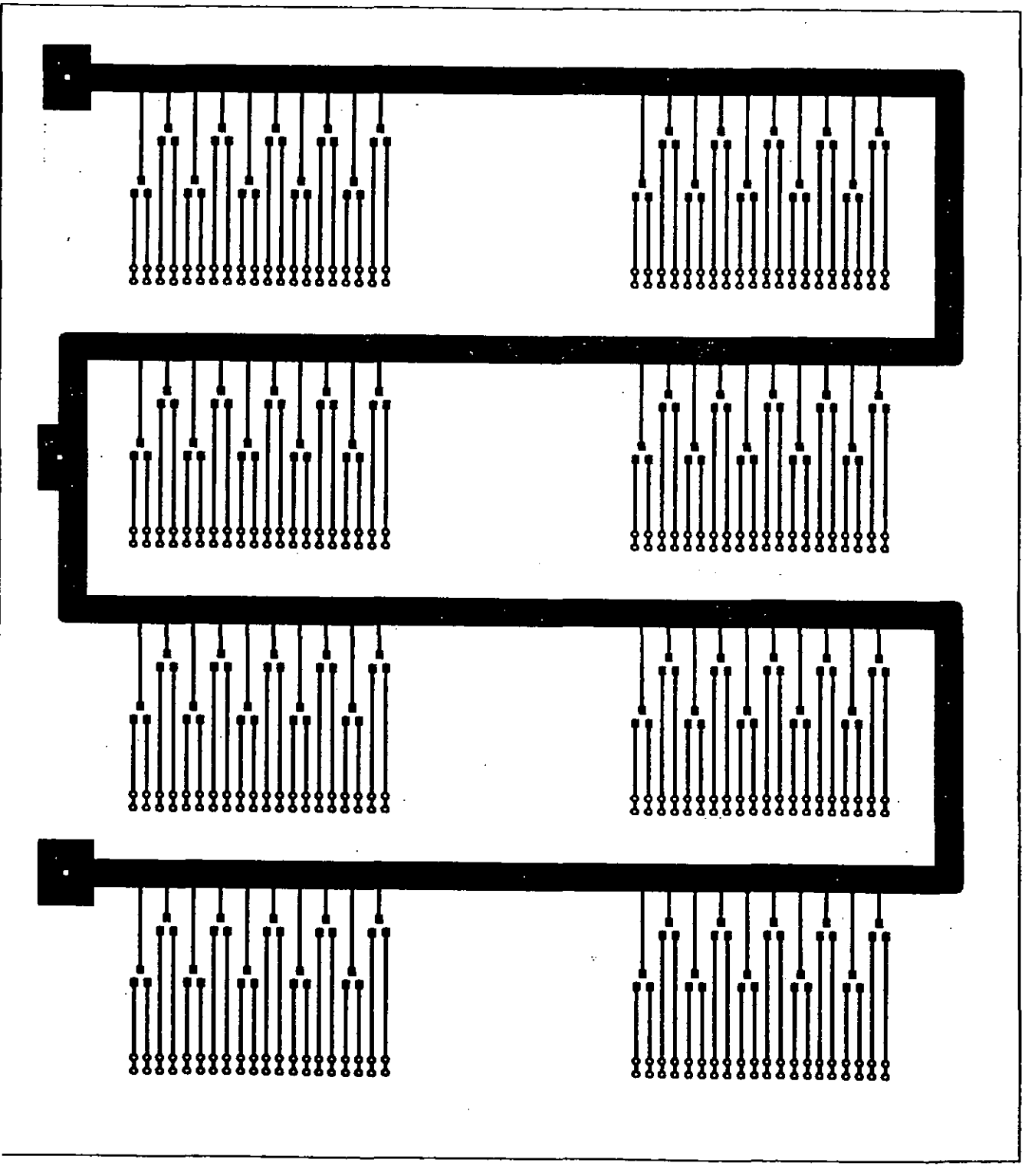


Figure 40 SOT-23 Potential Divider Coupon

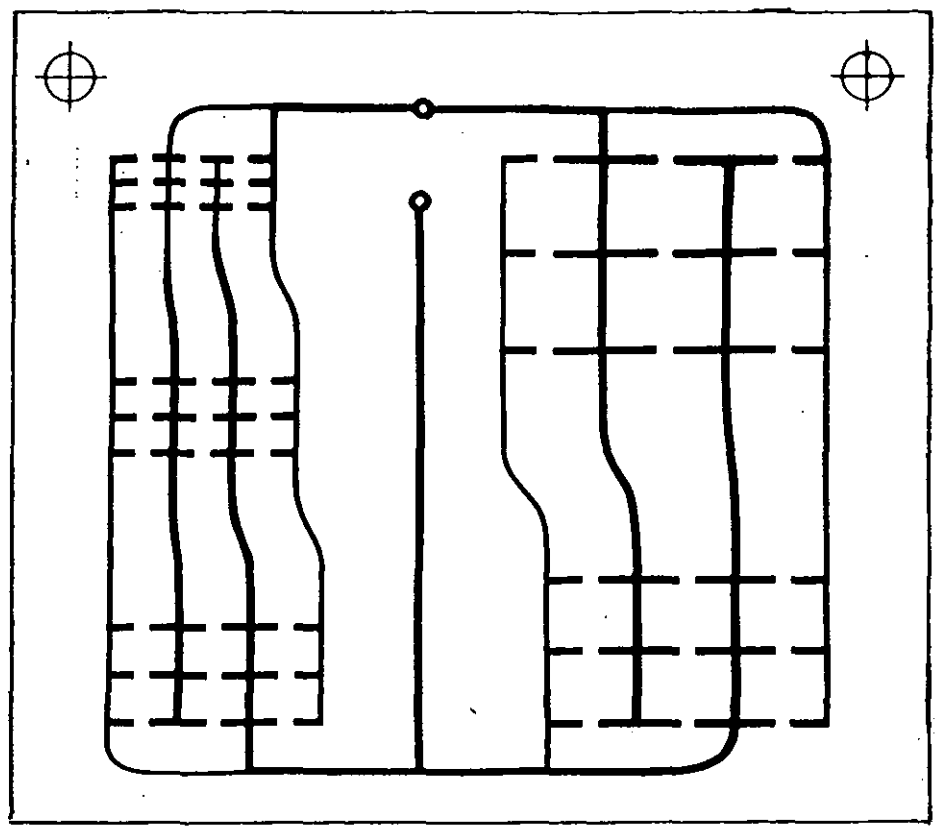


Figure 41 Thermal Mapping Coupon

CHAPTER SIX - MEASUREMENT TECHNIQUES

6.1 Resistance Measurement

A matrix technique (Figure 42) for resistance measurement was initially investigated. This method simplifies the hardware and greatly reduces the amount of cabling between computer and components. In the diagram the resistance of component A is being measured. The technique relies upon the voltage drop across the ammeter (I) being negligible. Points 1, 2, 3 and 4 are consequently at the same potential and thus no current flows through components E, F, G, H and I. Components B, C and D have the full source voltage applied to them but the current through them is not measured. The ammeter therefore only measures the current through component A and R_A may be calculated using Ohm's Law.

Experiment has however showed this technique to be insufficiently accurate. This is because in practice the voltage burden of the ammeter is not zero and consequently point 1 is at a slightly lower potential than 2, 3 and 4 and therefore current flows through E and F, G and H etc. This method was therefore abandoned and a simple scanning technique was used (Figure 43). Thus four terminal (Kelvin) connections were used in order to eliminate errors due to the resistance of the interconnecting leads, relay contacts etc. The measuring instrument used was a Solartron 7061 or 7065 DVM.

6.2 Capacitance Measurement

Capacitors were measured using a similar system to that described in 6.1. but using a Wayne-Kerr 4210 LCR meter instead of the DVM.

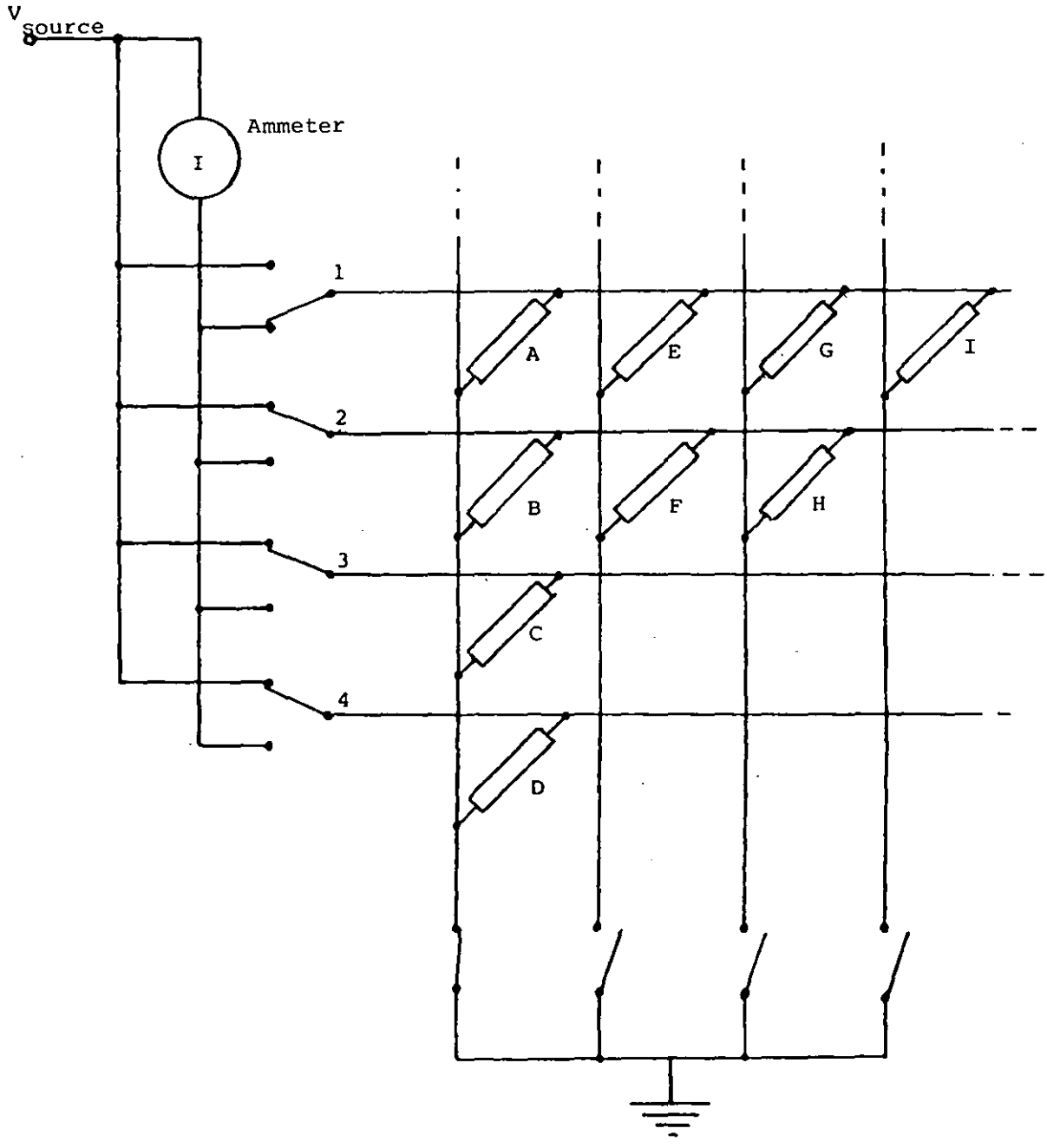


Figure 42 Matrix Method for Resistance Measurement.

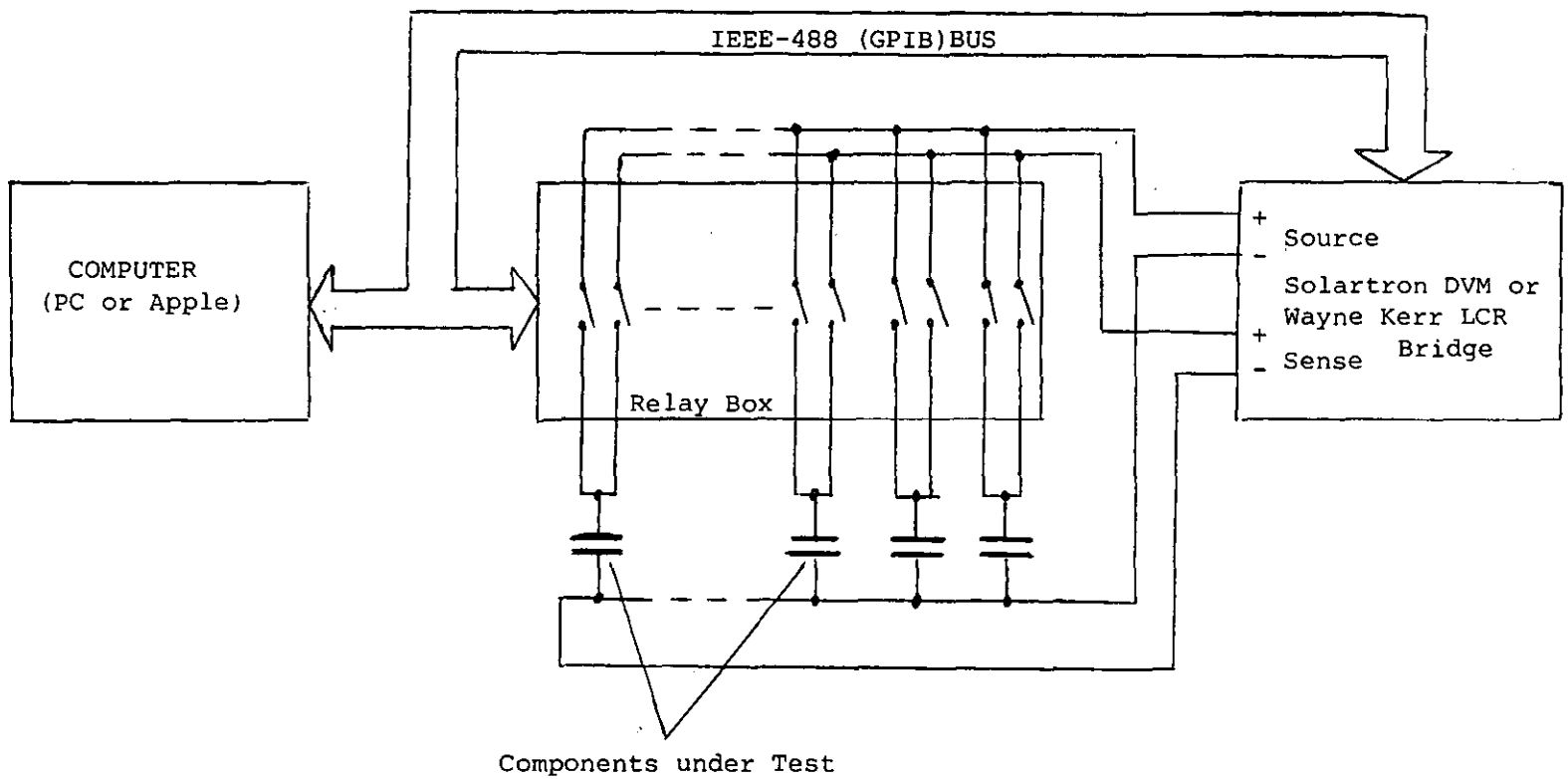


Figure 43 Resistor/Capacitor measurement

This instrument allows measurement of both capacitance and equivalent series resistance (ESR) and from these the dissipation factor (tan δ) may be calculated.

6.3 Third Harmonic Measurement

Any non-linearity in an electronic component will add third harmonic distortion to an applied sine wave signal. Many components have some intrinsic level of distortion due to non-linearity of the materials from which they are constructed. For example, the dielectric constant of the ferro-electric materials used in ceramic capacitors vary depending on electrostatic field strength and thus the capacitors show a voltage coefficient of capacitance.

Non intrinsic distortion will however be generated by faults in the component or by instability of the contacts within and to the component [1].

The non-linearity or third harmonic index (THI) is defined as the ratio of the 3rd harmonic voltage and the applied fundamental voltage, expressed in dB:-

$$THI = 20 \log \frac{V_{3 \times fundamental}}{V_{fundamental}} \text{ (dB)} \qquad (16)$$

The technique will detect the same sorts of defects as current noise measurement, but is more sensitive and is less influenced by externally generated electromagnetic noise.

The test equipment used is a Radiometer CLT1a which consists of a 10 kHz sine wave source and a 30 kHz voltmeter. The 30 kHz voltmeter has a 0 to 1V d.c. output which is monitored by a digital voltmeter connected to the computer via the 1EEE488 bus (Figure 44), allowing automatic testing of components.

6.4 Leakage Current Measurement

The leakage current is an important parameter of any capacitor and is the steady state current at full rated voltage. It is thought that the glues used to attach components before soldering and also any flux residues trapped under components, may provide leakage paths under conditions of high humidty. Leakage currents are also of particular interest in the Corning 1812 capacitors. This is because the non-noble electrodes employed in their construction involve a relatively new technology, and any information on their reliability under environmental testing is of value.

The leakage current of a capacitor is normally measured 300 s after applying full rated voltage. It would however take over 10 hours to individually measure each capacitor on a coupon of 128. In order to speed up this measurement a technique has been developed to charge groups of 32 capacitors simultaneously for 60s and then during the next 30s individually measure their leakage currents (Figure 45).

6.5 Thermal Mapping

Thermal mapping is important in the determination of the actual operating stresses encountered in surface mounted devices. Stresses

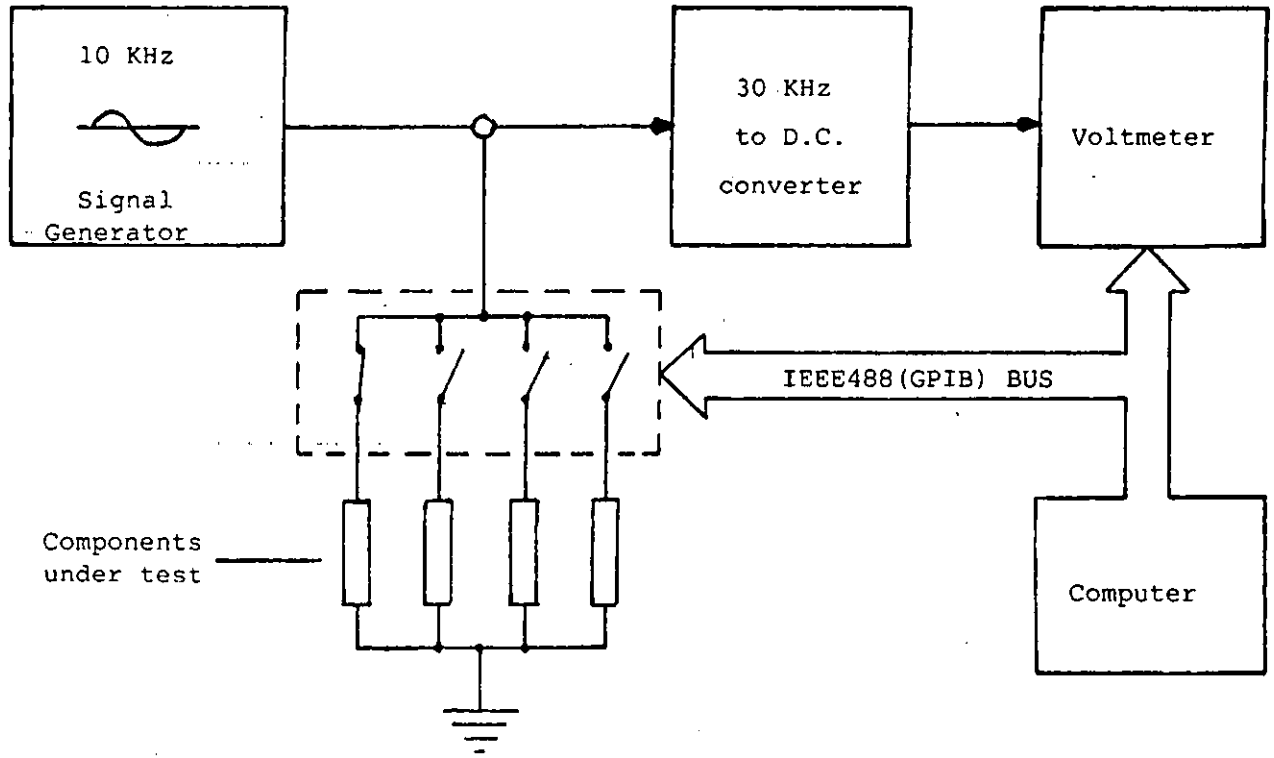


Figure 44 Non-linearity Measurement System

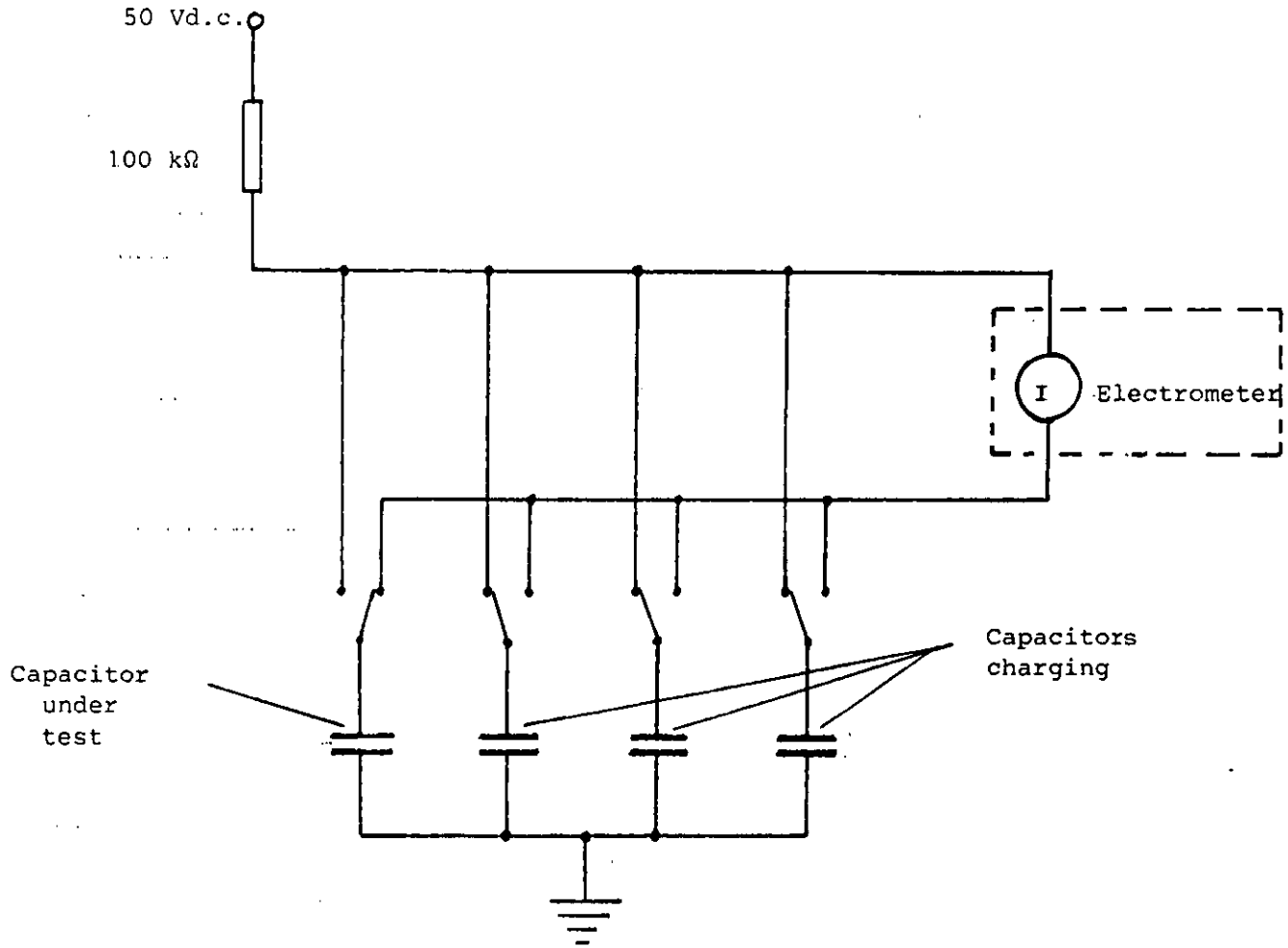


Figure 45 Leakage Current Measurement

occur due to power dissipation within components causing differential expansion of the components and substrate.

Initial thermal mapping work was undertaken using a fine tip temperature probe constructed at LUT (Figure 46). This is attached to a manual X-Y table allowing temperature measurement at any point on the test coupon. This technique is however time consuming, and the purchase of an infra-red thermal imaging system has subsequently enabled a rapid and very accurate picture of the thermal characteristics of components to be obtained. The resolution of this equipment is 100 μm, with a temperature resolution of 0.1°C.

6.6 References

1. V. Peterson, P. Harris, "Harmonic Testing Pinpoints Passive Component Flaws". Electronics, pp 93-100, 11th July, 1966.

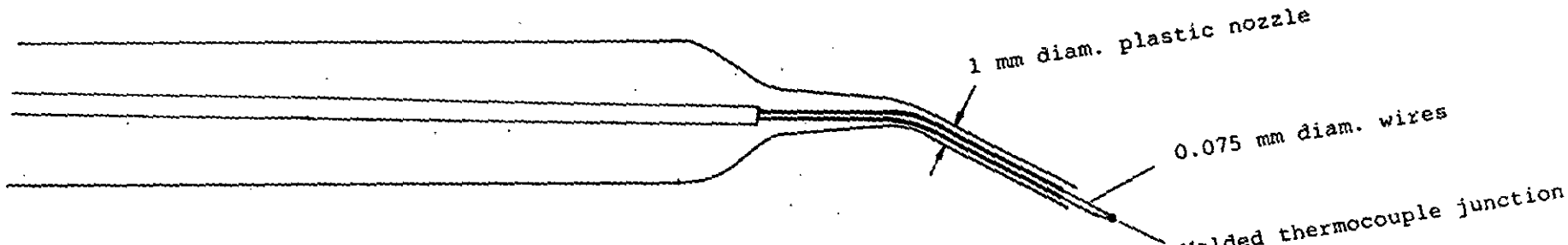


Figure 46 Fine Wire Thermocouple Temperature Probe.

CHAPTER SEVEN - RESULTS

7.1 Power Cycling

7.1.1 1206 Resistor Chips

The power cycling test on the coupon of 128 '1206' size thick film resistor chips completed 15,000 cycles (30 mins. at 125mW, 30 mins off). Two failures occurred and several of the resistors show small changes in resistance (Figure 47). The first failure was due to fracture of a solder fillet and was observed after 6500 cycles. The fillet was poorly formed and its failure shows that this shape of fillet is unacceptable for long term reliability. The second failure was a short circuit failure of a component and was observed after 8500 cycles. The other small changes in resistance observed are also due to drift of the actual component resistances.

No correlation has been found between either initial or final linearity (third harmonic measurement) and these changes in resistance (Figures 48 and 49).

Unfortunately, the failed solder joint was destroyed during sectioning so no further analysis has been possible, but a view of the failed fillet is shown in Figure 50.

7.1.2 SOT-23 Resistor Chips

The power cycling test on SOT-23 packaged thin film potential divider chips completed 2000 cycles (30 mins. at 300mW, 30 mins. off).

Fig 47.Resistance changes / failures in power cycle test on 1206 size resistor chips.

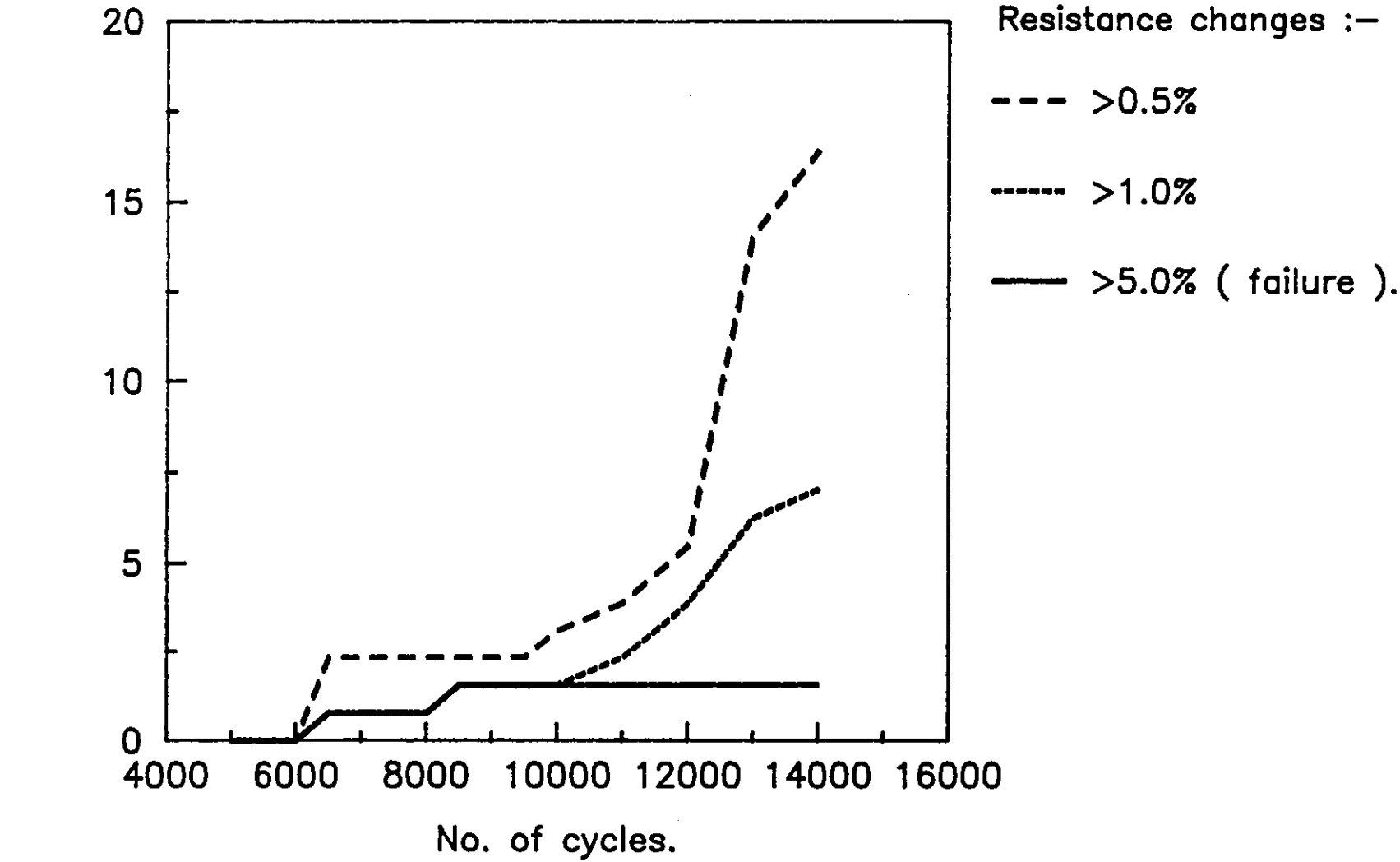


Fig 48. Scattergram of initial linearity against resistance change in power cycling test on 1206 resistors.

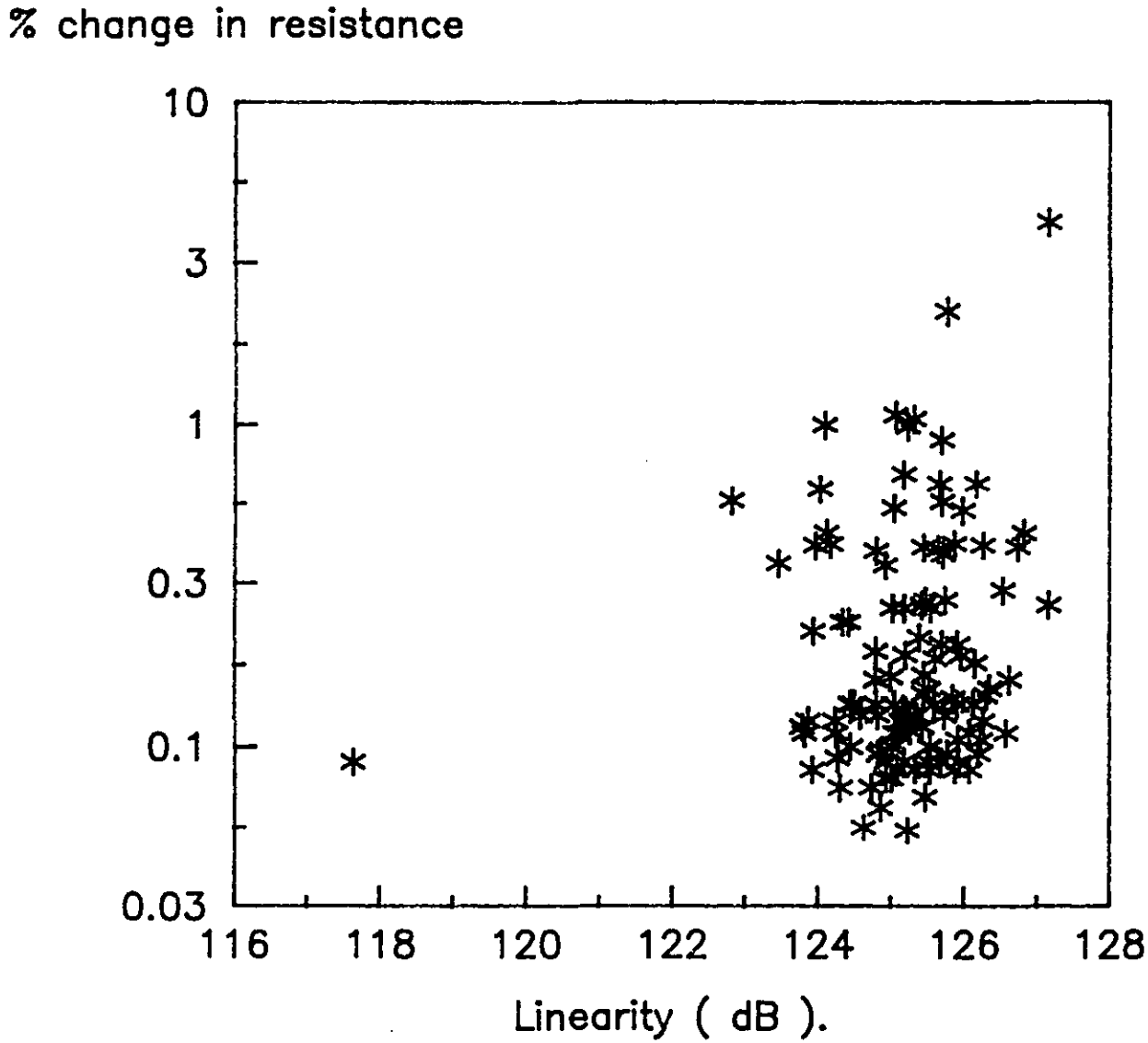
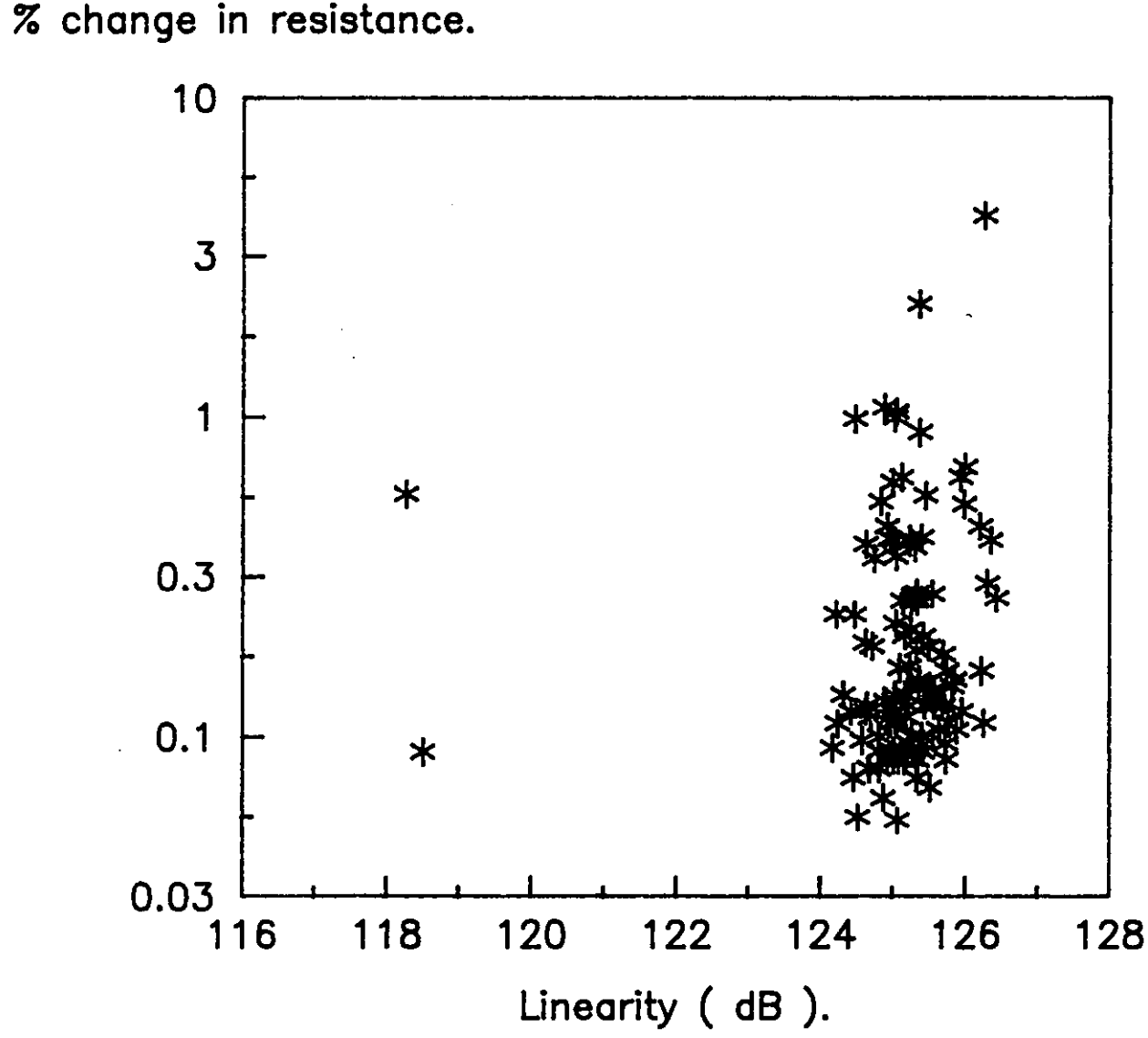


Fig 49. Scattergram of final linearity against resistance change in power cycling test on 1206 resistors.



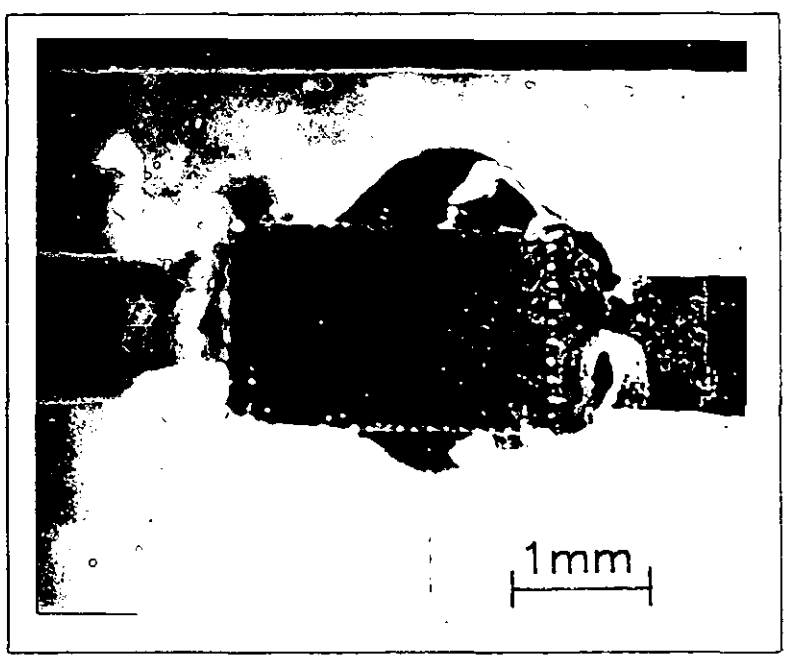


Figure 50 Solder Joint Failure in Power Cycle Test

There were two initial component failures (open circuit), three further resistance failures occurred during the test ($\Delta R>5\%$) and smaller resistance changes were observed in a number of other components (Figure 51). These resistance changes are all associated with the components themselves rather than their interconnections. The manufacturer had unspecified manufacturing problems with this batch of components and this suggests their instability may be due to them being from a poor batch rather than there being a general problem with this type of component.

7.2 Thermal Cycling

7.2.1 1206 Size Jumper Chips

The results of temperature cycling 1206 'zero-ohm' jumper chips are shown in Table 11 and Figure 52. The results show that the most severe change in resistance occurs in cycling to a peak temperature of +95°C. A model for this effect is described in the paper attached as Appendix 3. The changes in resistance are distributed throughout the test coupons (Figures 53 to 57), that is, the changes in resistance observed are not attributable to one particular jumper chip.

No solder joint failures occurred in these tests.

7.2.2 0805 and SOT-23 Jumper Chips

The resistance changes observed in the temperature cycling tests on SOT-23 jumper chips show a peak in the -55 to +95°C test similar to

Fig 51. Resistance failures / changes in power cycling test on SOT–23 potential divider chips.

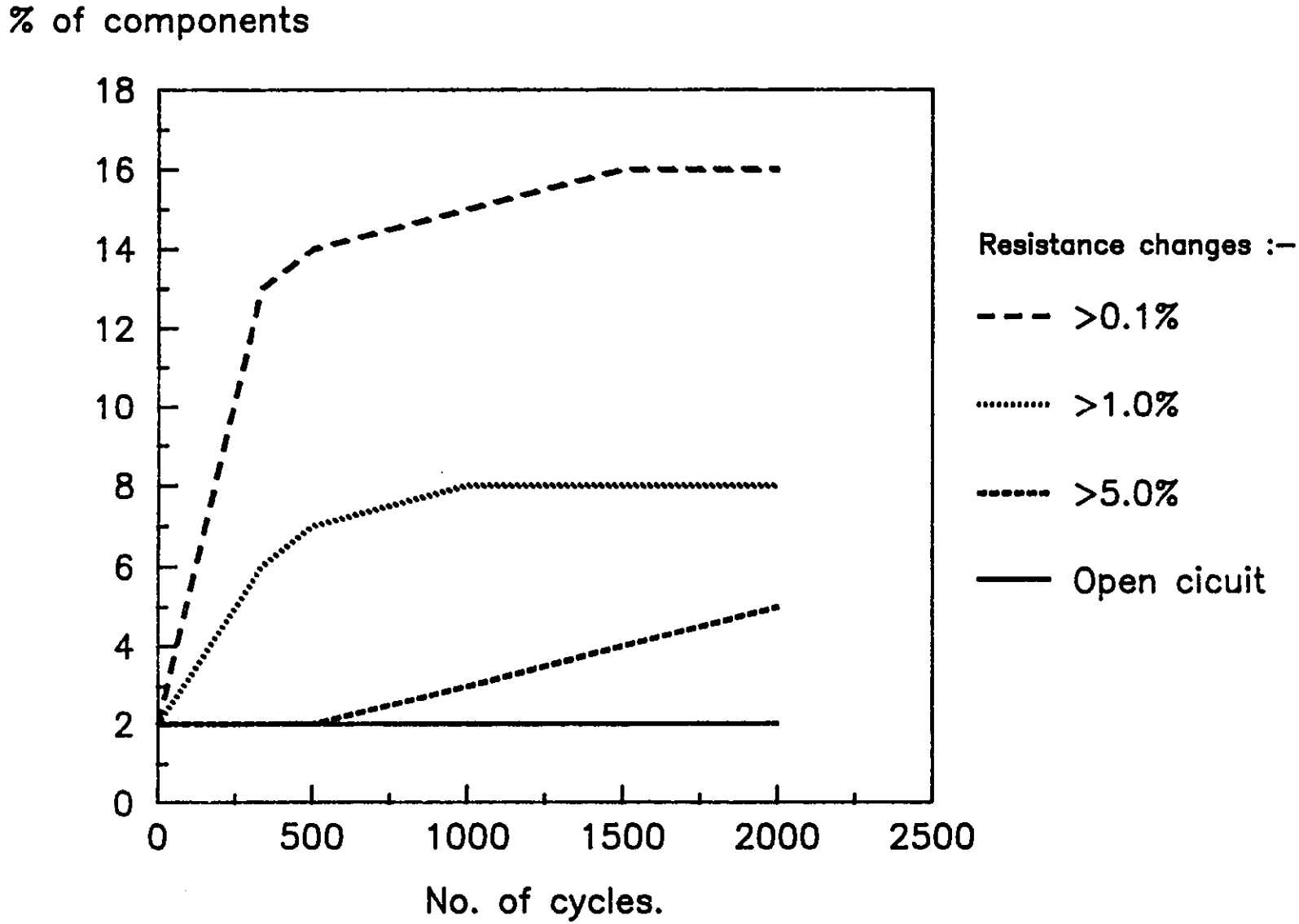
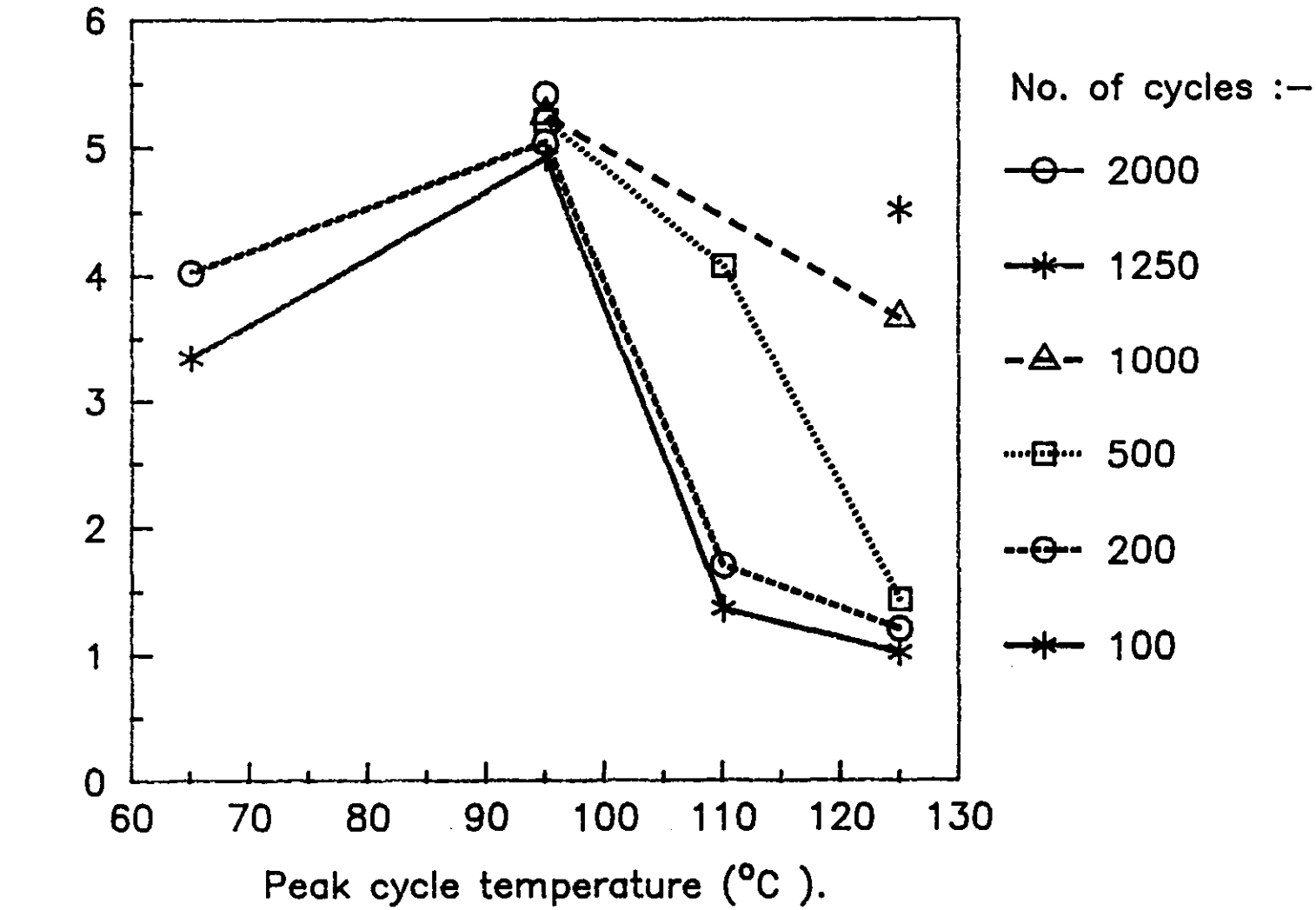


Table 11. Resistance changes in temperature cycling tests on 1206 size jumper chips.

Cycle range (°C)	Initial chain resistance (Ω)	Total % change in chain resistance. Number of cycles. 100	200	500	1000	1250	2000
−55 to +125	5.907	1.02%	1.20%	1.43%	3.66%	4.51%	—
−55 to +110	5.161	1.36%	1.70%	4.07%	—	—	—
−55 to +95	5.625	4.92%	5.04%	5.21%	5.25%	—	5.41%
−55 to +65	6.512	3.34%	4.02%	—	—	—	—
−55 to +5	5.614	3.42%	—	—	—	—	—

Fig 52. Resistance changes in temperature cycling tests on 1206 size jumper chips.



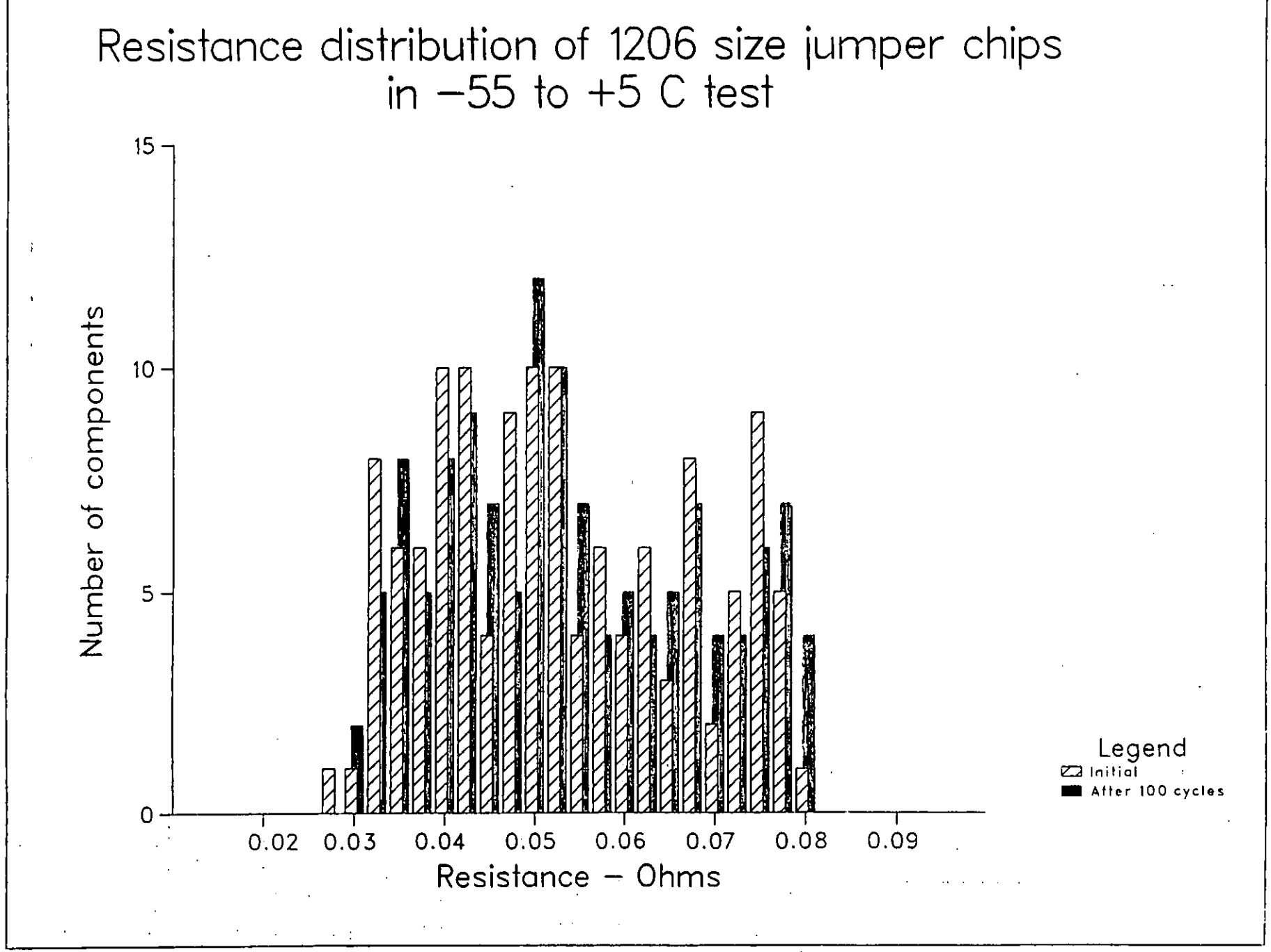

Resistance distribution of 1206 size jumper chips
in −55 to +5 C test
Number of components
15
10
5
0
0.02
0.03
0.04
0.05
0.06
0.07
0.08
0.09
Resistance − Ohms
Legend
Initial
After 100 cycles

Figure 54

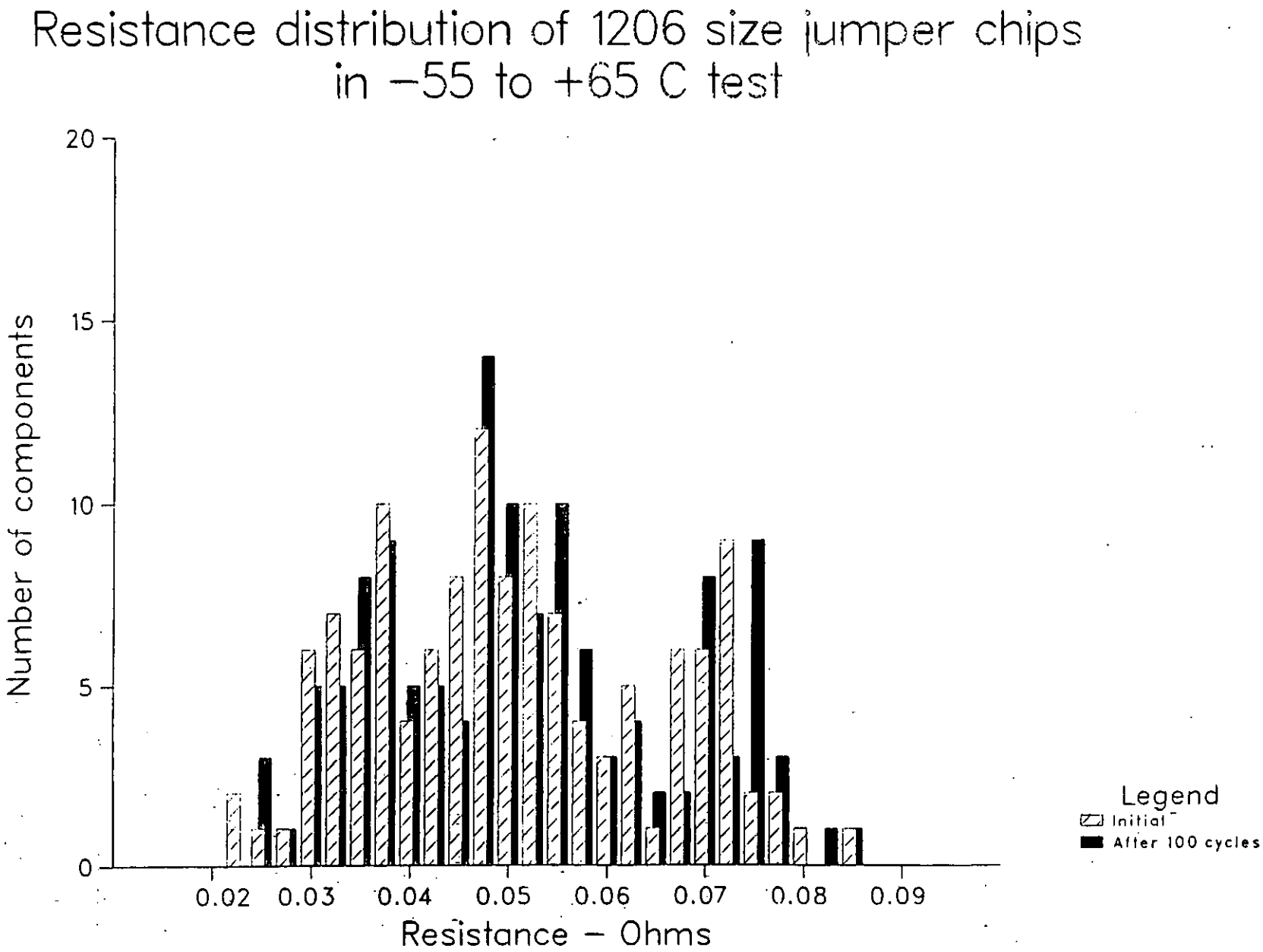
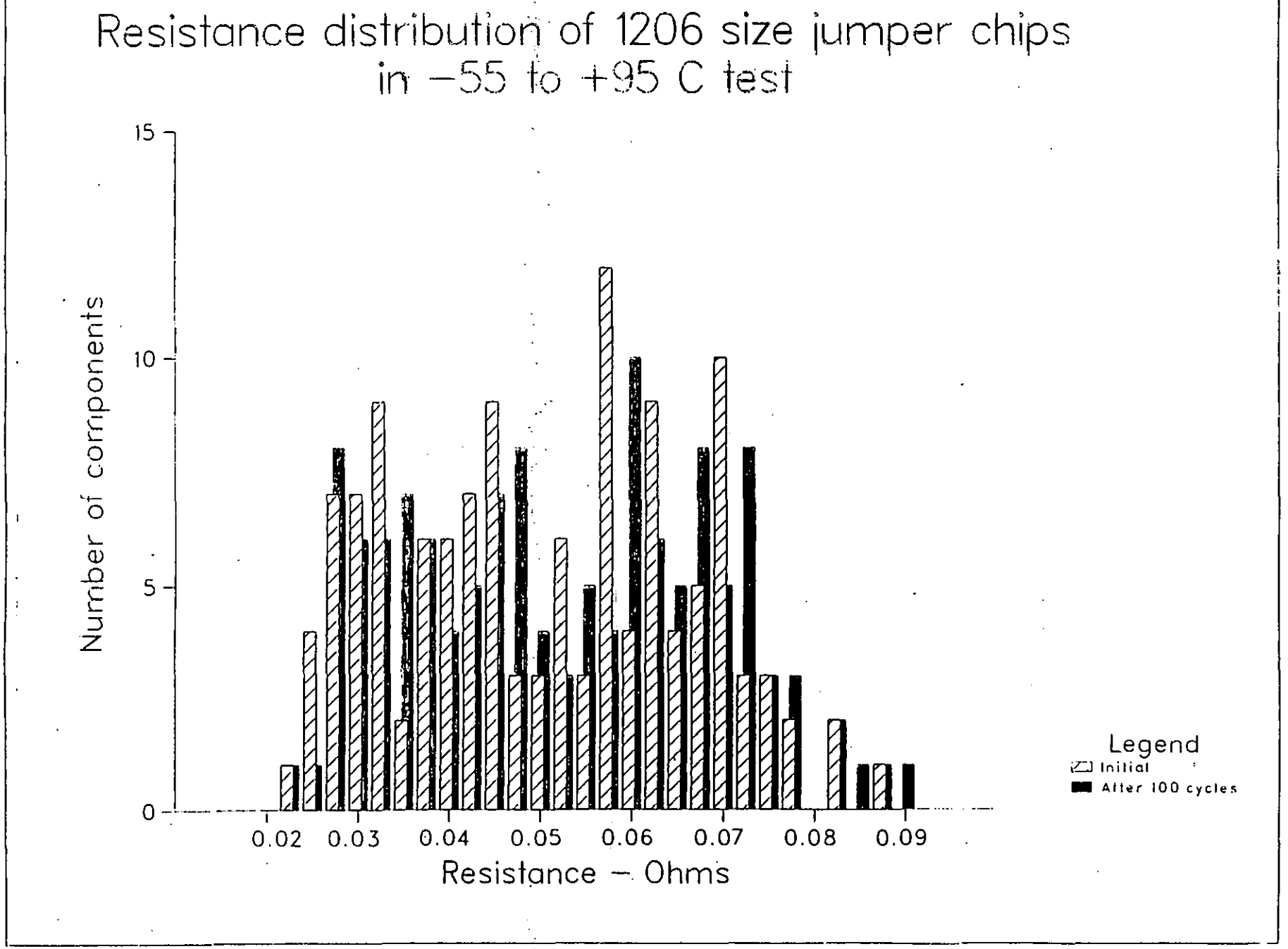
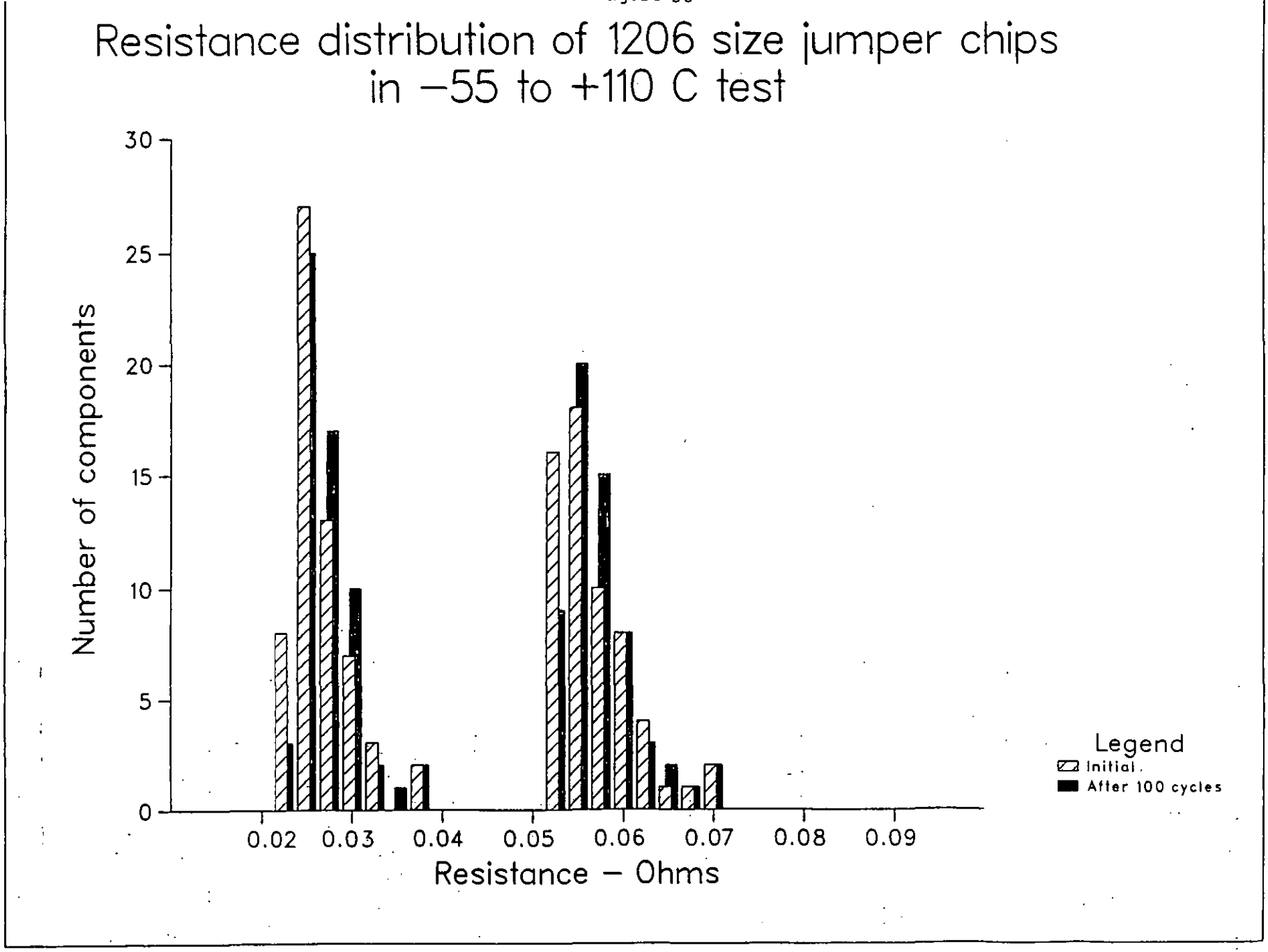
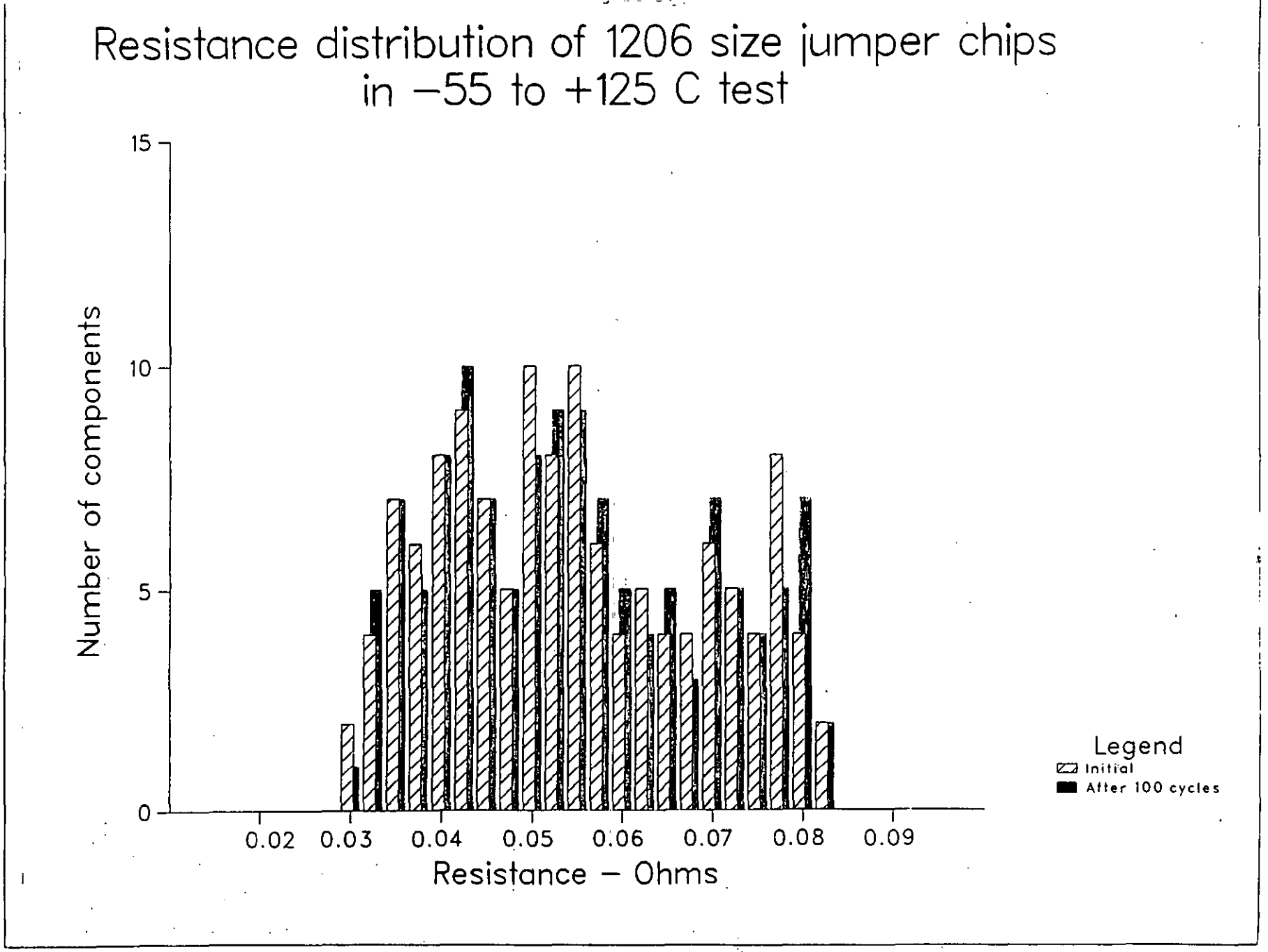

Resistance distribution of 1206 size jumper chips
in −55 to +65 C test
Number of components
20
15
10
5
0
0.02
0.03
0.04
0.05
0.06
0.07
0.08
0.09
Resistance − Ohms
Legend
Initial
After 100 cycles

Figure 55


Resistance distribution of 1206 size jumper chips
in −55 to +95 C test
Number of components
15
10
5
0
0.02
0.03
0.04
0.05
0.06
0.07
0.08
0.09
Resistance − Ohms
Legend
Initial
After 100 cycles


Resistance distribution of 1206 size jumper chips
in −55 to +110 C test
Number of components
30
25
20
15
10
5
0
0.02
0.03
0.04
0.05
0.06
0.07
0.08
0.09
Resistance − Ohms
Legend
Initial
After 100 cycles


Resistance distribution of 1206 size jumper chips
in −55 to +125 C test
Number of components
15
10
5
0
0.02
0.03
0.04
0.05
0.06
0.07
0.08
0.09
Resistance − Ohms
Legend
Initial
After 100 cycles

that occurring with the 1206 jumper chips (Table 12). No solder joint failures occurred in the tests, but in the -55 to +125°C test one jumper chip failed internally and one chip was physically damaged in transit between STL and LUT. The results on these two chips were therefore not included in the calculations of resistance change.

The 0805 jumper chips were only tested from -55 to 95°C and as expected the resistance changes observed are considerably lower than those occurring in the 1206 jumper tests from -55 to +95°C (Table 13).

7.2.3 1206 and 1812 Size Capacitor Chips

No electrical failures occurred in these tests (Table 14), but severe cracking of a number of the solder fillets occurred in the tests on 1812 Corning capacitors (Figures 58 and 59) but no electrical degradation was attributable to these cracks. Significant drifts of capacitance and ESR in the overall populations were observed. These changes could be caused by:-

(a) Aging of the ceramic dielectric [1]. Table 15 shows the effects of aging on the control coupon of 1812 capacitors.

(b) Hysteresis in the temperature dependence of the dielectric materials properties - Figures 60 and 61 show the changes of capacitance with temperature for the two types of capacitor.

Table 12. Resistance changes in temperature cycling tests on SOT–23 jumper chips.

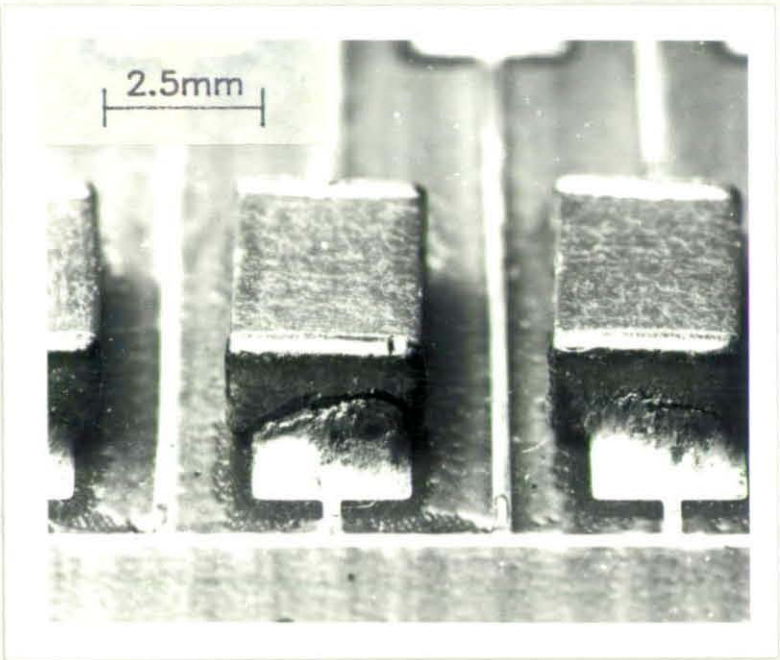
Cycle range (°C)	Initial chain resistance (Ω)	Total % change in chain resistance.			
		100	200	250	1000
–55 to +125	4.246	——	——	2.91%	——
–55 to +95	4.160	1.79%	5.82%	——	7.02%
–55 to +65	4.248	1.24%	——	——	——

Table 13.Resistance changes in temperature cycling test on 0805 size jumper chips.

Cycle range (°C).	Initial chain resistance (Ω).	% change in chain resistance. Number of cycles.			
		100	500	1000	2000
−55 to +95	5.96	1.66%	1.83%	2.24%	2.70%

Table 14. Failures in temperature cycling tests on capacitors

Cycle range (°C).	Component type	No. of cycles completed	No. of electrical failures
−55 to +95	1812 Corning	2000	0
−55 to +125	1812 Corning	1000	0
	1206 STC	2000	0



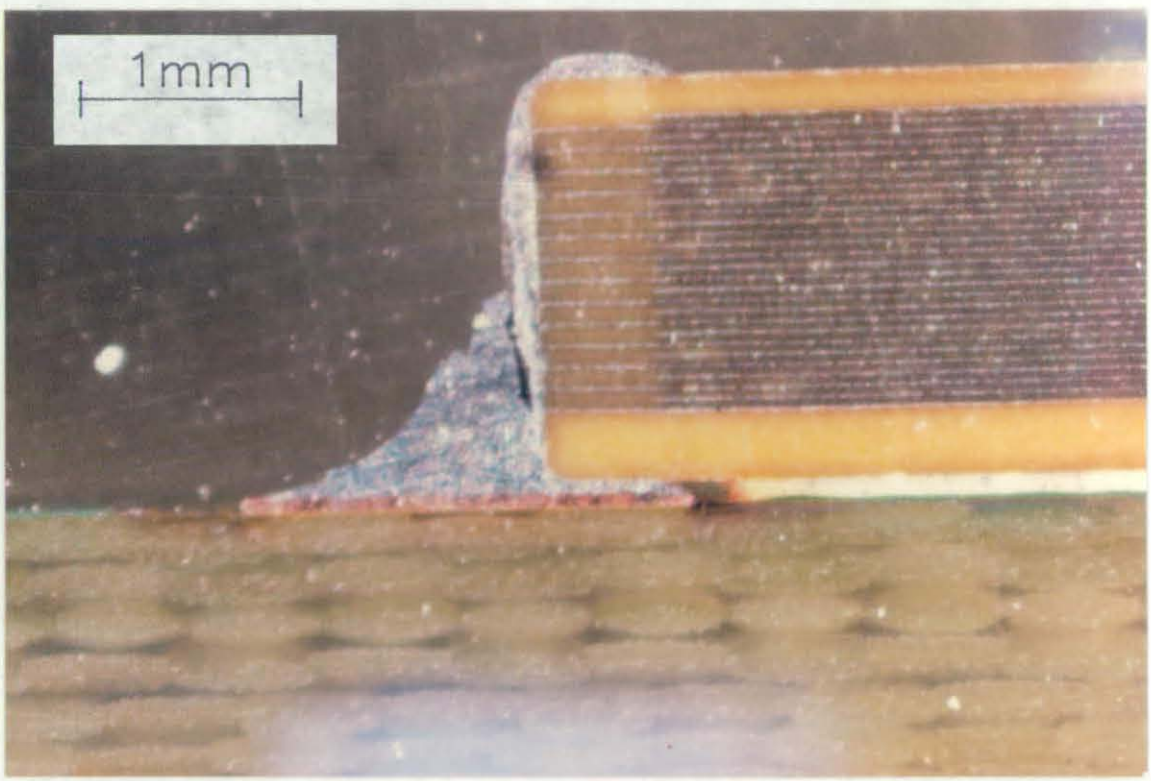
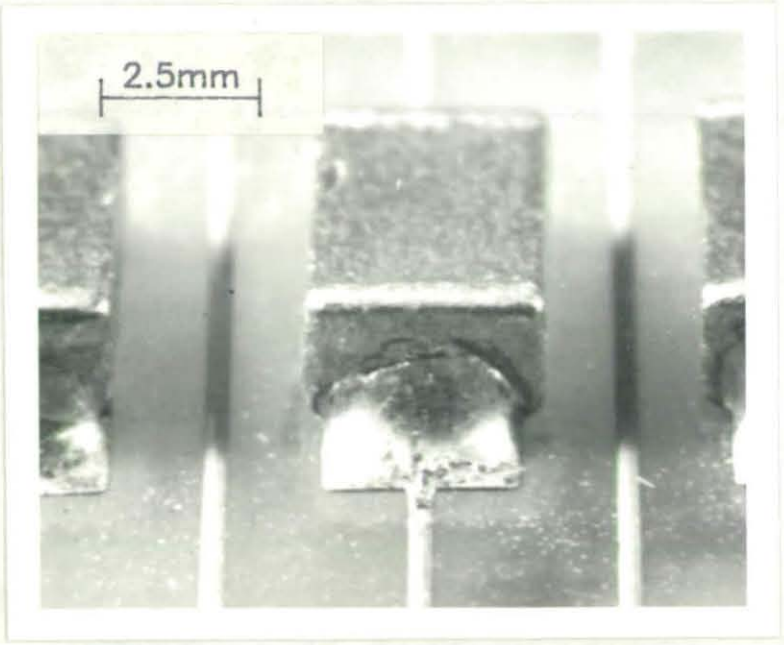


Figure 58 Solder Fillet Cracking in -55 to + 125°C Test on 1812 Size Corning Capacitors



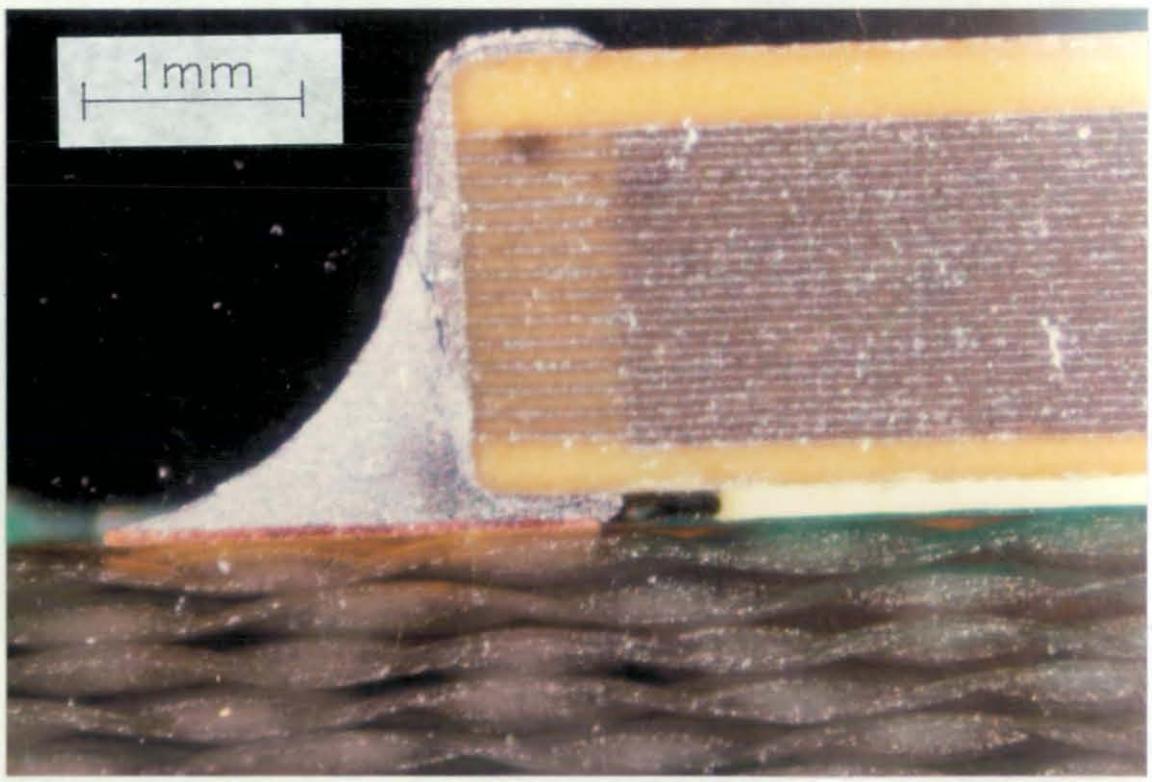


Figure 59 Solder Fillet Cracking in -55 to + 95°C Test on 1812 Size Corning Capacitors

Table 15. Changes in 1812 Corning capacitors on control coupon (stored at room ambient).

		Initial	10,000hrs	% change
Capacitance (nF)	AVG	102.60	100.90	−1.6%
	S.D.	3.20	3.20	
Dissipation	AVG	0.014	0.013	−6.6%
	S.D.	0.05%	0.08%	

Fig 60. Variation of capacitance with temperature of 1206 size STC capacitors (X7R dielectric).

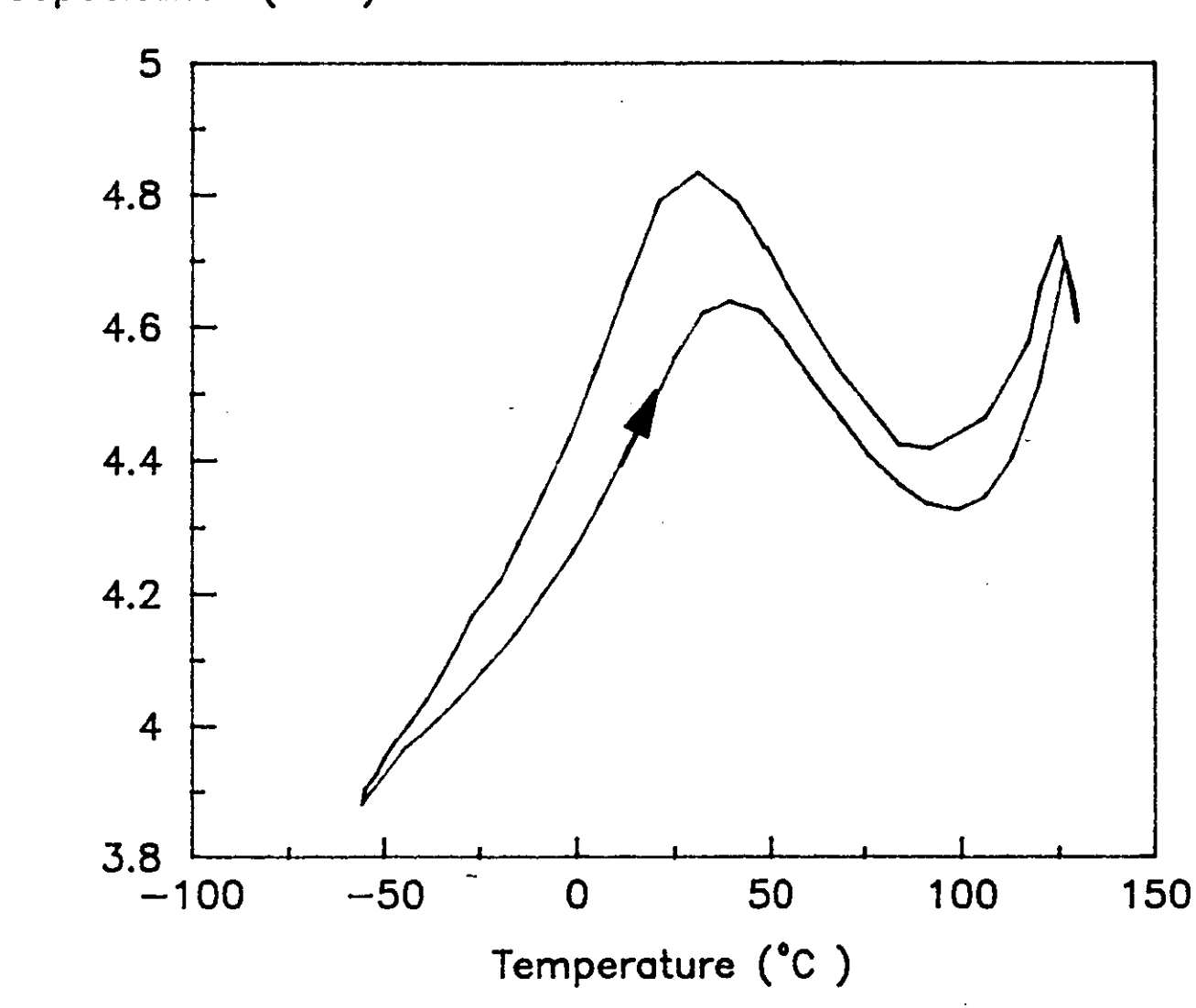
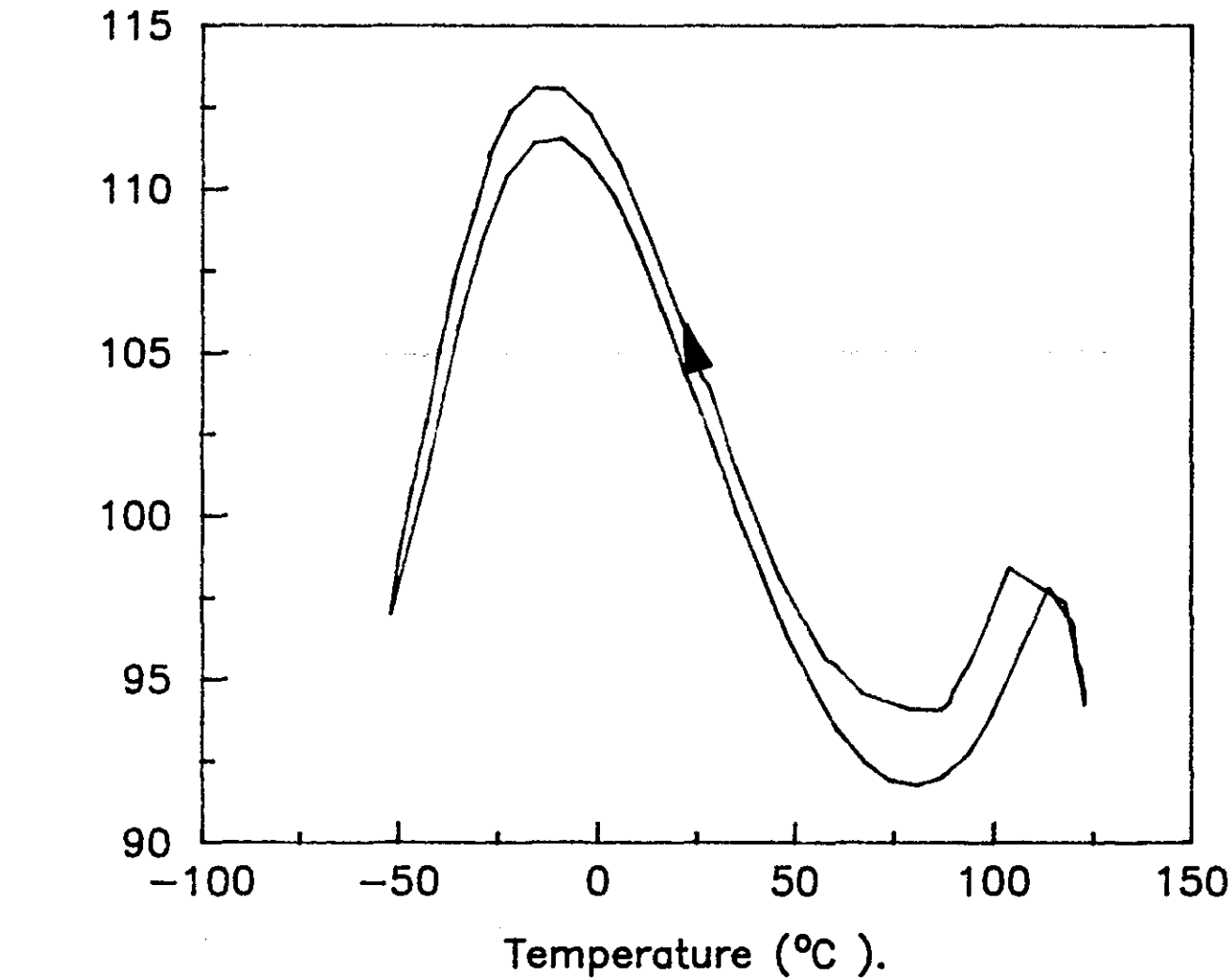


Fig 61. Variation of capacitance with temperature of 1812 size Corning capacitors (X7R dielectric).



7.3 Mechanical Cycling

The board bending tests have been conducted with a surface strain in the PWB Of 0.18% which is approximately equal to the strain generated by cycling from -55°C to +125°C. The tests on 1206 size resistor chips were conducted at three cycle speeds - 1/hour, 30/hour and 600/hour. The results are shown in Figure 62.

Mechanical cycling tests have also been conducted on 1812 size capacitors at 1 cycle/hour and 30 cycles/hour and the results are shown in Figure 63.

The test waveform for the two slowest cycle speeds (1/hour and 30/hour) was a squarewave, that is the PCB was bent and held for half the cycle duration and then released for the remainder of the cycle. The fastest cycle test waveform was sinusoidal as the motor was running continuously.

In the tests on both sizes of components the cracks in the solder fillets generally initially open and close as the board is bent and released, but eventually become permanently open. This effect is probably due to oxidation of the fracture surfaces. This will both force the crack to open wider and prevent electrical contact between the fracture surfaces. Figure 64 shows a typical fracture of a solder fillet after mechanical cycling.

In a purely mechanical fatigue test such as this, the Coffin-Manson relation [2] is a good model for the fatigue life, that is:-

Fig 62. Failures in board bending test on 1206 size resistor chips.

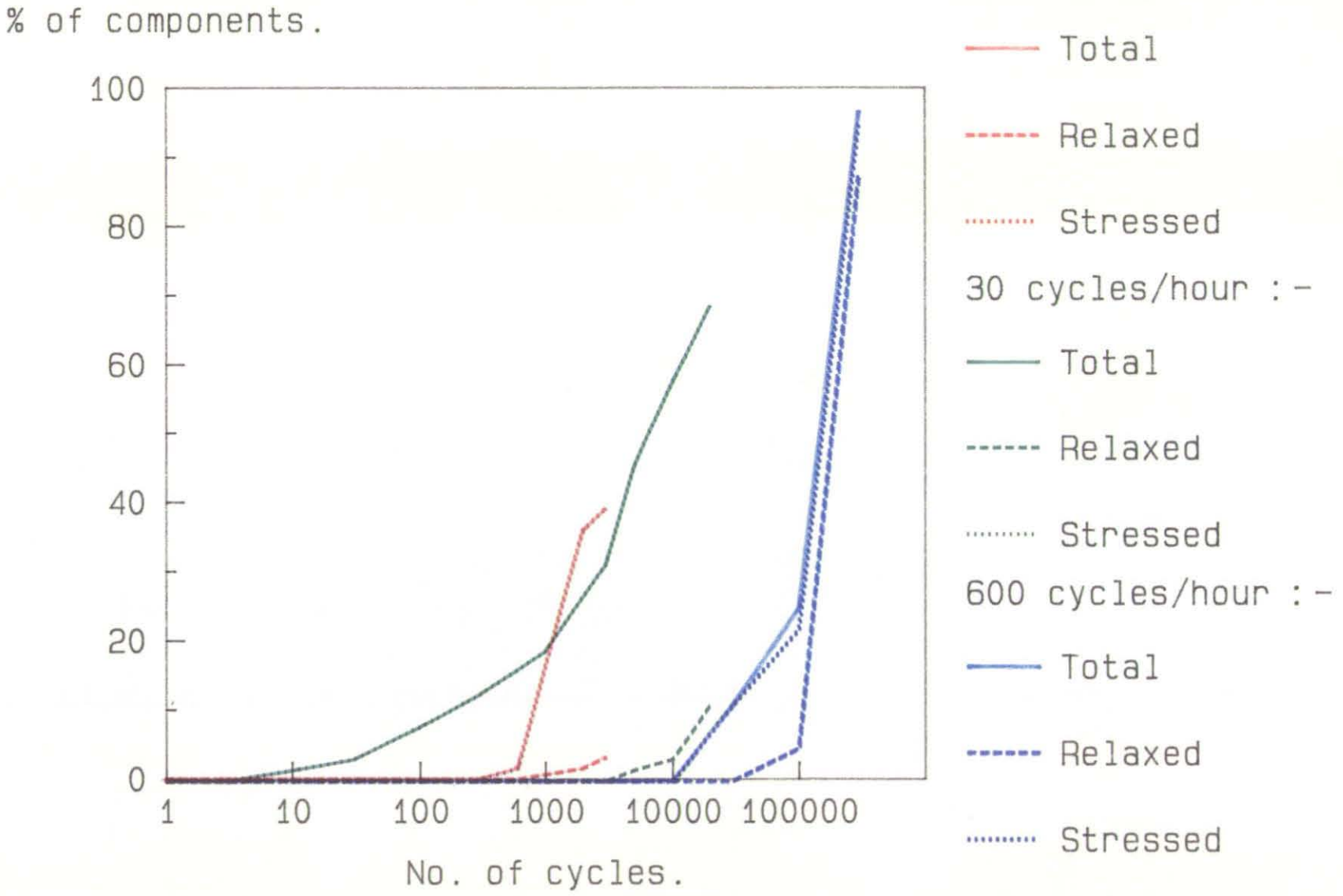
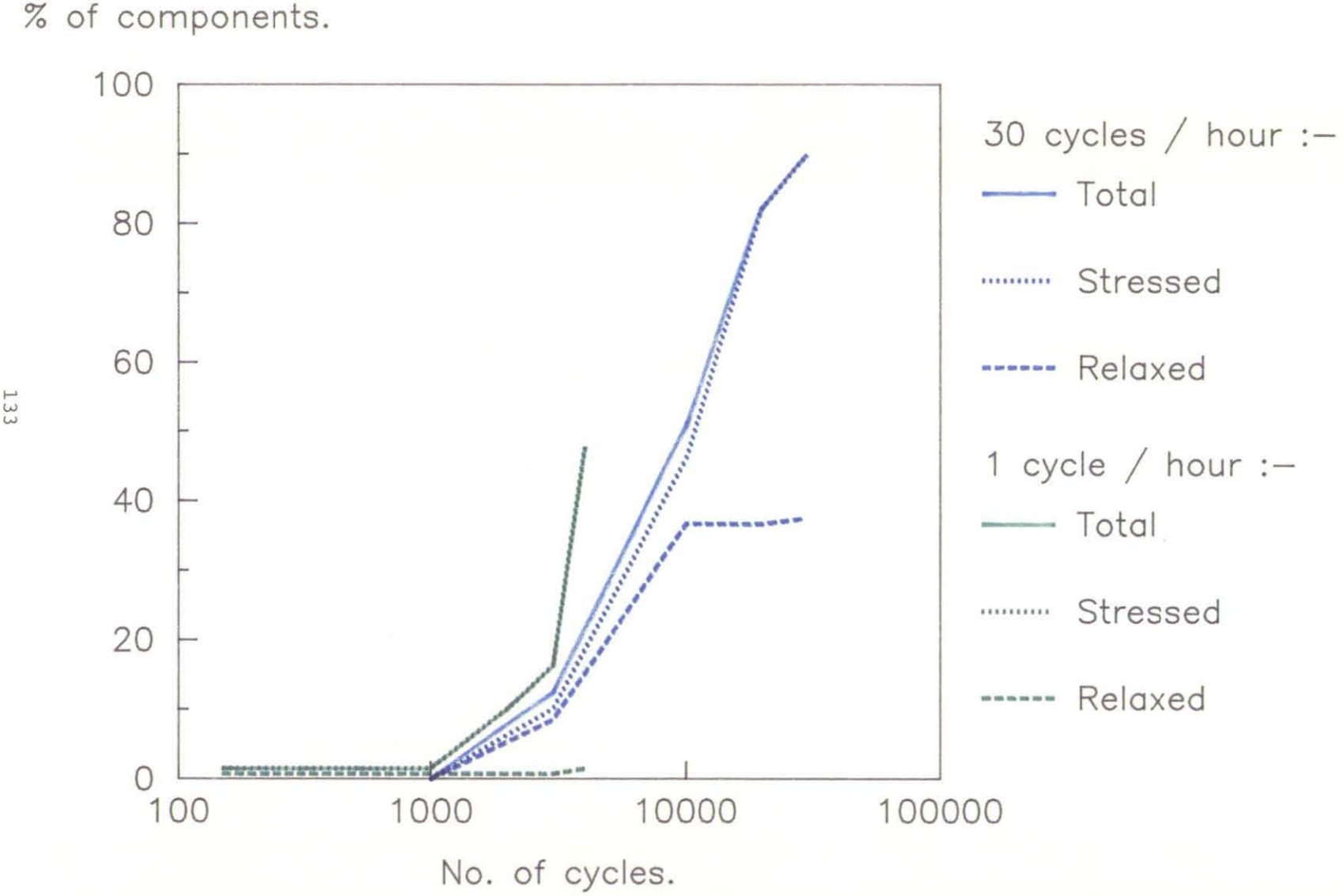


Fig 63. Failures in board bending tests on 1812 size Corning capacitors.



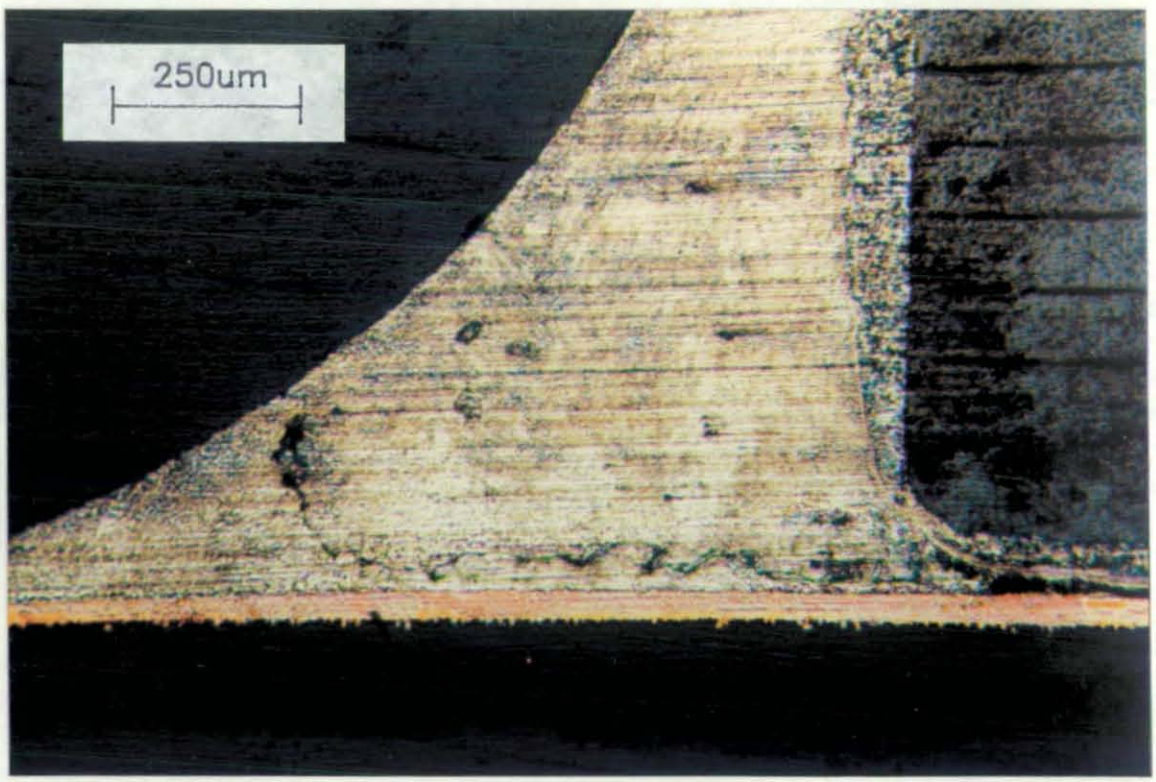


Figure 64 Fracture of Solder Fillet After Mechanical Cycling

$$Nf = (\epsilon f/2\epsilon p)^2 \quad (7)$$

Where Nf is the number of cycles to failure, ϵf is the fracture ductility of the solder and ϵp is the plastic strain per cycle. If the fracture ductility of the solder joints follows a normal distribution as expected, then the distribution of failures should fit a log-normal distribution. The data in Figures 62 and 63 have therefore been fitted to a log-normal distribution and the estimates of mean lives to failure against cycle speed are shown in Figure 65.

7.4 Damp Heat

The initial damp heat tests on 1206 STC capacitors and 1206 resistors were limited by the mechanical failure of the connectors used to connect the test coupons to the measuring system. These were total mechanical failures caused by deterioration of the plastic moulding after between 1000 and 2000 hrs. Both steady state and combined damp heat tests were conducted. Only small changes were detected in the parameters of the components tested and the leakage currents of the capacitors were not monitored during these tests.

Subsequent steady state damp heat tests at 85°C/85%RH have been conducted on 1206 size STC and 1206 and 1812 size Corning capacitors. Additionally a combined temperature cycling/damp heat test has been performed on a coupon of 1812 size Corning capacitors. These tests have included monitoring of leakage currents and significant numbers of leakage current failures were detected in addition to capacitance and dissipation failures (Figure 66, 67, 68 and 69). The discontinuities in Figure 69 are due to the changes occurring in the components

Fig 65. Relationship between solder joint fatigue life and frequency in board bending tests.

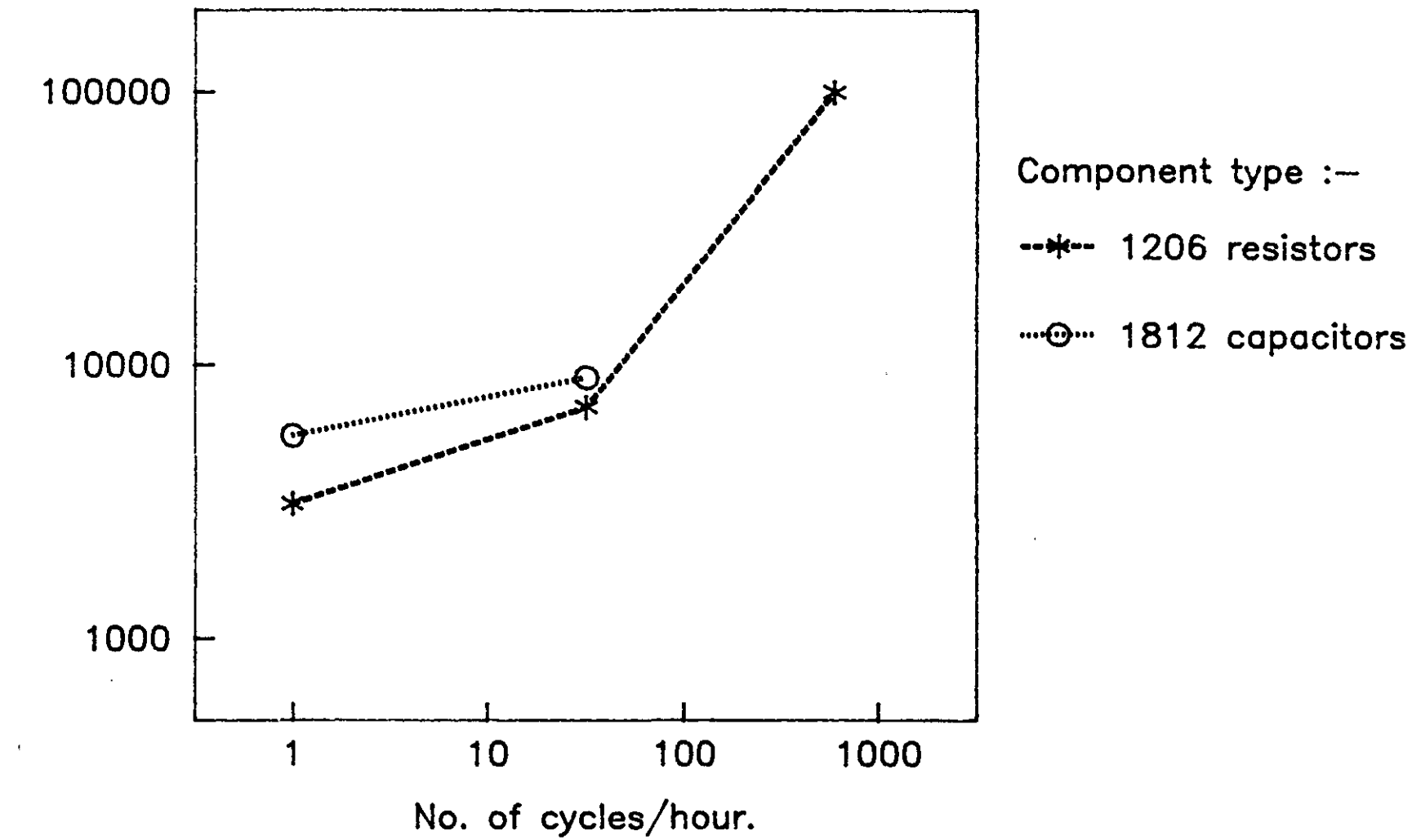


Fig 66. Failures in damp heat test (85 ℃/85%R.H.)
on 1206 size STC capacitors.

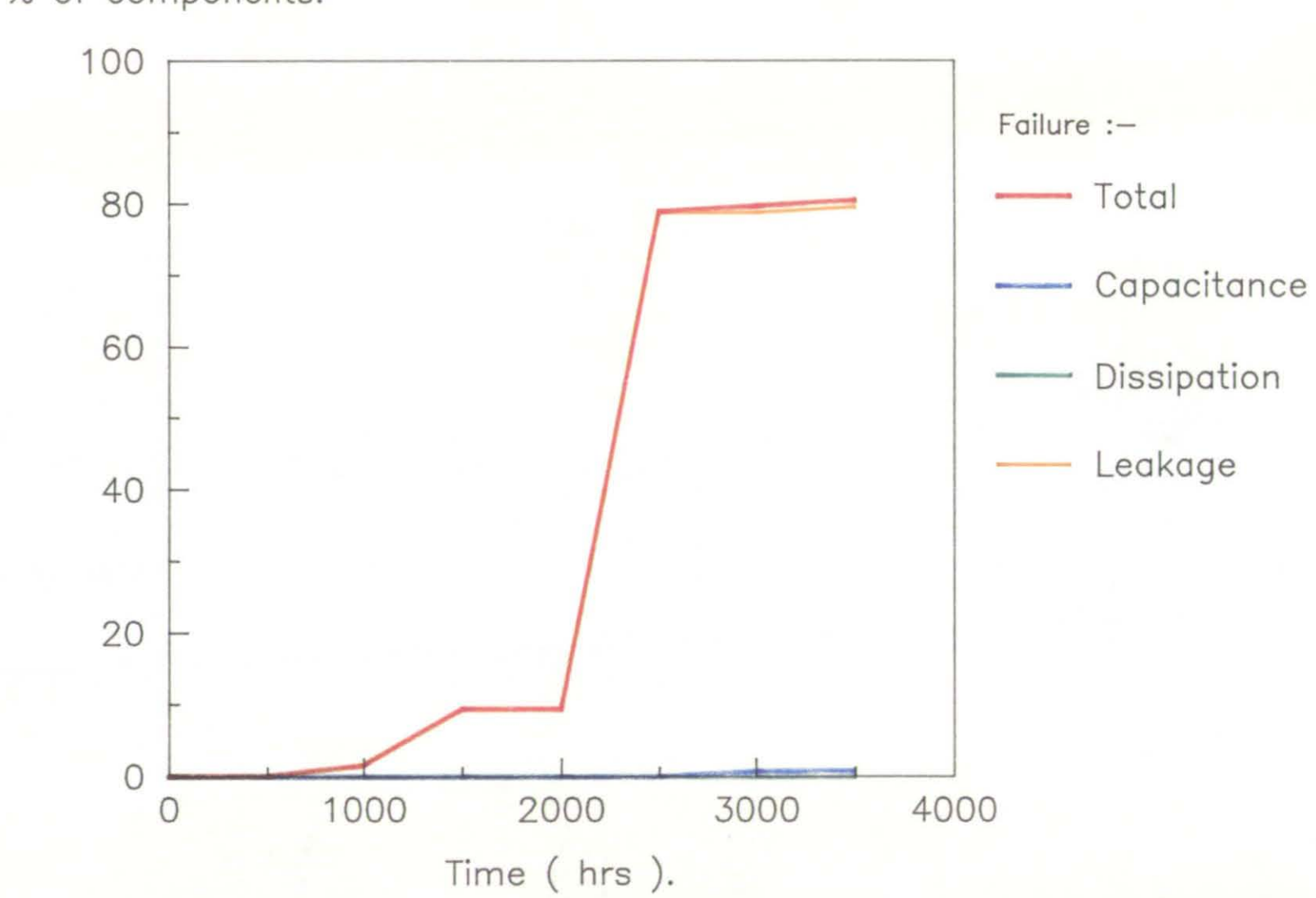


Fig 67. Failures in damp heat (85°C/85%R.H.) test on 1206 size Corning capacitors.

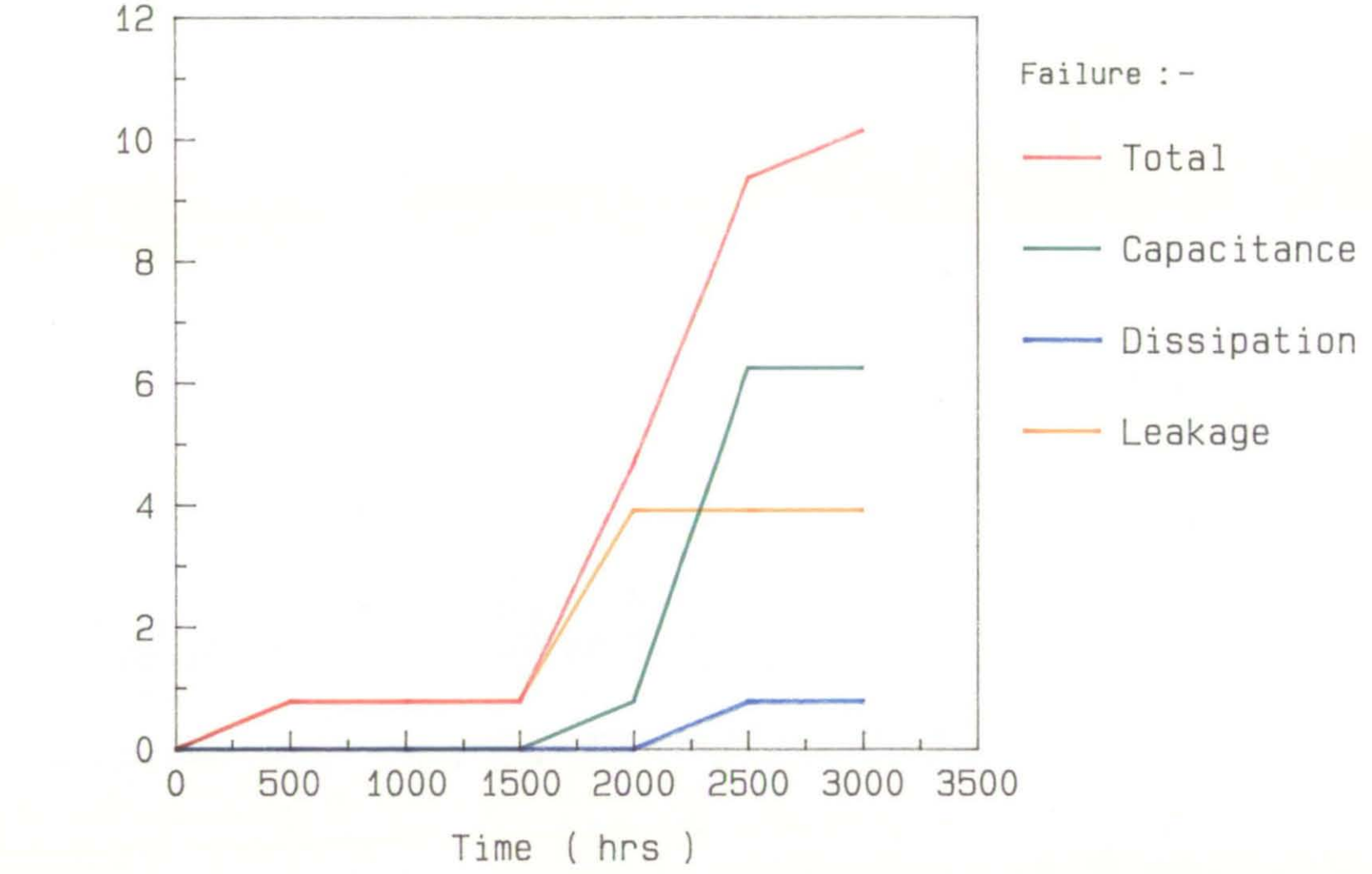


Fig 68. Failures in damp heat test (85 ℃/85%R.H.)
on Corning 1812 capacitors.

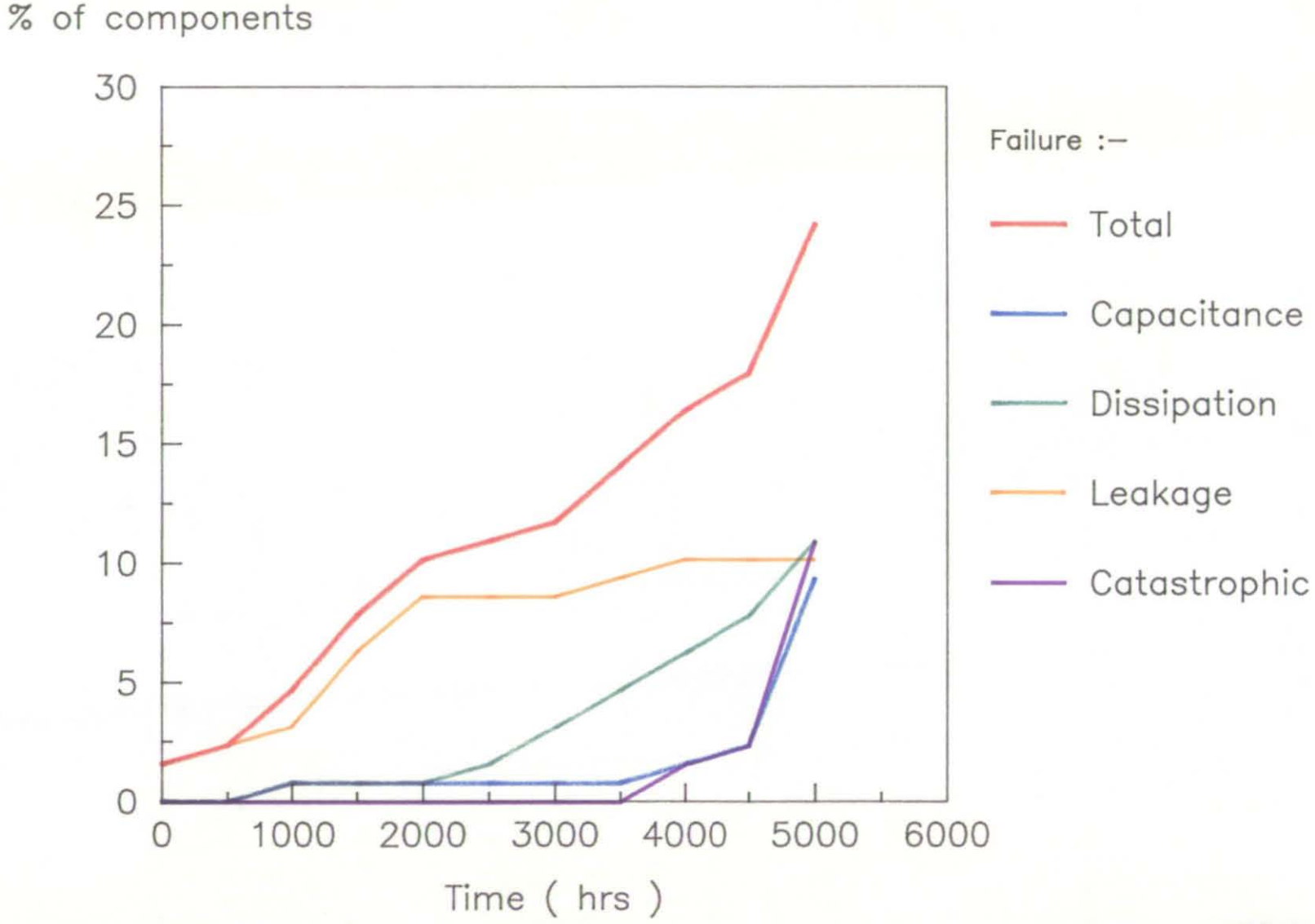
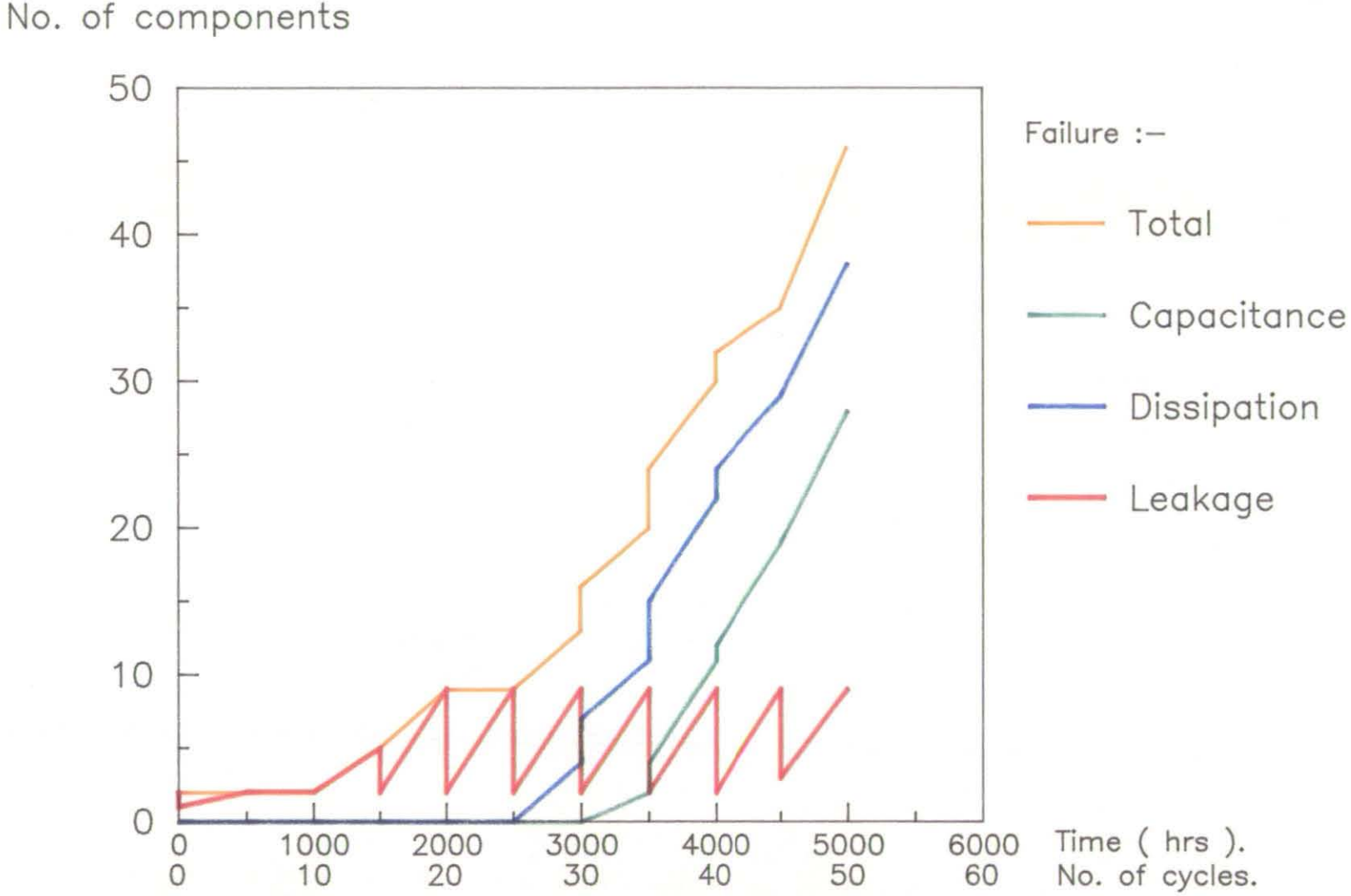


Fig 69. Failures in combined damp heat / temperature cycling test on 1812 size Corning capacitors.



parameters during the temperature cycling phase of the combined test, i.e., every 500 hours. The fact that the temperature cycling phase reduces the number of apparent leakage current failures suggests that the conduction mechanism is caused by the presence of moisture, i.e. is ionic. This moisture is subsequently dried out by the temperature cycling phase and hence the conductive path is temporarily removed.

In order to try to isolate whether these leakage current failures were attributable to the component or the attachment method, three further coupons were tested. Two of these coupons carried no components, but had a dot of adhesive placed between the PWB pads. One of these coupons was passed through the wave soldering machine ('glue A') and the other was not ('glue B'). A third of these coupons was assembled using dummy components. These dummy components were resistor chips which had their resistive track removed by air abrasion to leave a ceramic block with metallised ends.

The results of these tests are inconclusive (Figure 70), but do suggest that the glue used may have some influence on the situation.

7.5 Thermal Mapping

The thermal response of a 1206 size resistor chips is shown in Figure 71 and an estimate of the thermally induced strains occurring in the solder joints given in Figure 72. This estimate of strain is based on a simple linear expansion model using thermal expansion coefficients of 7×10^{-6}/°C for the resistor, 14×10^{-6}/°C for the capacitor and 23×10^{-6}/°C for the PWB. Estimating the strains occurring in the

Fig 70. Failures in damp heat (85 °C/85%R.H.) test on glue spots and dummy components.

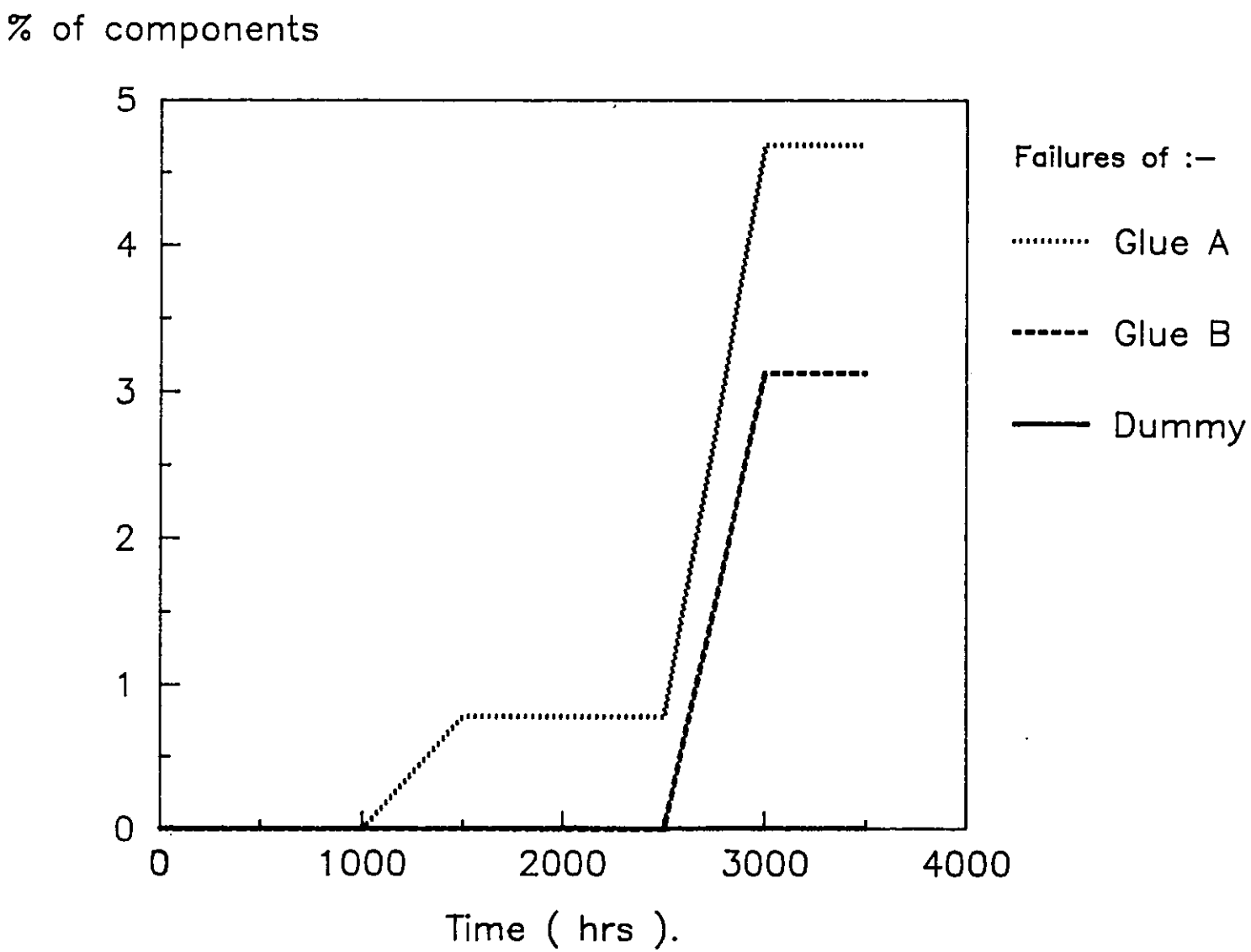


Figure 71 Temperature Changes in 1206 Components During a Power Cycle.

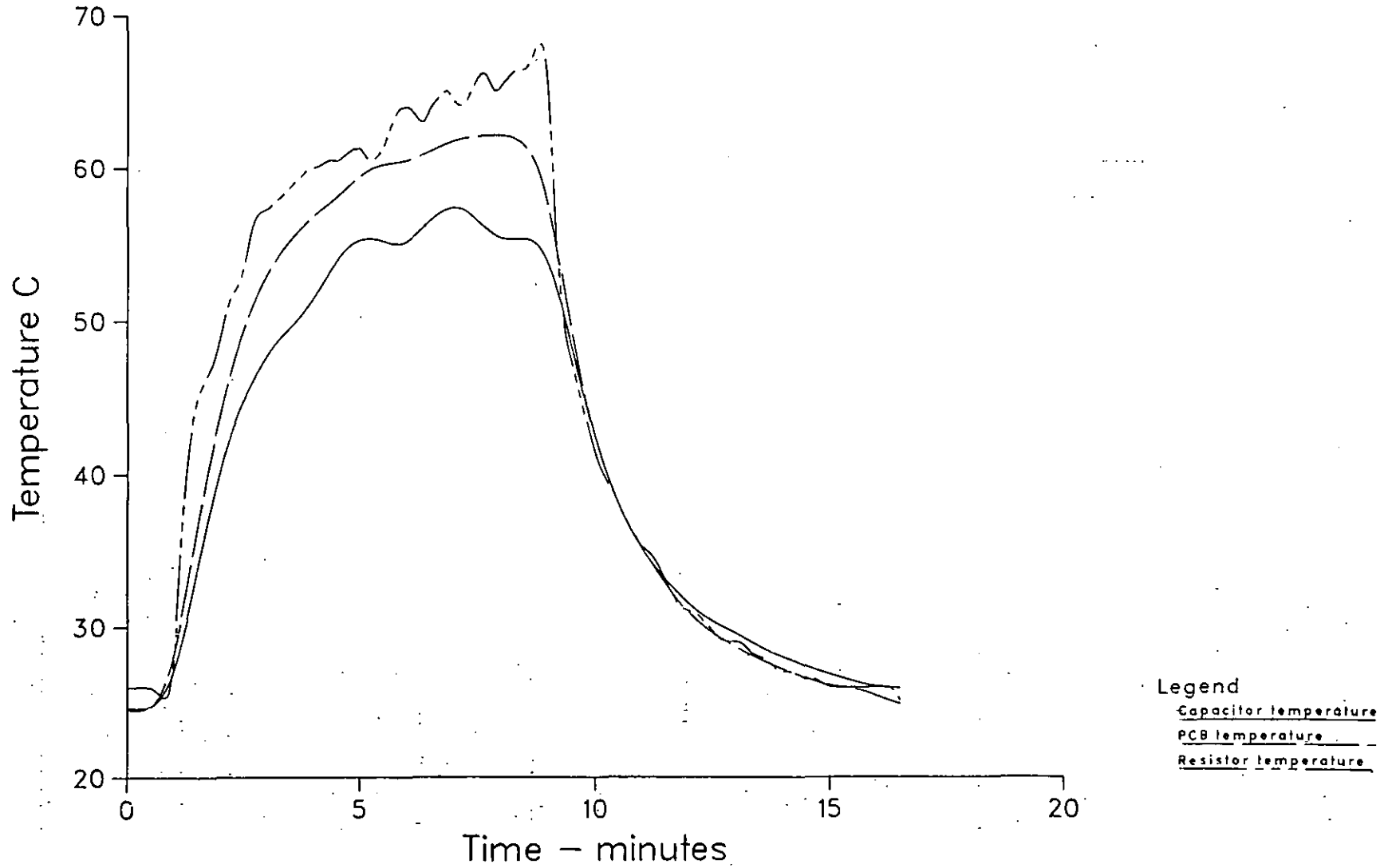
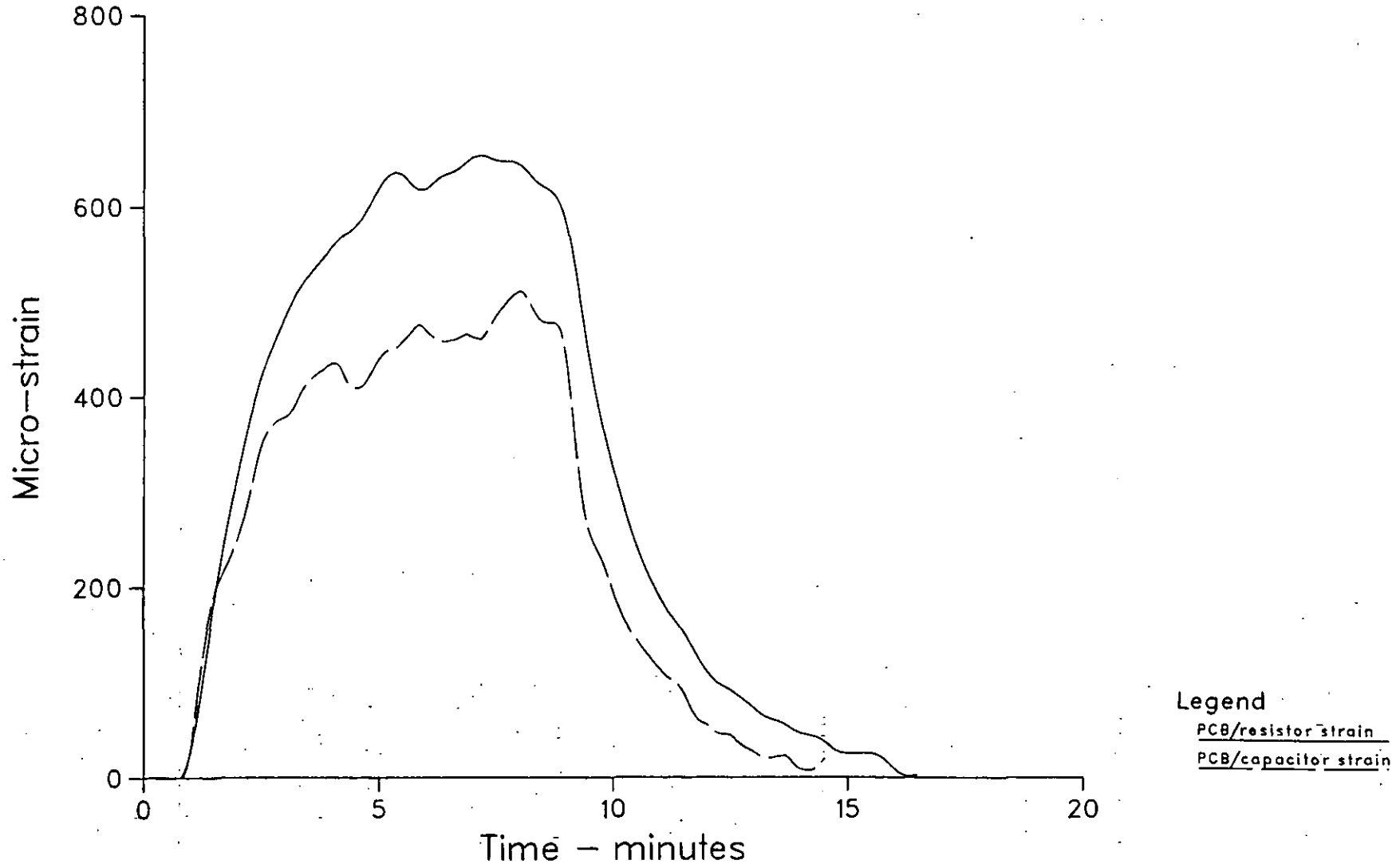


Figure 72. Strain Levels in 1206 Components During a Power Cycle



SOT-23 packages is much more complex because the package is non-homogeneous, i.e. it consists of the chip resistor, the lead frame and the encapsulant, all with very different mechanical properties. Finite element modelling is considered the only way of accurately assessing the stresses in this type of package.

The Agema thermal imaging system has allowed an examination of the temperature distriubtions occurring for both the chip components (Figure 73) and the SOT-23 components (Figure 74). In Figure 73 the most densely packed group of components on the thermal mapping coupon is shown, with the eight film up resistors dissipating full power (125mW) surrounding a ceramic chip capacitor. The two imaging boxes called AR1 and AR2 are drawn to the same size as the capacitor and resistor. The figures in the table at the side of the image show the temperature extremes (EXT) and average and standard deviation of temperature (STA) within the boxes. Little difference was found between components on 1.6mm FR4 and those on 0.8mm FR4. It may be seen from Figure 73 that the temperature rise of the capacitor is close to that of the resistor.

The SOT-23 resistor chips are specified to be capable of dissipating 500mW when soldered to a substrate with heat sink capability of 150°C/W or less. The maximum package temperature is specified to be 125°C at an ambient temperature of 50°C, i.e. a package temperature rise of 75°C. The actual temperature rise on an alumina substrate was found to be 40°C, i.e. a substrate thermal resistance of 80°C/W. The temperature rise on a large area of 1.6mm FR4 substrate however is 105°C at 500mW (210°C/W). The temperature rise when these components

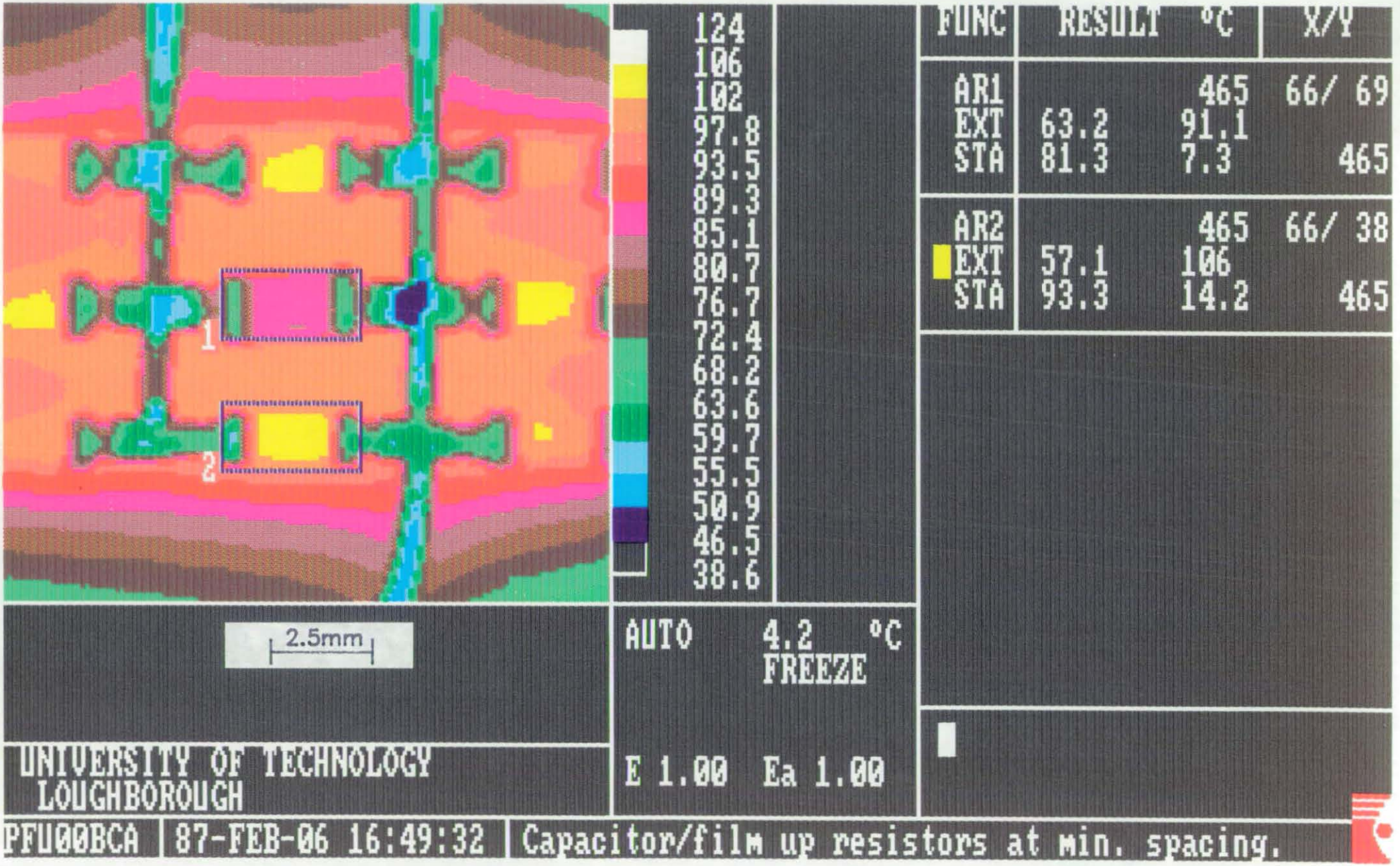


Figure 73 Thermograph of 1206 Size Components

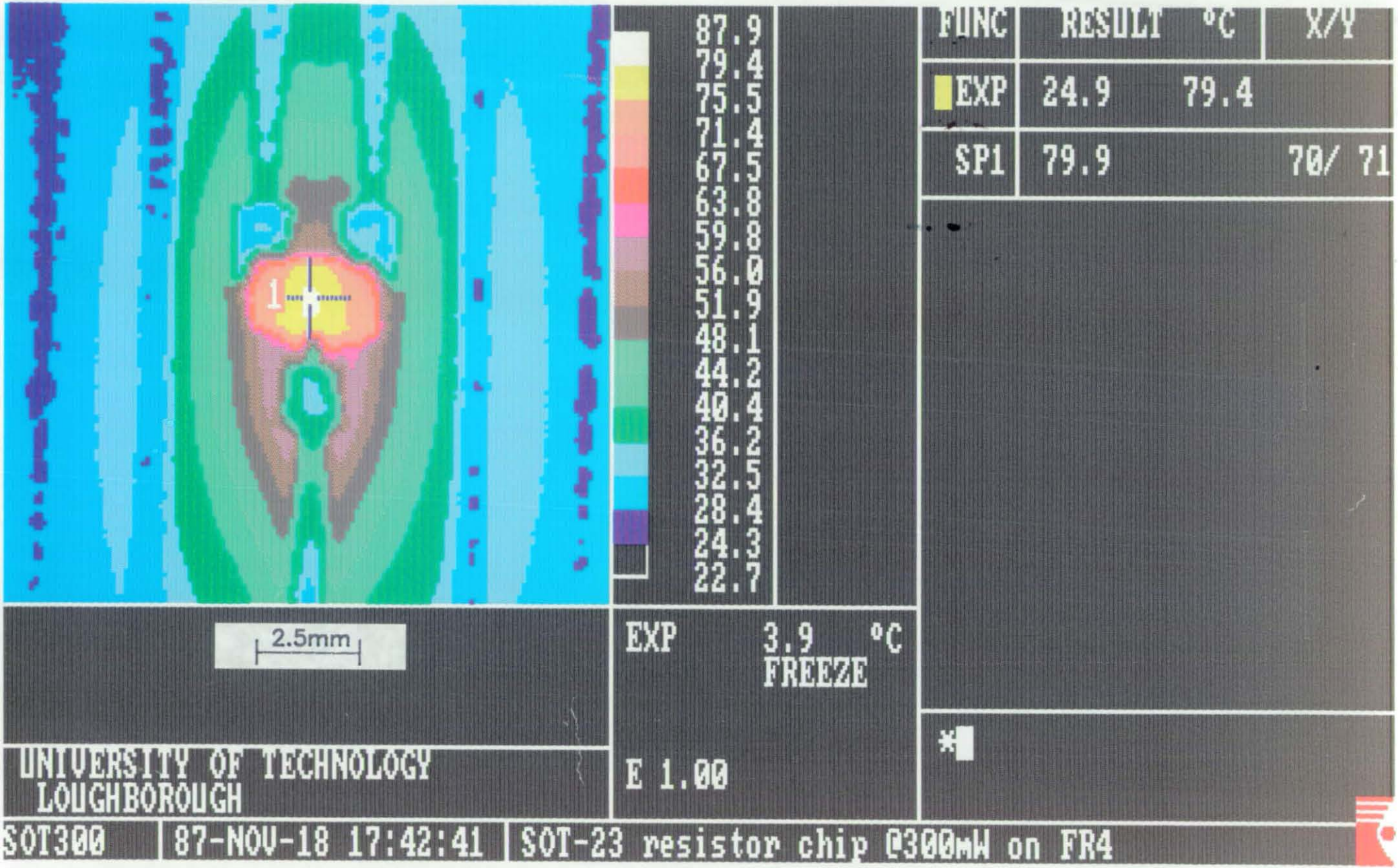


Figure 74 Thermograph of SOT-23 Resistor Chip

are densely packed is even higher and thus the power dissipation in the power cycling test has been limited to 300mW per device to limit the temperature rise to 75°C. Figure 74 shows a single SOT-23 chip dissipating 300mW on a large area of FR4, giving a temperature rise of 55°C (the spot reading SP1 at the point marked by the cursor '1' is 79.9°C and the ambient temperature was 25°C.

7.6 References

1. J. Herbert, "Ceramic Dielectrics and Capacitors", Electrocomponent Science Monographs, p 145, Vol. 6, 1984.

2. S.S. Manson "Thermal Stress and Low-cycle Fatigue", McGraw-Hill Book Co., 1966.

CHAPTER EIGHT - CONCLUSIONS

1. The reliability of the solder joints of the small chip components tested appears to be adequate provided they are initially well soldered. Only one solder joint failure has been observed in all the power and temperature cycling tests conducted and this was in a poorly soldered joint. The tests have included over 1500 components and nearly 5 million component hours of testing.

2. Mechanical cycle testing is the most rapid testing technique for these types of assemblies. Even greater accelerations might be achieved by adding conditions to the test which promote fracture surface corrosion and crack growth, for example damp heat.

3. Temperature cycling from -55° to +95° gives the fastest degradation of solder joint resistance in this type of test on FR4 printed circuit boards, i.e. an increase of 5% in 100 cycles compared with only 1% in 100 cycles for the -55 to +125°C test.

4. Whilst the damp heat tests were conducted for very long periods of time and were therefore very severe, the results suggest care must be exercised in component choice and assembly techniques and materials. This is especially so when the leakage currents of capacitors and semiconductors are an important aspect of circuit design.

APPENDIX 1

TEST EQUIPMENT

(a) Thermal chamber system

The thermal chamber requires a 0 to -5v signal to set its temperature and returns a 0 to -5v signal giving its current temperature. Additionally a 24V signal is required to switch the heat pumps off and turn the heating coil on. Figure 75 shows the circuit diagram of the interface that has been built between these signals and a PET computer.

The thermal chamber control program is listed below.

(b) Board bending system

The board bending system is driven by a stepper motor interfaced to a PET computer. The circuit diagram of the interface is shown in Figure 76 and the program is listed below.

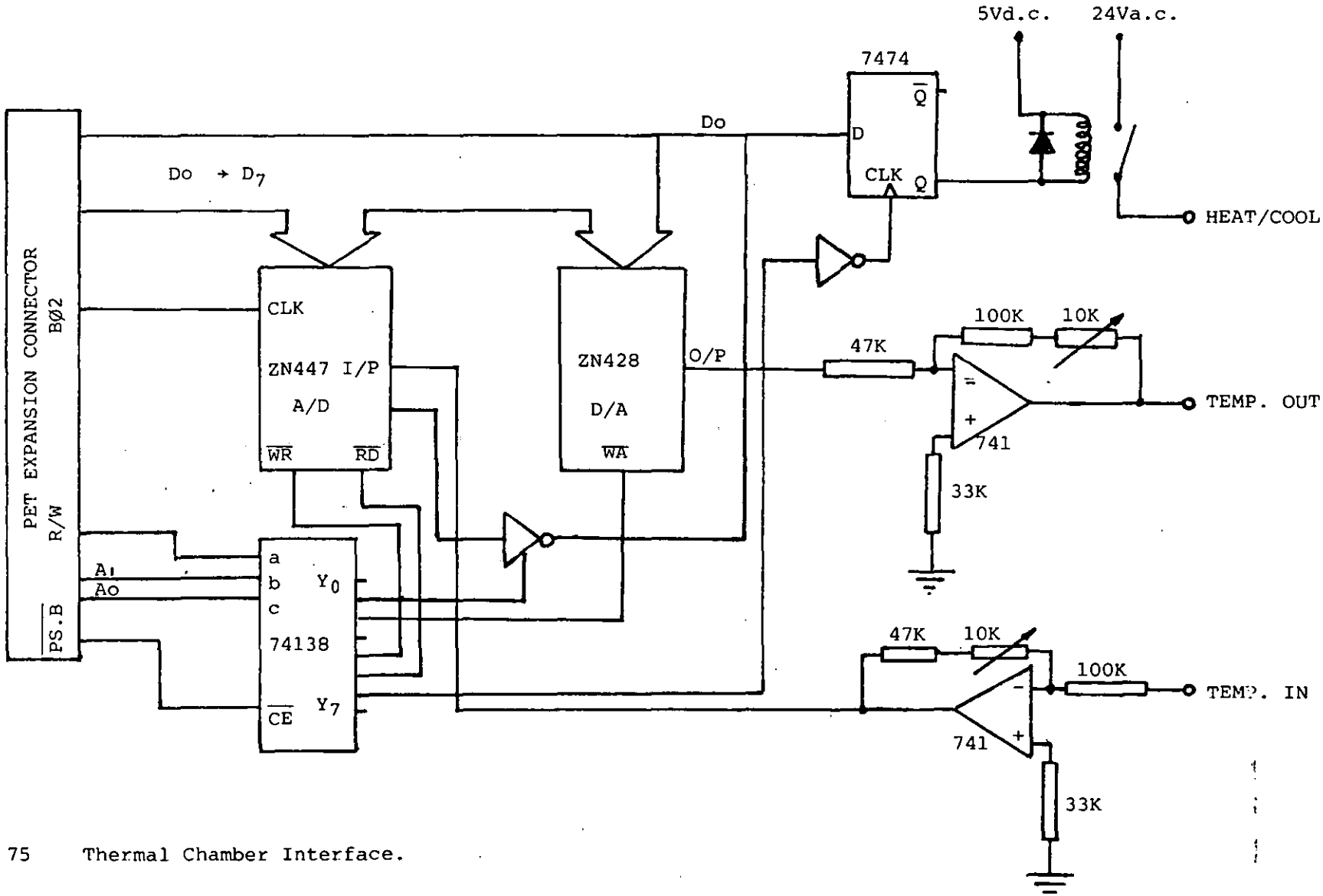


Figure 75 Thermal Chamber Interface.

```
5 poke 59459,255
10 print"■":for x=1 to 7:print:next
20 print:print"        tmax";:input ht
30 print:print"        tmin";:input lt
40 print:print"tmax d time";:input d1
50 print:print"tmin d time";:input d2
60 print:print"numb cycles";:input n
70 print:print"dt/min  max";:input dt
80 ht=ht+100:lt=lt+100:ct=d1+d2
90 tr=(ht-lt)/dt:if tr>d1 or tr>d2 then 10
95 d2=3600*d2:d1=d1*3600
100 for a=1ton:gosub200:next
110 tw=130:poke 40962,tw
120 poke40963,0:poke59457,255
130 gosub1000
140 ift<130then130
160 end
200 poke 40963,0:ti$="000000"
205 poke59457,255
210 poke40961,0:l=0:z=0
220 t=peek(40961)
230 if(ht<t)and a=1 then l=1:goto300
235 ifa>1or t>ht thent=lt
240 for b=ttoht
245 gosub1000
250 p=b+5
255 ift>htthenp=ht-v:v=v+.005
260 poke40962,p
265 tw=ht
270 gosub 1000
280 if(ti-z)<(3600/dt)and ht>t then 270
285 z=ti
290 next
291 poke59457,0
292 ift>htthenpoke40962,ht-v:v=v+.005
293 ifv<0then poke40963,0
294 ift<htthenpoke40962,ht-v:v=v-.005
295 ifv>1then poke40963,91
296 gosub1000
298 if ti<d1 then 292
299 v=0 : z=0
300 poke40963,91:ti$="000000":z=0
302 poke 59457,255
305 if l=0then t=ht
310 for b=t to lt-5 step-1
315 gosub1000
320 p=b-10
325 ift<ltthenp=lt+v:v=v+.005
330 poke40962,p
335 tw=lt
340 gosub1000
350 if(ti-z)<(3600/dt) then 340
355 z=ti
360 next
365 poke59457,0
370 gosub1000
374 ift>ltthenpoke40962,lt+v:v=v-.005
375 ift<ltthenpoke40962,lt+v:v=v+.005
376 if l=1thenft=ti
380 if ti<d2 then370
390 v=0
400 return
```

```
1000 print"S"
1010 poke40961,0
1020 t=peek(40961)
1025 tn=((a-1)*(d1+d2)+ti)/3600
1026 d=int(tn/1440)
1030 print"        current temperature is";"      ■■■■■";(t-100):print
1040 print"       required temperature is";"      ■■■■■";( tw-100 ):print
1050 print"number of cycles completed is";( a-1 ):print
1060 print"             time from start is";d;":";( int((tn-d*1440)/ 60 ))
1070 return
```

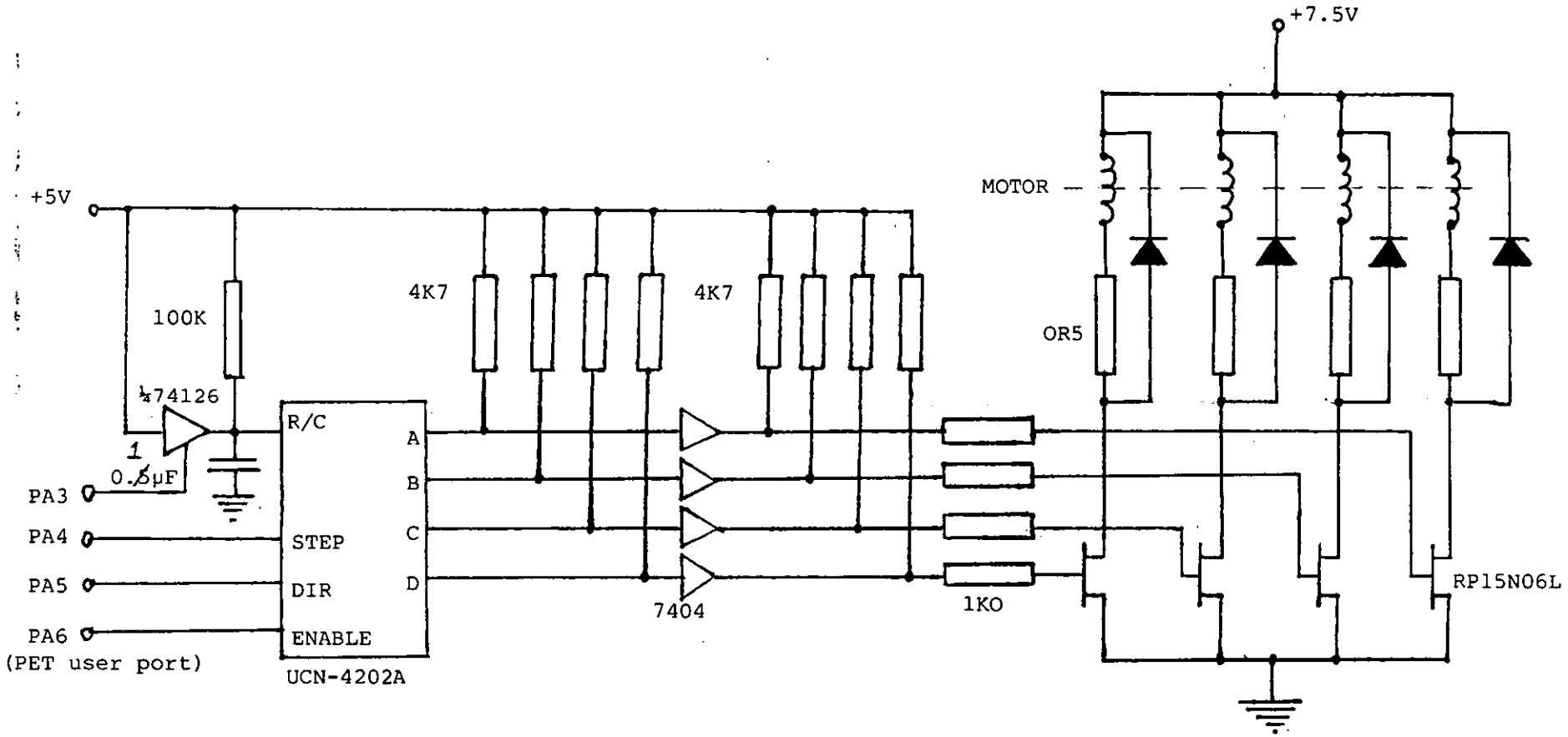


Figure 76 Stepper motor interface

```
 print"■"
0 poke59459,255
5 gosub 1000:print"■"
0 print"   number of cycles required";
0 input n0:print
0 print"sine or square profile (0/1)";
0 input s:s=s+1
0 on s gosub 3000,2000
0 goto 40
0 end
000 for x=0to14
010 read y
020 poke 700+x,y
030 next
040 data 169,24,141,79,232,234,234,234,234,169,00,141,79,232,96
050 print:print:print"press < or > to zero shaft, return":print"to continue"
060 get a$:if a$=""then 1060
070 if a$=">"then poke 59457,56
080 if a$="<"then poke 59457,24
090 poke 59457,0
100 if a$=chr$(13) then return
110 goto 1060
2000 print:print"    no stress dwell time (s)";
2010 input d1
2020 print:print"     stressed dwell time (s)";
2030 input d2
2035 print:print:printn;"   cycles completed"
2040 ti$="000000"
2050 for x=1to100
2060 poke 59457,28:poke 59457,4
2065 next
2066 poke59457,64
2070 if ti<60*d2then gosub 5000:goto2070
2080 ti$="000000"
2090 for x=1to100
2100 poke 59457,24:poke 59457,0
2105 next
2110 poke59457,67
2115 n=n+1:print "■";n:if n=n0 then end
2120 if ti<60*d1then gosub 5000:goto 2120
2130 goto 2040
3000 print:print"              cycle time (s)";
3010 input t
3015 print:print:printn;"   cycles completed"
3020 ti$="000000"
3030 for x=1to200
3040 sys(700)
3050 if ti/x<3/10*t then 3050
3060 next
3065 poke59457,2
3070 n=n+1:print "■";n:if n=n0 then end
3080 goto3020
5000 print:print:print:print
5005 print"              ";ti$
5010 print"■■■■";
5020 return
```

CORNING CAPACITOR CONSTRUCTION

CORNING'S A.C.E. CERAMIC CAPACITOR

A.C.E. is Corning's acronym for the Advance Corning Electrode process, a patented technology, perfected by Corning. Hundreds of millions of A.C.E. capacitors have been inserted in electronic equipment worldwide since their market introduction in 1977.

The A.C.E. process forms the capacitor by injecting lead alloy electrodes into the ceramic chip's electrode sites. The ceramic body, the dielectric, is optimally fired prior to the injection of the electrodes. The process differs from the common practice of firing the ceramic and electrodes simultaneously. This eliminates the possibility of co-firing delaminations, a major contributor to reduced reliability in MLC's. The A.C.E. process parallels thick film hybrid construction because co-firing of dissimilar materials is not practiced. Materials are fired in a step by step process to optimize their circuit characteristics.

A.C.E. TECHNOLOGY ADVANTAGES

RELIABILITY
Dramatic Reduction of Internal Defects.

- Delamination free characteristic
- High density, comparatively void-free dielectric. Outstanding low voltage performance (<10 V DC).
- Reliable dielectric thickness
- Non-Noble lead alloy electrodes — least susceptible to low voltage failure mode.

COST

- Lead alloy replaces precious metals or their alloys.
- Cost stability, freedom from fluctuations in precious metal markets.

PERFORMANCE
Reliable Low ESR Inherent in Construction.

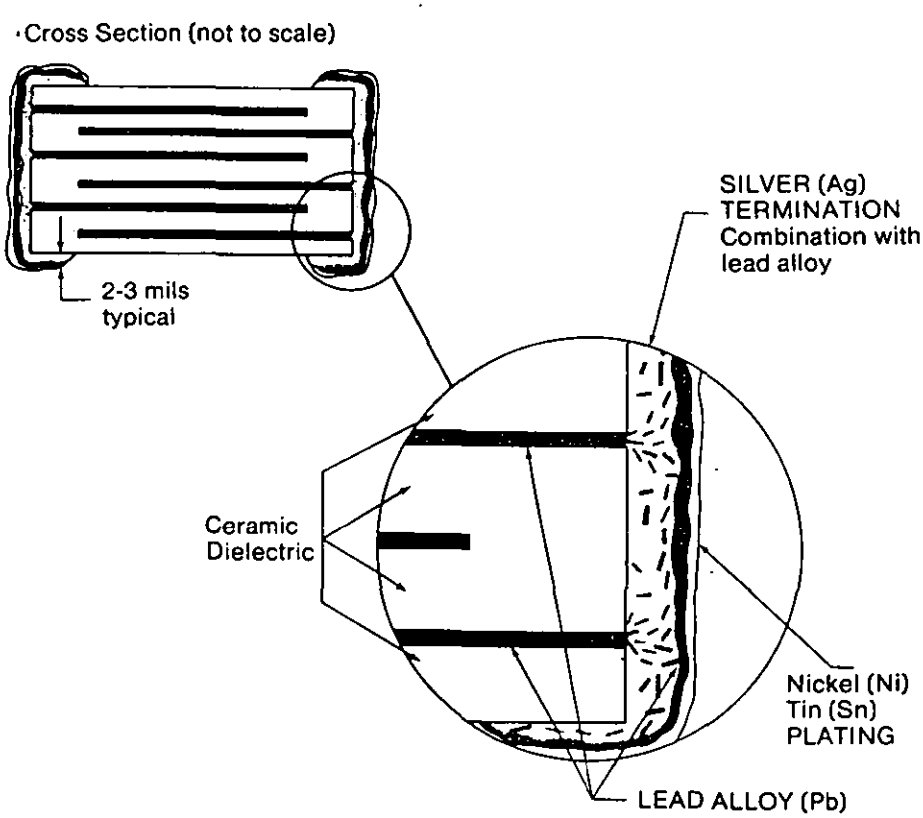
- Elimination of bonding difficulties between external terminations and internal electrodes ensures a continuous low resistance connection.
- Optimized Dielectric properties -- Freedom to optimize dielectric due to absence of electrodes during firing. Important to low ESR at high frequencies.

CONSERVATIVE DESIGN

- Dielectric thickness and electrode margins comply with high reliability specification design practice.
- Designed with comparatively lower dielectric operating stress (volts per mil).

THE DOUBLE BARRIER LAYER TERMINATION

- Double Barrier Layer prevents leaching and allows soldering with standard solders (non-silver bearing). This termination is leach resistant to relatively harsh wave reflow and vapor phase soldering systems, withstanding immersion in 260°C solder beyond 90 seconds.
- Beneath the nickel barrier a softer lead alloy layer acts as a compliant termination providing stress relief from thermal expansion coefficient mismatch to the substrate or circuit board.



CORNING LIMITED, Electrosil Division, P.O. Box 37, Pallion, Sunderland, Tyne & Wear SR4 6SU.
Tel: Sunderland (0783) 44155. Telex 53273

CORNING LIMITED
Electrosil Division P.O. Box 37, Pallion, Sunderland. Tyne & Wear. SR4 6SU. Tel: Sunderland (0783) 44155. Telex: 53273

A.C.E. (Advance Corning Electrode) Technology IMPROVES THE RELIABILITY OF MULTI-LAYER CERAMIC CAPACITORS

Multi-layer ceramic capacitors no longer have to suffer the effects of delamination or porosity, two virtually undetectable defects that are the chief reasons for field failures. This is due to a new manufacturing process developed by CORNING LIMITED.

DELAMINATION

Delamination is a partial separation of one or more of the ceramic and metal layers of the capacitor, as shown in *fig. 1.*

Delamination is caused by a failure in manufacturing and not by a failure in application, but the presence of delamination as the capacitor starts in service may lead to field failure. High voltage, High temperature, time, moisture, and low polarizing voltages in combination with moisture can promote field failures in the presence of delamination. Field failures usually manifest themselves as low values of insulation resistance, or in the extreme case, as electrical shorts.

POROSITY

The porosity shown in *fig. 1,* (small black dots), is also a manufacturing defect. Its usual cause is an underfired body.

Porosity, like delamination, can lead to field failures. If the porosity is extensive, there is usually some degree of interconnection among the pores. The interconnection paths allow external moisture, which inevitably permeates the capacitor coating, to reach opposing electrodes. In presence of moisture and polarizing voltages, the metal electrodes can form electrochemical dendrites that bridge the pores and cause electrical short circuits. The shorts are self-clearing under certain conditions of applied voltage and circuit impedance, but the self clearing process injects noise into the circuit. If the shorts do not clear, the capacitor fails and sometimes causes failure of circuit function.

The conventional process to manufacture multilayer ceramic capacitors is to sinter a structure composed of alternate layers of dielectric powder ($BaTiO_3$) and precious metal powders (Pd,Ag) which have very different coefficients of expansion. The sintering process presents a real challenge to the ceramic engineer, who must define the firing temperature by taking into account the non-uniform shrinkage of these dissimilar materials and the evaporation temperature of the electrode metals. To manufacture capacitors with this technique four objectives must be met.

The ceramic dielectric must be sintered to develop its electrical properties and then its density must be increased to maximise mechanical strength. The precious metal electrode must also be fired to obtain correct electrical conductivity and finally create a large metal to ceramic seal between adjacent dielectric layers.

Optimizing all four objectives is very difficult because of the chemical and mechanical differences between the metal and the ceramic. Not only are their chemical bonds different, but they also shrink at different rates during the heating and holding portions of the firing, thus creating a displacement between ceramic and metal. Additional displacement occurs because palladium experiences a 25% volume change during oxidation and reduction when heated in air at 500°C to 900°C. As the rigid ceramic cools, a difference in thermal expansion rates between the metal and the ceramic generates large shear stresses at the interface of the two materials.

Each of these incompatibilities – chemical bond, shrinkage rate, and co-efficient of expansion renders a reliable ceramic-to-metal seal between layers difficult to obtain. If the seal is bad, delamination occurs, and if the ceramic is not dense enough, the capacitor is porous.

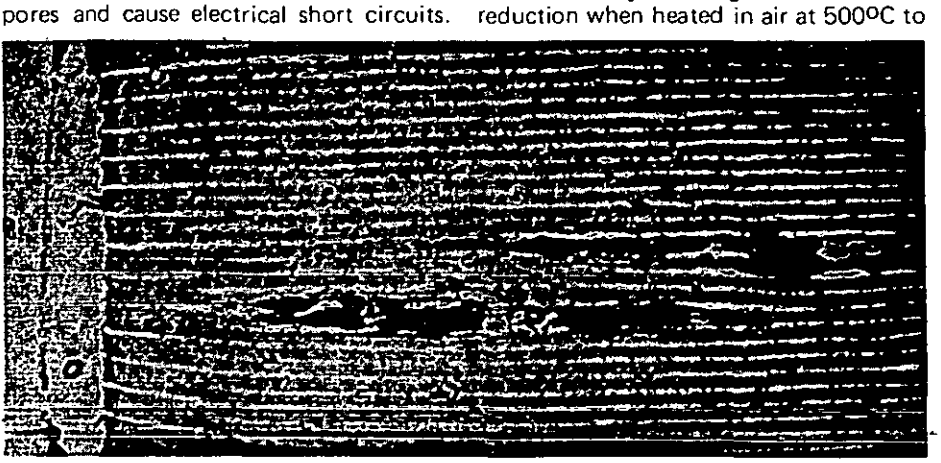


Figure 1

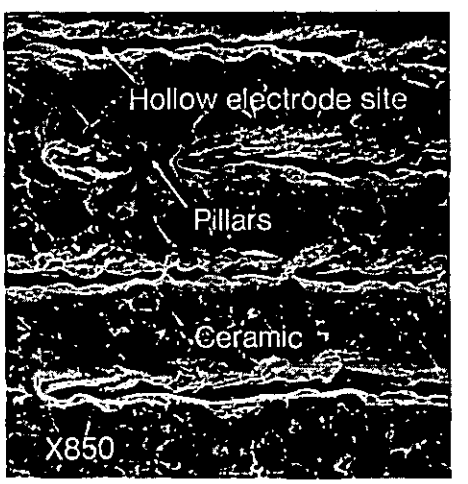


Figure 2

In contrast to the conventional approach, the Corning A.C.E. (Advanced Corning Electrode) process does not co-fire the ceramic dielectric and electrode metals. Instead, hollow electrode sites are built into the ceramic body before firing. And then, after the ceramic has been optimally fired by itself, the hollow electrode sites are backfilled with electrode material. All the problems associated with co-firing are avoided. The hollow electrode sites, as shown in *fig. 2,* are created by using a temporary fugitive electrode. In the A.C.E. process, the temporary electrode is a carbon-like material that survives stacking and warm-pressing, but oxidizes and escapes during baking, creating hollow electrode sites.

The electrode cavity, however, needs some support; therefore pillars are inserted by blending tiny ceramic particles into the carbon-like electrode ink. When the ink burns away, the particles remain, fusing the floor and ceiling together. This first phase of the process yields a strong, monolithic ceramic block ready for termination and electrode injection.

In both processes, terminations are made using a silver alloy. It is thin and dense in the conventional process and thick and porous in the A.C.E. process as shown in *figures 3 and 4* respectively.

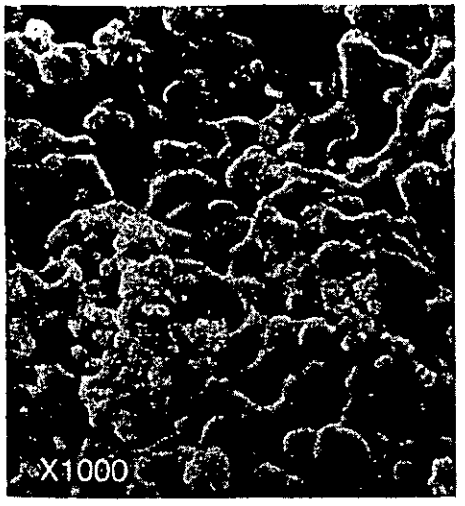


Figure 3

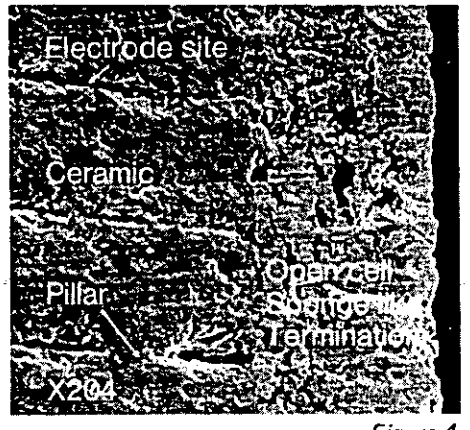


Figure 4

The A.C.E. termination is porous because the electrode material must pass through the termination to fill the hollow sites during the injection process. The injected electrode material must have certain defined characteristics. It must not wet the dielectric in order to avoid coating the body. The electrode material must also be solderable to the leads because the injected electrode material coats the termination material. Additionally, the electrode must have a high melting point so that it does not re-melt during subsequent processing. Finally, the material must be cost effective. For the injected electrodes, Corning chose a lead alloy.

The lead-injection process is simple and direct. First the terminated chips are preheated to prevent thermal shock. Next they are placed in a vacuum to pull the air from the cavities and then submerged in a bath of molten lead alloy. Finally, hydrostatic pressure is applied to force the lead through the termination into the electrode cavities, as shown in *figures 5 and 6*.

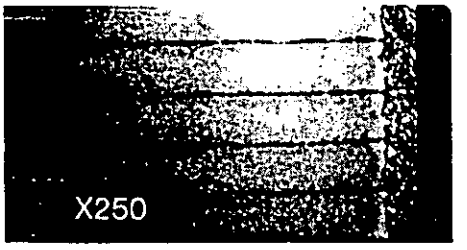


Figure 5

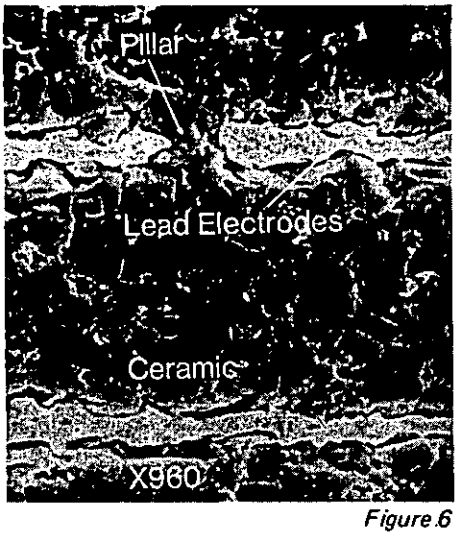


Figure 6

The molten lead alloy has now filled the metal sponge and the electrode sites and made a complete metal-to-ceramic seal, with no chance of delamination. In addition, porosity is dramatically reduced.

Porosity is caused by bubbles of gas trapped in the ceramic as it hardens in firing. In the conventional M.L.C. capacitor, the bubbles can escape only via a long thin path to the edges. However, in the A.C.E. units, the bubbles travel only to the surface of the hollow sites, usually a distance of less than 0.001 inches. As a result the majority of the bubbles get out.

Using the conventional process the leads are attached and the chip encapsulated. With the Corning Spinseal® encapsulation process the capacitor easily passes a 56 day Damp heat test.

The A.C.E. process also produces a capacitor with improved high-frequency characteristics. The lead-filled sponge termination and the electrode are one and the same, the equivalent series resistance (E.S.R.) of the Corning units is very low. For example, a 0.1uF A.C.E. multilayer capacitor with axial leads has an E.S.R. of only 0.1 Ω at 7.5 MHz. E.S.R. is higher in conventional M.L.C.s because it is difficult to make good electrical contact between the silver-paste termination material and the thin edges of all of the printed, fired palladium electrodes.

Another important feature of an A.C.E. capacitor is the stability in its design. The electrode material and dielectric material are free of continual technical change. In conventional M.L.C. capacitors, increasing material costs have forced changes in the electrode system away from the traditional gold-platinum alloys, to lower cost palladium alloys.

The palladium alloys, in turn, are now yielding to less expensive silver alloys, which in the future, may yield to inexpensive nickel alloys. Each time the electrode system changes, the dielectric system must change as well. It is hard to establish a customer's confidence in the reliability of a capacitor, when the capacitor is undergoing continual technical change. With an A.C.E. capacitor, the stable cost of the injected lead electrode material is not forcing further changes in either the electrode or the dielectric. The A.C.E. capacitor has stability in its design.

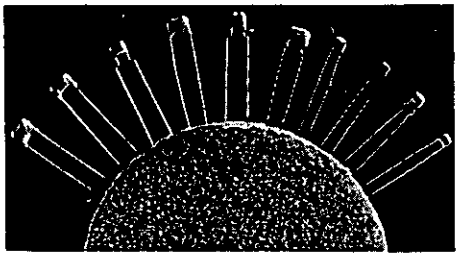


Figure 7

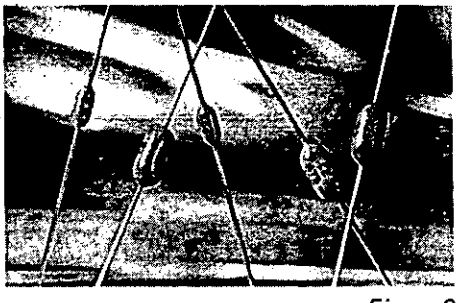


Figure 8

This process is used to manufacture the CAC range, of axial capacitors (approved to BS9075 F050/51/52) a comprehensive range of radial capacitors, Type CRC (approved to CECC 30601-013 and CECC 30701-026/27) and the CC range, of chip capacitors. Shown in figures 8, 7 and 9 respectively.

The performance of A.C.E. capacitors has been proven by extensive testing and field performance, internal tests, BS/CECC testing, competitive evaluations and customer qualifications. Over one billion A.C.E. capacitors have been sold since their introduction in 1977.

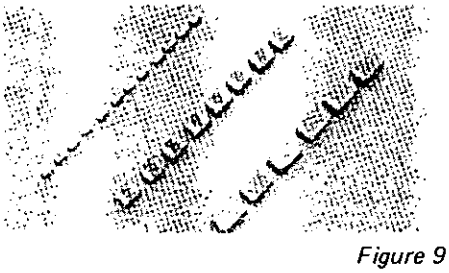


Figure 9

General Features of Multilayer Ceramic Capacitors

Manufacturing Method — The Corning 'A.C.E.' Process

Corning Electronics has been producing high quality ceramic capacitors utilizing the A.C.E. (Advanced Corning Electrode) process since 1977. The principal difference between the A.C.E. process and the conventional process of manufacturing MLC capacitors is that in the A.C.E. process the metal electrodes are not co-fired with the ceramic dielectric. Electrode sites are built by screening fugitive electrode material during capacitor formation. Early in the firing process this fugitive electrode material is burned out, leaving hollow electrode sites and freeing the ceramic to be optimally fired by itself. Subsequently, the hollow electrode sites are injected with electrode material. All the problems associated with co-firing are avoided.

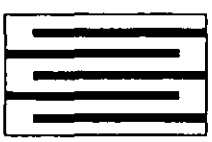


Fig. 1. STACKING OF CERAMIC WAFERS

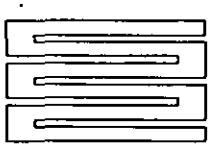


Fig. 2. SINTERING OF CERAMIC AT 1400°C AND EVAPORATION OF CARBON ELECTRODES

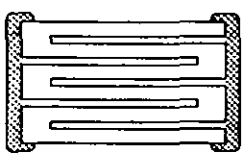


Fig. 3. SILVERING OF THE ENDS

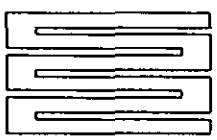


Fig. 4. INJECTION OF LEAD BASED ELECTRODES THROUGH THE SILVER ENDS

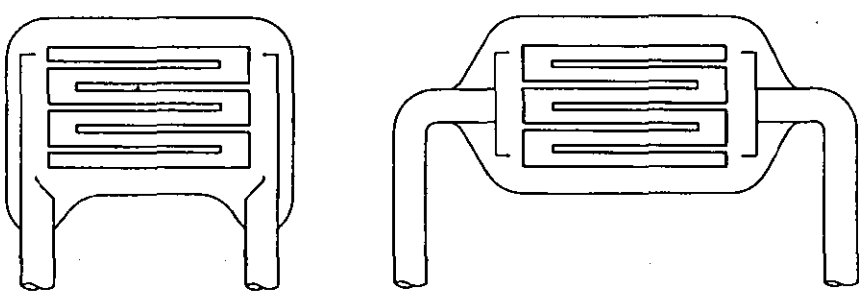


Fig. 5. SOLDERING OF THE LEADS AND ENCAPSULATION

Performance Benefits of A.C.E.

- Delamination free electrodes
- Excellent high frequency characteristics due to low ESR (Equivalent Series Resistance). For example, an X7R.1uf has an ESR of .066 Ohms at 6.5 Mhz and a Z5U.18uf has an ESR of .038 Ohms at 6 Mhz.
- Very reliable for low voltage applications
- Optimised dielectric properties:
  - Low porosity
  - Fine grain structure
  - High voltage strength
- Excellent field performance — over 4 billion A.C.E. capacitors in the field since 1977

Other important Features of A.C.E.

- Non-noble injected electrodes allow freedom from precious metals' cost fluctuations.
- The design of an A.C.E. capacitor emphasizes reliability without compromising dielectric thickness.

The A.C.E. process is used in the manufacturing of Corning Electronics' monolithic ceramic capacitors. Corning pioneered and introduced in 1972 SPINSEAL™ axial ceramic capacitors coated with epoxy for commercial applications.

During 1980 the Electrosil Division began manufacturing the CAC range of capacitors using this proven technology, and our products are qualified to BS/CECC specifications. They are available taped and packaged in either Ammo-packs or on Reels. See page 16 for details.

Product Safety

Operation outside the stated ratings may result in premature failure or a safety hazard.

APPENDIX 3

Temperature Cycling of Surface Mounted Thick Film 'Zero-ohm' Jumpers

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Electronic Component Technology Group, Department of Electronic and Electrical Engineering, University of Technology, Loughborough, Leicestershire, England

ABSTRACT—Thermal cycling tests for surface mounted components are usually taken around a mean temperature of approximately 35°C (e.g., −55°C to +125°C; −40°C to +110°C). To test the effect of different maximum temperatures thermal cycling tests using a lower temperature of −55°C have been conducted with alumina/thick film 'zero-ohm' jumper chips with nickel barriers. These are connected in series chains and wave soldered on to FR-4 test coupons (128 chips/coupon).

The test regimes used were −55°C to +5°C; +65°C; +95°C, +110°C and +125°C. Resistance changes before and after cycling were observed at room temperature. After 100 cycles changes of approximately +200 mΩ were observed against a total resistance of 5·5 Ω. However, more detailed examination showed that a top temperature of +95°C gives optimum results with a total change over 100 cycles of +4·9%.

INTRODUCTION

The introduction of any new manufacturing technology brings with it the requirement of an analysis of any reliability hazards associated with it. It is agreed[1,2,3] that in the case of surface-mounting techniques the primary reliability hazard is thermally induced fatigue failure of the solder fillets. This fatigue is caused by cyclic thermal stresses which are generated by variations both in ambient temperature and power dissipation within components. Such behaviour will ultimately constitute a 'wear-out' phenomenon in the majority of practical situations. The requirement is, therefore, to develop testing techniques to determine whether a particular surface mounted assembly will have a satisfactory life under the expected service conditions.

Previous studies have defined solder joint failure either by the visually observed presence of cracks or total electrical failure of the joint. Both these criteria however have disadvantages. Visual inspection is time consuming and the extent of cracking may only be fully determined by the destructive sectioning of the solder joint. Furthermore, the electrical performance of a component may be degraded by poor contacts before total failure of the connections to it.

The ready availability of 'zero-ohm' thick film jumper chips allows the possibility of making detailed resistance measurements without the relatively large component resistance of resistor or the impedance values of capacitor chips swamping the much smaller resistance changes expected in the joint resistances. A program has therefore been established to apply temperature cycling tests to these devices.

EXPERIMENTAL DESIGN

Components

The components used are 1206 size jumper chips. They are constructed using a thick film conductor on an alumina substrate and have nickel barrier plated terminations to prevent solder leaching.

Measurement Techniques

In order to easily study small changes of resistance, chains of components are connected in series and monitored using four-terminal resistance measurements. The experiment is also designed to allow individual four-terminal measurements of each component to be made in order to determine whether one particular component has been responsible for any observed change in the total chain resistance.

Test Coupon

The test coupons (Figure 1) have been designed to allow attachment of 120 jumper chips in series chains. They are manufactured using 1·6 mm FR-4. They are assembled using an epoxy adhesive (Amicon D 124F) and then double-wave soldered using 60Sn/40Pb solder.

Tests

Thermal cycling tests have usually been conducted symmetrically about a mean temperature of approximately 35°C (e.g., −55 to +125°C; −40 to +110°C), but there was reason to doubt that the severity of these tests was only related to the temperature range.

It was therefore decided to test the effect of maximum cycle temperature by using tests with a fixed lower temperature of −55°C, but a number of different maximum temperatures. The test cycles used were −55°C to 5°C, +65°C, +95°C, +110°C and +125°C all at 12 cycles per day and a rate of change of temperature of 3·5°C per minute (Figure 2). As a result the dwell times at both the maximum and minimum temperatures will be different for the different cycles.

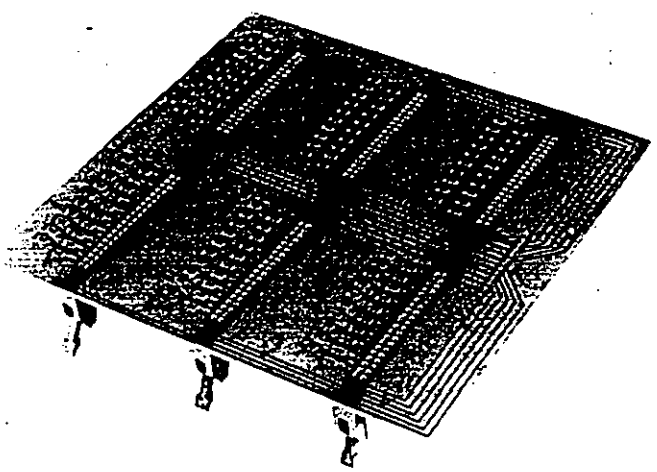

Fig. 1 *Temperature cycle test coupon.*

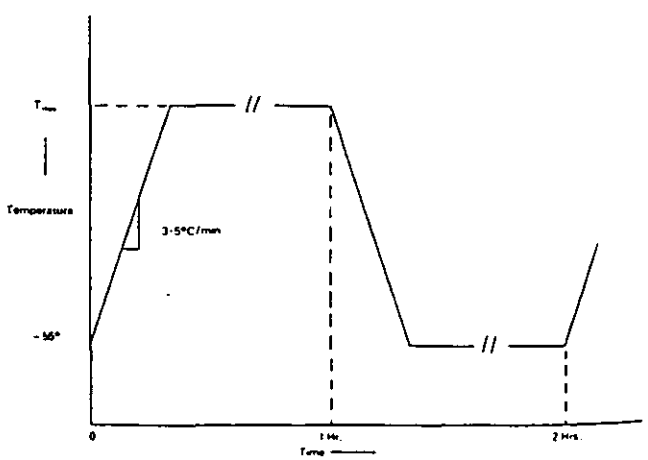

Fig. 2 *Temperature cycle test profile.*

The environmental chamber used was a LEC CL10HB, controlled by a PET microcomputer to give maximum flexibility in cycle profile.

In addition to these temperature cycling tests, two separate groups of jumper chips have been subjected to high temperature exposure tests. One group was tested in accordance with MIL-R-55342 paragraph 4.7.6. (100 hours at +125°C) and the second group was subjected to a similar test, but at a temperature of +95°C. These tests were undertaken in order to

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assess whether any drift in component resistances would affect the results of the temperature cycling tests.

RESULTS

The results of temperature cycling over the five ranges are shown in Figure 3. All measurements were taken at room temperature (20°C). Figure 3 demonstrates that the largest increase in resistance occurs in cycling from −55°C to +95°C with smaller increases occurring due to cycling to higher and lower peak temperatures. Detailed examination of individual jumper resistances reveals that, rather than one or two components accounting for the resistance rise, there is a general trend upwards in resistances. This is illustrated in the histogram of Figure 4 where the total resistance of each jumper is shown before and after cycling between −55°C and +95°C. Similar results were obtained for cycling over the other temperature ranges.

In the high temperature exposure at +125°C an average change in jumper resistances of +0·3 mΩ, amounting to an overall chain resistance change of ≅+0·5%, was observed.

In the +95°C high temperature exposure test there were even smaller resistance changes, i.e., an average change in individual jumper resistances of +0·1mΩ which amounts to an ≅+0·2% change in overall chain resistance. These resistance changes are well below those observed in the temperature cycling tests and it can therefore be concluded that temperature cycling changes are not caused by drifting of the component resistances.

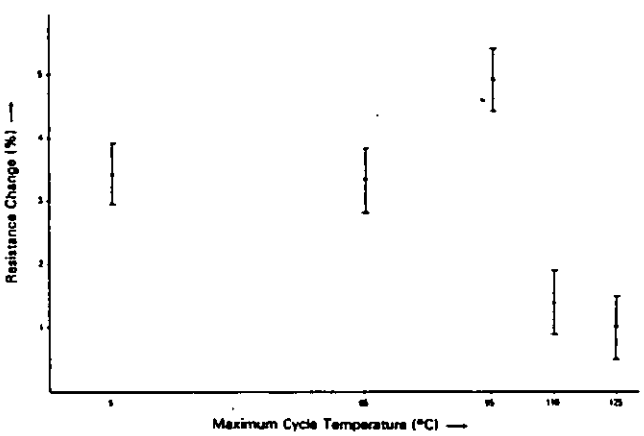

Fig. 3 *Resistance changes versus maximum cycle temperature.*

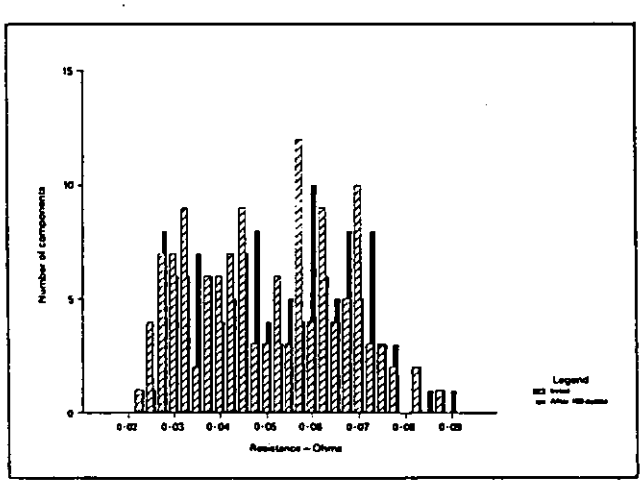

Fig. 4 *Changes in jumper resistances due to temperature cycling.*

DISCUSSION

Thermal stresses are caused by differential thermal expansion between component and substrate. This leads to shear strains in the solder fillet. Figure 5 shows an idealised component attachment. The thermal strain $\Delta\varepsilon$ for such an attachment is given by:

$$\Delta\varepsilon = L(\alpha_c \Delta T_c - \alpha_s \Delta T_s)/h \quad (1)$$

where L is the component length
h is the solder joint thickness
α_c and α_s are the thermal expansion coefficients of component and substrate
ΔT_c and ΔT_s are the changes in temperature of component and substrate.

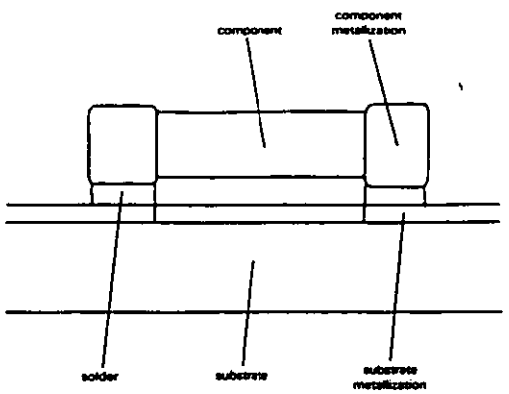

Fig. 5 *Idealised component attachment.*

This strain may be absorbed in three ways: elastic deformation of the whole structure (ε_e), instantaneous plastic deformation of the solder fillet (ε_i) and creep or time dependent plastic deformation of the solder fillet (ε_c).

At room temperature and above the solder creep is rapid and the elastic strain quickly falls to zero. Hence the total plastic strain (ε_p) may be assumed to be:

$$\varepsilon_p = \varepsilon_i + \varepsilon_c = \varepsilon \quad (2)$$

The fatigue life of a material may be calculated using the Coffin-Manson relation[4]:

$$N_f = \left(\frac{\varepsilon_f}{2\varepsilon_p}\right)^2 \quad (3)$$

where N_f is the number of cycles to failure and ε_f is the fracture ductility of the material. The fracture ductility of solder, however, increases substantially with temperature (Figure 6)[5] so that a given level of strain will cause less damage when absorbed at a higher temperature.

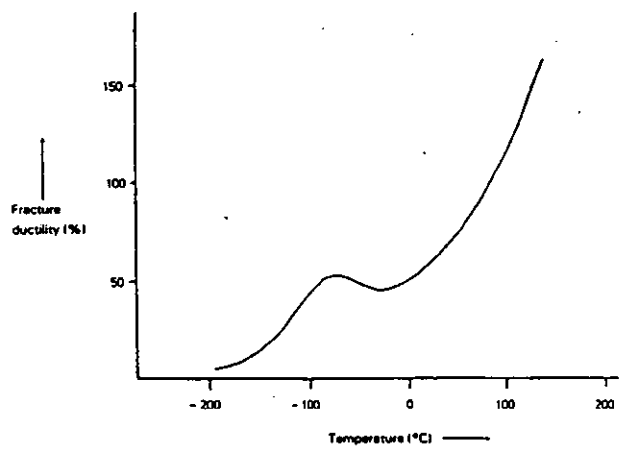

Fig. 6 *Variation of fracture ductility with temperature for 60Sn/40Pb solder.*[5]

From (3) the damage per cycle (D) can be obtained where a change level of 1 represents failure:

$$D = \left(\frac{2\varepsilon_p}{\varepsilon_f}\right)^2 \quad (4)$$

Assuming a linear damage summation, i.e., that the damage per cycle is the sum of the damage caused by each finite change in strain $\Delta\varepsilon$, the damage per cycle may be expressed as:

$$D = \left(\sum_{T_{min}}^{T_{max}} \frac{\Delta\varepsilon}{\varepsilon_f(T)} + \sum_{T_{max}}^{T_{min}} \frac{\Delta\varepsilon}{\varepsilon_f(T)}\right)^2 \quad (5)$$

For a temperature cycling test $\Delta T_c = \Delta T_s = \Delta T$ (Equation 1), so from equation one is obtained:

$$\Delta\varepsilon = \Delta T(\alpha_c - \alpha_s)L/h = k\Delta T \quad (6)$$

The fracture ductility (ε_f) for a given temperature may be approximated by the function:

$$\varepsilon_f = ae^{bT} \quad (7)$$

Using Equations (5), (6) and (7) one can calculate the damage expected to be caused by the idealised temperature cycle shown in Figure 7. It is assumed that for the step increase in temperature all the strain is absorbed at the new temperature and that the subsequent reduction in temperature is slow enough for the strain to be absorbed at the temperature at which it was generated. In a practical situation some of the strain will be absorbed at lower temperatures and thus the damage will be higher.

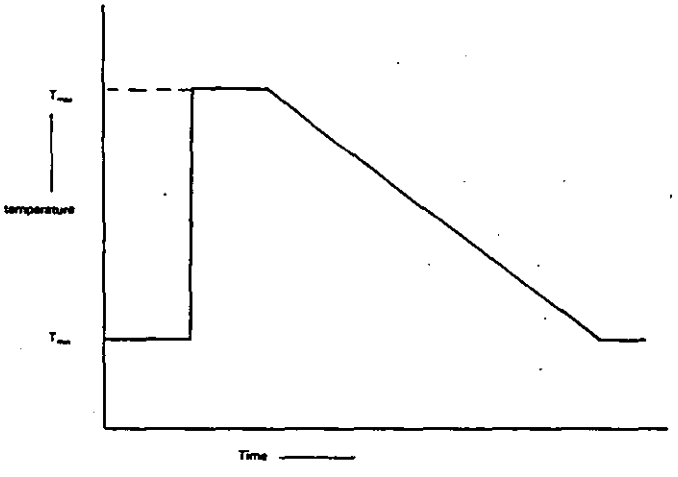

Fig. 7 *Idealised temperature cycle.*

The damage caused by the step change in temperature from T_{min} to T_{max} may therefore be expressed by:

$$D = \left[\frac{k(T_{max} - T_{min})}{ae^{bT_{max}}}\right]^2 \quad (8)$$

and the damage caused by the slow change in temperature from T_{max} to T_{min} is:

$$D = \left[\int_{T_{max}}^{T_{min}} \frac{k}{ae^{bT}}\,dT\right]^2 = \int_{T_{max}}^{T_{min}} \left[\frac{k}{ab}e^{-bT}\right] \quad (9)$$

From Equations (8) and (9) the total damage for the cycle is:

$$D = k^2\left[\frac{T_{max} - T_{min}}{ae^{bT_{max}}} + \frac{e^{-bT_{min}} - e^{-bT_{max}}}{ab}\right] \quad (10)$$

This equation has been plotted against maximum cycle temperature in Figure 8 using a minimum cycle temperature of $-55°C$. The graph does show that the maximum damage is expected for cycling from $-55°C$ to $+95°C$, with slightly less damage for higher maximum temperatures.

This effect is however small and is insufficient to explain the experimental results obtained. Therefore there must be other factors involved. These may be:

(a) The large drop in the modulus of elasticity of the resin matrix of the FR-4 PCB at its glass transition temperature of 110°C. This may result in less of the strain being plastically absorbed at higher temperatures.

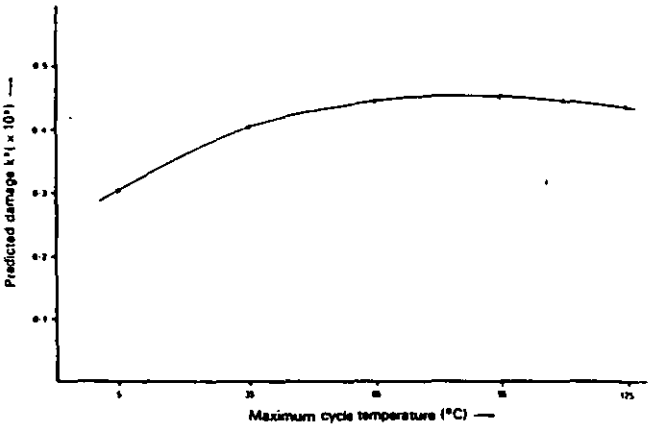

Fig. 8 *Predicted damage versus maximum cycle temperature.*

(b) Other changes in the solder such as work hardening/annealing processes altering the solder's mechanical properties and consequently the way in which the strain is absorbed. Intermetallic growth or changes in the bulk resistivity of the solder fillet may also occur.

CONCLUSIONS

1 Both theoretically and practically it has been shown that the effect of temperature cycling on surface mounted devices depends on the cycling temperatures. For a minimum temperature of $-55°C$, the most effective top temperature with regard to causing resistance increase in the solder fillets is 95°C.

2 Temperature cycling tests from $-55°$ to temperatures between $+5°C$ and $+125°C$ result in a quite complex interaction of the changes in mechanical properties of the materials involved.

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