Advanced electrical characterisation of thin-film solar cells

Advanced Electrical Characterisation of Thin Film Solar Cells

by

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Contents

Abstract

The work presented in this thesis focuses on both standard and advanced characterisation techniques applied to solution-processed CIGS and vacuum-processed CdTe thin film solar cells. Characterisation techniques such as capacitance spectroscopy, tempeture dependent *J-V* measurements, PDL Hall effect and along with other fundamental measurement techniques are used to extract the key parameters and material properties of these solar cells. Capacitance spectroscopy offers valuable insight to material properties such as defect density, energy level of defects and carrier concentration, which is especially important to understand in the operation of thin film solar cells and their limiting processes.

Antimony (Sb) was introduced into the solution-processing CIGS absorbers which led to an increase in *EQE*, hence an increase in $\boldsymbol{J_{sc}}$. A bilayer structure of large-grain top layer and a fine-grain bottom layer was observed by *SEM*. The devices with Sb showed a low net carrier concentration and defect density compared to the devices with no Sb doping, indicating that adding Sb might be passivating the defect in the bulk, rather than doping the absorber. A shift in the long wavelength decay of *EQE* spectra for the device with Sb is observed, indicating a decrease in bandgap and only the change in In/Ga ratio able to explain this behaviour. From the $\boldsymbol{V_{oc}(T)}$ analysis, the main recombination mechanism for the device with Sb is found to be in the bulk of the absorber, whereas the device without Sb is dominated with the interface recombination. Adding Sb into the absorber layer has reduced the rollover seen at low temperatures in the *J-V* characteristics, and has removed the barrier at the CdS/CIGS interface. This may be due to the incorporation of Sb into the CIGS absorber, resulting an improved band alignment of CdS/CIGS. The admittance spectroscopy measurements for the device without Sb revealed an admittance step with an activation energy of $\boldsymbol{E_A}$ = 330 meV. This step is considered as a deep level

defect, which has often been referred to as the N2 defect. The N2 defect has been removed with Sb doping and left with a shallow level defect, N1 ($\boldsymbol{E_A}$ = 42 meV). After 1 hour of light soaking under 100 mWcm^{-2} illumination at room temperature, the devices showed a significant increase in the cell performance especially in the junction capacitance and net carrier concentration.

A detailed study of the defects for N1 and N2 steps were performed using capacitance spectroscopy for devices with and without tellurium (Te) at the back-contact, and devices with and without CdSeTe (CST) layer of CdTe devices. The admittance measurements revealed different activation energies, $\boldsymbol{E_A}$ between 20 meV and 279 meV at different temperatures for each device. Adding Te to the CST/CdTe devices removed the N1 step. The N1 step corresponds to a shallow defect with low a $\boldsymbol{E_A}$, suggesting that the defect might be located at the absorber/back-contact, since Te is added at the back of the device. For the CdTe devices without CST layer, Te has removed the N2 defect and left only the N1 defects. The CST&CdTe with Te devices showed high efficiencies around ~14-15% with high $\boldsymbol{FF}$. The `CST with Te` device has shown an `*S*` shaped *J-V* curve, which can relate to a conduction band offset (CBO) or a presence of a significant current barrier. Non-diode behaviour *J-V* characteristics have been observed with the `CST/CdTe without Te` and this is due to having a low $\boldsymbol{FF}$, a large $\boldsymbol{R_s}$ and a low $\boldsymbol{R_{sh}}$. The dominant recombination mechanism by the activation energy ($\boldsymbol{E_a}$) is extracted from the intercept of $\boldsymbol{V_{oc}(T)}$ at $\boldsymbol{T = 0\ K}$ and this found to be at or close to the interface for all the devices. Adding Te to the CdTe devices has slightly reduced the interface recombination, leading to a smaller barrier height and improved *J-V* characteristics. Both *C-V* and *DLCP* measurements showed typical `*U*` shaped depth profiles with similar net carrier CST/CdTe . The difference in depth profiles is due to high level of deep level and shallow defects. Thus, measurements are affected by the N1 and N2 steps.

The metastable behaviour found in CdTe devices with MZO buffer layers resulted in variations from the *J-V* characteristics depending on prior exposure history of light and environmental stresses, such as temperature and climate. Different preconditioning procedures have been studied that are used to recover the performance of the devices. *J-V* characteristics before preconditioning have shown an `*S*` shaped behaviour, with significant current loss in forward bias which is

removed after preconditioning. Also, the depth profiles before preconditioning showed an unusual double minima, and the second minima towards the back of the device became less pronounced after preconditioning. The *"Atmospheric"* preconditioning procedure resulted in a significant recovery of the device *Vacuum"* preconditioning. Temperature dependent *J-V* and capacitance measurements before and after preconditioning revealed the presence of recombination centres and defect levels at the MZO/absorber interface. Light and voltage bias have improved the degree of these metastable behaviours by reducing the formation of a blocking layer at the interface. Despite all the preconditioning attempts, the recovery of PV parameters remained only for 3 days while the devices were maintained under vacuum in the dark. Since the temperature dependent capacitance and *J-V* measurements showed defects and recombination centres at the MZO/absorber interface, the Hall effect measurements have been studied in an attempt to extract carrier concentration, mobility and the conductivity of the MZO films. Conductivity measurements on MZO films showed no significant changes before and after preconditioning. However, $CdCl_2$ treated MZO films showed slight improvement in the linearity of the *I-V* response. Although the response was improved, no linear sheet resistance or proper Hall signal were detected in order to extract reliable and accurate carrier concentration, or mobility of the MZO films. Alternatively, Ga as a dopant is used in MZO layer (GMZO), which should enhance the film conductivity and the carrier concentration. The annealed GMZO films showed an improved *I-V* response and a large improvement in conductivity after light soaking. However, a gradual decrease in Hall signal over time was observed and no reliable results could be extracted from the Hall effect measurements.

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List of Publications

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Chapter 1

Introduction

1.1 Motivation

Converting abundant solar energy into electricity at low-cost is a very attractive option for sustainable production of electrical energy since the escalating concerns of fossil fuels over the serious negative impact on the environment. Photovoltaic (PV) technologies based on Silicon (Si) solar cells have been the focus of research since the 1950s and are commercially abundant today. Nevertheless, due to the processing limitations of Si wafer-based solar cells, inflexibility of wafers and high production costs, many new approaches in device processing and alternative solar cell materials have achieved increased attention over the years. This has opened new prospects in development of thin film solar cells (TFSCs) and research to overcome some of these limitations.

TFSCs are some of the most promising candidates for low-cost and efficient large-scale solar energy conversion which offer a wide variety of choices in device structure, fabrication, and applications. A variety of rigid and flexible substrates can be used, as well as a range of different deposition and processing techniques when designing and fabricating layers (absorber, buffer, contacts, TCOs, etc.) to improve the device performance. The main thin film single-junction PV technologies such as amorphous silicon (a-Si), cadmium telluride (CdTe), $Cu(In,Ga)(S,Se)_2$ (CIGS), $Cu_2ZnSn(Se,S)_4$ (CZTS) and gallium arsenide (GaAs) have much in common, in spite of having different absorber properties and device structures. However only a-Si, CdTe and CIGS technologies are commercialised on a large scale so far. Significant progress has been made over the years by improving device structures and fabrication techniques, despite a full lack of understanding the recombination mechanisms and electrical defects which determine the behaviour of the device.

Polycrystalline CIGS TFSCs exceed power conversion efficiencies ($\boldsymbol{PCEs}$) ~23% vacuum-grown in laboratory-scale devices [1] and 18.7% in solution-grown CIGS solar cells [2]. These films with direct bandgaps and high absorption coefficients are established absorbing materials for rigid and flexible TFSCs. In addition, there are a number of methods to prepare CIGS absorbers [3][4][5][6][7][8] (which will be covered in Chapter 2). However, there are still several uncertainties about the relation between the compositional, structural, and electronic properties of the absorber layers, and various metastabilities within the devices which limits the device performance.

Currently, CdTe solar cells have reached $\boldsymbol{PCE}$ up to ~22% [9]. Since the photocurrent collection for CdTe absorbers has approached the theoretical limit [10], modifications with the device structure are needed to achieve an increase in open-circuit voltage ($\boldsymbol{V_{oc}}$). The way forward with next generation CdTe-based solar cells is utilising graded absorber structures and tuneable buffer layers to enhance the device efficiency further. However, there are numerous reports in the literature of

and transient metastable behaviours with prior exposure history (such as temperature, climate and irradiance) of the devices [11][12][13][14][15].

Continued research into the behaviour of different solar cell materials, better understanding of techniques and data interpretation is required before some of these technologies, to be out in the field or competing in the energy, and PV market. This thesis utilises several standard and advanced characterisation techniques (described in chapter 3) as methods for understanding limiting processes in different TFSC materials and devices. These techniques offer valuable insight to material properties such as defect density, energy level of defects and carrier concentration, which is especially important to understand in the operation of TFSCs using new materials and processing techniques. In addition, these techniques can be especially useful when exploring metastable behaviour due to prior exposure history of light and environmental stresses such as temperature and climate. Used in conjunction with standard electrical characterisation methods, it is possible to form a comprehensive picture of the device in an effort to improve the overall performance and stability. Chapter 4 – 6 uses both standard and advanced characterisation techniques applied to solution-processed CIGS and vacuum-processed CdTe TFSCs and investigates

among other complexities such as material degradation due to the presence of atmospheric humidity, metastability effects with substantial transients, *p-n* junctions with current barriers, and preconditioning procedures attempting to recover PV parameters.

The complexity of the device structure, along with the presence of many interfaces and defects can greatly impact the electrical measurements, and therefore the interpretation of the results. It is important to understand the distribution of defects in the absorber layer or at the interface (between the *p-n* junction) which has a crucial role in the operation of solar cells. Capacitance spectroscopy by means of capacitance-voltage (*C-V*), drive-level capacitance profiling (*DLCP*) and admittance spectroscopy (*AS*) techniques are widely used for the investigation of defects, based on monitoring the junction capacitance as a function of voltage, frequency, and temperature. Analysis of the *C-V* behaviour of the depletion region is a non-destructive method in determination of the doping profile in semiconductors. *DLCP* gives a more accurate determination of carrier concentration. Likewise, *C-V* profiling can lead to incorrect determination due to the presence of deep defects or interface defects. *AS* is useful to quantify defect activation energies and estimate the density and energy level of the states and the position of the Fermi level in the bulk.

In addition, Hall effect is a well-established and understood technique based on the simplicity of the van der Pauw geometry [16]. It is used in many practical applications revealing the fundamental information of thin films properties, such as carrier concentration, majority charge carrier type (*p* or *n*), mobility and resistivity. These properties are important in understanding the working principle of each layer of a solar cell and provide feedback to the fabrication process. The traditional Hall effect system uses static field (DC) measurements which might be problematic to measure materials with low mobility, or very low or high resistance due to very low signal to noise (S/N) ratio. Materials with such characteristics are usually semiconductors, metals, and thermoelectric materials. The parallel dipole line (PDL) system generates an alternating (AC) field along with a numerical Lock-in detection which can measure materials with a mobility of below 0.1 cm^2/Vs [17]. Such a technique will provide valuable insight in understanding the properties of thin film materials and exploring different options of materials in device applications.

1.2 Thesis Organisation

The rest of the thesis discusses the basic solar cell principles based on *p-n* junction semiconductor devices which are commonly used for TFSCs. These materials such as, CIGS and CdTe with different absorber layer growth processes are explained in chapter 2. Alongside with processes and deposition techniques, most common device configurations with working principles and recombination mechanisms are explained. Following an explanation of different solar cells and principles in chapter 2, experimental and analytical procedures using different electrical characterisation techniques such as current density-voltage (*J-V*) and capacitance spectroscopy are described in chapter 3. Additionally, other techniques such as external quantum efficiency (*EQE*), scanning electron microscopy (*SEM*), electroluminescence (*EL*) imaging and Hall effect measurements are also explained. Chapter 4 includes the experimental results for solution-processed antimony doped CIGS devices which are fabricated in CREST, at Loughborough University. Moreover, chapter 5 and 6 include MZO/CdSeTe/CdTe devices which are provided by Colorado State University (CSU). Finally, overall conclusions are given in chapter 7.

Chapter 2

Solar Cell Basics and Devices

2.1 Introduction

This chapter covers the physics of solar cells and semiconductor materials that are used in manufacturing solar cells. It gives an overall explanation of how the energy levels between semiconductors affect the collection of charges to generate electron-hole pairs and the recombination processes that limit the current generation. The main focus of this chapter will be on copper indium gallium di-selenide (CIGS) and cadmium telluride (CdTe) thin film solar cells (TFSCs). These material-based devices have reached laboratory efficiencies above 22%, and there are still improvements that can be made to push the efficiency further. Different configurations with multiple layers can be deposited on various substrates to build a working device. Up to date, high efficiency was obtained from a substrate cell configuration for CIGS devices and superstrate for CdTe devices. In addition, the growth processes and deposition techniques of each layer for both conventional CIGS and CdTe devices, and the most common problems and metastabilities associated with these materials will be discussed.

2.2 The Physics of Solar Cells

2.2.1 Semiconductor Materials

Semiconductors are materials which have conductivity between conductors and insulators under certain conditions, either due to the addition of an impurity or because of temperature effects. The amount of impurity added to an intrinsic (pure or undoped) semiconductor varies its conductivity, and doped semiconductors are referred as extrinsic [18].

Silicon has been used in the electronic industry for many years [19]. The photovoltaic (PV) market is currently dominated by silicon based solar cells. However, the main issues of silicon are associated with its purification and crystallisation that require energy intensive processes [20]. Other materials that are often used to manufacture solar cells are gallium arsenide (GaAs), amorphous silicon (a-Si), copper indium gallium di-selenide (CIGS) and cadmium telluride (CdTe). For an efficient absorption, absorber material should be a direct bandgap semiconductor, with a bandgap between 1.3 eV and 1.4 eV [18] and a high optical absorption [21]. Silicon is in Group IV of periodic table [22] and it is an indirect semiconductor with a bandgap of 1.1 eV, which makes it a non-ideal solar cell material [23].

2.2.2 Band and Energy Gaps

Semiconductors have a narrow energy gap which is in between the valence band ($\boldsymbol{E_V}$) and the conduction band ($\boldsymbol{E_C}$). This energy gap is also called a bandgap ($\boldsymbol{E_g}$) and classified into two types on the band diagram depending on its energy, a direct and an indirect bandgap. The bandgap represents the minimum energy difference between the top of the $\boldsymbol{E_V}$ and the bottom of the $\boldsymbol{E_C}$, and is a fundamental material property for PV applications which determines the energy of photons that can be absorbed. Only photons with an energy $\boldsymbol{E > E_g}$ are absorbed from the incident sunlight. A direct bandgap semiconductor is one which the maximum energy level of the $\boldsymbol{E_V}$ aligns with the minimum energy level of the $\boldsymbol{E_C}$ with respect to momentum. If the two levels are misaligned with respect to momentum, then it is called an indirect bandgap [24].

Figure 2.1 shows the alignment of conduction band and valance band for the direct and indirect bandgap (where $\boldsymbol{E}$ is the electron energy and $\boldsymbol{k}$ is the lattice spacing).

The Fermi level (E_F) describes the top of the collection of electron energy levels at 0 K, and lies ın the middle between E_V and E_C [25]. In direct bandgap semiconductors, an electron at the minimum of E_C can excite an unoccupied state in the E_V through the emission of a photon with energy equalling $E = h\nu$ (where h is the Planck`s constant and ν is the radiation frequency) [26]. In indirect bandgap semiconductors to excite an electron, the transition requires a change of momentum (phonon) in combination with a photon. Thus, materials with a direct bandgap are more likely to absorb a photon than an indirect bandgap semiconductors since light travels shorter distances through the material before being completely absorbed. These differences between direct and indirect band structures are particularly important on deciding which semiconductors to be used for solar cell applications [21].

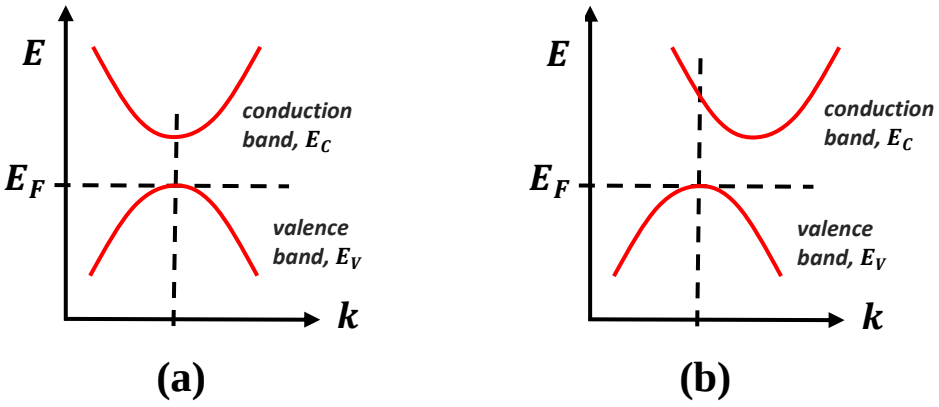

Figure 2.1: (a) Direct and (b) indirect absorption process.

2.2.3 P-N Junction

A single-junction solar cell consists of *n*-type (negatively charged) and *p*-type (positively charged) semiconductors which forms the *p*-*n* junction. A *p*-*n* junction is created by adding an acceptor or a donor to a semiconductor. The *p*-type region contains an excess of holes, while *n*-type region contains an excess of electrons and combination of these regions which are doped differently creates an interface between the materials. Electron and hole diffusion is due to higher concentration in different regions that creates an electric field at the junction, causing a separation to the photogenerated electrons and holes to move opposite sides [27]. The thin layer between *n*-type and *p*-type regions is known as the depletion region and becomes non-conductive intrinsic semiconductor material. This separation of charges at the *p*-*n* junction creates a potential barrier. The potential barrier can be achieved by

controlling the doping level of both *p* and *n* type materials which allows producing higher voltages. Figure 2.2 shows the formation of a *p*-*n* junction; the depletion, *n*-type and *p*-type regions where $\boldsymbol{W}$ stands for depletion region width, $\boldsymbol{N_D}$ and $\boldsymbol{N_A}$ are the doping levels of donor and acceptor materials respectively.

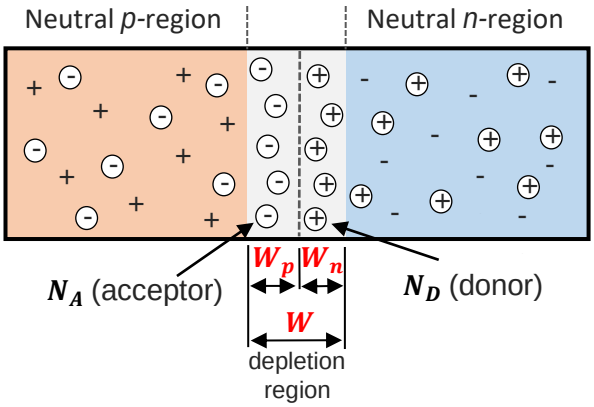

Figure 2.2: *p*-*n* junction formation.

The *p*-*n* junctions are the most common model of a solar cell which consist of semiconductor electronic devices such as diodes. The current through a diode only flows in one direction and the anode of the diode corresponds to *n*-type, while the cathode is *p*-type semiconductor. If a diode is forward biased, current will increase slightly as voltage increases from 0 V. The majority carriers are pulled towards the junction by the applied external potential, allowing current flow by lowering the barrier for the electrons and holes. Thus, the depletion region narrows down to smaller width. If the diode is reverse biased, only the leakage current of the intrinsic semiconductor flows and attracts majority carriers away from the junction. This causes the depletion region width to increase since the majority carriers are attracted to the external potential, making it harder for carriers to cross the junction [25].

Figure 2.3 shows the *I*-*V* characteristics of a *p*-*n* junction diode. The x-axis in the below figure represents the amount of voltage applied across the junction and the y-axis the amount of current. If the voltage applied on the diode is increased continuously, the *p*-*n* junction diode reaches to a state where junction breakdown occurs, and reverse current increases rapidly. The leakage current occurs when a reverse bias is applied and depends on the temperature. If temperature increases the generation of minority charge carriers increases. Hence, the reverse current increases with the increase in voltage. For a constant temperature reverse current is

almost constant though applied reverse voltage is increased up to certain limit. The leakage current becomes very serious when the diode`s reverse bias reaches breakdown, when causes a large amount of current to flow [28] [29].

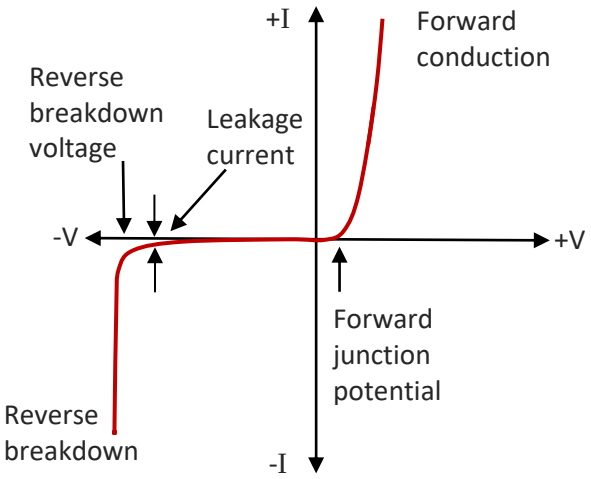

Figure 2.3: *I-V* characteristics of a diode.

2.2.4 Generation and Recombination

Carrier generation and recombination occur when an electron makes transition from the $\boldsymbol{E_V}$ to $\boldsymbol{E_C}$ in bandgap of a semiconductor, as a result of interaction with other electrons, holes or photons. In the generation process, electron-hole pairs are created by exciting an electron, thereby creating a hole in the $\boldsymbol{E_V}$. Recombination is the reverse process where electrons from $\boldsymbol{E_C}$ and holes from $\boldsymbol{E_V}$ bands recombine, resulting in the emission of a photon. The lifetime of carrier generation for semiconductors relies on recombination processes that limit the current generation, hence the performance of the device. There are three different types of typical recombination processes [25][30]:

Auger Recombination

Auger recombination is significantly effective in semiconductors with high carrier concentration caused by heavily doping under concentrated sunlight. It involves three carriers. An electron and a hole recombine, but instead of emitting a photon, the energy is transferred to a third carrier, an electron in the $\boldsymbol{E_C}$. This process limits the lifetime and efficiency of the solar cell.

Radiative (band-to-band) Recombination

Radiative recombination is the recombination mechanism that dominates in direct bandgap semiconductors. It occurs when an electron from E_C directly combines with a hole in the E_V and releases a photon which has similar energy to the bandgap of the semiconductor.

Shockley-Read-Hall (SRH) Recombination

Shockley-Read-Hall recombination, also called recombination through defects. It occurs when an electron/hole is trapped by an energy state in the forbidden gap which is introduced through defects in the crystal lattice. The free carriers are captured by the traps and released by thermal activation process subsequently.

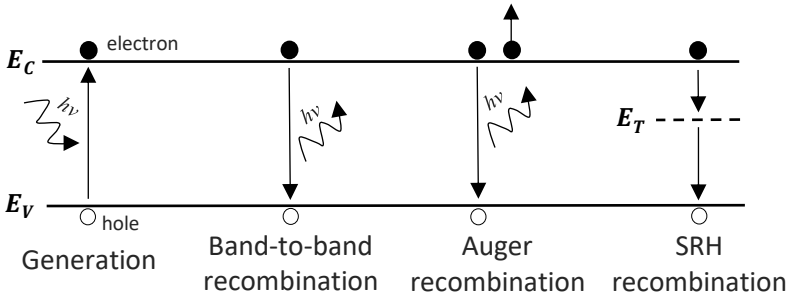

Figure 2.4: Generation and types of recombination processes.

2.3 Cu(In,Ga)Se_2 Solar Cells

2.3.1 Introduction and Device Configuration

CIGS is a I-III-VI_2 compound semiconductor material with a direct bandgap in the range 1.0 1.4 eV, and a high absorption coefficient (~10^5 cm^{-1}) [31], resulting in complete absorption of the sunlight in absorber layers of 2 µm thickness. Most common CIGS solar cells are grown in substrate configuration (Figure 2.5), which gives the highest efficiency but requires an additional encapsulation layer to protect the cells surface [32]. CIGS solar cells can be deposited on a variety of substrate such as soda-lime glass (SLG) and flexible metal or polymer foil [33]. The standard device configuration consists of a Molybdenum (Mo) back-contact, a *p*-type CIGS absorber layer, an *n*-type CdS buffer layer [23], a transparent conductive oxide (TCO), metal grids (usually Ag) and an antireflection coating..

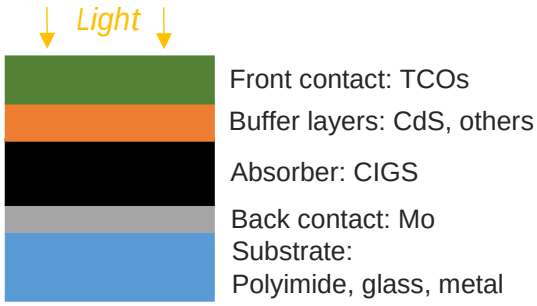

Figure 2.5: Substrate configuration for CIGS solar cells.

For an efficient solar cell, the front and back layers have to provide a good electric contact to the absorber layer. The front-contact layer is used for collecting and moving electrons out of the cell while absorbing as little light as possible. It is deposited using radio frequency (RF) sputtering onto the buffer layer. The buffer layer is deposited via chemical bath deposition (CBD) [34] or physical vapour deposition (PVD) [35]. The back-contact is used as an optical reflector which can reflect most of the unabsorbed light back in CIGS absorber and usually deposited on the substrate by RF sputtering. The absorber layer is central to the energy conversion process and deposited by several techniques such as co-evaporation [36], spray pyrolysis [37] or sputtering [38].

2.3.2 Absorber Layer Growth Processes

Several vacuum and non-vacuum process methods have been used to grow the absorber layer for CIGS TFSCs. Vacuum deposition methods include sputtering and thermal evaporation. Non-vacuum methods include ink printing, electroplating, spray pyrolysis and ultrasonic spray coating [3]. Each deposition method has several advantages and disadvantages. Even though, few processes are only limited by the small area depositions. However, the absorber deposition process is complex and the researchers are looking for economical and reliable methods to grow quality CIGS absorbers in large areas. For an efficient charge collection, the absorber layer requires a high mobility, a high open-circuit voltage ($\boldsymbol{V_{oc}}$) and low recombination mechanism. The carrier concentration of CIGS absorbers depending on the device configuration, absorber thickness and the absorber treatments can vary between 10^{16} and 10^{18} cm^{-3} with high mobility above 10 $cm^{-2}V^{-1}s^{-1}$ [39]. Few examples of absorber layer growth processes are given below:

Co-Evaporation from Elemental Sources

Co-evaporation is the most successful technique for high efficient solar cells, where a simultaneous evaporation of the elements (Cu, In, Ga and Se) from multiple sources are used in single or sequential processes [4]. This process has three different recipes, where Se is added in excess during the whole deposition processes. These different co-evaporation recipes are the constant rates, bilayer/Boeing process [40][41] and 3-stage process.

In the constant rate process, $Cu(In,Ga)Se_2$ is deposited throughout the process with a homogeneous Cu distribution, leading to a Cu-poor absorber layer for high efficiency solar cells.

The bilayer process starts with the deposition of Cu-rich $Cu(In,Ga)Se_2$ and gradually transforms to an In-rich composition at the end of the process. This process results in larger grain sizes compared to the constant rate process.

The 3-stage process leads to the most efficient solar cells up to now and was introduced by the National Renewable Energy Laboratory (NREL) [5]. In the 1st stage, first a precursor layer of In and Ga together with Se is deposited. In the 2nd stage Cu is deposited together with Se until the layer becomes stoichiometric. In the

3rd stage In and Ga are added again together with Se until the layer becomes Cu-poor. Films prepared by this process exhibit a smooth surface, which reduces the number of defects and recombination at the junction [3].

Spray Pyrolysis of Metal Chalcogenides and Selenisation

The spray pyrolysis technique is currently being developed at CREST for CIGS devices [8]. It is one of the low-cost atmospheric deposition techniques and a viable alternative to the vacuum-based methods. The vacuum-based techniques require high capital investment and therefore, the avoidance of techniques could potentially reduce the manufacturing costs of the solar cells. Spray pyrolysis method is a solution-based technique and allows the potential of easily adjusting the precursor solution and deposition parameters, depending on the required material properties. The solutions are sprayed in air, using a manual or an automated chromatography atomizer. However, the sprayed materials are often of lower quality than the vacuum-based deposited materials [42]. Therefore, spray pyrolysis is a challenging technique, and a deposition process should be fully optimised in order to obtain good material properties. The CIGS film formation requires a second process step. Deposition of precursor solution is followed by rapid thermal annealing (RTA) with Se pellets as a source of Se in a furnace, to obtain an optimum compound formation via the chalcogenisation reaction. This is commonly referred as selenisation process and is a critical step in the absorber formation which defines the properties of the final CIGS film [6][7][43].

2.3.3 Working Principle

A schematic diagram of a substrate CIGS based solar cell having a structure of glass substrate/Mo/*p*-type CIGS/*n*-type CdS/intrinsic ZnO/TCO is shown in Figure 2.6 (a). The incident light falling on the TCO front contact passes through CdS buffer layer ($\boldsymbol{E_g}$ ~ 2.4 eV) and it gets absorbed up to 2.4 eV in the CIGS absorber layer where electron-hole pairs are mainly generated [44]. Only photons with energy larger than the band gap can be absorbed and used for energy. Photogenerated carriers are separated because of the intrinsic field and the charge carriers are transported across the heterojunction (between CIGS/CdS) [26]. Electrons within the diffusion region are pushed away from the *p*-type absorber to the *n*-type buffer layer and

collected by the *n*-type electrode. Similarly, the opposite process is applied for the holes.

The Mo layer acts as a reflector and reflects unused light back into the absorber. Selenisation of CIGS layer in Se vapor results in the formation of $MoSe_2$ layer at CIGS/Mo interface. It is believed to be essential in fabricating of highly efficient solar cells and acts as a quasi-ohmic electrical contact [45][46]. The thickness of $MoSe_2$ layer plays a big role in the cell performance, and a thicker layer may cause a high resistivity (in the range of 10^1 10^4
peeling off the CIGS/$MoSe_2$/Mo layers from the glass substrate [47][48].

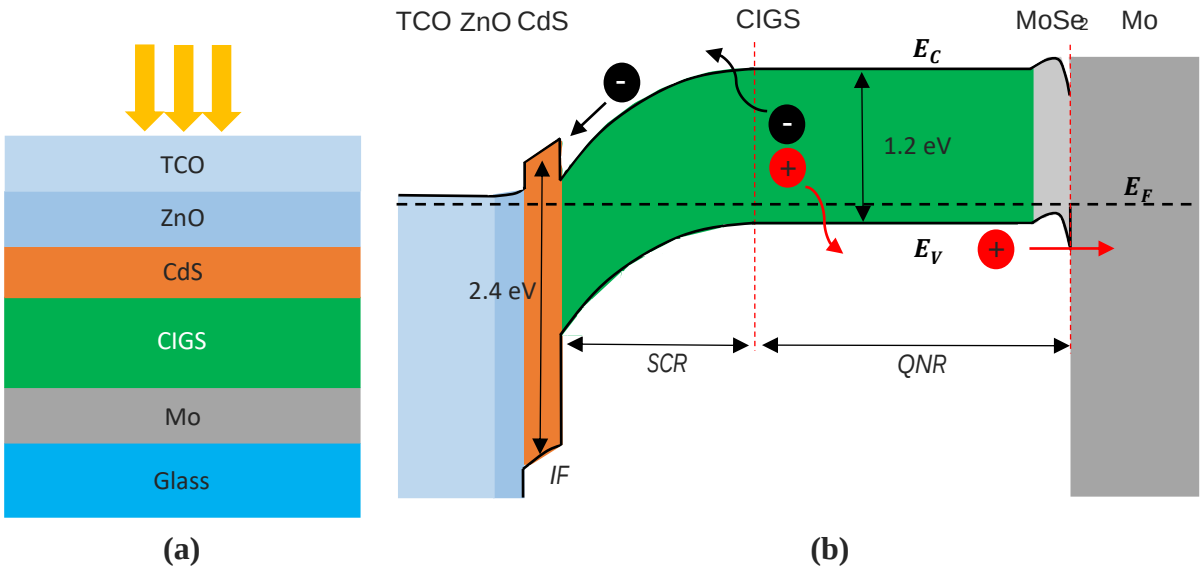

Figure 2.6: (a) Substrate configuration and (b) band diagram of a CIGS solar cell.

2.3.4 Recombination Mechanisms

Three main recombination mechanisms that may occur in a CIGS device are shown in Figure 2.6. These are the recombination at the interface (CdS/CIGS), space-charge region (SCR) and quasi-neutral region (QNR) [30]. Different rate of recombination mechanisms can be probed using temperature dependent electrical measurements which are discussed in depth in Chapter 3.

1. The CdS/Cu(In,Ga)Se_2 Interface Recombination

Interface recombination (IF) is affected by the band alignment at the emitter/absorber interface and can be enhanced by tunnelling. This results in a strong temperature

dependence of the ideality factor (A). The band alignment at the absorber interface results in a conduction band offset (CBO) and can play a significant role in the device performance [49]. There are two possible types of CBO depending on its

or

alignment is sufficiently large then the photogenerated current is blocked, thus efficiency will rapidly drop to zero [50]

shown in Figure 2.7 (b), the interfacial recombination current increases which becomes a problem in forward bias, hence reduces the fill factor and voltage of the device [51] [52]. The optimal CBO is found to be +0.3 eV which offers a good device performance, and further increase in CBO will introduce an energy barrier against the photogenerated electrons [53][54][55].

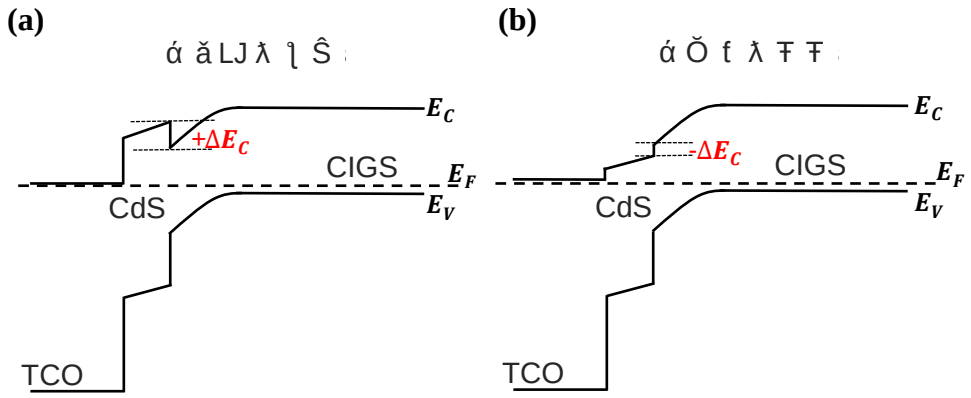

Figure 2.7: (a) a positive [spike] and (b) a negative [cliff] conduction band offset configuration.

2. The SCR and QNR Recombination

The SCR is the region where the E_V and the E_C bands bends in a certain region towards to the interface in order to reach electrostatic equilibrium [56]. The bending of the energy bands involves displacement of charge carriers near the interface. The region on either side of the SCR towards the back contact is called quasi-neutral region. In forward bias, injected minority carriers diffuse through QNR and recombine at the semiconductor surface. In reverse bias, minority carriers generated at the semiconductor surface, diffuse through the QNR, and extracted by SCR. In both SCR and QNR recombination, the V_{oc} is limited by the E_a = E_g. If A = 2, then the device is dominated by the SCR recombination, whereas with A = 1 then device is

dominated by QNR recombination [31]. Recombination can be reduced by optimizing the buffer/absorber offset, tunnelling and reducing the defects in the absorber.

2.4 Cadmium Telluride (CdTe) Solar Cells

2.4.1 Introduction and Device Configuration

CdTe is a II-VI group semiconductor which has an ideal bandgap (E_g of ~1.5 eV) for solar absorption (~10^4 cm^{-1}) according to the Shockley-Queisser limit [10][57]. The devices can be grown in both substrate and superstrate configurations (Figure 2.8), but the highest efficiency is achieved using the superstrate configuration [32]. The most common CdTe solar cells consist of a *p*-*n* heterojunction containing a *p*-doped CdTe layer with an *n*-doped CdS layer [58] and grown on TCO coated glass substrates. The choice of glass substrate depends on the growth process temperatures for temperatures below 550°C a low-cost SLG or high-temperature processes (550 600°C) an alkali-free glass can be used.

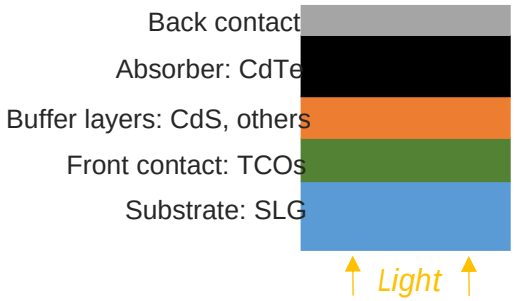

Figure 2.8: Superstrate configuration for CdTe solar cells.

The most commonly used TCOs are fluorine-doped tin oxide (FTO) or indium tin oxide (ITO) depending on the device configuration and can be RF-sputtered. TCOs require to have an electron affinity below 4.5 eV in order to form an ohmic contact and have a good band alignment with the CdS layer [32]. If the electron affinity of the TCO is higher, then a blocking Schottky contact is formed.

The CdS layer has a E_g of 2.4 eV and the absorption of light becomes stronger above this bandgap. Thus, the absorbed light within CdS cannot reach the absorber layer and causes photogenerated carriers not to be collected, hence limiting the J_{sc}. In addition, significant interfacial recombination occurs at CdS/CdTe interface. This is [59]. Using a buffer layer which have a higher bandgap

can overcome this absorption problem.

A completed device requires back contacts. A *p*-type CdTe has a work function of ~ 5.7 eV and forming an ohmic contact at the back of the device requires metals with higher work function than CdTe. Such metals are not available and thus a Schottky barrier forms at the back-contact which results in the rollover effect on the *J-V* characteristics. To overcome this problem, chemical etching on the CdTe surface or a post-deposition annealing or a buffer layer with high carrier concentration are often used [60]. Commonly used metal contacts with different metallisation combinations are Cu/Au [61][62], Cu/graphite [63], ZnTe doped with Cu and Au or Ni metallisation [64][65], Cu/Mo [66]. Alternatively, Ni:P, ZnTe, Au [67] or Sb_2Te_3/Ni [68] Cu-free back contacts have also been considered. Cu-based back-contacts are often used in CdTe devices. Initially devices show an improvement on *J-V* characteristics, especially at higher bias voltages where the rollover effect occurs. However, in some cases the degradation is reported indicating the electromigration of ionised Cu atoms. This can be a problem for the long-term stability and suggests that Cu-based contacts should be avoided for commercial modules [60].

2.4.2 Absorber Layer Growth Processes

CdTe is an excellent material that can be grown by many deposition techniques [69]. Techniques with deposition temperature above 500°C such as close-spaced sublimation (CSS) or close-spaced vapor transport (CSVT) are classified as high temperature processes, and deposition temperatures below 450°C such as electrodeposition, high vacuum evaporation (HVE) and sputtering are classified as low temperature processes. The carrier concentration of CdTe absorbers depending on the device configuration, absorber thickness and the absorber treatments varies between 10^{14} and 10^{17} cm^{-3} with high mobility above 10 $cm^{-2}V^{-1}s^{-1}$ [70].

Close-Spaced Sublimation (CSS)

CSS is one of the simplest vapor deposition techniques where semiconductor materials that evaporate below 800°C can be coated on glass substrates in both vacuum and atmospheric pressure with certain gas like Ar or N_2. The source materials are in the form of solid in either chunk or powder form [71]. The substrate and the source material are held close to one another in a vacuum chamber, and then heated using two radiative heat elements (usually halogen lamps). The source

material is heated to some fraction of its melting temperature, and the substrate some lower temperature, causing sublimation of the source material. This allows vapours to travel a short distance (~2 mm) to the substrate, where condensation takes place to produce a thin film. The important process parameters are source temperature, substrate temperature, source/substrate spacing, pressure, and ambient. CdTe can be deposited at around 600°C with a thickness of 1

among other physical vapor deposition (PVD) methods, and can be simply scaled up for manufacturing purposes. The higher temperature for the CdTe growth enhances the depositions rates, and the quality of the junction formation, which results better device performance [71][72].

2.4.3 The $CdCl_2$ Treatment of CdTe

The cadmium chloride ($CdCl_2$) treatment is a key processing step identified in fabrication of high efficiency CdTe photovoltaic devices [73]. As deposited CdTe cells exhibit poor electrical performance after growth. The $CdCl_2$ treatment results in the removal of high densities of stacking faults, increase in grain size and reorientation of grains, thus enhances the electrical performance of the device. Moreover, there are several reports of Cl accumulation at CdTe grain boundaries with $CdCl_2$ treatment where it provides an electronic effect on diffused with the device performance through passivation [74][75] and also known to promote diffusion of sulphur in CdS/CdTe devices [76].

Using high temperature processes, deposited CdTe layers can exhibit large grain sizes of up to 10 µm due to the enhanced mobility of atoms at the growth surface. Applying $CdCl_2$ treatment does not always show an increase in grain size from the morphological point view, but reduces the structural defects and affects the grain boundaries. This results in a higher effective acceptor concentration [77]. In low temperature deposited CdTe layers, the grain size can be about 0.1-0.5 µm and post-deposition annealing or $CdCl_2$ treatment can be enhanced the grain growth [77].

2.4.4 Metastabilities and Recombination Mechanisms

In the recent past, laboratory device efficiencies above 22% have been reported [9]. Like other TFSCs, CdTe devices suffer from recombination mechanisms and

metastabilities prior exposure history of light and environmental stresses. These factors are critical in the device performance, especially $\boldsymbol{V_{oc}}$ [78][79]. Different recombination rates at different location can be found in CdTe devices depending on the device configuration. Locations such as, the interface (buffer/absorber or absorber/back-contact) and the bulk of the absorber (depletion region or quasi-neutral). In a generic CdTe device the architecture follows, soda lime glass/TCO/CdS buffer/CdTe absorber/back-contact as discussed before. The main recombination often found in CdTe devices is the buffer/absorber interface which is usually due to the CBO between the buffer and CdTe layer [80].

Transient and metastable changes in CdTe devices cause difficulties to obtain stability in device performance. Deep level defects, and migration or electronic activation of copper may be responsible for these behaviours. To measure reliable performance data at different laboratories, an appropriate sequence of preconditioning or stabilisation steps require prior performance testing. National Renewable Energy Laboratory (NREL) has introduced preconditioning procedure that can be employed prior to accurate performance testing [81]. Preconditioning includes such as, light soaking, temperature stress and forward/reverse bias on the devices. Such preconditioning procedures are used in Chapter 5 and 6 to investigate these metastibilities and attempt to obtain accurate measurements.

Chapter 3

Characterisation Techniques

3.1 Introduction

In this chapter, experimental and analytical procedures will be described with utilised instrumentations for electrical and optical characterisation techniques. The current density-voltage (*J-V*) is the most fundamental measurement technique which provides information on the overall performance of the device under standard test conditions (STC). The four key solar cell parameters are the open-circuit voltage ($\boldsymbol{V_{oc}}$), short-circuit current density ($\boldsymbol{J_{sc}}$), fill factor ($\boldsymbol{FF}$), and power conversion efficiency ($\boldsymbol{PCE}$). For more advanced electrical properties of semiconductors such as defect density, energy level of defects and carrier concentration, which are not highlighted in standard material characterisation, the capacitance spectroscopy is used as a measurement approach to cover these properties. Knowledge of these properties will help in understanding how these devices behave with different electrical excitation to improve the device efficiency. The *J-V* and capacitance spectroscopy techniques can be especially informative for the case of solution-processing devices which exhibit different recombination mechanisms to the vacuum-processing devices, and metastabilities due to prior exposure history of light and environmental stresses.

The objective of this chapter is to discuss the standard and advanced device characterisation techniques which help to determine the response of a solar cell under applied voltage, illumination intensity, temperature and frequency. Additionally, other techniques such as external quantum efficiency (*EQE)* for probing optical and recombination losses of a device, scanning electron microscopy (*SEM*) for morphological properties, electroluminescence (*EL*) imaging for evaluation the

device quality across the entire cell area and Hall effect measurements for the conductivity, carrier concentration and mobility of the films are also discussed.

3.2 Current Density-Voltage *(J-V)*

The *J-V* measurements under standard illumination, 1 Sun AM1.5G at 25°C are the most common and standard tool for device evaluation and characterisation. These measurements determine the response of a solar cell to optical and electrical excitation. Measurement equipment and standardised techniques are described elsewhere [21]. A precise characterisation of TFSCs is very important when obtaining PV parameters, recombination rates, or material properties. Among many electrical characterisation techniques, the 4-wire probe configuration is mainly used to eliminate the load resistance to provide high accuracy of measurements, since 2-wire probe configuration results in a huge internal resistance, reducing the photogenerated current density at smaller voltage biases. The electrical contacts between the samples and the measurements were utilized using micro-positioners (shown in Figure 3.1) with 4-wire kelvin probes (feature a unique Z adjustment capability), which offer a linear motion of 12 mm in each axis X-Y-Z, and 1.0 µm resolution. These micro-positioners are beneficial when working with small size solar cells, and in establishing a good connection to provide accurate measurements. The *J-V* characteristics for substrate devices (such as CIGS and CZTS) were measured using an ABET solar simulator (Figure 3.1) under 1 Sun illumination with Class A AM1.5G spectral match and uses a xenon arc lamp. The simulator has an in-house built temperature stage using an Adaptive® JUNIOR PID controller to maintain the sample temperature constant at 25°C. The controller is capable of operating temperatures between -25°C and 85°C. The stage has a metallic block (6 cm x 6 cm) where the samples are placed, and temperature is adjusted by a peltier with heat sinks and highly efficient DC fans. It uses an embedded reference Si photodiode (S1133-01) embedded to the stage for calibration. This set-up can be also used for preconditioning of TFSCs (such as CIGS and CdTe devices) where they exhibit metastable effects on *J-V* characteristics prior to exposure history. In these conditions, devices require temperature stress or light soaking in order to restore the *J-V* characteristics. National Renewable Energy Laboratory (NREL) introduced a standard protocol for preconditioning or stabilisation of devices which can be utilised to obtain accurate measurements [81]. For the superstrate devices (such as CdTe), the *J-V* characteristics were performed using an in-house solar simulator set-up with a xenon arc lamp and AM1.5G filter under 1 Sun illumination, calibrated using a reference Si photodiode.

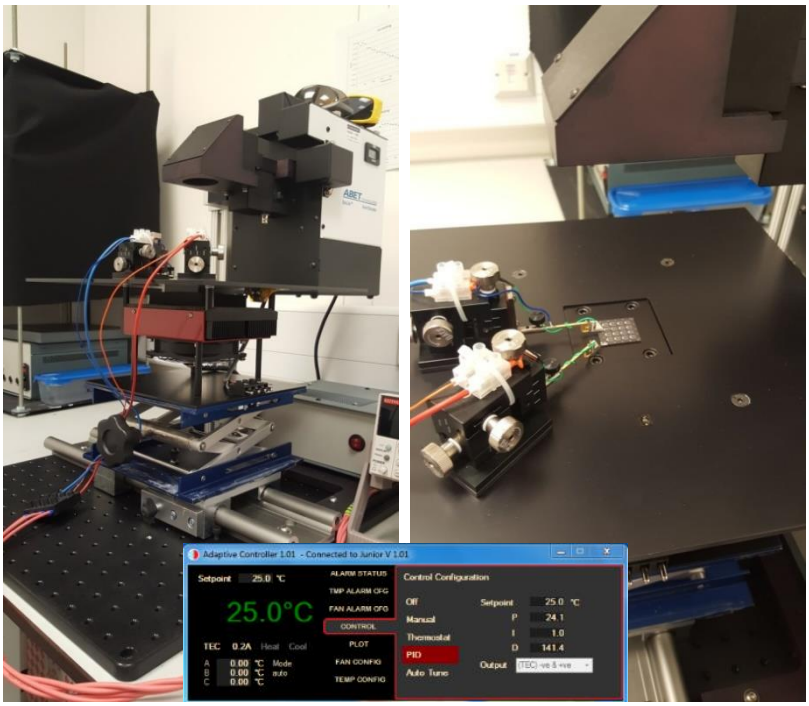

Figure 3.1: The ABET solar simulator with in-house built temperature-controlled stage for characterisation of substrate devices.

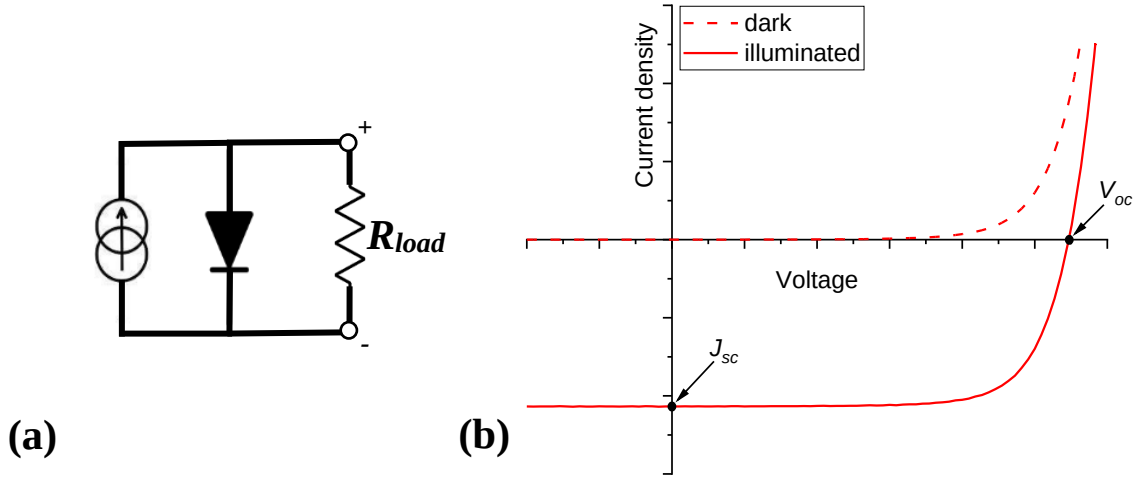

Figure 3.2: (a) An equivalent circuit for the ideal solar cell, and (b) the *J-V* curves under dark and light conditions.

The *J-V* measurements provide the basic parameters of a solar cell such as $\boldsymbol{V_{oc}}$ and $\boldsymbol{J_{sc}}$, which are determined from a *J-V* curve. These parameters are indicators of solar cell performance, and they are dependent on the light intensity and temperature. Figure 3.2 shows an equivalent circuit for an ideal solar cell and the *J-V* characteristics under dark and light conditions.

For an ideal diode, the dark current density when there is no illumination to the solar cell is given by:

$$\boldsymbol{J_{dark}(V) = J_0 \left\{ exp\left[\frac{qV}{AkT}\right] - 1 \right\}} \quad \textbf{(3.1)}$$

where $\boldsymbol{T}$ is the temperature of the cell in Kelvin, $\boldsymbol{k}$ is the Boltzmann`s constant (1.38×10^{-23} $m^2kgs^{-2}K^{-1}$), $\boldsymbol{J_0}$ is the saturation current density, $\boldsymbol{q}$ is the elementary charge, and $\boldsymbol{A}$ is the ideality factor (generally has a value between 1 and 2, and describes the recombination in the cell). If $\boldsymbol{A}$ = 2, then the device is dominated by the space-charge region recombination (SCR) recombination and if $\boldsymbol{A}$ = 1, then the device is dominated by quasi-neutral recombination (QNR) or interface recombination (IF) [31]. The illumination of the solar cell generates photocurrent. The overall current density-voltage as the sum of the $\boldsymbol{J_{sc}}$ and the dark current can be written as:

$$\boldsymbol{J(V) = J_{sc} - J_{dark}(V) = J_{sc} - J_0 \left\{ exp\left[\frac{qV}{AkT}\right] - 1 \right\}} \quad \textbf{(3.2)}$$

A real solar cell may suffer from power dissipation of parasitic resistances such as series resistance, $\boldsymbol{R_s}$ and shunt resistance, $\boldsymbol{R_{sh}}$. When the parasitic resistances are taken into account, the *J-V* behaviour can be described by a general single exponential diode equation:

$$\boldsymbol{J = J_{sc} - J_0 \left\{ exp\left[\frac{q}{AkT}(V - JR_s)\right] - 1 \right\} - \frac{V - JR_s}{R_{sh}}} \quad \textbf{(3.3)}$$

The $\boldsymbol{R_s}$ and $\boldsymbol{R_{sh}}$ represent of the losses that occur in series or parallel with the diode [82]. The $\boldsymbol{R_s}$ is a result of the material`s resistance to current flow in the bulk of the absorber layer or the contact resistances of the device. The $\boldsymbol{R_{sh}}$ is due to *p-n* junction non-idealises and impurities near the junction which cause partial shorting of the junction from the current leakage through shunt pathways around the edges of the cells. The $\boldsymbol{J_0}$ can be defined as:

$$\boldsymbol{J_0 = J_{00}\, exp\left(-\frac{E_a}{AkT}\right)} \quad \textbf{(3.4)}$$

with an activation energy E_a and prefactor J_{00} dependent on the specific recombination mechanism that dominates through forward current J_0 [83]. Combining equation (3.4) and (3.3), for $R_{sh} << J_{sc}/V_{oc}$, the open-circuit voltage is:

$$V_{oc} = \frac{E_a}{q} - \frac{AkT}{q} ln\left(\frac{J_{00}}{J_{sc}}\right) \quad \textbf{(3.5)}$$

There are two other important characteristic parameters beside V_{oc} and J_{sc} for solar cells. The first is the fill factor, FF:

$$FF = \frac{J_{mpp}V_{mpp}}{J_{sc}V_{oc}} \quad \textbf{(3.6)}$$

where J_{mpp} and V_{mpp} are the current density and voltage at the maximum power point (mpp). The mpp represents the point on the *J-V* curve under illumination, where the solar cell outputs the maximum net power. The FF is often used to characterise the quality of a solar cell junction, where expresses the ratio of the maximum power ($J_{mpp}V_{mpp}$) rectangle to the rectangle of $J_{sc}V_{oc}$ and is dependent on R_s and R_{sh}. The influence of R_s and R_{sh} on the *J-V* curve shown in Figure 3.3 (b) and (c). For an optimal device performance, the R_s should be minimized and the R_{sh} should be maximized, where both types of parasitic resistance can have a significant impact on the ***FF*** [84].

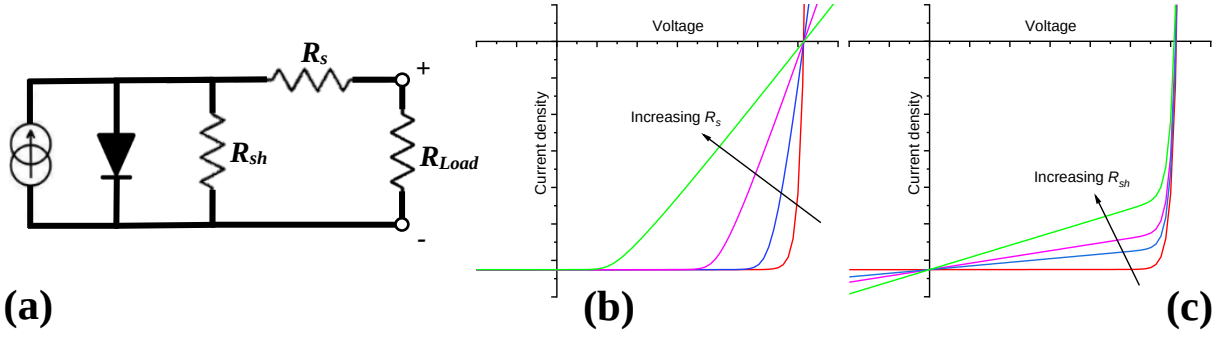

Figure 3.3: (a) Solar cell equivalent circuit with parasitic resistances. The effect of increasing (b) series resistance and (c) shunt resistance.

Finally, the power conversion efficiency, PCE relates the energy output from the cell to the incident light power density, P_s and it is given by:

$$PCE = \frac{P_{out}}{P_{in}} = \frac{J_{sc}V_{oc}FF}{P_s} \quad \textbf{(3.7)}$$

where P_{in} input power of the solar irradiance.

3.3 Temperature Dependent *J-V (JVT)*

The temperature ($\boldsymbol{T}$) dependence of $\boldsymbol{V_{oc}}$ in TFSCs yields the activation energy ($\boldsymbol{E_a}$) of the dominant recombination mechanism which limits the performance of the device. Activation energy can be defined as the minimum energy requires for the recombination to occur between an electron from the conduction band and a hole from the valance band. At $\boldsymbol{V_{oc}}$, there is no current through the device. Thus, the device performance is not affected by non-ohmic contacts or blocking barriers [85]. This technique can be used as a qualitative assessment of the recombination paths as it uses only the 1-dimensional temperature dependence of $\boldsymbol{V_{oc}}$ at a fixed light intensity, $\boldsymbol{V_{oc}(T)}$. It only identifies Shockley-Read-Hall (SRH) recombination at different locations such as at the buffer/absorber interface or in the bulk regions but does not consider absorber/back-contact interface. However, Paul and Li *et al.* reported here [78][86], that the separation and quantification of the SRH recombination at different locations, such as at the buffer/absorber interface, in the bulk region or absorber/back-contact interface can be identified by 2-dimensional temperature dependence of $\boldsymbol{V_{oc}}$ either at fixed/variable light intensity ($\boldsymbol{G}$), $\boldsymbol{V_{oc}(T,G)}$ or wavelengths ($\boldsymbol{\lambda}$), $\boldsymbol{V_{oc}(T,\lambda)}$. However, $\boldsymbol{V_{oc}(T,G)}$ and $\boldsymbol{V_{oc}(T,\lambda)}$ are not studied in this chapter due to the limitations of the instrument. Figure 3.4 (a) shows typical *JVT* curves for a CIGS device and Figure 3.4 (b) extrapolation of the open circuit voltage.

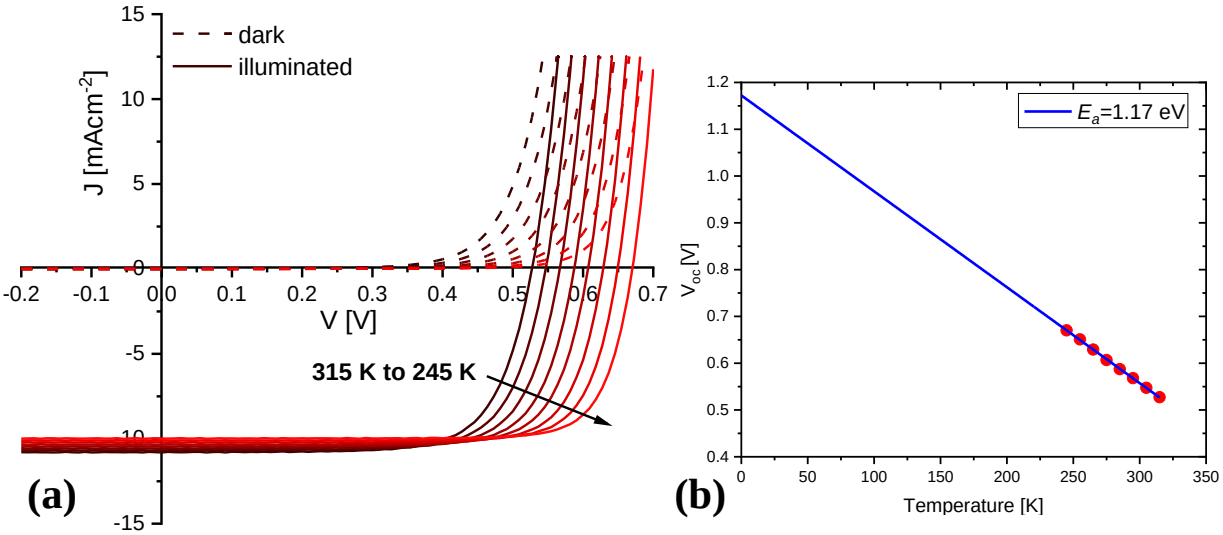

Figure 0.4: (a) The *J-V* curves at different temperatures for a CIGS device, and (b) extrapolation of the open circuit voltage towards 0 K.

The linear fit allows determination of E_a of the recombination which can be extracted from the intercept of $V_{oc}(T)$ at $T = 0\,K$ and slope provides J_{00}. The recombination is caused by the deep defects in absorber layers [87] or at the interface which reduces the device performance. Reduction of recombination requires different approaches in material and device engineering. The improvement of V_{oc} and FF, reduction of defects in the absorber and optimising the buffer/absorber band offset can be attributed to a decrease in recombination [88]. The E_a is not always equal to E_g, if other recombination mechanisms dominate the device such as IF recombination [89] or SRH recombination in the bulk [90]. Moreover, if $E_a = E_g$ is consistent SRH recombination dominates in the absorber. Whereas, if $E_a < E_g$, then the recombination mechanism dominates at the buffer/absorber interface [91].

The temperature dependent electrical measurements for this thesis were carried out in an evacuated closed-cycle helium cryostat (Janis CCS-150) with a measurement range of 40 to 320 K (Figure 3.5). The device temperature was adjusted using a LakeShore 335 temperature controller with the temperature measured by a Si diode attached to the bottom of the sample stage and a TENMA 72-7715 thermometer. The *JVT* curves were acquired using a Keysight B2902A source-measurement unit with a halogen, or a white LED light source (most recently installed).

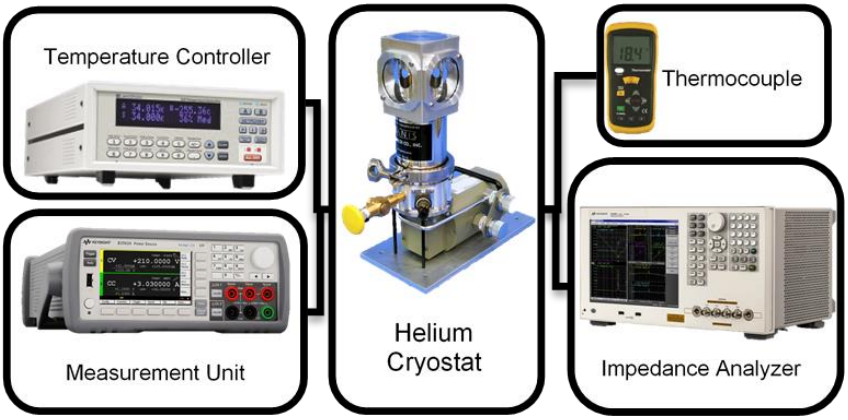

Figure 3.5: Schematic of experimental setup for electrical measurements.

3.3.1 Back-Contact Barrier

The rollover effect is a common deviation known as the current limiting in the forward bias of the *J-V* characteristics, especially seen in CdTe TFSCs [67]. This limiting effect is generally due to the back-contact barrier [92]. The apparent R_s values can

be an indicator of the rollover effect [93][94]. Most metals do not have sufficiently high work functions to form a good ohmic contact. Typically, metal-organic semiconductors form Schottky-type contacts [95]. The presence of any back-contact barrier can significantly affect the *J-V* characteristic of the device. The rollover effect can be modelled by an additional diode to the single diode equivalent circuit that has opposite polarity to the primary photodiode. Figure 3.6 shows the equivalent circuit for the double-diode behaviour where R^b_{sh} is the shunt resistance of the Schottky barrier [25].

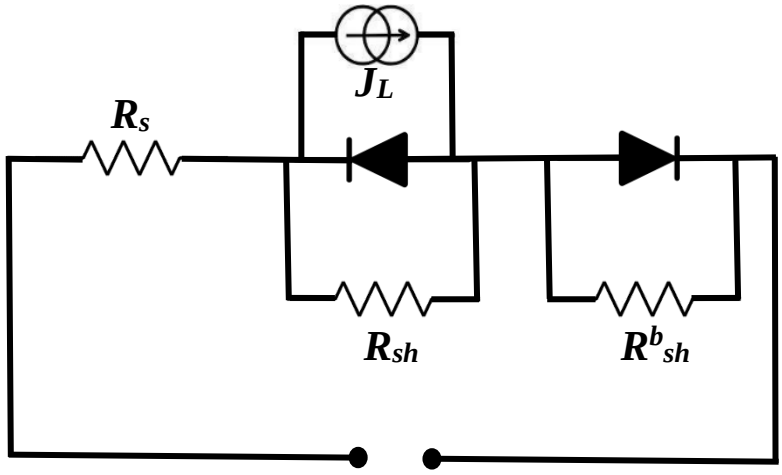

Figure 0.6: The two-diode equivalent circuit model showing the behaviour of the Schottky barrier at the back-contact.

Another common limiting behaviour that is commonly observed in TFSCs is crossover effect, where the dark and illuminated *J-V* curves crossover each other. The crossover effect can be caused by photoconductivity in the part of the device that contributes to parasitic resistances [96], a photo induced reduction in the junction barrier height [40] or a high density of deep states at the junction [83]. Both rollover and crossover effects are commonly observed in many CIGS and CdTe solar cells which limit the device performance [41][97][98].

3.3.2 Back-Contact Barrier Height Using *JVT*

The back-contact barrier height can be obtained using illuminated or dark *JVT* curves to determine the turning current (J_t). The J_t is the current at the transition from the positive *J-V* curvature of a diode to the negative curvature associated with current limitation at a contact barrier, and is approximately the saturation current. Figure 3.7 shows an example of an experimental *J-V* of a CdTe device with a

measurable value of back-contact barrier. The J_t can be calculated from the intersection of two linear fits to the data points above and below the onset of the rollover. The saturation current flow over a barrier (at the back-contact) at a T when a voltage applied is given by [25]:

$$J_0 = J_t = A^* T^2 e^{-\frac{q\Phi_b}{kT}} \quad (3.8)$$

where A^* is the Richardson constant for thermionic emission and k is the Boltzmann constant. The slope of the linear fit from the Arrhenius plot of the turning current dependency on the temperature ($ln(J_t/T^2)$ versus $1/T$) gives the barrier height, $q\Phi_b$ at the back-contact.

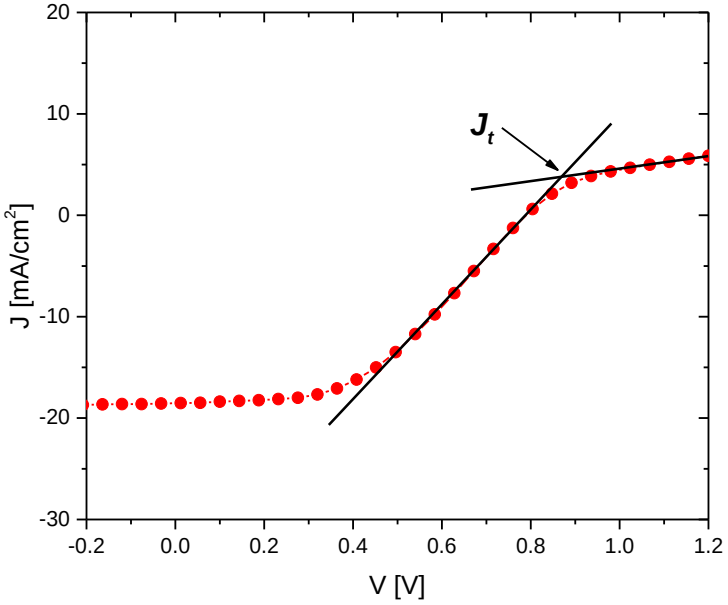

Figure 3.7: Example of an illuminated *J-V* curve for a CdTe device at 255 K with linear fits to determine the turning current, J_t.

3.4 External Quantum Efficiency *(EQE)*

Real solar cells encounter optical and recombination losses which are responsible for reducing the J_{sc}. The *EQE* measurements are valuable tool for characterisation of photocurrent, determination of the recombination losses, and describes of how well the cell converts solar energy to electrical energy. It also allows a comparison to be made with the measured J_{sc} from the *J-V* measurements. The *EQE* spectra for the measurements were acquired with chopped light using a Bentham PVE300 system (Figure 3.8) [99]. The systems consist of tuneable light source based on xenon-quartz tungsten halogen dual source and single monochromator with a spectral resolution of 5 nm.

Figure 3.8: Bentham PVE300 system for *EQE* measurements.

The *EQE* at given wavelength λ is defined as the ratio between the total number of collected carriers per incident photons on the solar cell given by [30]:

$$EQE(E_{ph}) = \frac{1}{q}\frac{dJ_{sc}(E_{ph})}{d\Phi(E_{ph})} \quad \textbf{(3.9)}$$

where $d\Phi(E_{ph})$ is the incident photon flux. It is possible to calculate the J_{sc} from an absolute measurement of the EQE for a given illumination spectrum:

$$J_{sc} = q\int EQE\,(\lambda)\Phi(\lambda)d\lambda \quad \textbf{(3.10)}$$

When the reflectance of the solar cell is known, $R(E_{ph})$ it is also possible to calculate the internal quantum efficiency, IQE [30]:

$$IQE = \frac{EQE(E_{ph})}{1-R(E_{ph})} \quad \textbf{(3.11)}$$

and it is defined as the ratio between the total number of collected carriers per absorbed photons on the solar cell.

3.5 Capacitance Spectroscopy

Capacitance spectroscopy investigates the capacitance of a rectifying junction as a function of the frequency, temperature and bias voltage. It can be measured by means of different techniques, such as capacitance-voltage (*C-V*), drive level capacitance profiling *(DLCP)* and admittance spectroscopy *(AS)*. These techniques are advanced measurement approaches which are not used in standard material characterisation. The measurement of junction capacitance is suited for probing the bulk and interface properties of the absorber layer in solar cells, such as density of defect states, defect levels and carrier concentration. The capacitance spectroscopy measurements were performed with a Keysight E4990 impedance analyser using the same cryostat (Figure 3.5) and the same electrical contacts utilised for the *JVT* measurements.

3.5.1 Admittance Spectroscopy *(AS)*

The *AS* investigates the capacitance of a *p-n* junction as a function of frequency and temperature [100]. It helps to estimate the density and energy levels due to the capture and emission of the electrically active defects and the position of the Fermi level in the bulk [101][102]. The *AS* technique assumes several conditions in the absorber layer of the device when measurements are carried out; these conditions are the following: 1) having a conductive enough absorber layer and neglecting the dielectric relaxation frequency of bulk absorber material; 2) ohmic back and front contacts with a single junction; and 3) only majority-carrier traps are observed [100].

When the frequency is too high at low temperatures, there is no time for carriers in the bulk to move in and out of the depletion edge in response to the applied bias, and this condition is called freeze-out [103]. With increasing temperature, or decreasing frequency, and vice versa an admittance step between low frequency, $\boldsymbol{C_{Lf}}$ and high frequency, $\boldsymbol{C_{Hf}}$ will be observed [104]. From literature, these admittance steps often referred as N1 and N2 steps [105][106], and can be probed either in the space charge region (deep defect) or close to the heterointerface (shallow defect). A controversial discussion in literature exists for many years concerning the origin of these admittance steps. N1 step was assigned to a minority carrier trap state close to the absorber/buffer heterointerface [104][107][108][109], or to a barrier for the diode current [109], or from a bulk region of the absorber [110].

There are several reports correlating N1 step to blocking of the diode current, which strengthens the origin to be due to a barrier [109][111][112][113]. N1 step typically has activation energies, $\boldsymbol{E_A}$, between 40 meV and 200 meV depending on the source of information [97][109][114]. These defects can be probed either in the space charge region next to the heterointerface or inside the buffer layer. Whereas N2 step is commonly assign to a response of a bulk in the absorber layer, and typically has $\boldsymbol{E_A}$, above 200 meV and above, and is considered as a deeper defect [105][107][114][115].

The junction capacitance is given by space charge capacitance:

$$\boldsymbol{C_{SCR} = \frac{\varepsilon_s}{w_d} = \sqrt{\frac{\varepsilon_s q N_A}{2V_{bi}}}} \qquad \textbf{(3.12)}$$

where $\boldsymbol{w_d}$ is the space charge width. The electrically active defects in the SCR of the rectifying junction make contribution to the junction capacitance at low frequencies or high temperatures. The effect of a single majority carrier trap to the junction capacitance is given by:

$$\boldsymbol{C(w_d) = C_{SCR} + \frac{C_{LF} - C_{SCR}}{1\, w_d{}^2 \tau^{*2}}} \qquad \textbf{(3.13)}$$

where $\boldsymbol{C_{LF}}$ depends on the $\boldsymbol{N_A}$ and trap density $\boldsymbol{N_T}$ of a p-type semiconductor, $\boldsymbol{\tau^*}$ the time constant of trap level and depends on $\boldsymbol{N_A}$, $\boldsymbol{N_T}$. In case of small trap concentration, $\boldsymbol{N_T \ll N_A}$, the time constant becomes $\boldsymbol{\tau^* = 1/\omega_0}$, where ω_0 is the inflection frequency.

$$\boldsymbol{\omega_0(T) = 2e_T(T) = 2v_{th}\sigma_{p,n}N_{C,V}\, exp\left(-\frac{E_A}{kT}\right) = \xi_0 T^2\, exp\left(-\frac{E_A}{kT}\right)} \qquad \textbf{(3.14)}$$

The inflection frequency is related to the emission rate $\boldsymbol{e_T}$ in the limit of small trap concentration, where $\boldsymbol{\sigma_{p,n}}$ is the capture cross section for electrons and holes, $\boldsymbol{v_{th}}$ the thermal velocity, $\boldsymbol{N_{C,V}}$ the effective density states in the conduction and valance band, $\boldsymbol{E_A}$ the activation energy of the defect level with respect to the corresponding band edge and $\boldsymbol{\xi_0}$ the temperature dependent emission parameter. By scanning the temperature and frequency, an Arrhenius plot of $\boldsymbol{ln(\omega_0/T^2)}$ versus $\boldsymbol{1000/T}$ can be constructed consisting of the frequency of either the inflection points in the

capacitance or the peaks in the conductance spectra $\boldsymbol{G/\omega}$. The $\boldsymbol{E_A}$ and $\boldsymbol{\xi_0}$ can be obtained from an Arrhenius plot slope and Y-intercept, respectively.

3.5.2 Capacitance-Voltage *(C-V)* Technique

The *C-V* technique investigates the depth profile of the net carrier concentration in the absorber layer. An ac voltage perturbation is applied to the dc bias voltage, and the current response is measured to obtain the junction capacitance. The variation in junction capacitance with dc bias is then recorded. Deep level defects can influence the measured capacitance depending on the temperature and the frequency of the ac voltage. Thus, sometimes it can lead to incorrect determination of carrier concentration.

The Schottky junction behaves as a parallel-plate capacitor with plate spacing equal to the depletion width and is a bias dependent. The small signal capacitance is defined as the charge response, $\boldsymbol{\partial Q}$ to a small change of voltage, $\boldsymbol{\partial V}$. The charge moving in and out of the cell with changing bias can be written as [30]:

$$\boldsymbol{C = \frac{\partial Q}{\partial V}} \qquad \textbf{(3.15)}$$

where $\boldsymbol{Q}$ is the charge. The amount of charge in a *p*-type semiconductor at a junction is:

$$\boldsymbol{Q = -A\sqrt{2q\varepsilon_s N_A(V_{bi} - V)}} \qquad \textbf{(3.16)}$$

giving capacitance to be:

$$\boldsymbol{C(V) = A\sqrt{\frac{q\varepsilon_s N_A}{2(V_{bi} - V)}}} \qquad \textbf{(3.17)}$$

where $\boldsymbol{q}$ is the elementary charge, $\boldsymbol{\varepsilon_s}$ the semiconductor`s dielectric constant, $\boldsymbol{N_A}$ the acceptor doping density, $\boldsymbol{V_{bi}}$ the built-in voltage, $\boldsymbol{w_d}$ the depletion width, and $\boldsymbol{A}$ the junction area. $(\boldsymbol{V_{bi} - V})$ is the expression for the capacitance of a parallel-plate capacitor with plate spacing equal to the depletion width. The depletion region has positive charges in the *n*-type material and negative charges in the *p*-type material, and completely free from the majority carriers [115]. Figure 3.9 shows a schematic diagram of the *p-n* junction and the built-in potential across the junction. The applied

voltage changes the steady-state balance between drift and diffusion, which can unleash the flow of diffusion current i.e., $\boldsymbol{V_{applied} < V_{bi}}$ = current is nearly zero and $\boldsymbol{V_{applied} > V_{bi}}$ = current flows through the *p*-*n* junction [116].

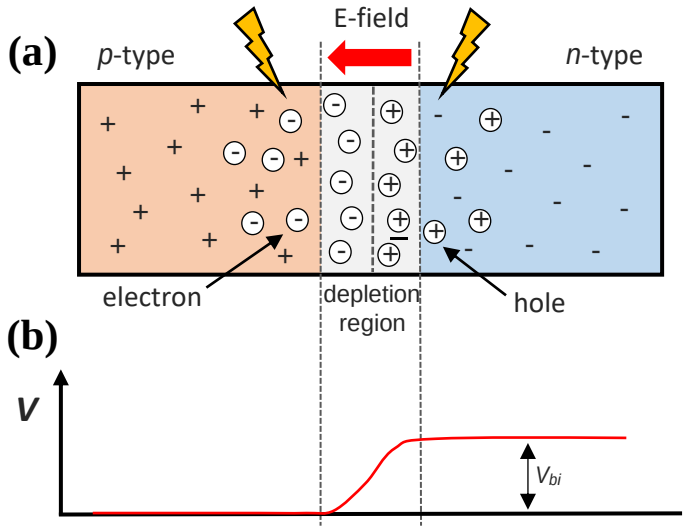

Figure 3.9: (a) *p*-*n* junction and (b) V_{bi} potential.

The width of the depletion region increases with decreasing doping density. The layer with lower doping will have a wider depletion region, thus more of the $\boldsymbol{V_{bi}}$ will be dropped into the layer [116]. The width of the depletion region can be approximated by:

$$\boldsymbol{w_d = \sqrt{\frac{2\varepsilon_s}{qN_A} V_{bi}}} \qquad \textbf{(3.18)}$$

Combining the depletion width (eq. 3.17), the capacitance (eq. 3.16) for a parallel-plate capacitor can be expressed as:

$$\boldsymbol{C = \frac{A\varepsilon_s}{w_d}} \qquad \textbf{(3.19)}$$

with plate spacing equal to the depletion width. When $\boldsymbol{C^{-2}}$ is plotted against $\boldsymbol{V}$ from (Mott-Schottky plots) equation 3.19, a linear response is obtained. Slope of the linear response is related to doping density, $\boldsymbol{N_A}$ and intercept is built-in voltage, $\boldsymbol{V_{bi}}$. The $\boldsymbol{V_{bi}}$ is an important parameter that decides that affects the $\boldsymbol{V_{oc}}$ and thereby the efficiency of the device.

$$\boldsymbol{\frac{1}{C^{-2}} = \frac{2(V_{bi} - V)}{A^2 q \varepsilon_s N_A}} \qquad \textbf{(3.20)}$$

This analysis is only valid for a *p-n* junction where the doping densities are different on both sides of the materials. If the doping densities are similar on each side, then the doping density at *p-n* junction in equation 3.20 needs to include both materials. Therefore, the equation 3.20 becomes:

$$\frac{1}{C^{-2}} = \frac{2(V_{bi}-V)}{A^2 q \varepsilon_s N_A}\left(\frac{1}{N_A}+\frac{1}{N_D}\right) \quad \textbf{(3.21)}$$

assuming the dielectric constant is the same on each side.

Assuming the charge density at the edge of depletion region, carrier concentration from *C-V* measurements is given by [117]:

$$N_{CV}(w_d) = \frac{2}{q\varepsilon_s C_1}\frac{1}{A^2(1/C^2)\partial V} \quad \textbf{(3.22)}$$

3.5.3 Drive-Level Capacitance Profiling *(DLCP)*

The *DLCP* measures the change in junction capacitance with a varying peak to peak oscillating voltage, V_{ac} (drive level) and allows an estimation of the defect density from both shallow and deep defects [118]. Assuming a small enough drive level amplitude (δV), the capacitance can be estimated as $C \approx C_0 + C_1(\delta V) + \cdots$ where C_0 can be denoted as the capacitance in the limit of zero drive level and C_1 as the first order correction to the junction capacitance for finite drive level [8]. These two parameters can be used to determine the bulk defect concentration (N_{DLCP}), including both the carrier concentration and the deep level defect states that can respond at the signal frequency. Defining the area of the cell A, q as the charge of an electron and ε as the dielectric constant of the material, then:

$$N_{DLCP} = -\frac{C_0^3}{2q\varepsilon_s A^2 C_1} \quad \textbf{(3.23)}$$

At low frequencies, *DLCP* should give similar results as *C-V* technique, since defects response to change their charge with dc and ac biases in *C-V* measurements [118]. Additionally, *DLCP* technique can be used to yield the deep level defect density as a function of frequency, that responds rapidly enough to follow the frequency of the signal. From defect density versus frequency plot the defect density at high frequency can be interpreted as the carrier concentration, and the difference between the defect densities at low and high frequencies to the deep level defect

density [118]. Addition of these two defect densities should provide a close agreement to the carrier concentration from the *C-V* technique.

3.6 Hall Effect Measurements

The Hall effect measurement is one of the most important characterisation techniques for TFSC materials to reveal the fundamental information about the majority charge carrier type (*p* or *n*), density, mobility and resistivity. These parameters are used to determine the overall device architecture which affect the performance of the device. A standard conventional Hall effect system operates with DC (static field) Hall measurements using van der Pauw technique.

The van der Pauw measurements are used to determine the sheet carrier density ($\boldsymbol{n_s}$) and the mobility (μ) by measuring the Hall voltage ($\boldsymbol{V_H}$) with a combination of a resistivity measurement and a Hall measurement. The technique consists of a series of voltage measurements with a constant current and a constant magnetic field applied perpendicular to the plane of the sample. Sample geometry is preferable to be square or rectangle to have a uniform magnetic field across the sample. The basic physical principle underlying the Hall effect is the Lorentz force [119], which is a combination of electric and the magnetic forces.

For the resistivity measurements, the sheet resistance $\boldsymbol{R_s}$ is determined and Van der Pauw demonstrates that there are two characteristic resistances $\boldsymbol{R_A}$ and $\boldsymbol{R_B}$, associated with the corresponding terminals shown in Figure 3.10. For $\boldsymbol{R_A}$, the voltage is measured by applying a current through the pair of contacts 1 and 2 and the voltage is measured across the remaining pair of contacts 3 and 4. Whereas for $\boldsymbol{R_B}$, the current is applied for the pair of contacts 2 and 3 and the voltage is measured across the remaining pair of contacts 1 and 4.

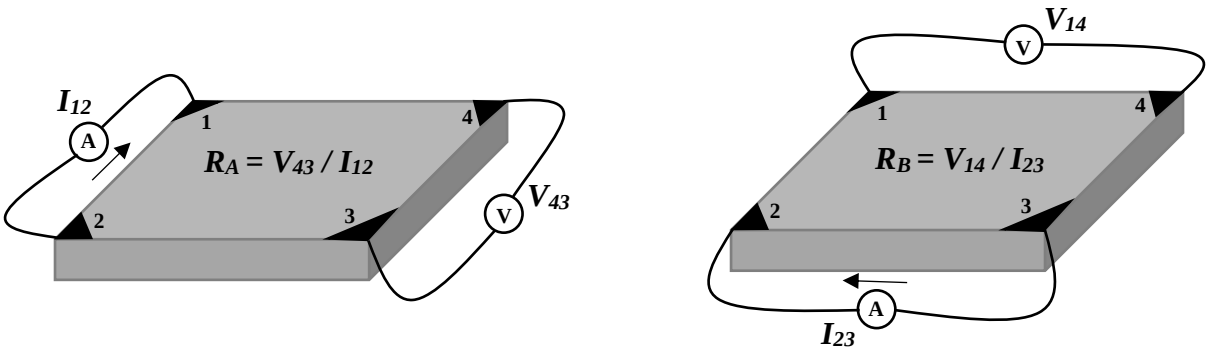

Figure 3.10: Van der Pauw configuration for resistivity measurements.

These two characteristic resistances are related to the R_s through the van der Pauw nist-equation and R_s can be solved numerically:

$$exp(-\pi R_A/R_s) + exp(-\pi R_B/R_s) = 1 \qquad (3.24)$$

If the film thickness is known, then the bulk resistivity can be calculated from $\rho = R_s d$.

For the Hall measurements, the sheet density of charge carriers in semiconductors can be determined ($n_s = nd$) by measuring the Hall voltage V_H. The Hall voltage is measured by applying a current through the opposing pair of contacts 1 and 3 and the voltage is measured across the remaining pair of contacts 2 and 4 (shown in Figure 3.11). If the V_H is negative then the measurement corresponds to *n*-type semiconductors and positive for *p*-type semiconductors [120].

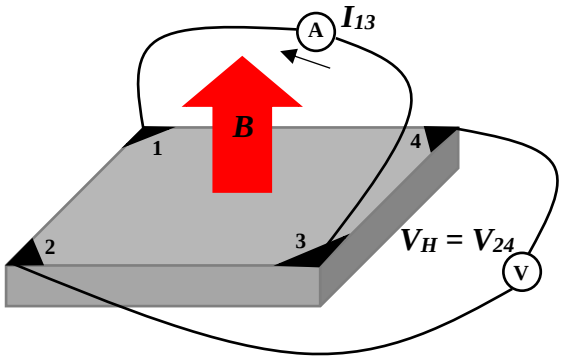

Figure 3.11: Van der Pauw configuration for Hall measurements.

Assuming a rectangular or a square sample with very small ohmic contacts at the corners, the Hall voltage is given by:

$$V_H = \frac{IB}{qnd} \qquad (3.25)$$

where d is the film thickness, I is the current applied, B is the magnetic field applied perpendicular to the sample surface, q is the elementary charge and n is the (bulk) carrier density. The Hall mobility can be determined from the nist-equation (equation 3.24), since the sheet resistance involves both sheet density and mobility:

$$\mu = \frac{V_H}{R_s IB} = \frac{1}{(qn_s R_s)} \qquad (3.26)$$

The Hall effect measurements were performed using a High sensitivity Parallel Dipole Line (PDL) Hall effect measurement system from SemiLab (Figure 3.12). This system is capable of both AC and DC Hall measurement modes [17], where the AC field can be used for materials with mobility of below 0.1 cm^2/Vs. This system uses a master and slave magnet with a large magnetic field approximately 2.5 T peak to peak. Hall measurement yields resistivity, sheet resistance, mobility, carrier concentration and carrier type. It provides critical and decisive information in development of new emerging solar materials (absorber, buffer, back-contact, y

low resistance films are very difficult or problematic to measure due to very low signal to noise (S/N) ratio. This AC PDL system generates alternating magnetic field and performs Lock-in detection of the Hall signal which provides more accurate results. The numerical Lock-in detection performed on the Hall signal is used to separate the in phase or the desired Hall signal component (X) from the out of phase parasitic component (Y) Furthermore, a positive sign of X indicates a *p*-type material and a negative sign a *n*-type material. Extending the Hall analysis with oscillating magnetic field, then the captured Hall signal becomes:

$$\boldsymbol{R_{XY}(t) = \frac{B_{max}\cos\omega t}{qn_s d} + \frac{B_{max}\omega A}{I}\sin\omega t + \alpha R_{XX} + N(t)} \quad \textbf{(3.27)}$$

where:

$\boldsymbol{R_{XY}}$ = the Hall signal, $\frac{V_H}{I} = \frac{B}{qnd}$

$\boldsymbol{R_{XX}}$ = the resistance associated with the corresponding terminals in Figure 3.11

$\boldsymbol{A}$ = effective loop area

$\boldsymbol{\alpha}$ = fraction of $\boldsymbol{R_{XX}}$ that appears in $\boldsymbol{R_{XY}}$ ($0 < \alpha < 1$) due to sample asymmetry

$\boldsymbol{N(t)}$ = noise or the rest of signal

For a successful and reliable Hall effect measurements from the PDL system followings are required:

- ¶ linear *I-V* responses from the contact check (step 1) and sheet resistance measurements (step 2)
- ¶ Hall resistance measurements (step 3)

- at least 10 cycles of magnetic field
- a visible signal variation which is following the signal of the magnetic field (and this is hard to see for highly resistive samples)
- a clear Fourier Transform (FT) peak
- a stabilised Lock-in out
    - Á where magnitude of Lock-in X > magnitude of Lock-in Y
- results from the Lock-in and the Fourier analysis are close to each other

Figure 3.12: SemiLab AC PDL Hall effect measurement system.

3.7 Electroluminescence *(EL)* Imaging

The *EL* is an imaging technique used in photovoltaic modules to evaluate the device quality across the entire cell area [121]. In this technique, the solar cell is exited with voltage bias, then a camera is used to capture the infrared light emitting from the excited solar cell. Areas of the cell with higher conversion efficiency present brighter luminescence on the image. The *EL* images were obtained using an Apogee Alta F800 camera, with a Qioptiq Inspec X IR lens and an aperture f-stop of 2.8 (Figure 3.13).

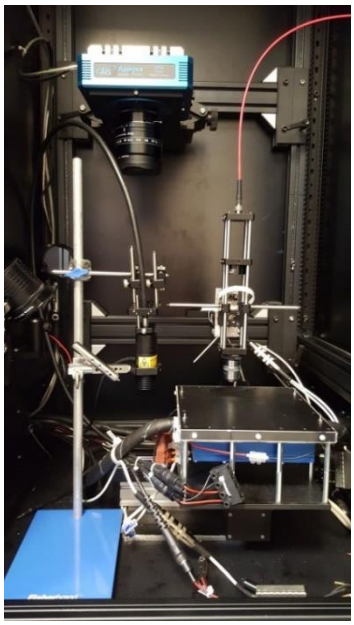

Figure 3.13 - Schematic of experimental setup for *EL* imaging.

3.8 Scanning Electron Microscopy *(SEM)*

The *SEM* is a powerful technique for characterising sample morphology which produces images by scanning the surface with a focused beam of electrons. The electrons interact with the atoms inside the sample and produce various signals containing information about the composition and surface tomography of the sample.

The film morphology was investigated using a Carl Zeiss 1530 VP field emission gun scanning electron microscope (FEGSEM) with 30 µm aperture size (Figure 3.14) and 5 kV operation voltage.

Figure 3.14: Carl Zeiss 1530 VP FEGSEM for film morphology.

Chapter 4

Solution-Processed Sb-Doped CIGS Thin Film Solar Cells

4.1 Introduction

Cu(In,Ga)Se_2 (CIGS) based polycrystalline absorbers with direct bandgaps and high absorption coefficients are promising solar cell materials. Power conversion efficiencies ($\boldsymbol{PCEs}$) exceed ~23% in laboratory-scale devices [1]. To reduce fabrication costs, solution-processing of CIGS absorbers is an attractive prospect. So far, the best performing solution-processed CIGS solar cell with a $\boldsymbol{PCE}$ of 18.1% was developed using hydrazine as a solvent [122]. However, using hydrazine raises safety concerns as it is highly toxic and explosive. As a safer alternative, a solvent combination based on an amine-thiol can be used to dissolve metal chalcogenides effectively for use in solution-processed thin film solar cells (TFSCs) and is presented elsewhere [123]. To enhance the $\boldsymbol{PCE}$ further, dopants such as sodium (Na), antimony (Sb) and potassium (K) are often added to the solar cells when processing the CIGS absorbers [124][2]. These dopants have shown improvements in electrical and structural properties of CIGS devices [125][126]. However, excessive doping can cause reduced grain growth, if not carefully controlled. Despite improvements in solar cell efficiency and significant progress in understanding of electrical properties, the loss mechanisms and formation of bulk defects have not yet been explained satisfactorily, especially with solution-processed devices [107].

This chapter is a comparative study of solution-processed CIGS devices with and without Sb doping, which investigates electronic, structural and defect properties. The CIGS absorbers were fabricated using metal chalcogenides dissolved in an

amine-thiol solvent mixture and combined with Sb as a dopant, in an effort to enhance the grain growth of CIGS, and improve the electronic properties of the device [127].

Capacitance spectroscopy is used as a tool to identify the effect of Sb doping on carrier concentration, density of states, defect concentration and the activation energy of defect levels [101]. Efficiencies of CIGS solar cells are affected by these properties, especially in solution-processed devices, and their determination is important for understanding limiting factors of the device performance. In this chapter, a range of measurement methods including drive-level capacitance profiling (*DLCP*), admittance spectroscopy (*AS*) and capacitance-voltage (*C-V*) profiling were used to characterise and identify these limiting factors. A series of light soaking experiments were studied to investigate any metastable behaviours that might occur in these devices. Additionally, the devices have been characterised by external quantum efficiency (*EQE*), scanning electron microscopy (*SEM*) and electroluminescence (*EL*) imaging for more insights into the understanding the device properties.

4.1.1 Device Preparation and Fabrication

The CIGS devices were fabricated by Farwah Bukhari using a molecular solution approach currently being developed at CREST [8]. This approach involves the spray deposition of metal sulphide solutions, based on a dithiol-diamine solvent combination. The soda-lime glass (SLG) substrate with a pre-sputtered Molybdenum layer (Mo, ~600 nm) has a MoN_x barrier layer (~30 nm) deposited by DC magnetron sputtering, which prevents selenium (Se) diffusion and excessive $MoSe_2$ growth, followed by sacrificial Mo layer (~50 nm). CIGS solutions were prepared using Cu_2S, In_2S_3 and elemental Ga with Se precursors dissolved in 1,2-ethanedithiol/1,2-ethylenediamine (1/10 v/v) solvent mixture, to target a composition of $Cu_{0.9}In_{0.7}Ga_{0.3}Se_2$. 2 mol% of Sb was added to the precursor solution. The final solution was then deposited by hand-spraying with a chromatography atomizer to a thickness of approximately 2 µm. The as-deposited films were then selenised in a graphite box contained of 12 pellets of selenium, inside a tube furnace for 90 minutes at 540°C. A buffer layer of CdS (~50 nm) was then deposited by chemical bath deposition (CBD) followed by i-ZnO and Al:ZnO layers both deposited using RF

sputtering (~50nm and 500 nm, respectively). Finally, ~500 nm thick front-contact silver grids were deposited by thermal evaporation (see Figure 4.1). The details of the solution preparation and techniques used in the fabrication of CIGS devices are provided in our previous work [123].

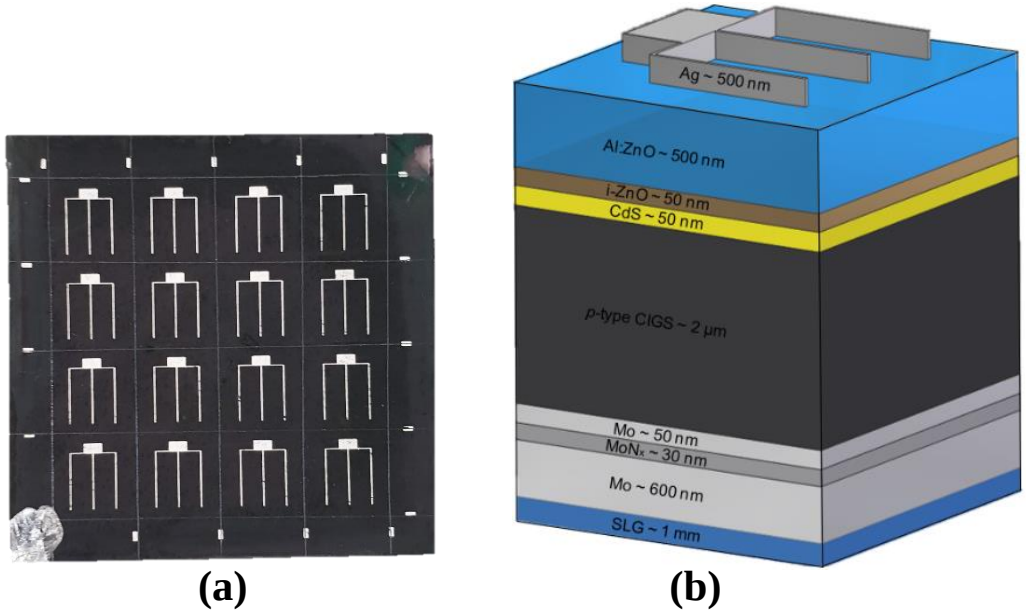

Figure 4.1: (a) A photo of a CIGS device, consisting of 16 cells with each cell area of 0.25 cm^2 (delimited by mechanical scribing), and (b) a schematic diagram of a cell (not to scale).

4.2 Results

4.2.1 *J-V* and *EQE* Analysis

The current density-voltage (*J-V)* characteristics of the best cells for each device are displayed in Figure 4.2. The measurements were taken at room temperature under 100 mWcm^{-2}, AM1.5G. The PV parameters corresponding to each of the *J-V* curves are summarised in Table 4.1. The Sb doping led to an increase of fill factor ($\boldsymbol{FF}$), open-circuit voltage ($\boldsymbol{V_{oc}}$), and short-circuit current ($\boldsymbol{J_{sc}}$). The increase in $\boldsymbol{FF}$ is most likely associated with the improved crystallisation in the bulk of the absorber causing lower series resistance ($\boldsymbol{R_s}$) losses. The improved crystal growth seen by *SEM* (Figure 4.3) results in an increased $\boldsymbol{J_{sc}}$ with the Sb doping.

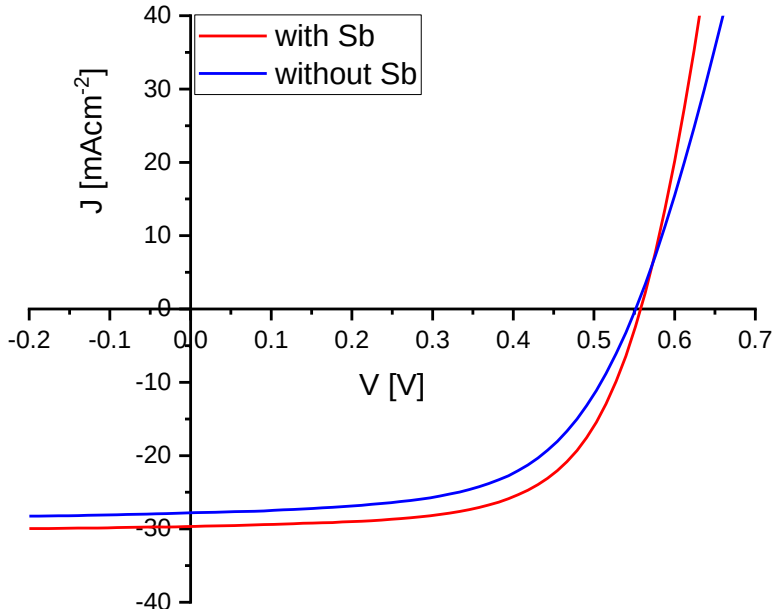

Figure 4.2: Illuminated *J-V* curves (100 mWcm^{-2}) at room temperature, AM1.5G.

	V_{oc} [mV]	J_{sc} [mAcm^{-2}]	FF	PCE [%]	R_s [Ω cm^{-2}]	R_{sh} [Ω cm^{-2}]
without Sb	551	27.8	0.585	8.96	21.83	3639.3
with Sb	556	29.7	0.626	10.3	8.625	5237.7

Table 4.1 - PV parameters of the best cells for both devices.

Typically, solution-grown CIGS films form a bilayer structure of a large-grain top layer which covers a fine-grain bottom layer [128][129][130], and this is also observed with the Sb doped devices. Although the bottom and top grains do not

extend through the entire depth of the absorber layer, the large-grain top layer is adequate to allow the device to function. Similar bilayer structures have been observed with the devices without Sb, and the other solution-processing absorbers in literature, such as $CuInSe_2$ (CIS) and $Cu_2ZnSn(Se,S)_4$ (CZTS) [131][132]. This bilayer structure has been often attributed to the incomplete selenisation process, or presence of impurities introduced by the precursors [132] [133] [134] [135]. Additionally, the absorber layer morphology contains some voids which might contribute as recombination centres to limit the solar cell device performance.

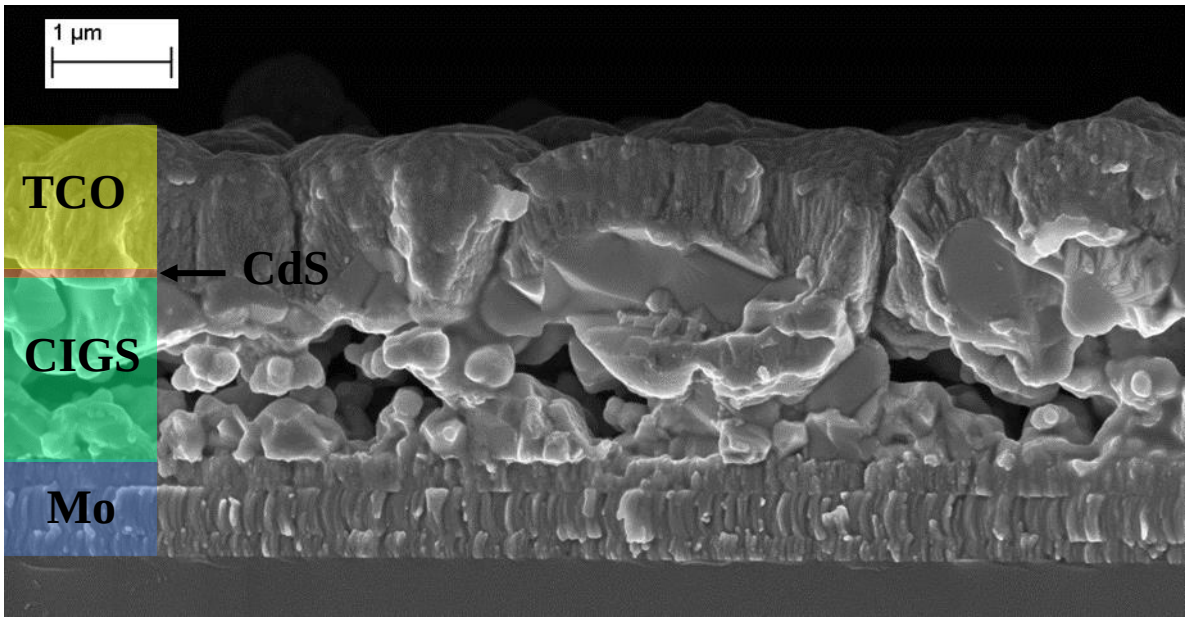

Figure 4.3: The *SEM* cross-section of the best cell for device with Sb, where a large-grain top layer and a fine-grain bottom layer of the absorber layer are visible.

To study the device quality across the entire cell area, the *EL* image (in Figure 4.4) was performed under a current load of ~ J_{sc} with acquisition time of 10 minutes. The *EL* imaging maps the degree of radiative recombination across the entire active area of the solar cell. The image shows inhomogeneous patterns of dark and bright regions over the cell area. This uneven signal might be due to random crystal CIGS grains (seen by *SEM)* amplified by their solution-based nature, presence of local shunts, or grain boundary recombination in the absorber layer [136]. The brighter regions around the front-contact grid may be attributed to higher losses across the TCO when the collection occurs further from where the injection current was applied. Although the cell has low material quality and higher radiative recombination, it is still

adequate to allow the cell to function and achieve power conversion efficiency ($\boldsymbol{PCE}$) of 10%.

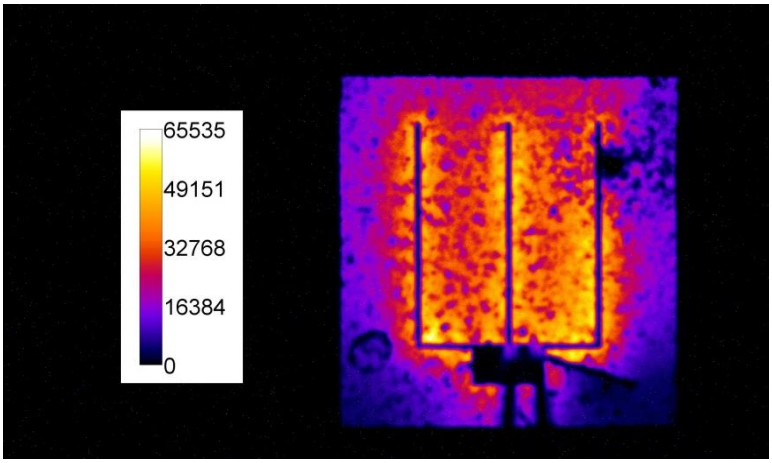

Figure 4.4 - *EL* image of the best cell with Sb. The image maps the electronic quality of the absorber with higher counts showing areas of higher radiative recombination and lower counts or dark regions corresponding to small cracks, scratches, or low material quality.

The *EQE* spectra for the best cells for the devices with and without Sb are shown in Figure 4.5. Both devices have a high collection just above 80% in the range of 500 to 700 nm and a gradual decay of the *EQE* at longer wavelengths. This may be attributed to recombination losses as a result of incomplete generation or collection in the fine-grain absorber layer. The small decay below 480 nm is due to the absorption in the CdS layer. There is also a shift observed in the long wavelength decay with Sb doping. This indicates a decrease in bandgap ($\boldsymbol{E_g}$), with only the change in In/Ga ratio able to explain this behaviour. Whilst the In/Ga ratio in the precursor solution is fixed, there is a clear effect of Sb which changes the final In/Ga ratio in the selenised absorber. The absorber $\boldsymbol{E_g}$ is extracted from the peak of the derivative of the long wavelength slope in the *EQE* data and found to be $\boldsymbol{E_g} = 1.15$ eV and 1.20 eV for the devices with and without Sb, respectively. Whilst the bandgap change is significant, it is currently not fully understood why it happens in this solvent/precursor system. Further work is being undertaken separately to understand this phenomena. Nonetheless, the *EQE* yields $\boldsymbol{J_{sc}}$ of 30.5 mAcm^{-2} for the device with Sb, and 27.3 mAcm^{-2} for the device without Sb. These values are in closed agreement with the $\boldsymbol{J_{sc}}$ values from the *J-V* measurements shown in Table 4.1.

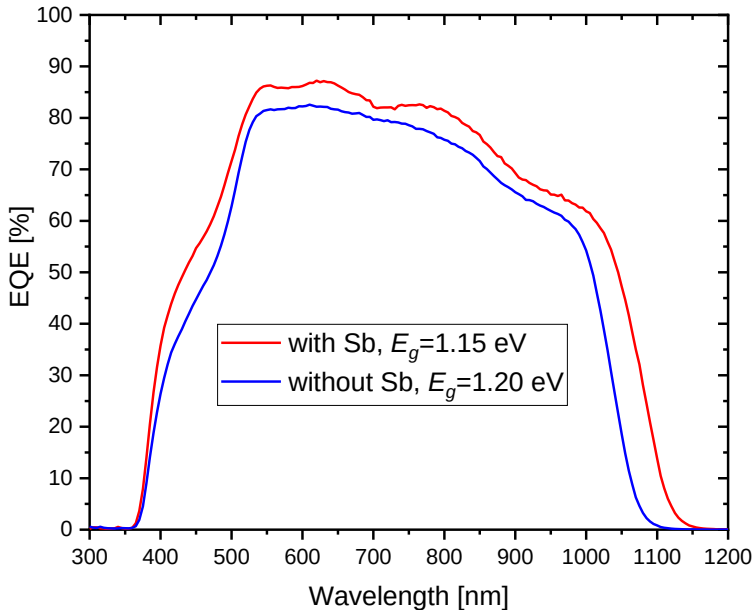

Figure 4.5: The *EQE* spectra of the best cells for the devices with and without Sb. The absorber bandgaps (E_g) are extracted from the peak of the derivative of the long wavelength slope in the *EQE* data.

In an effort to investigate further effects of the Sb doping on the *J-V* characteristics and the loss mechanisms, the devices were loaded into a helium cryostat to perform temperature dependent *J-V* (*JVT*) measurements. The *JVT* technique is a valuable tool for characterisation of the recombination mechanisms which limit the performance of PV devices. These measurements were carried out at 50 mWcm^{-2} with a halogen light source for temperatures between 315 K and 115 K.

Figure 4.6 (a) and (b) show the *JVT* curves for the best cell of the devices with and without Sb, respectively. The device with Sb has shown a strong temperature dependence of J_{sc}, visible at reverse bias as compared to the one without Sb. Since there is a significant shift in the bandgap between these two devices, and the halogen light source has a heavy infrared component, the significant change in J_{sc}, may be explained by the increased spectral response under the infrared light of the device with the narrower bandgap. This change is further reflected with the decreasing bandgap, a result of increased cell temperature. The crossover effect occurs for both devices where the dark and illuminated *J-V* curves cross each other. This may be caused by photoconductivity in the part of the device that contribute to parasitic resistances [96] or a high density of deep states at the junction [83]. For the device without Sb, there is more pronounced rollover effect appearing at low

temperatures, suggesting that at low temperatures the back-contact might start to behave non-ohmic, or a blocking barrier may be being formed [85][67]. Adding Sb to the absorber of the device helped to reduce the rollover at low temperatures. This shows more ohmic behaviour, suggesting that there might be less formation of a blocking barrier at the back-contact of the device.

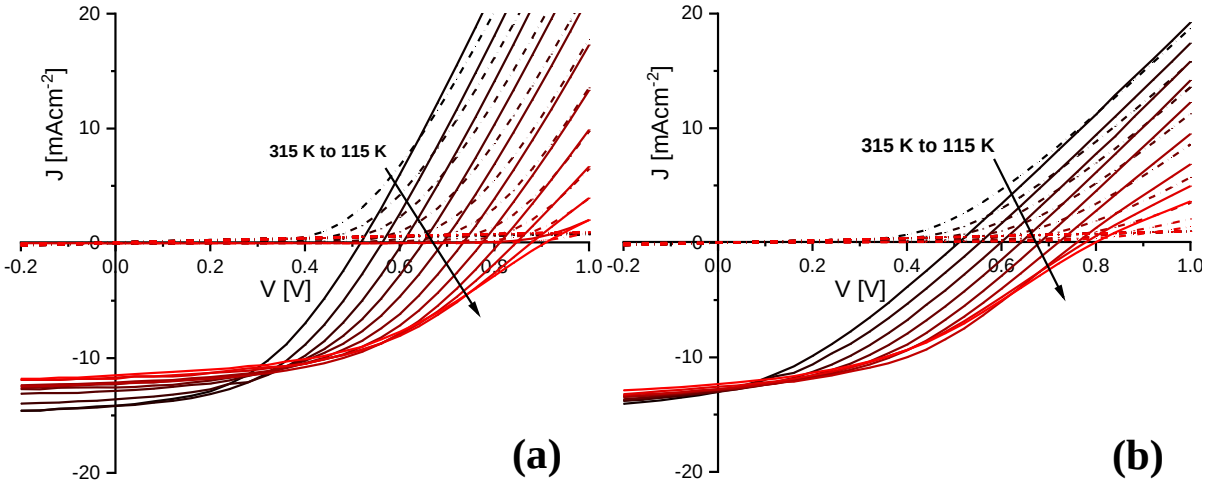

Figure 4.6: The dark and illuminated (50 mWcm^{-2}) *J-V* curves are displayed for temperatures between 315 K and 115 K (in 20 K steps) for the devices with (a) and without (b) Sb doping.

The open-circuit voltage ($\boldsymbol{V_{oc}}$) versus temperature ($\boldsymbol{T}$) analysis from the *JVT* measurements for the recombination mechanism yields an activation energy of $\boldsymbol{E_a}$ =1.17 eV (Figure 4.7) for the Sb doped cell, which is close to the bandgap ($\boldsymbol{E_g}$ =1.15 eV) determined from the *EQE* spectra (Figure 4.5). This indicates that the main recombination mechanism dominates in the bulk of the absorber. For the cell without Sb, $\boldsymbol{E_a}$ is found to be 1.11 eV and confirms that the cell is limited by the interface recombination, which is common for CIGS solar cells [109]. The incorporation of Sb into the CIGS might benefit the surface passivation and reduces the blocking barrier at the CdS/CIGS interface. The reduced barrier at the interface due to compositional changes might improve the band alignment of CdS/CIGS, thus improved PV parameters and better *J-V* characteristics.

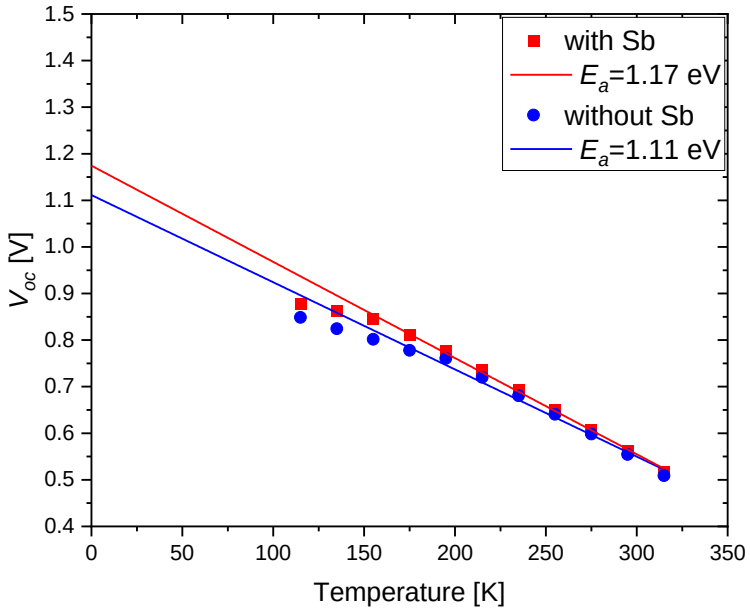

Figure 4.7: Temperature dependence of V_{oc} data, determined by the illuminated *J-V* curves from Figure 4.6 (a) and (b), yielding an activation energy for recombination for the devices with and without Sb, $E_a = 1.17\ eV$ and $1.11\ eV$, respectively.

4.2.2 Admittance Spectroscopy

The admittance measurement under equilibrium conditions (0 V bias, in the dark) for the device with and without Sb are shown in Figure 4.8 (a) and (b), respectively. The device doped with Sb shows an admittance step at low temperatures (between 265 K and 105 K) and high frequencies. This admittance step is often discussed in the literature as the N1 defect, and there has been considerable controversial discussion about the origin of the N1 step. Originally, the N1 step was assumed to be a response from defect states at the CdS/CIGS interface [107][108][109]. However, there are also other findings that assigned the origin of the step as a bulk defect in the absorber layer. Heath *et al.* [110] carried out a series of light soaking experiments on the *DLCP* measurements to demonstrate the origin of the defects. The results showed a significant increase in net carrier concentration after light soaking, thus indicates that the defects might originate from the bulk region of the CIGS absorber, and not from the CdS/CIGS interface.

The N1 defect has typical activation energies E_A, between 40 meV and 200 meV (depending on the reference, [109][97][114]), and is considered as a shallow level defect. The E_A was obtained from the slope of the Arrhenius plot (Figure 4.10) of the

inflection points determined from the maxima of the conductance spectra (Figure 4.9 (a)). It is estimated to be 42 meV, which can correspond to the N1 defect. The light soaking study presented in section 4.2.4 shows no significant changes in *C-V* depth profiles after 2 hours of light soaking. This might be an indication of the defect origin, which believed to be the CdS/CIGS interface for the case of Sb doped device.

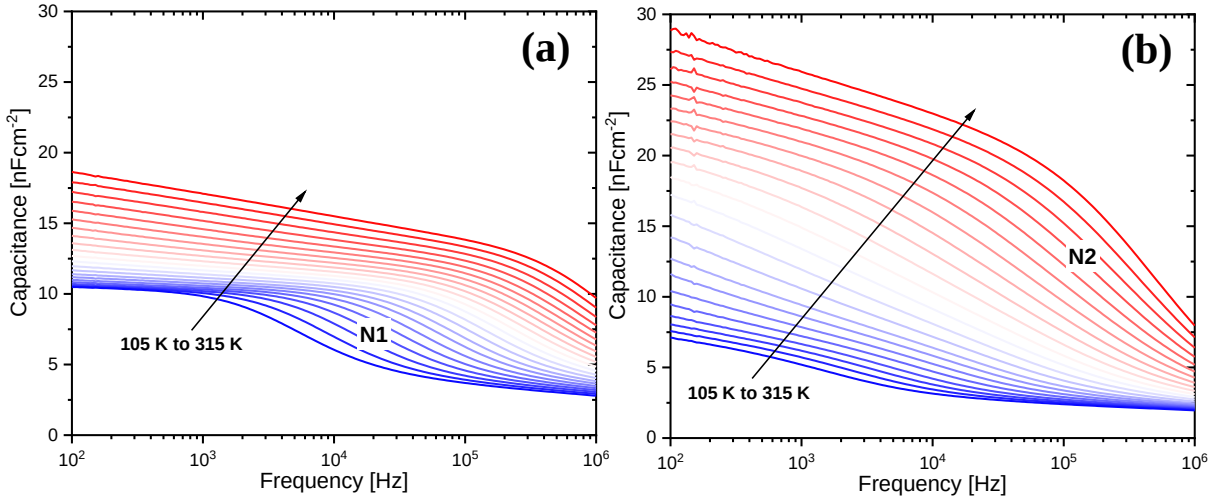

Figure 4.8: Admittance spectra in the dark at 0 V between 105 K and 315 K for the cell (a) with Sb, an admittance step is visible between 265 K and 105 K which is marked as "N1" and (b) without Sb, an admittance step is visible between 315 K and 265 K which is marked as "N2".

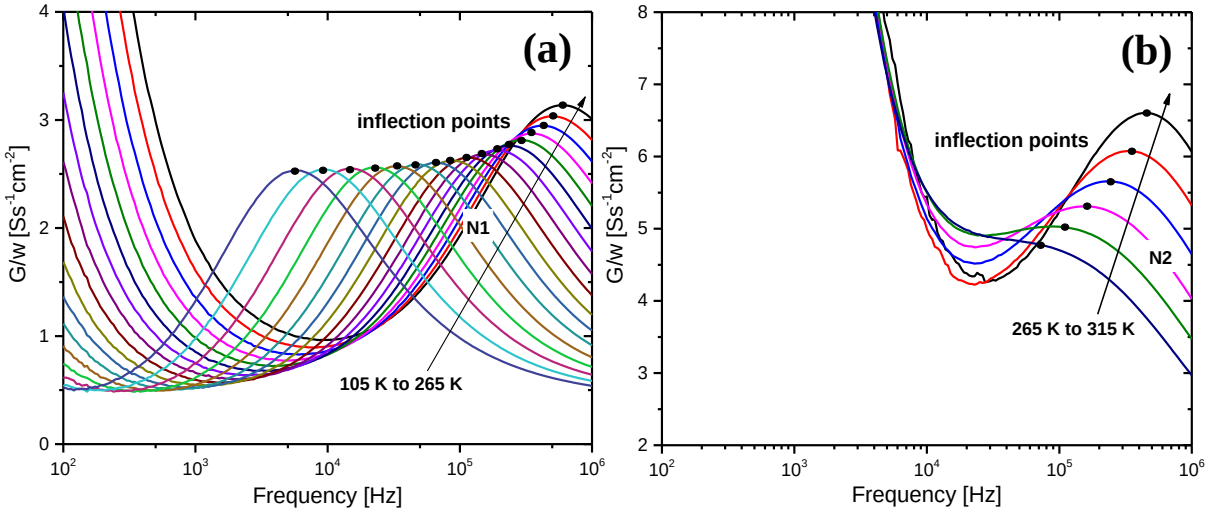

Figure 4.9: Conductance spectra for the device (a) with Sb shows the N1 step between 105 K and 265 K, and (b) without Sb shows the N2 step between 265 and 315 K. γ being the angular emission frequency of the inflection points and inflection points are marked in black at the maxima of each curve.

The device without Sb shows an admittance step at high temperatures (between 315 K and 265 K) and high frequencies with E_A of 330 meV (N2 is marked in Figure 4.8). This admittance step with higher activation energies is often discussed in the literature as the N2 defect. The N2 defect is considered as a deeper defect and has typical E_A>200 meV [114][137][138]. Although the origin of the N2 step is not fully understood, it is assumed to associate with the defects in the bulk of the absorber.

Figure 4.10 shows the Arrhenius plots for both with and without Sb doping. Since the device doped with Sb showed a reduced E_A (of 42 meV), it suggests that the dominant defects in the bulk without Sb have been removed. This reduction in E_A as a result of Sb doping could be due to increased crystallisation. When the bulk of the absorber has a higher degree of crystallinity there are fewer grain boundaries which might result in a lower density of defects [139] [87] [140] [141]. More about defect density will be discussed in section 4.2.3.

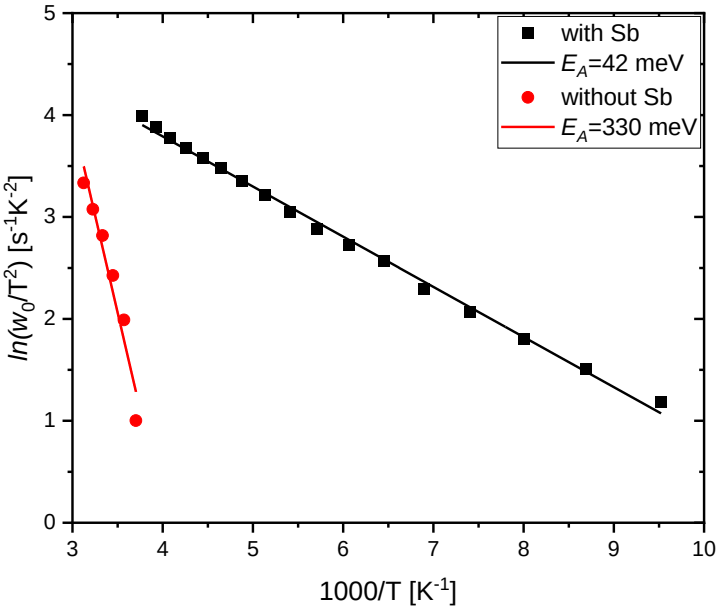

Figure 4.10: Arrhenius plot of the inflection points derived from conductance spectra in Figure 4.9 for the device with (black squares) and without Sb (red circles).

4.2.3 Capacitance-Voltage Analysis

The depth profiles were measured by means of the *DLCP* and *C-V* profiling techniques, shown in Figure 4.11 for the device with and without Sb doping. Both methods showed typical U-shaped depth profiles commonly reported in literature [110], however had an unusual tail off shape towards the back-contact of the device.

During the voltage sweep, the depletion width may possibly cross the interface between the large-grain and fine-grain, and causing this tail off behaviour seen in capacitance profiles. A significant difference in the net carrier concentration of roughly 3.19 x 10^{16} cm^{-3} was observed for the device with Sb when both techniques are compared. Whereas the devices without Sb showed no significant changes in net carrier concentration from both *C-V* and *DLCP* measurements. The *C-V* profiles can be affected by the presence of deep defects or interface defects. Thus, it can sometimes lead to an incorrect determination of the net carrier concentration. For this reason, *DLCP* profiles were used to estimate the net carrier concentration, as the *DLCP* measurements feature an improved signal-to-noise ratio and insensitive to the response from the interface defects, which will provide more accurate and reliable determination of the net carrier concentration.

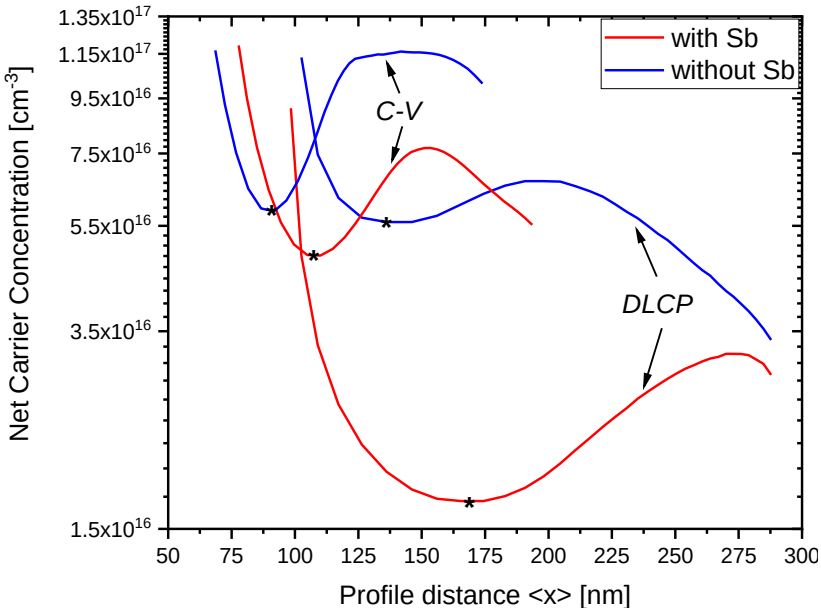

Figure 4.11: Comparison between *DLCP* and *C-V* depth profiles for the device with and without Sb, at room temperature. The net carrier concentration values are extracted at 0 V (marked as `*`).

The best cell for the device (from the *DLCP* measurements) with Sb showed a net carrier concentration of 1.69 x 10^{16} cm^{-3}, whereas the device without Sb had a net carrier concentration of 6.63 x 10^{16} cm^{-3}. This indicates that adding Sb into the precursor solution does not necessary dope the absorber layer, suggesting that the defects might be getting passivated by Sb doping. Moreover, the defect density was extracted from the *DLCP* technique under equilibrium conditions (at 0V bias and room temperature) to investigate the effect of the Sb doping on the device

properties. The measurements start by recording the capacitance data at 21 drive levels spaced by intervals of 10 mV over a range of 10 mV to 210 mV, where these values represent the amplitude of the oscillating voltage (drive level). At each drive level, measurements were recorded at 77 frequencies on a log scale. It is important to extend the measurement range to the highest frequency possible, as only shallow defects respond at these frequencies. However, if the frequency is too high, measurements can be affected by the series resistance of the probes. For this reason, the measurements were limited from 100 Hz to 100 kHz. At 100 Hz and 100 kHz, the capacitance was plotted versus the oscillating voltage (shown in Figure 4.12) in order to extract the values of $\boldsymbol{C_0}$ and $\boldsymbol{C_1}$ (from equation 3.23, in Chapter 3).

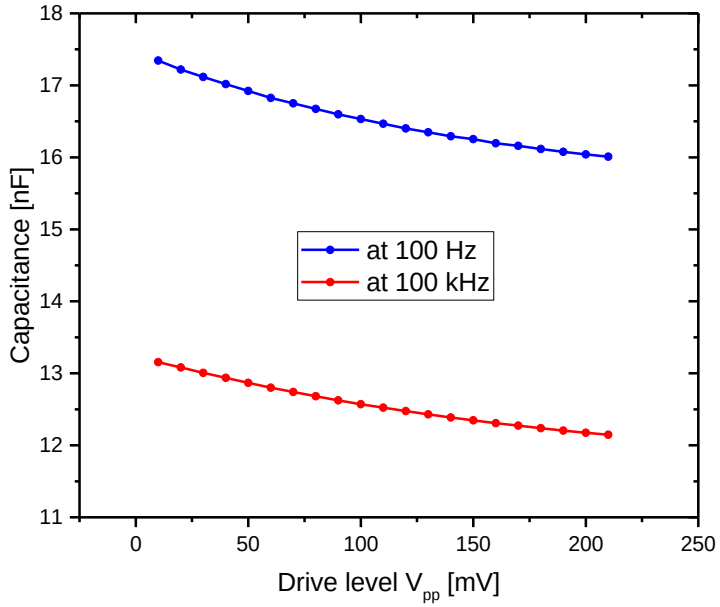

Figure 4.12: Capacitance versus drive level (peak-to-peak voltage) for the Sb doped device measured at 100 Hz and 100 kHz to extract $\boldsymbol{C_0}$ and $\boldsymbol{C_1}$ values in order to estimate the defect density.

The defect density for the device with Sb at 100 kHz can be interpreted as the net carrier concentration of 1.69 x10^{16} cm^{-3}. This value is in close agreement with that extracted from the *DLCP* depth profile displayed in Figure 4.11, and the difference between the defect densities at 100 Hz and 100 kHz can be attributed to the deep level defect density of 1.27 x10^{16} cm^{-3}, shown in Figure 4.13. For the device without Sb, the deep level defect density was found to be 3.02 x10^{16} cm^{-3}. Table 4.2 summarises the data extracted from the *DLCP* and *C-V* measurements. It is clear that the Sb doping did not have any positive effect on the net carrier concentration, but the defect density is reduced slightly.

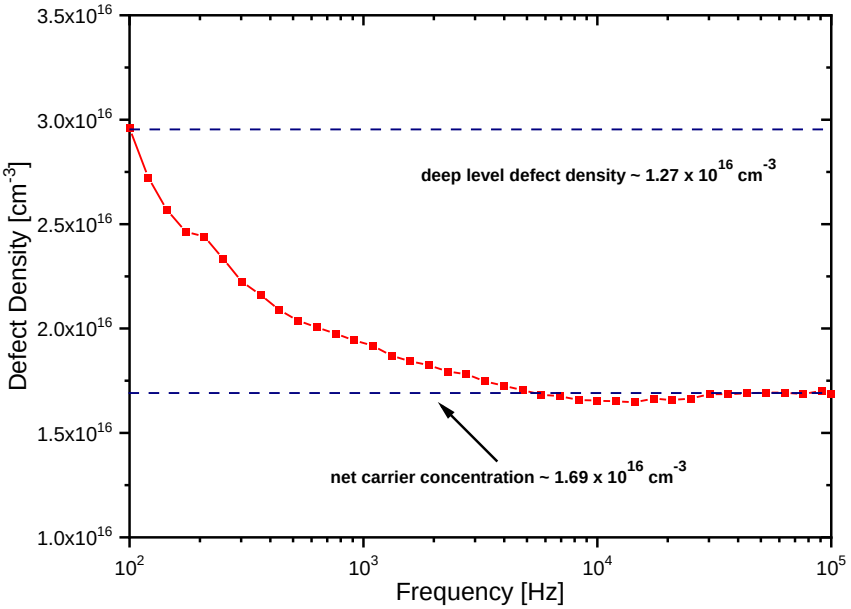

Figure 4.13: Defect density from the *DLCP* measurements for the device with Sb. The lower dashed line indicates the defect density interpreted as the carrier concentration and the difference between the dashed lines represent the deep level defect density.

	N_{CV} [cm^{-3}]	N_{DLCP} [cm^{-3}]	N_{defect} [cm^{-3}]
without Sb	5.49 x 10^{16}	6.63 x 10^{16}	3.02 x 10^{16}
with Sb	5.93 x 10^{16}	1.69 x 10^{16}	1.27 x 10^{16}

Table 4.2 – Summary of *C-V* and *DLCP* measurements.

4.2.4 Light Soaking Analysis

CIGS based solar cells exhibit various metastabilities in electrical, and optical characteristics caused by prolonged illumination and voltage bias sweeps [85]. The defects may change state during response to these measurements, thus it is important to follow specific measurement procedures to induce changes in the defects at room temperature [104]. In addition to measuring the defect density, carrier concentration and defect levels, devices were exposed to 100 mWcm^{-2} under AM1.5G for 2 hours (in 1 hour increments) to examine these characteristics. The effect of light soaking mainly results in the enhancement of the $\boldsymbol{FF}$, $\boldsymbol{V_{oc}}$ and $\boldsymbol{PCE}$ with illumination time. For the light soaking analysis, a different set of cells from the same device with Sb were used, compared to the cells used for the *C-V and DLCP* measurements.

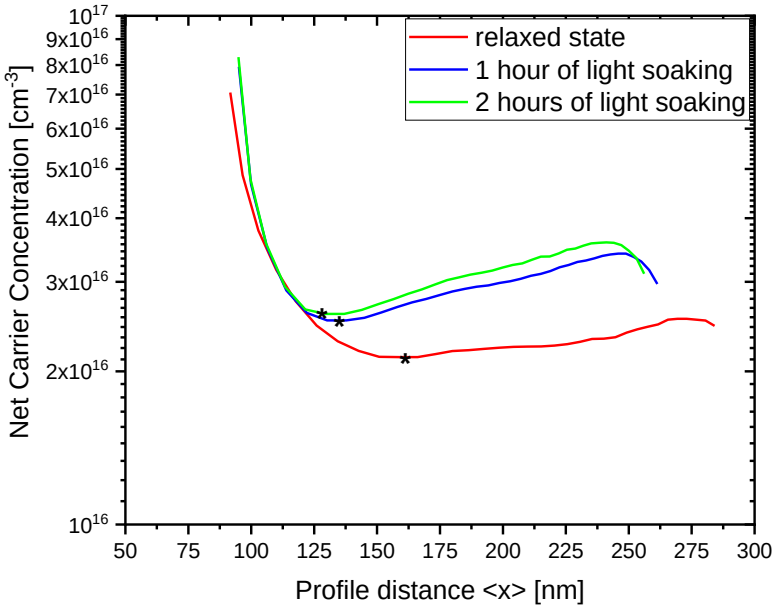

Figure 4.14: Net carrier concentration at room temperature from the *C-V* measurements for the Sb doped device. The net carrier concentration values are extracted at 0 V (marked as `*`).

The devices with Sb were left in the dark at room temperature for 24 hours to ensure a relaxed state (to restore the original state of the device and remove all history of light exposure from previous measurements). Initially, the capacitance measurements were taken before the light soaking. After every 1 hour of light soaking (with no temperature control of the device), the light was turned off and measurements were recorded. 1 hour of light soaking results in a slight increase in net carrier concentration and junction capacitance. The net carrier concentration (Figure 4.14) was increased from roughly 2.13 x 10^{16} cm^{-3} to 2.73 x 10^{16} cm^{-3}, and the junction capacitance (Figure 4.15) from 15.3 $nFcm^{-2}$ to 18.6 $nFcm^{-2}$. After 2 hours of light soaking, no significant increase in net carrier concentration and junction capacitance is observed. The shape of the capacitance curves remained the same. However, the depletion width from the depth profiles at 0 V got smaller with the light soaking. This was expected due to the increase observed in net carrier concentration after light soaking [142]. When the light is turned off and the samples are left in the dark after the measurements, this metastable increase relaxes [98][143], and the junction capacitance and the net carrier concentration reduce to the initial values the next day.

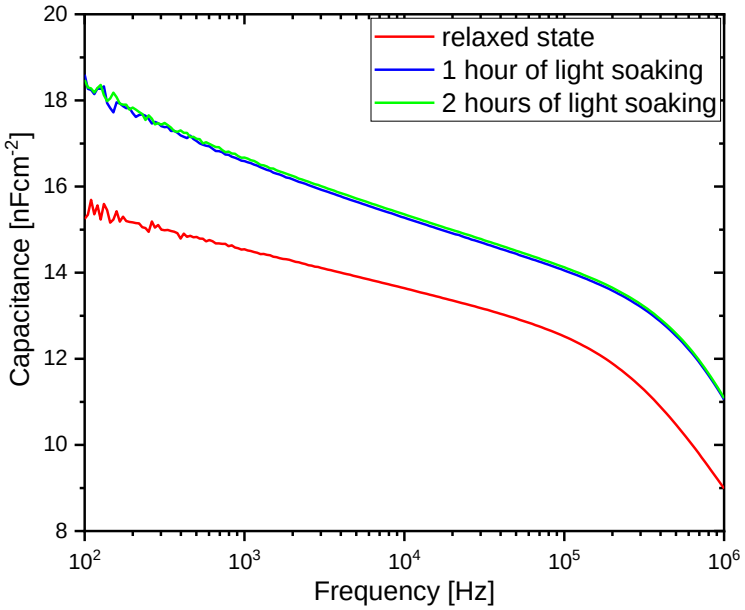

Figure 4.15: Capacitance versus frequency curves for the Sb doped device from the admittance spectroscopy, showing the change in capacitance before and after light soaking at room temperature.

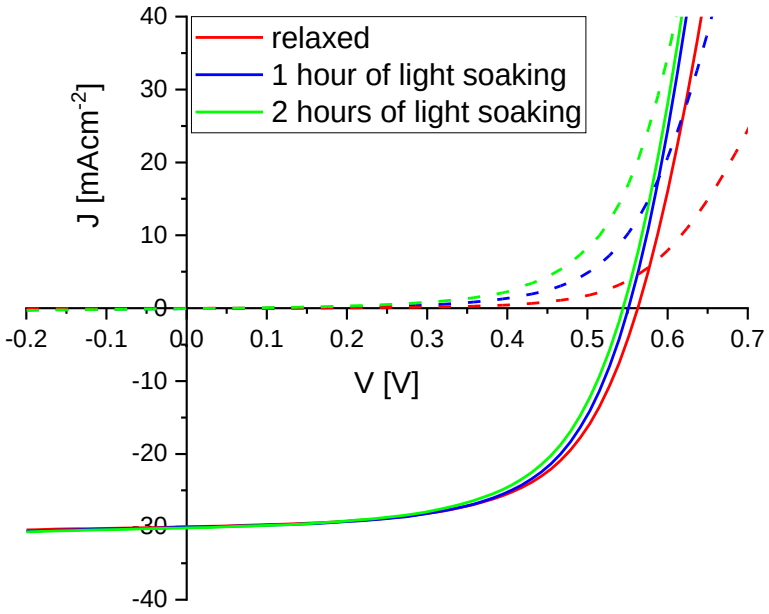

Figure 4.16: Illuminated (solid) and dark (dashed) *J-V* curves for the Sb doped device in the relaxed state, after 1 hour and 2 hours of light soaking.

Table 4.3 summarises the PV parameters extracted from the *J-V* curves in Figure 4.16. After 1 hour of light soaking, an increase in ***FF***, and improved diode characteristics of the dark *J-V* curves have been observed. As the net carrier concentration increases with the light soaking, the depletion region gets smaller, and

both the bulk resistance and contact resistance of the absorber layer decrease. This results in a decrease in the R_s of the device hence an increase in the FF. 2 hours of light soaking leads to deteriorated PV parameters due to sample heating, and no further improvements have been observed. As the V_{oc} is strongly dependent on the cell temperature, after 2 hours of light soaking a significant decrease in V_{oc} is visible. The slight increase observed in J_{sc} is because the field strength becomes stronger throughout the cell with illumination, thus extracting more of the electron-hole pairs. Additionally, the R_{sh} is slightly decreased after light soaking for a yet unknown reason, but not expected to have a significantly effect on the performance of the device.

Condition	V_{oc} [mV]	J_{sc} [mAcm^{-2}]	FF	PCE [%]	R_s [Ω cm^{-2}]	R_{sh} [Ω cm^{-2}]
relaxed	561	29.9	0.611	10.3	13.02	2952.5
1 hour of light soaking	550	30.1	0.614	10.2	10.21	2857.2
2 hours of light soaking	543	30.2	0.602	9.85	9.378	2709.0

Table 4.3 - PV parameters for the device with Sb after light soaking.

Exposure to light source onto the devices after 1 hour is found to improve the net carrier concentration of the absorber layer, the junction capacitance and the FF of the *J-V* characteristics. The metastable increase of the junction shows that the light induced metastability is a bulk phenomena due to the increase of the net carrier concentration observed from the *C-V* measurements. While these improvements are reversible when devices are kept in the dark, the metastable behaviours from the *J-V* and capacitance measurements are less sensitive after 1 hour of light soaking. Thus, no further significant improvements have been observed after 2 hours of light soaking. Lany-Zunger model [144] suggests that the light induced metastable behaviour often seen in CIGS solar cells is related to the consequence of donor-acceptor transition of the Se Cu divacancy complex (V_{Se}-V_{Cu}), which leads to the increased net carrier concentration.

The results from the *C-V* measurements with increased net carrier concentration and junction capacitance, main recombination mechanism which dominates in the bulk, and also the findings from the literature suggest that this metastable behaviour might

originate from the bulk of the CIGS. Although 1 hour of light soaking was beneficial for the overall PV parameters, the presence of metastable defects is a concern.

4.3 Conclusions

Antimony (Sb) was introduced in the absorber layer for hydrazine-free solution-processing CIGS solar cells. The effect of Sb on the device performance and morphology was investigated. Adding Sb enhanced the growth of the grains and the electrical properties of the device, especially J_{sc}. However, the morphology of the absorber layer showed a bilayer structure of large-grain top layer and a fine-grain bottom layer, which is commonly seen in solution-processing CIGS and CZTS solar cells. This bilayer structure agrees well with the trend observed in *EQE* signal with a high collection just above 80%, followed by a gradual decay of the signal at longer wavelengths. A shift in *EQE* spectra in the long wavelength decay with Sb doping is observed. This indicates a decrease in E_g and only the change in In/Ga ratio is able to explain this behaviour. The *EL* image for the best cell showed inhomogeneous patterns of dark and bright regions over the cell area, which might correspond to random crystal CIGS grains seen in *SEM*.

The admittance spectroscopy revealed an N1 step as a result of shallow level defect with an E_A estimated to be 42 meV and a deeper level defect (N2, E_A= 355 meV) for a device without Sb. The reduction of E_A indicates that the N2 defect has been removed by Sb doping. The best cell for the Sb device showed a net carrier concentration of 1.69 x10^{16} cm^{-3} whereas the device without Sb had a higher net carrier concentration of 6.63 x 10^{16} cm^{-3}. This may indicate that adding Sb into the absorber does not necessary dope the layer, possibly passivates the defect since Sb devices showed reduced defect density from the *DLCP* measurements. The depth profiles from *C-V* and *DLCP* showed an unusual shape which might correspond to the interface of the bilayer as depletion width crosses with the voltage sweep. This behaviour is often seen in solution-processed CIGS devices fabricated at Loughborough University.

The effect of light soaking after 1 hour improved the FF, net carrier concentration and the junction capacitance. After 2 hours, there was no significant change in with these parameters. These metastabilities are well established evidence for CIGS based solar cells that have a positive effect on their electrical and optical characteristics. Following the Lany-Zunger model and the results from the *C-V* measurements, the origin of these metastable behaviours induced by light is

believed to be in the bulk and relates to the consequence of donor-acceptor transition of the Se Cu divacancy complex (V_{Se}-V_{Cu}).

From $\boldsymbol{V_{oc}}$ versus $\boldsymbol{T}$ analysis, activation energy of recombination mechanism agrees well with the bandgap of the absorber layer, which indicates that the main recombination mechanism for the device with Sb is in the bulk. Although the Sb doping showed some significant increase in the PV parameters and reduced defects compared to the device without Sb, there are still improvements can be made by optimising the amount of Sb into the precursor solution, or the selenisation conditions, and using different approaches to introduce Sb into the absorber, such as evaporation and spin coating. However, precise control of the amount of Sb in the absorber is necessary in order to achieve the optimum doping level for enhanced device performance, and reduced defects.

Chapter 5

The Effect of Te at the Back-Contact in Mg-Doped ZnO Vacuum-Processed CdTe and CdSeTe/CdTe Thin Film Solar Cells

5.1 Introduction

The most common cadmium telluride (CdTe) solar cells consist of a *p*-*n* junction containing a *p*-doped CdTe layer with an *n*-doped cadmium sulphide (CdS) layer [58]. Using CdS as a window/buffer layer has some major drawbacks. Parasitic absorption of light in the CdS layer of photons with energy above the CdS bandgap (2.45 eV) prevents some of the usable photons reaching to the absorber layer [61]. This causes photogenerated carriers not to be collected and the light absorbed here is wasted, hence limiting the short-circuit current density ($\boldsymbol{J_{sc}}$). To overcome this limitation, many groups have introduced different buffer layers with a high bandgap, such as magnesium-doped zinc oxide (MZO) to replace the CdS layer [145][80]. MZO has a bandgap of $\boldsymbol{E_g} > 3.3$ eV and can transmit a larger fraction of the solar spectrum compared to CdS. One of the advantages of using MZO is its tuneability of the conduction band alignment with CdTe [59]. This can be achieved by changing the concentration of Mg in the film and the ratio of MgO/ZnO, varying the bandgap from MgO (7.8 eV) to ZnO (3.1 eV) depending on the metal ratios [146].

The CdTe has an ideal bandgap (of ~1.5 eV) for solar absorption, but its performance is limited by the presence of high level of defects at the middle of the bandgap [58]. When these defects are present, the doping the in *p*-type CdTe is weak and the hole density is low as a result of relatively deep acceptor levels of Cd

vacancy [147][148]. The change in doping density will affect the open-circuit voltage ($\boldsymbol{V_{oc}}$) and to increase the efficiency further, an increase in $\boldsymbol{V_{oc}}$ is required. There are many other ways to improve the cell performance and reduce the deep level defects inside the cells. One effective way is to modify the cell architecture by introducing new materials into the absorber layer or to the back of the device. Selenium (Se) was introduced to form a CdSeTe (CST) alloy to grade the CdTe bandgap and absorb more light in infrared spectrum [149]. Se passivates the defects in the absorber layer and also helps to improve the band alignment at the buffer/absorber interface. The CST/CdTe devices have shown very long lifetimes and diffusion length in the bulk which resulted in an improved current collection in forward bias [150]. Also, the evaporation of tellurium (Te) layer in combination with Cu (Cu_xTe) has introduced at the back surface of the device to help forming an ohmic contact. This Cu_xTe layer has shown a major impact on improving the fill factor ($\boldsymbol{FF}$), and in reduction of the reverse saturation current [151][152]. Devices with these additional layers and modifications showed an improvement in power conversion efficiency ($\boldsymbol{PCE}$) above 19% [153].

This chapter investigates the behaviour of Te at the back-contact in vacuum processed MZO/CdTe and MZO/CST/CdTe thin film solar cells (TFSCs). Capacitance spectroscopy was used as a tool to identify the defect energy levels and their density, and variations in carrier concentration as a result of CST and Te layers being included. Additionally, the temperature dependent current density-voltage (*JVT)* measurements were studied to locate the recombination centres in the devices. Such information helps understand the limitations of the device performance, as current barriers might appear at low temperatures in *J-V* characteristics.

5.1.1 Device Preparation and Fabrication

This is a comparative study of CdTe devices with different cell architectures. The devices were fabricated at Colorado State University (CSU) using an in-line vacuum deposition system [154] and electrical characterisation was performed at Loughborough University. The details of the system used in the fabrication of CdTe devices are provided elsewhere [154]. The cell architectures for the devices used for this chapter are shown in Figure 5.1.

The device fabrication starts with 100 nm of MZO buffer layer deposited on 3 mm thick 79 x 91 mm fluorine doped tin oxide (FTO) coated soda lime glass substrates (NSG Pilkington, TEC 10) using by RF magnetron sputtering [145]. The CST film ([Se]/[Se+Te] = 0.4) of ~1.5- - osited by closed space sublimation (CSS) onto the MZO layer followed by 600 seconds of $CdCl_2$ passivation at 430°C. The CST layer was sublimated at 3 different temperatures (standard, low and high) to investigate the effect on the device performance. The devices with low temperature deposition are referred as LTD and high deposition HTD, respectively. The vapour source for the CdTe sublimation was heated to 555°C while the substrate heater was maintained at 500°C. After the $CdCl_2$ treatment, the films were treated with CuCl for 110 seconds by sublimation at 140°C followed by 220 seconds of annealing at 220°C. A 30 nm thick layer of tellurium was deposited by evaporation to complete the back-contact. A back electrode was

paint layer. The details of the fabrication of CST/CdTe devices are provided elsewhere [75].

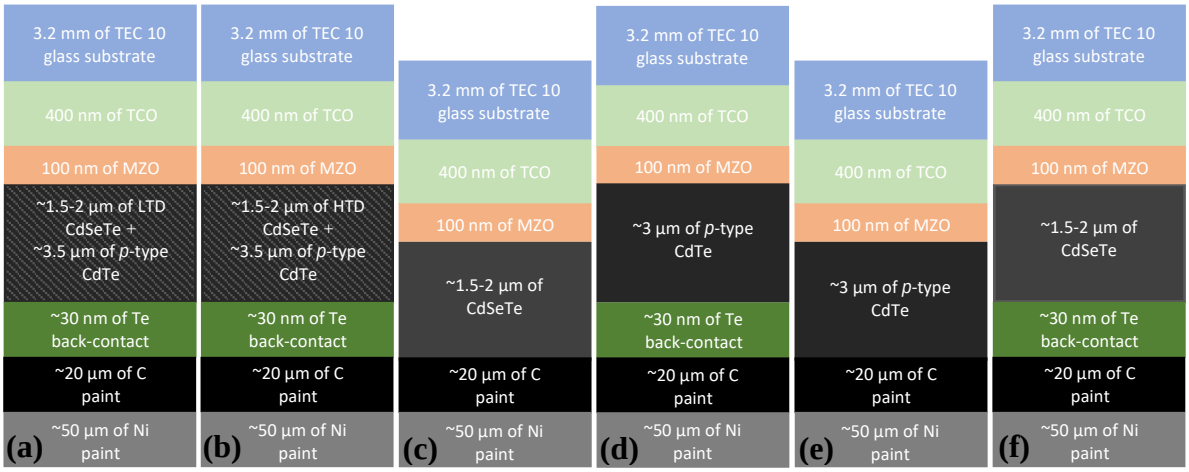

Figure 5.1: Schematic of (a) `LTD CST/CdTe with Te`, (b) `HTD CST/CdTe with Te, (c) `CST/CdTe without Te`, (d) `CdTe with Te`, (e) `CdTe without Te`, and (f) `CST with Te` devices (not to scale).

5.2 Results

5.2.1 *J-V* and *EQE* Analysis

The *J-V* characteristics of the devices were taken at room temperature (Figure 5.2) under 100 mWcm^{-2}. Table 5.1 summarises the device parameters from *J-V* curves which were measured at Loughborough University. Each device has 25 cells with a cell area of ~0.66 cm^2 and the best performing cells for each device were used for further analysis.

	V_{oc} [mV]	J_{sc} [mAcm^{-2}]	FF	PCE [%]	A	R_s [Ý c^{-2}]	R_{sh} [Ý c^{-2}]
LTD CST/CdTe with Te	824	25.31	0.667	13.9	2.166	9.097	348443
HTD CST/CdTe with Te	835	25.71	0.693	14.9	1.731	9.447	8693
CST/CdTe without Te	831	12.87	0.215	2.3	-	-	-
CdTe with Te	852	22.35	0.622	11.9	1.075	8.121	494
CdTe without Te	819	20.61	0.598	10.1	3.972	8.896	461
CST with Te	570	18.00	0.212	2.2	-	-	-

Table 5.1 – Summary of the device parameters of the best performing cells for each device, where *A* is the diode ideality factor (LTD and HTD refer to low and high temperature deposition of CST, respectively).

The CST/CdTe with Te for devices with LTD and HTD showed high $PCEs$ around ~14-15% with high FF and increased J_{sc}. All the devices had V_{oc} above ~800 mV, except the `CST/CdTe without Te` device. The low FF observed with the `CST/CdTe without Te` device is due to a large R_s and a low R_{sh}. Having Te at the back of the device has shown improvements on the PV parameters and the *J-V* characteristics. The `CST with Te` device has a significant current barrier which results an `*S*` shaped *J-V* curve. This is commonly refer as a `*kink*` type anomaly in the illuminated *J-V* curves and occurs in the third or fourth quadrant of the *J-V* characteristics [18]. This `*S*` shaped behaviour can be due to a conduction band offset (CBO) or a presence of a significant current barrier.

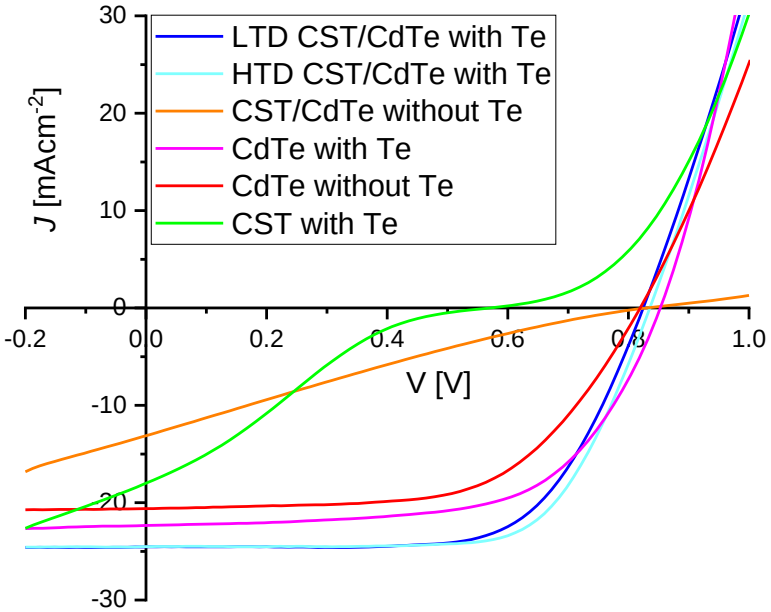

Figure 5.2: Illuminated *J-V* curves (100 mWcm^{-2}) at room temperature, AM1.5G.

The *EQE* spectra for the best cells of the devices are shown in Figure 5.3. The CdTe with/without Te and HTD/LTD CST/CdTe devices results in a high current collection just above 80% in the range of 400 to 900 nm and a gradual decay of the *EQE* at longer wavelengths. Whilst the `CST with Te` device results in a low collection just above 55% in the range of 350 to 825 nm and a gradual decay of the *EQE* at longer wavelengths. This is due to a significant photocurrent barrier which limits the collection, resulting in an `*S*` shaped behaviour in the *J-V* characteristics and consequent reduction in $\boldsymbol{J_{sc}}$. The `CST/CdTe without Te` device results in a poor collection just above 25% in the range of 400 to 850 nm. This is due to having a non-linear diode behaviour seen in Figure 5.2 from the *J-V* characteristics. For the `CdTe with Te` device, the current collection is more efficient towards the back compared to the `CdTe without Te` device, which shows a decay of current collection from 625 nm to longer wavelengths. The sharp decrease below 350 nm is due to the absorption in the MZO layer. The $\boldsymbol{J_{sc}}$ from the *EQE* data for all the devices are in closed agreement with $\boldsymbol{J_{sc}}$ from the *J-V* measurements shown in Table 5.1. There is a shift in the long wavelength decay of the *EQE*, corresponding to the absorber bandgap ($\boldsymbol{E_g}$) variation with the devices which had a CST layer compared to without. This indicates a decrease in $\boldsymbol{E_g}$. The $\boldsymbol{E_g}$ for each device is extracted from the peak of the derivative of the long wavelength slope in the *EQE* data, ranging between $\boldsymbol{E_g = 1.42 - 1.49}$ eV which are expected from CST/CdTe devices [75].

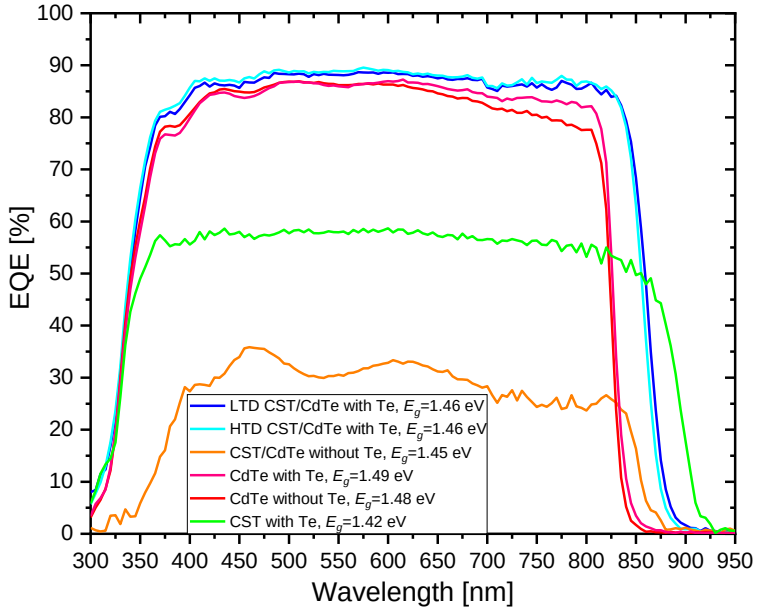

Figure 5.3: The *EQE* spectra of the best cells for all the devices. The absorber bandgaps (E_g) are extracted from the peak of the derivative of the long wavelength slope in the *EQE* data.

In addition to room temperature *J-V* measurements, temperature dependent *J-V* measurements (*JVT)* were carried out in an evacuated closed-cycle helium cryostat for temperatures between 315 K and 115 K with 10 K steps. Figure 5.4 shows the *JVT* curves for all the devices. All measurements were carried out at 50 mWcm^{-2} with a halogen light source (details are provided in Chapter 3). There is a strong temperature dependence of the J_{sc} with `LTD CST/CdTe with Te` device which may imply a photocurrent barrier and it becomes less pronounced with `HTD CST/CdTe with Te` device (Figure 5.4 (a) and (b)). This suggests that the high temperature deposition of CST improves this barrier. In case of the CdTe devices, a significant improvement can be seen with the R_s and R_{sh} parameters at low temperatures when Te is added at the back of the device (Figure 5.1 (d) and (e)). The *J-V* characteristics at different temperatures exhibit crossover effect, where the dark and illuminated *J-V* curves cross each other in all devices. This crossover may be caused by photoconductive effects in the buffer layer or a light-dependent barrier, and it is a common phenomenon seen in the TFSCs [85]. The `CST/CdTe without Te` and `CST with Te` devices show a poor performance at different temperatures compared to the other devices and similar *J-V* characteristics to the room temperature measurements at 100 mWcm^{-2} (Figure 5.2).

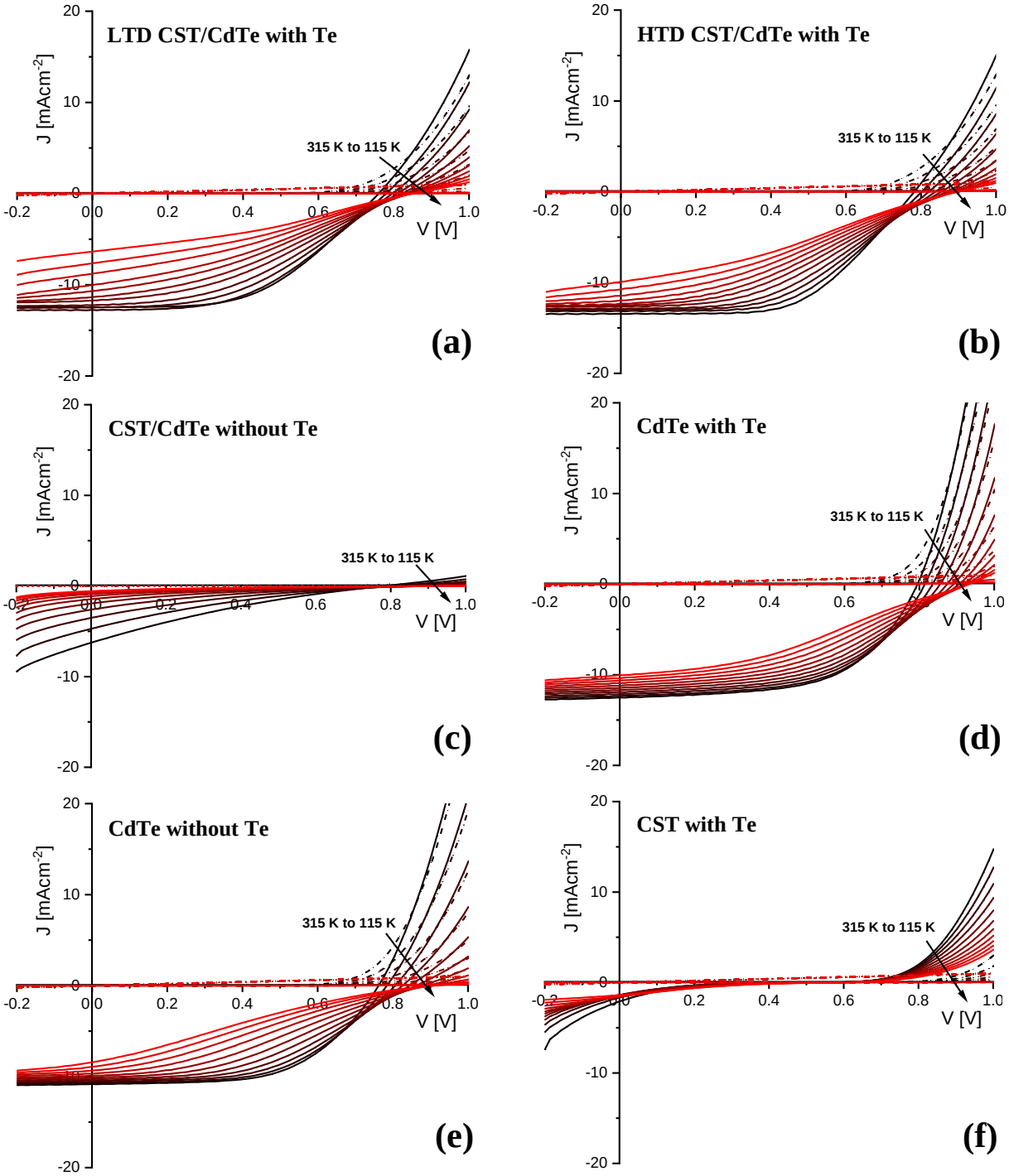

Figure 5.4: Dark and illuminated *J-V* curves (at 50 mWcm^{-2}) are displayed for temperatures between 115 K and 315 K (in 10 K steps) for the devices; (a) `LTD CST/CdTe with Te`, (b) `HTD CST/CdTe with Te`, (c) `CST/CdTe without Te`, (d) `CdTe with Te`, (e) `CdTe without Te`, and (f) `CST with Te`.

The *JVT* curves from Figure 5.4 are used in determination of the recombination mechanisms dominating in the cell. This is done by extracting the activation energy ($\boldsymbol{E_a}$) of the recombination from the intercept of $\boldsymbol{V_{oc}(T)}$ at $\boldsymbol{T}$ = 0 K (Figure 5.5). This technique has been used as a qualitative assessment of where the recombination

centres occur, to identify what the major electrical losses are in the cell which limits the performance of the device [78]. From the literature, if E_a and E_g are consistent or $E_a > E_g$, the recombination mechanism dominates in the bulk. Whereas, if $E_a < E_g$, then the recombination mechanism dominates at the buffer/absorber interface [91]. Table 5.2 summarises the E_a of the recombination mechanisms for each of the devices along with the E_g which are extracted from the *EQE* spectra in Figure 5.3. From $V_{oc}(T)$ analysis, the recombination mechanism for all the devices dominates at/close to the interface with different E_a values below the E_g in all cases.

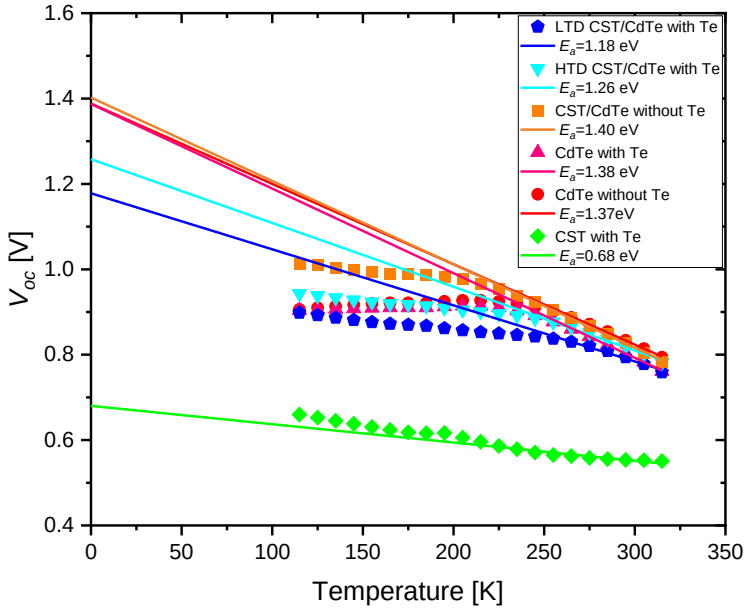

Figure 5.5: Temperature dependence of V_{oc} data, determined by the illuminated *J-V* curves from the Figure 5.4, yielding activation energy for recombination mechanisms for each device.

The CdTe devices with and without Te showed similar E_a values, suggesting that the addition of Te layer at the back does not change the location of the dominant recombination centre. However, it slightly reduces the interface recombination, leading to a smaller barrier height [155]. This reduction of interface recombination is also observed with the HTD and LTD CST/CdTe devices, where `HTD CST/CdTe with Te` device leads to an increased E_a. The `CST with Te` device has the lowest E_a value, suggesting that the recombination mechanism heavily dominates at the interface with a very large barrier height. This can be related to the `*S*` shaped behaviour seen in the *J-V* characteristics, which showed a significant current loss in

forward bias. The `CST/CdTe without Te` device has the highest E_a which can be related to the non-diode behaviour seen in the *J-V* characteristics.

	E_a [eV]	E_g [eV]	Recombination dominates
LTD CST/CdTe with Te	1.18	1.46	at the interface
HTD CST/CdTe with Te	1.26	1.46	at the interface
CST/CdTe without Te	1.40	1.45	at the interface
CdTe with Te	1.38	1.49	at the interface
CdTe without Te	1.37	1.48	at the interface
CST with Te	0.68	1.42	at the interface

Table 5.2 – Summary of the E_a from $V_{oc}(T)$ and E_g from EQE analysis.

5.2.2 Admittance Spectroscopy

Figure 5.7-5.12 show the admittance and conductance spectra under equilibrium conditions (in the dark, at 0 V) for the devices between 315 K and 45 K. Prior to cooling, the samples were kept in the dark for one hour to ensure a relaxed state. Ideally the frequency range of the measurement would extend to the lowest possible values to allow measurements of defect states as low below the conduction band minimum (CBM) as possible, and extend to highest values of frequency possible to allow the best separation of the carrier concentration from the deep level defect density [156] [157]. For this reason, the measurements were limited from 100 Hz to 100 kHz.

capacitance and conductance spectra for each device. From the literature, these two defects correspond to different response (either bulk or interface) with different activation energies. However, there is a controversial discussion in literature about the origin of these admittance steps. The N1 step has been assigned to a shallow defect at the surface of the absorber layer (i.e. at the buffer/absorber interface) and has typical activation energies, E_A, between 40 meV and 200 meV depending on the reference [109][104]. Moreover, this admittance step occurs when a defect crosses the Fermi level at or close to the interface [156]. For the N2 step, the defects are commonly located in the bulk of the absorber layer with activation energies about

200 meV or above [114]. The N2 defect is considered as a deeper defect and this admittance step occurs when a defect crosses the Fermi level within the *p*-side of the space charge region (SCR) [156]. Additionally, the presence of a Schottky barrier may also contribute to an admittance response, and it is sometimes hard to distinguish if the response is from a barrier or a defect state [157]. A barrier at the back-contact affects the *J*-*V* characteristics of the device by limiting the current in forward bias which is also known as rollover effect. From the admittance spectra at the temperatures where N1/N2 steps occur, there is no visible rollover effect seen on the *J*-*V* curves. This may suggest that the admittance response is from a defect state rather than a barrier.

The activation energies of the admittance steps were obtained from an Arrhenius plot (Figure 5.6) using the maxima of the conductance spectra (Figure 5.7-5.12), Table 5.3 summarises the results of the defects with assigned locations according to literature. Adding Te at the back of the device removes either the N1 or N2 defects depending on the device configuration. Introducing Te to the CST/CdTe devices has removed the shallow defect. Although the location of the N1 step from the literature has often been assigned to defects at the buffer/absorber interface, the interpretation of the N1 step in this case may imply that it is located at the absorber/back-contact interface, since Te is added at the back of the device. In the case of CdTe devices, Te has removed the deep level defect and left with only shallow defects remaining. Te might be passivating back surface defects, helping to reduce the interface recombination and enhancement of $\boldsymbol{V_{oc}}$ which were observed from the $\boldsymbol{V_{oc}(T)}$ analysis and room temperature *J*-*V* measurements. The `CST with Te` device has revealed a shallow defect with $\boldsymbol{E_A}$ of 20 meV, which corresponds to the N1 defect. Additionally, an increase in junction capacitance at low temperature was observed for all of the devices, except the `CST with Te` and `CST/CdTe without Te` devices. The reason for increased junction capacitance is not fully understood and will require further investigation.

	Defect Type	*Possible Defect Locations*	E_A *[meV]*
LTD CST/CdTe with Te	N2	in the bulk	279
HTD CST/CdTe with Te	N2	in the bulk	272
CST/CdTe without Te	N2 & N1	in the bulk & at the interface	241 & 51
CdTe with Te	N1	at the interface	33 & 39
CdTe without Te	N2 & N1	in the bulk & at the interface	24 & 236 & 102 & 24
CST with Te	N1	at the interface	20

Table 5.3 – Summary of the defects and activation energies, E_A.

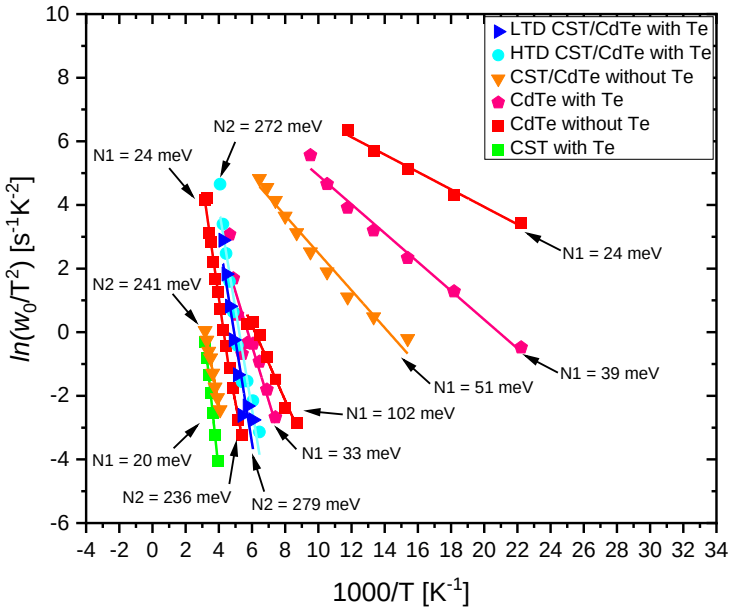

Figure 5.6: Arrhenius plot of the inflection points derived from conductance spectra in Figures 5.7-5.12 for the `CdTe with Te` (pink hexagons), `CdTe without Te` (red squares), `CST with Te` (green squares), `LTD CST/CdTe with Te` (blue triangles), `HTD CST/CdTe with Te` (turquoise circles), and `CST/CdTe without Te` (orange triangles).

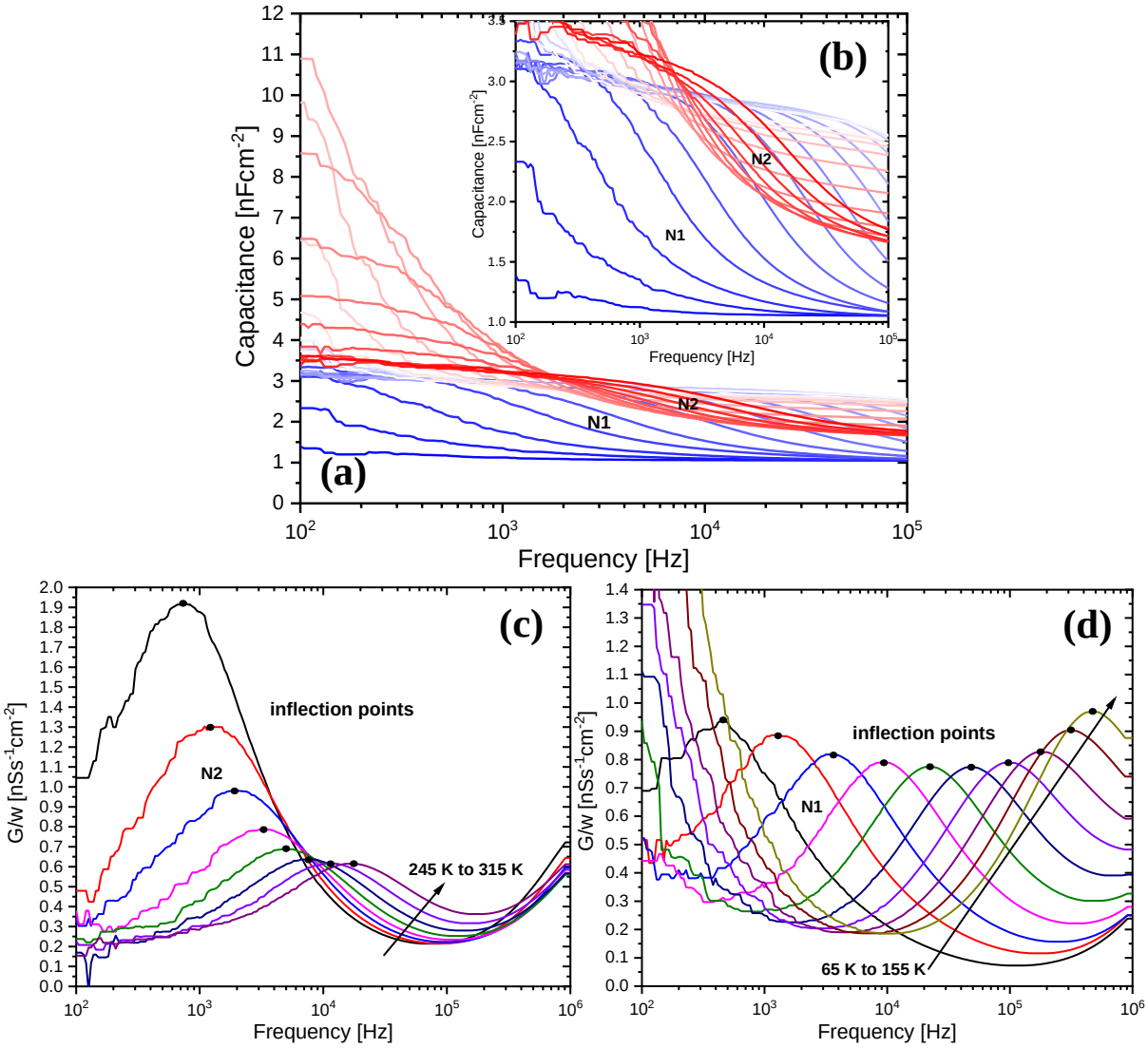

Figure 5.7: (a) Admittance spectra in the dark at 0 V between 315 and 45 K for the `CST/CdTe without Te` device. An admittance step is visible between 245 K and 315 K which is marked as "N2" and another step between 65 K and 155 K which is marked as "N1". For clarity, a zoomed-in spectra with less curves are displayed in (b). (c) Conductance spectra between 245 K and 315 K for the N2 step and (d) between 65 K and 155 K for the N1 step are shown in (c) and (d). Inflection points are marked in black at the maxima of each curve.

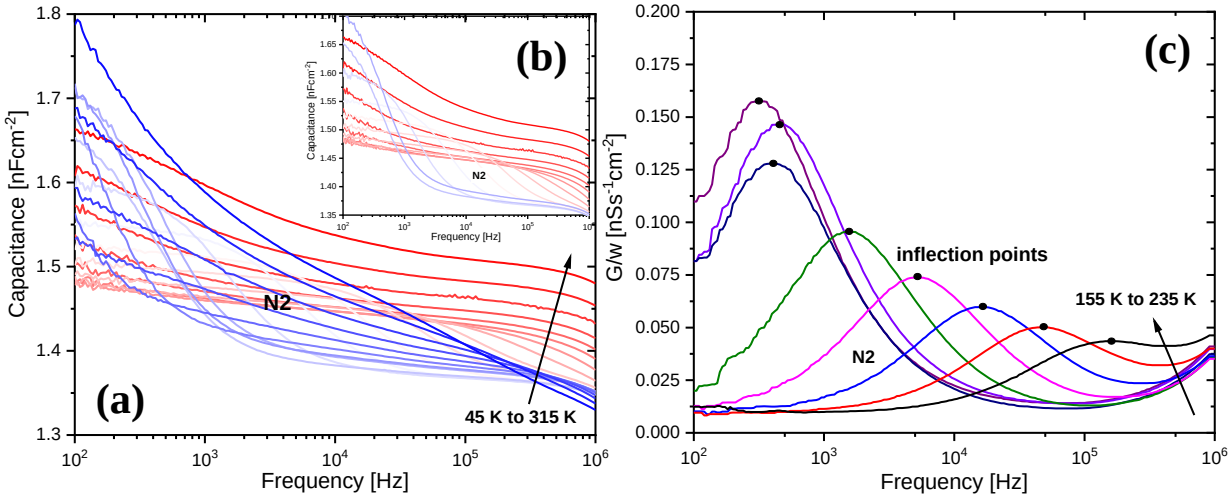

Figure 5.8: (a) Admittance spectra in the dark at 0 V between 315 K and 45 K for the `LTD CST/CdTe with Te` device. An admittance step is visible between 155 K and 235 K which is marked as "N2". For clarity, a zoomed-in spectra with less curves are displayed in (b). Conductance spectra between 155 K and 235 K for the N2 step is shown in (c). Inflection points are marked in black at the maxima of each curve.

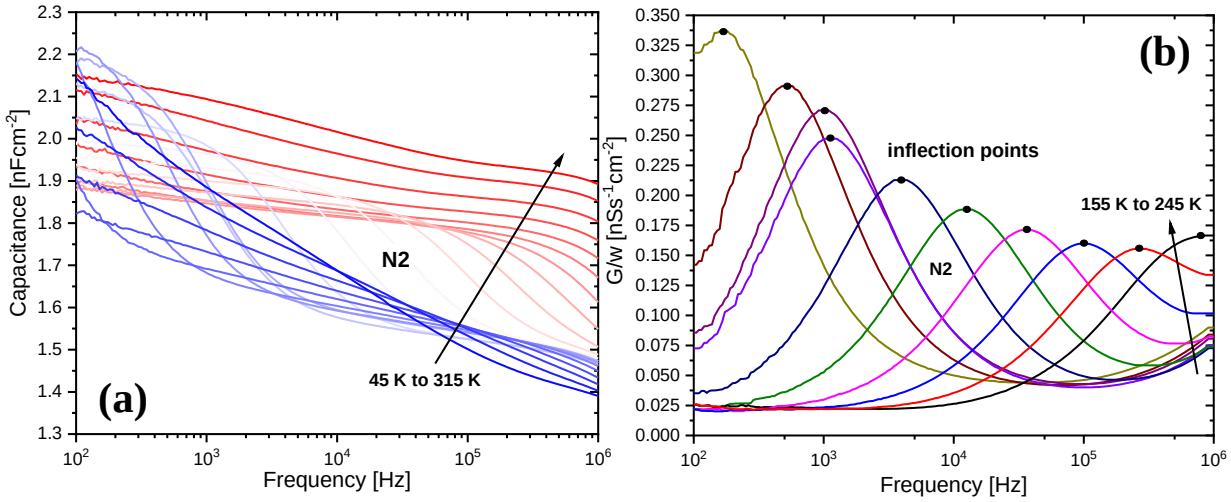

Figure 5.9: (a) Admittance spectra in the dark at 0 V between 315 K and 45 K for the `HTD CST/CdTe with Te` device. An admittance step is visible between 155 K and 245 K which is marked as "N2". Conductance spectra between 155 K and 245 K for the N2 step is shown in (b). Inflection points are marked in black at the maxima of each curve.

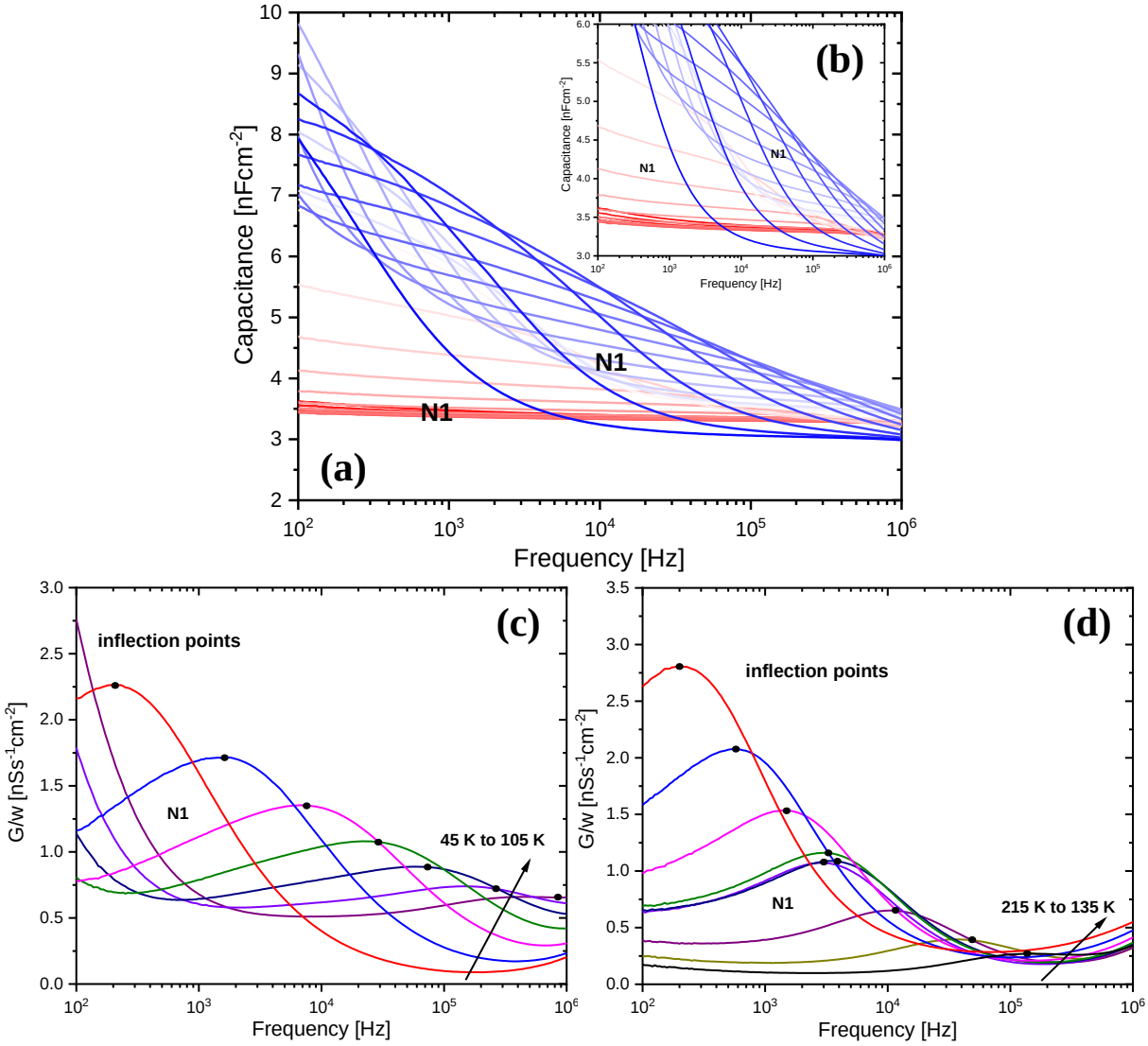

Figure 5.10: (a) Admittance spectra in the dark at 0 V between 315 and 45 K for the ` CdTe without Te` device. Admittance steps are visible between 185 K and 205 K which is marked as "N2", another step 65 K and 155 K which is marked as "N1". For clarity, (b) a zoomed-in spectra with less curves are displayed. (c) Conductance spectra between 245 and 315 K for the N2 step and (d) between 65 K and 155 K for the N1 step. Inflection points are marked in black at the maxima of each curve.

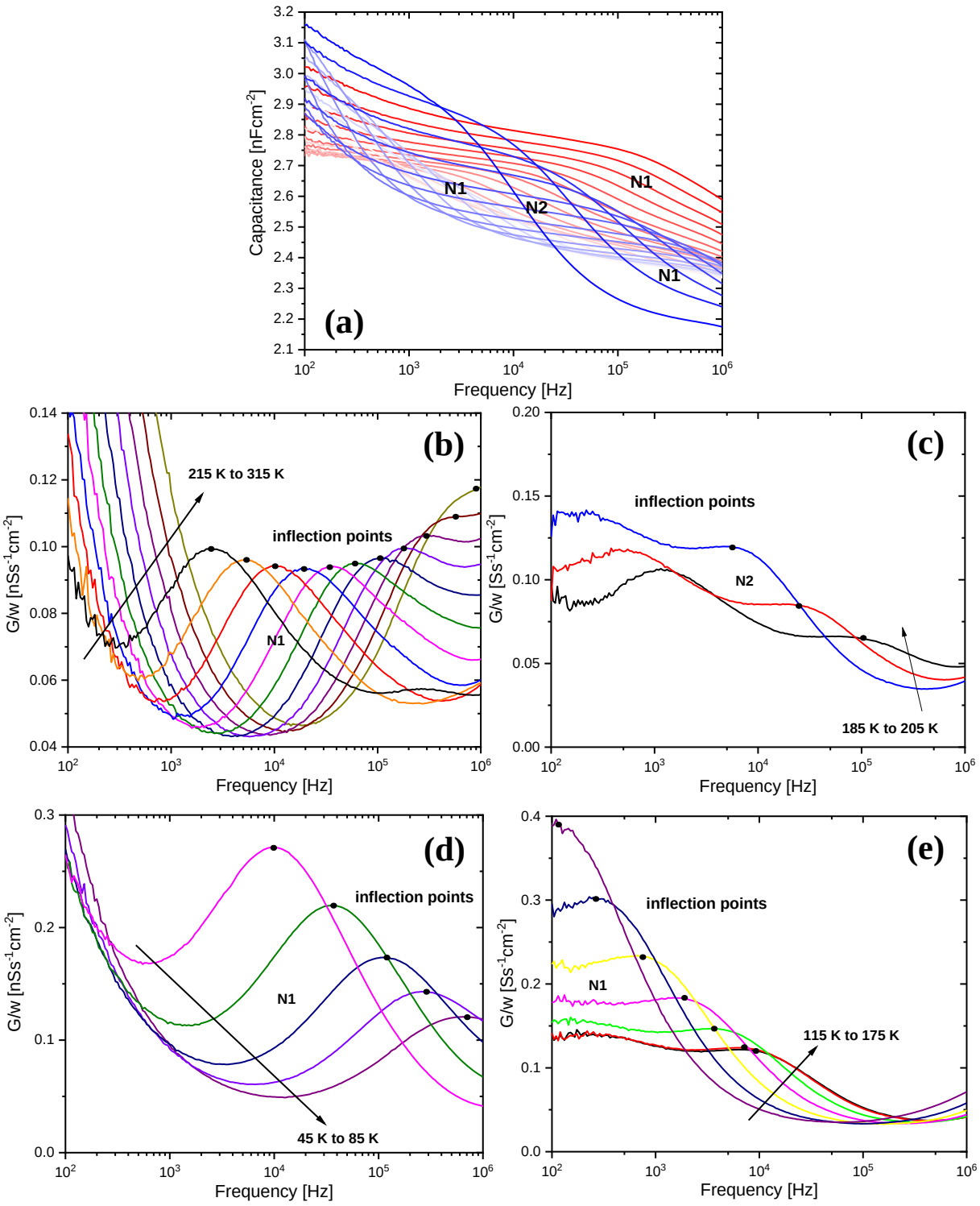

Figure 5.11: (a) a) Admittance spectra in the dark at 0 V between 315 and 45 K for the `CdTe with Te` device. An admittance step is visible between 45 K and 105 K which is marked as "N1" and another step between 135 K and 215 K which is marked as "N1". For clarity, a zoomed-in spectra with less curves are displayed in (b). (c) Conductance spectra between 45 K and 105 K for the N1 step and (d) between 135 K and 215 K for the N1 step are shown in (c) and (d), respectively. Inflection points are marked in black at the maxima of each curve.

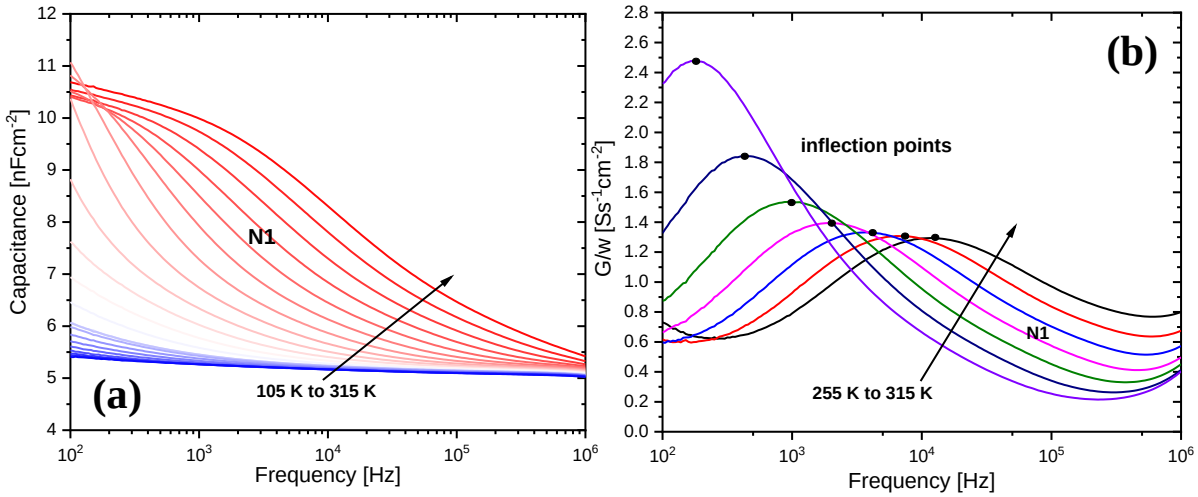

Figure 5.12: (a) Admittance spectra in the dark at 0 V between 105 and 315 K for the `CST with Te` device. An admittance step is visible between 315 K and 255 K which is marked as "N1". Conductance spectra between 315 and 105 K for the N1 step is shown in (b). Inflection points are marked in black at the maxima of each curve.

5.2.3 Capacitance-Voltage Analysis

The depth profiles of the net carrier concentration were investigated using capacitance-voltage (*C-V)* profiling and drive level capacitance profiling (*DLCP*) techniques. *C-V* measurements were carried out in the dark and at room temperature. Initially, the dc bias voltage was varied in the range of 1 to -1 V and then the negative values of net carrier concentration have been removed from the depth profiles. The oscillating voltage was 10 mV at a frequency of 100 kHz. *DLCP* measurements were carried out in a similar way to *C-V* measurements with varied oscillating voltage in the range of 10 mV to 210 mV. This method gives a more accurate determination of carrier concentration. Likewise, *C-V* profiling can lead to incorrect determination due to the presence of deep defects or interface defects. The defect density was measured by *DLCP* technique under equilibrium conditions at room temperature. This measurement involves a frequency sweep with a fixed bias voltage where the capacitance data were recorded at 21 drive levels (oscillating voltage) spaced by intervals of 10 mV over a range of 10 mV to 210 mV. Moreover, the total concentration from the sum of the $\boldsymbol{N_{defect}}$ and $\boldsymbol{N_{DLCP}}$ should approximately be equivalent to the net carrier concentration from the *C-V* measurements, $\boldsymbol{N_{CV}}$ (i.e., $\boldsymbol{N_{DLCP} + N_{defect} \approx N_{CV}}$).

Figure 5.13 shows the depth profiles for both *C-V* and *DLCP* measurements for all the devices. The depth profiles exhibit very similar shape for all the devices, except the `CST/CdTe without Te` device. This might be due to a higher deep level defect density compared to other devices, hence affecting the measurement. The depth profile for *C-V* does not extend all the way up to ~4550 nm unlike *DLCP* for the same bias range (in Figure 5.13 (c)). Thus, when the depletion width extends with applied bias the defects might be getting filled up and the profile is limited to 3250 nm. Another possible explanation for the created profile could be an effect of the admittance steps (N1 and N2). If a bias is large enough, the depth profile extends all the way into the absorber layer and can be used as an approximation of the thickness of the absorber layer. When the depth profile reaches to the edge of the layer, the measurement goes to a negative value (excluded from any of the depth profiles). The thickness of the CST/CdTe and CdTe layers deposited for these devices was ~2- thickness estimation from the depth profiles shows a range of 3.6-4.2 close to thicknesses reported in Figure 5.1.

In addition to the defect density measurements, the built-in potential ($\boldsymbol{V_{bi}}$) of the junction at room temperature and the depletion width ($\boldsymbol{w_d}$) at 0 V were estimated from the *C-V* measurements. The $\boldsymbol{V_{bi}}$ is an important parameter that decides the behaviour of a solar cell and it affects the $\boldsymbol{V_{oc}}$ thus, the efficiency of the device. The difference in electric field strength between the *p-n* junction determines the $\boldsymbol{V_{bi}}$ and from the intercept of a Mott-Schottky plot ($\boldsymbol{1/C^2}$ versus $\boldsymbol{V}$) in forward bias gives an estimation of $\boldsymbol{V_{bi}}$. In case of $\boldsymbol{V_{bi} < V_{oc}}$, the *J-V* characteristics maintained the exponential nature of a diode characteristics. However, in case of $\boldsymbol{V_{bi} > V_{oc}}$ or $\boldsymbol{V_{bi}}$ close to the $\boldsymbol{V_{oc}}$, device might lead to nonlinear *J-V* characteristics as $\boldsymbol{V_{bi}}$ becomes larger [25][158]. Comparing estimated $\boldsymbol{V_{bi}}$ with measured $\boldsymbol{V_{oc}}$, the `CST with Te` and `CST\CdTe without Te` devices had a higher $\boldsymbol{V_{bi}}$ estimation, suggesting a non-linear *J-V* characteristic and this behaviour can be also seen in Figure 5.2 from the *J-V* curves.

The LTD/HTD CST/CdTe with Te and CdTe with/without Te devices had net carrier concentration in the order magnitude of 10^{14} cm^{-3}, whereas the `CST/CdTe without Te` device had net carrier concentration in the order magnitude of 10^{13} cm^{-3}. These values are in agreement with the data in literature for CdTe devices, where the carrier concentration is around 10^{14} cm^{-3} [70].

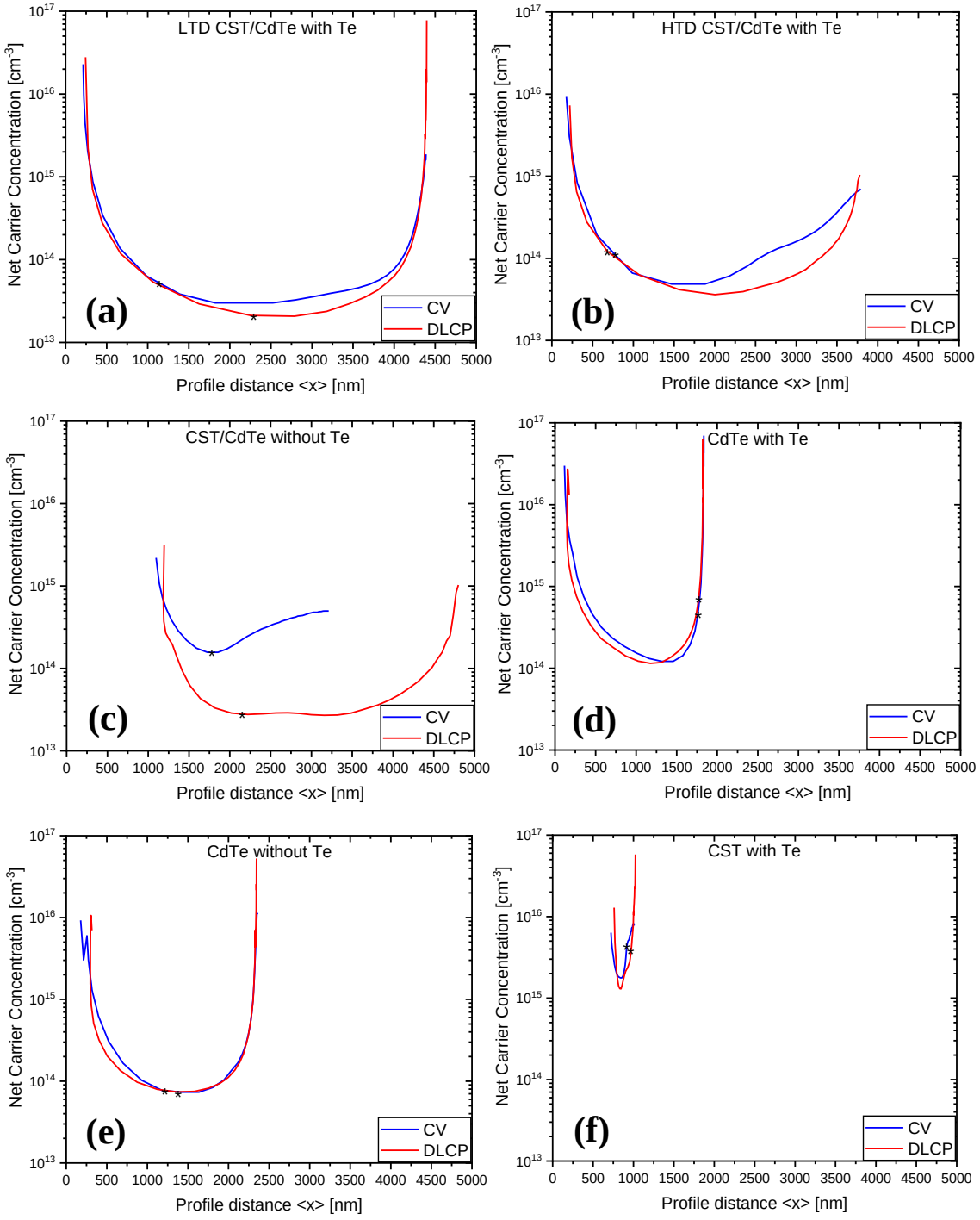

Figure 5.13: Comparisons between *DLCP* and *C-V* depth profiles of the samples, at room temperature. The net carrier concentration values are extracted at 0 V (marked as `*`).

The reason for having a low net carrier concentration, and a significant difference in net carrier concentration between *C-V* and *DLCP* depth profiles for the `CST/CdTe without Te` device might be due to having a high defect density, and the presence of deep defects in the bulk of the absorber layer. Te passivates the shallow defects

resulting in a lower defect density for the LTD and HTD CST/CdTe with Te devices. Whereas with the CdTe devices, Te at the back showed no significant changes in defect density. Nonetheless, the device with Te showed a lower net carrier concentration compared to the device without Te. The `CST with Te` device had the highest net carrier concentration, indicating a narrower depletion width compared to other devices. Although the net carrier concentration was high, the device has the lowest efficiency as a result of high defect density.

	N_{DLCP} [cm^{-3}]	$N_{defects}$ [cm^{-3}]	N_{CV} [cm^{-3}]	w_d [nm]	V_{bi} [mV]	V_{oc} [mV]
LTD CST/CdTe with Te	1.42 x10^{14}	1.69 x10^{13}	5.65 x10^{13}	1207	610	824
HTD CST/CdTe with Te	1.36 x10^{14}	9.55 x10^{12}	1.18 x10^{14}	844	623	835
CST/CdTe without Te	2.72 x10^{13}	1.03 x10^{14}	1.96 x10^{14}	762	842	831
CdTe with Te	7.58 x10^{14}	1.34 x10^{15}	4.49 x10^{14}	408	555	852
CdTe without Te	8.18 x10^{14}	1.33 x10^{15}	7.05 x10^{14}	369	712	819
CST with Te	3.41 x10^{15}	2.06 x10^{15}	4.42 x10^{15}	226	1677	570

Table 5.4 – Summary of the *C-V* and *DLCP* measurements for the devices at room temperature.

5.3 Conclusions

Te and CST layers were introduced into the MZO/CdTe TFSCs. The effect of these layers on the device performance was investigated by using capacitance spectroscopy and temperature dependent *J-V* measurements. The CST/CdTe devices with Te showed a major improvement on the $\boldsymbol{FF}$ and resulted no rollover in the fourth quadrant on the *J-V* curves. This improvement is mainly due to an increased $\boldsymbol{R_s}$. The HTD and LTD CST/CdTe devices with Te showed $\boldsymbol{PCEs}$ above 14%. Adding a CST layer has enhanced the current collection in devices with and without Te at the back-contact. The `CST with Te` device resulted in a `*S*` *J-V* curve, which might be a result of higher interface recombination or a conduction band offset. The `CST/CdTe without Te` device showed a really low $\boldsymbol{FF}$ with high $\boldsymbol{R_s}$ and low $\boldsymbol{R_{sh}}$, resulted a non-diode behaviour in *J-V* characteristics. The $\boldsymbol{V_{oc}(T)}$ analysis revealed recombination mechanisms which dominate at/close to the interface for all the devices with different $\boldsymbol{E_a}$ values. Adding Te has slightly improved the interface recombination by passivating the back surface defects which resulted in better *J-V* characteristics and enhanced $\boldsymbol{V_{oc}}$. Additionally, `HTD CST/CdTe with Te` device showed a higher $\boldsymbol{E_a}$ compared to `LTD CST/CdTe with Te` device, thus the interface recombination has improved with the high temperature deposition of CST, possibly passivating the defects. Moreover, there is no any sign of rollover effect at any temperature for all the devices, however *J-V* curves exhibit strong illuminated-dark crossovers and it is a common phenomenon seen in the TFSCs due to photoconductive effects in the buffer layer or a light-dependent barrier at the back-contact.

The N1 and N2 admittance steps with different activation energies (shallow or deeper) were detected using *AS* under equilibrium conditions. The activation energies of the admittance steps were obtained from an Arrhenius plot for the inflection points which were obtained from the conductance spectra. Te has removed either the N1 or N2 defects depending on the if the devices had a CST layer. In the case of CST/CdTe devices, adding Te has removed the shallow defect i.e., N1 step. The defect might be located at the absorber/back-contact interface, since Te is added at the back of the device. In addition, the CST/CdTe with Te devices resulted in a low defect density from the *DLCP* measurements compared to the device without Te. Thus, Te might be passivating some of these defects seen in *AS*

measurements. In the case of CdTe devices, adding Te did not have any significant changes in defect density. However, removed the deep level defect and left only with shallow defects. All the devices showed an `*U*` shaped depth profiles from both *C-V* and *DLCP* measurements with net carrier concentration ranging 10^{13} and 10^{14} cm^{-3}. However, the `CST/CdTe without Te` device showed a higher net carrier concentration with smaller depth profile from the *C-V* measurements compared to *DLCP.* This difference could be due to the presence of deep level defects, affecting the measurements since *C-V* technique is sensitive to these defects.

Chapter 6

Metastable Behaviour of Mg-Doped ZnO Vacuum-Processed CdSeTe/CdTe Thin Film Solar Cells

6.1 Introduction

Recent research has focused on introducing new materials for the buffer and absorber layers in CdTe PV devices, which have mainly resulted in significant improvements in the device $\boldsymbol{J_{sc}}$ and power conversion efficiency ($\boldsymbol{PCE}$). The most significant improvements have been developed by introducing magnesium doped zinc oxide (MZO) as a highly transparent buffer layer, and as well as the introduction of Se into the absorber to form a CdSeTe (CST) layer with a reduced bandgap [75]. The MZO offers more flexibility in adjusting the buffer/CdTe interface such as the band alignment by changing the concentration of Mg in the film, which leads to a change in the bandgap and the conduction band level of the buffer. These adjustments contribute towards improved $\boldsymbol{PCE}$ and also have shown to exhibit very long lifetimes [159]. Incorporation of Se diffuses into the absorber, inducing bandgap grading which may increase the carrier lifetime and thus open circuit voltage [160]. However, modifying the cell architecture introduces more complexity in understanding the factors that limit performance, stability issues and transient metastable behaviour. Furthermore, for consistent comparisons between different laboratories of different PV materials, it is advisable to have a common preconditioning procedure to follow, in order to measure accurately and interpret reliable performance data.

This chapter aims to explain the metastable behaviour of PV parameters seen in MZO/CST/CdTe devices measured in different laboratories under different ambient conditions. It also reports on different preconditioning approaches that have been used to attempt at recovering the performance of highly efficient devices. Approaches including light soaking, annealing studies under different temperature and atmospheric ambient conditions, and various cooling procedures. Another possible reason for this discrepancy in performance might be due to degradation of the MZO layer, which is sensitive to the presence of atmospheric humidity [161]. From temperature dependent *J-V* and capacitance measurements, recombination centres and defect levels are found located at the interface. These defects can contribute to metastable behaviour and the associated degradation observed in the devices. A series of Hall effect measurements have been performed on the MZO films before and after preconditioning to investigate the changes in conductivity and carrier concentration using a Parallel Dipole Line (PDL) Hall system [17]. In addition, Ga doped MZO (GMZO) films, where Ga doping in general is considered to be more moisture resistant [162] and provides high conductivity [163] is presented in this chapter.

6.1.1 Device Preparation and Fabrication

The CST/CdTe devices, the MZO (MgO 11%, ZnO 89% by weight) and the GMZO (Ga_2O_3 3%, MgO 2%, ZnO 95% by weight) films used for this chapter were fabricated at Colorado State University (CSU) using an in-line vacuum deposition system, also referred as the Advanced Research and Development System (ARDS) [154] and further electrical characterisation for preconditioning studies were performed at Loughborough University. The samples were packaged under vacuum and then shipped to Loughborough, UK by courier from Fort Collins, Colorado USA. All samples were kept in the dark under vacuum at Loughborough before and after measurements. The device architecture used for preconditioning was as follows: Glass/TCO/MZO/CST/CdTe/($CdCl_2$&CuCl-treatment)/Te/C/Ni. The thicknesses of the *n* and *p* type layers were: 100 nm of MZO, 0.5 µm of CST and 3 µm of CdTe. The full details of the fabrication process of CST/CdTe devices are provided elsewhere [75].

The MZO and GMZO films were deposited using an RF magnetron sputtering system [145] on NSG-Pilkington TEC^{TM} SB glass (includes a sodium barrier layer with a thin SiO_2 overcoat) with film thicknesses of 500 nm and 520nm, respectively. Two sets of samples, as deposited, and annealed were provided. The MZO films were annealed at 620°C for 140 seconds in the ARDS [154]. Whereas the GMZO films were annealed in Rapid Temperature Cycling (RTC) for 30 minutes and the substrate temperature measured under the pyrometer at the end of the process was 480°C. Compared to a full device stack (which uses 100 nm of MZO as a buffer layer), thicker MZO films were used to ensure lower resistance to aid the Hall effect measurements. 0.5 cm x 0.5 cm samples were cut from the substrates, and 4 contacts were put at the corners of each sample using an ultrasonic iron. Subsequently, samples were mounted on a holder with thin wires for each contact using a soldering iron. The full details of the system capabilities are provided in Chapter 3 - Characterisation Techniques, Hall effect measurements.

6.1.2 Preconditioning Procedures

Following a similar procedure to NREL`s Standard Protocol for Preconditioning and Stabilisation of Polycrystalline Thin Film Photovoltaic Modules [81], two different preconditioning procedures have been applied on the MZO/CST/CdTe devices. These procedures were categorised as *Vacuum* and *Atmospheric* preconditioning and the sequence of each procedure is described below:

Vacuum preconditioning involves annealing at 65°C (using a substrate heater) under vacuum (in the dark) at a pressure of ~ $7.8x10^{-6}$ Torr for an hour. Then, the devices were taken out of vacuum and light soaked for 15, 30, and 60 minutes under 100 $mWcm^{-2}$. Light soaking was performed at open circuit conditions with no temperature control of the device. Dark and illuminated *J-V* curves were recorded before and after the annealing and between each time interval.

Atmospheric preconditioning involves annealing and cooling down the device at different temperatures, under atmospheric conditions, whilst maintaining the device temperature. Preconditioning starts with 60 minutes of light soaking under 100 $mWcm^{-2}$ at 25°C. Then, 30 minutes of light soaking at 85°C followed by 30 minutes of light soaking at 10°C and finally, 30 minutes of light soaking at 25°C. Dark and

illuminated *J-V* curves were recorded before and after the preconditioning and between each temperature.

Similar preconditioning methods have been applied to the MZO and GMZO films (both as deposited and annealed) for conductivity measurements. The films were light soaked under 100 $mWcm^{-2}$ at 25°C for 60 and 120 minutes. Furthermore, as deposited MZO films were $CdCl_2$ treated to identify the potential effect this device level treatment has on the individual film properties itself. $CdCl_2$ was deposited by thermal evaporation at ~1×10^{6} Torr for 20 minutes using 0.5 g of $CdCl_2$ pellets inside a quartz crucible. A set of samples were then annealed on a hot plate in air at a dwell temperature of 420°C, whilst another set was annealed in nitrogen under vacuum at ~400 Torr. Both samples were heated for 1, 5 ,10 and 20 minutes. After the annealing steps, the MZO films were rinsed with DI water to clean the excess $CdCl_2$ on the surface. Treated MZO films were also light soaked in the same procedure as annealed and as deposited films. Additionally, *Atmospheric* preconditioning was applied to the MZO films before conductivity and Hall effect measurements.

Alternatively, *current* biasing was performed on the full devices to attempt recovering the *J-V* characteristics without any illumination or temperature control of the device. The preconditioning was performed by placing the device at forward bias with a current equal to short-circuit current ($\boldsymbol{I_{sc}}$) under 1 Sun injected into the device, using a Keithley source measurement unit. The *J-V* curves were recorded before and after current biasing for 30, 60 and 120 minutes.

6.2 Results

6.2.1 Room Temperature *J-V* Characteristics

The devices were fabricated at CSU, where an initial *J-V* measurement was obtained after fabrication. Figure 6.1 shows *J-V* measurements directly after fabrication (measured in Colorado, labelled as CSU), and before (pre light soaking) and after 15 minutes of light soaking (15 mins of light soaking). The light soaking measurements were performed at Loughborough. The initial *J-V* curve measured at CSU is well behaved showing the typical *J-V* response expected for a high efficiency device, with high fill factor ($\boldsymbol{FF}$). However, upon receipt in Loughborough and before any preconditioning, the *J-V* curves show an `*S*` shaped behaviour, which is commonly referred as a `*kink*` type anomaly in the illuminated *J-V* curve and occurs in the third or fourth quadrant of the *J-V* curve [18]. This can be due to a conduction band offset or a presence of a significant current barrier. After 15 minutes of light soaking under 100 mWcm^{-2} at open circuit conditions, this `*S*` shape behaviour reduces significantly and shows better *J-V* characteristics with improved $\boldsymbol{FF}$ and series resistance ($\boldsymbol{R_s}$). However, 15 minutes of light soaking did not recover the device performance fully. There is also a slight mismatch of short-circuit current density ($\boldsymbol{J_{sc}}$). This is due to the different reference diodes used at the two laboratories and is not a metastable effect.

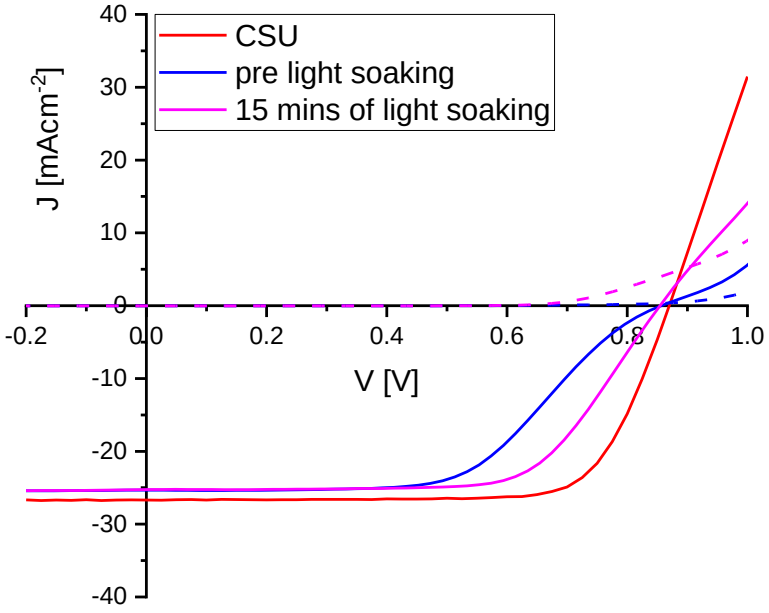

Figure 6.1: Illuminated (solid) and dark (dashed) *J-V* curves at room temperature measured at CSU and before and after light soaking upon receipt to Loughborough. (N.B. dark *J-V* curve for CSU is not provided).

Vacuum preconditioning was applied to the same device after the device was kept under vacuum in the dark for approximately 3 days. The initial `*S*` shaped behaviour appears again (pre-anneal) before any preconditioning. After an anneal under vacuum in the dark (post-anneal) no improvement in *J-V* characteristics is seen (Figure 6.2 (a)). However, after 15 minutes of light soaking the `*S*` shape behaviour reduces and starts showing better *J-V* characteristics. Furthermore, with increased light soaking duration (Figure 6.2 (b)) the `*S*` shape behaviour is removed but the performance of the device was not totally recovered.

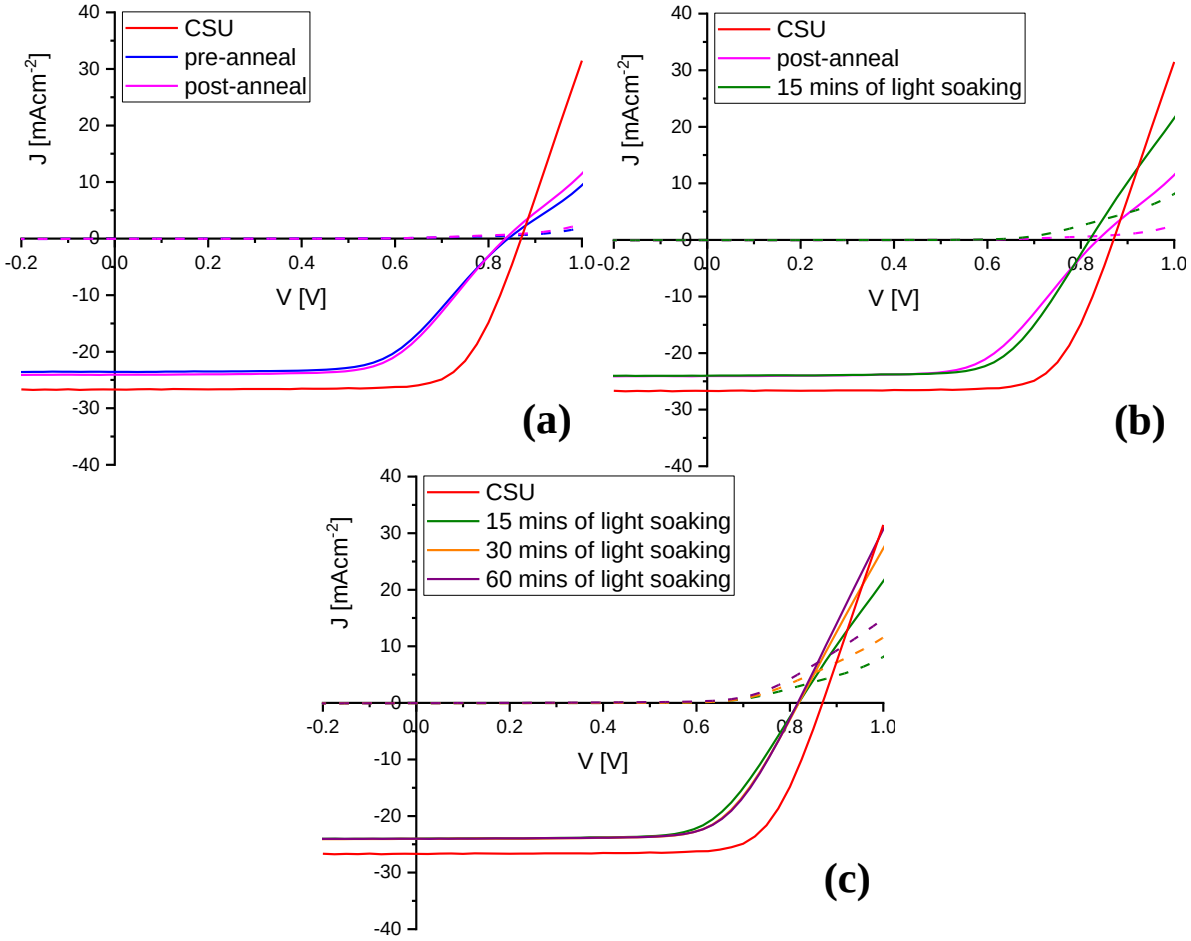

Figure 6.2: Illuminated (solid) and dark (dashed) *J-V* curves for *Vacuum* preconditioning study. *J-V* curves (a) before and after annealing, (b) 15 minutes light soaking after annealing, and (c) 30, 60 minutes of light soaking on the *J-V* characteristics.

The same approach was applied for the *Atmospheric* preconditioning study, where the same device was kept under vacuum in the dark for approximately 3 days. Prior to preconditioning, *J-V* curves were obtained which again showed the `*S*` shaped

behaviour (Figure 6.3). Like *Vacuum* preconditioning, *Atmospheric* preconditioning showed similar *J-V* characteristics with improved $\boldsymbol{R_s}$ when light soaked.

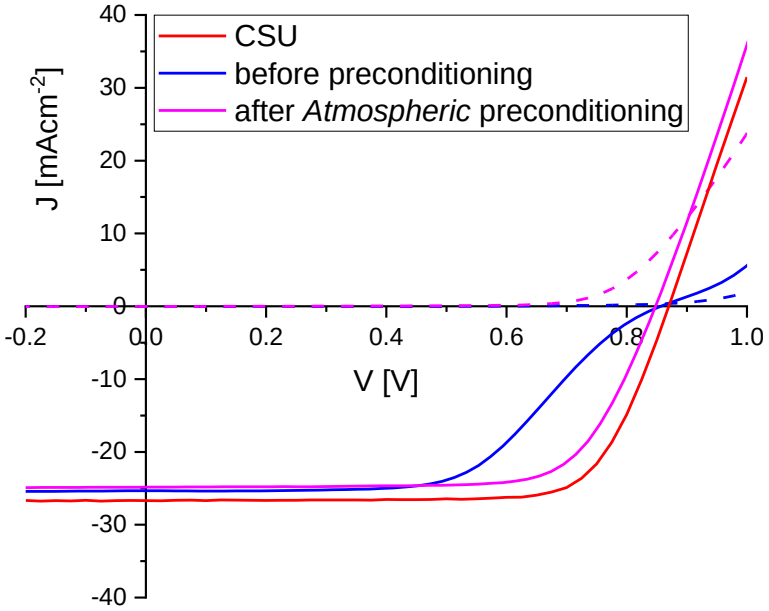

Figure 6.3: Illuminated (solid) and dark (dashed) *J-V* curves for *Atmospheric* preconditioning study (N.B. *Atmospheric* preconditioning: 60 mins of light soaking at 25°C / 30 mins of light soaking at 85°C / 30 mins of light soaking at 10°C / 30 mins of light soaking at 25°C).

Current biasing was applied to a different device after the device was kept under vacuum in the dark for approximately 3 days since the last preconditioning measurements. Prior to *current* biasing at $\boldsymbol{I = I_{sc}}$, *J-V* curves were obtained which once again showed the `*S*` shaped behaviour (Figure 6.4). After 30 minutes of current biasing, the `*S*` shape behaviour reduces significantly and shows better *J-V* characteristics which had similar effect to the light soaking preconditioning procedures previously. Furthermore, *J-V* characteristics slightly deteriorated after 120 minutes of *current* biasing, due to sample heating. Although the `*S*` shape behaviour is removed, the performance of the device was not totally recovered.

Light soaking can establish a stronger built-in ($\boldsymbol{V_{bi}}$) field which may promote an improvement in the band alignment at the interface between the buffer and absorber layer [164]. The $\boldsymbol{V_{bi}}$ can be determined from the slope of the Mott-Schottky plot using the *C-V* profiling technique [165], along with carrier concentration and this analysis is discussed in section 6.2.3.

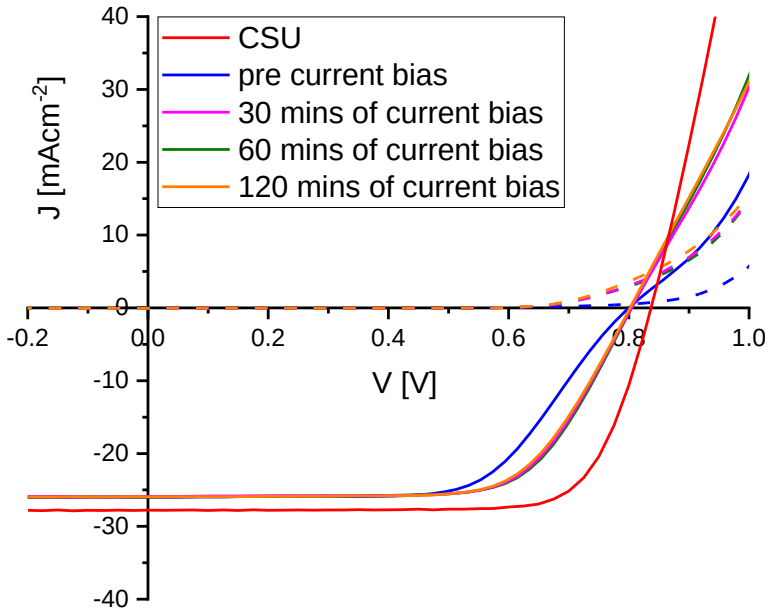

Figure 6.4: Illuminated (solid) and dark (dashed) *J-V* curves for *current* biasing preconditioning study.

	V_{oc} [mV]	J_{sc} [mAcm^{-2}]	FF	PCE [%]	Scaled PCE [%]
CSU	870	26.7	0.750	17.43	17.43
Before preconditioning	842	24.0	0.676	13.66	15.20
Vacuum preconditioning	817	24.0	0.699	13.72	15.26
Atmospheric preconditioning	847	24.8	0.727	15.30	16.44

Table 6.1 – Summary of the device parameters before and after preconditioning.

Table 6.1 summarizes the PV parameters extracted from before and after any preconditioning, the initial measured PV parameters from CSU, and estimated efficiencies if the J_{sc} was the same as that measured at CSU, 26.7 mAcm^{-2}. This was done to effectively normalised the data to compare among the measurements in different laboratories. Despite all the preconditioning attempts, device performance was not recovered to initial parameters (measured at CSU straight after fabrication), suggesting that the devices might be showing some degradation alongside the metastable behaviour. The *Atmospheric* preconditioning is used for the rest of the analysis, as devices showed better recovery compared to other procedures.

6.2.2 Temperature Dependent *J-V* Characteristics

The temperature dependent *J-V* (*JVT*) measurements were carried out for temperatures between 315 K and 115 K with 10 K steps. Figure 6.5 shows the *JVT* curves for the device (a) before and (b) after *Atmospheric* preconditioning. All measurements were carried out at 50 mWcm^{-2} with a white LED light source.

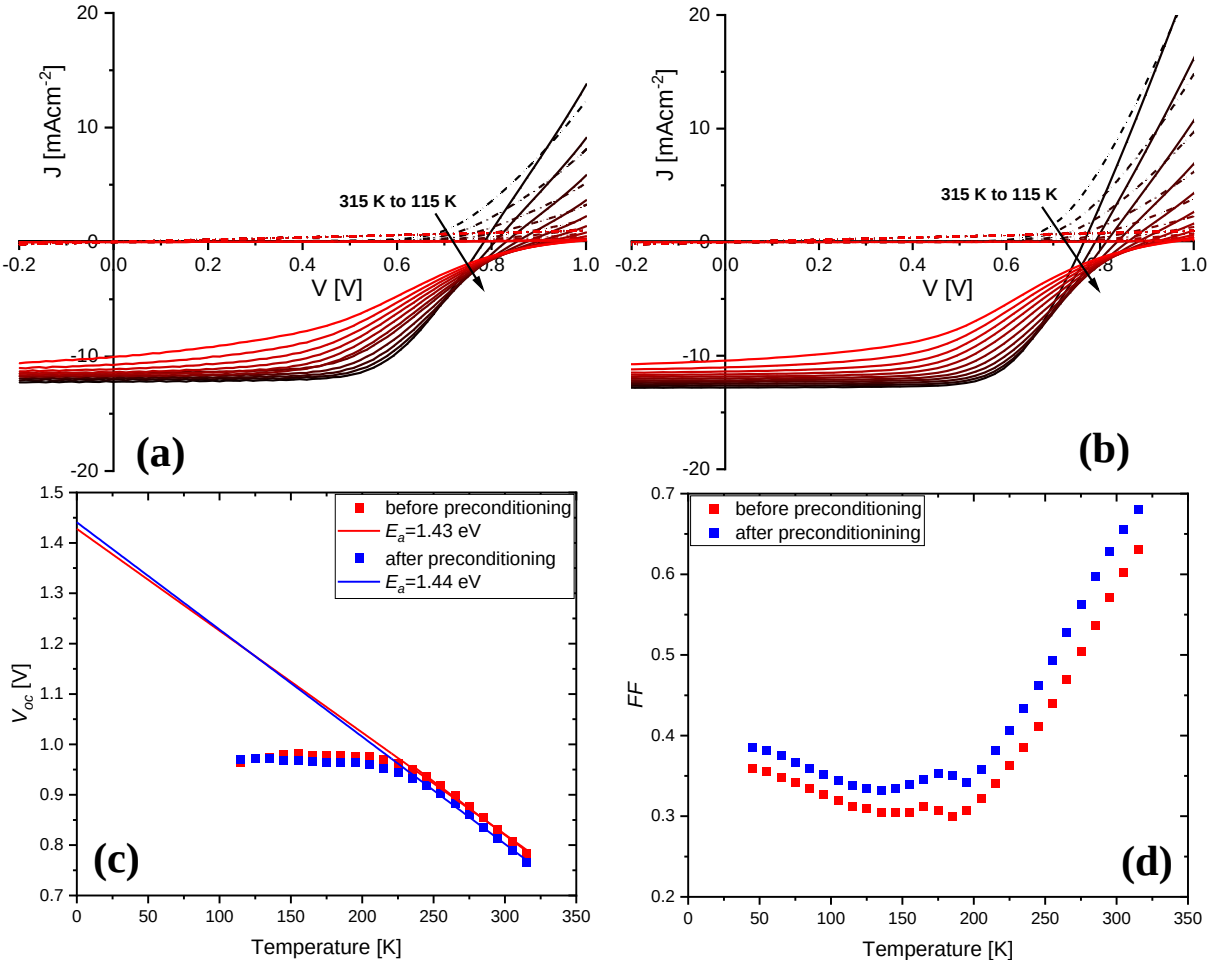

Figure 6.5: The dark and illuminated (50 mWcm^{-2}) *J-V* curves are displayed for temperatures between 115 K and 315 K (in 20 K steps) for the full device (a) before, (b) after *Atmospheric* preconditioning, (c) extrapolation of the V_{oc} to 0 K for high temperatures (315-235 K) which falls below the E_g of the device, and (d) *FF* versus temperature.

The V_{oc} versus T analysis shows a small increase in activation energy (E_a) of the recombination mechanism before (1.43 eV) and after (1.44 eV) preconditioning (shown in Figure 6.5 (c)). Comparing E_a with the E_g = 1.45 eV of the device, the recombination mechanism before and after preconditioning dominates at the interface and similar results have been observed with other CSU samples studied in Chapter 5. There are several reports of CdTe based solar cells that the

nonuniformity at the interface which affects the voltage distribution can be improved after light soaking under 1 Sun (AM1.5G), resulting in an increase in $\boldsymbol{PCE}$ [164] [166][167]. The buffer/absorber band alignment or a small barrier can play significant role in the interface recombination [59]. Light soaking can promote an increase of positive charges in the buffer layer, leading to an increase of the barrier height. This barrier determines the transport of holes to the buffer/absorber interface and acts as a blocking layer, thus reducing the interface recombination. The reduction of interface recombination after the device light soaked suggests that the current blocking barrier in forward bias has slightly improved, resulting in less pronounced rollover at low temperatures, shown in Figure 6.5 (d).

6.2.3 Capacitance Spectroscopy

Figure 6.6 shows the admittance spectra for the device (a) before and (b) after *Atmospheric* preconditioning. The measurements were performed under equilibrium conditions (0 V bias) in the dark, between temperatures 45 K and 315 K, and show an increase in junction capacitance after preconditioning. This indicates an increase in charge carrier density, assuming a homogeneous doping within the absorber layer. There are two cases that needs to be considered. In case there is no Fermi level pinning, the energetic distance from the Fermi level to the conduction band minimum would increase due to an increased band bending in the absorber layer. If there is Fermi level pinning, the energetic distance would remain constant. Therefore, the activation energy ($\boldsymbol{E_A}$) of the defects should either increase or remain constant after light soaking.

The device before and after *Atmospheric* preconditioning shows an admittance step at low temperatures (between 225 K and 135 K) and high frequencies, marked as N1. This admittance step is often discussed in the literature as the N1 defect, and there has been considerable debate about the correct interpretation about the origin of the N1 step. Most published findings assume that it is a response from defect states at the buffer/absorber interface, and [107][108][104][109] there are also other findings that assigned the origin of the step as a bulk defect in the absorber layer, especially with CIGS solar cells [110]. The complexity of the structure of these solar cells has opened the way for many interpretations in providing direct answers about the origin of the observed steps. The relation between the energy of the N1 step and

current blocking at low temperature is an important aspect when interpreting the origin of the N1 defect.

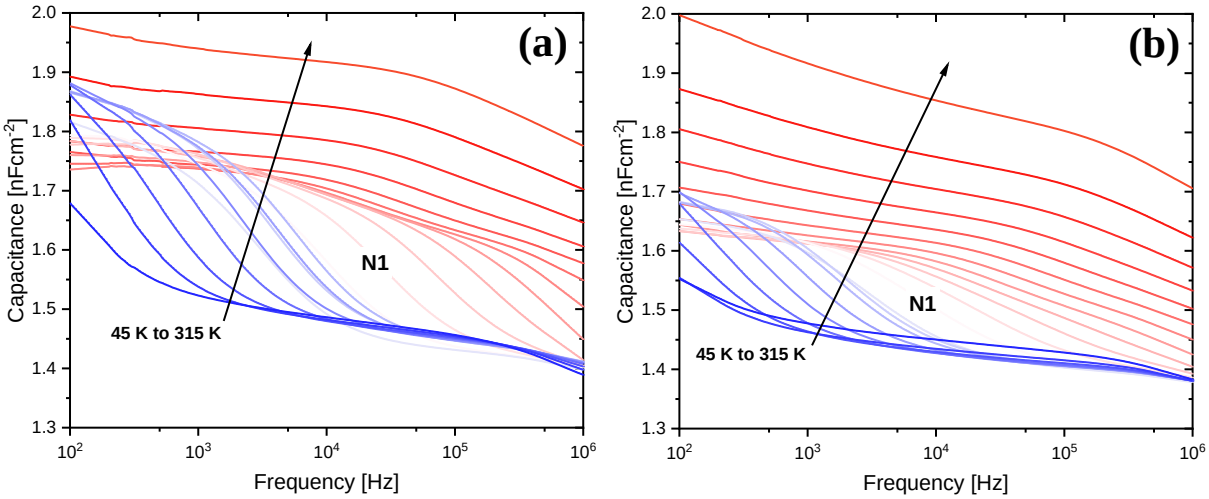

Figure 6.6: Admittance spectra in the dark at 0 V between 45 K and 315 K for the full device before (a) and after (b) *Atmospheric* preconditioning. Admittance step is visible between 135 K and 225 K which is marked as "N1" for both spectra.

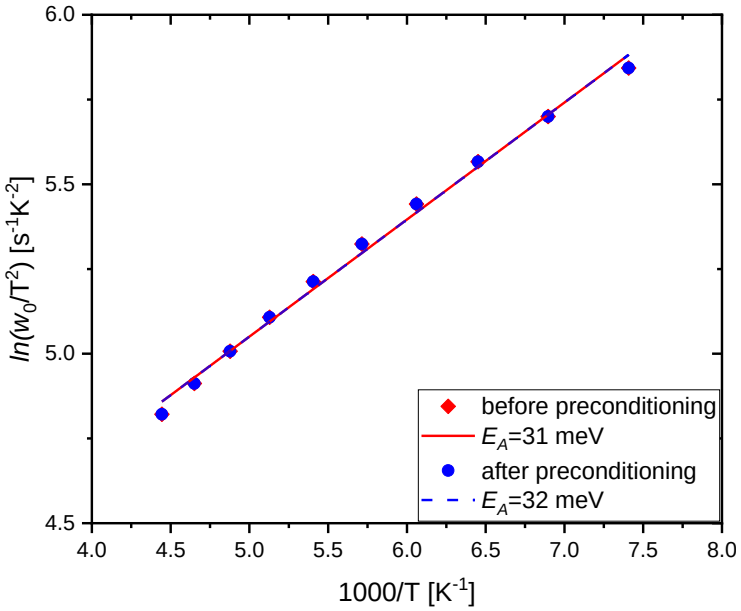

Figure 6.7: Arrhenius plot the full device before (red squares) and after (blue circles) *Atmospheric* preconditioning.

The activation energies for before and after *Atmospheric* preconditioning were obtained from Arrhenius plots (Figure 6.7) using the maxima of the conductance spectra, and found to be $\boldsymbol{E_A}$ = 31 meV and $\boldsymbol{E_A}$ = 32 meV, respectively. Based on the measured activation energies, the energetic position of these steps link to the N1

defect (a shallow level defect), which may possibly be originating from the buffer/absorber interface. Furthermore, preconditioning did not cause any significant changes in terms of the defect levels. However, the junction capacitance has slightly improved at low frequencies due to light soaking and more pronounced N1 step observed.

The depth profiles of the net carrier concentration before and after preconditioning were investigated using capacitance-voltage (*C-V)* and drive-level capacitance profiling (*DLCP*) techniques. For this study, *Vacuum* preconditioning was also applied to investigate the effects of annealing on the depth profile characteristics. All measurements were carried out in the dark at room temperature, with dc bias voltage varied at a fixed frequency. Figure 6.8 shows the depth profiles for both *C-V* and *DLCP* measurements before and after *Atmospheric* preconditioning.

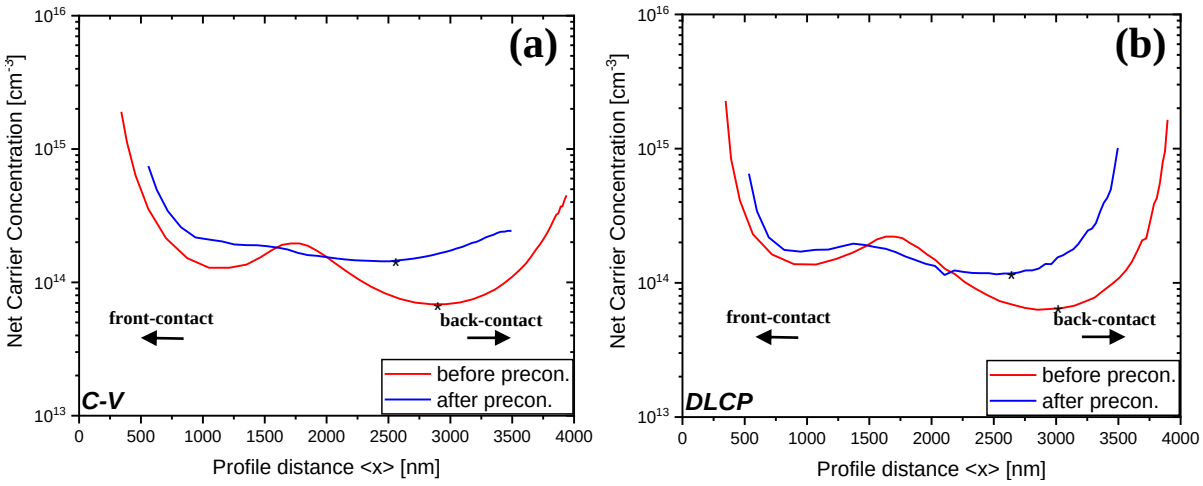

Figure 6.8: Comparisons between (a) *C-V* and (b) *DLCP* depth profiles before and after *Atmospheric* preconditioning, at room temperature. The net carrier concentration values are extracted at 0 V bias (marked as `*`).

Depth profiles exhibit very similar shape and profile distance for both techniques. Before any preconditioning, depth profiles showed an unusual double minima, often seen in solution-processed CIGS devices fabricated at Loughborough University, which have a bilayer structure (a large-grain top layer covers a fine-grain bottom layer in the absorber layer) [123][168][129]. The double minima for solution-processed CIGS devices is usually caused by the bilayer structure in the absorber layer when the depletion width crosses between the two layers during the voltage sweeps. Another reason for this double minima might be due to the presence of

defects, which affects the shape of the depth profiles. The double minima in this case might be due to the graded absorber, CST/CdTe.

Figure 6.9 shows the depth profiles for both *C-V* and *DLCP* measurements before and after *Vacuum* preconditioning, where a different cell from the same device was used. Furthermore, *Vacuum* preconditioning resulted in similar effects on the depth profiles. However, annealing did not show any significant changes in the shape of depth profiles. After both *Atmospheric* and *Vacuum* preconditioning, the second minima towards the back of the device becomes less pronounced. Hence, the depth profiles become more U-shaped commonly reported for CdTe devices.

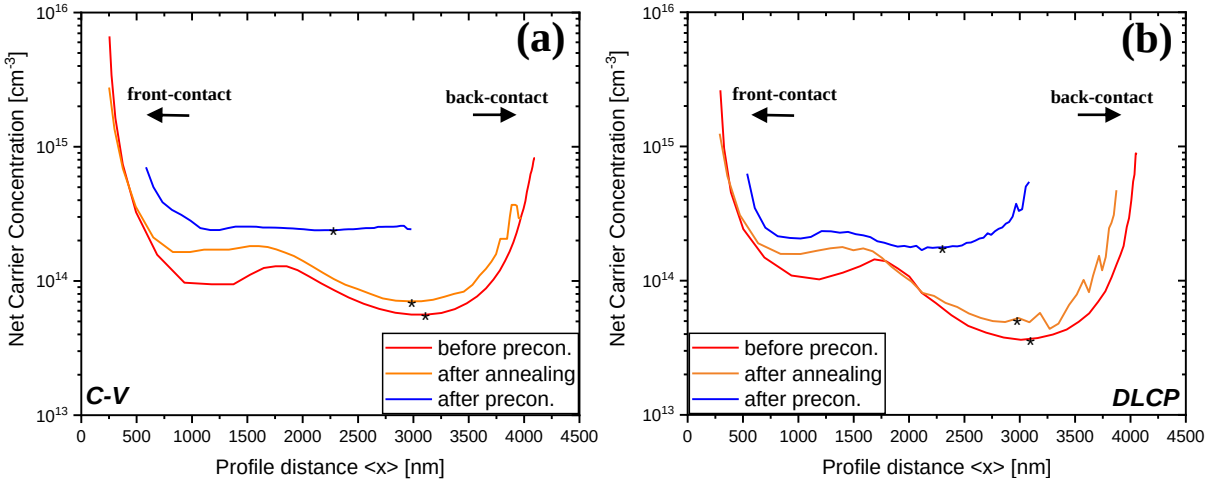

Figure 6.9: Comparisons between (a) *C-V* and (b) *DLCP* depth profiles before and after *Vacuum* preconditioning, at room temperature for a different cell. The net carrier concentration values are extracted at 0 V bias (marked as `*`).

Table 6.2 summaries the effects of preconditioning (on different cells but from the same device) on the net carrier concentration for both *DLCP* and *C-V* methods (N_{DLCP} and N_{CV}), deep level defect densities (N_{defect}), built-in voltage (V_{bi}) and depletion width (w_d) at 0 V. The V_{bi} before and after preconditioning was extracted from the Mott-Schottky plots (Figure 6.10) using the linear portion of plots. An increase in V_{bi} is observed in devices after preconditioning with both *Atmospheric* and *Vacuum*
(ITO)/CdTe devices and believed to improve the band alignment between ITO and CdTe [164]. However, it remained only for short time period, likewise to what has been observed in MZO/absorber devices in this study.

	N_{DLCP} [cm^{-3}]	N_{defect} [cm^{-3}]	N_{CV} [cm^{-3}]	w_d [nm]	V_{bi} [mV]
Before *Atmospheric* preconditioning	7.32 x10^{13}	2.35 x10^{13}	8.27 x10^{13}	1133	787
After *Atmospheric* preconditioning	1.16 x10^{14}	2.83 x10^{13}	1.45 x10^{14}	885	842
Before **Vacuum* preconditioning	4.32 x10^{13}	4.05 x10^{13}	5.61 x10^{13}	1319	723
After **Vacuum* preconditioning	1.76 x10^{14}	9.17 x10^{13}	2.43 x10^{14}	702	886

Table 6.2 – Summary of *C-V* and *DLCP* measurements for the device before and after *Atmospheric* and *Vacuum* preconditioning (*N.B. different cells used for *Vacuum* preconditioning).

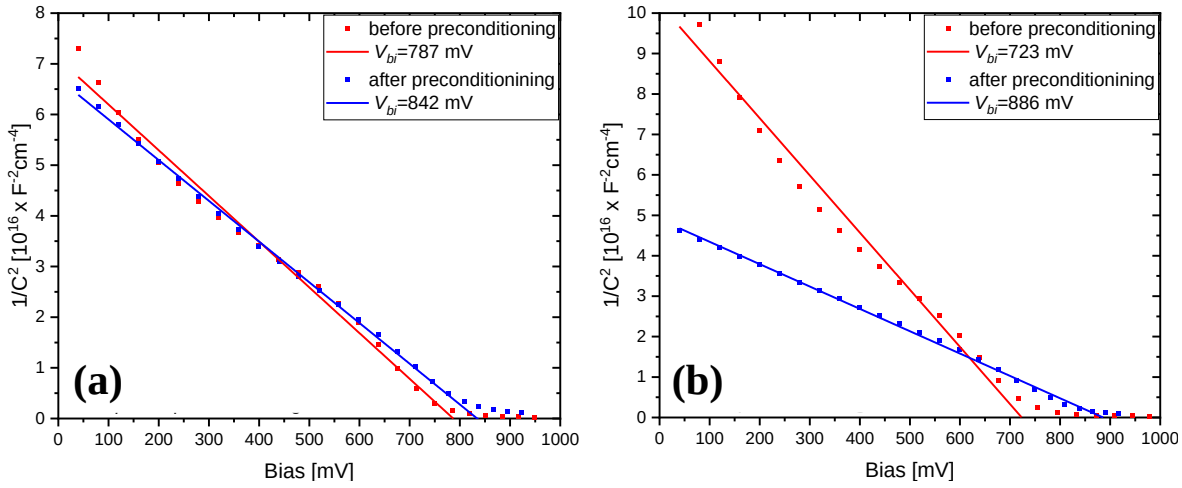

Figure 6.10: Mott-Schottky plots for different devices which are (a) *Atmospheric* and (b) *Vacuum* preconditioned. V_{bi} is estimated using the linear portion of plots.

The net carrier concentration was extracted at 0 V from the depth profiles, and an increase was observed after preconditioning. This increase was expected as devices were light soaked and values after preconditioning are now much more closer to reported values for CdTe devices in literature [70]. The depth profiles became narrower after preconditioning and these changes follow well with the increase observed in net carrier concentration. The defect density was measured by *DLCP* in the dark at room temperature for varied frequency and oscillating voltage. Moreover, the total concentration from the sum of the N_{defect} and N_{DLCP} should approximately

be equivalent to the net carrier concentration from the *C-V* measurements, $\boldsymbol{N_{cv}}$. Preconditioning results for both *Vacuum* and *Atmospheric* procedures show $\boldsymbol{N_{DLCP}} + \boldsymbol{N_{defect}} \approx \boldsymbol{N_{CV}}$ compared to results before any preconditioning applied on both devices. The net carrier concentration has increased significantly after light soaking, resulting a small increase in defect density in the absorber. Due to high net carrier concentration, the small increase in defect density shows no significant effect on the device performance. The increased net carrier concentration after light soaking shows a similar effect to a doped absorber layer with an increased $\boldsymbol{V_{bi}}$ and a narrower $\boldsymbol{W_d}$.

Despite all the preconditioning attempts, the recovery of PV parameters and the *J-V* characteristics remained only for 3 days while the devices were maintained under vacuum in the dark. Since the capacitance and temperature dependent *JVT* measurements before and after preconditioning showed recombination centres, and defect levels at/ close to the buffer/absorber interface, the next appropriate step would be investigating the buffer layer. The characteristics of the buffer layer before and after preconditioning will provide better understanding in observed metastable behaviours, and any relation between the measured devices.

6.2.4 MZO Films

The MZO films were measured using an AC PDL Hall effect system to investigate the effect of preconditioning on the film properties. The Hall effect measurement consists of measuring the conductivity, carrier concentration and mobility of the film. The measurements cover 3 important steps in order to extract accurate results, the contact check, the sheet resistance measurement, and Hall resistance measurement. The sequence of each step is described below:

In step 1, contacts between the sample and the sample holder are checked to ensure there is a good connection established. 2-point resistance for each contact is extracted. If the resistance mean is reasonable and there is linear *I-V* response, then step 2 follows.

In step 2, the resistivity measurements were performed using van der Pauw configuration (more details in Chapter 3) and the *I-V* response of the signal is measured. The conductivity measurements consist of measuring the sample

resistivity from sheet resistance based on the algorithm of NIST (see Chapter 3). For measurements to be successful, conductivity measurements should give a linear *I-V* response since the mobility is calculated from this step. The linearity of the *I-V* response can be assessed by the correlation coefficient (*R*) of the measurements. The measurement with correlation coefficient equal or bigger than 0.98 (maximum *R*=1) indicates a linear response which will provide accurate and reliable measurements.

In the final step, Hall voltage is recorded simultaneously from van der Pauw configuration with changing magnetic field as two magnets rotate at a constant angular speed. Moreover, numerical Lock-in detection is performed, and Fourier spectra of the magnetic field and raw Hall signal is extracted to be used in determination of carrier concentration and its carrier type.

Table 6.3 shows the linearity of *I-V* response for conductivity results on as deposited, and annealed MZO films before and after preconditioning, and $CdCl_2$ treatment for different annealing conditions. Most of the results have shown non-linear *I-V* response for the sheet resistance measurements, and longer light soaking has shown no further improvements. Therefore, alternatively the changes in linear response of the *I-V* characteristics have been studied to investigate any improvements in conductivity, since non-linear measurement will provide incorrect values.

The MZO films which were either light soaked, annealed in the ARDS, *Atmospheric* preconditioned, or annealed at atmosphere after $CdCl_2$ treatment did not show any significant changes in conductivity, thus no proper Hall signal was detected to resume with the Hall measurements. However, the MZO films which were $CdCl_2$ treated and annealed in nitrogen under vacuum have showed significant improvements in conductivity, and improved response of the signal from the measurements. Since the MZO films are sensitive to the presence of atmospheric humidity and oxygen, annealing the films at atmosphere after $CdCl_2$ treatment may introduce more oxygen into the film, causing the conductivity to decrease. However, annealing in nitrogen under vacuum could prevent the introduction of oxygen into the film, benefiting the conductivity. Annealing for a longer time in nitrogen has shown significant improvements in linearity of the *I-V* response compared to those annealed

for shorter time. For a standard $CdCl_2$ treatment (at Loughborough University) on CdTe devices, annealing occurs on a hot plate in air at a dwell temperature of 420°C for 1 minute. The MZO films might require longer annealing time for the treatment to be effective as it has done on the complete devices.

***Red* = not a linear response** ***Yellow* = improved response but still not linear** ***Green* = a linear response**		***2-point Resistance***		***Sheet Resistance***	
		before light soaking	*after* light soaking	*before* light soaking	*after* light soaking
Initial (as deposited)		0.937683	0.947090	0.926245	0.907673
Atmospheric preconditioning		0.959260	0.960678	0.958685	0.909451
***$CdCl_2$* treatment on as deposited films**					
Duration [minutes]	**Annealing conditions**				
1	at atmosphere	0.935538	0.944430	0.906781	0.934729
	in nitrogen	0.944018	0.996457	0.943156	0.953456
5	at atmosphere	0.961995	0.962282	0.954220	0.952093
	in nitrogen	0.945343	0.967892	0.948304	0.952996
10	at atmosphere	0.955767	0.966202	0.815548	0.829598
	in nitrogen	0.984175	0.999952	0.838606	0.893446
20	at atmosphere	0.953088	0.941040	0.938090	0.927659
	in nitrogen	0.956965	0.999862	0.936151	0.956751
Annealed MZO film at 620°C for 140 seconds in ARDS					
		0.965068	0.947552	0.9083923	0.840719

Table 6.3 – Summary of the linearity of *I-V* response for conductivity measurements for the MZO films before and after 1 hour light soaking, *Atmospheric* preconditioning, and effect of $CdCl_2$ treatment.

Despite all attempts to recover the *I-V* response of the measurements, films were still resistive, and at the limit of the system to provide any reliable results. Therefore, no linear sheet resistance response and proper Hall signal were detected. Since the MZO films in an as deposited state are insulating, MZO as a buffer layer (in the traditional sense as a highly doped emitter) should not work in the device. It is therefore clear that another mechanism is present which enables the MZO to function as a window/buffer/emitter layer. For example, oxygen vacancies could be created within the MZO film during full device processing, possibly during the $CdCl_2$ treatment. Oxygen vacancies create electron donors which would result in improved carrier concentration in the film [169]. Also, the incorporation of excess chlorine

atoms from $CdCl_2$ treatment into the ZnO bulk might be another mechanism that enables the MZO to function, as chlorine vacancies substitute the oxygen vacancies in the lattice [126].

In an effort to fully understand the doping profile across the *p-n* junction, Hall effect measurements were made on the bare CST/CdTe absorber layer to determine the film carrier concentration. The film thickness is around 3.5 µm and conductivity measurements showed a linear *I-V* response. Table 6.4 summarises the extracted parameters from the Hall effect measurements. The carrier concentration was calculated as 1.63 $x10^{14}$ cm^{-3} which is in close agreement with the values measured from capacitance measurements. Since the doping density is low on the absorber side, the buffer layer must have a higher doping density to create a strong and long field into the absorber to achieve high charge separation. Hence, the MZO films should have a high carrier concentration above 10^{14} cm^{-3}. However, as deposited MZO films were too resistive from the conductivity measurements, suggestions that the films might have a low carrier concentration before any device processing or treatment.

Sheet Resistance [Ý / Ĭ]	***Sample Resistivity [Ý . c m]***	***Mobility [cm^2/Vs]***	***Carrier Concentration [cm^{-3}]***	***Carrier Type***
$8.72x10^9$	$1.65x10^6$	4.486	$1.63x10^{14}$	*p*-type

Table 6.4 – The conductivity and Hall effect measurements on CST/CdTe absorber layer.

Although MZO substitution as a buffer layer in CST/CdTe devices results in high $\boldsymbol{PCE}$, the metastability and degradation are one of the main concerns in the variation of PV parameters from different laboratories, under different ambient conditions. As deposited and annealed MZO films before and after any preconditioning, and $CdCl_2$ treatment showed non-linear *I-V* response, thus no proper Hall signal was detected to extract the carrier concentration and mobility. One potential way of improving the film preparation to extract the Hall signal is to do a standard fabrication process on a glass/MZO/CST/CdTe stack, and exfoliate the CST/CdTe layer after $CdCl_2$ treatment. In this way, any potential effect on the material properties and conductivity of the MZO layer will be analysed on a device level treatment and provide a more accurate representation of the effect on the MZO layer. This exfoliation technique has been used before on CZTS based solar cells in performing Hall effect

measurements [170][171]. However, due to the time constraints, complexity of getting samples and scope of the project, an exfoliation study could not be completed.

6.2.5 Ga-Doped MZO Films

Alternatively, doping of the MZO layer can enhance the film conductivity. Intrinsic doping can be achieved via oxygen vacancies, whilst extrinsic doping can be achieved by incorporation of different impurities in the film. Zinc oxide (ZnO) has been widely used as TCOs [172] or buffer layers [173] and gained a lot of research interest. The undoped ZnO thin films have high resistivity, and using different dopants help to enhance the electrical conductivity of the films [162]. Different elements can be chosen in the III column of the periodic table as a dopant (for example, B, Al, Ga, In, etc and gallium (Ga) doping has been shown to be one of the best dopants for ZnO [174]. Another key advantage of Ga over is that it is more moisture resistant and stable in oxidising environment [162][175]. Hence, a low amount of Ga could be a suitable dopant for the MZO, which should enhance the carrier concentration of the film slightly to that expected for a buffer/emitter layer.

Light soaking conditions	***2-point Resistance [Ý]***	***Sheet Resistance [Ý / Ĭ]***	***Sample Resistivity [Ý . c m]***
Initial (no light soaking)	3.96 x10^{8}	2.92 x10^{9}	1.64 x10^{5}
1 hour	4.85 x10^{7}	3.28 x10^{7}	4.08 x10^{3}
2 hours	3.57 x10^{6}	1.83 x10^{6}	3.26 x10^{2}

Table 6.5 – The effect of light soaking on conductivity measurements in annealed GMZO films.

As deposited and annealed GMZO films were still too resistive for further Hall effect measurements, thus no proper Hall signal was detected. Although both films were resistive, annealed GMZO films showed improved *I-V* response. Light soaking experiments have shown no improvements in conductivity for as deposited GMZO films. However, annealed GMZO films showed a large improvement in conductivity after light soaking. Table 6.5 shows the effect of the light soaking on conductivity measurements for the annealed GMZO films. After 1 hour of light soaking, measurements showed an improvement in conductivity and linearity of *I-V* response. Moreover, further improvements have been observed after 2 hours of light soaking,

while longer light soaking duration did not show any further improvements both in conductivity and the linearity of the *I-V* response. Nonetheless, as deposited GMZO films showed no improvements in conductivity after 1 or 2 hours of light soaking. Figure 6.11 shows the variation in resistivity (after 1 hour of light soaking) for annealed GMZO films which were exposed to the atmosphere for 3 days. From before to after light soaking, a very rapid increase in conductivity is observed. Following the initial light soak, the film was kept in the dark and the resistivity increases when the film is measured next day. This increase in resistivity continues for the next 3 days.

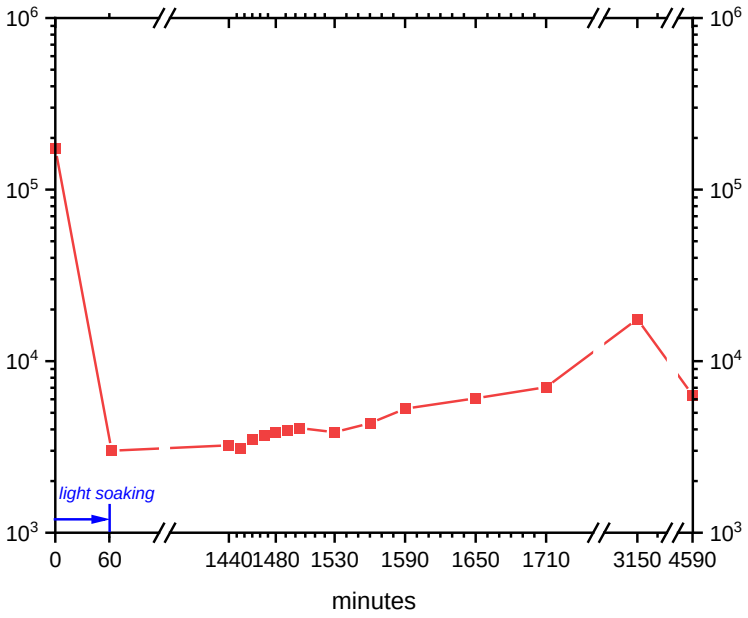

Figure 6.11: The analysis of the resistivity of annealed GMZO films exposed to atmosphere after 1 hour of light soaking.

Measuring the Hall effect on films which are highly resistive and exhibit metastability (when exposed to the atmosphere) can be quite challenging. Since annealed GMZO films have a linear *I-V* response from step 1 and 2, measurements can proceed further in an attempt to extract the carrier concentration and mobility. Table 6.6 shows the extracted data from the Hall effect measurements for annealed GMZO film before and after 2 hours of light soaking (analysis includes all 3 steps of attempting to achieve accurate results). The duration of the measurements in step 3 with these metastable films is crucial as the films degrade over time, as seen in Figure 6.11. On an attempt of measuring films after 1 hour of light soaking, a gradual decrease in Hall signal was observed, and the resistivity went back to its initial value

after measurement was completed. However, with 2 hours of light soaking Hall signal was more stable throughout the measurements. Many attempts have been made to extract the carrier concentration and mobility by varying the duration time of the measurement, drive current, and the speed of the rotating magnets. Although the Hall signal was fully resolved after 2 hours of light soaking, the results from the Lock-in and FT analysis in step 3 are not in close agreement, and no clear FT peak has been observed. Hence, the measurements were not successful. The decrease in resistivity does indicate some increase in carrier concentration. Since the resistivity has improved by 3 orders of magnitude, the carrier concentration was expected to increase by 3 orders of magnitude as well. However, no change in carrier concentration and increased mobility were observed.

Condition	***Before light soaking***	***After light soaking***	
2-point Resistance [Ω]	3.96 x10^{8}	3.57 x10^{6}	**STEP 1**
Contact Check – Linear Response?	Yes	Yes	
Sheet Resistance [Ω/□]	2.92 x10^{9}	1.83 x10^{6}	**STEP 2**
Sample Resistivity [Ω.cm]	1.64 x10^{5}	3.26 x10^{2}	
Linear *I-V* Response?	Yes	Yes	
>10 cycles of Magnetic Field?	Yes	Yes	**STEP 3**
Drive Current [A]	1x10^{-12}	1x10^{-10}	
Clear Fourier Transform (FT) Peak and Stabilised Lock-in?	No & Yes	No & Yes	
Carrier Concentration [cm^{-3}]	3.10 x10^{14}	1.54 x10^{14}	
Mobility [cm^2/Vs]	0.1235	222.3	
Carrier Type?	N	N	
Measurement – Pass/ Fail?	**FAIL**	**FAIL**	

Table 6.6 – Steps of the Hall effect measurement for before and after light soaking on the annealed GMZO film.

6.3 Conclusions

The PV parameters of MZO/CST/CdTe devices have been measured following transport between two laboratories. Different preconditioning procedures were applied to recover the device performance. Annealing the device did not show a significant improvement. However, the longer light soaking time with controlled temperature resulted in a significant recovery of the device performance. The devices showed an unusual double minima in depth profiles from both *C-V* and *DLCP* measurements. This double minima could be attributed by having a graded absorber layer, and the minima towards the back of the junction becomes less pronounced after preconditioning. Additional to light soaking, *current* biasing was applied to the devices in an attempt to recover the PV parameters, and results showed similar behaviour to light soaking. Despite all the preconditioning attempts, storing the device in the dark for approximately 3 days appears to reverse the PV parameters. From temperature dependent *J-V* and capacitance measurements, recombination centres and defect levels are found located at the interface for before and after preconditioning. These defects can contribute to metastable behaviour and the associated degradation observed in the devices.

One of the possible reasons for observed differences in PV parameters might be due to degradation of the MZO layer, since temperature dependent measurements shows recombination centres and defect levels dominate at the MZO/absorber interface. Furthermore, analysis of preconditioning, light soaking and $CdCl_2$ treatment on MZO films were studied to investigate the effect on the conductivity and Hall effect measurements using PDL Hall effect system. The MZO films which were either annealed, light soaked or preconditioned have shown no significant changes in conductivity and found to be too resistive. Thus, no proper Hall signal was detected. After $CdCl_2$ treatment in nitrogen under vacuum followed by light soaking, films showed an improvement in *I-V* response. Although the signal was improved, it was still not a linear in order to extract reliable results from Hall effect measurements. Recent studies with an addition of Ga in to the MZO films showed a significant improvement in conductivity and Hall signal. However, a gradual decrease in signal was observed over time after films were light soaked and removed from the desiccator. Thus no reliable and accurate results could be extracted.

Chapter 7

Conclusions

CIGS and CdTe based solar cells have achieved high efficiencies among all the other thin film technologies. However, these solar cells suffer from material degradation, the presence of deep level defects, light induced metastabilities and current barriers at the junction which limit the device performance. The most fundamental measurement techniques only provide information on the overall performance of the device under standard test conditions and additional techniques require to understand these limiting processes. Capacitance spectroscopy has been used as a tool to identify the defect density, energy level of defects and carrier concentration of semiconductors by means of admittance spectroscopy, *C-V* profiling and *DLCP* techniques. Admittance spectroscopy provides the energy levels of the defects (shallow or deep level defects) from the admittance steps, N1 and N2. There are different interpretations in literature concerning the origin of these steps depending on the device configurations. N1 step often contributes to the defects at the buffer/absorber interface and N2 the defects in the bulk of the absorber layer. The *DLCP* measurements can provide the defect density and the net carrier concentration of the absorber. Likewise, the *C-V* measurements can be used to extract the net carrier concentration. However, it is sensitive to the presence of deep level defects and the interface defects. Thus, affecting the measurements. Along with the capacitance spectroscopy, temperature dependent *J-V* technique is used to identify the locations of recombination mechanism in the devices. In addition, PDL Hall effect measurements are used in an attempt to extract the carrier concentration and mobility of the films. Knowledge of these properties will provide feedback to fabrication process in understanding the behaviour of the devices at different electrical excitation or prior exposure history of light and environmental stresses to

improve the device efficiency further. Especially with thin films solar cells, these are crucial information in understanding the different recombination mechanisms and limiting factors of the devices.

The effect of Sb in CIGS devices resulted in an improved device performance, especially $\boldsymbol{J_{sc}}$. The bilayer structure of large-grain top layer and a fine-grain bottom layer of the absorber has been observed, and it is common structure often seen in solution-processing CIGS and CZTS solar cells. The Sb doping resulted in a shifted *EQE* spectra in the long wavelength decay, indicating a decrease in $\boldsymbol{E_g}$. Although the In/Ga ratio in the precursor solution is fixed, the change in the final In/Ga ratio in the selenised absorber as an effect of Sb doping might be the only reason to explain this behaviour. The *EL* imaging showed an uneven signal which might be due to random crystal CIGS grains amplified by their solution-based nature, presence of local shunts, or grain boundary recombination in the absorber layer. The admittance spectroscopy revealed a N1 step as a result of shallow level defect by Sb doping and has removed the N2 defects from the absorber layer which has been observed with the devices without Sb doping. Since the light soaking experiments have shown no significant changes in the net carrier concentration from the *C-V* measurements, the N1 step might be an indication of the defect origin and possibly located at the CdS/CIGS interface. The $\boldsymbol{V_{oc}}$ versus $\boldsymbol{T}$ analysis for the recombination mechanism indicates that the main recombination mechanism for the device with Sb dominates in the bulk. The incorporation of Sb into the CIGS might benefit the surface passivation and reduces the blocking barrier at the CdS/CIGS interface which was observed with the devices without Sb doping. This could be due to compositional changes which might improve the band alignment of CdS/CIGS, leading to improved device performance. The Sb doped devices showed lower net carrier concentration and defect density compared to devices without, indicating that adding Sb into the absorber does not necessary dope the layer, possibly passivates the defects. The differences in the depth profiles from both *C-V* and *DLCP* measurements indicate the presence of the defects which affects the depth profiles. The light induced metastabilities observed in the *J-V* and *C-V* measurements resulted an increase in the $\boldsymbol{FF}$, net carrier concentration and the junction capacitance, which the origin of these metastable behaviours is believed to be in the bulk and relates to the

consequence of donor-acceptor transition of the Se Cu divacancy complex from the literature.

The effect of Te at the back of the MZO/CST/CdTe devices have shown a major improvement on the $\boldsymbol{FF}$, mainly due to an increased $\boldsymbol{R_s}$ and no rollover on the *J-V* curves. These devices resulted in $\boldsymbol{PCEs}$ above 14%. Adding Te has slightly improved the interface recombination in the devices without CST layer by passivating the back surface defects which resulted in better *J-V* characteristics and enhanced $\boldsymbol{V_{oc}}$. The CST/CdTe devices without Te showed a low $\boldsymbol{FF}$ due to a large $\boldsymbol{R_s}$ and a low $\boldsymbol{R_{sh}}$. The CST with Te device showed a significant current barrier, resulting an `*S*` shaped J-V characteristics. This behaviour might due to a conduction band offset (CBO) or a presence of a significant current barrier. From the $\boldsymbol{V_{oc}(T)}$ analysis, recombination mechanism for all the devices dominates at/close to the interface with different $\boldsymbol{E_a}$ values. Adding Te at the back of the device passivates either the N1 or N2 defects depending on the devices with/without CST layer. In the case of CdTe devices, Te has removed the N2 defects and left with only shallow defects remaining. Whereas with the CST/CdTe devices, Te has removed the N1 defect. From the *DLCP* measurements, the defect density for the CdTe devices without CST layer is found to be above 10^{14} cm^{-3}. This might be due to the presence of N1 and N2 defects at different temperatures which were extracted from the admittance spectroscopy. In case of the CST/CdTe devices, Te passivates the defects resulting in a reduced defect density. The devices showed net carrier concentration in the range of 10^{13} - 10^{15} cm^{-3}, which are in agreement with the data in the literature for CdTe devices. The depth profiles for all the devices from both *C-V* and *DLCP* measurements shows similar `*U*` shaped behaviour, except the CST/CdTe device which didn`t have Te at the back. The differences in the depth profiles from both measurements might be due to the presence of both N1 and N2 defects and high defect density, which is affecting the measurements.

The MZO/CST/CdTe devices in Chapter 6 showed metastabilities in the *J-V* characteristics following transport between two laboratories, CSU (US) and CREST (UK). The *J-V* characteristics upon receipt in Loughborough and before any before any preconditioning have shown an `*S*` shaped behaviour, with significant current loss in forward bias and is removed after preconditioning. Annealing the devices did not show a significant improvement in the *J-V* characteristics. However, the longer

light soaking resulted in a significant recovery of the device performance. Additionally, the depth profiles before preconditioning showed an unusual double minima, and the second minima towards the back of the device became less pronounced after preconditioning. From the $\boldsymbol{V_{oc}(T)}$ analysis and admittance spectroscopy, recombination centres and defect levels are found located at the MZO/absorber interface with shallow defects for before and after preconditioning. These defects can be one of the reasons for the observed metastable behaviours. Despite all the preconditioning attempts, storing the device in the dark for approximately 3 days appears to reverse the PV parameters. The MZO films on a bare glass were studied to investigate the effect of preconditioning, light soaking, annealing and $CdCl_2$ treatment on the conductivity and Hall effect measurements using PDL Hall effect system. The MZO films which were either annealed, light soaked or preconditioned have shown no significant changes in conductivity and found to be too resistive for the Hall effect measurements. However, after $CdCl_2$ treatment in nitrogen under vacuum followed by light soaking, films showed an improvement in *I-V* response. Although the signal was improved, it was still not a linear for Hall effect measurements in order to extract reliable results. In addition, Ga doped MZO films were studied in a similar way to MZO films. The GMZO showed a significant improvement in conductivity and Hall signal. However, a gradual decrease in Hall signal during the measurements was observed over time after films were light soaked. Although there`s an improvement in electronic properties, films still exhibit metastability and degradation over a period of time. This raises a big concern as a 25-year warranty is offered with most of the PV modules and a more stable transparent buffer layer might be required.

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